A class-d audio amplifier

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Publication date:
2018

Document Version
Publisher's PDF, also known as Version of record

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 November 2018 (22.11.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/211085 A1

(51) International Patent Classification:
H03F 1/32 (2006.01) *H03F 3/217* (2006.01)
H03F 3/185 (2006.01)

(21) International Application Number:
PCT/EP2018/063132

(22) International Filing Date:
18 May 2018 (18.05.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
17172028.7 19 May 2017 (19.05.2017) EP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: A CLASS-D AUDIO AMPLIFIER

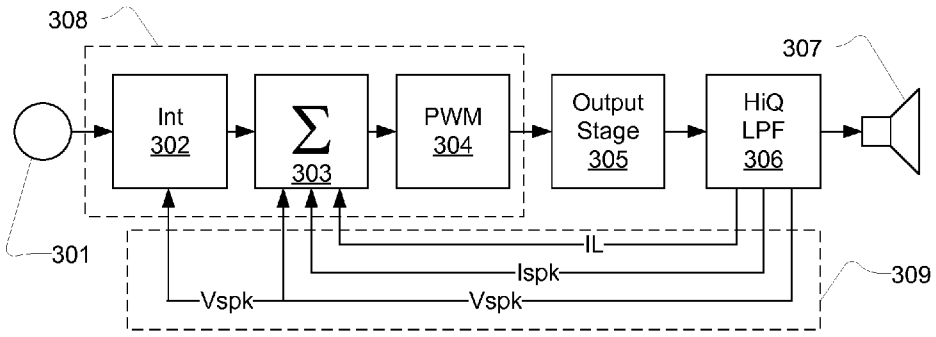

Fig. 3

(57) Abstract: Aclass-D amplifier with an amplifier input and an amplifier output, comprising: an input stage (308) with a self-oscillating pulse-width modulator (304) configured to receive an analog input signal via the amplifier input and to output a digital signal; an output stage (305) configured with semiconductor devices to amplify the digital signal; an output filter (306), configured as a low-pass, high Q filter, coupled between the output stage and the amplifier output; and a feedback circuit (309) coupled to the output filter (306) and to the input stage (308). The feedback circuit (309) is coupled at the output filter (306) to measure a set of states comprising at least two of: current (IL) through the output filter inductor, output current (Ispk) and output voltage (Vspk); and the feedback circuit (309) and the input stage (308) are operatively coupled as a controller configured to control all of the states in the set of states while operatively suppressing a frequency peak at a resonance frequency of the output filter.

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A class-D audio amplifier

Class-D amplifiers, which are based on a switching principle, have become a common choice for audio applications. This is due to the superior efficiency these amplifiers offer compared to other traditional linear amplifiers, such as class-B amplifiers. Class-D amplifiers may reach efficiency levels close to 90%, which allow much more compact implementation than traditional linear amplifiers. In general, a class-D audio amplifier comprises a modulator, a power stage, and an output filter.

In terms of linearity, class-D amplifiers have shown great performance with total harmonic distortion as low as 0.001%. The class-D power amplifier operates by modulating an input audio signal into a high frequency discrete signal which drives an output stage. The output stage drives a load, such as a loudspeaker, via an output filter that suppresses the high frequency passes the audio signal.

The modulation of the audio signal is one of the primary sources of distortion due to the non-linearities in the modulation. Another source of distortion is the output stage. The output stage is connected directly to the supply voltage which results in disturbances in the supply voltage being reflected in the audio. To prevent these disturbances and non-linearities from introducing excessive distortion and noise to the amplified audio signal, the principals of feedback and control theory have been utilized to correct and suppress the unwanted behaviours of the class-D amplifier.

Conventional modulators use pulse width modulation (PWM) where the audio signal is modulated with a fixed high frequency carrier waveform. Typically this waveform will have a triangle or saw-tooth shape. Normally the modulation is performed by comparing the audio input with the carrier which generates a pulse train at a given frequency with varying pulse lengths. The length or on-time of the pulses are also known as the duty cycle, D, of the PWM signal.

The output stage is where the amplification takes place and it consists of semiconductor devices which are switched on and off using the PWM signal. This means that the output stage amplifies the PWM signal. The most common type semiconductor device for switch-mode power applications is the Metal Oxide Field Effect Transistor (MOSFET). The output stage is typically using a buck topology. This topology can be realized either in a half- or full-bridge configuration. The half bridge requires a dual voltage supply while the full bridge only requires a single supply. The component count in the full bridge is twice the component count in the half bridge. The full bridge configuration is commonly referred to as Bridge Tied Load (BTL).

The output filter is formed by a filter inductor, a filter capacitance, and the load impedance – which can be simplified as a purely resistive load. The output filter can in this simplified model be considered a second order low pass filter with a cut-off frequency also denoted a resonance frequency. Typically the cut-off frequency is placed one decade lower than the switching frequency. The main purpose of the filter is to remove the switching transient from the amplified audio signal. This ensures that the dissipated energy in the load is mainly coming from the audio source. Moreover it is beneficial for EMI reasons. The filter should have a flat frequency response in the audio bandwidth, i.e. 20 Hz to 20 kHz, while attenuating with 40 dB/decade above its' cut-off frequency. Moreover the filter will have a quality factor, Q, which determines how much the filter is dampened at its resonance.

Switching losses in the semiconductor devices in the output stage are among the most destructive losses as they can be of significant magnitude even at low power and thus increase the temperature of the semiconductor devices eventually destroying them if the temperature becomes too high. Conventionally, switching losses are difficult to minimize since they relate to the configuration of the semiconductor devices.

Dominating losses can be categorized as:

1) Gate losses, which are generated by charging and discharging the gate capacitances, Cgd and Cgs, of a switching device.
2) Conduction losses, which are generated when the switching device is in its' on state.
3) Switching losses, which occur while a switching device switches from an on-state to an off-state and vice versa.
4) Reverse conduction losses occur in the situation where the body diode in the switching device starts or continue conducting the instantaneous inductor current during the dead time period.
5) Filter losses, which are mainly due to the filter inductance in the output filter. These filter losses can be separated into wire losses and inductor core losses. The inductor core losses relate to the core material and the magnetic flux, B, in it.

The total losses are a sum of the above losses. Class-D amplifiers are usually designed for maximum output power, whereby the conduction losses, the switching losses, and the filter losses normally are the dominant losses. Generally, the losses occur as heat dissipation.

The majority of class-D power amplifiers have been using the principals of classical control due to its straight forward theory and the ease of implementing it in single-input, single-output systems. However, limitations in the theory often result in the control solution being only sub-optimal.

RELATED PRIOR ART

US 6,249,182 (assigned on its face to Intersil Corp.) describes a class-D amplifier with a high-Q low-pass filter which removes the resonance peak. The class-D amplifier comprises a low-pass, high-Q output filter, a pulse width modulator and a feedback compensation circuit. The pulse width modulator includes an integrator with feedback from the output of the amplifier and a comparator coupled to the output of the integrator for converting an input analogue audio signal into a digital audio signal and for amplifying said digital

audio signal. The low-pass, high-Q output filter is coupled between the output of the pulse width modulator and the load impedance for converting the amplified digital signal into an output amplified analogue audio signal. The feedback compensation circuit is coupled between the output of the low pass filter and the integrator for reducing the Q of the output filter.

The low-pass, high-Q output filter serves to keep the transfer function of the class-D amplifier independent of load impedance, but comes at unacceptable costs of creating a peak at the resonance frequency in the transfer function of the class-D amplifier. The feedback compensation circuit implements a filter that places a pole-zero combination in the transfer function of feedback loop of the class-D amplifier to compensate for the high Q output filter creating a transfer function of the class-D amplifier which has a flat frequency response at least in an audio band.

However, there remain unsolved problems in terms of enhancing performance of the class-D amplifier. The feedback compensation circuit provides only a poor reduction of audible distortion and lack of stability of the class-D amplifier may be an issue. Further, problems related to heat losses of the class-D amplifier remain unsolved.

SUMMARY

There is provided a class-D amplifier with an amplifier input and an amplifier output, comprising: an input stage with a self-oscillating pulse-width modulator configured to receive an analog input signal via the amplifier input and to output a digital signal; an output stage configured with semiconductor devices arranged in a configuration comprising a half-bridge to amplify the digital signal; wherein the semiconductor devices in the half-bridge are operated to have a dead time; an output filter, configured as a low-pass, high Q filter, coupled between the output stage and the amplifier output; and a feedback circuit coupled to the output filter and to the input stage; wherein the feedback circuit is coupled at the output filter to measure a set of states comprising all

of: current through the output filter inductor and output voltage; wherein the class-D amplifier is configured to perform Zero Voltage Switching (ZVS) or Reduced Voltage Switching (RVS) at least at duty-cycles in the range of 30 to 70%; and wherein the feedback circuit and the input stage are operatively coupled as a controller configured to control all of the states in the set of states while operatively suppressing a frequency peak at a resonance frequency of the output filter.

Thereby switching losses, conventionally resulting in heat dissipation in the semiconductor devices of the output stage, can be shifted to filter losses resulting in heat dissipation in the output filter, in the inductor thereof, rather than in the semiconductor devices. This has one or more of the advantages that heat sinks attached to the semiconductor devices may be dispensed with or reduced in size and that more output power can be delivered via the output stage. The heat dissipation shifted to the output filter is less of a problem since conventionally the inductor of an output filter is much larger than the semiconductor die of a semiconductor device and hence has a greater heat capacity which makes it able to withstand larger losses without damaging the inductor. When heat sinks are reduced in size or completely dispensed with, manufacturing costs can be lowered and the class-D amplifier can be reduced in size.

The class-D amplifier can be configured to perform Reduced Voltage Switching (RVS) or Zero Voltage Switching (ZVS) when the parasitic drain-source capacitance of the semiconductor devices in the output stage is partially (RVS) or completely (ZVS) charged/discharged by the inductor current during the dead time period. In some aspects the class-D amplifier is configured to perform Zero Voltage Switching or Reduced Voltage Switching at least at duty-cycles in the range of 15 to 85% or in the range of 10 to 90%.

In a comparative test, semiconductor components in the output stage of a class-D amplifier configured to control all of the states above operated at

temperatures in the range of 55.5 to 56.7°C compared to temperatures in the range of 93.0 to 98.9°C for a class-D amplifier

Each of the states, comprising current (IL) through the output filter inductor, output current (Ispk) and output voltage (Vspk), may be measured at the output filter by a sensing circuit and a respective signal, proportional to the current through the output filter inductor, output current and output voltage, may be supplied, via respective feedback paths, to the input stage or a circuit integrated therewith to act as a controller controlling all of the states. The controller may be implemented in this way by means of analogue circuitry i.e. as an analogue controller.

The controller may be configured based on modelling the class-D amplifier as a state-space model (cf. fig. 1) with at least the above mentioned two states, full controllability of all of the states and optionally an integration term. Controllability is ensured e.g. when the class-D amplifier is implemented in accordance with a state-space model with a controllability matrix with a full rank – representing that all states are controllable. The class-D amplifier in accordance with the state-space model may implement the integration term by means of an integrator coupled in a forward path of the input stage. The forward path couples the input signal to the output stage. The integrator corrects stationary errors and improves tracking such that the amplifier maintains proportionality between an input voltage signal and an output voltage signal across the load and prevents clipping while the input signal is in a non-clipping region. The controller may be configured as a Linear Quadratic Regulator (LQR) which can be configured by conventional methods. The Linear Quadratic Regulator may be configured using so-called penalty matrixes to emphasize performance of specific states and control signals (measured states). The controller may be configured as a static controller at least in a predefined audio band such as within an audio band from 20Hz to 20KHz or within a sub-band thereof e.g. from 200Hz to 4KHz or e.g. from 20Hz to 200Hz. A static controller may have a transfer function void of poles and

zeroes within the audio band or a sub-band thereof. In some embodiments the static controller is an analogue controller. An analogue, static controller may be implemented using simple gain stages and/or resistors coupled in the feedback path. The analogue, static controller may comprise a feedback loop enclosed by a dynamic controller e.g. comprising an integrator e.g. arranged in a forward path to the class D amplifier e.g. for the purpose of reducing distortion. Without departing therefrom, an analogue, static controller may comprise “noise decoupling capacitors” which act to decouple noise in a frequency band above the audio band as it is known in the art.

A first penalty matrix may be designed to heavily penalize integration. This will move the pole of the integrator to the left in the s-plane and make it settle somewhere close to the poles of the 2^{nd} order filter, thus making the time constant of the integrator about the same as the output filters. It is thereby expected that the Linear Quadratic Regulator will further increase the damping of the output filter such that oscillations are reduced. These pole movements generate a growth in the control signal, which is limited by the supply voltage. Hence, there is a risk that the control signal is clipped – causing the class-D amplifier to act as an open-loop amplifier, which is undesired. To avoid this, a second penalty matrix is designed (by large matrix values) to emphasize the size of the control signal, thereby effectively reducing the control signal in the class-D amplifier in accordance with the state-space model. For the sake of completeness it is mentioned that the parameters, constant gains, for the controller can be estimated by solving the well-known Riccati equation. In accordance therewith, the controller operatively suppresses the frequency peak at the resonance frequency of the high-Q output filter.

The class-D amplifier may be couple to receive an input signal from an input source, such as an audio source, via its amplifier input. At the amplifier input, the input signal is an analogue input signal. The class-D amplifier may be configured with a digital-to-analogue converter to enable reception of a digital

input signal. The class-D amplifier may be coupled to a load, such as a loudspeaker, to supply an output signal, via its amplifier output, thereto.

The class-D amplifier may be implemented in discrete components on a circuit board to deliver output power in the range of a few Watts to several hundreds of Watts e.g. to thousand Watts or more. The class-D amplifier, except or including one or both of an inductor and capacitor of the output filter, may be implemented on a semiconductor die, such as on a single semiconductor die.

In some aspects the output filter is a second order filter with an inductor coupled in series with a load and a capacitor coupled in parallel with the load. In some aspects the output filter is a third order filter or a filter of a higher order, such as a fourth order filter. The inductor may have ferrite core or an air core or another type of core. The high Q of the output filter may be larger than about 2, larger than about 2.4, larger than about 3, larger than about 3.5, larger than about 4 or larger than about 8. The high Q of the output filter may be in the range between 2 and 10, e.g. between 4 and 10.

In some aspects the output stage is configured as a half-bridge or as a full H-bridge. In some aspects each side of the full H-bridge comprises multiple half-bridges coupled in parallel. A semiconductor device comprises a source terminal, a drain terminal and a gate terminal. A half-bridged comprises a pair of semiconductor devices, with a first semiconductor device coupled in series with a second semiconductor device between a positive power supply terminal and a negative power supply terminal. The first semiconductor device and the second semiconductor device are interconnected at a circuit node at their drain terminals. The output filter is coupled between the load and the circuit node at the drain terminals.

The semiconductor devices are driven by the input stage, such as by an output of the self-oscillating pulse-width modulator, via their gate terminals. The semiconductor devices in a pair of semiconductor devices are driven out-of-phase to avoid periods of short-circuiting the power supply. In some aspects a

delay element, such as an inverter gate, is coupled between the output of the self-oscillating pulse-width modulator and a semiconductor device to deliberately introduce a delay between the first semiconductor device turning 'off' and the second semiconductor device turning 'on'. Thereby, short-circuiting the power supply can be avoided.

In some embodiments the set of states comprises output current. The output current flows from the output of the class-D amplifier and through a load, such as a loudspeaker. When the set of states comprises the output current, the class-D amplifier has improved linearity.

In some embodiments the feedback circuit comprises: a measurement circuit outputting respective measurement signals proportional to one or more of: current through the output filter inductor, output current, and output voltage; and a gain element applying a respective gain to the respective measurement signals to output respective feedback signals to the input stage. Thereby the controller can act on signals proportional to the respective measurement signals which accurately represent the states the controller are controlling.

In some embodiments the feedback circuit has a substantially flat gain across frequencies in a frequency range between 20 Hz and 10 KHz or between 20 Hz and 20 KHz or between 20 Hz and an upper frequency; wherein the upper frequency is located approximately at the resonance frequency of the output filter or an upper -3dB cut-off frequency of the class-D amplifier. Thereby the controller can act on signals proportional to the respective measurement signals which accurately represent the states the controller are controlling. The feedback circuit may comprise filters configured to suppress noise above or below the claimed frequency ranges.

In some embodiments the class-D amplifier is configured with: a reactive ripple current through the output filter inductor which is larger than a continuous output current; and soft switching factor in the range of 20% to 100%. This minimizes switching losses which occur in the semiconductor devices. Instead,

at least to some degree, losses are shifted to occur in the output filter inductor. The reactive ripple current through the output filter inductor may be deliberately larger, such as significantly larger, than a continuous output current. By deliberately larger is understood larger than, such as significantly larger, during normal operating conditions of the class-D amplifier.

As discussed above, to reduce the need for bulky heat sinks on Class-D audio amplifiers it is desired to deliberately design and dimension power losses in the Class-D amplifier so that the total power loss do not generate critical temperature rise in any component of the amplifier. Since, conventionally, the output filter of a Class-D audio amplifier is of larger physical size than the semiconductor devices, or at least their semiconductor dies, it makes sense to dissipate more energy in the inductors than in the semiconductor devices so that the component temperature gets more evenly distributed. In some embodiments this is achieved by configuring the class-D amplifier to charge and/or discharge the drain-source capacitance, C_{ds}, of the semiconductor devices with the reactive ripple current during the dead time period prior to a switching event. The amount of soft switching experienced by a power stage switch can be expressed as the soft switching factor, V_P. For semiconductor devices in a Class-D audio amplifier the soft switching factor can be written as:

$$V_P = \frac{V_{Cds}}{V_S} = \frac{t_{dt} i_L}{2 C_{ds} V_s}$$

Where V_{Cds} is the drain-source voltage of the switching device, V_S is the supply voltage and i_L is the inductor current in the switching event, i.e. Δi_L, , t_{dt} is the dead time period (where both semiconductor devices in the half bridge is off). 100% soft switching factor equals Zero Voltage Switching (ZVS) meaning no switching losses. 0% soft switching equals full Hard Switching meaning full switching losses. Soft switching factors between 1% and 99% equals Reduced Voltage Switching (RVS) meaning that switching losses are reduced. However if the soft switching factor is too low, e.g. below about 15 or 20%, the improvement in the switching capabilities may be negligible compared to

conventional Hard Switching. The terminology used herein refers mainly to semiconductor devices of the MOSFET type however the semiconductor devices may also be of FET type, BJT type or another type suitable to be operated as a switching device, mutatis mutandis.

Opposed to power supplies, a Class-D audio amplifier has a dynamic output voltage as it is a music signal. Therefore the output stage will undergo many different duty cycle conditions during normal operation. To ensure good soft switching capabilities during normal operation of a class-D amplifier:

1. The reactive ripple current through the output filter inductor is larger than a continuous output current;
2. The output stage has a dead time period e.g. in the range of 5 to 20 nanoseconds, e.g. 5 to 40 nanoseconds, 10 to 20 nanoseconds;
3. The soft switching factor is in the range 20% to 100%, and
4. The Q of the output filter is larger than 2.5, or 3 or 3.5.

Points 1, 2 and 3 may be satisfied at least for duty cycles of 30% to 70% of the output stage at least in some embodiments.

In some embodiments the reactive ripple current in the output filter inductor is larger than the continuous output current at least within a range of duty-cycles from 30% to 70% duty-cycle. The duty-cycle refers to the duty-cycle of a digital signal output from the self-oscillating pulse-width modulator. In some aspects the reactive ripple current in the output filter inductor is larger than the continuous output current at least within a range of duty-cycles from 15 to 85% or 10 to 90%.

In some embodiments the class-D amplifier comprises an integrator coupled in a forward path between the amplifier input and the self-oscillating pulse-width modulator; wherein at least a first path of the feedback circuit is coupled to an input of the integrator and to a first circuit measuring the output voltage. The first circuit, measuring the output voltage, outputs a signal proportional with the output voltage to the controller implemented by one or both of the

feedback circuit and the input stage. In some aspects, e.g. where the output stage comprises a full H-bridge, the first circuit is configured as a difference amplifier sensing the voltage at each side of a two-port load, such as a loudspeaker.

In some embodiments the class-D amplifier comprises a summing circuit coupled in a forward path between the amplifier input and the self-oscillating pulse-width modulator; wherein at least a second path of the feedback circuit is coupled to an input of the summing circuit and to a second circuit measuring the current through the output filter inductor. The second circuit, measuring the current through the output filter inductor, outputs a signal proportional with the current through the output filter inductor to the controller implemented by one or both of the feedback circuit and the input stage. The second circuit may comprise a sensing resistor coupled in series with the output filter inductor and a difference amplifier sensing the voltage at each side of the sensing resistor.

In some embodiments at least a third path of the feedback circuit is coupled to an input of the summing circuit and to a second circuit sensing the output current. The third circuit, measuring the output current, outputs a signal proportional with the output current to the controller implemented by one or both of the feedback circuit and the input stage. The third circuit may comprise a sensing resistor coupled in series with the output filter inductor and a difference amplifier sensing the voltage at each side of the sensing resistor.

In some embodiments the self-oscillating pulse-width modulator is configured as an astable integrating modulator or a hysteresis offset modulator. Thereby the class-D audio amplifier achieves good audio performance with very low Total Harmonic Distortion, THD. Opposed to fixed frequency pulse width modulators, the self-oscillating pulse-width modulator operates with a modulator frequency that varies with the input signal.

In some embodiments the class-D amplifier has a step response with a peak of the output current which is limited to three times the current of a settled

portion of the step response. In response to a step type input signal, the output current exhibits a conventional step response, which has some ringing towards the beginning of the step and which decays to a settled level. The peak refers to a maximum of the ringing. In some aspects the output current is limited to 2.4 times or 2.2 times the current of a settled portion of the step response.

In some embodiments the controller is implemented as an analogue controller.

There is also provided a semiconductor die comprising a class-D amplifier as set out above, excluding the output filter or an inductor thereof. Since switching losses are significantly reduced close integration of the semiconductor based output stage and input stage is possible. In some aspects the semiconductor die is integrated in a semiconductor package, such as in a plastics package. However, the output filter or an inductor thereof may require implementation as a discrete component, such as as a copper wire based coil.

In some embodiments there is provided a class-D amplifier with an amplifier input and an amplifier output, comprising: an input stage with a self-oscillating pulse-width modulator configured to receive an analog input signal via the amplifier input and to output a digital signal; an output stage configured with semiconductor devices to amplify the digital signal; an output filter, configured as a low-pass, high Q filter, coupled between the output stage and the amplifier output; and a feedback circuit coupled to the output filter and to the input stage; wherein the feedback circuit and the input stage is configured for state-space control of the class-D amplifer; wherein at least two states, e.g. three states are controlled state-space control.

Here and in the following, the terms ‘class-D amplifier’ and ‘class-D audio amplifier’ are intended to comprise any circuit and/or device suitably adapted to perform the functions described herein. In particular, the above terms

comprise electronic circuits, such as electronic circuits which are integrated on fully or in part on a printed circuit board, general purpose or proprietary programmable microprocessors, Digital Signal Processors (DSP), Application Specific Integrated Circuits (ASIC), Programmable Logic Arrays (PLA), Field Programmable Gate Arrays (FPGA), special purpose electronic circuits, etc., or a combination thereof.

BRIEF DESCRIPTION OF THE FIGURES

A more detailed description follows below with reference to the drawing, in which:

fig. 1 shows a diagram for a state-space model of a class-D amplifier driving a load;

fig. 2 shows a state-space model of a class-D amplifier with state-space control;

fig. 3 shows a time-domain block-diagram of the class-D amplifier with state-space control;

fig. 4 shows a first output stage and an output filter with sensing components and sensing circuit nodes;

fig. 5 shows a second output stage and an output filter;

fig. 6 shows current sensing amplifiers;

fig. 7 shows an output voltage sensing amplifier;

fig. 8 shows an integrator with a feedback input;

fig. 9 shows a summation amplifier;

fig. 10 shows a self-oscillating pulse-width modulator;

fig. 11 illustrates ripple current over mean current as a function of duty-cycle for different filter Q; and

fig. 12 illustrates temperatures related to heat dissipation at different areas of a circuit board carrying a class-D amplifier with and without state-space control.

DETAILED DESCRIPTION

In the below the class-D amplifier is modelled as a 2nd order system with a state-space controller with three states. An integrator is coupled in a forward path of the class-D amplifier inside an outer feedback loop. However, it should be noted that the integrator may be dispensed with. Also, without departing from the scope of the present invention, the class-D amplifier may be modelled as a third, fourth or higher order system. Correspondingly, the state-space controller may have a number of states equal to or greater than the order of system as it is modelled.

In general it is desired to model all the internal states of the class-D amplifier since it will provide the most accurate description of the system. However, when designing an analogue full state controller only the internal states that are directly measurable are of interest. This is because the full state controller must have a feedback path for every state which makes it crucial that the state is measureable. In embodiments wherein the class-D amplifier is configured to drive a load in the form of a speaker (i.e. a loudspeaker), the measurable states in the class-D amplifier may comprise: The speaker voltage (V_{out}), the speaker current (I_{out}) and the inductor current (I_L), where the output filter comprises an inductor coupled in series with the speaker. The measureable states are represented by a vector x(t), wherein 't' denotes that x(t) is a function of time.

$$x(t) = \begin{bmatrix} I_L \\ I_{Out} \\ V_{Out} \end{bmatrix}$$

Fig. 1 shows a diagram for a state-space model of a class-D amplifier driving a load. The state-space model is an example of a model accounting for dominating poles and zeros in the transfer function for the class-D amplifier. The state-space model comprises a signal source, 101, generating an input signal, V_{in}, which is input to a gain stage 102, which is modelled as an ideal gain stage with a gain, G. The gain stage 102 supplies a signal proportional to the input signal to a 2nd order output filter which is modelled by an inductor, L_{ind}, 104 with a series resistance, R_{ind}, 103 and by a capacitor, C, 107. The load, in this example a speaker, is modelled as an inductor, L_{spk}, 106 with a series resistance, R_{spk}, 105. For this model the states can be measured as indicated by I_L, V_{out}, and I_{out} as indicated in the fig. 1.

In case the output filter of the amplifier is a 2nd order low pass filter, only two states are needed to describe it, but more states may be used. Correspondingly, the number of states is larger than or equal to the order of the output filter e.g. if the order of the filter is N, then the number of states may be N+1, wherein N is an integer number.

The states are used in a general state-space model known in the art of modern control, wherein:

$$\dot{x}(t) = Ax(t) + Bu(t)$$
$$y(t) = Cx(t) + Du(t)$$

Wherein, the matrixes A and B, when the equations governing the state-space model depicted in fig. 1 are taken into account, becomes:

$$A = \begin{bmatrix} -\frac{R_{ind}}{L_{ind}} & 0 & -\frac{1}{L_{ind}} \\ 0 & -\frac{R_{spk}}{L_{spk}} & \frac{1}{L_{spk}} \\ \frac{1}{C_O} & -\frac{1}{C_O} & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{G}{L_{ind}} \\ 0 \\ 0 \end{bmatrix}$$

wherein the unified gain of the modulator and the power stage of a class-D amplifier is represented by G. The equation below provides an approximate gain through the amplifier based on the voltage amplification and a desired maximum linearized modulation index, M_{lin}.

$$G = \frac{V_{out}}{V_{in}} \cdot M_{lin}$$

The output of the state-space model is selected to be the voltage across the speaker, V_{out}, hence the so-called output matrix, C, and feed-through matrix, D, becomes:

$$C = [0 \quad 0 \quad 1]$$
$$D = 0$$

With this, a linear state-space model of the class-D amplifier is complete.

In one example, a class-D amplifier may have:

Cut-off freq. (fc)	155	KHz
Quality factor (Q)	4.5	
Idle switch freq. (fsw)	1.9	MHz
Modulation index (Mlin)	76	%
Input voltage, pk-pk	2	V
Gain (G)	9.12	V/V

With:

$$A = \begin{bmatrix} -\frac{37m\Omega}{1\mu H} & 0 & -\frac{1}{1\mu H} \\ 0 & -\frac{37\Omega}{1mH} & \frac{1}{1nH} \\ \frac{1}{660nF} & -\frac{1}{660nF} & 0 \end{bmatrix}$$

and

$$B = \begin{bmatrix} \frac{9.12}{1\mu H} \\ 0 \\ 0 \end{bmatrix}$$

And C and D as set out above.

As mentioned herein, the class-D amplifier in accordance with the state-space model may implement the integration term by means of an integrator coupled in a forward path of the input stage. The forward path couples the input signal to the output stage. The integrator corrects stationary errors and improves tracking such that the amplifier maintains proportionality between an input voltage signal and an output voltage signal across the load and prevents clipping while the input signal is in a non-clipping region. This is especially useful when the controller is used in a real class-D amplifier since it counteracts non-linear behaviours. The controller may be configured as a Linear Quadratic Regulator (LQR) which can be configured by conventional methods. The Linear Quadratic Regulator may be configured using so-called penalty matrixes to emphasize performance of specific states and control signals (measured states).

To dimension the integration term, the state-space model needs to be modified. This is because the controller design methods used in modern control only consider the state-space model, resulting in the integration being neglected. To solve this, an integral transform is applied to the state-space model. The matrixes below show the transformation of the state-space model to accommodate the integration term.

$$A_i = \begin{bmatrix} A & 0 \\ -C & 0 \end{bmatrix}, \quad B_i = \begin{bmatrix} B \\ 0 \end{bmatrix}, \quad C_i = [C \quad 0]$$

With this representation, a Linear Quadratic Regulator design approach is applied to the system. The Linear Quadratic Regulator (LQR) is an optimization method used to find the optimal full state controller with time varying gains. However, time varying gains are often not practical nor necessary hence a simplified steady state LQR method has been developed which will be used for the system. This method optimizes the following quadratic performance index, which is given as an example of a performance index; a person skilled in the art may choose another performance index:

$$J(u) = \lim_{t\to\infty} \int_0^t x^T(t) R_1 x(t) + u(t) R_2 u(t) dt$$

Wherein x(t) is the states of the model, u(t) is the control signal to the system, t designates time, and superscript 'T' designates the transpose. R1 and R2 are penalty matrices which are used to emphasize the performance of specific states and control signals. The index J(u) in the equation above is solved numerically for non-linear systems – and is computationally heavy i.e. very time consuming. By using a linearized state-space model the computational effort is reduced and static optimization can be used to find steady state gains for the full state feedback controller. It can be shown that the limiting constant solution P to the performance index can be found by solving the well-known Algebraic Riccati Equation below.

$$0 = A^T P + PA + R_1 - PBR_2^{-1}B^T P$$

From this, the minimum value J_{min} for the performance index *J* can be found to be:

$$J_{min} = \frac{1}{2} x_0^T P_\infty x_0$$

And the constant gains, K_∞, for the full state controller becomes:

$$K_\infty = R_2^{-1} B^T P_\infty$$

For the class-D amplifier it is desired to compensate for any non-linearities as fast as possible and to reduce the damped oscillation on the output. To realize this, the penalty matrix R1 is designed to heavily penalize the integration state. This will move the pole of the integrator to the left in the s-plane and make it settle somewhere close to the poles of the 2nd order filter, thus making the time constant of the integrator about the same as the output filters. Since the damped oscillation limits the movement of the integrator, it is to be expected that the LQR will further increase the damping of the output filter such that the oscillation will be reduced. All these pole movements generate a growth in the control signal which is limited by the supply voltage. It is important that the control signal does not clip since this would result in the system acting as an open-loop system. To avoid this, the penalty matrix R2 is increased to emphasize the size of the control signal thereby reducing it. Examples of penalty matrixes R1 and R2 are shown below:

$$R_1 = \begin{bmatrix} 0.7 & 0 & 0 & 0 \\ 0 & 10^{-3} & 0 & 0 \\ 0 & 0 & 10^{-3} & 0 \\ 0 & 0 & 0 & 10^{11} \end{bmatrix}, \quad R_2 = 30$$

By providing a small penalty to the inductor current, the in-rush current is limited thus eliminating any overshoot at the output. Using the obtained model in and the penalty matrices, the feedback gains are found using the above equations. The resulting gains comprised by the vector K_∞ are shown below. Here it is particularly noticeable that the state, describing the current through the speaker, is of next to no interest for the controller. This is probably because the controller focusses on controlling the voltage across the speaker and since the speaker current is a result of the voltage across the speaker, the current does not matter for the control of the amplifier.

$$K_\infty = [K_{ind\_I} \quad K_{spk\_I} \quad K_{spk\_V} \quad -K_i]$$

$$K_\infty = [0.177 \quad -1.062 \cdot 10^{-5} \quad 0.056 \quad -5.774 \cdot 10^4]$$

In the above, the last gain, K_i is the negative inverse of the time constant of the integrator, thus the time constant becomes:

$$\tau_i = \frac{1}{-K_i} = 1.8982\mu s$$

With the feedback gains and the time constant found, the loop can be closed according to the closed system shown in fig. 2.

Fig. 2 shows a state-space model of a class-D amplifier with state-space control. Please note that in fig. 2 gain elements A, B and C are multidimensional gain elements with a dimensionality in accordance with the dimensionality of state-space matrixes A, B and C in the expressions above (wherein A, B and C may be scalars). Regarding K, K in fig. 2 corresponds to K in the expressions above excluding the last element i.e. for fig. 2:

$$K = [K_{ind\_I} \quad K_{spk\_I} \quad K_{spk\_V}]$$

Thus, for example, gain element 211 has three paths with a respective gain (scalar).

In fig. 2 it is shown that the integration term is included as an integration element 203. The integration element 203 is located in a forward path of the class-D amplifier in series with a gain element 204, with gain Ki, following a summation element 202 which receives an input signal, IN, and subtracts therefrom a feedback signal provided via a gain element 212, with gain 1/G, to provide the resulting difference to the integrator term 203. The gain element 212 receives its input signal from an output designated 'OUT' of the model. An outer feedback loop is thereby provided, implementing the integration term.

Further down the forward path, a summation element 205 receives a signal from the gain element 204 and subtracts therefrom a feedback signal received from a gain element 211, with gain $K = K_\infty$, to provide the resulting difference to a gain element 206 with gain B. Thereby a further feedback loop is provided.

Still further down the forward path, a summation element 207 receives a signal from the gain element 206 and subtracts therefrom a feedback signal received from a gain element 210, with gain A, to provide the resulting difference to an integrator element 208. Thereby a yet further feedback loop is provided. Output from the yet further feedback loop is provided to a gain element 209, with gain C, to the output.

It should be noted that Ki is the gain of the integrator. 1/G is the reciprocal of G, which is the gain of the class-D amplifier.

Using the state-space model, a linear full state integral controller can be designed, using the LQR method, and verified on a linear and non-linear model. Finally, the controller can be implemented on a class-D amplifier.

Total Harmonic Distortion, THD, measurements showed up to 10 time improvements compared to an amplifier without the controller. This proved that the principals of modern control achieve a very good performance even when the output filter has a resonance peak.

Fig. 3 shows a block-diagram of the class-D amplifier with state-space control. The block-diagram comprises elements, the details of which are explained in more detail with reference to the following figures.

The block-diagram comprises a signal source 301, an input stage 308, an output stage 305, an output filter 306 in the form of a high-Q low-pass filter, and a load in the form of a speaker 307. The input stage comprises an integrator 302, a summing component 303 and a self-oscillating modulator in the form of a pulse-width modulator, PWM, 304. These elements form part of a forward path of the class-D amplifier.

The integrator 302 and the summing component 303 are coupled to receive a feedback signal, V_{spk}, measured at the output filter 306. The summing component 303 is additionally coupled to receive feedback signals, I_{spk} and I_L, at the output filter 306.

Fig. 4 shows a first output stage and an output filter with sensing components and sensing circuit nodes. In this embodiment, the output stage is configured as an H-bridge with semiconductor devices Q1 and Q2 in a left hand side of the H-bridge and semiconductor devices Q3 and Q4 in a right hand side of the H-bridge. The semiconductor devices Q1, Q2, Q3 and Q4 may be of the MOSFET type, FET type, BJT type or another type suitable to be operated as a switching device. The semiconductor devices Q1, Q2, Q3 and Q4 are controlled by respective control signals PWM1, PWM2, PWM3, and PWM4 where PWM1 and PWM4 are mutually in-phase control signals, which are in opposite phase with PWM3 and PWM2, which are mutually in-phase control signals. In this way short circuiting of the supply voltage through Q1 and Q2 and through Q3 and Q4 is avoided. The control signals have a square shape. The semiconductor devices Q1, Q2, Q3 and Q4 may have an 'on-state' and an 'off-state' selectively controlled by the control signals. In some time intervals, semiconductor devices Q3 and Q2 are in their on-state, while Q1 and Q4 are in their off-state, resulting in current flowing through a load, such as speaker 403, from a supply voltage terminal, Vs, to a ground terminal, Vgnd, via Q3 and via Q2. In other time intervals, semiconductor devices Q1 and Q4 are in their on-state, while Q2 and Q3 are in their off-state, resulting in current flowing through the load in the opposite direction, from the supply voltage terminal, Vs, to the ground terminal, Vgnd, via Q1 and via Q4. The ratio between the duration of 'on-period' to the duration of 'off-period' defines the duty-cycle.

The load 403 is arranged in the path between the left hand side of the H-bridge and the right hand side of the H-bridge. The path comprises a series connection of a first output filter inductor, L1f; a first sensing resistor, R1s; the speaker, Spk; a second sensing resistor, R2s; and a second output filter inductor, L2f. The sensing resistors have relative small Ohmic impedance compared to the Ohmic impedance of the speaker.

The path also comprises a capacitor, Cf, coupled in parallel with the speaker, Spk, and the second sensing resistor, R2s.

As shown, sensing nodes are named ILs, VOA, VOB and IOs. The sensing nodes are coupled to sensing circuits as described in more detail below.

Fig. 5 shows a second output stage and an output filter. The second output stage is configured as a half-bridge, comprising semiconductor devices Q1 and Q2 as described above. The half-bridge requires a double-sided voltage power supply with a positive voltage supply terminal, Vs, a negative voltage supply terminal, -Vs, and a ground terminal, Vgnd. In this configuration a single output filter inductor, Lf, is coupled between the speaker, Spk and the half-bridge.

Sensing resistors may be coupled in series with the output filter inductor, Lf, and in series with the speaker, Spk, to provide sensing nodes ILs, VOA and IOs. In this embodiment VOB is not needed since the speaker is connected to ground, Vgnd.

Fig. 6 shows current sensing amplifiers. The current sensing amplifier 601 is coupled to the sensing nodes IOs and VOB described above and is configured to output a measurement of the current, Ispk, through the speaker. The current sensing amplifier 602 is coupled to the sensing nodes ILs and VOA described above and is configured to output a measurement of the current, ILf, through the inductor of the output filter.

The current sensing amplifier 601 and the current sensing amplifier 602 are configured as summing amplifiers based on operational amplifiers U1 and U2 as it is known in the art.

Current sensing amplifier 601 comprises resistors R11, R16, R10 and R5. Resistor R5 is coupled to a voltage reference, Vref. The current sensing amplifier 601 provides a voltage output, Ispk, which is proportional to the difference between voltage VOB and IOs, i.e. the voltage drop across the

second sensing resistor R2s, which in turn is proportional to the current through the speaker. Thus, current sensing amplifier 601 outputs a measurement of the current through the speaker.

Current sensing amplifier 602 comprises resistors R22, R23, R21 and R17. Resistor R17 is coupled to a voltage reference, Vref. The current sensing amplifier 602 provides a voltage output, ILf, which is proportional to the difference between voltage VOB and ILs, i.e. the voltage drop across the first sensing resistor R1s, which in turn is proportional to the current through the inductor of the output filter. Thus, current sensing amplifier 602 outputs a measurement of the current through the speaker.

Fig. 7 shows an output voltage sensing amplifier. The output voltage sensing amplifier 701 comprises resistors R8, R9, R7 and R6 and is based on an operational amplifier U3. Resistor R6 is coupled to a voltage reference, Vref. The output voltage sensing amplifier 701 provides a voltage output, Vspk, which is proportional to the difference between voltage VOB and VOA, i.e. the voltage drop across the speaker, Spk. Thus, output voltage sensing amplifier 701 outputs a measurement of the voltage across the speaker.

One or more of: current sensing amplifier 601, current sensing amplifier 602 and output voltage sensing amplifier 701 are comprised by a measurement circuit. The measurement circuit measures a set of states comprising two or more of: current (IL) through the output filter inductor, output current (Ispk) and output voltage (Vspk).

Fig. 8 shows an integrator. The integrator 801 receives an input signal, Vin, via an input terminal of the class-D amplifier. The integrator 801 also receives the feedback signal, Vspk, which may be generated as described above. The output of the integrator is a voltage signal denoted, Ierr. The integrator 801 is this arranged in a forward path of the class-D amplifier and receives a feedback signal. The integrator 801 is based on an operational amplifier U4 and comprises resistors R13 and R12 and capacitors C7 and C8.

In some embodiments the integrator 801 is an implementation of the integrator 302 shown in fig. 3. The integrator 801 subtracts Vspk from Vin and provides the result thereof as its output, Ierr. The integrator improves proportionality between an input signal to the class-D amplifier and an output from the class-D amplifier. However, in some embodiments, the integrator 801 is dispensed with.

Fig. 9 shows a summation amplifier. The summation amplifier 901 is based on an operational amplifier U5 and receives feedback signals, Vspk, Ispk, ILf and forward signal, Ierr, which are summed via resistors R20, R19, R18, R14 and feedback resistor R15 to output a sum signal, Verr. The summation amplifier 901 may also be denoted a state control feedback summation amplifier which sums state control signals Vspk, Ispk and ILf.

The summation amplifier 901 is comprised by the state controller. The summation amplifier 901 has a substantially flat gain across frequencies in a frequency range between 20 Hz and 10 KHz or between 20 Hz and 20 KHz or between 20 Hz and an upper frequency; wherein the upper frequency is located approximately at the resonance frequency of the output filter or an upper -3dB cut-off frequency of the class-D amplifier. In some embodiments the summation amplifier 901 is an implementation of the summing circuit 303 shown in fig. 3.

Fig. 10 shows a self-oscillating pulse-width modulator. The self-oscillating pulse-width modulator 1001 outputs the signals PWM1 and PWM2 which are pulse width modulated signals mutually in opposite phase. From these two signals PWM3 and PWM4 may be generated as it is known in the art. The self-oscillating pulse-width modulator 1001 is based on an operational amplifier U6 and comprises resistors R1, R2, R4 and R5 and capacitor C.

The signal Verr, which is an analogue signal, is received from the summation amplifier 901 and in response to the amplitude of the signal, Verr, pulse width modulated signals PWM1 and PWM2 are output. PWM2 may be generated

from PWM1. In some embodiments positively going flanks of PWM2 are slightly delayed, e.g. by one or more semiconductor elements, relative to negatively going flanks of PWM1 to ensure that short circuiting through Q1 and Q2 and through Q3 and Q4 is avoided.

Fig. 11 illustrates ripple current over mean current as a function of duty-cycle. To facilitate Zero Voltage Switching (ZVS) or Reduced Voltage Switching (RVS) for a given duty cycle span the reactive ripple current in the output filter inductor must be dimensioned so that the ripple current is larger than continuous output current for all duty cycles within that span, that is $\Delta i > I_{out}$.

It is illustrated how the ZVS/RVS region increases with higher quality factors of the output filter and a self-oscillating modulation scheme as it shows the ratio between the ripple-current and the continuous output-current vs. duty cycle for various quality factors, Q-factors, of the output filter for both conventional fixed frequency- and self-oscillating-modulators.

Fig. 12 illustrates temperatures related to heat dissipation at different areas of a circuit board carrying a class-D amplifier. The circuit board 1201 carries among other components of the class-D amplifier four semiconductor devices configured in an H-bridge in the output stage; the four semiconductor devices are arranged within a semiconductor region 1202. The four semiconductor devices are arranged e.g. as shown in the circuit shown in fig. 4. The circuit board 1201 also carries two inductor coils arranged within an inductor coil region 1203. The two inductor coils are arranged e.g. as shown in the circuit shown in fig. 4.

Temperature measurements were conducted in connection with a class-D amplifier arranged on a circuit board as described above in a first situation without state-space control as described above and in a second situation with state-space control as described above. Six temperatures at points 1 through 6 were measured in the first situation and six temperatures were measured in the second situation:

Measurement point	With or without state-space control, $Q \sim 0.7$ [°C]	With state-space control $Q \gg 0.7$ [°C]
1	93.0	55.5
2	97.3	56.7
3	98.9	56.0
4	98.2	55.9
5	51.6	64.2
6	51.6	64.3

Thus, temperatures at the semiconductor region are lowered whereas temperatures at the conductor region are increased.

In some embodiments there is provided a class-D amplifier with an amplifier input and an amplifier output, comprising: an input stage with a self-oscillating pulse-width modulator configured to receive an analog input signal via the amplifier input and to output a digital signal; an output stage configured with semiconductor devices to amplify the digital signal; an output filter, configured as a low-pass, high Q filter, coupled between the output stage and the amplifier output; and a feedback circuit coupled to the output filter and to the input stage; wherein the feedback circuit is coupled at the output filter to measure a set of states comprising all of: current through the output filter inductor and output voltage; and wherein the feedback circuit and the input stage are operatively coupled as a controller configured to control all of the states in the set of states while operatively suppressing a frequency peak at a resonance frequency of the output filter.

In some embodiments the class-D amplifier is configured to perform Zero Voltage Switching (ZVS) or Reduced Voltage Switching (RVS) at least at duty-cycles in the range of 30 to 70%.

CLAIMS

1. A class-D amplifier with an amplifier input and an amplifier output, comprising:

an input stage (308) with a self-oscillating pulse-width modulator (304) configured to receive an analog input signal via the amplifier input and to output a digital signal;

an output stage (305) configured with semiconductor devices arranged in a configuration comprising a half-bridge to amplify the digital signal; wherein the semiconductor devices in the half-bridge are operated to have a dead time;

an output filter (306), configured as a low-pass, high Q filter, coupled between the output stage and the amplifier output; and

a feedback circuit (309) coupled to the output filter (306) and to the input stage (308);

CHARACTERIZED in that

the feedback circuit (309) is coupled at the output filter (306) to measure a set of states comprising all of: current (IL) through the output filter inductor, and output voltage (Vspk);

the class-D amplifier is configured to perform Zero Voltage Switching (ZVS) or Reduced Voltage Switching (RVS) partially or completely charging/discharging a drain-source capacitance of the semiconductor devices by the inductor current during the dead time period of the output stage at least at duty-cycles in the range of 30 to 70%; and

the feedback circuit (309) and the input stage (308) are operatively coupled as a controller configured to control all of the states in the set of states while operatively suppressing a frequency peak at a resonance frequency of the output filter.

2. A class-D amplifier according to claim 1, wherein the set of states comprises output current (Ispk).

3. A class-D amplifier according to any of the above claims wherein the feedback circuit comprises:

a measurement circuit outputting respective measurement signals proportional to one or more of: current (IL) through the output filter inductor, output current (Ispk), and output voltage (Vspk); and

a gain element (211) applying a respective gain to the respective measurement signals to output respective feedback signals to the input stage (308).

4. A class-D amplifier according to any of the above claims wherein the feedback circuit has a substantially flat gain across frequencies in a frequency range between 20 Hz and 10 KHz or between 20 Hz and 20 KHz or between 20 Hz and an upper frequency; wherein the upper frequency is located approximately at the resonance frequency of the output filter or an upper -3dB cut-off frequency of the class-D amplifier.

5. A class-D amplifier according to any of the above claims, configured with:

- a reactive ripple current through the output filter inductor which is larger than a continuous output current; and

- a soft switching factor in the range of 20% to 100%.

6. A class-D amplifier according to any of the above claims, wherein the reactive ripple current in the output filter inductor is larger than the continuous output current at least within a range of duty-cycles from 30% to 70% duty-cycle.

7. A class-D amplifier according to any of the above claims, comprising an integrator (302) coupled in a forward path between the amplifier input and the self-oscillating pulse-width modulator (304); wherein at least a first path of the feedback circuit is coupled to an input of the integrator (302) and to a first circuit (701) measuring the output voltage (Vspk).

8. A class-D amplifier according to any of the above claims, comprising a summing circuit (303) coupled in a forward path between the amplifier input and the self-oscillating pulse-width modulator (304); wherein at least a second path of the feedback circuit is coupled to an input of the summing circuit (303) and to a second circuit (602) measuring the current through the output filter inductor.

9. A class-D amplifier according to claim 8, wherein at least a third path of the feedback circuit is coupled to an input of the summing circuit (303) and to a second circuit (601) sensing the output current.

10. A class-D amplifier according to any of the above claims, wherein the self-oscillating pulse-width modulator is configured as an astable integrating modulator or a hysteresis offset modulator.

11. A class-D amplifier according to any of the above claims, wherein the class-D amplifier has a step response with a peak of the output current which is limited to 3 times the current of a settled portion of the step response.

12. A class-D amplifier according to any of the above claims, wherein the controller is implemented as an analogue controller.

13. A semiconductor die comprising a class-D amplifier according to any of the above claims, excluding the output filter or an inductor thereof.

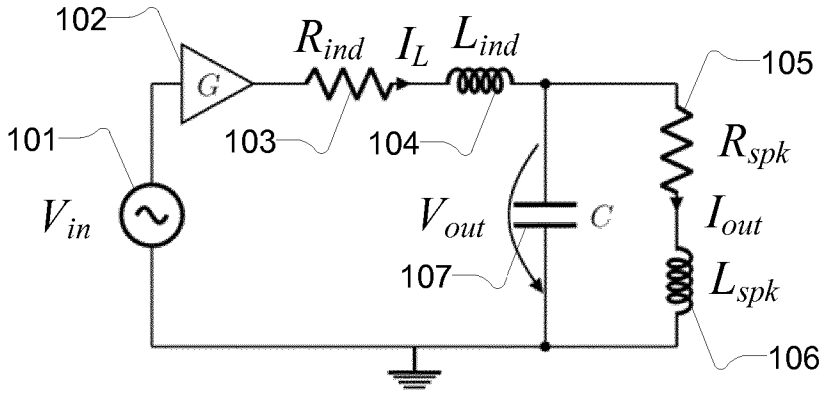


Fig. 1

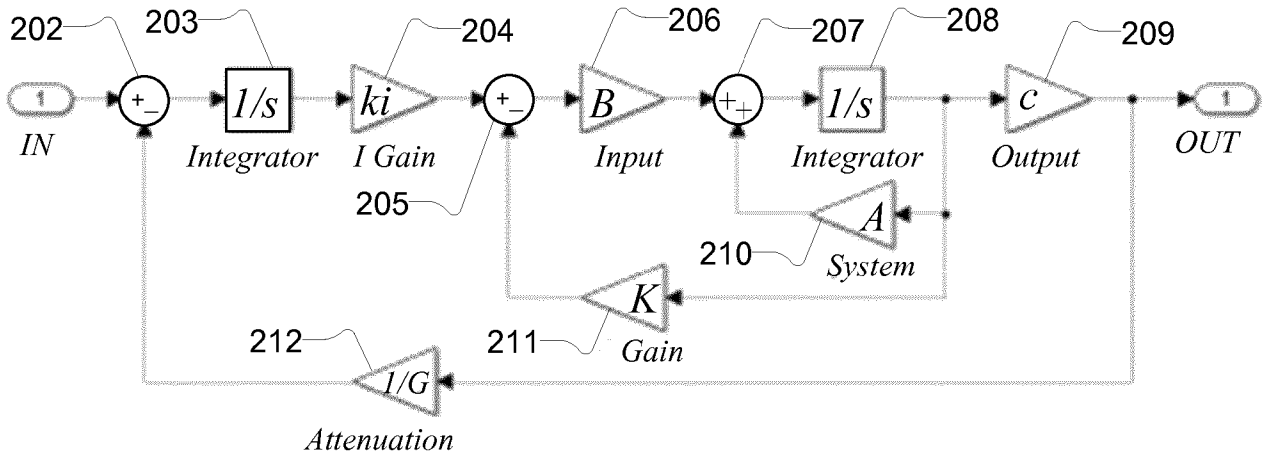


Fig. 2

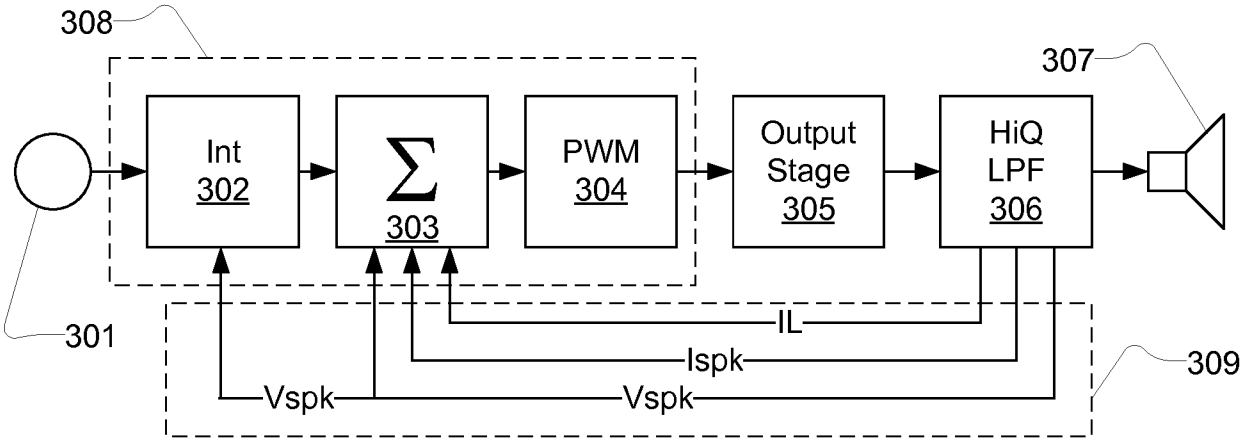


Fig. 3

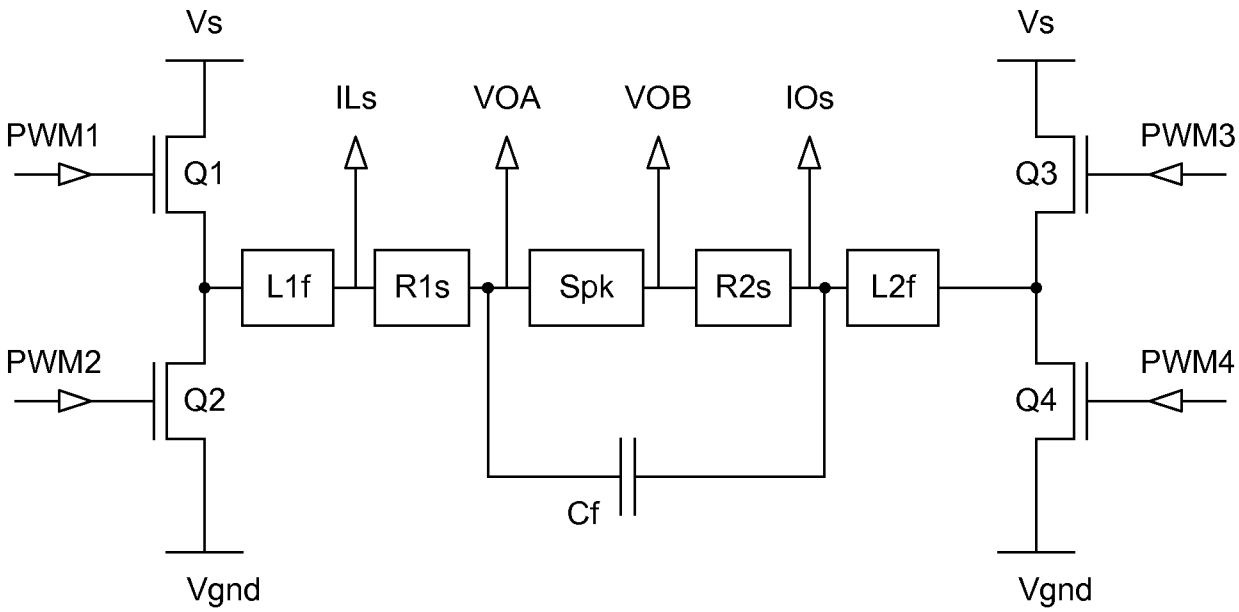
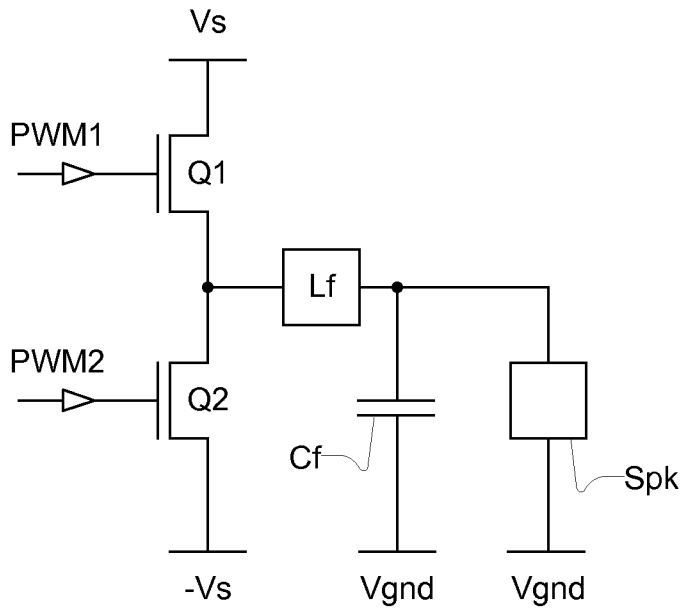

Vs
Vs
ILs
VOA
VOB
IOs
PWM1
Q1
Q3
PWM3
L1f
R1s
Spk
R2s
L2f
PWM2
Q2
Q4
PWM4
Cf
Vgnd
Vgnd

Fig. 4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PWM1
Q1
Lf
PWM2
Q2
Cf
Spk
-Vs
Vgnd
Vgnd

Fig. 5

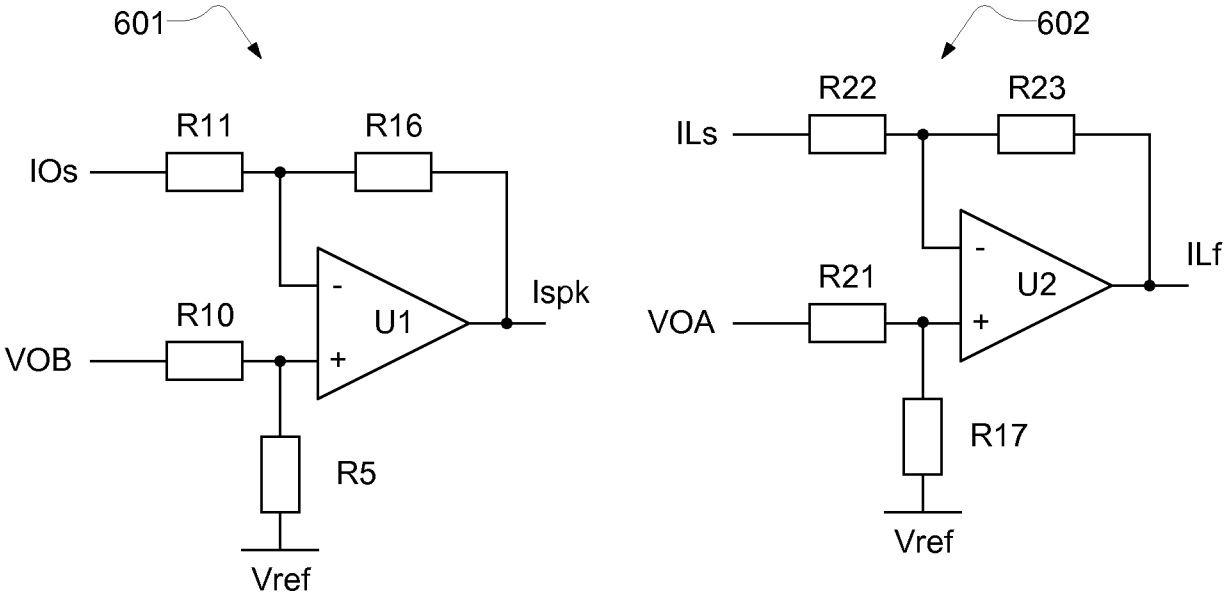

601
602
R11
R16
IOs
R10
VOB
U1
Ispk
R5
Vref
R22
R23
ILs
R21
VOA
U2
ILf
R17
Vref

Fig. 6

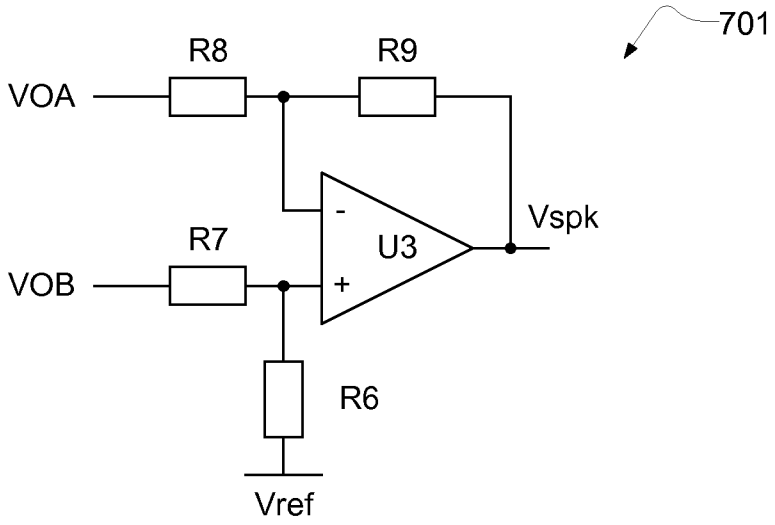

701
R8
R9
VOA
R7
VOB
U3
Vspk
R6
Vref

Fig. 7

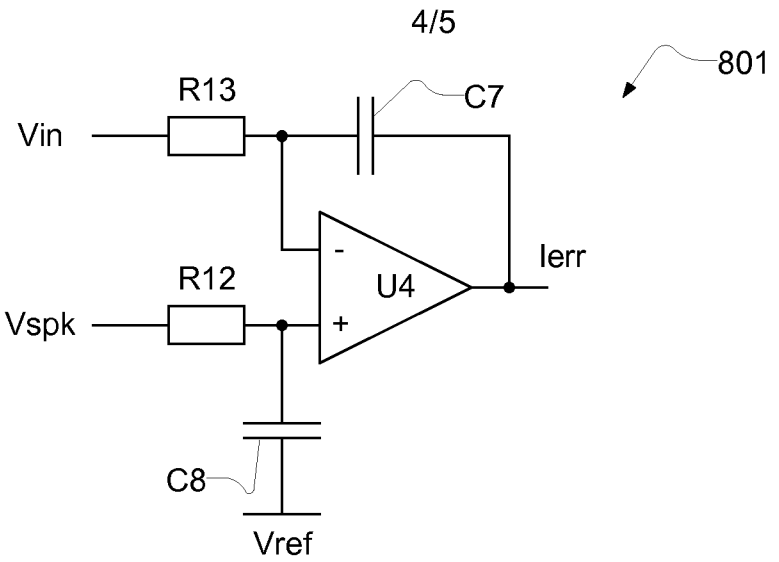


Fig. 8

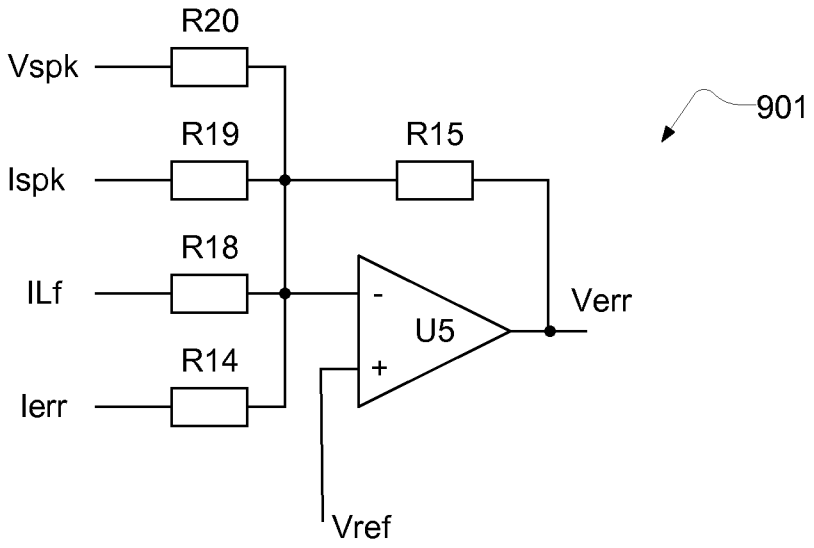


Fig. 9

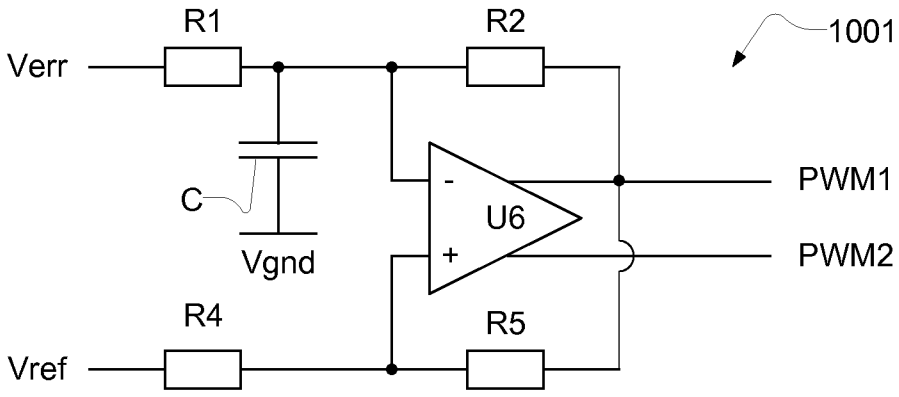
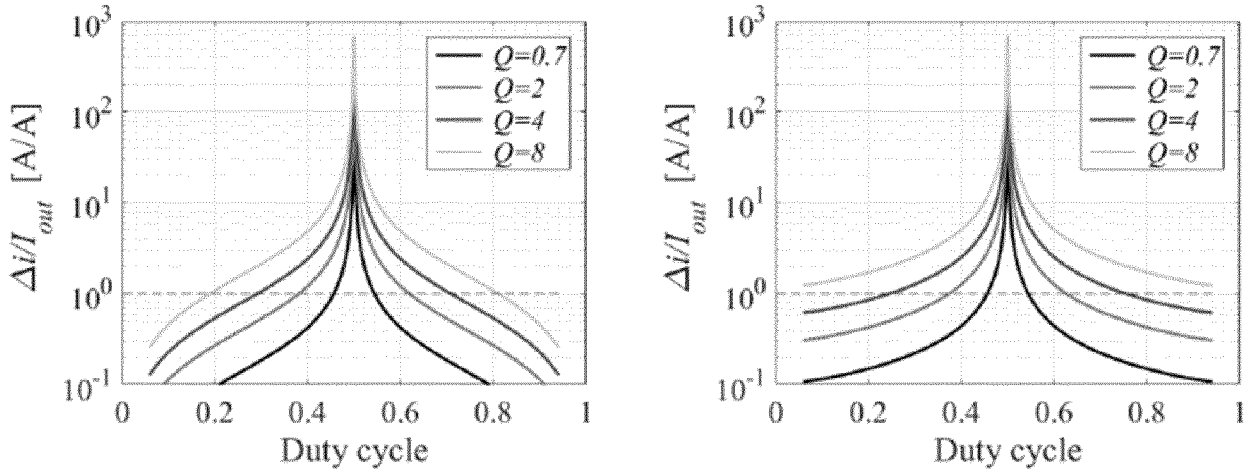


Fig. 10



(a) Fixed frequency modulation.

(b) Self-oscillating modulation.

Fig. 11

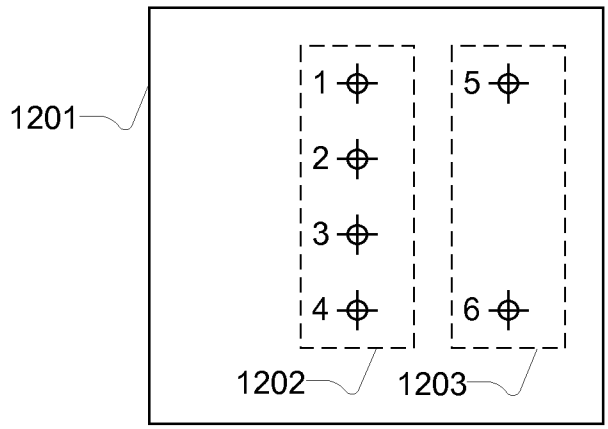


Fig. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/063132

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/32 H03F3/185 H03F3/217
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2005/002050 A1 (TC ELECTRONIC AS [DK]; FREDERIKSEN THOMAS MANSACHS [DK]; PEDERSEN KIM) 6 January 2005 (2005-01-06) page 14, lines 12-13; figures 1C, 5, 10 page 14, line 29 - page 15, line 2 page 16, lines 8-9 page 16, lines 17-18 page 47, line 16 - page 48, line 6; figures 22A-22C -----	1-13
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 July 2018	17/07/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Zakharian, Andre

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US 2015/124982 A1 (BERTHELSEN KIM SPETZLER [DK] ET AL) 7 May 2015 (2015-05-07) paragraph [0040]; figure 3	2-13
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A	SHIANG-HWUA YU ET AL: "Optimal Control of a Nine-Level Class-D Audio Amplifier Using Sliding-Mode Quantization", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 58, no. 7, 2 July 2011 (2011-07-02), pages 3069-3076, XP011355900, ISSN: 0278-0046, DOI: 10.1109/TIE.2010.2077611 abstract; figures 1,7	1-13
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