Micromachined integrated 2D transducers for super resolution ultrasound imaging

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Publication date:
2022

Document Version
Publisher's PDF, also known as Version of record

DTU Health Tech
Department of Health Technology

Technical University of Denmark

Ph.D. Thesis

Micromachined Integrated 2D Transducers for Super Resolution Ultrasound Imaging

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30th August 2022

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Cover image: A row-column addressed ultrasound probe developed in this work and presented in [1].

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Preface

This PhD thesis has been submitted to the Technical University of Denmark, in partial fulfilment of the requirements for the degree of Doctor of Philosophy. The research presented in this thesis has been conducted in the period from May 2019 to August 2022, including an extension period of four months, at DTU Health Technology, Technical University of Denmark. The project has been supervised by Professor Erik Vilain Thomsen and co-supervised by Professor Jørgen Arendt Jensen. During this project, the author has had the privilege attending of attending three international conferences. These are the IEEE International Ultrasonics Symposia in 2019 (United Kingdom, Scotland), 2020 (Virtually in USA, Las Vegas) and 2021 (China, Xi'an).

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Summary

Medical ultrasound imaging is a widely used real-time technique for non-invasive diagnostics. Conventional ultrasonics 1D linear probes produce 2D images of the human body. Organs and tissues are, however, not confined to a 2D plane in the body. Vital information out of plane may therefore be lost due to the three dimensional nature of the organ and any movement of the probe. A major drive in the field of ultrasound is therefore to progress towards 3D ultrasound imaging using 2D arrays. To achieve a good focus and a high resolution, a large number of elements are needed, which translates to probes with large surface areas. In fully addressed 2D matrix arrays, this increases the complexity of the underlying technology. The number of interconnections needed in probe will also scale with, N^2, which quickly makes the process infeasible for large arrays with a high channel or element count, N.
Recently, a different type of technology using a row-addressing element scheme has been introduced. This reduced the complexity of the arrays by addressing only the N row and N column elements, and the required number of interconnects is only $2N$.

The main goal of this project has to develop large scale 2D 190+190 row-column-addressed (RCA) capacitive micromachined ultrasonic transducer (CMUT) arrays for the use in three dimensional real-time volumetric imaging. The CMUT platform was chosen as offers a high degree of flexibility, low self-heating and a large bandwidth beneficial for imaging applications. This has been achieved through the successful fabrication of two chip designs. These were based on two different fabrication techniques, and investigated to produce stable and reliable transducers. The techniques are using the local oxidation of silicon (LOCOS) based process combining fusion and anodic bonding with highly doped silicon as bottom electrodes, and using a purely anodic bonding process with metal bottom electrodes. They each have their advantages as CMUT platforms for building arrays with a uniform pressure output for all elements.

These chips were integrated in custom made hand-held transducer probes. One of these probes being a modular prototype probe for rapid prototyping developed in this research group. The electrical and acoustical performance of the two transducers were evaluated, and the 3D imaging capabilities for one of them was demonstrated. The imaging depth was found to be 3.6 cm. In conclusion, results show that the row–column technology is a realistic alternative to matrix probes for volumetric imaging. Furthermore, it is shown that the two processing techniques can be used as viable platforms for producing stable transducers. Further development is needed for achieving optimal performance.

Resumé

Medicinsk ultralydsbilleddannelse er en hyppigt anvendt metode til at udføre ikke-invasiv diagnostik i realtid. Konventionelle 1D ultralydsprober bliver brugt til at tage 2D-billeder af den menneskelige krop. Kroppens væv og organer er dog ikke begrænset til at ligge i et 2D-plan i kroppen. Der kan derfor gå vital information tabt under en scanning fra organer som befinder ude af planet. Dette kan nemt forekomme ved bevægelser af organet eller hvis proben flyttes. En stor indsats inden for ultralydsfeltet har derfor været at gå mod 3D ultralydsbilleddannelse ved brug af 2D-arrays. For at opnå god fokusering og en høj opløsning er et stort antal elementer nødvendigt. Dette betyder at prober med et stort overfladeareal kræves. Fuldt adresseret 2D matrix-arrays kan bruges til dette formål, men dette øger kompleksiteten af den bagvedlæggende teknologi. Antallet af elektriske forbindelse krævet skalere med N^2, hvilket hurtigt gør processen nær umulig for store arrays med et højt antal kanaler eller elementer, N. For nylig er en anden type teknologi, der anvender en række-søjle adresserings metode for elementerne, blevet introduceret. Dette reducerer kompleksiteten af 2D arrays ved, at der kun skal adresseres N række- og N kolonneelementer. Det nødvendige antal elektriske forbindelser er derfor kun $2N$.

Hovedmålet med dette projekt er at udvikle store 2D 190+190 række-kolonne-adresserede (RCA) CMUT-arrays til brug i tredimensionel volumetrisk billeddannelse i realtid. CMUT'en som Fabrikationsplatform er blevet valgt på grund af at den tilbyder en høj grad af fleksibilitet, lav selvopvarmning og en stor båndbredde som er gavnlig for billeddannelse. Dette er opnået ved at fremstille to vellykkede chipdesigns. Disse var baseret på to forskellige fremstillingsteknikker og er undersøgt med det mål at kunne producere stabile og pålidelige transducere. Den ene teknisk er baseret på den såkaldte lokale oxidation af silicium (LOCOS), som er en proces der kombinerer fusion og anodisk bonding med et højt doteret silicium substrat som bundelektroder. Den anden teknik anvender en anodisk bonding proces med bundelektroder af metal. De har hver deres fordele som CMUT-platforme til at fremstille store arrays arrays med et ensartet tryk output for alle elementerne. Disse chips blev integreret i håndholdte transducerprober. En af disse prober er en modulær prototypeprobe til hurtig prototyping, og er udviklet i denne forskningsgruppe.

Den elektriske og akustiske ydeevne af de to transducere blev evalueret, og muligheder for at udføre 3D-billeddannelse blev demonstreret for en af dem. Billeddannelse blev vist muligt ned til en dybde på 3,6 cm. Som konklusion viser resultaterne, at række-søjle-teknologien er et realistisk alternativ til matrixprober til 3D volumetrisk billeddannelse. Endvidere er det vist, at de to fremstillingsmetoder kan bruges som mulige platforme til fremstilling af stabile transducere. Videre udvikling er nødvendig for at opnå optimal ydeevne.

Acknowledgements

First of all I would like to thank my main supervisor Professor Erik V. Thomsen and my co-supervisor Professor Jørgen Arendt Jensen. I thank you for your immense guidance and many interesting discussions both in the MEMS and CFU group. I am truly happy that I have had the opportunity to be a part of this research project in a group working on state-of-the-art ultrasonic devices.

I have learned a great many things from you Erik. Your great optimism, patience and both moral and academic support has helped me through the ups and downs of this PhD thesis, without which I am uncertain if I would have finished.

I would like to sincerely thank my colleagues at DTU Health Technology and in the MEMS group, both current and former. I thank my PhD peers, both in and out of the cleanroom, for providing a social and positive atmosphere. Thank you for always being there for both private and interesting CMUT related research discussion. A special thanks if given to Martin Lind Ommen and my fellow Master's and then PhD students Stine Løvholt Grue Pedersen and Kitty Steenberg for the great moral support.

For the great help and support during the various fabrications processes in the cleanroom facilities, I would like to extend my thanks to the staff at DTU Nanolab (former DTU Danchip). Without their help, this project would not have been possible.

I would also like to thank our Christopher Beers and our partners at BK Medical for their collaboration, including their branch in Herlev, Denmark, and in State College, PA, USA

Last, but not least, a huge thanks goes to my close friends, my mother and my late father for always supporting me.

Acronyms

AC	alternating current
AFM	atomic force microscope
AIMS	Acoustic Intensity Measurement System AIMS III
AR	augmented reality
ASE	advanced silicon etcher
ASIC	application specific integrated circuit
BCB	benzocyclobutene
BHF	buffered hydrofloric acid
BOX	buried oxide
CCB	chip carrier board
CFU	Center for Fast Ultrasound Imaging
CMP	chemical mechanical polishing
CMUT	capacitive micromachined ultrasonic transducer
DC	direct current
DOE	design of experiments
DREM	deposit, remove, etch, multistep
DRIE	deep reactive-ion etch
DSP	double-side polished
EMI	electromagnetic interference
FEM	finite element method
FFT	fast Fourier transform
FPM	fully populated matrix
FWHM	full-width-half-maximum
HCP	hexagonal close packed
HF	hydrofloric acid
IBE	ion-beam etcher
KOH	potassium hydroxide
LOCOS	local oxidation of silicon

LPCVD	low pressure chemical vapour deposition
MLA	maskless aligner
NIL	nano imprint lithography
PCB	printed circuit board
PDMS	polydimethylsiloxane
PRF	pulse repetition frequency
PSF	point spread function
PSOI	poly-silicon-on-insulator
PZT	lead zirconium titanate
RCA	row-column-addressed
RIE	reactive-ion etching
RoHS	reduction of hazardous substances
RTV	room temperature vulcanizing
SA	synthetic aperture
SARUS	synthetic aperture real-time ultrasound system
SEM	scanning electron microscopy
SNR	signal to noise ratio
SOI	silicon-on-insulator
SSP	single-side polished
TOBE	top-orthogonal-to-bottom electrode
UV	ultraviolet

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Chapter 1

Introduction

The use of medical ultrasound or ultrasonography dates back to around the middle of the 20th century [2], [3] where it was already then seen as a new tool or modality with a lot of potential for medical therapy [4]. The technology has since then grow into the multi-functional diagnostic tool we know from hospitals today in the form of lightweight hand-held transducer probes. Ultrasonic imaging is seen as a harmless and non-invasive technique when compared to other imaging techniques like standard X-ray or computed tomography (CT) scans and even magnetic resonance imaging (MRI) as no ionising rays or harmful contrast agents are used. Medical ultrasound is relatively inexpensive compared to the previously mentioned techniques and the probe is used in conjunction with a portable computer, which can placed right beside the patient. This allows doctors to obtain diagnostic images of patients in real time right at their bedside. Ultrasound however might offer poor resolution with increasing scanning depth compared to other modalities, unless the ultrasonic probe is brought closer to the tissue of interest by inserting it into the body with laparoscopic methods or the footprint of the transducer is increased.
Ultrasound images are made by mapping the echoes generated when transmitted acoustic pulses are fully or partially reflected or scattered from structures in the scanned medium. These reflections arise from an acoustic impedance mismatch in-between two types of tissue or structures in the human body. Bone in particular gives a large reflection of the signal and makes it difficult to scan structures behind bone or dense tissue. Similarly, the lungs and potentially the colon will be difficult to scan due to the presence of air, which creates large reflections.

Most ultrasonic probes used in hospitals for medical imaging are made using the poly-crystalline piezoelectric ceramic material lead zirconate titanate (PZT) which is also used for many different sensing devices, actuators, and low-power systems. These probes usually have between 64-256 long ceramic crystal elements with a width in the micrometer scale for generating ultrasound used for imaging. This device works by utilising the piezoelectric effect by applying an alternating current (AC) signal with a megahertz frequency across the crystal to make it vibrate in the same frequency. PZT has been an industry standard for several decades due to its high piezoelectric coefficient, electromechanical coupling coefficient and dielectric constant desirable for impedance matching [5]. Alternative piezoelectric ceramics such as the lead-free ceramic potassium sodium niobate (KNN) or lead magnesium niobate-lead titanate (PMNT) also exist. Ceramics different from PZT, including lead-free types, however, usually have poorer material parameters and are often more expensive, which makes PZT synonymous with piezo ceramics in ultrasound. PMNT, albeit more costly, can be grown as a single crystal and could be a likely candidate for replacing PZT due to its excellent piezoelectric properties.

The PZT arrays used in probes are often fabricated using the dice-and-fill method [6]. Here the kerf between the crystal elements is limited by the width of the dicing blade to around 15 µm [7]. This can pose a problem for high frequency probe designs, where the element width becomes comparable

to the kerf for small pitch probes. This results in a small relative active area for transmitting ultrasound, which reduces the pressure of the array. The resonance frequency of PZT crystals given by speed of sound in the material over the crystal thickness. Thus, for high frequency probes the thickness becomes small, which makes them fragile and more difficult to fabricate.

Furthermore, in the recent years there has been an increasing concern over environment and health related risks over the use of lead containing materials. As much as 100 metric tonnes of lead is used in the field of medical ultrasound each year, with approximately 90 tonnes emitted to the atmosphere. The total annual production of lead zirconium titanate (PZT) material is estimated to be around 5000 tonnes [8] of which a 60 weight percentage is comprised of lead [9]. The reduction of hazardous substances (RoHS) directive from 2006, also called the "lead-free directive", list lead as a banned substance for use in electrical and electronic equipment. The exemption is of PZT ceramics for use in medical devices, and other applications using ultrasound [10] where no optimal alternative is found. An alternative to the continued used of lead based PZT for medical ultrasonic probes is sought, which also eases the fabrication process for high frequency operation, which is used for a wide range of applications,

1.1 CMUT

One alternative to the piezoelectric transducer is the CMUT based on silicon microfabrication. A CMUT is a small device in the micrometer range which can transmit ultrasound, much like the PZT crystal. The difference is that it instead consists of a micromachined cavity on a substrate and a vibrating plate (or membrane) separated by an electrically insulated material, such as a dielectric. Such a CMUT structure is referred to as a cell and is illustrated in Fig. 1.1. Typically it has lateral dimensions in the range of 10 µm to 100 µm, vertical dimensions in the range of 200 nm to 800 nm for the gap in the cavity, and 1 µm to 6 µm for the vibrating plate. Hundreds of these cells comprising a single element are used to transmit ultrasound in unison. These cells can be defined through the use of simple ultraviolet (UV) lithographic processes. UV lithography can make features down to ≈0.6 µm in width and CMUT devices can therefore be made smaller than what is usually possible for piezoelectric transducers, and the pitch can more easily be controlled. This allows for an element pitch of $\lambda/2$ to be kept for high center frequencies, which minimises grating lobes [11]. A smaller feature size and precise definition of structures also allows for easier integration with integrated circuits (ICs) on chip.

The idea of utilising a capacitive structure as an ultrasonic actuator for studying pressure fields in liquids and air was presented in the early 1990s. In an IEEE IUS conference paper from 1991 by Schindel et al. [12] describes how conventional IC manufacturing techniques can be used for constructing capacitive devices, capable of radiating ultrasound in the megahertz regime, with a fixed conductive back electrode and a suspended vibrating membrane. These studies were further developed simultaneously by Hietanen et al. in 1993 [13] (using a V-grooved backplate electrode) and in a journal paper in 1995 [14] Schindel et al. Common for these are that they use semiconductor microfabrication to create silicon bottom electrode and utilise metallised Mylar polyester foil or Kapton tape as the membrane.

The first and most influential paper accredited to the birth of what came to be known as the CMUT is a conference paper from 1994 titled "A Surface Micromachined Electrostatic Ultrasonic Air Transducer" by Matthew I. Haller and Butrus T. Khuri-Yakub [15]. This paper describes the theory of operation, fabrication and characterisation of a fully surface micromachined silicon based transducer with a 750 nm silicon nitride membrane. The air-coupled transducer operates at a resonance frequency of 1.9 MHz, and the cavity was fabricated by a sacrificial release process using a silicon dioxide layer. This study was followed by a journal paper by the same authors in 1996 [16]. Same year, broadband emission of transducer arrays with frequencies at 4 MHz, 6 MHz and 8 MHz from the same group were studied in immersion which showed a wide bandwidth in the range from 1 to 20 MHz and high signal-to-noise ratio capable of competing with piezoelectric devices [17].

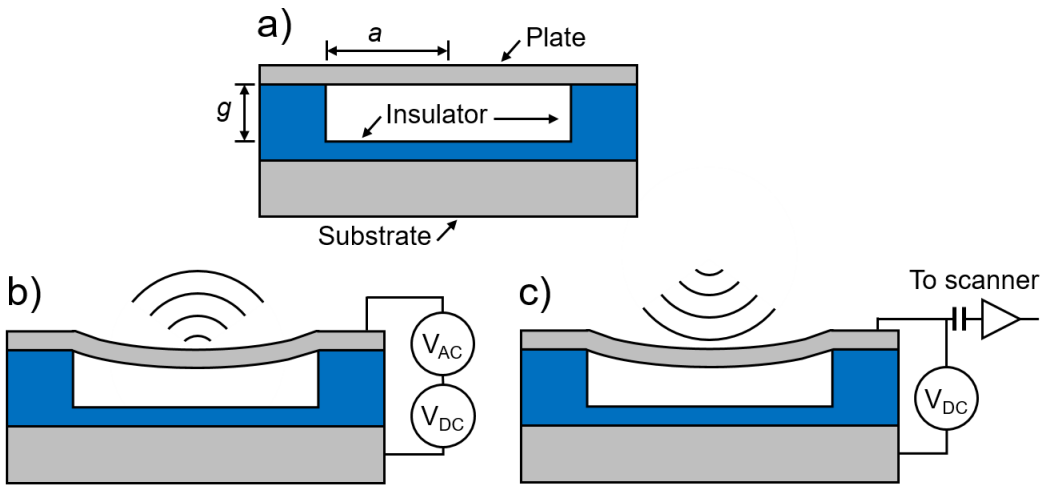


Figure 1.1: Cross-sectional sketch of signel CMUT cell. a) The dimensions and components of the cell are indicated. The vibrating plate is shown with the radius of half side length a, and the substrate and insulating dielectric is shown with the vacuum gap g. b) The CMUT operating as a transmitting device, with a DC voltage bias and an AC signal is applied between the plat (top electrode) and substrate (bottom electrode) to send out an ultrasound signal. c) The CMUT operating as a receiving device, with a DC voltage bias applied and the incoming ultrasound signal converted to an AC signal for the scanner.

In 2000 the first experimental pulse-echo results on a wire phantom in immersion using a 16 element 1-D CMUT array is presented by Oralkan and Khuri-Yakub [18] and shows a B-scan image made from RF beamforming. This research was further developed in 2002 [19] [20] showing capabilities of fabricating 128 by 128 element 2-D CMUT arrays with the potential for 3-D volumetric ultrasonic imaging. Due to the large amount of interconnections needed, only a smaller sub-array was measured. A follow-up article from 2003 shows the first volumetric scans using the arrays [21].

A new type of fabrication technique for CMUT devices was presented in a paper from 2003 by Huang et al. [22] based on wafer bonding. In this technique a silicon-on-insulator (SOI) wafer is bonded to a micromachined silicon wafer with cavities through silicon direct bonding (fusion bonding) to form the transducers. The device layer of the SOI wafer is a high resistivity silicon, which when the SOI wafer is etched will form the CMUT membrane.

In 2004 and 2005, the design, fabrication and characterisation of a 64 element 3 MHz 1D CMUT probe was presented by Caliano et al. [23], [24], using sacrificial release methods and compared to a commercial PZT probe with a lens.

The same group from the Roma Tre University, presented a different type of sacrificial release method using a novel reserve fabrication process (RFP), presented by Caliano et al. in 2005 in [25]. The CMUTs are defined on top of a silicon handle substrate with a silicon nitride layer deposited. The thickness determines the CMUT plate thickness. After the CMUTs cavities have been defined through the sacrificial release method, the diced chips are wire bonded to a printed circuit board (PCB) and a backing layer is applied. The silicon handle layer can then be etching from the backside using a mixture of hydrofluoric, nitric, and acetic acids (HNA). The backside, which is now the front side, reveals the CMUT array and the nitride plate of the cells. This technique was used to fabricate a 192 element 12 MHz 1D CMUT probe, presented in 2012 by Savoia et al. [26].

A different wafer bonding approach was demonstrated in 2009 by Olcum et al. [27] by CMUTs fabricated with anodic bonding. In this technique a glass wafer is usually structured and bonded to a silicon substrate, which is subsequently thinned to a specified plate thickness. Functional 1D linear CMUT arrays utilising anodic bonding has since been published [28]–[30].

Since the first use for 2D imaging [18], the CMUTs technology has been successfully used for fab-

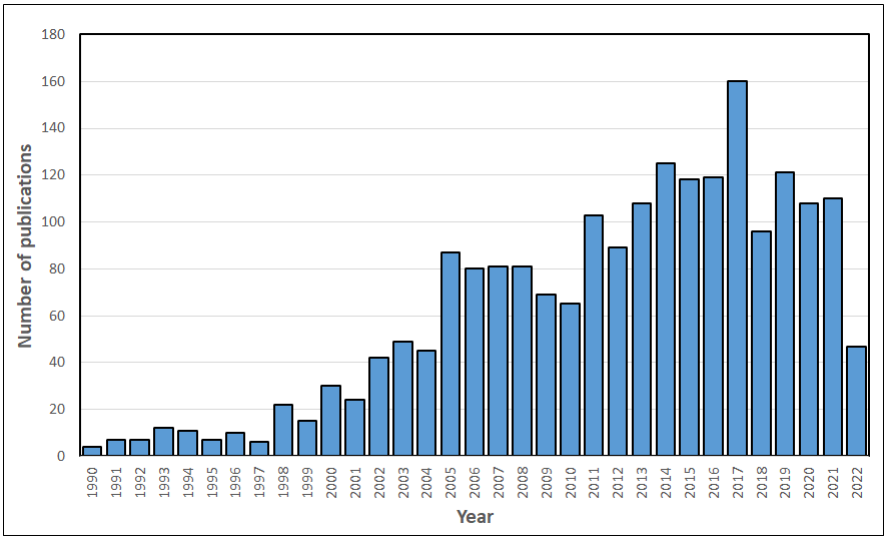


Figure 1.2: Number of CMUT publications from 1990 to 2022. This graph has been generated from the Scopus database using the following keystring: Capacitive Micromachined Ultrasonic Transducer* OR CMUT OR CMUTs OR Electrostatic Ultrasonic Air Transducer OR Capacitive Transducer* OR Surface Micromachined Transducer" OR Surface Micromachined Transducer". A total of 2212 publication are listed.

rication 1D linear array probes by several academic and industrial research groups [23], [24], [26], [31]–[38] and more recently such probes have become commercially available. The field of CMUTs is rapidly expanding, which is illustrated in the Fig. 1.2 as the number of publications per year. The final count in 2022 is taken at the point in time of hand-in for this PhD thesis, which also happens right before the large International Ultrasound Symposium (IUS), where a substantial amount of CMUT papers are published.

1.2 3D imaging

When ultrasound imaging is performed, it is most often the so-called B-mode or brightness mode which is used. Using a linear 1D transducer, this produces 2D gray-scale images in real time of the brightness or intensity of the reflected sound waves in the body. The images display a scanned plane orthogonal to the transducer surface with scan depth and width and at the axes. A-mode or amplitude modulation is a simpler type of ultrasound consisting of just a single intensity line, which makes up the B-mode images, and amplitude on the y-axis and imaging depth on the x-axis. M-mode, or motion mode, is a mode used for rapid imaging, where many line scans are taken in succession together with B-mode images to monitor the movement of organs and vessel boundaries. Another type of mode is the Doppler mode, which makes use of the Doppler effect to measure the directivity and velocity of the blood flow in vessels. This can be used to display full color maps of blood flow in real time by color flow mapping (CFM), which enables easier diagnosis of vascular problems. The blood direction and velocity can be colour coded as colour intensity and displayed on top of B-mode images.

Blood vessels and organs in the body will when imaged with a linear 1D transducer, however, be confined to a 2D plane. Important out of image plane information may be lost due to the three-dimensional nature of the organ and any movement of the probe. A natural further development and also a major drive in the field of ultrasound is therefore to progress towards 3D ultrasound imaging using 2D arrays.

3D volumetric imaging with ultrasonic probes can be achieved with 2D arrays. Such an array can be constructed by extending or replicating a 1D array design in the orthogonal direction N number

of times, corresponding to the element count in the 1D array. This is called a fully populated matrix (FPM) array and has $N \times N$ elements. Each of these elements in the matrix need to be individually accessed and this requires the same amount of inter-connectors. To achieve a good focus and a high resolution with an ultrasonic probe a large number of elements are necessary.
The focusing ability is proportional to the wavelength of the ultrasonic signal and the ratio of the imaging depth to the width of the array. If the same resolution is to be kept in both dimensions of the array, the same number of elements are needed in both directions of the array. Higher resolution at a large imaging depth requires that the ultrasonic probes, and therefore also the arrays, becomes larger to maintain the ratio between depth and width.

If a 2D FPM probe should have the same resolution in both dimensions as e.g. an 1D linear probe with 190 elements, this would require $190 \times 190 = 36100$ elements and inter-connections. This can make it highly infeasible to make large scale matrix probes.

Smaller state-of-the-art matrix probes made using PZT can be acquired from commercial suppliers from e.g. Philips (X6-1 xMATRIX array transducer with 9212 elements). Probes used for research can also be acquired through Verasonics (Matrix Array Transducer with 1024 elements (32×32)).

The high connection count of matrix probes can be reduced significantly by utilising other array design which use alternative element addressing schemes. Recently, a new type of scheme was proposed by Morton and Lockwood [39] as a crossed electrode design. This is a so-called RCA array. It is essentially the combination of two 1D linear array layered orthogonal to each other, illustrated in Fig. 1.3. The section where each element overlap is defined as a sub-element or a unit cell. In this scheme the long rows and columns of the array are addressed individually similar to a 1D array, instead of the corresponding single matrix elements in an FPM array. This reduced the number of connections to just $N + N$, which for a $190 + 190$ RCA array equals 380 elements. This row-column technique has since been used by multiple research groups for fabricating arrays for 3D imaging.

It has been shown by Rasmussen and Jensen [40] that the imaging resolution of RCA arrays will always be higher for the same number of elements when compared to an FPM array, e.g. a $128+128 = 256$ row-column array corresponding to a 16 matrix array. The latest details regarding the imaging capabilities of the RCA arrays for 3D volumetric super resolution imaging can be found in [41].

1.3 2D CMUT arrays

2D Row-column arrays have been fabricated with a variety of different materials and array sizes, such as using PZT, by Seo at al. as 64×64 and 256×256 arrays (addressed as $64 + 64$ and $256 + 256$ row-column arrays) [42], [43], and by Chen et al. using a combination of PZT and a P[VDF-TrFE] copolymer [44]. The row-column addressing scheme has also been presented by a Canadian ultrasonic research group from the University of Alberta with a different terminology named top-orthogonal-to-bottom electrode (TOBE). Such an array was presented using a PNM-PT electrostrictive ceramic by Latham et al. in [45]. A research probe was recently presented in our group with an integrated PZT based $62+62$ RCA array by Engholm et al. in 2018 [46]. Commercial row-column probes made using PZT are available from Vermon and Verasonics (RC6gV Row-Column Array Transducer), which have 128+128 rows and columns with a 6 MHz center frequency. Recently prototype probe with 128+128 rows and columns with a 12 MHz center frequency was introduced by Daxsonics.

The row-column addressing scheme has also been used for CMUTs, which is the focus of this PhD thesis. These have been fabricated using many different etching and bonding methods, such as by using the sacrificial release method [47], [48], with a TOBE array architecture, adhesive wafer bonding [49], [50], fusion bonding [46], [51]–[54] and anodic bonding [55]–[57]. Some of the listed probes from this group have been integrated in hand-held probes and interfaced the scanners from the company BK Medical. These are presented in [46] as a 62+62 RCA 2D CMUT probe alongside a PZT row-column probe with also 62+62 elements, and in [54] as two 92+92 RCA 2D CMUT probes with and without integrated diverging lenses. Commercially available probes using RCA addressed

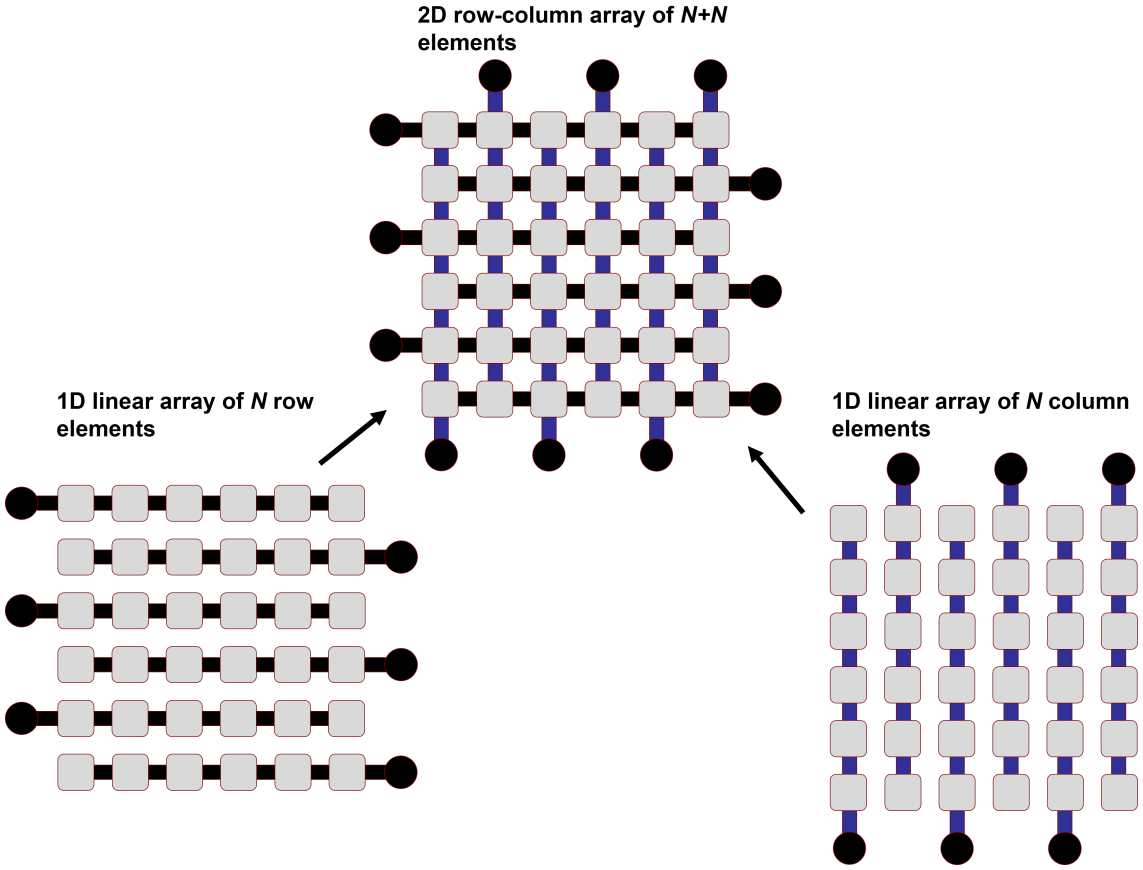


Figure 1.3: Sketch of the 2D row-column addressed array structure as a combination of two orthogonal N element 1D linear arrays with alternating electrodes pads.

CMUT technology are not yet available.

However, recently the company Butterfly Network, Inc. (Guilford, CT, USA) made a 2D CMUT transducer called Butterfly iQ. It is a type of 2D phased array matrix transducer with $140 \times 64 = 8960$ elements, which can be used in different configurations as curved, linear and phased arrays if needed. The CMUT chips are integrate with a large application specific integrated circuit (ASIC) die. The probe is designed to be connected to a phone or tablet and be run without external power. Images are shown directly on the mobile device and can be used together guided scanning based on augmented reality (AR).

1.4 Designing large CMUT arrays

It was introduced in the previous section that the 3D imaging technique utilizing RCA scheme requires a 2D row-column CMUT array with many elements to capture a 3D volume with a high resolution. It is inevitable that the trend will then be a progression towards large arrays to accommodate the elements. When designing large RCA arrays there are a number of important criteria to ensure optimal performance as well as a few choices of fabrication techniques.

1.4.1 Electrode resistance

When an element is excited by an AC signal the pressure emitted along each element, whether rows or columns, and across neighbouring elements should be uniform. If this is not the case, the pressure

field of the array when performing imaging will not match simulated fields and can be detrimental to the image quality. The pressure drop which is a direct result of an attenuation of the voltage potential along the element can be modelled as a so-called delay-line effect [58], which can be derived from a diffusion equation describing the element potential along the element. In Section 2.1.8 this will be explained more in detail, the result, however, is a an expression describing the remaining voltage potential at the end of the element and a dimensionless product ωRC, which can be used as a criterion when designing the arrays. The product contains the angular excitation frequency, ω, the element electrode resistance, R, and the total capacitance of the element, C.

To keep a uniform pressure distribution, the potential drop along the element is set to a maximum of 1 %. This corresponds to an ωRC value of

$$\omega RC \leq 0.35 \tag{1.1}$$

This value, which should be as low as possible, sets requirements for the material used to fabricate the top and bottom electrodes and the techniques needed. Bottom electrodes are typically made with either deposited metal, e.g. in Al, Cr, or Au on top on an insulating substrate, or with a highly doped silicon substrate used directly as an electrode.
If silicon is used as bottom electrode material, a limit of around $10^{21}\,\mathrm{cm}^{-3}$ which is designated as heavy doping [59], is set as the highest n-type doping level which can be achieved by doping with phosphorus [60, p. 377], which is a limit governed by the solid solubility of the dopant in silicon. A slightly higher concentration can be achieved using As instead of P.

This corresponds to a resistivity of $10^{-4}\,\Omega\,\mathrm{cm}$ [60, p. 18]. Higher concentrations can likely be achieved near the substrate surface using ion-implantation and by the pile-up effect through annealing [60], but whether these dopants are electrically active and can contribute to the conductivity is not fully known. However, it does seem possibly that even higher active donor doping levels are possible through using the chalcogen donor Te [61].

Depending on the dopant and doping level this can prove problematic for long arrays as the resistance is proportional to the length $R \propto L$ and capacitance proportional to the electrode area $C \propto A$. CMUTs fabricated with a silicon substrate using fusion/direct bonding process [62], [63] requires a high temperature post annealing step at >1000 °C to fuse the dielectric insulation layer with a top plate.

Such a device is illustrated in Fig. 1.4(a) fabricated on an SOI wafer made with direct or fusion bonding. The temperature step makes this technique incompatible with metal bottom electrodes, and one has to rely on doped silicon for the bottom electrodes to keep the resistance sufficiently low. In applications where the doped silicon wafer substrate or the silicon device layer serves as the bottom electrode, the handle or layer thickness can be increased to decrease the resistance.

Metal electrodes have a resistivity on the order of $10^{-6}\,\Omega\,\mathrm{cm}$ [66], which being two orders of magnitudes lower than doped silicon, will reduce resistance problems and be sufficient for most applications, depending on the electrode shape. The use of metal electrodes and their low thermal budget limits the number of techniques which can be used for CMUTs to mainly three types.

1) Adhesive polymer bonding [67] using e.g., benzocyclobutene (BCB) [65], see Fig. 1.4(b). This is a versatile method for joining different types of substrates and top plates with a polymer spacer. The great advantage of using polymers is that they can be patterned as a standard UV-sensitive resist or using nano imprint lithography (NIL). Polymer bonding can be used with both silicon and metal bottom electrodes, here demonstrated with metal deposited and patterned on a fused silica wafer.

2) Sacrificial release methods [68], see Fig. 1.4(c). For this technique an intermediate sacrificial layer, often a metal layer, between the substrate and a dielectric layer is dissolved. This leaves CMUT cavities covered by a dielectric plate which are sealed using silicon dioxide or silicon nitride plugs. This can be used with both metal and silicon electrodes.

3) Anodic bonding [28], see Fig. 1.4(d). In this technique bottom electrodes are made by etching CMUT cavities into a glass substrate using a mask, metal electrodes are deposited and structured in

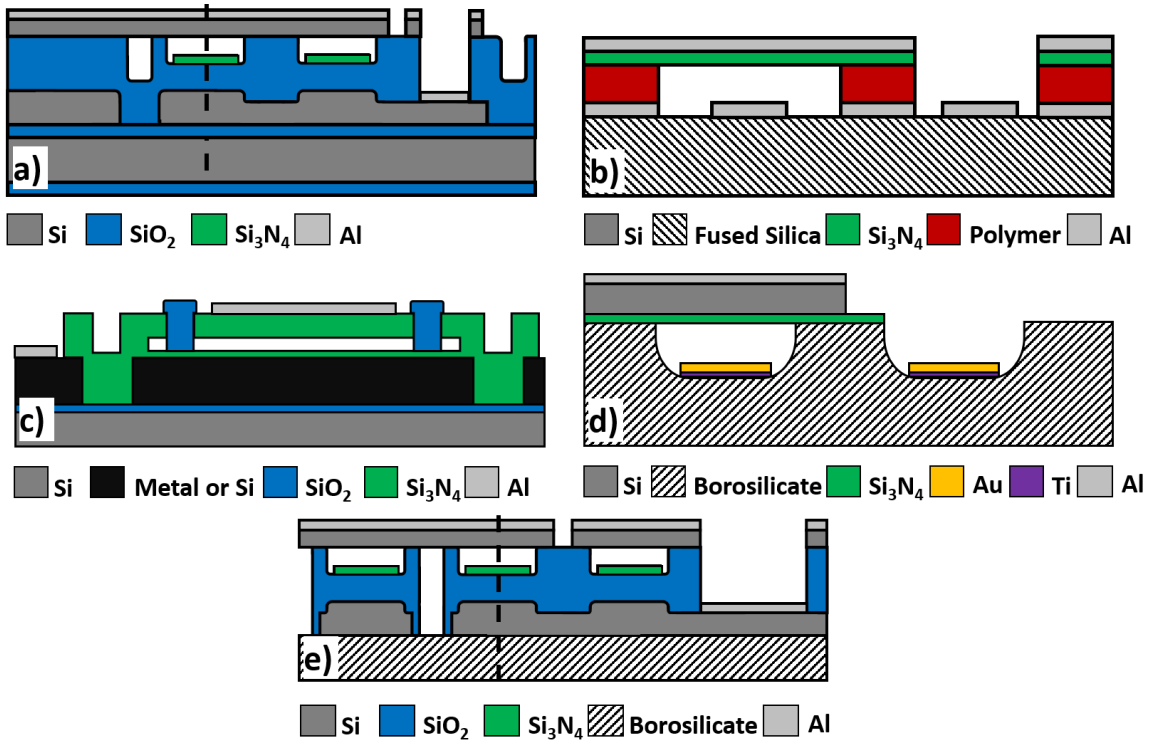


Figure 1.4: Cross-sectional view of five different RCA CMUT fabrication technologies. (a) Fusion bonding of a silicon top plate to a LOCOS structure grown on a doped SOI substrate. Figure is adapted from [64]. (b) Adhesive polymer bonding of a silicon nitride membrane to a fused silica wafer with metal electrodes using polymer [65]. (c) Sacrificial release method using a metal or doped silicon bottom electrode, where cavities are formed by etching of a sacrificial layer encapsulated in silicon nitride. (d) Anodic bonding of an insulated top plate to a structured borosilicate glass substrate with metal electrodes [55]. (e) A combination of a silicon top plate fusion bonded to a LOCOS structure and a borosilicate glass plate anodically bonded to the backside. A doped silicon substrate separated with a trench etch is utilised as bottom electrodes [1].

the cell cavities, and the substrate is bonded to a silicon top plate. This has a maximum processing temperature of 375 °C and can like (1)-(3) utilise a broad range of metals.

In contrast, CMUT top electrodes are typically made using a wafer-bonded plate of silicon or a membrane of silicon nitride, which is then covered with a thick metal layer of low resistivity. For typical electrode designs the electrode resistance of the top electrode will not affect the pressure field [69]. The metal deposition happens as one of the last process steps and is not affected by previous high temperature processes. It can therefore be used in combination with various types of CMUTs.

An ideal structure for low resistance signalling could be a glass wafer patterned with CMUT cells, using a relatively thick metal bottom electrode [28], [55], [57], such as the anodically bonded structure in Fig. 1.4(d). An alternative is the adhesions bonded device in Fig. 1.4(b). These types of devices will, if the plate or membrane collapses in one cell, short-circuit and possibly destroy the whole element if a protective dielectric layer is not used. The process of structuring cell cavities in a glass substrate with an etching process or by utilising a dielectric layer for the plate can, however, create stability issues and dielectric charging of the device [70]–[72]. Charging is a highly unwanted phenomenon which is currently not fully understood [73]. The effect can decrease the performance of the CMUT devices over time by opposing the electrical field inside the cells set up by an applied direct current (DC) bias voltage.

A fabrication process based on an SOI substrate together with the LOCOS technique [63] and fusion bonding have been shown to exhibit little to no charging [64]. The structure is illustrated in

Fig. 1.4(a). The LOCOS process, when used for CMUT fabrication, allows for reduced parasitic capacitance, high dielectric strength, good uniformity and tightly controllable CMUT dimensions and vacuum gap height down to under 10 nm precision due to the predictability of the oxide thickness [74]. Care should be taken to use an SOI wafer with a sufficiently thick device layer with a low resistivity to reduce the adverse attenuation in the bottom electrodes. The fusion bonding process is, however, very sensitive to particles present on the wafer surface during bonding on the top plate to the bottom substrate, and the surfaces need a very low RMS roughness of $\leq 0.5\,\text{nm}$ to $1.0\,\text{nm}$ [28], [75], [76]. There is therefore a high risk of a reduced array yield through the fabrication process. This problem will quickly scale with large RCA arrays as the defect free surface area needed scales with the number of elements.

The anodic bonding process is in comparison far less sensitive to particles caught between the wafers during bonding [77] and this can be a tremendous factor in increasing yield for large RCA arrays.

The two methods of fabricating bottom electrodes for CMUTs with highly doped silicon and metal electrodes are explored in this PhD thesis.

1.4.2 Substrate coupling

Another important consideration or criterion is that the receive sensitivity of both rows and columns should be equal to ensure even performance. The sensitivity will depend on how well the substrate coupling or cross-talk between elements [78] can be suppressed. The performance of each element in regards to the signal attenuation caused by the electrode resistance will likely also have an affect on the sensitivity. CMUT elements which are fabricated with a silicon substrate often utilise an SOI wafer during fabrication with an insulating layer to separate bottom electrodes from the handling substrate [47], [52], [64], [79]. This allows the elements to capacitively couple to each other through the substrate, giving rise to parasitic capacitance which will lower the receive sensitivity of the array as explained in [78]. This effect is primarily seen for the bottom electrodes integrated directly on top of the SOI or silicon substrate. By utilising only the columns (bottom electrodes) for transmitting and rows (top electrodes) for receiving, this problem can be reduced but will prevent complex transmit and receive sequences using both rows and columns.

A way to mitigate coupling effect could be to increase the signal path length between the elements by partially separating them with an etching process [69]. In this way the ωRC product is utilised by providing a high resistance path vertically in the elements, thereby attenuating the signal propagating through the substrate to the neighbouring element. To preserve a low ωRC along the elements, a highly-doped silicon electrode is needed. An alternative solution could be removing the electrical path through the substrate completely, which has previously been demonstrated in this group [65], [80]. If for example, a silicon device layer is used as bottom electrode, the elements can be completely separated by a deep silicon etching process and an insulating glass substrate can be bonded to the backside as an alternative to silicon. This structure is shown in Fig. 1.4(e) as a combination of a conventional, to this group, LOCOS based process, which is combined with deep trench etch and bonded to an insulating borosilicate glass substrate [1].

1.5 The super resolution imaging project

This PhD project is part of the Super Resolution Imaging (SRI) project supported by Innovationsfonden. The SRI project is a collaboration between DTU Health Technology, Rigshospitalet, KU and the company BK Medical. By combining the strengths of the partners, DTU will be able to make a significant contribution to the field of 3D super resolution ultrasound imaging. The PhD project is centrally located within the strategy of DTU Health Tech, with a focus on medical components, materials development, transducers and new technology. The project combines micro and nanotechnology for development of ultrasonic transducers. Recent results show that this opens up new possibilities for design of ultrasonic scanner probes suitable for 3D super resolution imaging.

Thus, the scientific hypotheses are clear and well-defined. The project is highly innovative and the results will, in addition to publication in international journals, be used to develop a new generation of ultrasound scanner probes having integrated microfabricated 2D transducer arrays which will enable 3D super resolution visualization.

The main idea of the project is built on the concept of super resolution, which relies on imaging objects smaller than the diffraction limit of the wavelength used. By definition, objects below the limit cannot be resolved with conventional methods and will appear blurred and highly distorted by the point spread function of the imaging system. The spatial position of the sub-wavelength objects can instead be estimated by center of mass calculations. This principle can be used for super resolution imaging using ultrasound by injection gas micro-bubbles into the blood stream. Since the acoustical impedance of the bubbles is higher than the surrounding blood and tissue, a large ultrasonic echo is received. This can be used to accurately localise the sub-wavelength bubbles for super resolution imaging. This was previously demonstrated in 2D imaging using 1D probes [81]. However, in in-vivo experiments in the blood vessels the bubbles will occasionally move out of the 2D imaging plane as they are not confined in a single plane, but instead spread out in three-dimensional space. By utilising 2D ultrasonic transducer arrays, producing 3D volumetric images, the bubbles can be accurately tracked in blood steam. If the signals contributed from all the tracked bubbles are combined, a 3D map of the vascular network of organs can be generated and used for diagnostic imaging of vascular diseases and for spotting the onset of malicious tumours.

1.6 This PhD project

In this thesis is presented the culmination of the research, design processing, fabrication, and characterisation performed in this PhD project.

This PhD project thesis is split into two parts. In Part I a hand-held RCA CMUT based probe for volumetric imaging with a potential use in medical applications is treated in detail. This probe uses a generation of RCA CMUT chips called *transducer rodent 2* (TR2) based on a previous *transducer rodent 1* (TR1) chip, presented in the PhD thesis by Andreas Spandet Havreland [82]. These chips mounted in the probe were meant to be used for clinical pre-trials on rats before later clinical trials are to be performed on humans, using either this probe or another generation of chips. This device is based on a LOCOS process fabricated on a doped silicon wafer. The elements are made in a combination with fusion bonding to an SOI wafer and a physical separation of the bottom electrodes to reduce cross-talk between the elements, which was presented by the author in [80]. This is realised using a deep reactive-ion etching (RIE) based process. For improved mechanical stability, while also providing element-to-element insulation and low capacitive substrate coupling, a borofloat glass wafer is anodically bonded to the backside of the elements after the separation process. The separated electrodes have a cross-section of almost $100 \times 100\,\mu m^2$ which combined with a highly doped silicon substrate will mitigate delay-line effects.

The various aspects of the probe development, e.g. the chip design and fabrication, the probe electronics and probe handle and the imaging techniques, was done in a collaboration between the company BK Medical ApS and their ultrasound probe development department and the research groups at DTU: the Center for Fast Ultrasound Imaging (CFU) and the MEMS-Applied Sensors group at DTU Health Technology, which the author of this thesis is a part of. The fusion-anodic double bonded structure is illustrated in Fig. 1.4(e) and as a cross-sectioned 3D sketch in Fig. 1.5. This device should benefit from stable high-performing CMUTs while also exhibiting low element-to-element coupling and high transmit pressure uniformity.

In Part II a hand-held RCA CMUT based prototype probe is presented and the design, development, fabrication and characterisation of the *transducer human 1* (TH1) generation of RCA CMUT chips are treated in detail. The design of these are based on previous anodically bonded arrays from the PhD projects of Mathias Engholm [83] and Andreas Spandet Havreland [82] and the Masters'

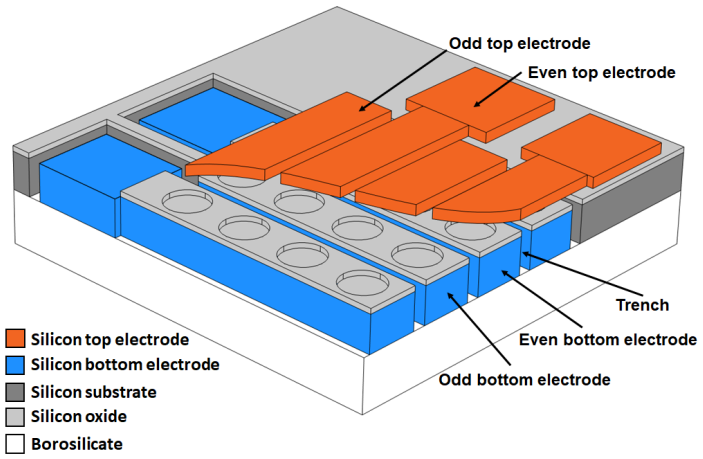


Figure 1.5: A 3D sketch of the corner of an RCA array made using the fusion-anodic double bonded method. The orthogonal blue bottom electrodes and orange top electrodes, made of silicon, are shown encapsulating the structured oxide layer with the circular CMUT cells. A wide trench is shown separating the bottom electrodes laterally, and a glass substrate (borosilicate) is shown bonded to the backside of the structure.

projects by Kitty Steenberg [84] and Magnus Galsgård Petersen [85]. The anodic bonded structure is illustrated in Fig. 1.4(d) and a previously fabricated structure is presented in [55]. This device uses a substrate made of borosilicate glass to reduce substrate coupling or cross-talk between the elements. The top electrode and plate will be made of poly-silicon covered by aluminium, and will be insulated from short circuits in the cell cavities with a silicon nitride layer, as illustrated in Fig. 1.4(d). The bottom electrodes will be made of metal which will mitigate delay-line effects. In [55] an improvement to the design is made, which makes it possible to reliably perform wafer level characterisation on the arrays in air without the need for insulating encapsulation material. This is done by extending the silicon layer to the edge of the bottom electrode contact pad.

This TH1 chip in the prototype probe is made in collaboration with the same partners in the SRI project and was also meant to be used first for clinical pre-trials on rats before later clinical trials are to be performed on humans.

1.7 Publications

This thesis is partly based on the following publications of which the author is either a main or co-author. These publications are: four IEEE IUS conference proceedings and one journal article published in special issue on micromachined ultrasonic transducers in the IEEE OJUFFC.

Paper A Rune Sixten Grass, Andreas Spandet Havreland, Mathias Engholm, Jørgen Arendt Jensen and Erik Vilain Thomsen, "188+188 Row–Column Addressed CMUT Transducer for Super Resolution Imaging," in *Proc. IEEE Ultrason. Symp.*, IEEE, 2019, pp. 746–749.

Paper B Erik Vilain Thomsen, Kitty Steenberg, Magnus Galsgård Petersen, Mads Weile, Andreas Havreland, Martin Lind Ommen, Rune Sixten Grass, and Mathias Engholm., "Wafer Level Characterization of Row-Column Addressed CMUT Arrays," in *Proc. IEEE Ultrason. Symp.*, IEEE, 2019, pp. 770-773.

Paper C Andreas S. Havreland, Mathias Engholm, Rune S. Grass, Jørgen A. Jensen, and Erik V. Thomsen. Wafer bonded CMUT technology utilizing a poly-silicon-on-insulator wafer. In *Proc. IEEE Ultrason. Symp.*, pages 758–761. IEEE, 2019.

Paper D Rune Sixten Grass, Kitty Steenberg, Andreas Spandet Havreland, Mathias Engholm and Erik Vilain Thomsen, "Large Scale High Voltage 192+192 Row-Column Addressed CMUTs Made with Anodic Bonding," in *Proc. IEEE Ultrason. Symp.*, IEEE, 2020, pp. 1–4.

Paper E R. S. Grass, M. Engholm, A. S. Havreland, C. Beers, M. L. Ommen, S. L. G. Pedersen, L. N. Moesner, M. B. Stuart, M. T. Bhatti, B. G. Tomov, J. A. Jensen, and E. V. Thomsen, "A Hand-Held 190+190 Row–Column Addressed CMUT Probe for Volumetric Imaging," *Submitted for review in IEEE Open J. Ultrason., Ferroelec., Freq. Contr. in a special edition on micromachined ultrasonic transducers*, 2022.

1.8 Thesis outline

This thesis is divided into three introductory chapters, followed by two parts detailing the design, fabrication, assembly and electrical and acoustical characterisation of two TR2 and TH1 probes. The two parts each consist of three chapters consists. Finally a conclusion is given.

A description of each chapter is given

Chapter 1 - Introduction This chapter provides an introduction to the background of medical ultrasound imaging and a few of the different modalities used when scanning patients. An introduction the the CMUT as a platform for ultrasound imaging is given together with a brief literature study and a view into the state-of-the-art of arrays and probes. The benefits of using 2D CMUT row-column arrays for 3D imaging are discussed. Furthermore, criteria for large CMUT arrays regarding the electrode resistance and substrate coupling in relation to the choice of bottom electrode material are discussed. The CMUT designs chosen for this PhD thesis are then justified and details of the research project is given. These two designs are; 1) a LOCOS based CMUT design, which combines highly doped silicon electrodes with low resistivity, a fusion bonding process for cell encapsulation and an anodically bonded glass substrate for reduced capacitive substrate coupling. 2) a glass based substrate with etched CMUT cavities, using anodic bonding for cell encapsulation, and metal electrodes with low resistivity.

Chapter 2 - CMUT RC design This chapter presents a method for designing CMUT devices using a combination of analytical expressions and simulations using finite element method (FEM) software. Starting from the desired center frequency of the CMUT device in immersion, the element pitch, cell geometry, center frequency in vacuum, and electrical parameters used in operation can be modelled. The predicted signal attenuation of long elements can also be evaluated based on the electrode resistance and the value of the dimensionless ωRC product, and can used be used in an iterative design process to optimise electrical and acoustical performance.

Chapter 3 - Wafer level characterisation This chapter shows the methodology of the various electrical tests performed on CMUT arrays using an automatic wafer probing station. The purpose of each test in the performance evaluation of the array is described.

Part 1 - LOCOS-based CMUTs - Transducer Rodent 2 (TR2)
This part treats the development of the Transducer Rodent 2 (TR2) probe

Chapter 4 - Design In this chapter the TR2 CMUT design considerations are presented. These are based on the CMUT RC design method in Chapter 2. The geometry of the CMUT cell and center frequency were determined from the center frequency in immersion. The Bragg and substrate ringing frequencies were found and the estimated signal attenuation of the transmitting elements were calculated based on the ωRC product. Changes to the design were briefly discussed and the array and wafer layout presented.

Chapter 5 - Fabrication This chapter provides a detailed overview of the fabrication process for the TR2 chip and its main steps. Various process recipes and parameters are listed for each step. The fusion and anodic bonding processes and their mechanisms are briefly discussed.

Chapter 6 - Transducer characterisation The chapter describes the characterisation of the TR2 chip and probe. The fabricated TR2 chip is first electrically characterised before it is mounted in the probe handle. This involves impedance measurements and pull-in tests. The probe assembly process is described and details are provided when available. Then the performance of the probe is evaluated by acoustical characterisation. This involves performing measurements in transmit, by receiving the probe signal with a hydrophone, and in pulse-echo, by using the probe in both transmit and receive with a reflector plate. A short thermal characterisation of the probe is also given. In addition the 3D volumetric capabilities and resolution of the probe is evaluated by scanning on three different phantoms.

Part 2 - Anodic bonding based CMUTs - Transducer Human 1 (TH1)
This part treats the development of the Transducers Human 1 (TH1) probe

Chapter 7 - Design In this chapter the TH1 CMUT design consideration are presented. Specifically the TH1-A array generation is presented. An iteration of the TH1-A design, based on its fabrication results, called the TH1-B design, is included in Appendix A. The design process is based on the CMUT RC design method in Chapter 2. The geometry of the CMUT cell and center frequency were determined from the center frequency in immersion. The Bragg and substrate ringing frequencies were found and the estimated signal attenuation of the transmitting elements were calculated based on the ωRC product. Changes to the design were briefly discussed and the array and wafer layout presented.

Chapter 8 - Fabrication This chapter provides a detailed overview of the fabrication process of the TH1-A chip and its main steps. Various process recipes and parameters are given for each step. A list summarising which processes that need optimisation is presented. Some of these have been implemented in the fabrication of the TH1-B chip described in Section A.2.

Chapter 9 - Transducer characterisation The chapter describes the characterisation of the TH1 chip and the prototype probe. The fabricated TH1 chip is first electrically characterised before it is mounted in the probe handle. This involves, IV, CV, and impedance measurements and pull-in tests. The probe assembly process is described and details are provided when available. Then the performance of the probe is evaluated by acoustical characterisation. This involves performing measurements in transmit, by receiving the probe signal with a hydrophone, and in pulse-echo, by using the probe in both transmit and receive with a reflector plate.

Chapter 10 - Conclusion and outlook An overall conclusion is given, summarising some of the important results of the development of the two large row-column probes and the challenges lying ahead.

Chapter **2**

CMUT RC design

2.1 Determining CMUT design parameters

The task of designing a CMUT array layout from the bottom is a process that involves numerous steps and choices pertaining to the purpose of the transducing array, the tools and trade-offs when designing, and the fabrication process and materials used. Both analytical expressions and FEM based simulation software are viable tools which demonstrates high conformity. All the design parameters can be found by completely relying on the analytical expressions presented, however, the equations used for finding the plate thickness relies on the deflection model for thin single layer plates. Several previously presented arrays in this research group [82], [83], [86] can be categorised as being close or belonging to the category of thick plates. The thin plate models will therefore by subject to a certain degree of uncertainty. The complicated full models incorporating both thin and thick plate regimes, used when deriving the resonance frequency by the Rayleigh-Ritz method, will not be derived/presented here. This is a subject currently under investigation in our group to improve the accuracy of the analytical model for a wide range of plates. Instead, the parameters found from the models presented will as a part of the design process by used as a starting guess for the FEM simulation tools. In this way the effects not completely described by the analytical models are accounted for in the final parameter set obtained through simulation. The specific FEM tools used in this group are the COMSOL Multiphysics software (COMSOL AB, Sweden) [87] and OnScale Computer-Aided Engineering (OnScale, USA) (formerly known as PZFlex). The author of this PhD thesis has only worked with COMSOL which will be the tool used to determine the final design parameters.

The most important steps involved in the design process are listed below, and these will each be further elaborated in the following sections

- Center frequency in immersion and number of elements
- Element pitch
- CMUT Cell layout and bonding area
- Plate thickness
- Operating voltage - 80% to 90% of the pull-in voltage
- Gap and pull-in voltage
- Finite element modelling
- Bragg frequency, substrate ringing and modes

Table 2.1: Table of approximate attenuation values for the human body from [88]

Tissue	Attenuation [dB/MHz·cm]
Liver	$0.6 - 0.9$
Kidney	$0.8 - 1.0$
Spleen	$0.5 - 1.0$
Fat	$1.0 - 2.0$
Blood	$0.17 - 0.24$
Plasma	0.001
Bone	$16.0 - 23.0$

- Electrode resistance (pressure uniformity) - ωRC
- Method of fabrication based on electrode design and style

2.1.1 Frequency and size of the array

The first design choice used in defining the transducer array is the center frequency in immersion. As was briefly mentioned in the introduction the center frequency is chosen according to the penetration or image focusing depth, and the resolution required for the application. When performing medical ultrasound imaging, the human body is the medium of interest, or rather the human body tissue is the medium. The speed of sound in the soft tissue for imaging is generally accepted to be around $1540\,\mathrm{m\,s^{-1}}$. This value, however, depends on the type of tissue and type of organ and will vary depending on the tissue density. If a material, such as bone, with a high density is imaged the speed of sound can be several factors higher than surrounding soft tissue.
The propagating wave itself will also be attenuated due to scattering and absorption in the tissue [88]. Approximate values of attenuation is given in Table 2.1. These demonstrate that the attenuation of an ultrasonic wave will be more pronounced with increasing frequency, the imaging depth and the type of organ. A backscattered 5 MHz wave which makes a round-trip in an organ, e.g. the kidney, at a depth of 7 cm, will experience an attenuation of $5\,\mathrm{MHz} \times 2 \times 7\,\mathrm{cm} \times 0.8\,\mathrm{dB\,MHz^{-1}\,cm^{-1}} = 56\,\mathrm{dB}$.

The center frequency and the number of elements in the array are directly linked to the possible spatial resolution of the transducer. The resolution is determined ultimately by the size of the point spread function (PSF) of the system, and can be quantified by the axial and lateral resolutions. The axial resolution, also called the longitudinal resolution (the z-direction perpendicular to the transducer surface), is determined by the wavelength of the ultrasonic wave or pulse. This describes the smallest resolvable object size in the axial-direction. If a 5 MHz wave is used, the wavelength will be $\lambda = 1540\,\mathrm{m\,s^{-1}}/(5 \times 10^6\,\mathrm{s^{-1}}) = 0.308\,\mathrm{mm} = 308\,\mu\mathrm{m}$. The axial resolution of a pulsed signal, d_{ax}, can be found from the wavelength and the pulse cycle number, M, as following [89]

$$d_{\mathrm{ax}} = \frac{M}{f_0}\frac{c}{2} = \frac{M}{2}\lambda \tag{2.1}$$

where M is usually set to 2 or 1-3, giving resolutions comparable to λ. It follows that a shorter pulse increase the resolution.

The lateral resolution at a focus point in the x-y plane (parallel to the transducer surface) can determined by considering the size of the PSF of a scatterer or its full-width-half-maximum (FWHM), measured at $-6\,\mathrm{dB}$

$$FWHM = \lambda\frac{R}{2r} = \lambda F_{\#} \tag{2.2}$$

$$F_{\#} = \frac{R}{2r} = \frac{F}{D} \tag{2.3}$$

where $2r$ or D is the width or aperture of the array if the full array is used. $F_{\#}$ is the F-number which is typically between 1-5 and F is the distance to the focal point or focal plane. If a sub-aperture is

used for synthetic aperture (SA) the resolution at specific focal depths can be changed by adjusting the width. The full width is of course determined by the number of elements and their width, which includes the individual cell size and bonding area, and the kerf or distance between the elements. This is also referred to as the element pitch.

2.1.2 Element pitch

A periodicity of half the wavelength ($\lambda/2$) is usually chosen as the element pitch. This due to the wave diffraction happening as a result of the periodic nature of the array elements. This effect manifest as image artefacts in the form of grating lobes. These lobes appear as ghost echoes of off-axis objects, which will be superimposed on the desired image and the quality and image contrast will likely be reduced. These grating lobes appear at specific angles where constructive interference is achieved. If we refer to the formula used for diffraction

$$\theta_m = \arcsin\left(\frac{m\lambda}{p}\right) \tag{2.4}$$

$m = \pm 1, \pm 2, ... \pm n$ refer to the (grating) lobe number, λ wavelength, p periodicity and θ the angle of the lobe when plotted according to directivity [11]. A main lobe will appear when $m \neq 0$ perpendicular to the transducer surface containing most of the transmitted energy. If a period of $p \leq \lambda/2$ is used the grating lobes (side-lobes beside the main lobe) appear at $\pm\pi/2$ and are avoided.

A realistic example of a $\lambda/2$ pitch could for a 10 MHz transducer be

$$\lambda = \frac{1540\,\mathrm{m\,s^{-1}}}{10 \times 10^6\,\mathrm{s^{-1}}} = 0.154\,\mathrm{mm} = 154\,\mu\mathrm{m} \tag{2.5}$$

$$p = \frac{\lambda}{2} = \frac{154\,\mu\mathrm{m}}{2} = 77\,\mu\mathrm{m} \tag{2.6}$$

2.1.3 Cell layout

With the element pitch set, the next task is then choosing a cell layout. Commonly each sub-element or unit cell is either made up of a single CMUT capacitor cell or a grid of two, four or more cells, as shown in Fig. 2.2.

An upper limit on the size of the cells, which can fit in an element width, could naïvely be set to $\lambda/2$ for one cell and $\lambda/4$ if two cells are used. If the cells are closely packed in a square grid this is almost possible, as illustrated by the Tabla I-III (1D array, 128 elements) design in Fig. 2.2 with 5 cell across the element. However, as mentioned before, included in the pitch is also the kerf separating the elements, d_{kerf}, and the bonding area, or length in this case, d_{bond}, which constitutes all the area in the element not taken up by the cells.

It is in the best interest to pack the cells as close as possible to increase the active area and therefore also the pressure generated. There is a trade-off between the pressure, the acoustical transmit and pulse-echo sensitivity, and the bandwidth. A higher cell radius has been shown to increase the aforementioned factors but lower the bandwidth, and likewise, lowering the cell radius and the plate thickness to keep the same frequency will, increase the bandwidth but lower the output pressure and sensitivities. The packing or fill factor, F, can be adjusted to accommodate the most cells. The design with the highest number of cells being the hexagonal close packed (HCP) scheme, also illustrated in Fig. 2.2 for Tabla IV (1D, 128 elements) ,V-VI and HF (1D, 192 elements), with a fill factor of

$$F_{\mathrm{HCP}} = \frac{A_{\mathrm{circle}}}{A_{\mathrm{Hex,unit}}} = \frac{2\pi a^2/4}{\sqrt{3}a^2} = \frac{\pi}{2\sqrt{3}} \approx 0.907 \tag{2.7}$$

if the circles are touching. Here a is the radius of the circular cells with the nominator being the area of 2 quarters of a circular cell and the denominator the area of the rectangular unit cell of the

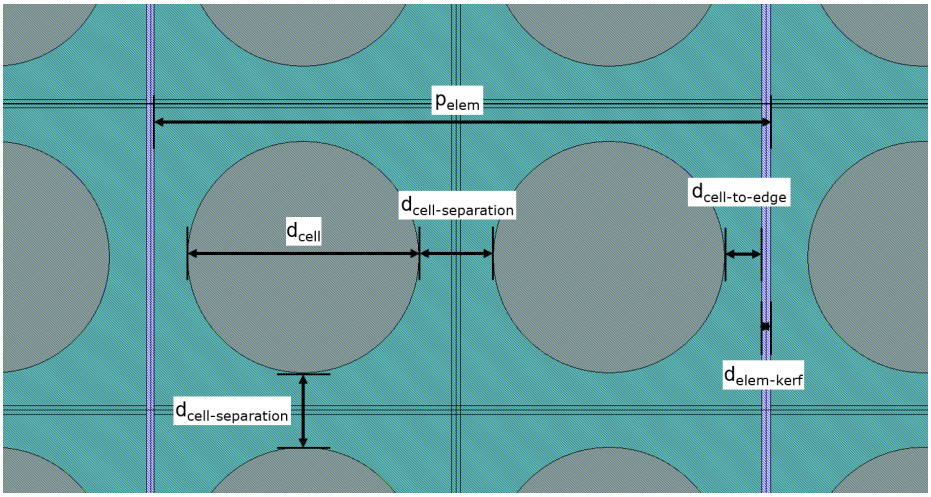


Figure 2.1: Illustrations of a mask layout demonstrating a two-cell element layout. The cells are arranged in a square grid and the layout dimensions are labelled according to Eq. 2.9.

hexagon with side lengths a and $\sqrt{3}a$. In comparison circular cells packed in a regular square grid will have a maximum fill factor of

$$F_{\text{square}} = \frac{2\pi a^2/4}{a^2} = \frac{\pi}{4} \approx 0.785 \tag{2.8}$$

with $2\pi a^2/4$ being a quarter of a cell fitting inside a square unit cell of a^2.

In this project circular cells packed in a square grid and square cells packed in a square grid have been used. These will be presented in the later design chapters of the TR2 and TH1 arrays in Chapter 4 and Chapter 7.

Taking the example from before, using a square grid with either circular or square cells the pitch can be expressed as following

$$p_{\text{elem}} = n\, d_{\text{cell}} + d_{\text{elem-kerf}} + (n-1)\, d_{\text{cell-separation}} + 2\, d_{\text{cell-to-edge}} \tag{2.9}$$

where d_{cell} is the cell diameter, $d_{\text{elem-kerf}}$ is the kerf separating the elements, $(n-1)\, d_{\text{cell-separation}}$ is the total cell separation distance of n number of cells side by side, and $d_{\text{cell-to-edge}}$ is the distance from the clamping edge of the cell to the edge of the element kerf. These dimensions are illustrated in the cell layout inFig. 2.1.

Drawing a line across the element straight through the cell, $d_{\text{cell-to-edge}}$ and half of the $d_{\text{cell-separation}}$ will be the bonding length available to the cell. The choice of how much of the area that will be used for bonding is based on trial and error of the previous successfully fabricated arrays.

A possible restraint on the minimum bonding distance is tied to how we consider the plate to be clamped to the cell wall. This was presented in [90]. The standard analytical solution for the pull-in voltage of a circular plate, which will be shown further down in Section 2.1.5, assumes that the plate is only clamped at the edge of the cell and does not take into account the stress distributed into the bonding region between the cells. This effect is not fully understood yet, but a heuristic model was proposed where the effective radius is replacing the radius in the pull-in model. This is defined as $a_{eff} = a + c\,h$, where a is the actual cell radius, h is the plate thickness and c is a fitted constant which depends on the geometry of the cell at the clamping point. The constant c was found to be around 0.62 showing a good fit with FEM simulations for an inverse aspect ratio h/a below around 0.1. This effectively means that the plate will appear softer than expected if $a_{eff} = a$ is assumed,

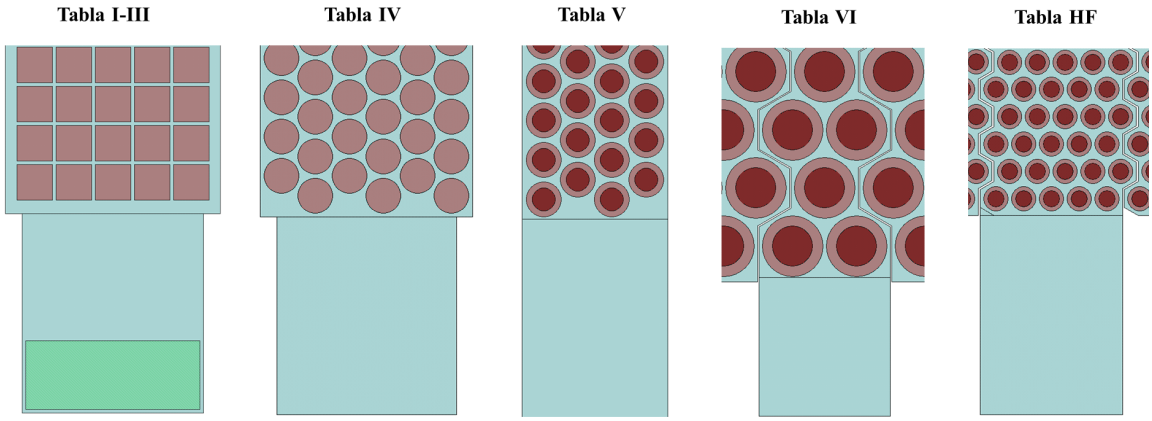


Figure 2.2: Illustrations of the mask layouts used for fabricating the linear Tabla CMUT arrays presented in [86]. Different cell packing schemes are demonstrated. For Tabla I-III a close packing optimal for square cells is used. Tabla IV and V used a type of HCP scheme. For Tabla VI and Tabla HF a type of interwoven HCP configuration is used where the elements overlap and the cell count either varies or is kept constant along the length of the element.

lowering the resonance frequency, and that the bonding length should at least be $c\,h = 0.62\,h$. This entails that the cell separation distance and distance from the cell to the edge of the kerf should be

$$d_{\text{cell-separation}} \geq 0.62\,h, \qquad d_{\text{cell-to-edge}} \geq 0.62\,h. \tag{2.10}$$

For an element pitch of $p = 77\,\mu\text{m}$ and a kerf of e.g. $4\,\mu\text{m}$ and by setting the edge distance equal to the cell separation, Eq. 2.9 becomes

$$77 = n\,d_{\text{cell}} + 4 + (((n-1)+2))\,d_{\text{cell-separation}} \tag{2.11}$$

$$d_{\text{cell}} \leq \frac{77 - 4 - (((n-1)+2))\,d_{\text{cell-separation}}}{n} = \frac{73 - (n+1)\,0.62\,h}{n}. \tag{2.12}$$

For a $3\,\mu\text{m}$ thick plate, this would give a maximum cell diameter as

$$d_{\text{cell}} \leq \frac{73 - (n+1)\,1.86}{n} \tag{2.13}$$

and for the case of one or two cells

$$d_{\text{cell}} \leq \begin{cases} 69.28 & \text{for } n = 1 \\ 33.71 & \text{for } n = 2 \end{cases}. \tag{2.14}$$

2.1.4 Plate thickness

The next task when designing the CMUT is relating the chosen operating frequency in immersion and the cell geometry to the plate material and thickness. The CMUT has a different operating frequency in immersion, in e.g. water or oil, due to the density of surrounding medium. This is described as an added effective mass to the plate given by the imaginary part of the radiation impedance of the system.

The resonance frequency in immersion is described by Lamb [91], using the Rayleigh-Ritz method, and by calculating the kinetic and potential energy of a thin vibrating plate clamped firmly along its circumference with water on one side.

This gives a relation between ω_r and ω_0, which are the resonance frequencies in the medium e.g. water and in vacuum or air, respectively, as

$$\omega_r = \omega_0 \frac{1}{\sqrt{1+\beta}} = \omega_0 \frac{1}{\sqrt{1+\Gamma \frac{a}{h}\frac{\rho_m}{\rho_p}}}. \tag{2.15}$$

β is the added virtual mass incremental factor (AVMI), consisting of the plate radius to plate thickness ratio, a/h and the ratio between the densities of the medium and the plate, ρ_m/ρ_p. Γ is known as the non-dimensionalised added virtual mass incremental factor (NAVMI) and is highly dependent on the clamping conditions of the plate to the cell cavity. The expression is valid for thin plates, which can be categorised as $8 \ldots 10 \leq a/h \leq 80 \ldots 100$ [92], or using the inverse aspect ratio, thin plates are $\approx h/a < 0.1$. The value stated by Lamb is $\Gamma = 0.6689$. From this model, it can be surmised that the value of $\Gamma a = h_w$ represents a plate of some medium, e.g. water, with the thickness h_w. This medium has the density described by the value of ρ_m. This plate or disc of water moves together with the plate of the transducer as an added mass.
It can be seen from the equation that the factor multiplied by the resonance in vacuum ω_0 will always be smaller than 1 due to the virtual mass added in the denominator. The ratio ω_r/ω_0 will give a reduced resonance frequency in the medium compared to vacuum.

The resonance frequency in air or vacuum can be found directly from the Rayleigh-Ritz equation by calculating the Rayleigh quotient $Ra = \omega_0^2$ for a clamped circular plate as

$$\omega_0 = 10.328\sqrt{\frac{D}{a^4 h \rho_p}} = 10.328\sqrt{\frac{Y}{12\left(1-\nu^2\right)\rho_p}}\frac{h}{a^2} \tag{2.16}$$

$$D = \frac{h^3 Y}{12\left(1-\nu^2\right)}$$

where D is the plate stiffness or the flexural rigidity, Y is Young's modulus and ν is Poisson's ratio of the plate material. ν usually takes the value of $0.28 - 0.30$ in the [100] direction for silicon plates but a mean value of the [100] and [110] direction is often used 0.177 [93]. A mean value for Young's modulus is taken as 148 GPa.

The Rayleigh quotient from Eq. (2.16) can now be combined with Eq. (2.15) to arrive at an expression for the frequency in immersion

$$\omega_r \sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}} = 10.328\sqrt{\frac{Y}{12\left(1-\nu^2\right)\rho_p}}\frac{h}{a^2}. \tag{2.17}$$

From this the thickness, h, can be isolated and found as the solution to a third order polynomial

$$\omega_r^2\left(1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}\right) = (10.328)^2\frac{Y}{12\left(1-\nu^2\right)\rho_p}\frac{h^2}{a^4}$$
$$(10.328)^2\frac{Y}{12\left(1-\nu^2\right)\rho_p}\frac{h^3}{a^4} - \omega_r^2 h - \omega_r^2 \Gamma a \frac{\rho_m}{\rho_p} = 0.$$

For a CMUT array with a resonance frequency in immersion of $\omega_r = 10$ MHz, a cell radius of $a = 30$ µm, a plate density of $\rho_p = 2.330\,\mathrm{g\,cm^{-3}}$ for silicon, a Poisson's ratio of 0.177, $Y = 148$ GPa, $\Gamma = 0.6689$, and a medium with the density of $\rho_m = 1.259\,\mathrm{g\,cm^{-3}}$ (corresponding to a silicone layer on the op the array [94]), the plate thickness becomes

$$h = 4.37\,\mu\mathrm{m}. \tag{2.18}$$

The plate aspect ratio is $a/h = 6.86$ or $h/a = 0.15$, just placing it in the category of thick plates.

The reduction in the resonance frequency from vacuum is for this case

$$\frac{\omega_r}{\omega_0} = 0.54 \tag{2.19}$$

where the vacuum frequency for this example would be 18.5 MHz.

2.1.5 Gap and pull-in voltage

The plate thickness is now set, and the obtained value is assumed to be reasonable and feasible to fabricate in the cleanroom. The gap of the CMUT can now be determined either analytically or through simulations. The value is governed by the operating voltage, V_{DC}, which will be set as the DC bias on the CMUT. The CMUTs in the MEMS Applied Sensors group and in this thesis are usually operated between 80 % and 90 % of the pull-in voltage, V_{pi}.

Depending on the CMUT structure the cavity or gap, g, between the bottom and top electrode will likely be an effective gap, g_{eff}. This is an expression of the summation of the various dielectric layers in the gap or in the plate, between the top and bottom electrode. This can be written as

$$g_{\text{eff}} = g + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \tag{2.20}$$

$$g_{\text{eff}} = \sum_{n=1}^{N} \frac{t_n}{\epsilon_n} \tag{2.21}$$

and the capacitance found for a simple multilayer parallel plate capacitor as

$$C_{t0} = \left(\frac{1}{C_{\text{vac}}} + \frac{1}{C_{\text{dielec}}} \right)^{-1} = \frac{\epsilon_0 A}{g_{\text{eff}}} \tag{2.22}$$

where g is the vacuum gap, A is the plate area, t_{ox} is the thickness of the oxide or intermediate layer. ϵ_n and ϵ_{ox} are the vacuum permittivity and permittivity of the oxide or medium of the layer.

When the plate of the CMUT is deflected with an applied bias voltage the gap decreases, due to the electrostatic force, which will be explained in Chapter 3. The plate deflection, $w(r)$, will depend on the radial distance r from the center of the plate, which can be derived from the isotropic plate equation for a circular clamped plate in a situation of pure bending [95] by

$$w(r) = w_0 \left[1 - \left(\frac{r}{a} \right)^2 \right]^2, \qquad w_0 = \frac{pa^4}{64D} \tag{2.23}$$

with w_0 being the center deflection for a circular plate with radius a, p the pressure difference across the plate, and D the flexural rigidity. A simple way to introduce deflection to the plate capacitance can be

$$C_{\text{plate}} = \frac{\epsilon_0 A}{g_{\text{eff}} - w(r)}. \tag{2.24}$$

The total capacitance can the calculated by integrating the plate area

$$C_t = \int_{A_{\text{plate}}} dA \tag{2.25}$$

which for a parallel plate is given by [93]

$$C_{t,parallel} = C_{t0} \frac{1}{1 - \eta} \tag{2.26}$$

where $\eta = \frac{w_0}{g_{\text{eff}}}$ is the normalized center deflection. Likewise the capacitance for the circular clamped plate is given by

$$C_{t,circ} = C_{t0}\sqrt{\frac{1}{\eta}}\operatorname{arctanh}\sqrt{\eta}. \tag{2.27}$$

The square plate does not have an analytical solution to the capacitance and can instead be found numerically. However, a second order polynomial written in the same form as the capacitance for the parallel plate can be used as an estimate, valid for relative center deflections between $\eta = 0$ to 0.5,

$$C_{t,square} = C_{t0}\frac{1}{1 - 0.296\eta - 0.136\eta^2}. \tag{2.28}$$

Knowing the capacitance of the system, the deflection at pull-in and the pull-in voltage can be found from the potential energy considerations of the system, which is derived in Chapter 3. The pull-in voltage is defined as the point where the effective spring constant of the CMUT capacitor becomes zero, when the electrostatic pulling force and the spring constant balances. It this unstable point the plate deflection increases drastically and it collapses to the bottom of the cavity.

The general expression for the pull-in voltage V_{pi} becomes

$$V_{\text{pi}} = \sqrt{\frac{2k_0}{C''(w_{\text{pi}})}} \tag{2.29}$$

and the deflection at which pull-in occurs, w_{pi}, can be found as

$$w_{\text{pi}} = \frac{C'(w_{\text{pi}})}{C''(w_{\text{pi}})} + pA_{\text{eff}} \tag{2.30}$$

where k_0 is the spring constant of the plate, C' and C'' are the derivatives of the CMUT capacitance with respect to the plate deflection w, p the atmospheric pressure on the CMUT plate and A_{eff} the effective area of the plate.

From the article [93] by Mette Funding la Cour from this research group, the pull-in voltage and deflection for a parallel plate capacitor is given as

$$V_{\text{pi,p}} = \sqrt{\frac{k_0}{C''(w_{\text{pi}})}} = \sqrt{\frac{k_0(g_{\text{eff}} - w(r)^3)}{2\epsilon_0 A}} = \sqrt{\frac{8k_0 g^3}{27\epsilon_0 A}} \tag{2.31}$$

$$w_{\text{pi,p}} = 1/3\, g_{\text{eff}}. \tag{2.32}$$

The pull-in voltage and deflection at pull-in is likewise given for a circular cell design as

$$V_{\text{pi,circ}} = \sqrt{\frac{89.4459 D g_{\text{eff}}^2}{a^2 C_{t0}}} = \sqrt{\frac{89.4459 D g_{\text{eff}}^3}{a^4 \epsilon_0 \pi}} = \sqrt{\frac{89.4459 Y\, h^3 g_{\text{eff}}^3}{12\,(1-\nu^2)\, a^4 \epsilon_0 \pi}} \tag{2.33}$$

$$w_{\text{pi,circ}} = \frac{C'(w_{\text{pi}})}{C''(w_{\text{pi}})} + pA_{\text{eff}} = 0.463\, g_{\text{eff}}, \tag{2.34}$$

and for a square cell as

$$V_{\text{pi,square}} = \sqrt{\frac{2.95118\, g_{\text{eff}}^2\, h^3 \xi_s}{C_{t0}\, L^2}} = \sqrt{\frac{2.95118\, g_{\text{eff}}^3\, h^3 \xi_s}{a^2\, \epsilon_0 L^2}} \tag{2.35}$$

$$w_{\text{pi,square}} = \frac{C'(w_{\text{pi}})}{C''(w_{\text{pi}})} + pA_{\text{eff}} \tag{2.36}$$

with the constant $\xi_s = 385.637\,\text{GPa}$ and L being the side length of the square.

From that equation we see that V_{pi} scales as $\propto \sqrt{g^3}$ both for the simple parallel plate capacitor and for circular plates with radius a. Isolating for g_{eff} gives Eq. 2.37 which can be used to directly calculate the gap height or effective gap height of the CMUT to find the theoretical C_{t0} capacitance of the unbiased CMUT cell. This equation can also be used for square plates as the deviation between the two model is small for relative small plate deflections [93], e.g. a relative deflection of $\eta = w_0/g_{\text{eff}} = 0.4$ results in a deviation of 1.4 %.

$$g_{\text{eff}} = \sqrt[3]{\frac{V_{\text{pi,circ}}^2\, a^4 \epsilon_0 \pi}{89.4459 D}} \tag{2.37}$$

Taking the example from before with $h = 4.37\,\mu\text{m}$ and by choosing $V_{pi,circ} = 200\,\text{V}$ the effective gap comes to be $g_{\text{eff}} = 205\,\text{nm}$, which depending on the dielectric layers is a reasonable size, which is also feasible to fabricate in the cleanroom.

2.1.6 Finite element modelling

At this point with most of the geometric dimensions calculated, the FEM tool can be used to find the pull-in voltage, cavity gap and plate thickness for the array based on the design parameters calculated in this chapter. This is an iterative simulation process where the desired geometry of the CMUT is adjusted, while e.g. the pull-in voltage or plate thickness is fixed. This is repeated until the extracted biased or unbiased resonance frequency is at the desired value. The COMSOL model used to simulate the CMUT cells and the MATLAB scripts used to execute it are described below.

Usually a single CMUT cell is simulated in 2D or 3D as an axisymmetric half-cell or quarter cell. The 2D hall-cell model is usually used as this is the least computationally demanding model, and gives results similar or equal to the corresponding 3D model.

The physics modules used in these models are the Solid Mechanics and the Electrostatics modules, which are used to simulate the deflection and resonance frequency of the plate with a set bias voltage. A MATLAB script has been developed in this group in which the CMUT geometry and parameters relevant for the simulation can be set. Briefly presented below is a list of available studies that can be toggled in the script, which each will then be executed through COMSOL and the relevant parameters extracted. The model can be saved for inspection in COMSOL.

Studies:

- *Stat_atmP* - Calculates the plate deflection at atmospheric pressure
- Find_VacG - Calculates the required vacuum gap to obtain a desired V_{pi} (pull-in voltage) set earlier in the script
- *Find_Vpi* - Calculates V_{pi} from the vacuum gap set earlier in the script
- *Stat_Force* - Calculates the spring constant of the plate at zero bias voltage
- *Stat_Vdc* - Calculates the plate deflection at a given DC bias voltage
- *Stat_VdcPlusV* - Calculates the effective spring constant of at a given bias voltage
- *Eigen_0* - Calculates the unbiased eigen frequencies of the vibrating plate
- *Eigen_Vdc* - Calculates biased eigen frequencies of the vibrating plate
- *Electric_Impedance* - Calculates the electrical impedance of the CMUT in a set frequency range

The above studies can be run one after the other and will use the parameters set in the script, unless a previous study calculates the same value. For example, if Eigen_Vdc is run after Find_Vpi (both are toggled on), the DC bias voltage used will be based on the V_{pi} found during Find_Vpi and not the V_{pi} value set by the user in the script.

In the beginning of the script, all of the geometric dimensions of the CMUT cell is set, e.g., the plate thickness, the cell radius, cell-to-cell distance, and the bump radius if a double LOCOS process is used [86]. The desired V_{pi} and bias voltage is also set. The various parameters are described briefly below.

Simulation parameter

- *Mod.Basic.Dimension* - '2D axisym.' or '3D'. This will set to the model to either a 2D or 3D model
- *CMUT_Type* - 'Square' or 'Circular'. This will set the cell to either a square or circular cell. If a 2D model is used, the choice of CMUT type is irrelevant
- *Clamping* - 'Realistic' or 'Analytic'. The plate is either clamped realistically and extends into the bonding region between the cells or 'analytically' clamped at end of edge of the cavity
- *Geometry* - 'Quarter' or 'Full'. The cell will either be quarter cell or a full cell, which for this variable is only relevant for 3D
- *Cols* - The number of cells, e.g., beside each other in the same column element

CMUT dimensions

- *Plate_Radius* - [µm] Radius or half side length of cell
- *Plate_Thickness* - [µm] Thickness of silicon plate
- *Cell_Separation* - [µm] Distance from edge of one cell to the next cell in the same element
- *Isolation_Oxide* - [nm] Isolation oxide thickness in the bottom of the cavity, relevant for LOCOS base devices
- *LOCOS_Nitride* - [nm] Nitride thickness at the bottom of the cavity, relevant for LOCOS base devices
- *Plate_Nitride* - [nm] Nitride thickness at the bottom of the plate, referring to a layer of insulation nitride on the same side of the plate facing into the cavity
- *Vacuum_Oxide* - [nm] Vacuum gap height
- *Substrate_Thickness* - [µm] Substrate thickness, 2 µm is usually used as the substrate is clamped
- *Electrode_Thickness* - [nm] Aluminium electrode thickness on top of the plate
- *Top_Electrode_Ratio* - [nm] Ratio of top electrode metal/material relative to cell radius, which is relevant if a different top electrode design not completely covering the plate is used
- *Bottom_Electrode_Inner_Ratio* - Ratio of the inner bottom electrode edge relative to the cell radius, which is relevant if e.g. a ring shaped bottom electrode is used
- *Bottom_Electrode_Outer_Ratio* - Ratio of the outer bottom electrode edge relative to the cell radius, relevant if a bottom electrode smaller than the cell cavity is used in e.g. the anodically bonded design
- *Element_Edge* - [µm] Distance from the outer most cell in the element to the clamping edge, referring to the distance to the kerf from the cell
- *Stress_Nitride* - Set to 1100×10^6 Pa, is the stress in the plate nitride, where positive stress is tensile and negative is compressive
- *Stress_PolySi* - Set to -160×10^6 Pa, is the stress in the poly-Si plate, where positive stress is tensile and negative is compressive
- *Vpi* - [V] The desired pull-in voltage

- *VdcRatio* - Set to 0.8, is the DC bias as ratio of pull-in voltage

2.1.7 Bragg frequency, substrate ringing and modes

The grating lobes, occurring for an element pitch that is $> \lambda/2$, are not the only array effect found when using vibrating plates positioned in a regular grid. The cells will for all the shown cell-configurations in e.g. Fig. 2.2 exhibit multiple cell pitches. An example can be given for the cells in a hexagonal packing scheme in Tabla IV, where the nearest-neighbouring cell in the [100], [110] and [010] directions etc. have the same pitch, whereas another can be found in e.g. the [210] and [120] directions.

The cells will experience a mutual coupling effect from the pressure exerted by the neighbouring cells. By considering that the CMUTs are placed in a semi-infinite fluid medium and that they vibrate like pistons, the total radiation impedance can be shown to be a combination of the individual so-called self radiation impedance and the mutual radiation impedance.

If the CMUT is modelled as a well-known harmonic oscillator in immersion, then in the frequency domain the radiation force, $F_{\mathrm{w}}(\omega)$, from the medium acting on the plate modelled as a moving piston with velocity $V(\omega)$ is given by

$$F_{\mathrm{w}}(\omega) = Z_{\mathrm{R}}(\omega)V(\omega). \tag{2.38}$$

The value of $Z_{\mathrm{R}}(\omega)$ is the so-called mechanical radiation impedance depending on the vibrational frequency of the piston/plate and its radius. This is a complex number, which can be expressed as

$$Z_{\mathrm{R}}(\omega) = Z_{\mathrm{Rr}}(\omega) + i\, Z_{\mathrm{Ri}}(\omega) \tag{2.39}$$

where the real part,$Z_{\mathrm{Rr}}(\omega)$, is called the radiation resistance and imaginary part, $Z_{\mathrm{Ri}}(\omega)$, is called the radiation reactance. The radiation resistance is related to the emitted pressure whereas the radiation reactance is related to the fact, that the moving CMUT plate carries some water with it as an added mass, corresponding to the parameters Γa and ρ_m from Eq. 2.15.

In [96] R. L. Pritchard describes the force, f_m, from an array of N radiators, or in this case CMUT cells, on one nth cell as a sum of the so-called mutual radiation impedance Z_{nm} between the nth and mth cell and the velocity of the mth cell, V_m, given by

$$f_n = \sum_{m=1}^{N} Z_{nm} V_m \tag{2.40}$$

while Z_{nn} is the self-radiation impedance of a single nth cell, identical to $Z_{\mathrm{R}}(\omega)$ from before. The force f_n is the same as $F_{\mathrm{w}}(\omega)$ for a single cell.

The net radiation impedance on the nth cell will be

$$Z_n = \frac{f_n}{V_n} = Z_{nn} + Z_{n1}\left(\frac{V_1}{V_n}\right) + ... + Z_{nN}\left(\frac{V_N}{V_n}\right). \tag{2.41}$$

For the case of two identical cells, the equation becomes the sum of the self-radiation impedance and the mutual radiation impedance

$$Z_1 = Z_{11} + Z_{12}\left(\frac{V_2}{V_1}\right). \tag{2.42}$$

This has also investigated in [97] using simulations for a single CMUT cell with a membrane of $20 \times 20\,\mu\mathrm{m}^2$ and cells placed an array with cells spacings of 5 µm (25 µm pitch) and 25 µm (45 µm pitch). They show the effect of fluid loading lowering the center frequency compared to frequency in air. It is also seen that the coupling of the cells for the two different pitches introduces new minima in

the their plotted average membrane speed spectrum when compared to single CMUT cells. Some of these minima at around 61 MHz and 33 MHz for the 5 µm and 25 µm spacing, respectively, correspond quite well with what will be referred to as the Bragg scattering frequency below.

The mutual coupling can be described as a Bragg scattering frequency

$$f_B = \frac{c_0}{d_{\text{Cell pitch}}} \tag{2.43}$$

where c_0 is the speed of sound in the radiated medium and $d_{\text{Cell pitch}}$ being one of the cell pitches considered. This coupling will manifest as a reduction of the particle velocity $u(\omega)$ and also the radiated acoustic pressure ($p = Z_{\text{R}}(\omega)\, u(\omega)$) at the Bragg resonance frequency. It is therefore desired to choose an array design with a low cell pitch so that the resonance is at least two times the designed resonance frequency of the array. This will ensure that the effect will not interfere with the bandwidth of the CMUT, which for transducers below 10 MHz can be around 100 %.

For a design with a desired $\lambda/2$ element pitch, with only one cell across placed in a square grid, the cell distance will give a Bragg frequency of

$$f_B = \frac{c_0}{c_0/(2\, f_r)} = 2\, f_r. \tag{2.44}$$

This will place the resonance right at the edge of the presumed 100 % relative bandwidth. Several Bragg frequencies can potentially appear in the impedance spectrum of the arrays as multiple different cell pitches can be found. Larger pitches will shift the frequencies further down into the transducer bandwidth, but the cell density will be sparse and the effect minimised.

Another type of array or substrate effect is the substrate ringing, described before in [98], [99]. When the CMUT is emitting sound the wave will propagate into the medium of interest on top of the plate, but also into the cavity and the substrate. The wave will travel to the bottom of the substrate and be reflected and interfere with the main pulse used for imaging. This ringing effect can reduce the image quality and resolution by lowering the amplitude and broadening the pulse in time. This effect can be described analytically as an echo

$$T_{\text{Sub}} = \frac{2\, t_{\text{Sub}}}{c_{\text{Sub}}} \tag{2.45}$$

with T_{Sub} the echo period or round-trip in the substrate, c_{Sub} the speed of sound and t_{Sub} the substrate thickness. For a single side polished silicon wafer with a thickness of 525 µm, this would give a period of 12.45 µs and a frequency of

$$f_{\text{Si}} = \frac{c_{\text{Si}}}{2\, t_{\text{Si}}} = \frac{8433\,\text{m}\,\text{s}^{-1}}{2 \cdot 525\,\mu\text{m}} = \frac{1}{12.45\,\mu\text{s}} = 8.03\,\text{MHz}. \tag{2.46}$$

When the wave hits the interface between silicon and the backside medium, e.g air, the wave will be fully or partially reflected if the second medium has a lower acoustic impedance, which can be expressed for an arbitrary wave as the pressure reflection coefficient [100, p. 110–111]

$$R_a = \frac{Z_2 \cos\theta_i - Z_1 \cos\theta_i}{Z_2 \cos\theta_i + Z_1 \cos\theta_i} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{2.47}$$

and likewise from $1 + R = T$ the pressure transmission coefficient

$$T_a = \frac{Z_2 \cos\theta_i}{Z_2 \cos\theta_i + Z_1 \cos\theta_i} = \frac{2\, Z_2}{Z_2 + Z_1} \tag{2.48}$$

where Z_1 and Z_2 are characteristic acoustic impedance of medium 1 and medium 2, and θ_i is the incident angle of the wave on the interface which for normal incidence is zero. The phase of the

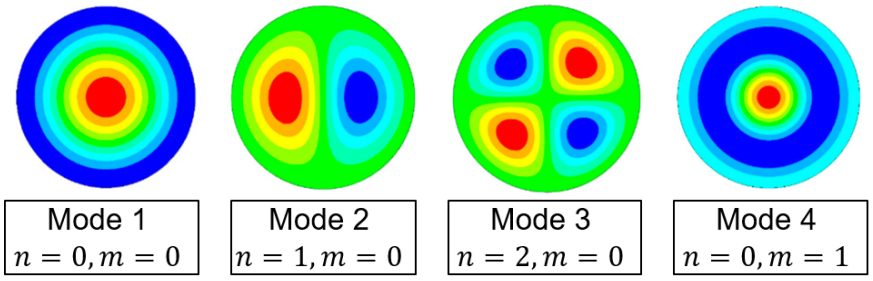


Figure 2.3: First four modes of the circular clamped plate. Modified from [102].

reflected wave will be the same as the incident is $R > 0$, whereas the reflected wave will have a phase shift of $\pi = 180°$ if $R < 0$.

The impedance can be found from the product of the density and speed of found in the material, $Z_0 = \rho_0 c_0$. In the case of air, the coefficient will be $R_a = -1$, meaning the pulse is fully reflected, and has the same amplitude as the incident wave ($|R| = 1$) and has a phase shift of π. This can create destructive interference with the transmitted CMUT pulse and reduce amplitude at f_{Si}. This can be avoided by tuning the substrate thickness or most commonly attaching a backing layer to the silicon substrate. Such a layer should have an characteristic acoustic impedance close to the main substrate and relative high attenuation (dB/MHz·cm). Adding an extra backing layer will, however, move the frequency $f_{\text{Sub,total}}$ further down, which can be expressed as

$$T_{\text{Sub,total}} = 2\left(T_{\text{Si}} + T_{\text{Sub,2}}\right) \tag{2.49}$$

$$\frac{1}{f_{\text{Sub,total}}} = \frac{2\,t_{\text{Si}}}{c_{\text{Si}}} + \frac{2\,t_{\text{Sub,2}}}{c_{\text{Sub,2}}} \tag{2.50}$$

$$f_{\text{Sub,total}} = \frac{1}{\frac{2\,t_{\text{Si}}}{c_{\text{Si}}} + \frac{2\,t_{\text{Sub,2}}}{c_{\text{Sub,2}}}} = \frac{1}{\frac{1}{f_{\text{Si}}} + \frac{1}{f_{\text{Sub,2}}}}. \tag{2.51}$$

The backing layer is introduced as a substrate thickness of $t_{\text{Sub,2}}$ and speed of sound $c_{\text{Sub,2}}$.

One other consideration when designing and operating CMUT arrays is, in which mode the vibrating plate is driven. These are found as the eigenmodes and eigenfrequencies of the plate equation of the particular plate shape. For a circular clamped plate the eigenfrequencies are given by [101]

$$\omega_{nm} = k_{nm}^2 \sqrt{\frac{D}{\rho_p\, h\, a^4}} \tag{2.52}$$

where k_{nm} is a factor found from the exact dynamic solution of the plate motion, obtained from

$$J_n(k_{nm})I_{n+1}(k_{nm}) + J_{n+1}(k_{nm})I_{n+1}(k_{nm}) = 0 \tag{2.53}$$

which is a combination of the Bessel functions, J_n, and modified Bessel functions, I_{n+1}, of the first kind. The factor k_{nm} can be found numerically and the modes are listed in Table 2.2. The first four modes for $n = 0, m = 0..3$ are illustrated in Fig. 2.3, showing the deflection of the plate. The numerical frequency values in vacuum, ω_{nm}, have been calculated for the previous example with $h = 4.37\,\mu\text{m}$ and $a = 30\,\mu\text{m}$ and are shown in Table 2.3 in [MHz].

If the driven frequency of the CMUT array is close to or at the eigenfrequency of the second mode ($\omega_{01} = 38.41\,\text{MHz}$ in air), it will transition into operating at that mode. The output pressure wave will as a result, as seen from the Fig. 2.3, be a combination of a positive and negative pressure pole, and the pressure amplitude is reduced.

An analytical model for the square clamped plate was compared to FEM simulations in [103], and was found to be between 1.3 % to 6.5 % higher than the simulated values. The modes for the square clamped plate lie close to the circular plate and the circular model will be used in this PhD thesis.

Table 2.2: Numerical values of k_{nm}^2

m \ n	0	1	2	3
0	10.22	21.26	34.88	51.04
1	39.77	60.82	84.58	111.00
2	89.10	120.10	153.80	190.30
3	158.20	199.10	242.70	289.20

Table 2.3: Numerical values of ω_{nm} [MHz]

m \ n	0	1	2	3
0	18.46	38.41	63.01	92.22
1	71.80	109.90	152.80	200.50
2	161.00	217.00	277.80	343.80
3	285.80	359.70	438.40	522.40

2.1.8 Electrode resistance

Now almost all of the geometric parameters have been locked; element pitch, number of elements, and cell radius from the resonance frequency in immersion and effective bonding area, as well as the plate thickness, pull-in voltage, cell gap and substrate thickness. These analytically calculated geometric parameters have been used in simulations to predict more accurate values. The electrode resistance which was brought up in the introduction Section 1.4.1 can now be calculated.

When a high frequency excitation AC signal is applied on a long CMUT element the electrode resistance can have significant influence on the transmit pressure uniformity. If the resistance is too high the system will behave as a low-pass filter and attenuate the applied signal along the element. This has been demonstrated in [58] for an RCA array with elements perpendicular to each other, where a fall in the measured pressure along the element is observed, and will make pressure fields more difficult to predict and compensate for in simulations and beamforming.

The voltage potential along the electrode of the CMUT can be modelled as a delay line [58]. The value of the dimensionless product ωRC, being a combination of the angular excitation frequency, ω, the element electrode resistance, R, and the total capacitance of the element, C, can be used as a criterion to minimise adverse attenuation.

The total resistance R and capacitance C of the element can be found by considering the contribution from each individual CMUT evenly placed along the element of length L. R_d and C_d describe the resistance and capacitance of a distributed length segment Δx of the full element length L

$$R_d = \frac{R}{L}\Delta x, \qquad C_d = \frac{C}{L}\Delta x, \tag{2.54}$$

where the capacitance of a CMUT and the electrode resistance of the element can be expressed as

$$C_{CMUT} = \frac{\epsilon A_{\text{plate}}}{g_{\text{eff}}}, \qquad R = \frac{\rho L}{tW} \tag{2.55}$$

where t and W is are the thickness and width of the element. The voltage distribution $u(x,t)$, dependent on position x, along the element in the limit where $\Delta x \to 0$ and time t can be described as the diffusion equation [82]

$$\frac{\partial u(x,t)}{\partial t} = \frac{L^2}{RC}\frac{\partial^2 u(x,t)}{\partial x^2} \tag{2.56}$$

with $\frac{L^2}{RC}$ is the diffusion coefficient. As it has been described in [82] and [83], the CMUT when in operation is subject to the following boundary and initial conditions

$$u(0,t) = U_0 F(\omega t) \tag{2.57}$$

$$\left.\frac{\partial u(x,t)}{\partial t}\right|_{x=L} = 0 \tag{2.58}$$

$$u(x,0) = 0. \tag{2.59}$$

The boundary condition in Eq. (2.57) describes the input signal function $F(\omega t)$ and the initial voltage of the AC signal on the contact pad. The second boundary condition in Eq. (2.58) describes a zero current density at the end of the element. The initial condition in Eq. (2.59) sets the AC voltage of the signal to zero. This equation has no closed form solution but can in the frequency domain be solved analytically with similar boundary conditions to achieve an expression for the voltage as a product between the input signal function $F(\omega t)$ and the transfer function $H(x,\omega)$ [82]

$$U(x,t) = F(\omega)H(x,\omega) \tag{2.60}$$

$$H(x,\omega) = \frac{\cosh\left(\kappa(1-\frac{x}{L})\right)}{\cosh\left(\kappa\right)} \tag{2.61}$$

where $\kappa^2 = i\omega RC$, with ωRC, being the dimensionless product of the angular frequency ω, resistance R and capacitance C of the system, which can also be interpreted as the inverse diffusion coefficient. This product can be used as a design criterion when choosing the aforementioned operating parameters of the CMUT.

The direct influence of the attenuation of the signal can be found from the absolute magnitude of the transfer function, assuming that the potential is measured at the end of the element $x = L$,

$$|H(L,\omega)| = \frac{1}{|\cosh(\kappa)|} \tag{2.62}$$

where the larger the ωRC product the more attenuation is seen. A criterion dictating a maximum drop of the signal voltage along the element of $100\,\% - |H(L,\omega)| = 1\,\%$ is usually set. This corresponds to

$$\omega RC \leq 0.35. \tag{2.63}$$

This can also be expressed in terms of the the sheet resistance, $R_\square = \rho/t$, the element or electrode length, L, and the capacitance per area $C'_A = C/A_{\text{plate}} = C/WL$

$$\omega R_\square C'_A L^2 \leq 0.35. \tag{2.64}$$

This allows one to predict the signal drop and adjust the design parameters without the need to directly measure the electrode resistance. The resistance can often only be estimated from the known electrode geometry and resistivity, and the precise value only measured in a testing environment on a dedicated electrode with two open ends. It furthermore shows that the choice of $R_\square = \rho/t$, which depends on the electrode resistivity, ρ, and thickness, t, becomes much more crucial for larger arrays as the effect scales with the area, L^2.

Taking the CMUT case from earlier with a resonance frequency in immersion of $\omega_r = 10\,\text{MHz}$, and a plate thickness of $h = 4.37\,\mu\text{m}$, a circular cell radius of $a = 30\,\mu\text{m}$, and a vacuum gap of $g = 205\,\text{nm}$ the capacitance C will be

$$C_{\text{cell}} = \frac{\epsilon_0\left(\pi a^2\right)}{g} = 0.12\,\text{pF} \tag{2.65}$$

using a simple parallel plate capacitor, using $\epsilon_0 = 8.85\times10^{-12}\,\text{F}\,\text{m}^{-1}$. For a RCA array with 128+128 elements, this will be approximately $C_{\text{elem}} = C_{\text{cell}} \times 128 = 15.6\,\text{pF}$.

Now if we assume that the element pitch is $p_{\text{elem}} = 77\,\mu\text{m}$, the kerf is $d_{\text{elem-kerf}} = 4\,\mu\text{m}$, and the cell separation is $d_{\text{cell-separation}} = d_{\text{cell-to-edge}} = 6.5\,\mu\text{m}$, the width of the element is $W_{\text{elem}} = 73\,\mu\text{m}$ and the element length is roughly

$$L_{\text{elem}} = (d_{\text{cell-separation}} + 2\,a) \times 128 = 8512\,\mu\text{m} \tag{2.66}$$

without any apodization regions.

If we then assume that the device is fabricated in silicon on an SOI wafer with a device layer (electrode) thickness of $t = 20\,\mu\text{m}$ and a low resistivity of $\rho = 0.025\,\Omega\,\text{cm}$, the bottom electrode resistance along the element becomes

$$R_{\text{elem}} = \rho \frac{L_{\text{elem}}}{W_{\text{elem}} t} = 1457.5\,\Omega. \tag{2.67}$$

Finally the ωRC product can be calculated

$$\omega R_{\text{elem}} C_{\text{elem}} = 2\pi 10\,\text{MHz} \times 1457.5\,\Omega \times 15.6\,\text{pF} = 1.43 \tag{2.68}$$

which corresponds to reduction of the signal amplitude at the end of the element to

$$|H(\omega L)| = 86.3\,\% \tag{2.69}$$

or an attenuation of 13.7 %. This reduction is larger than the recommended 1 % criterion and will affect the pressure fields, especially if the array is used at higher frequencies. This effect can be mitigated by decreasing the electrode resistivity or increasing the electrode thickness if possible, without changing the rest of the CMUT geometry. The resistivity of the silicon wafer available to us in the Nanolab Cleanroom facilities is ρ<0.025 Ω cm but wafers with ρ between 0.001 Ω cm to 0.005 Ω cm can also be acquired. Another option would be the change the design the electrodes or the fabrication technique to remake the electrodes in a different material with a lower resistivity, e.g. metal.

During the fabrication of the CMUT arrays, some of the geometrical parameters might change unexpectedly, which can also cause the ωRC product and the attenuation of the signal to increase. It is therefore desirable to design the array with a small ωRC close to 0.35 if possible. However, even though arrays with a 10 % to 20 % signal amplitude attenuation are not ideal they will still be usable for imaging.

In Table 2.4 is listed the resistivity of a few different electrode materials, comparing metals to silicon. In Table 2.5 the resistance, ωRC and signal amplitude $|H(\omega L)|$ is listed for the same three metals and and three different thickness of a silicon electrode. For this example, a metal electrode of 200 nm thickness and an average width of 10 µm is used and can be compared to the design in 1.4(d), even though the actual metal electrode design is often more complex than a single straight electrode. The silicon electrode geometry is the same as the previous example and the length L_{elem} and C_{elem}, corresponding to 128 cells, are chosen the same for both electrodes. This shows the clear benefit of either having thicker silicon-based electrodes or using thin and narrow metal electrodes. It is important to keep in mind that this attenuating delay-line effect becomes more prominent for longer elements. For the silicon electrode with $t = 20\,\mu\text{m}$, already at $2 \times L_{\text{elem}}$, $|H(\omega L)|$ becomes 64.6 %, which can be increased to 97.4 % by changing the electrode thickness to 100 µm.

2.1.9 Fabrication methods based on electrode design and style

In Chapter 1 Section 1.4.1 four distinct types of CMUT fabrication methods all using different techniques for defining the cell cavities and the corresponding bottom electrodes were briefly presented and illustrated in Fig. 1.4(a)-(d).

The two designs that will be presented in Part I and Part II of this thesis will be based on a wafer bonding approach. As explained in Section 1.6 these two designs will be:

Table 2.4: Resistivity of thin film metals and doped silicon. Two of the values have been measured at the DTU Nanolab cleanroom facilities.

Material	Resistivity [Ohm cm]
Au (measured)	3.15×10^{-6}
Al	2.7×10^{-6} [60]
Cr	15×10^{-6} [104]
Highly doped silicon (<0.025 Ohm cm) (measured)	4.3×10^{-3}
Heavily doped	1×10^{-3} to 5×10^{-3}

Table 2.5: Electrode resistance, ωRC and remaining signal amplitude $|H(\omega L)|$ listed for three different metals and silicon electrode thicknesses. The silicon used the same L_{elem}, C_{elem}, W_{elem} and as in the text example. The metal electrode are chosen to be an average $W_{\text{elem}} = 10\,\mu\text{m}$ and $t = 200\,\text{nm}$, with the same electrode L_{elem}, C_{elem} and ω as the silicon.

	Metal electrodes			Silicon electrode (<0.025 Ohm cm) varying thickness		
	Au	Al	Cr	525 um	20 um	5 um
Resistance [Ω]	134	115	638	56	1458	5830
ωRC	0.13	0.11	0.63	0.06	1.43	5.73
$\lvert H(\omega L)\rvert$ [%]	99.9	99.9	96.9	99.9	86.3	38.1

1) A combination of a commonly used LOCOS process for creating the CMUT cavities, with a thick highly doped silicon as bottom electrode material. The bottom electrodes will be fully physically separated using a deep RIE based process and a backside silicon etch. For mechanical stability and low capacitive substrate coupling, a borosilicate glass wafer is anodically bonded to the backside. The top plate will be a poly-silicon-based SOI wafer with deposited metal top electrodes.

2) A borosilicate-based glass substrate with etched cavities using deposited metal as the bottom electrodes. The top plate will also be a poly-silicon-based SOI wafer with a thick deposited metal layer as top electrodes.

In terms of electrode resistivity, both of the designs have been shown in the previous Section 2.1.8 to be viable methods for fabricating CMUT arrays with a low signal attenuation along the elements.

2.2 Chapter summary

In this chapter, a method for designing CMUTs was presented both analytically and through simulations. First the element pitch of the array and the various lateral dimensions of the element and cell were found from the operating frequency in immersion. With these parameters locked, the plate thickness could by found from the relation between the resonance frequency of the plate in vacuum and in immersion derived by Lamb. Various expressions of pull-in voltages and center deflections for different plate shapes were then presented, from which the means of calculating the vacuum gap of the CMUT cell and is capacitance was found. The analytically found geometric parameters of the CMUT cell could then be used as starting guesses and adjusted in the FEM simulation model presented in COMSOL. The array and substrate based effects which can affect the performance of the CMUT array was then presented and discussed. Finally an analysis of the effect of the electrode resistance and its effect on the signal uniformity was given with examples justifying the two array designs made in this thesis.

Chapter 3

Wafer level characterisation

The electrical characterisation of fabricated arrays through the use of wafer probing is an important initial step to ensure optimal performance of the CMUT device. The diced chips will ultimately be mounted in a transducer probe handle and encapsulated. Electrical measurements and subsequent adjustments on the individual elements can be performed post-encapsulation. However, exchanging to a different chip if an unacceptable number of non-working elements are found cannot be done. It is therefore crucial to gauge the performance of the arrays after fabrication and map potentially damaged or not working elements.

To ensure fully functional arrays in probes, all of the elements must be tested. This quickly becomes tedious if manual measurements of e.g. arrays with more than hundreds of elements are used. In this thesis arrays with a total of 380 elements will be tested. Automated wafer testers which probe the contact pads on the chip while performing electrical tests can be used. Linear arrays, which are conventionally used in commercial transducer probes, easily allows for characterisation because they are often designed with a common bottom or common top electrode. This means that two needle probes can be placed in a fixed position relative to each other and stepped along the side of the array to perform measurement between the top and bottom electrode of a single element. Two-dimensional arrays, such as the RCA CMUT arrays presented in this thesis cannot be probed in the same manner as top and bottom electrodes are all connected orthogonally. If a single row element, probed on the top electrode contact pad, is to be characterised, all of the perpendicular column elements and their bottom electrode contact pads need to be short-circuited to a single common bottom electrode. This can be achieved by using a prober with multiple needles to access all e.g. 190+190 row and column channels in addition to being connected to an electrical multiplexer. Both such tools are highly complex and very expensive and quickly becomes infeasible for designs with many hundreds of rows and columns.

A solution to this can be implemented in the layout of the array which was presented in a bachelor project in the MEMS-Applied Sensors group [105]. The design is illustrated in Fig. 3.1 and consists of arrays with a conducting frame, essentially an extended electrode, which connect either all rows, called a *top frame*, or all columns, called a *bottom frame*. This simplifies the array to a linear array and makes probing with only two probe needles possible. When the array has been characterised, the connecting frame can be separated in the chip dicing process. The downside to this is that the same array can only be characterised in this way on either all its rows or columns, as that would otherwise require two frames or two different arrays. The available area is also reduced on the wafer, and due to discrepancies in the fabrication process two large arrays might not perform the same, making them difficult to compare by rows and columns. A different technique or a method for selectively short-circuiting elements need, to be found.

A possible solution to this has been presented in this group by the author's supervisor Prof. Erik

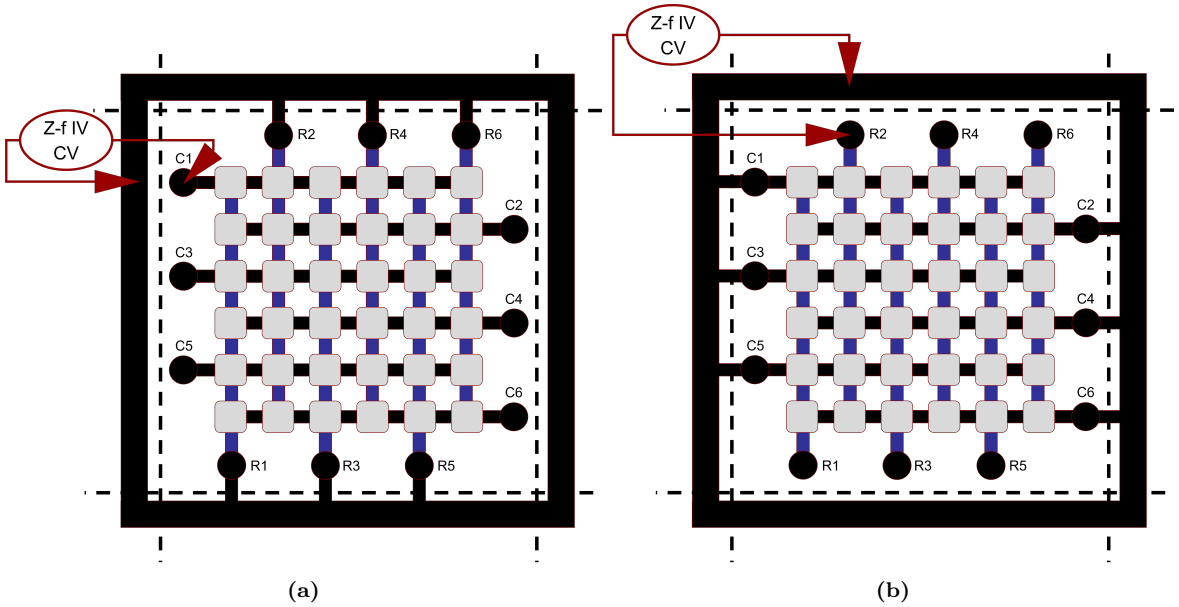


Figure 3.1: Sketch of two 6+6 row-column arrays with an extended electrode frame. This frame can be used to perform top to bottom electrode measurements, by connecting either all row elements (top electrodes) with a *top frame* (a) or by connecting all the column elements (bottom electrodes) with a *bottom frame* (b). The frames can be removed along the dotted lines in the chip dicing process. This makes it possible to use with an automated probe station with only two probes.

V. Thomsen [106] providing an automated and non-destructive wafer level testing of RCA arrays.

3.1 Method

When row-column arrays need to be characterised on a probing system such as the Cascade Summit 12K Probe Station used in this PhD thesis, usually only two probe needles are used. Instead of using a semi-permanent frame connecting either the top or bottom electrodes, the neighbouring elements can be probed. This is illustrated in the sketch in Fig. 3.2 where each probe needle is placed on opposite sides of the array, connected to the contact pad of an odd and even numbered element. One of the two probes is designated the *first* probe (often the High-Force) and the other the *second* (often the Low-Force). The first probe is placed on the first odd or even contact pad depending on what is measured.
For example, if odd rows are being measured on on an array with 190+190 rows and columns, the first probe is placed on the contact pad of row element 1 (E1) and the second on the opposite side on row element 2 (E2). The probes are then stepped so that the first probe contacts E3 and the second probe contacts E4, continuing till the first probe is positioned at E189. For the 190+190 array this gives a total of 95 measurements for the odd row elements.
Afterwards the probes are switched for measuring even row elements. The first probe starts at E2 and the second probe at E3, then they are moved so that they measure between E4 and E5, respectively, until the first probe is at E188. This gives a total of 94 even row measurements for the 190+190 array.

This probing scheme is performed for both the rows and the columns and the odd and even data series are appended to form a full dataset of 189 neighbour to neighbour measurements.

With this configuration it is proposed that the impedance measurements used to calculate the capacitance is now performed as if the two CMUT elements were connected in series. If the substrate coupling and other parasitic capacitances are momentarily ignored, a visual representation of this

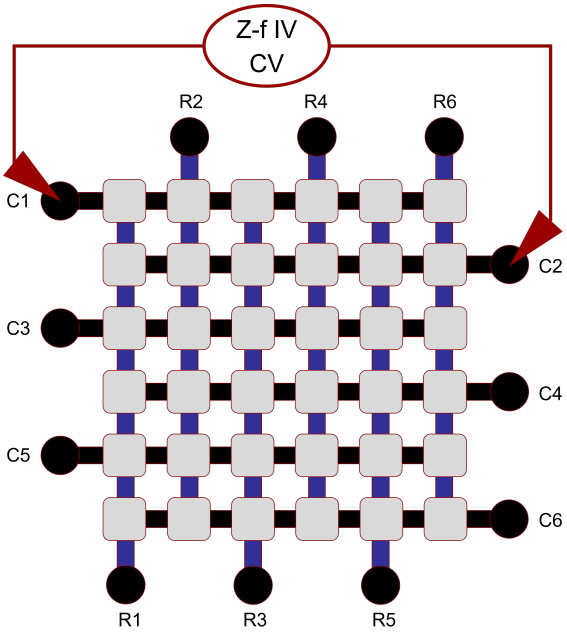


Figure 3.2: Sketch of an 6+6 row-column array. The method presented in [106] of probing neighbouring column or row elements when performing Z-f, IV and CV measurements is illustrated. This makes it possible to use with an automated probe station with only two probes.

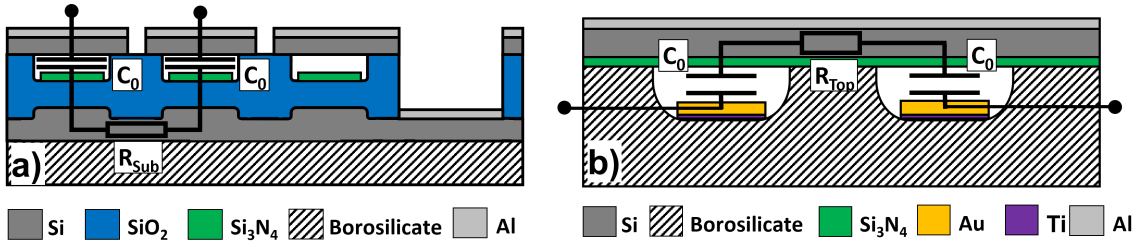


Figure 3.3: Cross-sections of CMUT devices measured between neighbouring elements. (a) shows a LOCOS based fusion-anodic structure with a cross-section of the top electrode pads. Two probes are placed on neighbouring top electrodes, measuring two CMUT elements in series through the substrate with resistance R_{Sub}. (b) shows an anodically bonded glass structure. Two probes are placed on neighbouring bottom electrodes pads, measuring two CMUT elements in series through the top electrode with resistance R_{Top}.

setup for the two devices presented in this thesis is seen in Fig. 3.3. These device cross-sections were also shown in Fig. 1.4.

In Fig. 3.3(a) the fusion-anodic LOCOS based device is shown where two top electrodes are probed and Fig. 3.3(b) shows how two bottom electrodes are probed for the anodically bonded glass device.

The total capacitance measured will be

$$C = \frac{1}{\frac{1}{C_0} + \frac{1}{C_0}} = \frac{C_0}{2} \tag{3.1}$$

where C_0 is the non-biased parallel plate capacitance. The capacitance C_0 can therefore simply be found by doubling the measured total capacitance and then compared to the theoretically predicted value. This is still assuming no parasitic capacitance or other discrepancies.
If the two elements have slightly different capacitances due to errors, non-uniform etching or other

defects during the fabrication process, the individual element capacitance can not easily be found from the measured value.

A short circuit between two neighbouring elements, e.g. E1 and E2, due to an incomplete top electrode etch, will likely show a very small capacitance and phase change, behaving as a resistor. If the capacitance is now measured between element E2 and E3, the total becomes

$$C = \frac{1}{\frac{1}{C_0} + \frac{1}{C_0 + C_0}} = \frac{2\,C_0}{3} \tag{3.2}$$

which can be written as the general expression

$$C = \frac{(m+1)(n+1)}{m+n+2} C_0 \tag{3.3}$$

where the capacitance C is measured between two non-shorted elements which each has m and n short-circuited neighbouring elements.

During chip characterisation mainly two different setups are used. The first one is using B1500A Semiconductor Device Parameter Analyzer (Keysight Technologies, Santa Rosa, California, USA) connected via a GPIB cable to an automatic Cascade Summit 12K Probe Station. The probe station is equipped with micro-manipulators with probe needles for probing the contact pads of the arrays. On the computer controlling the probe station it is possible to create wafer maps with the specific x and y coordinates of each contact pad on the array. These values are set up in a list from which they can easily be chosen and navigated to. In the B1500A a list of measurements to be performed on a single element is generated and repeated for each element with an in-between move command sent to the probe station. Each set of data is measured and saved to the B1500A before a new position is probed. The B1500A is used to perform current voltage (IV) measurements up to $\pm 100\,\mathrm{V}$ and impedance measurements (Z-f) up to 1 MHz, from which capacitance voltage (CV) measurements can be derived. The impedance measurements on this analyser is mainly used to ascertain the correct impedance and phase behaviour of the CMUT at low frequencies and to determine which frequency should be used when performing CV measurements. It should here be noted that the currently used source measurement unit (SMU) and capacitance measurement unit (CMU) for performing IV or CV measurements, can only supply $\pm 100\,\mathrm{V}$. This means that measuring between two adjacent top or bottom electrodes at maximum voltage, assuming that they have equal impedance, will essentially apply only 50 V to each element due to the voltage division. This is important to note, as the CMUTs are usually designed to be operated with a bias voltage from $V_{\mathrm{bias}} = 100\,\mathrm{V}$ to 200 V in commercial scanners like e.g. the BK3000 from BK Medical.

The second setup consists of an Agilent E4990A Precision Impedance Analyzer (Agilent Technologies, Inc., Santa Clara, California, USA) equipped with the Agilent impedance probe kit. This is connected to a Keithley 2410 Sourcemeter through a bias-T and BNC cables to a two-pin (ACP40-A-GS-250) or three-pin (ACP40-A-GSG-250) probing needle (Cascade Microtech) on the Cascade Summit 12K Probe Station. The E4990A Impedance Analyzer is capable of measuring impedance (Z-f) in the range from 20 Hz to 120 MHz, and is used to measure the impedance and phase behaviour at higher frequencies near resonance of the CMUTs. The analyser supplies an AC of 50 mV and the sourcemeter applies a DC bias, V_{bias}, of up to several hundreds of volts (higher than the limit for the B1500A) to bring the CMUTs near their pull-in voltage, V_{pi}. This often lies in the range from 125 V to 250 V, at $V_{\mathrm{pi}} = V_{\mathrm{bias}}/0.8$.

The measurement series made with the B1500A for each element consist of three types of measurements briefly explained below.

- Z-f - Impedance measurement performed between 1 kHz and 1 MHz
- IV - Current voltage measurement ranging from $-100\,\mathrm{V}$ to 100 V
- CV - Capacitance voltage measurement ranging from $-100\,\mathrm{V}$ to 100 V

In the following sections the individual measurements will be explained more in depth.

(a) Series resistance **(b)** Parallel resistance

Figure 3.4: The measurement modes used by the analysers for expressing the impedance parameters and calculating the relevant C, L, R parameters. (a) shows the equivalent series mode circuit, with R_s and C_s being the series resistance and series capacitance. (b) shows the equivalent parallel mode circuit, with R_p and C_p being the parallel resistance and parallel capacitance.

3.2 Z-f

The first type of measurement is the impedance measured against the applied frequency, with a small AC bias of 50 mV.

The impedance is the well-known complex parameter in a circuit, which is a measure for the frequency dependent opposition to an alternating current (AC) flow. This can be simplified as the frequency dependent "resistance" of the circuit, described as a complex vector

$$Z = R + iX = |Z|\angle\theta \tag{3.4}$$

where Z is the impedance, the real part R is the resistance, and the imaginary part X is the reactance.

Equivalent circuits are used by the analysers to model the capacitance and resistance of CMUTs and fit measured impedance values. The two modes used, which are shown in Fig. 3.4, is the series and parallel circuit modes.

The fitted series and parallel resistances and capacitances are R_s and R_p, and C_s and C_p, respectively.

The impedance of the pure capacitors in the circuits are by definition

$$Z_C = iX_C = -i\frac{1}{\omega C}, \qquad |Z_C| = \frac{1}{\omega C}. \tag{3.5}$$

When the impedance of a CMUT circuit is measured, the magnitude of the impedance $|Z|$ and the phase angle $\angle\theta$ are plotted against the frequency. These values are fitted to the two models and the parameters extracted are $|Z|, \theta, G, R_s, R_p, C_p, C_s$. The series and parallel case can be written as

$$\text{Series: } Z_s = R_s + iX_s, \qquad |Z_s| = \sqrt{R_s^2 + X_s^2}, \qquad X_s = -\frac{1}{\omega C_s} \tag{3.6}$$

$$\text{Parallel: } Z_p = \frac{iR_pX_p}{R_p + iX_p} = \frac{R_pX_p^2}{R_p^2 + X_p^2} + i\frac{R_p^2X_p}{R_p^2 + X_p^2}, \qquad |Z_p| = \sqrt{Re(Z_p)^2 + Im(Z_p)^2} \tag{3.7}$$

or described as the parallel admittance

$$\text{Parallel: } Y_p = G_p + iB_p, \qquad |Y| = \sqrt{G_p^2 + B_p^2}, \qquad G = \frac{1}{R_p},\ B = \omega C_p \tag{3.8}$$

with G_p being the conductance (measured in siemens, S) and B_p the susceptance.

A typical Z-f plot, seen in Fig. 3.5, consists of a logarithmic frequency x-axis and multiple y-axes. One showing the impedance magnitude $|Z_C|$ plotted on a logarithmic axis giving a characteristic

straight line for capacitors which can be realised by the transformation

$$\log(|Z_C|) = \log\left(\frac{1}{\omega C_s}\right) = -\log(\omega) - \log(C). \tag{3.9}$$

The second axis shows the phase angle on a linear scale, which for a capacitor is expected to be $-90°$.
The capacitance from the same expression is also plotted and used to gauge in which frequency range the capacitance versus voltage (CV) measurement should be performed and C_0, the base capacitance at zero bias, can be extracted.

Impedance measurements are also subsequently performed on the Agilent E4990A instrument from 20 Hz to 120 MHz with the setup mentioned in the previous section. This is usually done only on selected elements or test elements between top and bottom electrodes due to the limitations of using a single probe. Our current setup has not yet implemented a method for automatically scanning arrays using the Agilent E4990A. An impedance measurement performed for an applied bias voltage of 150 V ($0.8\,V_{\mathrm{pi}}$) is seen in Fig. 3.6.
The resonance and anti-resonance peaks, and the phase shift from $-90°$ to $23°$ are seen in the $|Z|$ amplitude plot and phase plot, respectively. These are both characteristics of the CMUT. The peaks will shift downwards in frequency with an increase in the DC bias. This is due to a phenomenon called spring softening, where the stiffness of the vibrating CMUT plate is reduced the further it is pulled by the attractive E-field set up by the applied DC bias. This downwards shift becomes larger closer to the pull-in voltage, at which point the resonance peaks will move to a higher frequency usually around the second harmonic.

3.3 IV

The purpose of the current-voltage (IV) measurements is to mainly determine whether an element is short-circuited; either between the top and bottom electrodes when probing single test elements or arrays with an attached frame, or between elements when the probes are placed on neighbouring top or bottom electrodes, which is usually what is done on RCA arrays. They are performed for both positive and negative voltages.

The first case usually manifests either right at the onset of an applied voltage (0 V to 1 V), pointing toward an existing defect already bridging the top and bottom electrodes, or at slightly higher voltages (10 V to 30 V) depending on the pull-in voltage, which might indicate insufficient plate insulation or breakdown [55].

The second case is usually due to an incomplete separation of the top electrodes, either during the metal etch or the subsequent silicon etch. Short-circuits during neighbour-to-neighbour measurements can also indicate that the top and bottom electrodes are connected, but this will require that both measured elements are shorted from top electrode to bottom electrode. An illustration of two short-circuited top electrodes can be seen in Fig. 3.7, in which the cross-section of two connected CMUT cells, the equivalent circuit diagrams, and a microscope image of a short-circuiting defect are shown.

Ideally, measurements between top and bottom (sometimes referred to at topbot measurements) and neighbouring elements (toptop or botbot) should be made, as well as the maximum current noted to catch all the failure modes. Based on the IV measurements the elements are further divided into three categories determined by an upper (100 µA) and lower (0.5 pA) compliance current limit; *short-circuited* element with a maximum current above the limit, *not connected* elements below the limit, and *working elements* in-between.

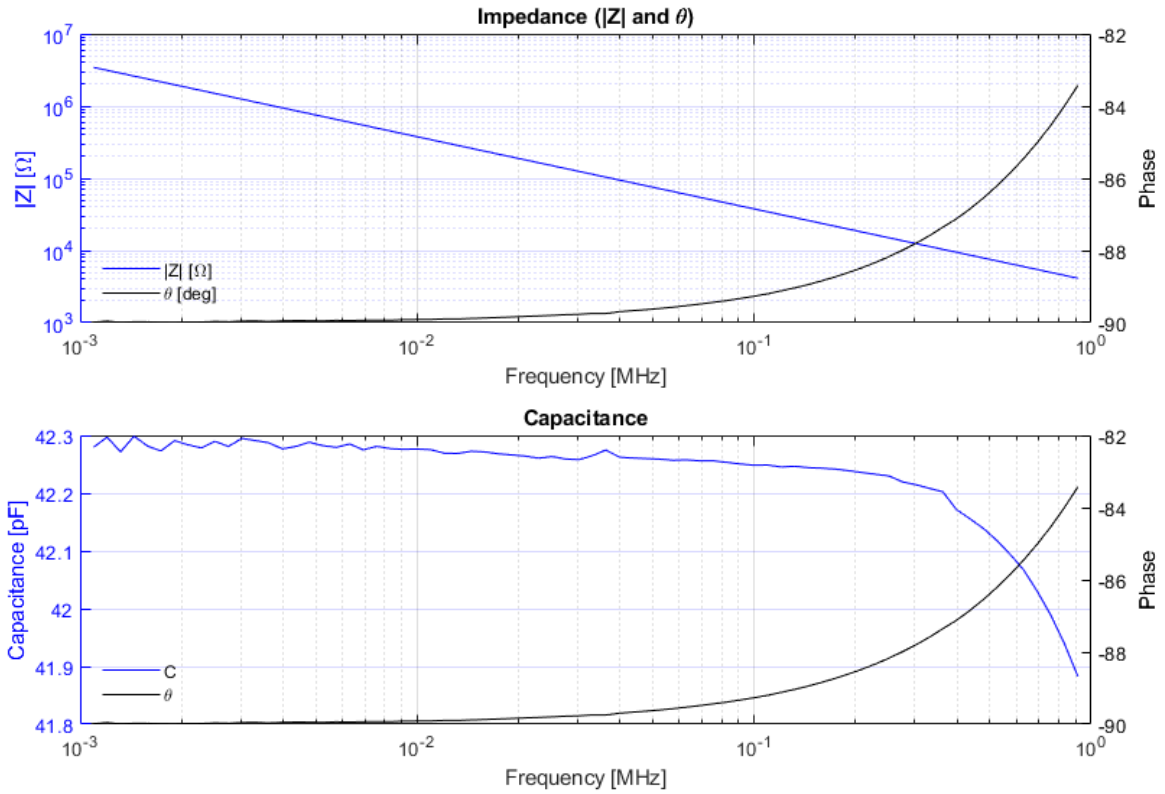


Figure 3.5: Plot of a typical Z-f impedance measurement on the B1500A. The magnitude of the impedance $|Z|$ in [Ω], the derived capacitance C in [pF] and the phase angle θ in [°] are plotted versus frequency from 1 kHz to 1 MHz. The capacitance versus frequency (C-f) can be used to find the optimal frequency for sweeping the capacitance versus voltage (CV).

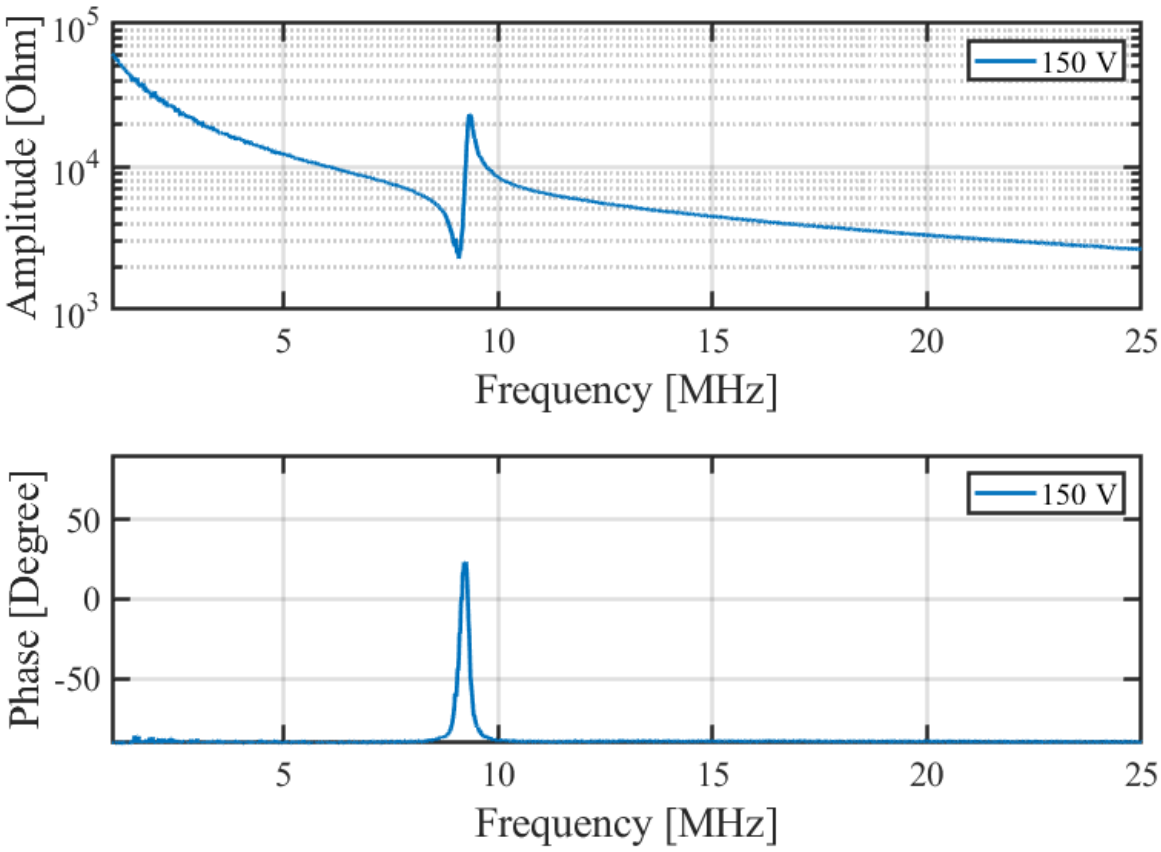


Figure 3.6: Plot of a typical Z-f impedance measurement on the Agilent E4990A, which can be measured from 20 Hz to 120 MHz. The magnitude of the impedance $|Z|$ in [Ω] and the phase angle θ in [°] are plotted versus frequency from 1 MHz to 25 MHz.

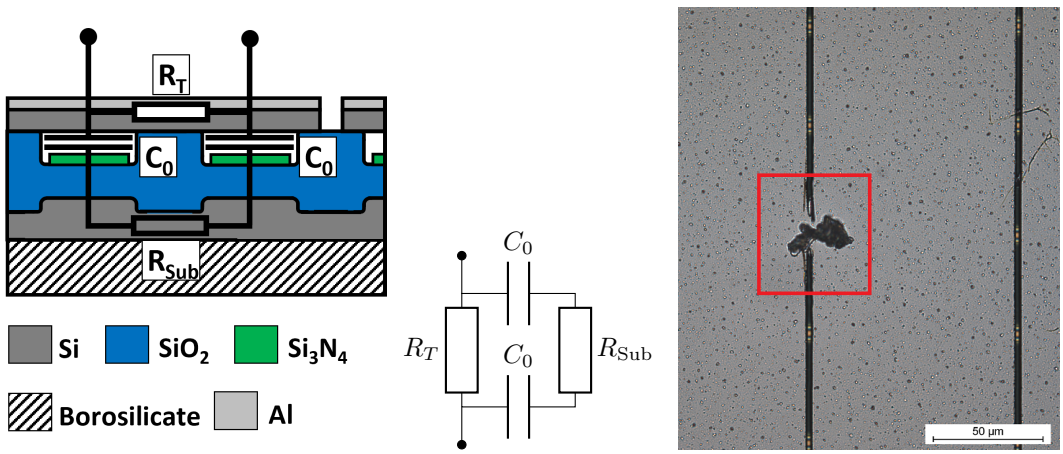


Figure 3.7: Illustration of the probe setup in the case of a short circuit between the top electrodes. (a) shows the cross-sectional sketch from previous with a connected top electrode with resistance R_T between the electrodes. (b) shows the equivalent circuit diagram with the resistance R_T short-circuiting the probes with a smaller resistance than the right-hand side. (c) shows a microscope image of two shorted top electrodes due to a particle shielding the metal and silicon from the etching processes.

3.4 CV

The third type of measurements performed is the capacitance versus voltage (CV). The capacitance is derived from the slope of the impedance magnitude $|Z|$ at a frequency where the capacitance frequency response is flat. This is often around 10 kHz to 50 kHz, seen in Fig. 3.5. The capacitance is measured for both a positive and negative bias up to ± 50 V as seen in Fig. 3.8. This plot can be used to verify the parabolic behaviour of the CMUT, and the minimum of the curve, C_0, extracted from the fit from [82]

$$C(V) = C_0 + C_0\beta(V - V_{\text{offset}})^2 \tag{3.10}$$

where β is a fitting constant and V_{offset} is an offset of the minimum of the parabola from $V = 0$ due to a built-in electric field in the CMUT caused by charging effects [107]. The square dependency of the capacitance on the applied voltage comes from the fact that the force between the plates in the CMUT is attractive and depends on V^2.

The CMUT in its simplest form with included plate bending can be considered a plate capacitor, with area A, with one of its plates fixed and the other attached to a spring, with spring constant k_0 and zero mass. An equation describing the attractive force F_{cap} of the capacitor and the spring F_{s} can be found from considering the energy in the system

$$U_{\text{tot}}(w, V) = U_e + U_s - U_{\text{battery}} = \frac{1}{2}C(w)V^2 + \frac{1}{2}k_0w^2 - C(w)V^2 \tag{3.11}$$

$$U_{\text{tot}}(w, V) = -\frac{1}{2}C(w)V^2 + \frac{1}{2}k_0w^2 \tag{3.12}$$

$$\tag{3.13}$$

where $U_e = \frac{1}{2}C(w)V^2$ is the potential energy in the capacitor dependent on the plate deflection w from w_0 with no bias voltage. $U_s = \frac{1}{2}k_0w^2$ is the energy stored in the spring with spring constant k_0, and the work done by the battery on the system to charge the capacitor plates is $U_{\text{battery}} = C(w)V^2$.

The resulting force on the system trying to restore an equilibrium is then found by differentiating with respect to the deflection as

$$F_{\text{res}} = -\left.\frac{\partial U_{\text{tot}}(w, V)}{\partial w}\right|_V = \frac{1}{2}\frac{dC(w)}{dw}V^2 - k_0w \tag{3.14}$$

for $F_{\text{res}} = 0$, when the forces are in equilibrium, it can be found that the stable position w_s will depend on the applied voltage squared and the first derivative of the capacitance

$$w_s = \frac{dC(w_s)}{dw_s}\frac{1}{2k_0}V_s^2 = \frac{C'(w_s)}{2k_0}V_s^2 \tag{3.15}$$

$$V_s^2 = \frac{2k_0}{C'(w_s)}w_s. \tag{3.16}$$

By differentiating V_s^2 with respect to the distance w_s, $\frac{dV_s^2}{dw_s} = 0$, a local extrema can be found, which indicates the onset of pull-in, V_{pi}, introduced earlier in Chapter 2

$$\frac{dV_s^2}{dw_s} = \frac{2k_0}{C'(w_s)} - \frac{2k_0C''(w_s)}{C'(w_s)^2}w_s = \frac{2k_0}{C'(w_s)}\left[1 - \frac{C''(w_s)}{C'(w_s)}w_s\right] = 0 \tag{3.17}$$

from where the pull-in position w_{pi} can be isolated and the pull-in voltage V_{pi} can be found by

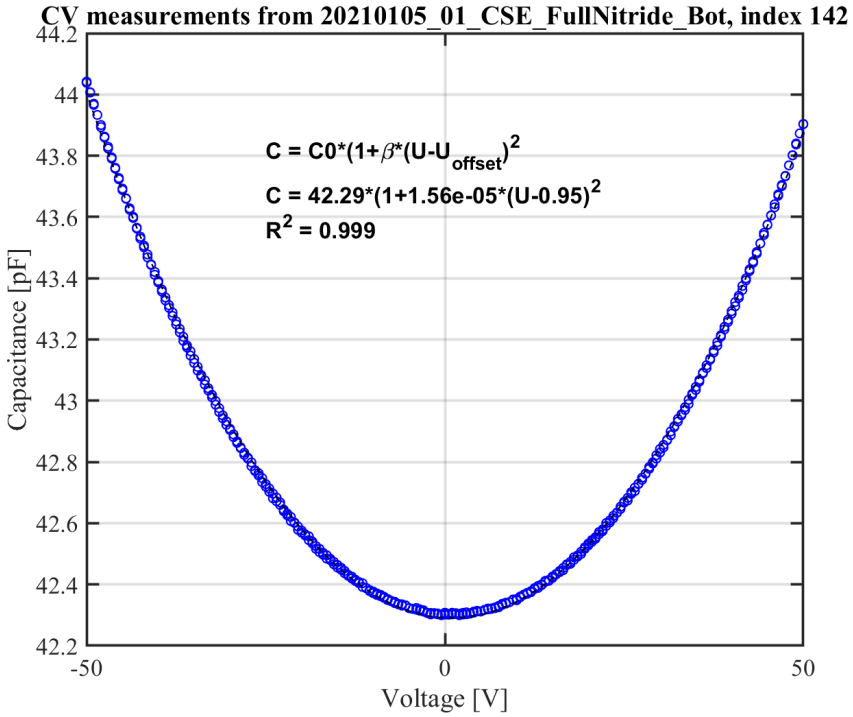


Figure 3.8: Plot of a typical capacitance voltage (CV) measurement. The capacitance is plotted for a negative and positive bias which illustrates the parabolic behaviour of the CMUT structure.

combining Eq. (3.16) and Eq. (3.17)

$$w_{\mathrm{pi}} = \frac{C'(w_{\mathrm{pi}})}{C''(z_{\mathrm{pi}})} \tag{3.18}$$

$$V_{\mathrm{pi}}^2 = \frac{2k_0}{C''(w_{\mathrm{pi}})}. \tag{3.19}$$

Knowing that the capacitance depends on the voltage as $C(w(V^2))$, it can be Taylor expanded around $V = 0$ to 2nd order giving

$$C(w(V^2)) \approx C(0) + C'(0)\frac{dw}{dV^2}\bigg|_{V=0} V^2 \tag{3.20}$$

which is valid for a small bias voltage far from the collapse or pull-in voltage of the CMUT $V \ll V_{\mathrm{pi}}$. The pre-factor $C'(0)\frac{dg}{dV^2}|_{V=0}$ is included in the β pre-factor in Eq. (3.10), and C can be substituted for any of the capacitances corresponding to the plate geometries presented in Chapter 2. The magnitude of V_{offset} in Eq. (3.10) is usually not more than a few volts.

During a CV measurement, the voltage is swept from 0 V to 100 V and then back to 0 V and likewise in the opposite polarity from 0 V to −100 V to 0 V. This is done to investigate whether any hysteretic behaviour is present in the CMUT which could indicate other dielectric charging phenomenons that can affect the performance stability [107].

The stability measurements are performed on individual elements to check for voltage and time dependent charging behaviour using the Agilent E4990A setup. The voltage is usually set directly to the operating voltage, $V_{\mathrm{bias}} \approx 80\,\%$ of V_{pi}, and a bias sequence from $+V_{\mathrm{bias}}$ to $-V_{\mathrm{bias}}$ is applied with resting periods of 0 V which is held for a couple of minutes to a couple of hours for each step. Such a sequence is plotted in Fig. 3.9 with each step lasting 60 min.

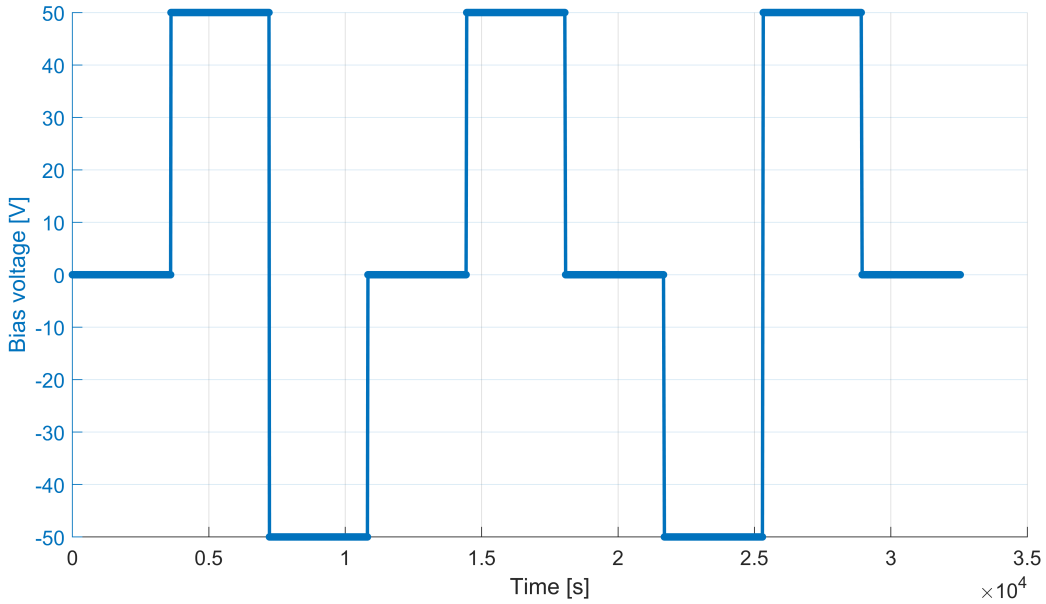


Figure 3.9: Bias voltage sequence used for testing the stability of the CMUT elements. The bias is held for an extended time period at each voltage step and the peak phase angle and capacitance is logged over time. The sequence depicted applies a ±50 V bias held for 60 min at each step.

The fitted capacitance and the change in peak phase angle are logged for each bias voltage step and should remain nearly constant without decaying over time. If this is not the case the change in capacitance per applied voltage $\Delta C/V$ will be reduced. This will reduce the effective electromechanical coupling coefficient, k_{em}, and lower the output pressure and receive sensitivity. The coupling coefficient will be introduced during the discussion on characterisation in Chapter 6. Ultimately it means that the penetration depth during ultrasound imaging, as well as the resolution, will decrease over time.

3.5 Chapter summary

In Chapter 3 the methodology used when performing electrical characterisation of the chips before the probe assembly was presented. Due to limitations of the automatic wafer probing station used, it was not possible to perform electrical test by measuring between the top and bottom electrodes of the large 190+190 arrays. These tests would require all rows or columns to be connected and was not possible in our current setup. To evaluate the performance of each element, a different measuring technique was developed to perform the measurements and test analysis with probes placed on neighbouring elements. This method allows for determination of the capacitance between two elements which was shown to be half of the capacitance of a single element. This method also allows one to deduce how many neighbouring elements are short-circuited.

Part I

LOCOS-based CMUTs Transducer Rodent 2 (TR2)

Chapter 4

Design

In this chapter the 2D RCA CMUT array which has been designated as *Transducer Rodent 2*, and will henceforth be referred to as TR2, will be presented. The design and the associated parameters will e found from the procedure in Chapter 2.

4.1 Specifications and requirements

The general design and development of the silicon-based row-column array presented in this part of the thesis is based on the probe development work presented by Engholm et al. in [46], [64] and the combined fusion and anodic bonded array introduced in the PhD thesis by Havreland in 2019 [82]. One iteration of the design, with electrodes in the shape of a zig-zag pattern, is also based on the study presented by Schou et al. [108].

The final generation of the array and probe in question was fabricated by Mathias Engholm from our group with assistance by the author of this PhD thesis and assembled by BK Medical. The design, fabrication, assembly, and fabrication of this array and the probe has not previously been described in any papers. The design of the finished array is of the same generation as the zig-zag shaped design [108] and the parameters very similar, with mainly the shape of the electrode differing. The author of this PhD thesis has previously worked on the fabrication of the zig-zag shaped electrode design, before complications in the fabrication process rose regarding particle contamination. The continuation of that design became the design used in current TR2 probe.

The CMUT design formula presented in Chapter 2 was finalised in the final stages of this PhD project, and the design for the final TR2 array was based on calculations and OnScale simulations performed by Mathias Engholm. The design does therefore not necessarily follow the steps as rigorously as is intended when new arrays are designed.

This array was originally designed to have an operating frequency of 8 MHz in immersion, corresponding to emitting into the human body tissue with an average speed of sound of $1540\,\mathrm{m\,s^{-1}}$. The fabrication was subsequently carried out with the simulated parameters and the associated plate thickness. However, the particular model used in OnScale was simulated as a 3D infinite array which unfortunately gave a much higher erroneous resonance frequency than when using a simple 2D model. For a ratio of plate radius to thickness of $a/h = 35/4 = 8.75$, used in this design, the difference in resonance frequency between the two models is approximately 35 % higher. This can be seen in Fig. 4.1 for the red data points with legends (a, 2D) and (a, 3D). This means that the designed center frequency instead will be closer to a value between 4.5 MHz to 5.5 MHz.

The array design is specified by the required center frequency in immersion, f_c, and the capabilities of the ultrasonic scanner in terms of the operating voltages, V_{DC} and V_{AC}. The scanner in question,

which will be used together with the designs for the probe presented in this chapter is a BK3000 from BK Medical. This is capable of supplying $V_{\mathrm{DC}} = 190\,\mathrm{V} (\pm 95\,\mathrm{V})$ and $V_{\mathrm{AC,peak}} = \pm 75\,\mathrm{V}$.

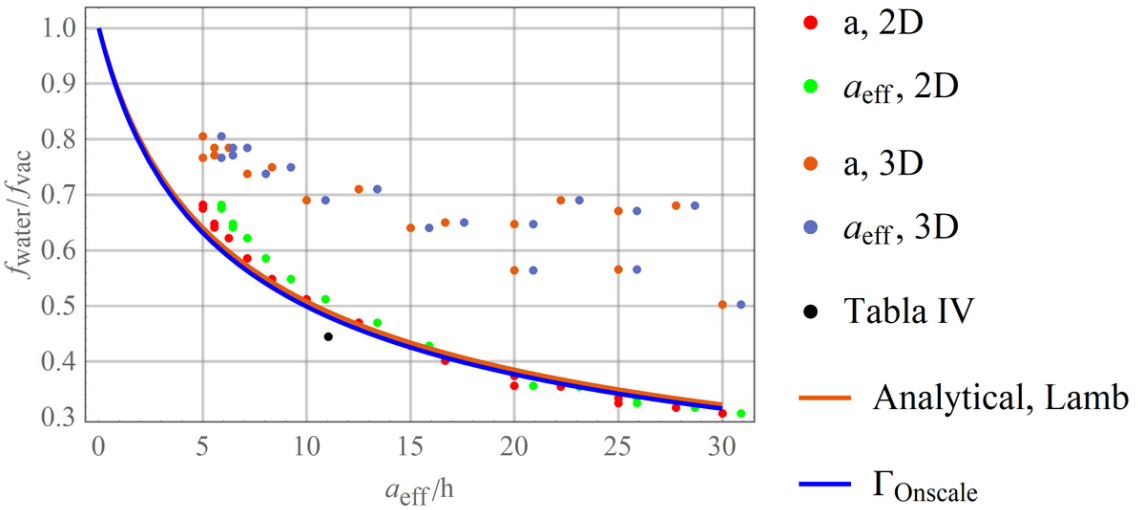


Figure 4.1: The ratio of the resonance frequency in water and the resonance frequency in vacuum/air plotted as a function of the plate aspect ratio. a_{eff} is used here for the cell radius, which takes into account the extended clamping region of the plate and results in a decrease of the resonance frequency compared to a, see Section 2.1.3. Data has been simulated for multiple plate dimensions in OnScale using a 2D (red a, 2D) and a 3D model (orange a, 3D). These data points are both shown with and without the effective radius effect taken into account. The analytical model Eq. 2.15 from Lamb is seen to fit well with data simulated in OnScale for a 2D model. Data for the Tabla IV probe has been included for comparison.

4.2 Design parameters

The center frequency of this array was originally designed for a frequency of 8 MHz in immersion, which is reflected in the element pitch of $\lambda/2$. In human tissue with a speed of sound of $\approx$1540 m s^{-1}, this corresponds to $1540\,\mathrm{m\,s^{-1}}/(2 \cdot 8\,\mathrm{MHz}) = 192.5\,\mu\mathrm{m}/2 = 96.25\,\mu\mathrm{m}$ with the design finalised with a pitch of 95 µm. The final design however will have a center frequency of around 4.5 MHz to 5.0 MHz, corresponding to an element pitch of $\approx \lambda/3.5$ when operated at those frequencies. The element count is 190+190 rows and columns and the cell design was chosen as a square grid of circular CMUT cell.

Following the expression in Eq. (2.9) in Chapter 2, with the element kerf set to $d_{\text{elem-kerf}} = 2.5\,\mu\mathrm{m}$ and the edge distance equal to the cell separation, the equation becomes

$$95 = n\,d_{\text{cell}} + 2.5 + ((n-1)+2)\,d_{\text{cell-separation}} \tag{4.1}$$

$$d_{\text{cell}} = \frac{1}{n}(95 - 2.5 - (n+1)\,d_{\text{cell-separation}}). \tag{4.2}$$

By including the effective clamping radius $a_{\mathrm{eff}} = a + c\,h = a + 0.62\,h$ as $d_{\text{cell-separation}} = 0.62\,h$, the expression simplifies to

$$d_{\text{cell}} \leq \frac{95.5 - (n+1)\,0.62\,h}{n} \tag{4.3}$$

which for the case of one or two cells becomes

$$d_{\text{cell}} \leq \begin{cases} 92.5 - 1.24\,h & \text{for } n = 1 \\ 46.25 - 0.93\,h & \text{for } n = 2 \end{cases}. \tag{4.4}$$

A single cell design was chosen with a $d_{\text{cell}} = 70\,\mu\mathrm{m}$, which sets the $d_{\text{cell-separation}} = d_{\text{cell-to-edge}} = 11.25\,\mu\mathrm{m}$.

Next the plate thickness can be found by combining the the ratio between the resonance in immersion and in air Eq. (2.15) given by Lamb with the Rayleigh-Ritz expression for the resonance frequency in air Eq. (2.16) as

$$\omega_r \sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}} = 10.328\sqrt{\frac{Y}{12\,(1-\nu^2)\,\rho_p}}\frac{h}{a^2} \tag{4.5}$$

which can be rearranged to a 3rd order polynomial of h as

$$(10.328)^2\frac{Y}{12\,(1-\nu^2)\,\rho_p}\frac{h^3}{a^4} - \omega_r^2\,h - \omega_r^2\,\Gamma a\frac{\rho_m}{\rho_p} = 0. \tag{4.6}$$

The density of silicone rubber RTV664 [94], $\rho_m = 1259\,\mathrm{kg\,m^{-3}}$ is used as the damping medium on top of the plate. A plate thickness of 3.20 µm is obtained using the analytical method, which does not in its current form take multiple plates or membrane layers into account [109].

With these initially calculated values the corresponding reduction in resonance from vacuum to a silicone medium is found as

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}}} = 0.45 \tag{4.7}$$

which results in the resonance frequency in air at around 10 MHz.

The pull-in voltage is set to $V_{\text{Pull-in}} = 190\,\mathrm{V}$, which means that the operating voltage will be between $V_{\mathrm{DC}} = 150\,\mathrm{V}$ to 170 V, corresponding roughly to 80 % to 90 % $V_{\text{Pull-in}}$. Using Eq. (2.33) the effective gap g_{eff} can be found now that a value for the plate thickness is known

$$g_{\text{eff}} = \sqrt[3]{\frac{12(1-\nu^2)V_{pi,circ}^2\,a^4\epsilon_0\pi}{89.4459 Y h^3}} \tag{4.8}$$

$$= \sqrt[3]{\frac{12(1-0.177^2)(190\,\mathrm{V})^2\,(35\,\mu\mathrm{m})^4\,8.854\times10^{-12}\,\mathrm{F}\,\pi}{89.4459\times148\,\mathrm{GPa}\times(3.20\,\mu\mathrm{m})^3}} = 343.6\,\mathrm{nm}. \tag{4.9}$$

The effective gap will for this LOCOS based structure by a combination of a thick insulation oxide of around $t_{\mathrm{ox}} = 375\,\mathrm{nm}$ to 400 nm, a insulation nitride used during the LOCOS process of $t_{\mathrm{ni}} = 50\,\mathrm{nm}$ to 60 nm, and a vacuum or air gap in the cavity. From Eq. (2.21) the vacuum gap can then be estimated as

$$g_{\text{eff}} = \sum_{n=1}^{N}\frac{t_n}{\epsilon_n} = g_{\mathrm{vac}} + \frac{t_{\mathrm{ox}}}{\epsilon_{\mathrm{ox}}} + \frac{t_{\mathrm{ni}}}{\epsilon_{\mathrm{ni}}} \tag{4.10}$$

$$g_{\text{eff}} = 343.6\,\mathrm{nm} = g_{\mathrm{vac}} + \frac{375\,\mathrm{nm}}{3.9} + \frac{55\,\mathrm{nm}}{6.86} \tag{4.11}$$

$$g_{\mathrm{vac}} = 239.4\,\mathrm{nm}. \tag{4.12}$$

These values will be used as starting guesses in the 2D CMUT COMSOL model described in section Chapter 2 Section 2.1.6. This is an iterative process where either the vacuum gap, the pull-in voltage or the resonance frequency (the first eigenfreqency) is found by giving a starting guess for all the remaining parameters. These values are then adjusted until a reasonable result for the desired resonance frequency is achieved and a feasible plate thickness and vacuum gap, which can be fabricated in the cleanroom, are found.

Table 4.1: Designed TR2 transducer parameters [1]

Design parameter		Unit
Array		
Number of elements	190+190	
Element pitch	95	µm
Element width	92.5	µm
Kerf	2.5	µm
Element length	20.95	mm
Element thickness	100	µm
Apodization length	1.45	mm
Apodization cell length	9	
Array side length	2.14	cm
Center frequency in air	9.15	MHz
Center frequency in immersion	4.5	MHz
CMUT cell		
Cell diameter (round)	70	µm
Distance to cell kerf	11.25	µm
Plate thickness	4.0	µm
Al electrode thickness	400	nm
Vacuum gap	196	nm
Nitride thickness	55.6	nm
Insulation oxide thickness	375	nm
Post oxide thickness	825	nm
Pull-in voltage	190	V

The resulting design parameters are listed in Table 4.1, with a final plate thickness of 4 µm and a vacuum gap of 196 nm, with a simulated resonance frequency in air of 9.15 MHz, matching the desired frequency in immersion at 4.5 MHz using $\omega_r/\omega_0 = 0.49$.

The finalised chip design is shown in Fig. 4.2 as a complete overview of the last lithographic mask of the fabrication process. All the masks and the design work has been carrier out in the CAD software L-Edit (Tanner Tools). The inset in the figure shows the 9-cell integrated apodization region present in both ends of the rows and columns. A simplified 3D sketch is provided in Fig. 4.3, which illustrates how the row-column structure is built with the orthogonal top and bottom electrodes, respectively. The bottom electrodes (column elements in blue), with a width of 92.5 µm, and the inter-element vacuum kerf/trench, with a width of 2.5 µm, are clearly shown. The CMUT cell cavities (in light gray) made the LOCOS fabrication technique and the top electrode plates (in orange) covering the cells are included. A electrically insulating borosilicate glass substrate (Borofloat 33 [110]) is seen bonded to the bottom of the silicon substrate.

Since the dielectric layer thickness and the finalised gap height has already been found the element capacitance can be calculated. The capacitance is estimated from from the simple parallel plate capacitance at zero bias from Eq. (2.22)

$$C_0 = \left(\frac{g_{\text{vac}}}{\epsilon_0 A_{\text{elem}}} + \frac{g_{\text{ni}}}{\epsilon_{\text{ni}}\epsilon_0 A_{\text{elem}}} + \frac{g_{\text{ox}}}{\epsilon_{\text{ox}}\epsilon_0 A_{\text{elem}}} \right)^{-1} \tag{4.13}$$

$$= \left(\frac{196\,\text{nm}}{8.854 \times 10^{-12}\,\text{F}\,A_{\text{elem}}} + \frac{55.6\,\text{nm}}{6.86 \times 8.854 \times 10^{-12}\,\text{F}\,A_{\text{elem}}} + \frac{375\,\text{nm}}{3.9 \times 8.854 \times 10^{-12}\,\text{F}\,A_{\text{elem}}} \right)^{-1} \tag{4.14}$$

$$= 23.6\,\text{pF} \tag{4.15}$$

where A_{elem}, at 799 559 µm^2, is the total area of the cell cavities of the element.

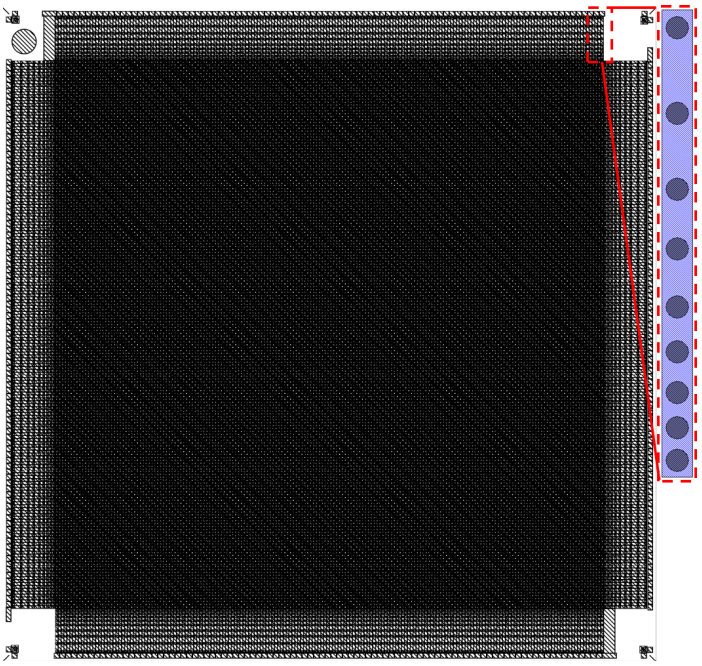


Figure 4.2: Single TR2 array design overview from L-Edit. The drawing shown is from the last mask layer for separating the deposited aluminium layer, called *Top electrode*. A zoom-in inset is shown to the right of one end of an element, illustrating the apodization region. This is made up of 9 CMUT cells with an increasing intercell distance placed according to a Hanning window. In each of the corners a small test element is placed with the same cell dimensions as the large array, and specifically in the north-western corner an orientation dot is placed for later chip alignment.

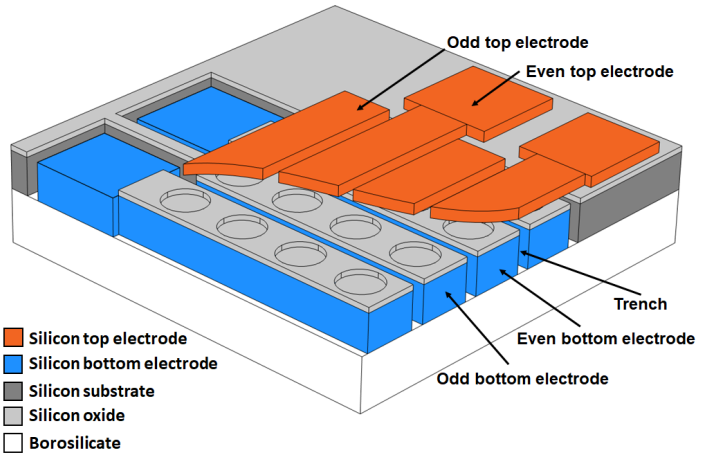


Figure 4.3: A 3D sketch of the corner of an RCA array with the same structure as the TR2 array. The orthogonal blue bottom electrodes and orange top electrodes, made of silicon, are shown encapsulating the structures oxide layer with the circular CMUT cells. A wide trench is shown separating the bottom electrodes laterally, and a glass substrate (borosilicate) is shown bonded to the backside of the structure.

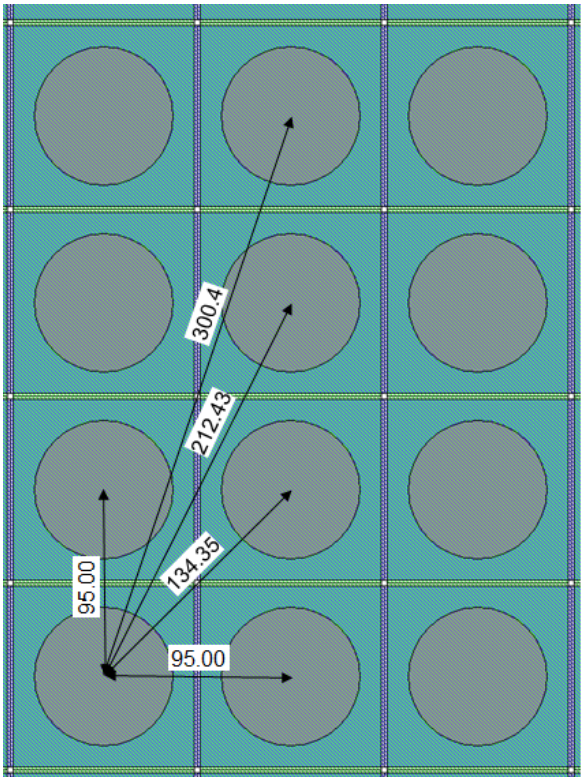


Figure 4.4: Four nearest cell distances [µm] in the TR2 array design.

In Eq. (2.43) the structural interferences which appears similar to a Bragg frequency was briefly introduced. These are caused by the mutual coupling of the oscillators, and can be found from the different cell pitches present in the design. The distances used for these calculations are taken from the array design seen in Fig. 4.4 as the four closest cell distances.

The first Bragg frequency, as seen in Eq. (2.44), lies at two times the resonance frequency at

$$f_{\mathrm{B},1} = 2 \cdot f_r = 2 \cdot 4.5\,\mathrm{MHz} = 9\,\mathrm{MHz}. \tag{4.16}$$

The next three closest distances measure

$$\sqrt{95^2 + 95^2} = 134.35$$
$$\sqrt{95^2 + 190^2} = 212.43$$
$$\sqrt{95^2 + 285^2} = 300.4$$

and are situated at the frequencies

$$f_{\mathrm{B},2} = \frac{1540\,\mathrm{m\,s^{-1}}}{134.35\,\mu\mathrm{m}} = 11.46\,\mathrm{MHz} \tag{4.17}$$

$$f_{\mathrm{B},3} = \frac{1540\,\mathrm{m\,s^{-1}}}{212.43\,\mu\mathrm{m}} = 7.25\,\mathrm{MHz} \tag{4.18}$$

$$f_{\mathrm{B},3} = \frac{1540\,\mathrm{m\,s^{-1}}}{300.4\,\mu\mathrm{m}} = 5.13\,\mathrm{MHz}. \tag{4.19}$$

They will appear inside the bandwidth of the signal measured in a transmission setup if a 100 % relative bandwidth is assumed. However, due to the increased distance between the cells, the density of the cells decrease and amplitude of the interference is presumed smaller.

Table 4.2: Numerical values of ω_{nm} in [MHz]

m \ n	0	1	2	3
0	12.42	25.83	42.37	62.01
1	48.30	73.89	102.75	134.85
2	108.20	145.90	186.84	231.18
3	192.19	241.90	294.9	351.30

The substrate ringing described in Eq. (2.51) for a stack of two materials can also be found. As mentioned, the CMUT substrate will consist of a layer of doped silicon, reduced in thickness to around 100 µm and a 500 µm borosilicate glass wafer is bonded to the backside. The silicon has a speed of sound of $8433\,\mathrm{m\,s^{-1}}$ and the glass $5560\,\mathrm{m\,s^{-1}}$ [111].

The substrate ringing should appear in the spectrum at

$$f_{\mathrm{Sub,total}} = \frac{1}{\frac{2\,t_{\mathrm{Si}}}{c_{\mathrm{Si}}} + \frac{2\,t_{\mathrm{Sub,2}}}{c_{\mathrm{Sub,2}}}} = \frac{1}{\frac{2\cdot 100\,\mu\mathrm{m}}{8433\,\mathrm{m\,s^{-1}}} + \frac{2\cdot 500\,\mu\mathrm{m}}{5560\,\mathrm{m\,s^{-1}}}} = 4.9\,\mathrm{MHz} \tag{4.20}$$

which is right in the bandwidth of the CMUT transducer array close to the resonance frequency and can interfere with the amplitude of the spectrum.

The reflection and transmission coefficients can also be found from Eq. (2.47) from the following acoustical impedances

$$Z_{\mathrm{Si}} = \rho_{\mathrm{Si}} c_{\mathrm{Si}} = 2330\,\mathrm{kg\,m^{-3}}\,8433\,\mathrm{m\,s^{-1}} = 19.65\times 10^{6}\,\mathrm{kg\,m^{-2}\,s^{-1}} = 19.65\,\mathrm{MRayl} \tag{4.21}$$

$$Z_{\mathrm{Boro}} = \rho_{\mathrm{Boro}} c_{\mathrm{Boro}} = 2200\,\mathrm{kg\,m^{-3}}\,5760\,\mathrm{m\,s^{-1}} = 12.23\times 10^{6}\,\mathrm{kg\,m^{-2}\,s^{-1}} = 12.23\,\mathrm{MRayl} \tag{4.22}$$

which gives

$$R_a = \frac{12.23\,\mathrm{MRayl} - 19.65\,\mathrm{MRayl}}{12.23\,\mathrm{MRayl} + 19.65\,\mathrm{MRayl}} = -0.233 \tag{4.23}$$

$$T_a = 0.767 \tag{4.24}$$

from the reflection of a wave travelling in silicon incident on the interface between silicon and glass.

The eigenfrequencies of vibrational modes of the CMUT cell can also be found from using the numerical values for k_{nm} in Table 2.2 and Eq. 2.52. These have been calculated for frequencies in vacuum and are given in Table 4.2. The first and second eigenfrequencies are $\omega_{00} = 12.42\,\mathrm{MHz}$ and $\omega_{10} = 25.83\,\mathrm{MHz}$, respectively, where is is seen that the former does not match the value found from COMSOL in vacuum at 9.15 MHz with $h = 4\,\mu\mathrm{m}$. The second can however be expected to lie at approximately double the resonance frequency at $f_{\mathrm{2nd}} = 2\times 9.15\,\mathrm{MHz} = 18.3\,\mathrm{MHz}$.

Since the structural design of the CMUT array is determined and both the frequency and capacitance is known, the theory from Section 2.1.8 can now be applied to gauge the which electrode parameter are needed to obtain a low ωRC product, preferably below $\omega RC < 0.35$. The resistance of the top and bottom electrodes can be found using the resistivity of aluminium and doped silicon from Table 2.4 and the formulas

$$R_{\mathrm{Top}} = \frac{L_{\mathrm{elem}}}{W_{\mathrm{elem}}\,t}\rho_{\mathrm{Al}}, \qquad R_{\mathrm{Bot}} = \frac{L}{W_{\mathrm{elem}}\,t}\rho_{\mathrm{Si}} \tag{4.25}$$

$$L_{\mathrm{elem}} = 20\,942.5\,\mu\mathrm{m}, \qquad W_{\mathrm{elem}} = 92.5\,\mu\mathrm{m}. \tag{4.26}$$

Table 4.3: Four point probe measurements of the sheet resistance of a single four inch (100 µm) wafer from the same batch used in the fabrication process, with batch purchase ID: SN 590. Thy are $525 \pm 20\,\mu m$ thick phosphorus doped silicon wafers specified with a resistivity of $\rho_{Si} < 0.025\,\Omega\,cm$. The measurements show an average resistivity of $0.0043\,\Omega\,cm$.

	Sheet resistance [mOhm/sq]	Resistivity [mOhm cm]
North	81.8	4.29
East	80	4.20
South	81.9	4.30
West	81.6	4.28
Center	81	4.25
Avg.	81.26	4.27

Table 4.4: Dimensionless ωRC values for the the two different resistivity values and the resulting signal amplitude and signal loss calculated from Eq. (2.62)

Resistivity [Ohm cm]	ωRC	Signal amplitude $\lvert H(L,\omega)\rvert$ [%]	Signal loss [%]
0.0043	0.065	99.97	0.04
0.025	0.378	98.8	1.17

The top electrode will be 400 nm thick, the capacitance is $C_{elem} = 23.6\,pF$ and the resonance frequency $f_r = 4.5\,MHz$, which results in

$$R_{Top} = 15\,\Omega \tag{4.27}$$

$$\omega R_{Top} C = 0.01, \qquad |H(\omega L)| = 99\,\% \tag{4.28}$$

and an attenuation far below 1 %.

For the bottom electrodes, the wafers will will be used in the fabrication process has a specification of $< 0.025\,\Omega\,cm$. So a worst case scenario of $\rho = 0.025\,\Omega\,cm$ will be used in the calculation. Later the actual resistance has been measured with four point probe measurements shown in Table 4.3 on a wafer from the same batch to be ≈ 6 times lower at $0.0043\,\Omega\,cm$.

By rearranging the equation for ωRC and the resistivity, it can be found that the electrode thickness should be around $t = 100\,\mu m$ or above if the supplier specified resistivity is chosen, and $t => 18.5\,\mu m$ if the measured value is used

$$t > \frac{\omega L_{elem} \rho_{Si} C}{0.35 W_{elem}} \tag{4.29}$$

$$t > \begin{cases} 108\,\mu m & \text{for } \rho_{Si} = 0.025\,\Omega\,cm \\ 18.5\,\mu m & \text{for } \rho_{Si} = 0.0043\,\Omega\,cm \end{cases}. \tag{4.30}$$

An electrode thickness of 100 µm was chosen, which gives an ωRC value of 0.065 and corresponds to a theoretical signal loss of 0.04 % calculated from Eq. (2.62), seen in Table 4.4.

4.3 Array Overview

The CMUT array has now been fully finalised and can be drawn in L-Edit. The array will be fabricated on a 4-inch (10 cm) silicon wafer. To fully utilise the area available on the wafer substrate multiple arrays will be fabricated at the same time. The overview of the wafer is seen in Fig. 4.5,

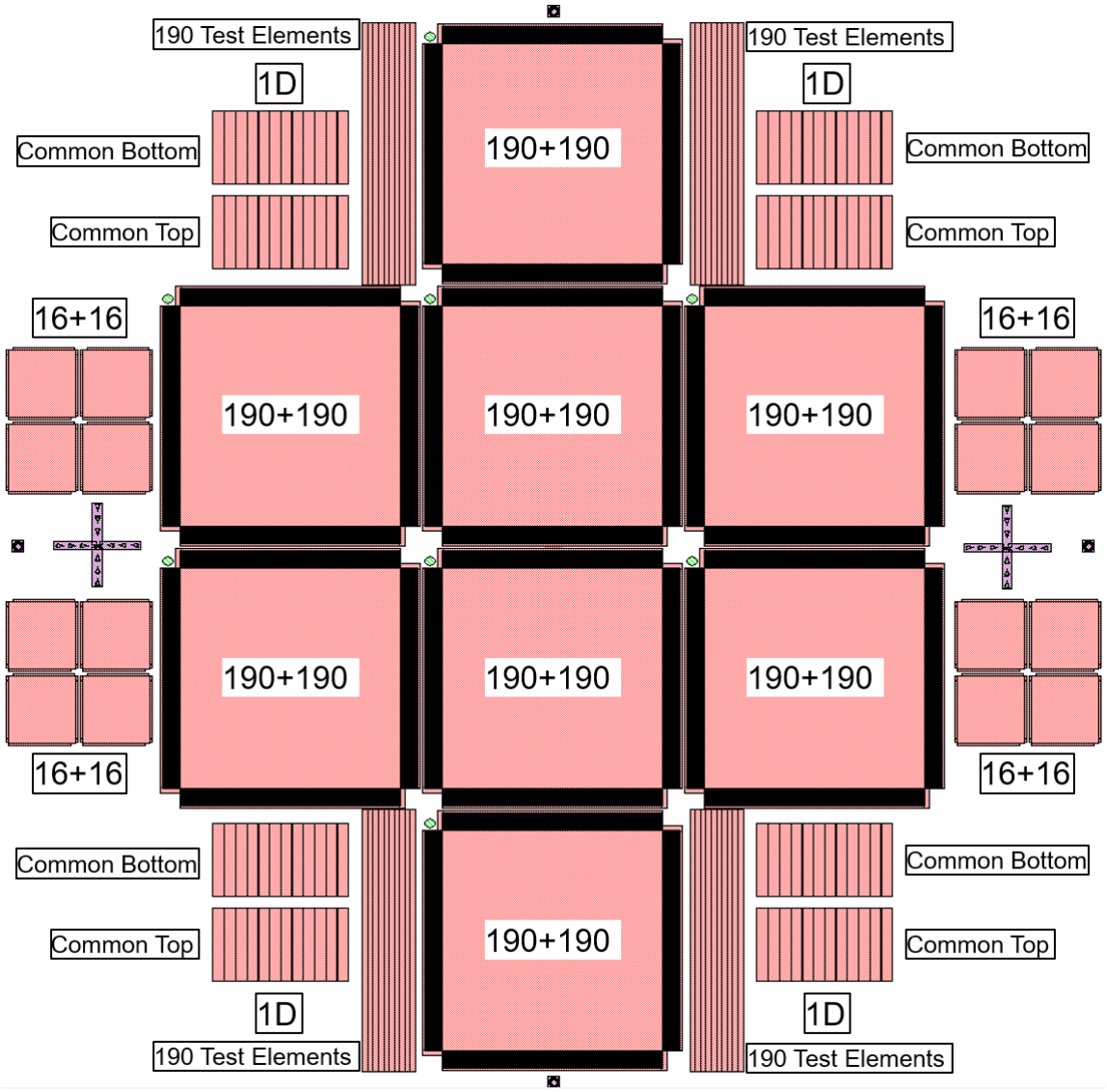


Figure 4.5: Overview of the wafer layout from L-Edit. In the centre region 8 large 190+190 RCA arrays, as depicted in Fig. 4.2, are placed. Beside the north and south most placed array, a section of 10 long test elements with the same amount of cells as the 190+190 elements is included. In the corners of the wafer two 1D arrays with either a common bottom electrode or a common top electrode are included. Finally four clusters of fours 16+16 RCA arrays are also included with the potential of being used for smaller acoustical measurements.

from the mask file *TR2_v2_round*, and this shows than several different structures are included in the design. These are

- 8 190+190 RCA arrays
- 4 sections of single test elements corresponding to 190 cell long elements
- 4 sections of 16+16 RCA arrays with 16 cells per sub-element
- 4 sections with 12 element linear 1D arrays, which either have a common top or bottom electrode. These elements are 10 cells across
- 2 alignment marks resembling a cross which are used for conventional lithographic alignment using glass masks
- 4 alignment marks places in the north, south, east and west of the wafer for alignment when automatic computer-guided alignment is performed with the maskless aligner (MLA) machines

The smaller 1D arrays and 190 long test elements, together with the small test elements in the corners of the 190+190 arrays, can be used for electrical characterisation of the larger arrays without probing these. This could be beneficial if the contact pads of the 190+190 arrays are fragile from the processing steps or if destructive tests should be performed. The smaller 16+16 arrays have the possibility of being integrated on a smaller PCB made for testing and acoustical characterisation can be performed.

4.4 Chapter summary

In this chapter, considerations regarding the design of the TR2 chip array was treated. The various geometrical parameters and properties of the CMUT cell was calculated using the procedure developed in the chapter on CMUT design. The initial design values were found from the resonance frequency in vacuum and adjusted using the COMSOL model developed in this group. The choice of the silicon electrode thickness was found based the the ωRC criterion and the wafer resistivity which will be used in the device fabrication. The Bragg and substrate ringing frequencies were found and can potentially affect the later acoustic measurements by reducing the signal amplitude and reduce the bandwidth. The transducer frequency was furthermore reduced from 8 MHz to 4.5 MHz in immersion as a result of a mismatch in the simulated resonance frequency of the two FEM simulation programs OnScale and COMSOL. Lastly the wafer layout was briefly presented with the various arrays fabricated.

Chapter 5

Fabrication

This chapter will describe in the fabrication process of the TR2 190+190 RCA CMUT array. First an overview of the main methods used are presented and then the two wafer bonding methods used, fusion and anodic bonding, are discussed. From this follows the process flow of the TR2 fabrication process with an included illustrative chart showing all the main steps, which are then all presented in individual sections.

This chapter is intended to provide an overview of the fabrication process used for the arrays, and the reader is referred to Appendix B.1.1 for the detailed process flows.

5.1 Methods

The fabrication of the CMUT array is based primarily on the LOCOS process [63] for structuring the oxide on the wafer surface to create cavities which will be used for the cells. The process is used in combination with fusion bonding for encapsulating the cells with a top plate. The LOCOS process is a widely used technique in semiconductor manufacturing for making oxide posts used for isolation between adjacent devices. By blocking off sections of silicon from in-diffusion of oxygen by using a masking material such as silicon nitride, Si_3Ni_4, one can selectively oxidise silicon.

As mentioned in Section 4.2 a physical trench separation will be used to isolate the bottom elements of the array, as illustrated in Fig. 4.3. The separation etching process used was developed at DTU Nanolab by the authors of [112] and is a modified 3-turn Bosch process called deposit, remove, etch, multistep (DREM). The multiple steps of the process have been fine-tuned to eliminate erosion of the masking material used during etching and to preserve scallop and hole uniformity even for very high aspect ratios ($d_{\text{hole depth}}/w_{\text{hole width}} \approx 100\,\mu\text{m}/2.5\,\mu\text{m} = 40$). In this way the process can achieve "infinite" etching selectivity to the mask. The backside of the wafer substrate will be etched to separate the elements completely and subsequently polished using a chemical mechanical polishing (CMP) process. This will create a surface with an average sub-nanometer roughness to which a borosilicate glass wafer can be bonded using an anodic bonding process.

The two bonding techniques used are briefly described in the following two sections.

5.1.1 Fusion bonding

Fusion bonding is also called direct wafer bonding and is a process used for fusing two wafers together using covalent bonds. This process has been used for CMUT fabrication by other groups [22], [51], [113]–[115]. It requires the two interfacing surfaces to have a very low RMS roughness of $\leq 0.5\,\text{nm}$ to $1.0\,\text{nm}$ [28], [75], [76]. This is also the measure used in this group to check the wafer surfaces before bonding or if bonding fails. The wafers also need to have minimal wafer bow and

be very clean, meaning a very low number of particles. Extensive cleaning procedures are included in the process flow before bonding to minimise particles, which can otherwise cause failed bonds or un-bonded void areas on the wafer surface. If voids are formed on top of an array, the plate will not be bonded to the CMUT cavities and some or all elements will be unusable.

The wafers are bonded in two to three steps, involving usually a hand-bonding step, a pre-bonding step and an annealing step. After the wafer surfaces are cleaned, they are aligned using the wafer flats by hand and pressed together. They are then transported to a bonding tool. During the fusion pre-bonding process, weak spontaneous bonds are formed at the wafer interface as Si−OH (silanol) and Si−H (hydrogen) bonds. This is performed by heating the wafer stack to a temperature between 50 °C and 400 °C and applying force from a piston. The wafer stack can now be handled with less care and is transported to the anneal-bonding furnace for a high temperature annealing process to form and strengthen the covalent bonds, fusing the wafers together.

The annealing process is believed to be a multi-step process which ultimately forms irreversible siloxane Si−O−Si bonds from hydrogen bonds and polymerization of the silanol. This process releases trapped water molecules which in turn further oxidises the surface, and this leads to the formation of more hydrogen bonds at an elevated temperature of 1100 °C for 70 min. At this temperature the oxide becomes viscous which increases the bonding area while bringing wafer surfaces in closer contact.

The fusion bonding process is a reliable method, which has been used for several previous generations of CMUT arrays in this group including the linear Tabla IV-VI and HF transducers.

5.1.2 Anodic bonding

The bonding of two wafers to create cavities and suspended plates or membranes by subsequently thinning down one of the wafers is an important technique in the fabrication of MEMS devices and CMUTs in this work. Anodic bonding is a method used when a glass wafer, a type of borosilicate wafer (Borofloat) and a silicon wafer needs to be bonded. This can also be performed through various thin intermediate layers of silicon and metal oxides. This has been demonstrated for the fabrication of CMUTs by [28], [55]–[57], [116] among others.

The bonding process is performed at an elevated temperature, which changes the conductivity of the glass substrate and allows a bias applied to the wafer stack to set up an electrostatic force pulling the two wafers into contact [77].

Method

The two wafers will form Newton's ring and adhere to each other due to Van der Waals forces immediately upon surface contact. The wafers are like the fusion bonding process brought into contact either by hand or in an wafer aligner tool as a pre-bonding step. This will initially keep the wafer aligned and prevent them from sliding. The wafer stack is then placed in a wafer bonding tool, between a bottom and top electrode designated as anode and cathode, respectively, with the silicon wafer facing the former. The orientation is important, and care has to be taken to not place the glass wafer against bottom electrode (anode) and the silicon wafer against the top electrode (cathode), as the glass wafer would bond to the bottom electrode of the tool.

The stack is then heated to a temperature usually between 300 °C − 500 °C. This decreases the glass resistivity and thereby increases the mobility of the ions present in the glass which assist in the bonding process . The movable ions mainly consist of positively charged sodium (Na^+), oxygen (O^-) and hydroxide (OH^-). The high temperature and bias ($\approx$500 V − 2000 V) drives the sodium towards the cathode and creates a negatively charged depletion zone of bound charges at the glass-silicon boundary. This depletion layer effectively functions as a plate capacitor with a gap of a few nanometers and the resulting strong electrostatic force pulls the wafers together. This intimate surface contact facilitates the permanent bond formation.

There is no overall agreement on how the bonds are created in anodic bonding, however two models are quite popular. One is where the oxidants are inherent in the glass wafer, where $O_2{}^-$ and OH^- oxidise silicon at the interface through this reaction

$$\mathrm{Si(s)} + \mathrm{O_2(g)} \longrightarrow \mathrm{SiO_2(s)}$$

creating strong siloxane bonds. The other model is the so-called water-pump model, where molecular water is trap between the glass and the silicon wafer and is decomposed and the hydroxide reacts with the silicon through a local oxidation process

$$\begin{aligned}\mathrm{Si(s)} + 2\,\mathrm{H_2O(g)} &\longrightarrow \mathrm{SiO_2(s)} + 2\,\mathrm{H_2(g)}\\ \mathrm{Si(s)} + 2\,\mathrm{OH^-(g)} &\longrightarrow \mathrm{SiO_2(s)} + 2\,\mathrm{H^+(g)} + 2\,\mathrm{e.}\end{aligned}$$

The excess hydrogen ions will flow towards the cathode together with the sodium ions and the excess electrons will drift towards the anode, this is what is detected as ionic currents during the bonding process.

Due to the strong electrostatic pulling force, small dust particles trapped at the interface or waviness/unevenness of the silicon surface can be more easily be tolerated compared to e.g. fusion bonding. Because of the viscous properties of the glass wafer, it will flow slightly and conform to the silicon wafer surface when the stack is heated during bonding. The glass also undergoes elastic deformation during the bond at elevated temperatures.

During bonding, particles of various sizes can get trapped in the interface of the two bonding wafers, even if these are cleaned beforehand. It is possible to bond over and absorb particles depending on their size and amount. It is however always preferable to clean wafers before bonding, to remove as many particles as possible.

A high particle count of small and large particles may render the wafer stack un-bondable. They simply will not stick during either pre-bonding, where the Newton's rings form upon initial contact, or they might come apart after the bonding process. If the bonding is successful, air pockets or voids can form in the bonding interface with particles at their centre.

The anodic bonding process is a technique still under development in the group, but has shown good results in terms of array yield due to the strong bond.

5.2 Process

Wafer preparation

The wafer base for the bottom substrate is a highly doped n-type substrate, either single-side polished (SSP) of $525 \pm 25\,\mu\mathrm{m}$ or double-side polished (DSP) of $350 \pm 15\,\mu\mathrm{m}$. Due to the resistance along an element of the finished array and potential delay-line effects, as mentioned in Section 1.4.1 and Section 2.1.8, it is desirable to reduce the resistance or increase the doping level. Row-column and linear arrays of smaller scale have previously been fabricated on SOI wafer or silicon wafers with resistivities of $\rho < 0.025\,\Omega\,\mathrm{cm}$ or higher, corresponding to a donor doping level of $N_d \approx 10 \times 10^{19}\,\mathrm{cm}^{-3}$

RCA cleaning

Before the wafers can be processed in a furnace or bonded in crucial fusion bonding step further in the process flow the wafers need to be thoroughly cleaned. This is done with a standard process two-step cleaning process called RCA clean which is an acronym of Radio Corporation of America where it was also developed by Kern and Puotinen prior to 1970 [60, p. 887].

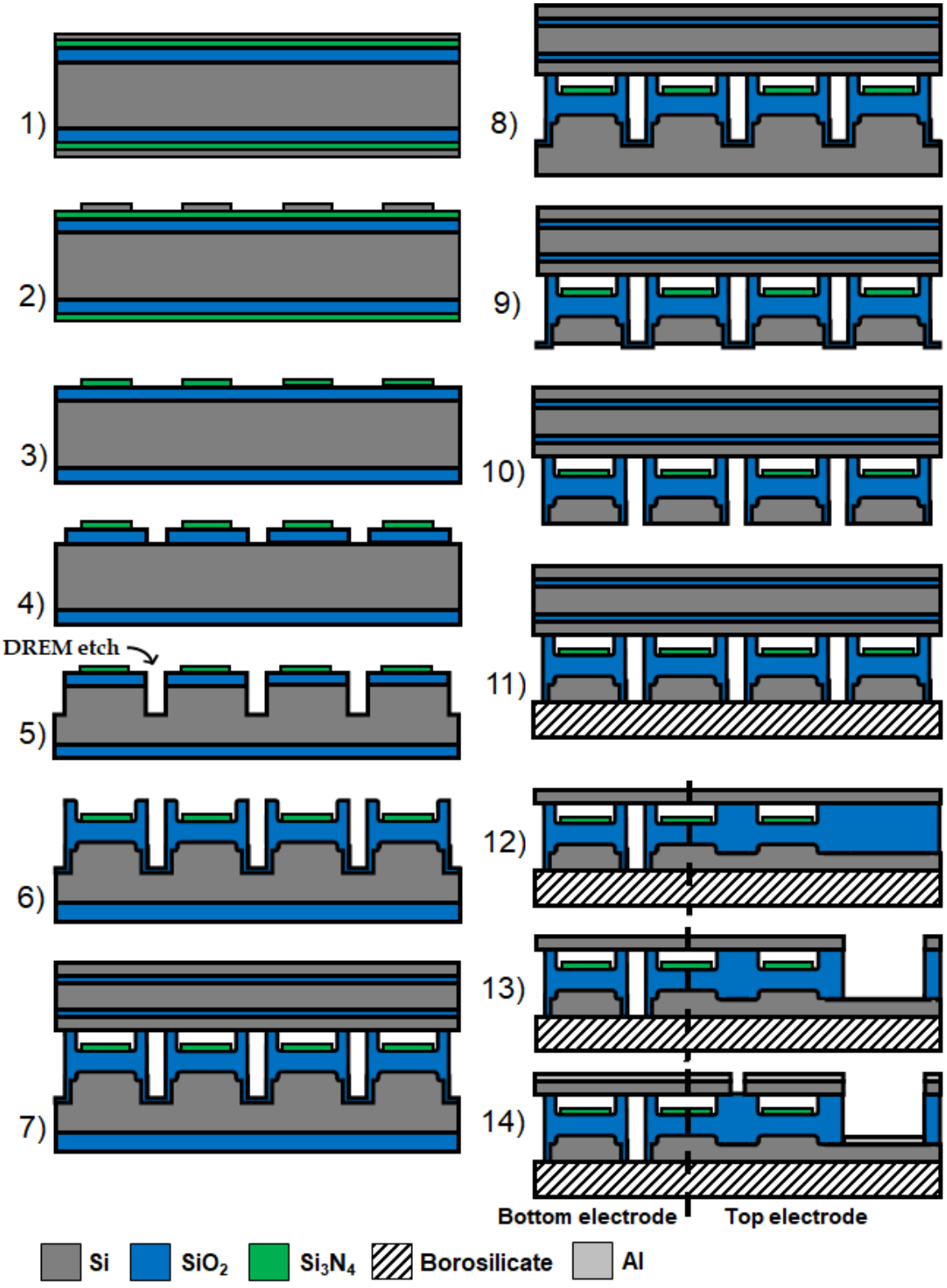


Figure 5.1: Fabrication process flow for the fusion and anodic row-column CMUT array. The dashed line in Fig. 12) through 14) represents a shift in perspective between a cross-section of the bottom electrode (to the left) and the top electrode (to the right). From [1].

Table 5.1: Overall fabrication steps of the TR2 array, based on the LOCOS process, fusion bonding and anodic bonding. These are illustrated in the sketch in Fig. 5.1.

Step	Description
1	A highly doped silicon substrate is prepared with a thermally grown oxide layer, a low pressure chemical vapour deposition (LPCVD) silicon nitride layer and poly-silicon layer
2	The poly-silicon layer is patterned by etching through a photoresist mask
3	Pattern is etch-transferred to the nitride.
4	Oxide is etched through a new photoresist mask, which defines the element width.
5	A deep RIE trench is etched into the silicon using the oxide layer as a mask.
6	The LOCOS process is performed, which defines the cavities.
7	A poly-silicon-on-insulator (PSOI) wafer is fusion bonded to the bottom substrate wafer.
8	The oxide layer on the backside of the structure is removed.
9	The handle layer is thinned from the backside by lapping and RIE etching.
10	The backside is polished prior to bonding.
11	A borosilicate glass wafer is anodically bonded to the backside of the stack.
12	The PSOI handle and buried oxide (BOX) layers are removed.
13	Opening to bottom electrode through poly-silicon and oxide.
14	Finally the top electrodes are separated and the top and bottom electrodes metallised.

The procedure is separated into two steps or chemical solutions and some intermediate steps, all of which are listed in Table 5.2.

The first solution used, RCA1 or SC-1 (standard clean 1), consists of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionised water in ratios NH_4OH:H_2O_2:DI (1:1:5) and has a high pH value. This acts a powerful oxidiser and will remove organic surface particles and metals such as Au, Ag, Cu, Zn, Cd, Cr, and Hg by making them water soluble. The process repeatedly oxidises the wafer surface and dissolves a $\approx 10\,\text{Å}$ thin silicon oxide layer to help dislodge particles. This also leaves the surface with a thin $\approx$1 nm layer of passivation oxide after this process.

The second solution used, RCA2 or SC-2 (standard clean 2), consists of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionised water in ratios HCl:H_2O_2:DI (1:1:5) with a low pH value. This removes heavy metallic ions, alkalis and metal hydroxides (of Al, Fe, Mg and Zn) left from the previous solution.

Both solutions are heated to 70 °C to increase the oxidising properties of the H_2O_2 present in both

Table 5.2: RCA procedure and process times in the cleanroom. In a rinse the waters are dipped in a deionised water bath, where dump rinse and bubble rinse is a rinse with flowing water, the latter with N_2 bubbled through.

	RCA1	RCA2	Dump rinse	HF 5 %	Rinse	Bubble rinse
Process 1	10 min	-	3 min	30 sec	20 sec	2 min
Process 2	-	10 min	3 min	30 sec	20 sec	5 min

mixtures. Due to decomposition of H_2O_2 at these temperatures the RCA solutions have an expected working time of one hour.

The wafers are dipped in a 5 % hydrofloric acid (HF) solution in-between SC-1 and SC-2 to remove the generated oxide layer and any particles trapped within. The cleaning process also end with an HF dip which will leave the wafer surface clean but hydrogenated and highly reactive. This improve surface activation for (anodic) bonding and increase bonding strength. The LOCOS process involves re-oxidation of an existing surface oxide layer and a cleaning of oxide cavities just before fusion bonding, and it is therefore preferable to not remove any of the oxide. In this particular process, only the first HF dip is performed and at a reduced time of 10-15 sec. A 5 % HF solution will have an etch rate in wet thermal oxide of $\approx 25\,\text{nm/min}$ which will only remove $\approx 4\,\text{nm} - 6\,\text{nm}$.

Thermal oxidation - BOX layer

The initial step, corresponding to the first part of step 1) in Fig. 5.1 and Table 5.1, begins with growing a 375 nm layer of silicon dioxide in a dry thermal oxidation process at 1000 °C. This is used as a buffer layer for the subsequent nitride deposition, to mitigate tensile film stresses, and as an insulation layer during CMUT operation and contributes to the total effective capacitance of the device. This step and subsequent furnace processing steps are performed using Tempress horizontal furnaces.

LPCVD nitride deposition

A layer of 55.6 nm LPCVD silicon nitride is then deposited to be used as a diffusion barrier for the later described LOCOS process. This works by blocking the diffusive transfer of O_2 or H_2O in the oxidation process to the silicon surface.

LPCVD poly-silicon deposition

The final part of step 1) involves the deposition of a 100 nm polycrystalline silicon layer (poly-Si) which will be used as a masking layer for structuring the nitride and oxide.

Poly-silicon patterning

In the next step the poly-silicon is patterned with circular discs representing CMUT cells. First a masking layer is made using photoresist, which is either exposed on the Süss MicroTec MA6/BA6 aligner (MA-2) or the MLA150 WM I Maskless Aligner (MLA-2 or MLA-3) depending on the availability of the masks used. The poly-silicon is etched in a wet solution (HNO_3:BHF:H_2O (20:1:20)), and the photoresist removed in a plasma asher with the following gas flows 400 mL/min O_2, 70 mL/min N_2 and a power set to 1000 W.

The name of the photolithographic mask is *Cavity* found in the L-Edit file *TR2_v2_round*

Silicon nitride etching and poly-silicon removal

The silicon nitride layer is then removed using the poly-silicon as a hard mask, effectively transferring the CMUT cell pattern into nitride.

The nitride is removed using the RIE SPTS Pegasus tool.

Silicon oxide etching

In step 4), the silicon oxide insulation layer is etched through a new photoresist mask with the mask layout name *Bottom electrode*. This mask defines the kerf width of the trenches separating the elements to 2.5 µm.

This etching of the oxide layer is done using a RIE machine (advanced oxide etcher (AOE) STS MESC Multiplex ICP) with a selectivity of around 2 for photoresist. The photoresist mask is also subsequently removed with plasma ashing using the same recipe as previous.

Deep reactive ion etching of trenches

To separate the elements, the silicon substrate is etched on the SPTS Pegasus using a process developed at DTU Nanolab called the DREM process, which is performed at −19 °C. A trench depth of ≈100 µm is reached, seen in Fig. 5.2. The photoresist mask is removed with plasma ashing.

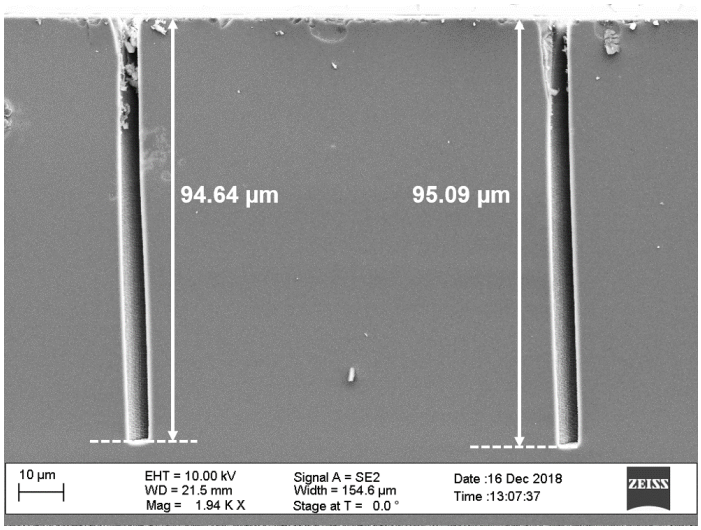


Figure 5.2: Scanning electron microscope image of the silicon trenches performed with the DREM process recipe on the deep reactive-ion etch (DRIE) Pegasus tool. From [1].

LOCOS process

The bottom substrates are RCA cleaned and the only the first HF dip is performed for a reduced time of 10 s to avoid etching the existing oxide buffer layer. The wafers are oxidised using a thermal process in a wet oxidising environment performed at 1100 °C. This is done to achieve a total oxide thickness of around 825 nm. This oxidation defines the CMUT cells cavities through the LOCOS process by selectively oxidising silicon and growing oxide in areas not covered by the nitride cell pads. This is described in [86]. The resulting vacuum cavity gap height is 196 nm, excluding the nitride pad thickness.

Fusion bonding

The bottom substrate, which has now been structured with CMUT cell cavities, is RCA cleaned together with a PSOI top wafer which has previously been demonstrated in [76] by Havreland et al. The fabrication of the PSOI will not be treated in this thesis, but a process flow is included in Appendix Appendix B.1.3. The bottom and top substrates are hand-bonded, just after cleaning, under a HEPA filter. This is carried out in hand by manually aligning the wafer flats and joining the CMUT side of the bottom substrate and the polished PSOI surface. The ambient exposure and handling time is kept short as possible. The wafer stack is pressed together, forming a temporary pre-bonding seal as soon as they are brought into contact if the surfaces are sufficiently flat and clean. They are then placed in a wafer transport box and transferred to the bonding room.

The wafer stack is mounted on the Süss SB6 wafer bonder (wafer bonder 02) chuck and held in place using three clamps, which prevents the wafers from sliding if they have been separated during transfer. The chuck is transported into the chamber which is pumped to a vacuum of 2×10^{-4} mbar and heated to 400 °C. A center rod holds the stack in place while the clamps are released and a larger piston applies a tool pressure of 4 bar for 30 min. This bonding process is illustrated in step 7) in Fig. 5.1.

To evaluate the bond quality the so-called "PL mapper" tool can be used. This is model RPM2000 used for photo luminescence (PL) and reflectance measurements. Reflectivity can be made of the interface of the two bonded wafers and the presence of voids formed during bonding can be inspected. The details will not be explained here.

Backside oxide removal

The oxide formed during the LOCOS process is subsequently removed from the backside of the bonded wafer stack with a 12.5 % ammoniumflouride buffered hydrofloric acid (BHF) solution.

Lapping and etching

The silicon which comprises most of the bottom substrate in the wafer stack is now thinned down to separate the bottom electrodes. This can be achieved in multiple ways of which a combination of lapping and RIE was used. Mechanical lapping performed on a Logitech PM5 Lapping & Polishing System was used to removed most of the silicon substrate, leaving approximately 150 µm − 180 µm, out of the initial thickness of 350 µm or 525 µm depending on the choice of substrate. A close-up of the electrodes and electrode pads after lapping from the backside of the wafer is seen in Fig. 5.3a.

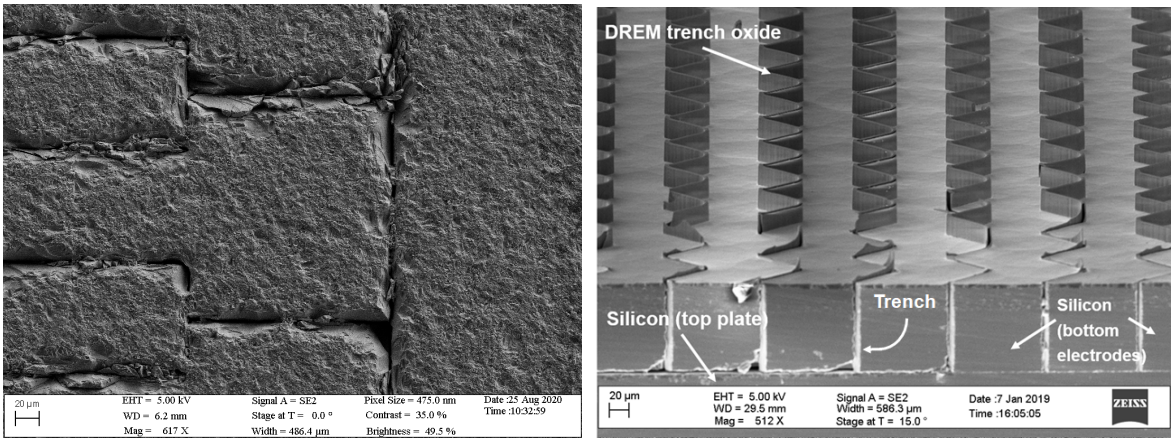
The remaining 50 µm − 80 µm silicon is removed in a RIE using the advanced silicon etcher (ASE) tool by etching until outline of the the bottom electrodes become visible. This takes approximately 1 h depending on the remaining silicon and this step is tuned per process.

This leaves the wafer structure as illustrated in step 9) in Fig. 5.1. The scanning electron microscopy (SEM) image in Fig. 5.3b taken from the backside of a test wafer, with an older electrode design, shows the oxide formed during the oxidation of the trenches in the LOCOS process.

Polishing

It is necessary to remove the oxide from the backside of the bonded stack, shown in Fig. 5.3b before a wafer can be bonded to the surface. It is therefore polished using a Logitech CM62 Orbis CMP system.

The surface roughness is checked using an atomic force microscope (AFM) and should preferably be around or below 1 nm. The cleaning procedure of the polished wafer stack is follows the same steps as for the cleaning of the polished PSOI wafers fabricated in this group, included in the process flow in Appendix Appendix B.1.3. The polished backside of the wafer is seen in Fig. 5.4.



(a) **(b)**

Figure 5.3: (a) Scanning electron microscope image of the backside of the silicon bottom electrodes after the lapping process occurring between step 8) and step 9). (b) Scanning electron microscope image of a test structure illustrating the cross-section of the backside of the wafer after step 9), before polishing. The exposed DREM trench oxide walls separating the bottom electrodes are clearly visible. This was also previously presented in [80].

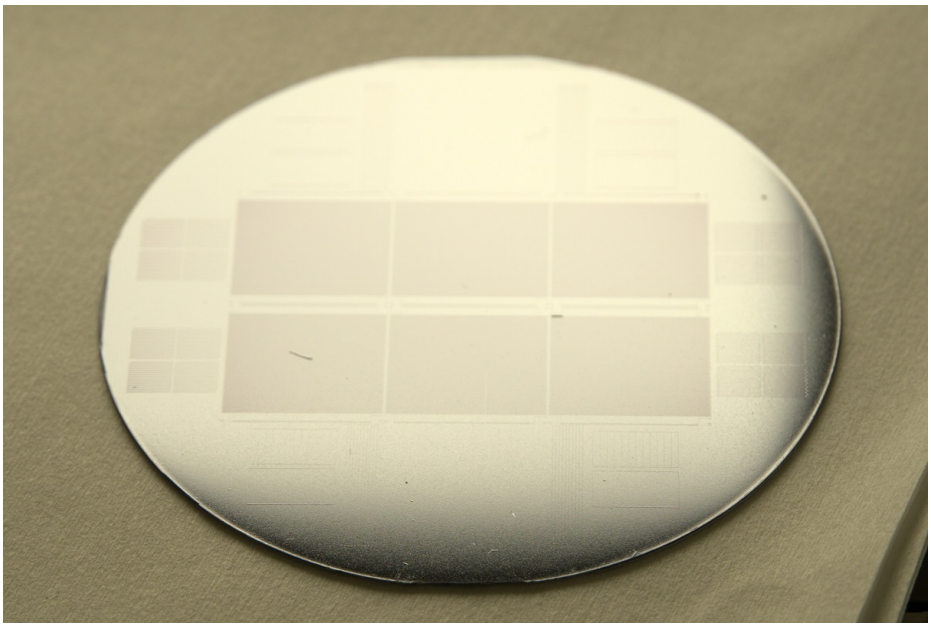


Figure 5.4: The backside of the TR2 wafer is after the lapping, the handle etching, and the polishing processes are completed. The outline of the arrays can be seen with the naked eye.

Anodic bonding

The polished wafer stack is RCA cleaned and a 500 µm thick borosilicate (Borofloat) is cleaned in a piranha solution (H_2SO_4:H_2O_2 in 4:1) to remove organic particles and metal ions for 10 min.

The wafers are again hand-bonded under a filter, as was done for the direct fusion bonding process. The polished underside of the bottom substrate, with the exposed $\approx 100\,\mu m$ thick electrodes, is merged with the glass substrate. The stack is similarly loaded in the wafer bonder and bonded anodically as described in Section 5.1.2. The vacuum chamber is pumped to 5×10^{-3} mbar at an elevated temperature of 350 °C. The voltage step-sequence used in the process is $300\,V \rightarrow 600\,V \rightarrow 800\,V$, with the peak current reaching 13.4 mA for each cycle. The whole sequence including a cool-down period takes around 45 min to 50 min.

Due to the transparent nature of the glass wafer, the wafer stack can be inspected from the backside and checked for voids.

Handle layer and BOX removal

The next step 12) involves removing the poly-silicon layer, BOX layers and the silicon handle from the PSOI. The poly-silicon can be removed in either a batch process as used previously with a wet etchant or with the ASE tool using a recipe tuned to etch the micrometer thick poly-Si layer, *shallolr* with the parameters listed in Table 8.3. The underlying BOX can similarly be removed in the ASE using the recipe *1SIOICP1* (not shown here) or by using BHF.

The silicon handle layer of the PSOI wafers used is 350 µm thick and can either by etched on the ASE or using a heated potassium hydroxide (KOH) solution. Previous experience from this group has shown that both methods, or even a combination, are viable. If the handle etch is performed as a dry etch on the ASE, the wafer needs to be rotated 180° after every 30 min to ensure an approximately uniform etch, which can be stopped on the last BOX layer. This can only be done as a single wafer process.

The wet etching batch process uses a 28 wt% solution of KOH heated to $80\,°C - 90\,°C$, which has an etch rate of 1.3 µm/min in the (100) silicon planes used for this device. The silicon is etched in the following reaction

$$Si + 2\,OH^- + 2\,H_2O \rightarrow Si(OH_4) + H_2(g)$$

which produces H_2 bubbles during the etch and can be used to check if the process is running.

The BOX layer is used as an etching stop layer since the selectivity to oxide is above 1:200. The uniformity during this etch is not perfect and the wafers are checked routinely when the estimated etching time is almost passed. The etching solution will often break through the silicon, beginning from the center and the silicon front will gradually move towards the wafer edge. This last step might not be equal for all the wafers in the batch, and care is taken as to not over-etch individual wafers.

If any voids are present from the bonding process or poorly bonded segments of the plate, they will most likely burst and fall off during the etch. This will expose underlying bottom electrodes and most likely under-etch the plate of open CMUT arrays.

After removing the BOX in BHF, the structure left is just a 4.0 µm thick poly-Si plate. The dashed line in Fig. 5.1 step 12) tries to illustrate both the rows and columns of the array by a shift in perspective between a cross-section of the top electrode to the right and the bottom electrode to the left.

Table 5.3: Parameters for the *shallolr* bosch etching process

Common paramters		Multiplexed parameters		
Parameter	Setting	Parameter	Etch	Passivation
Platen Temperature [°C]	10	SF_6 flow [sccm]	260	0
No. of cycles	5	O_2 flow [sccm]	26	0
Process time [min:s]	00:57	C_4F_8 flow [sccm]	0	120
APC mode	manual	Coil Power [W]	2800	1000
APC [%]	86.8	Platen Power [W]	16	0
		Cycle time [s]	6.5	5

Opening to bottom electrode

In step 13) opening to the bottom electrode contact pad is done by etching through the plate and post oxide to reach the underlying highly doped silicon.

First, a photoresist with the mask *Access to bottom* is defined and then the poly-Si is etched with the *shallolr* recipe on the ASE tool. Using the same mask, the oxide layer is also etched using the *1SIOICP1* recipe for approximately 3×4 min.

To align the photoresist mask using either an MLA (MLA-2 or MLA-3) or the MA6-2 aligner, the alignment marks have to be visible from the previous mask. It is possible to either manually or automatically align through the poly-Si plate by using the built-in microscope and software on the MLA, but this is often only doable if the plate thickness is below 1.5 µm to 2 µm. Voids often form over the alignment marks which can result in the plate breaking off during the handle etch. These or other similar exposed structures can be used for alignment if necessary. If this is not the case, it might be required to first define a mask to open the plate at the position of the marks, either by wafer flat alignment or manually, and then etch with the same recipe as described above.

The photoresist mask is then removed by plasma ashing.

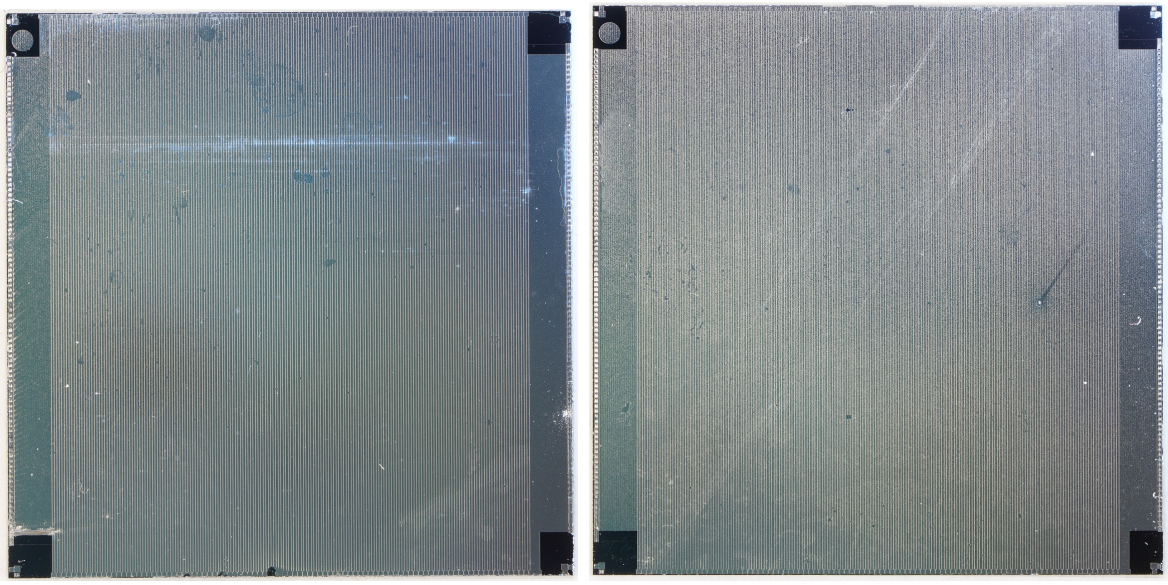
Metallisation and electrode separation

The wafer surface and open bottom electrode pads are now metallised by a coating of 400 nm aluminium. This is performed utilising a Temescal FC-2000 e-beam evaporator. A final photoresist mask is used, called *Top electrode*, to define to separation of the top electrodes. The aluminium is wet etched in a batch process using the etchant PES [117], which has a very good etching uniformity. The elements are then separated by using the poly-Si etching recipe *shallolr* on the ASE tool and the mask removed in plasma ashing.

Dicing

The final step is dicing the individual arrays on the wafer on the dicing saw (DISCO DAD-321). Two finished chips are seen in Fig. 5.5.

The element yield of the finished array has been measured to 132 (69.5 %) for the rows and 133 (70 %) for the columns. This is from acoustical measurements performed on elements with a high response which will be elaborated in Chapter 6. The lowered yield is likely the result of a sulphur compound forming during the opening to the bottom electrodes during step 13) in Fig. 8.1. This prevented a complete etch of the silicon covering the electrode contact pad making functioning wire bonds unreliable.



(a) **(b)**

Figure 5.5: Photos of two finished TR2 chips, labelled (a) *TR2_O_1_Chip_1* and (b) *TR2_O_1_Chip_2* or simply *TR2-1* and *TR2-2*. The TR2-2 chip is the chip which will be further integrated in the probe for acoustical characterisation.

5.3 Process result discussion

During the fabrication process it was discovered that not all post oxide was etched for some of the contact pads due to the formation of a sulphur compound, see Fig. 5.6. Multiple cleaning steps with RCA, HCl, HNO_3, and piranha were tried without success. As a result, this prevented a complete access to the incomplete bonding pads, making wire bonds unreliable and lowering the electrode yield. It is not clear how many elements were affected by this, but it is estimated to be around 40 %.

The contact pads for the bottom electrodes were to a varying degree affected by the presence of the sulphur compound, as seen in Fig. 5.7. This will likely result in a varying acoustical sensitivity across the array. This will make it more difficult to produce high quality images as the contrast is lowered due to the missing or poorly performing elements.

The formation of such sulphur compounds has not previously been seen when etching on dummy structures identical to the final device wafers. It is therefore unfortunate that it suddenly affected the device wafers. This problem can be avoided by further etch process design optimisation including temperature control, gas flow and careful chamber pre-conditioning, as several groups in the cleanroom use the etching tool with different recipes.

Only two chips from the batch, labelled *TR2-1* and *TR2-2*, were finished. This was due to time constraints, problems with top plate adhesion during wafer bonding and the bottom electrode etch discussed above. The *TR2-2* chip will in the following chapter be integrated in the 3D milled probe handle

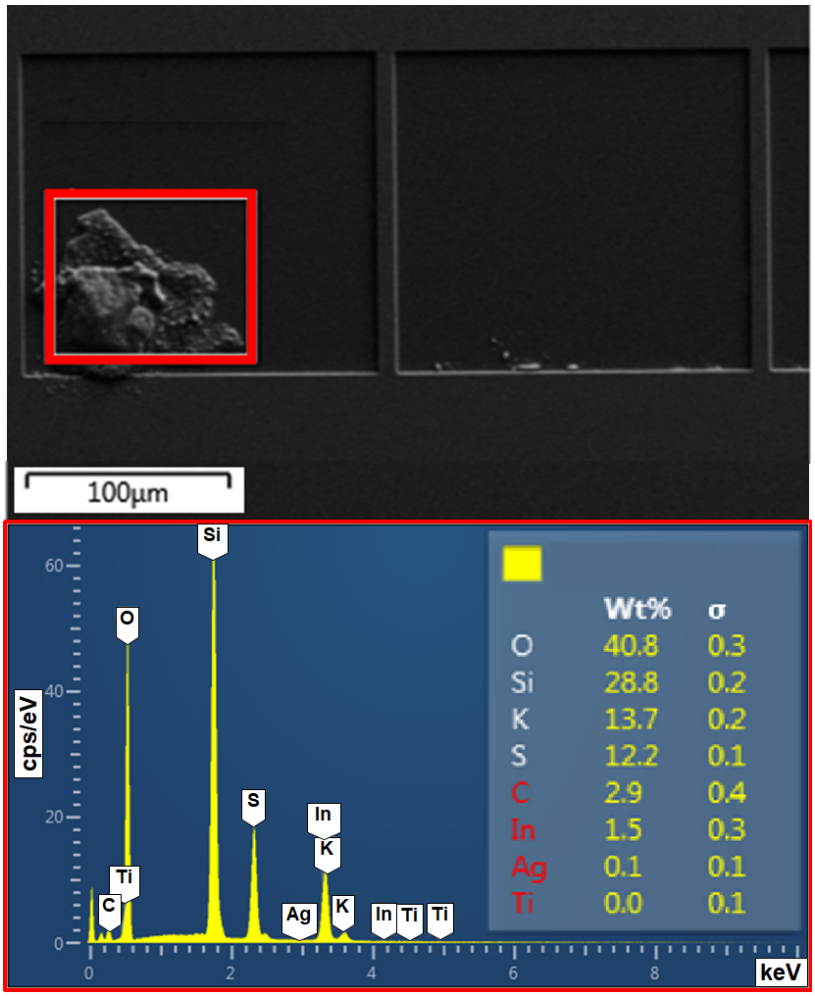
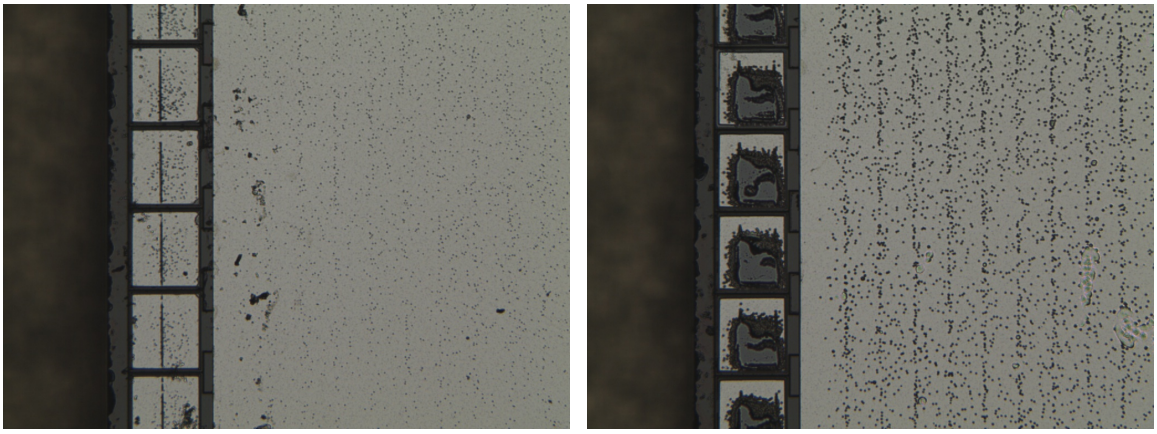


Figure 5.6: Scanning electron microscope image showing an example of a particle consisting of a sulphur compound. This partially blocks the SiO_2 etching process in step 13) in Fig. 4 which prevents the opening to some of the bottom electrodes, and leads to problems in the definition of top electrodes in step 14), thus reducing the yield. The inset represents an EDX spectrum of the area marked in red, showing a high concentration of sulphur and potassium which is not observed in particle-free areas. From [1].



(a) **(b)**

Figure 5.7: Images taken of the *TR2-2* chip after fabrication and dicing. In (a) a small amount of damage to the bottom electrode metal is seen. In (b) severe electrode damage is seen, presumably as a result of the incomplete bottom electrode access etch caused by the presence of the sulphur compound.

5.4 Chapter summary

In this chapter the fabrication process for the TR2 chip array was presented, which was carried out in the DTU Nanolab cleanroom facilities. The fusion and anodic bonding methods used in this process were also discussed. All the main steps of the fabrication were shown and details were provided for each of them. The resulting TR2 chips were shown in the end, and a problem with incomplete etching of the bottom electrode contact pads were discussed, which affected the yield of the elements. The next chapter will go into details about the electrical and acoustical characterisation of the chips and the assembly of the probe.

Chapter 6

Transducer characterisation

This chapter presents the characterisation performed on the assembled probe with the TR2 2D imbedded array. This is characterised before and after encapsulation. The electrical tests performed includes high frequency impedance measurements and pull-in tests. IV and CV tests were not performed.

The encapsulation of the chip in the probe handle will then be shown. Afterwards the acoustical characterisation on the probe with transmit and pulse-echo measurements will be presented and the uniformity and amplitude of the rows and column elements will be compared. A pressure uniformity map will also be presented as a method for evaluating the signal attenuation of the elements. Finally the probe is used to acquire B-mode images and imaging depth using three types of phantoms; a hydrogel scatter phantom, a matrix wire phantom in water, and a tissue mimicking cyst phantom.

6.1 Electrical Characterisation

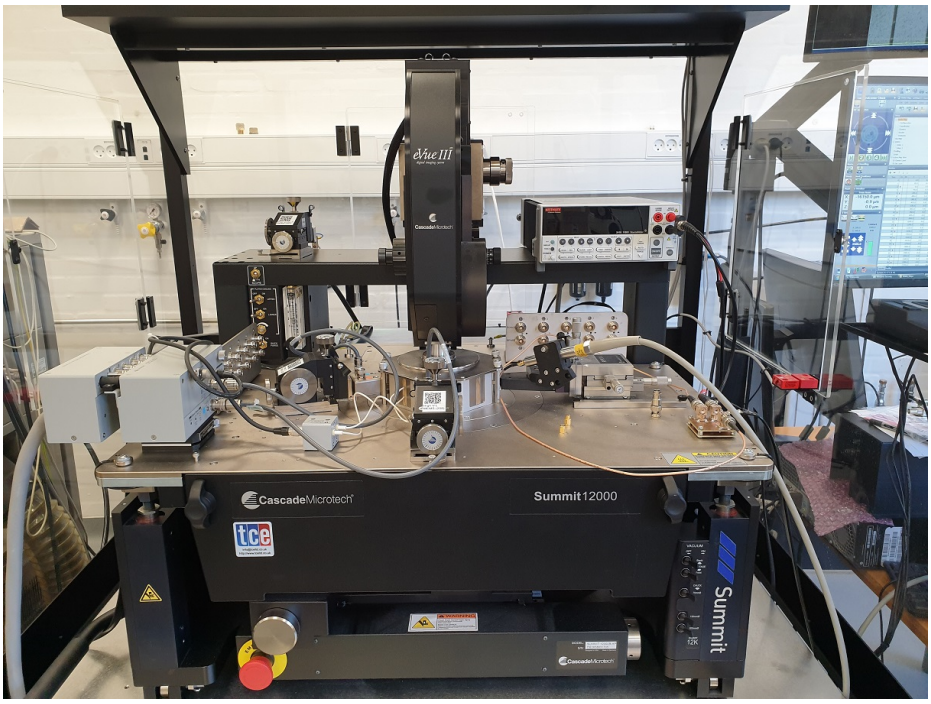
The CMUT array was electrically characterised before dicing, wire bonding and encapsulation in silicone by the means of impedance measurements using an Agilent E4990A Precision Impedance Analyzer (Agilent Technologies, Inc., Santa Clara, California, USA) and a Cascade Summit 12K Probe Station. This is used to measure the impedance, and the phase of the CMUT capacitors over a wide frequency range. The elements can be probed one by one from 20 Hz to 120 MHz using the attached Agilent impedance probe kit connected with a BNC cable to a two-pin (ACP40-A-GS-250) or three-pin (ACP40-A-GSG-250) probing needle (Cascade Microtech) in contact with the arrays.

The impedance analyser is connected to the probe through a bias-T, designed and made in-house, to a Keithley 2410 Sourcemeter. This is utilised to source a voltage of our choosing (up to 400 V to 500 V as rated by the components used) as the bias for our CMUT cells and superimpose the 50 mV AC signal from the analyser used to perform the impedance analysis. The bias can be adjusted manually on the sourcemeter but is controlled via GPIB together with the impedance analyser in a GUI on a separate computer also used for logging the data. The setup can be seen illustrated in Fig. 6.1.

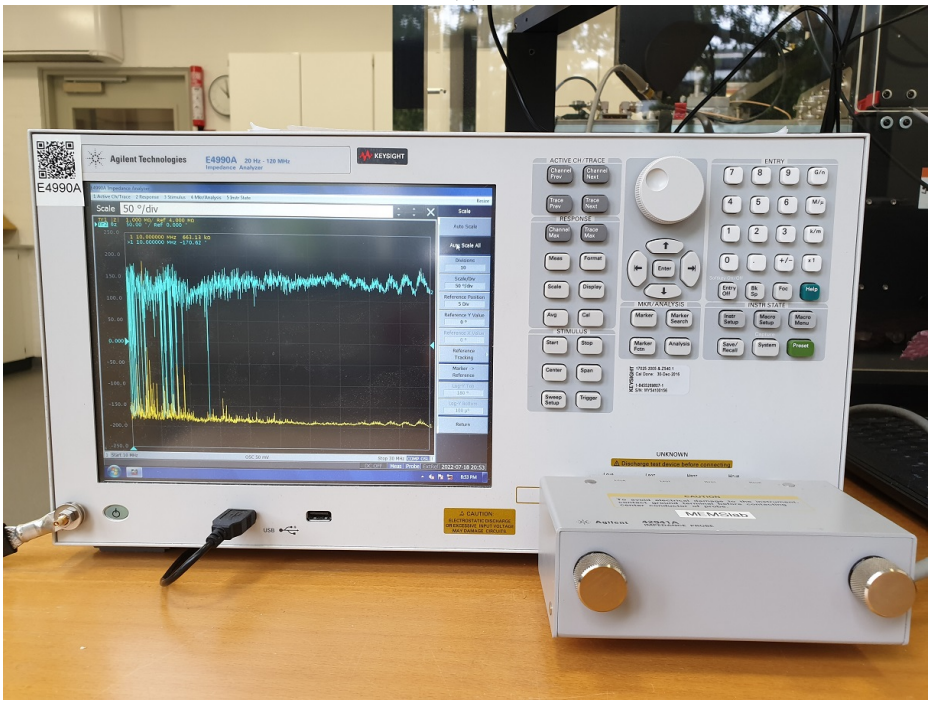
6.1.1 Impedance

Measurements were performed on separate linear test arrays and single test elements located in the corners of the 192+192 arrays to provide an estimate of the actual pull-in voltage for the array. The DC voltage supplied by the sourcemeter was varied from 0 V up to 190 V. The voltage sweep could then be used to find the pull-in voltage.

Measurements performed on a test element from chip 1 placed in the nothwestern corner of the wafer from Fig. 4.5, is plotted in Fig. 6.2 and in Fig. 6.3, showing the impedance magnitude and phase from



(a)



(b)

Figure 6.1: (a) Cascade Summit 12K Probe station with a Keithley 2140 Sourcementer connected to (b) E4990A Impedance Analyzer on the left, used to perform Z-f measurements for finding the resonance frequency. Stability tests of the peak phase angle or derived slope capacitance over time can also be performed using an external MATLAB GUI for controlling the analyser.

1 MHz to 25 MHz for a selected voltage range from 150 V to 187 V. The expected CMUT behaviour is observed with a noticeable resonance and anti-resonance peak in the impedance spectrum, as well as a shift in the resonance peaks towards lower frequencies with increasing bias voltage, which confirms the spring softening effect observed in CMUTs. At the resonance frequency a characteristic phase shift from $-90°$ towards $90°$ is also observed for the CMUT. From the impedance measurement on this test chip it can also be seen that the amplitude increases significantly the closer the cell gets to pull-in. At around 183 V or 184 V bias another set of peaks appear in the 20 MHz region for both impedance and the phase plots. Focusing on the resonance peak of the impedance plot, this increase in bias from 182 V to 184 V is coupled with a large downward shift in frequency for the peaks at 6.2 MHz to 3.9 MHz, indicating the beginning of pull-in for some cells. After 184 V the lower frequency peaks in the region from 3 MHz to 10 MHz disappear as all the cells go into pull-in. In Fig. 6.3 the impedance and phase is plotted only for the DC bias voltages 150 V, 184 V and 185 V, where the frequency shift and change in phase is clearly illustrated at around operational voltage and pull-in. This is also illustrated in the phase angle versus frequency plot and in Fig. 6.4, where at 185 V the phase shift peak disappears from $\approx$ 2.5 MHz and is only visible near 19 MHz. The estimated pull-in for the examined test element can therefore be estimated as 185 V.

Models describing the CMUT capacitor impedance can be fitted to the impedance spectrum and the resonance and anti-resonance peaks extracted to calculate the electromechanical coupling coefficient (squared) which, as described briefly earlier, can be found as

$$k^2_{\text{em}} = 1 - \frac{f^2_{\text{res}}}{f^2_{\text{a-res}}}. \tag{6.1}$$

These k^2_{em} values are plotted in Fig. 6.4 in percentage for increasing bias voltage, showing a maximum of 31 % right before pull-in. If a relative operating bias between $80\,\% - 85\,\%$ of V_{pi} is utilised, this corresponds to voltages in the range $148\,\text{V} - 157\,\text{V}$, which gives an approximate coupling coefficient between 4.4 % and 5.4 %. In comparison, a previous made linear array probe (TABLA IV, 128 elements) [86, p. 107] gave $k^2 \approx 7\,\%$ at $150\,\text{V}(0.8V_{\text{pull-in}})$ and a LOCOS based 90+90 2D CMUT array [82, p. 50] which gave $k^2 = 7.78\,\%$ to $9.57\,\%$ at 170 V to $190\,\text{V}(0.77V_{\text{pull-in}}$ to $0.86V_{\text{pull-in}})$ has almost double the coupling exhibited by the TR2 probe. An early prototype for the TR2 probe, also built with the fusion-anodic double bonded fabrication scheme, was presented in [82] with 188+188 RCA CMUT elements and gave a $k^2 = 3.92\,\%$ at $70\,\text{V}(0.78V_{\text{pull-in}})$, which is comparable to the TR2 probe, although with a lower pull-in voltage. A closer view on the spectrum plotted for 150 V is shown in Fig. 6.5.

A pull-in voltage of 184 V was chosen which matches well with the designed pull-in voltage of 190 V. This reference pull-in value becomes important during probe assembly when the bias voltage at the chip level will be adjusted. The measured center frequency at 150 V was 9.25 MHz which is also in good agreement with the COMSOL simulated value of 9.15 MHz in air.

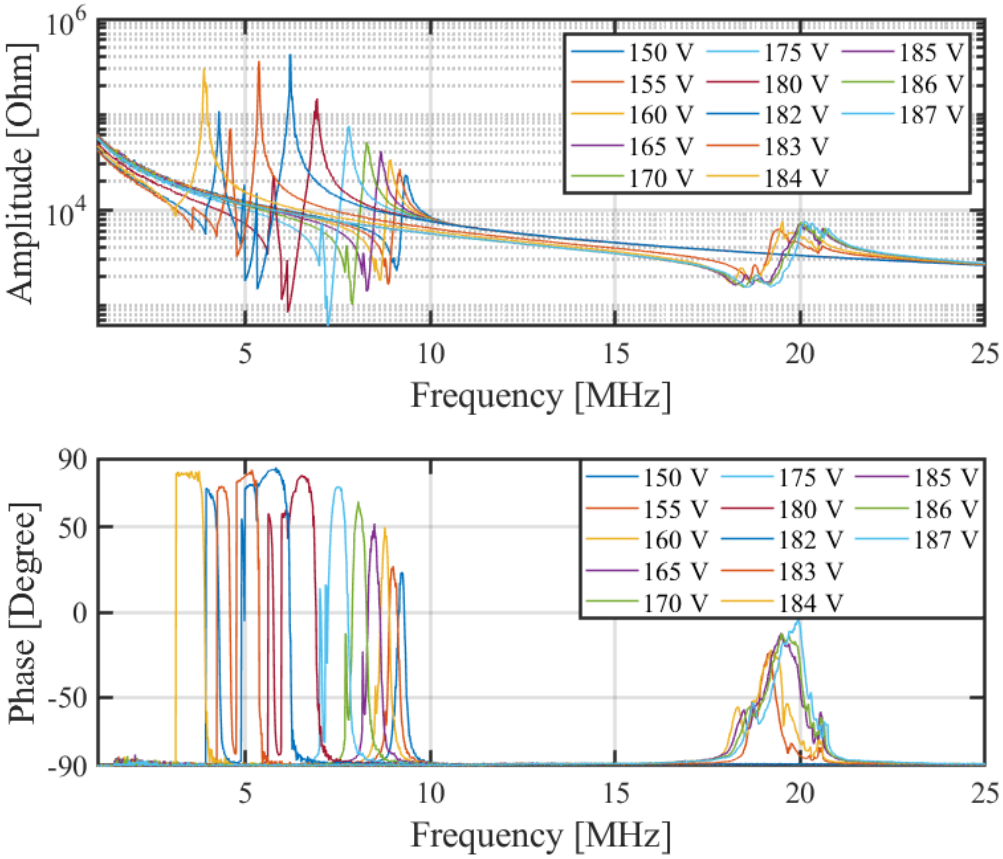


Figure 6.2: Impedance measurement of a CMUT test element from 150 V to 187 V DC bias and 50 mV AC. Data is from a north-western placed test element on chip 1.

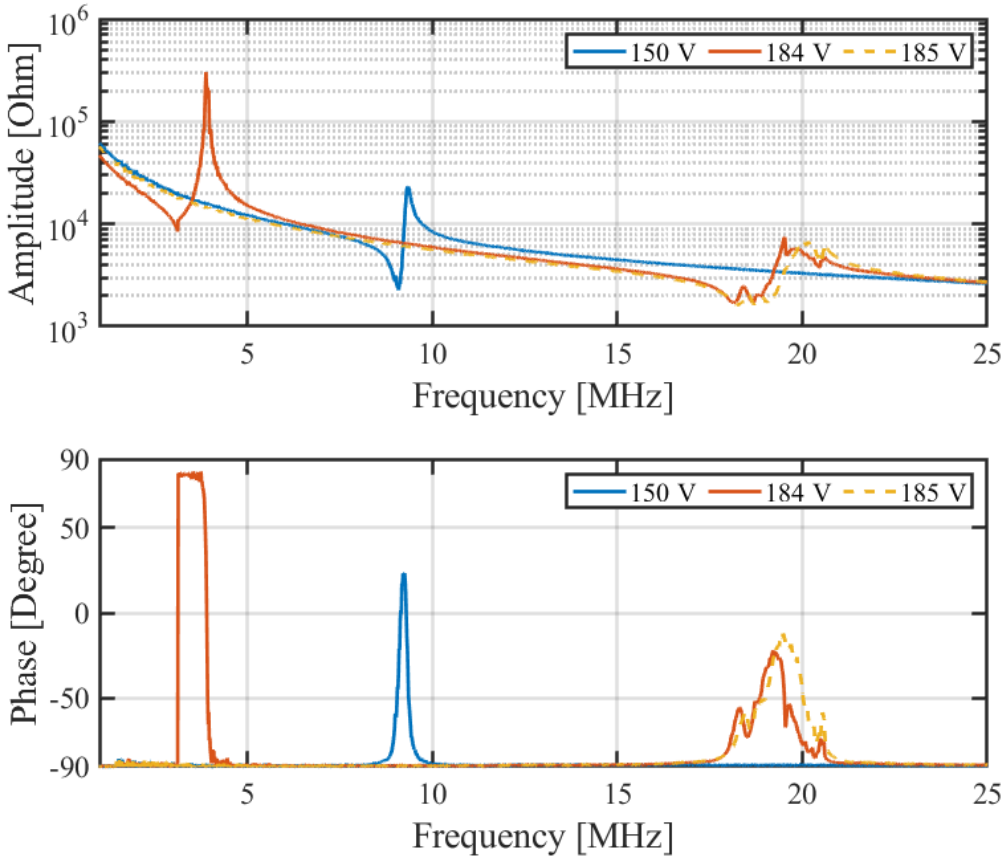


Figure 6.3: Impedance measurement of a CMUT test element from plotted for a DC bias of 150 V (operational voltage), 184 V (before pull-in) and 185 V (after pull-in). The AC voltage used is 50 mV. Data is from a north-western placed test element on chip 1.

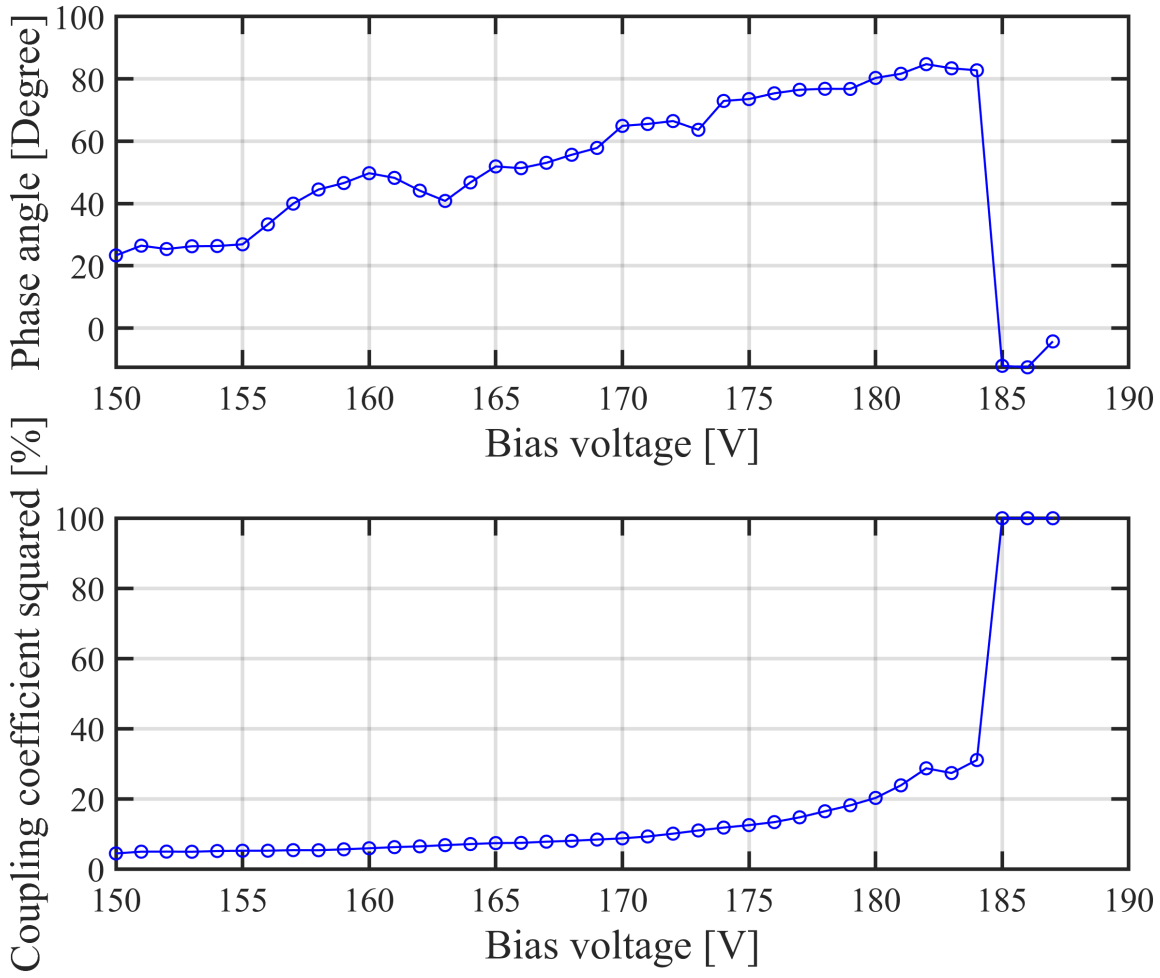


Figure 6.4: The maximum phase angle and coupling coefficient squared plotted as a function of DC bias voltage. The pull-in voltage is just at 184 V to 185 V as seen by the shift in phase angle and increase in coupling coefficient. Data is from a north-western placed test element on chip 1.

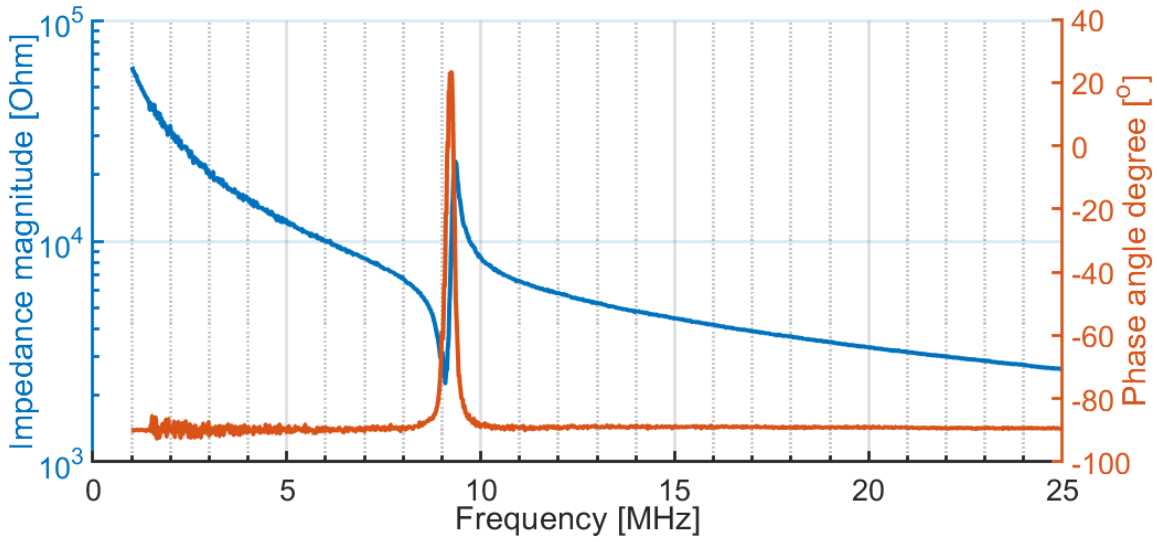


Figure 6.5: Impedance measurement of a CMUT test element at 150 V DC bias and 50 mV AC. The resonance and anti-resonance peaks are seen at 9.1 MHz and 9.3 MHz, respectively. Data is from a north-western placed test element on chip 1. From [1].

6.2 Probe assembly

The author of this thesis has not participated in the assembly of the probe. The following section will therefore give brief a overview of the steps involved, where further details are given when available. Most of the probe assembly was performed at BK Medical (State College, PA, USA), formerly known as Sound Technology, Inc., except for the chip mounting and wire bonding which as done at DELTA A/S (Hørsholm, Denmark).

6.2.1 Chip mounting and wire bonding

When the arrays of interest have been electrically characterised on wafer level, using the semi-automatic probe station, the arrays are diced into chips on the DISCO saw mentioned in Chapter 5. Two arrays were diced into chips and given the names *TR2-1* (chip 1) and *TR2-2* (chip 2), as mentioned in Chapter 5. Some of the electrical impedance measurements from these two were shown in 6.1.1. As mentioned in Chapter 5 both of the chips from the finished wafer showed some form of contact pad and element damage or short-circuiting. The assembly was done with both the TR2-1 and TR2-2 chip, with the most promising being TR2-2 chip which showed the least element damage. They are shown in Fig. 5.5, where multiple holes in the plate are seen in the northern part of the TR2-1 chip as dark spots. The diced chips were sent to DELTA where they were glued to a rigid-flexible four-armed PCB, which is represented as a 3D CAD drawing in Fig. 6.6. The bonded chips were then wire bonded using wedge bonding with aluminium wires connecting the row and column contact pads to the PCB pads. The glued and mounted TR2-2 chip, which will be the chip of interest in the following sections, can be seen in Fig. 6.7 and a close-up of the wire bonds shown in Fig. 6.8.

6.2.2 Encapsulation and shielding

To protect the chip and wire bonds from mechanical and chemical damage when handled it will be encapsulated in room temperature vulcanizing (RTV). This is also necessary to provide patient safety during operation of the probe. The silicone also ensures good acoustical matching from the CMUT to the scanned medium. An epoxy based glue is used to glue strips of plastic along the edge of the PCB to create a dam around the chip, seen in Fig. 6.9. The strips used were 485 µm

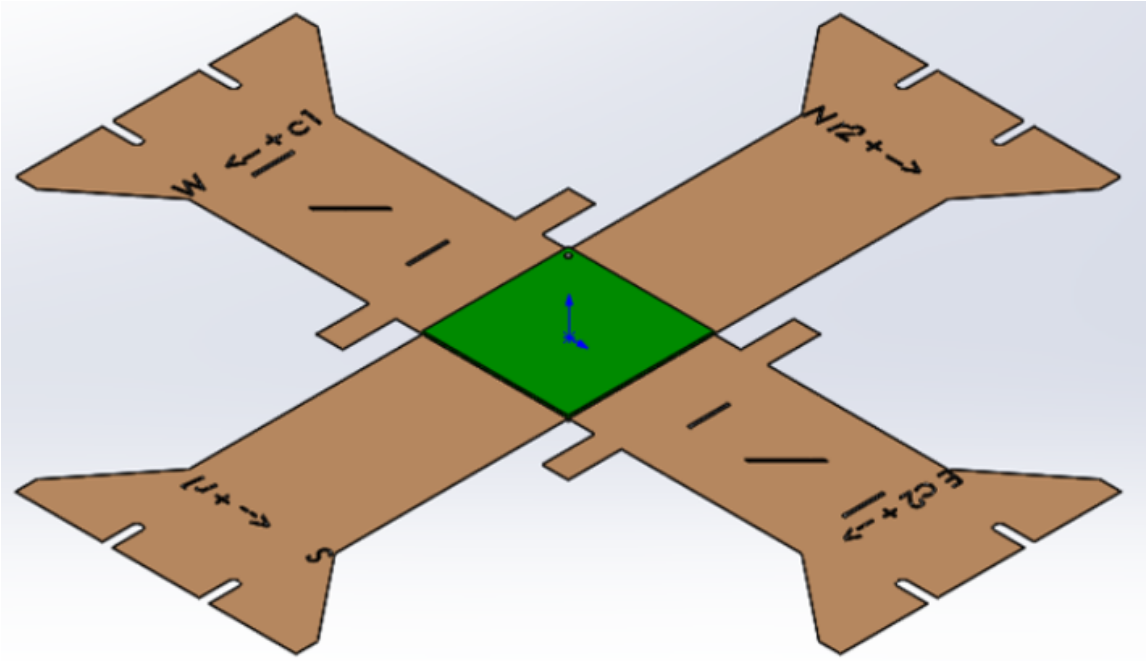
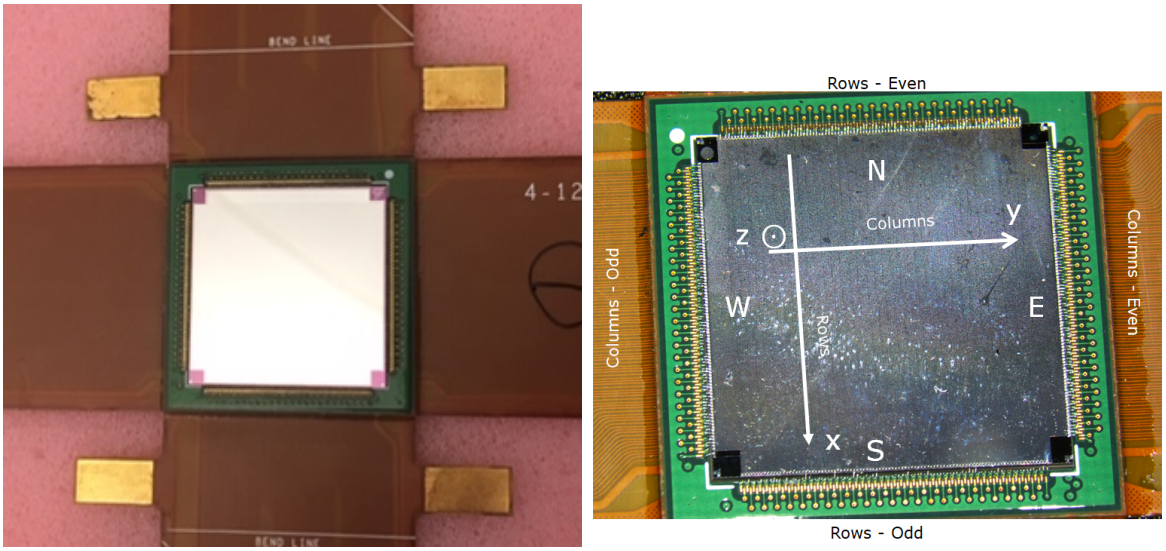
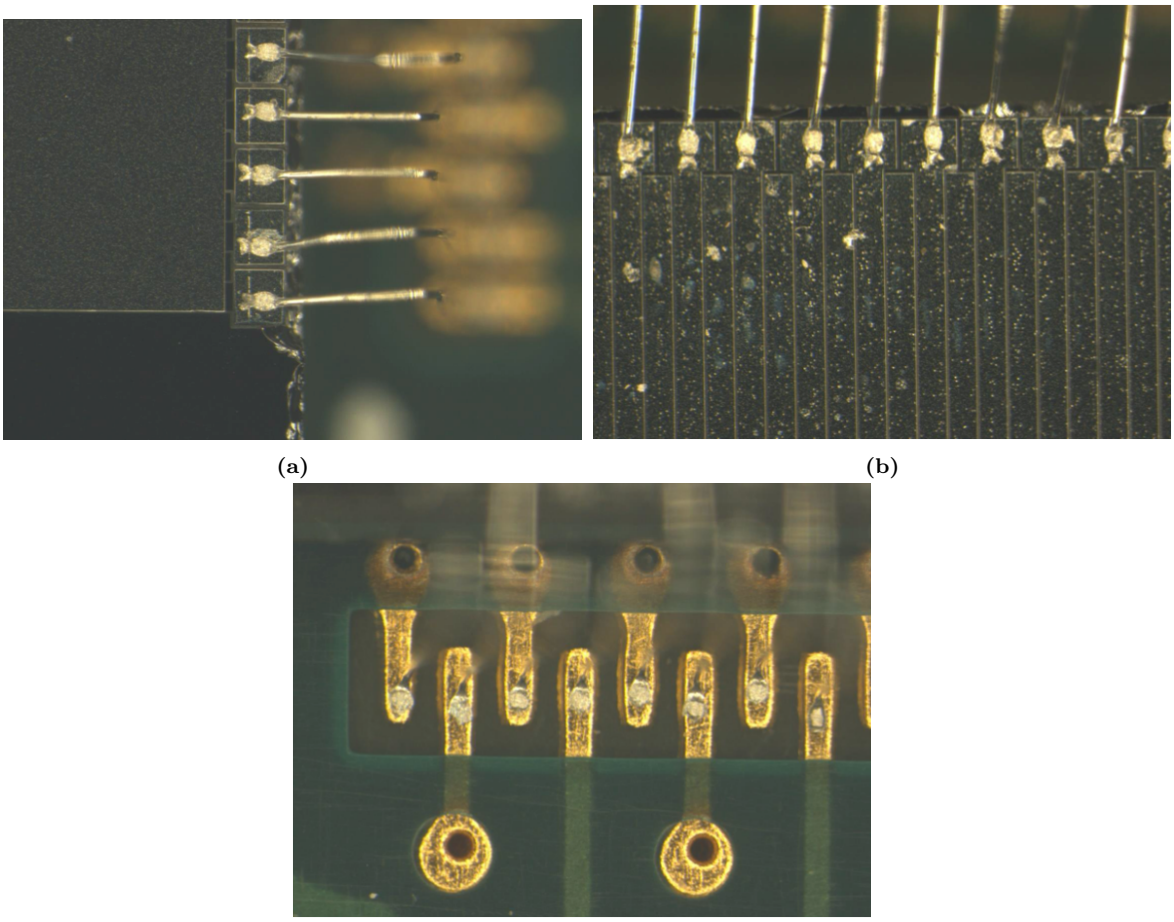


Figure 6.6: 3D drawing of the rigid-flexible PCB. The green center square of the rigid PCB part where the chip is mounted with glue. The dot in the north-western corner of the chip is aligned with the dot on the PCB. On each section of the flexible connectors are indicated the orientation of the chip of the starting row or column number for that connector, e.g. "N r2+->" indicating the north side of the chip starting with the even row element r2, counting up towards the right.



(a) **(b)**

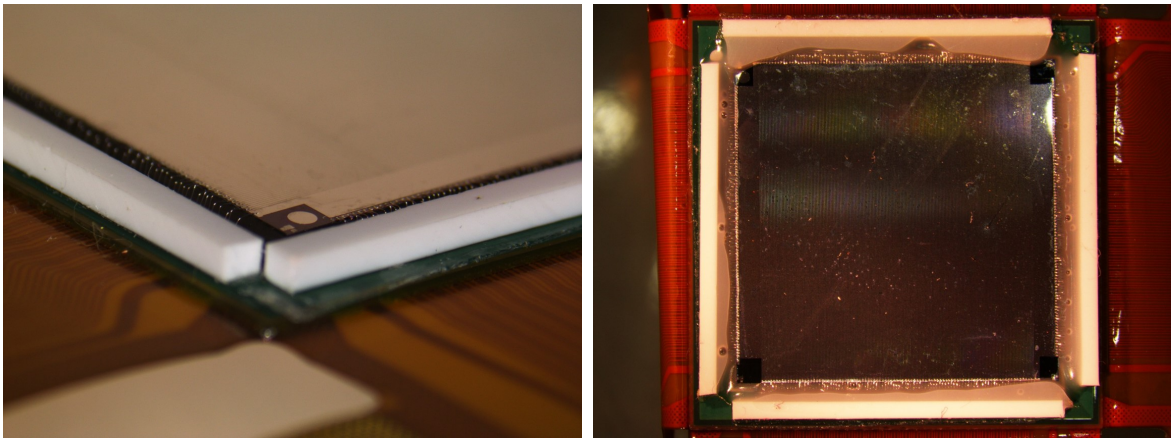
Figure 6.7: The TR2-2 chip is seen mounted on the PCB (a) [1]. and a closer look shows the chip alignment on the PCB as well the coordinate system in reference to the odd and even rows and columns (b).



(a) **(b)**

(c)

Figure 6.8: Close-up photos of the wedge wire bonding performed on contact pads of the columns (a) and of the rows (b) as well as on the PCB. None of the severely damaged contact pads with wire bonds have been documented.



(a) **(b)**

Figure 6.9: Photos showing (a) the placement of the plastic strips on the PCB and (b) the application of epoxy glue to protect the wire bonds and to create a dam for the first RTV polymer layer.

higher than the chip itself, which is approximately 600 µm thick, and the cavity is then filled with RTV, RTV664 (Momentive Performance Materials Inc., Waterford, NY, USA), which is described in more detail in [46] and [118]. The attenuation of the RTV was 2.3 dB mm^{-1} at 4.5 MHz, so the total one-way attenuation is 2.3 dB for this array.

Before the silicone cures, an aluminised film is layered on top of the dam and taped to the folded flex print and planarized. The film is an 12.5 µm polypropylene polymer with a sub-micron thick aluminium layer, sold as Torayfan PC3 (Toray Plastics (America), Inc., North Kingstown, USA). It is used as an electromagnetic interference (EMI) shield.
Fig. 6.10a shows the nose piece at this point in the assembly process.

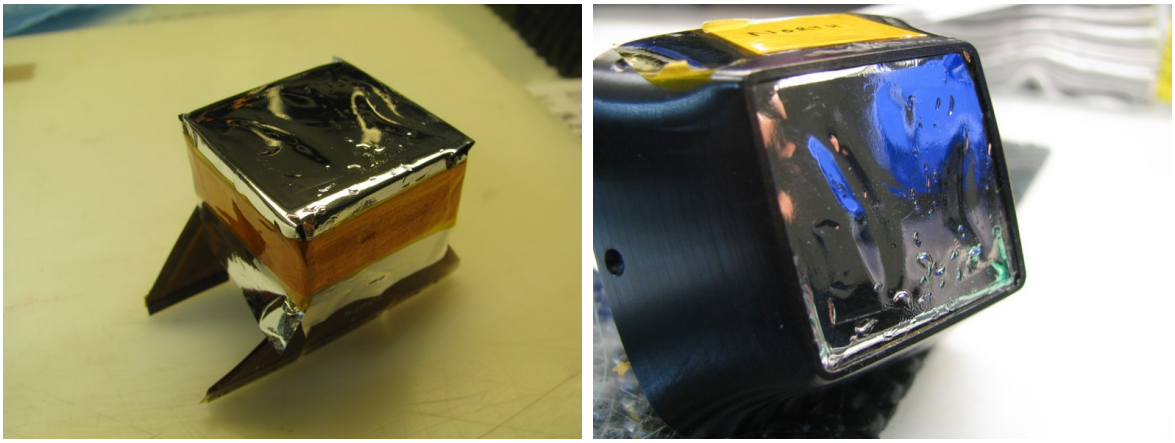
When the silicone is finally cured the flex-PCB is mounted in the nose piece, which is a separate section of the probe handle, seen in Fig. 6.10b. The handle is made up of three pieces; two shells for the main body and a nose piece, which are made in PPSU plastic using a 3D milling process. The pieces fit seamlessly together and is fully sealed when glued and assembled.

A final layer of 595 µm RTV664 silicone is mixed and applied on top of the shield and the front sole of the transducer is planarized while the silicone cures.

6.2.3 Electronics

The four sections from the flex-PCB are each connected to a preamplifier board also used for the Tabla-V probe (192 elements). The boards are each equipped with six MAX14822 16-channel high voltage (HV)-protected low noise operational amplifier ICs with a bandwidth of 45 MHz. These amplifiers are capable of passing the high voltage AC in transmit (TX) and receive (RX) individually on each channel of the probe. Each board has support for 96 channels, and two boards, pairing either the odd or even element, are connected with board-to-board connectors. A photo of a single board is seen in Fig. 6.11a. Each pair of amplifier boards were connected to a 192 odd or even channel coaxial scanner cable (BK Medical, Herlev, Denmark), as seen in Fig. 6.12c and Fig. 6.12b. The board pairs were then shielded in Kapton and copper tape. Two cooling hoses for inlet and outlet were then encapsulated along with the boards before the probe is sealed in Fig. 6.13.

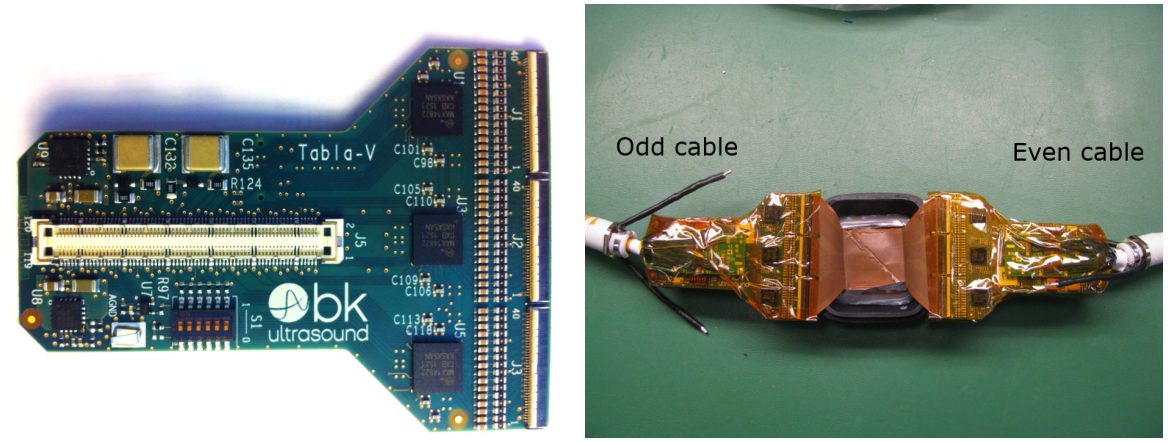
Before the probe is completely sealed, the bias voltage of ±95 V is applied (conforming to the maximum bias voltage of the BK3000 scanner) and the current and voltage is probed near the chip in the flex print for each element. This is done so to make sure that each element receives the same bias voltage. Due to element connectivity defects, such as varying high-resistance shorts between



(a) **(b)**

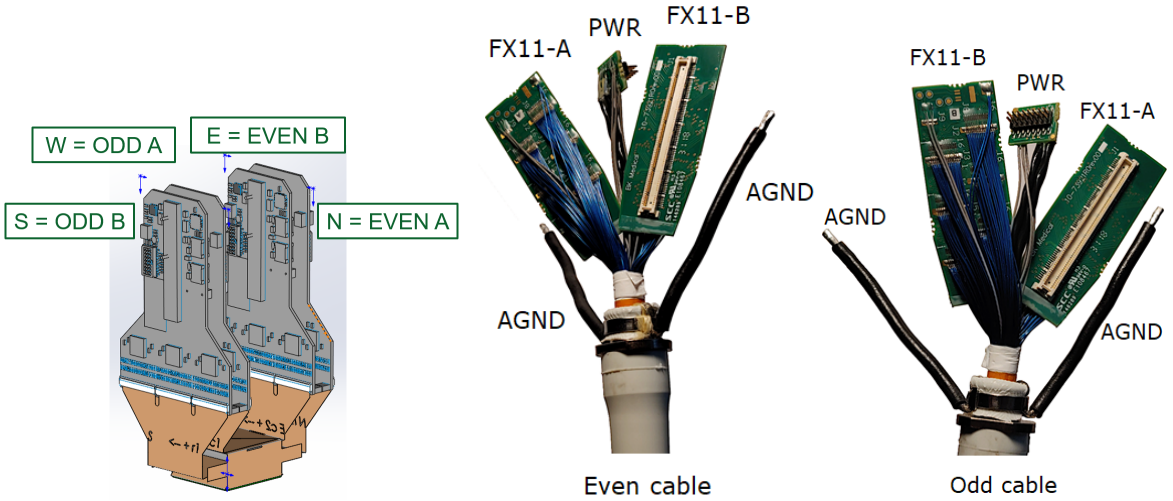
Figure 6.10: The photos show the assembly in progress just after the application of the first RTV silicone layer on the chip and the applied aluminised polymer grounding shield (a) and the subsequent mounting of the array in the nose piece (b).

elements, the bias voltage on many elements measured to be ±67 V. To accommodate for this voltage drop (as well as the drop across the probe electronics), the individual resistor values were adjusted to approach the target bias of ±80 V, which ultimately became ±82 V for a bias of 164 V($0.89V_{\text{pull-in}}$).



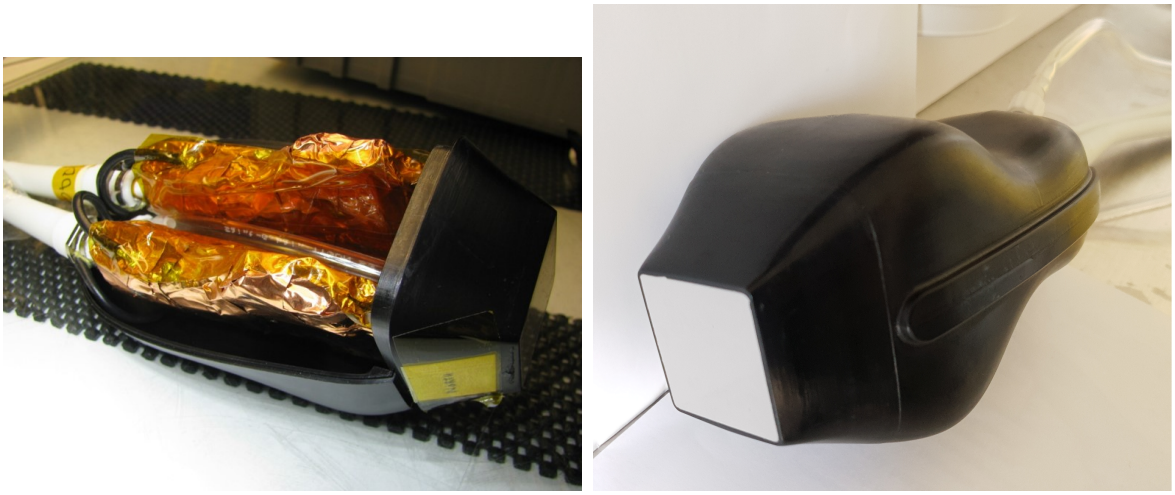
(a) (b)

Figure 6.11: In (a) an overview photo of the preamplifier board from BK Medical is shown. This was also used for the TABLA V probe, and three of the six MAX14822 low noise amplifier chips equipped on the board is shown on this side as well as the white connector socket for the BK cables. In (b) the probe nose piece is shown with the shielded odd (left) and even (right) stack of boards connected to their respective cables. The stiff black wires are grounding cables which will be connected to a shielding copper foil and the grounding shield on the chip. A 3D view of the stack as well as photos of the cables are seen in Fig. 6.12a.



(a) (b) (c)

Figure 6.12: A 3D model view of the connected odd and even preamplifier board pairs illustrated in (a). Photos of the even (b) and odd (c) cables are shown with the two board connectors together with black grounding cables (AGND) and power leads (PWR).



(a) (b)

Figure 6.13: Photos of the shielded electronics and inlet air tube half-assembled in the probe housing (a) and the finished sealed probe (b).

6.3 Acoustic Characterisation

The CMUT probe was acoustically characterised using the synthetic aperture real-time ultrasound system (SARUS) [119] which is a scientific research scanner at the CFU at DTU, capable of acquiring SA data for multiple probes. The scanner seen in Fig. 6.14. SARUS is equipped with 1024 individually programmable channels which can be used either in transmit or receive mode and is capable of transmitting arbitrary waveforms controllable from MATLAB. The system was used to perform a series of experiments for evaluating the performance of the probe. An automated scanning system, the Acoustic Intensity Measurement System AIMS III (Onda Corporation, Sunnyvale, USA), was used together with a water tank to perform measurements in immersion. The setup is illustrated in Fig. 6.16. A custom set of functions and control software was developed locally in MATLAB to interface with the accompanying software and in parallel with SARUS. The stage controlling the hydrophone is capable of translation in an x-y-z coordinate system and rotation in the x-y and z-y plane to account for tilt adjusting of the source probe.

The characterisation will be based on the following conducted experiments:

- First a hydrophone will be submerged in deionised (DI) water and used to perform one-way impulse transmission measurements.
- A planar PMMA reflector plate is placed in the water 35 mm from the transducer surface to perform two-way pulse-echo receive measurements.
- The hydrophone is used to generate pressure maps of the transmitting elements by scanning in a plane in front of and parallel to the probe surface.
- The imaging capabilities of the probe is characterised by performing volumetric imaging on 3D phantoms.

The first two experiment types are presented in the following Section 6.3.1 and the last two in Section 6.3.3 and 6.5.1.

6.3.1 Impulse response

The impulse response of the transducer probe is the response or reaction of the dynamic system when a signal or an impulse is used as excitation, ideally when a very short delta Dirac pulse is used.

Figure 6.14: Photo of the SARUS system.

The transfer function between the input pulse and the output response probe system, does not only include the probe but strictly includes both the SARUS system and the connected emitting probe. In other words the transfer function is here the signal path through the system which transforms the input pulse at MATLAB/SARUS to the output pressure emitted from the probe.
The purpose of these types of measurements is to the determine the transmit sensitivity and receive sensitivity as well as the frequency response of each of the CMUT elements to ascertain the operating frequency and bandwidth in immersion.
This is done for both rows and columns, referred to as top and bottom electrodes, respectively.
The sensitivity of the impulse response can be used to compare probes if they are of a similar fabrication structure with approximately the same element count and relative operating voltages to their respective pull-in voltage. However, it is likely not suitable for comparing different probe types. Instead a relative comparison of amplitude can be used between the probes, at 80 %-90 % of $V_{\text{pull-in}}$, and for comparison of the performance of the rows and columns in the same probe.

Both transmitting and receiving was done with one element at a time for all rows and columns, respectively. The DC bias was set to 160 V(±80 V) at chip level and the AC excitation voltage set to 150 V peak-to-peak (±75 V). The voltage levels were set to reflect the measured pull-in voltage mentioned in Section 6.1.1.

After the impulse response has been measured, performance of each element is then evaluated by considering two criteria. The first is the amplitude of the impulse response or the sensitivity. They are grouped into three different categories depending on their maximum impulse response values and designated as either *good* performing functional elements, *less good* semi-functional elements, and *bad/not connected (NC)* elements.
The cut-off threshold is not a fixed value used for both transmit and receive impulse responses. It was instead determined heuristically by inspecting how the elements are distributed according to their maximum impulse response values when plotted in a histogram. Alternatively, a threshold of < 0.6 of the average impulse can be used as a starting value. The second sorting criterion used to determine malfunctioning elements can be to find the time delay between a single element and the

(a) (b)

Figure 6.15: The TR2 probe fastened in CAD designed 3D printed formfitting holder for the Acoustic Intensity Measurement System AIMS III (AIMS) setup (a). Receiver Onda HGL-0400 hydrophone mounted on a the movable arm in in AIMS III tank (b).

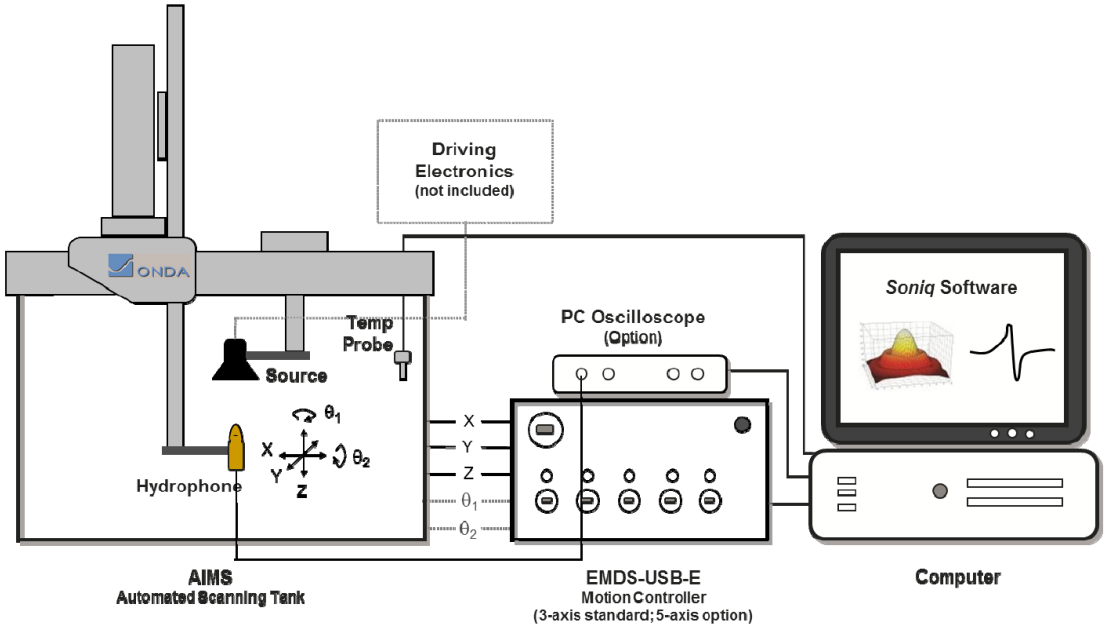


Figure 6.16: Sketch of Onda AIMS setup.

average of all the impulses by cross-correlation, and discard it if the lag is larger than $\lambda/2$.

Transmit

The transmission impulse response functions are acquired as mentioned before using SARUS to which the TR2 probe is connected using the odd and even scanner cables. The transmitting transducer probe is mounted in a CAD designed 3D printed formfitting adapter, see Fig. 6.15a, attached to a fixed arm connected to the Onda AIMS III water tank. The sole of the transducer is lowered just below the surface of the water. An Onda HGL-0400 hydrophone connected to an Onda AH-2010 amplifier is attached to the movable arm and submerged in the water tank just below the water surface filled with DI water, as seen in Fig. 6.15b without the probe.

For characterising the impulse response a burst signal is not used as excitation, instead a coded stochastic white noise signal generated in MATLAB, with near constant intensity for all frequencies, is repeated 50 times and averaged for each element. This is done to improve the signal-to-noise ratio of the recorded transmission. The pressure signal recorded by the hydrophone is then cross-correlated with the averaged stochastic signal to find the transmit impulse response, as described in [120], [121].

The results from the averaged transmit measurements are seen in Fig. 6.17 where the x-axis shows a cropped section view of the much larger recorded time signal and a 1 µs window is shown for illustrative purpose. The y-axis has the units $\mathrm{Pa\,V^{-1}\,s^{-2}}$ to factor out the area and distance dependency of the measurement when used to estimate the impulse response, which is explained in [120], [122]. All the elements have been grouped in Fig. 6.18 according to their peak amplitude and the cut-off values were chosen heuristically based on the groups. The elements with a peak sensitivity value $> 1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ are designated functional elements and amount to 109 rows and 123 columns. The number of semi-functional elements in the range between $2.9 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ is 52 rows and 32 columns. The NC elements amount to 29 rows and 35 columns. The numbers and yield in percentage are listed in Table 6.1.

Both the signal from the rows and the columns are plotted together in Fig. 6.17 with the envelope in dB, normalised to the maximum value of the signal. The average response is found by cross-correlating the responses to the middle element and aligning them by the calculated time delay.

The log-compressed spectra of the average impulse responses have also been calculated using fast Fourier transform (FFT) and plotted in Fig. 6.19 for rows and columns and normalised to their maximum impulse values $5.62 \times 10^{14}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.22 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$, respectively. The peak amplitude of the two spectra are surprisingly not located at the same frequency. The data will be discussed further in Section 6.3.2.

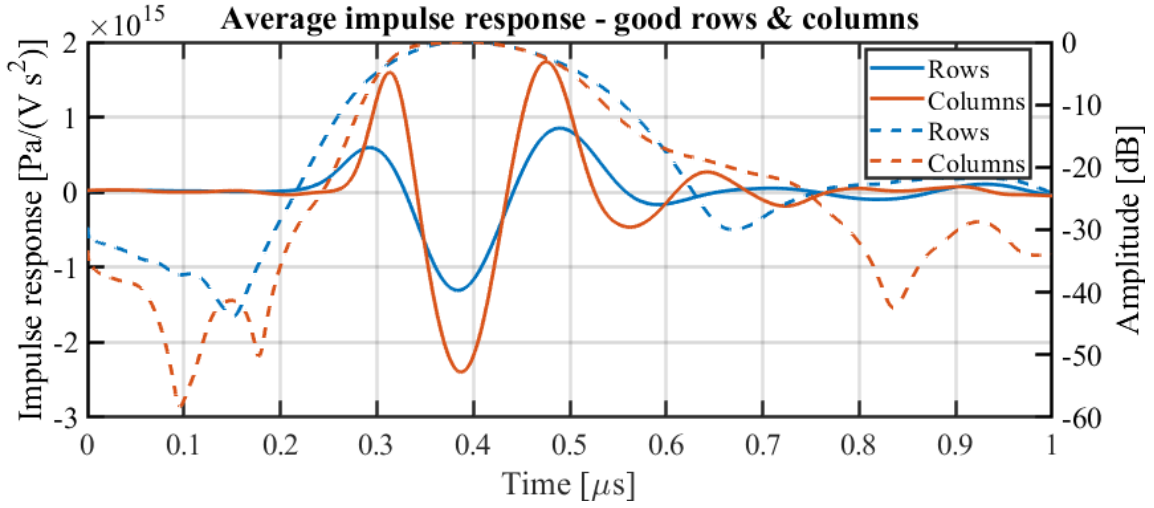


Figure 6.17: Average transmit impulse response (TX), as solid lines, and the normalised envelope (in dB), as dashed lines, of the functional row and column elements with amplitudes above 1.1×10^{15} Pa V^{-1} s^{-2}. From [1].

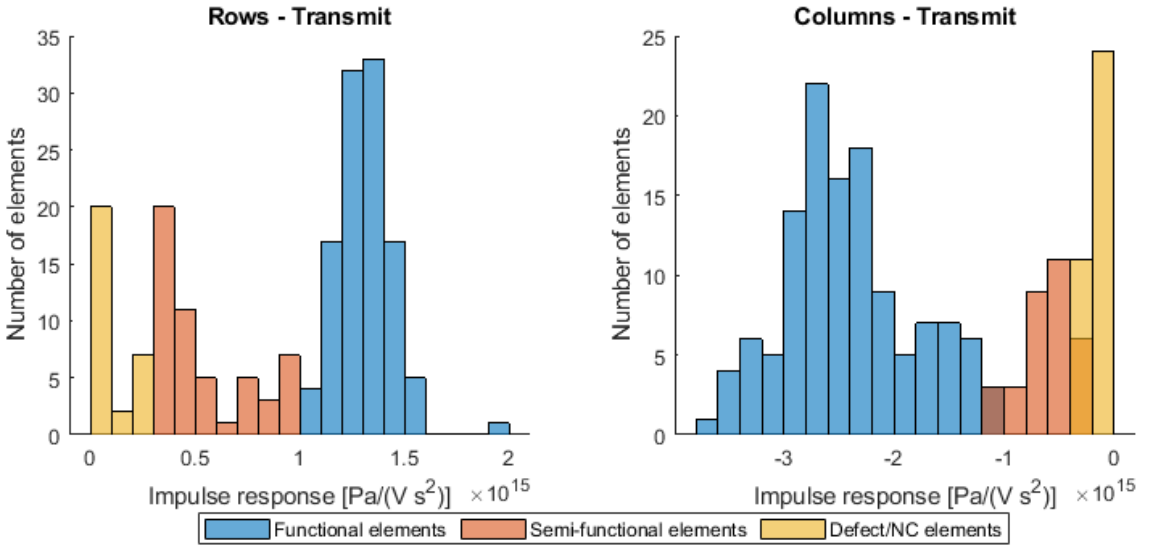


Figure 6.18: Histogram of the transmit impulse response of all row and column elements. The elements are grouped into three categories depending on their maximum impulse response values. From [1].

Pulse-echo

For characterisation of the pulse-echo (PE) impulse response, where the elements are used to transmit and then receive, a PMMA reflector plate was placed with a distance of 35 mm from the transducer surface. The reflecting plate was aligned with respect to tilt by inspecting the echo of selected elements of the probe. A coded stochastic signal was used with 50 averaged emissions as excitation.

The results from the averaged and aligned pulse-echo measurements are seen in Fig. 6.21. Both the signal from the rows and the columns are likewise plotted together with the envelope in dB. The y-axis is expressed in the units V V^{-1} as the value recorded by the transducer probe is relative to the amplitude of the transmitted pulse.

The elements used in the receive (pulse-echo) measurements are also grouped according to their

Table 6.1: Overview of the yield and associated transmit impulse amplitude cut-off values for each of the three element categories; functional, semi-functional and bad/NC.

Element category	Cut-off value $[\mathrm{Pa\,V^{-1}\,s^{-2}}]/10^{15}$	Amount (% yield of 190)		Total yield (of 380)
		Rows	Columns	
Functional	>1.1	109 (57.4 %)	123 (64.7 %)	61.1 %
Semi-functional	0.29<i ≤ 1.1	52 (27.4 %)	32 (16.8 %)	22.1 %
Bad/NC	<0.29	29 (15.3 %)	35 (18.4 %)	18.8 %

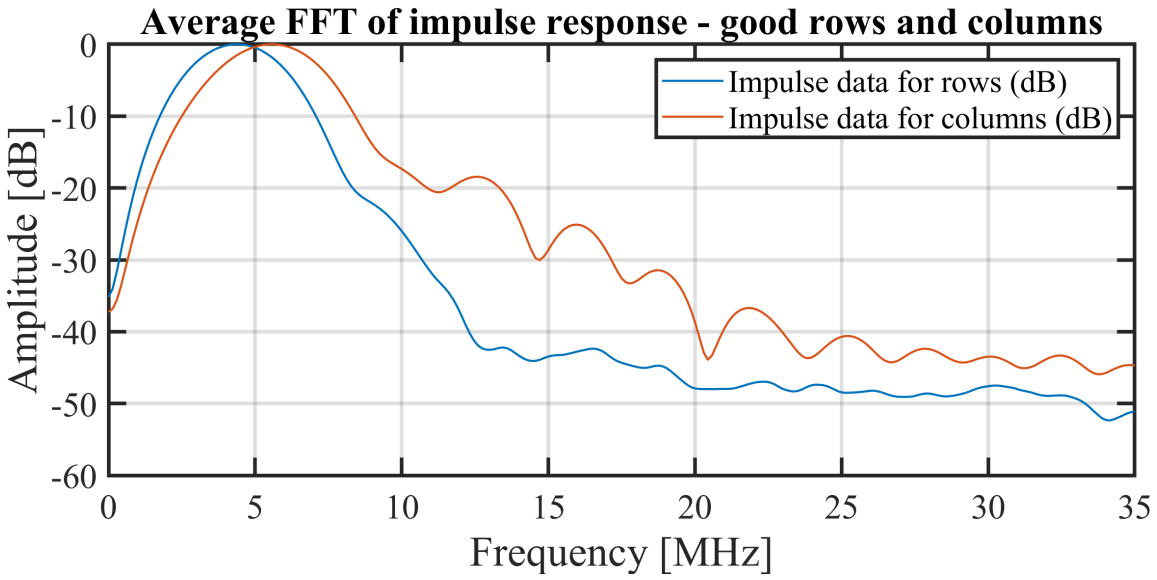


Figure 6.19: Average FFT spectra of the impulse response in transmit (TX) of the functional row and column elements with impulse response amplitudes above $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$. The spectra for the rows and columns are normalised to the maximum of the average impulse responses with the values $5.62 \times 10^{14}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.22 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$, respectively. From [1].

Table 6.2: Overview of the yield and associated pulse-echo impulse amplitude cut-off values for each of the three element categories; functional, semi-functional and bad/NC.

Element category	Cut-off value $[\mathrm{V/V}]/10^{-4}$	Amount (% yield of 190)		Total yield (of 380)
		Rows	Columns	
Functional	>1.4	125 (65.8 %)	83 (43.7 %)	54.7 %
Semi-functional	0.65<i *leq* 1.4	2 (1.1 %)	24 (12.6 %)	6.8 %
Bad/NC	<0.65	63 (33.2 %)	83 (43.7 %)	38.4 %

peak impulse response values, see Fig. 6.20. The peak impulse response cut-off threshold for the functional elements is set to $> 1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ (125 rows and 83 columns). The amplitude range for the semi-functional elements is between $6.5 \times 10^{-5}\,\mathrm{V\,V^{-1}}$ and $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ (2 rows and 24 columns). Finally the bad/NC elements below $6.5 \times 10^{-5}\,\mathrm{V\,V^{-1}}$ (63 rows and 83 columns). The numbers and yields are listed in Table 6.2.

The spectra of the average impulse responses are plotted in Fig. 6.19 for rows and columns and normalised to their maximum impulse values $2.11 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ and $7.63 \times 10^{-5}\,\mathrm{V\,V^{-1}}$, respectively.

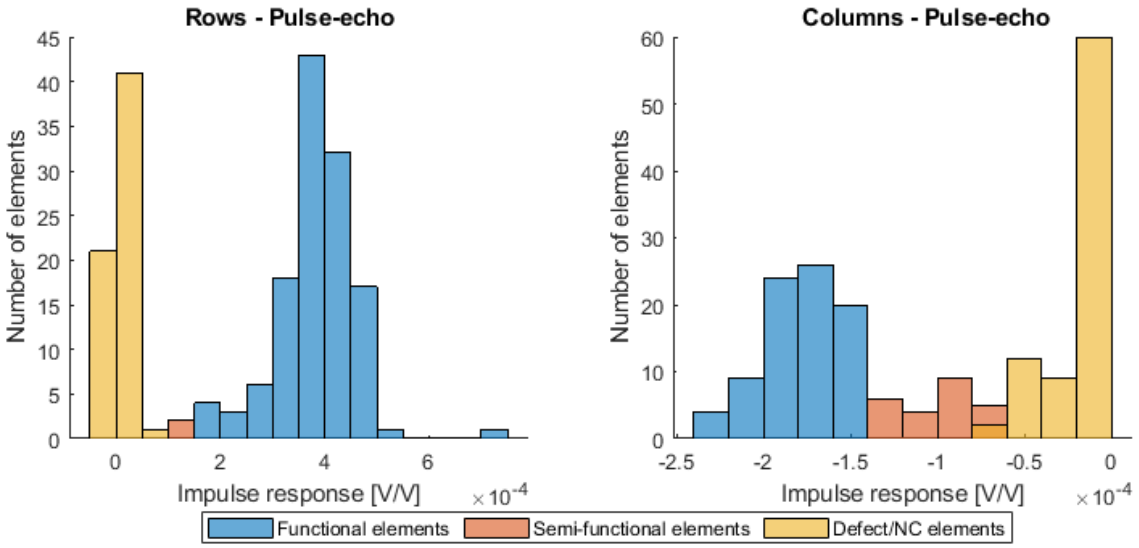


Figure 6.20: Histogram of pulse-echo impulse response of all row and column elements. The elements are grouped into three categories depending on their maximum impulse response values. From [1].

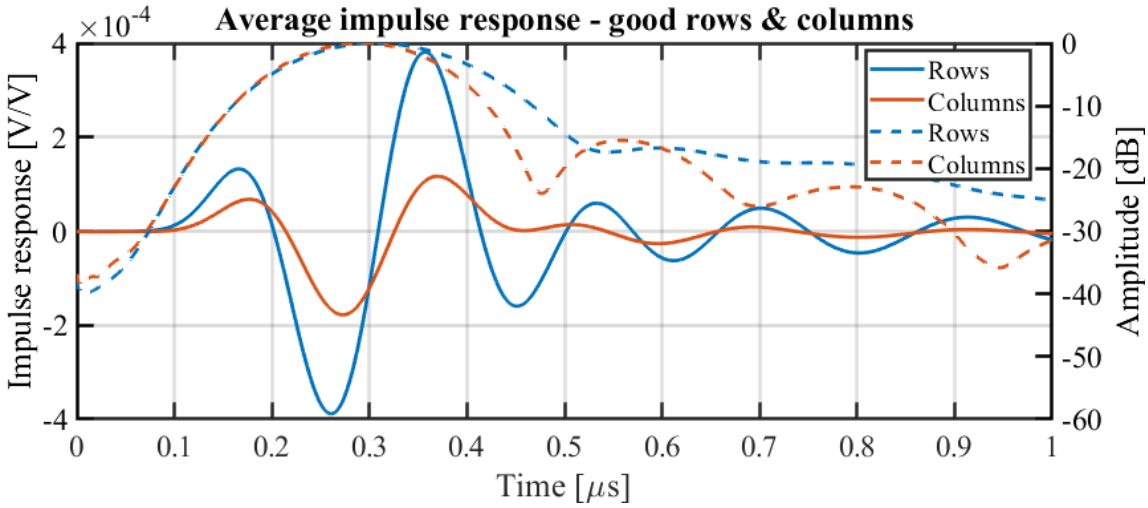


Figure 6.21: Average pulse-echo impulse response (PE), as solid lines, and the normalised envelope (in dB), as dashed lines, of the functional row and column elements with amplitudes above $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$. From [1].

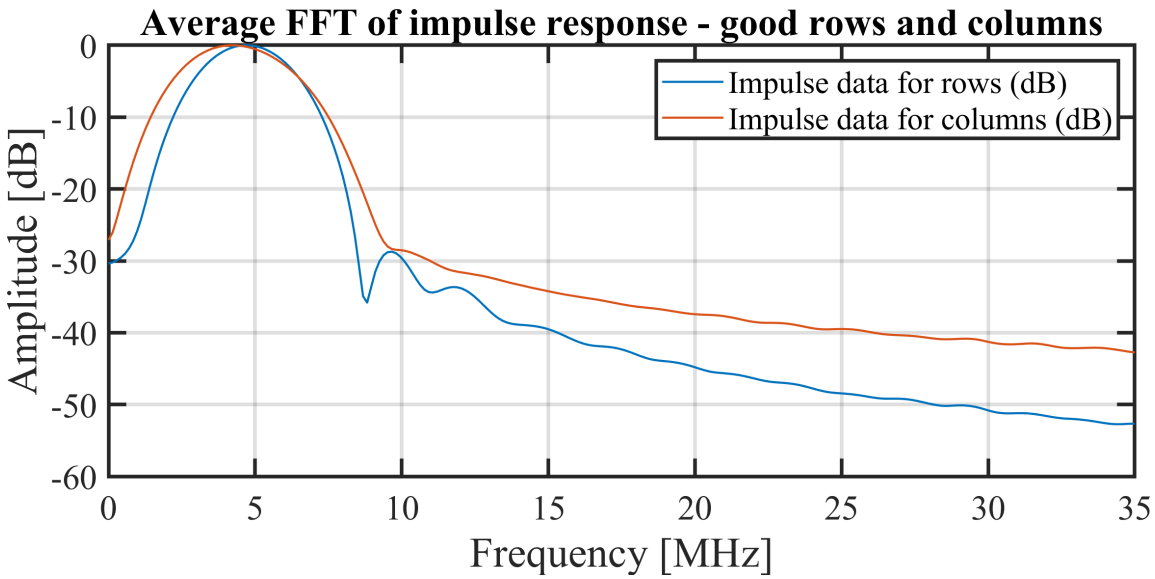


Figure 6.22: Average FFT spectra of the impulse response in pulse-echo (PE) of the functional row and column elements with impulse response amplitudes above $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$. The spectra for the rows and columns are normalised to the maximum of the average impulse responses with the values $2.11 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ and $7.63 \times 10^{-5}\,\mathrm{V\,V^{-1}}$, respectively. From [1].

6.3.2 Result analysis and discussion

The results and accompanying derived parameters will be discussed and compared between rows and columns for transmit and pulse-echo measurements.

With the impulse responses measured the center frequency can now be found from the spectra. The center frequencies of the rows and columns are found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses of the transmit and pulse-echo signals, which were plotted in Fig. 6.19 and Fig. 6.22, using the expression [46]:

$$f_c = \frac{\sum_{i=0}^{N/2} S(i\,f_s/N) \cdot i\,f_s/N}{\sum_{i=0}^{N/2} S(i\,f_s/N)} \tag{6.2}$$

where f_s is the sampling frequency which was 70 MHz and N is the number of frequency bins in the spectrum S. The sum is made up until 35 MHz (the Nyquist frequency at $f_s/2$), multiplying and weighing the amplitudes contained in S with the corresponding frequency and normalising with the sum of the components of S.

In the same vein, the bandwidth of the transducer can by found be normalising the spectra to the respective weighted center frequencies and finding the lower and upper frequency corresponding to a cut-off of $-3\,\mathrm{dB}$ ($\approx 0.71 \times$ signal amplitude) for the one-way transmission measurement (Fig. 6.19) and $-6\,\mathrm{dB}$ ($\approx 0.5 \times$ signal amplitude) for the two-way pulse-echo measurements (Fig. 6.22). The relative fractional bandwidth is then found, e.g. for $-3\,\mathrm{db}$, as

$$f_{\mathrm{rel.BW}} = \frac{f_{\text{-3dB,1}} - f_{\text{-3dB,2}}}{f_c} \times 100\,\% \tag{6.3}$$

where $f_{\text{-3dB,1}}$ and $f_{\text{-3dB,2}}$ are the two points on the frequency axis corresponding to $-3\,\mathrm{db}$.

The peak frequency is also extracted from the FFT spectra in Fig. 6.19 and Fig. 6.22, by taking the frequency on the x-axis associated with the maximum amplitude.

Transmit

From the averaged transmit impulse responses shown in Fig. 6.17 it can be seen that the rows has approximately half the transmit sensitivity (the amplitude on the y-axis) when compared to the columns ($\approx 55\,\%$ or a factor 1.8) but the shape of the envelope is the same except for a more pronounced side-lobe at around 0.8 µs to 0.9 µs. The impulse response of the columns (the bottom electrodes) show a slightly more pronounced ringing after the main pulse.

The probe is constructed with an additional borosilicate handling substrate as mentioned first in Section 1.4.2, which electrically insulates the elements from each other. It was therefore expected that the substrate coupling will be reduced significantly, and that the amplitude of the rows and columns were nearly the same. Any reduced sensitivity in the columns would be due to substrate coupling still present in the structure or a direct element-to-element coupling. Another unexpected parasitic capacitance in either the array or the probe and the integrated electronics might also contribute to a reduced sensitivity.

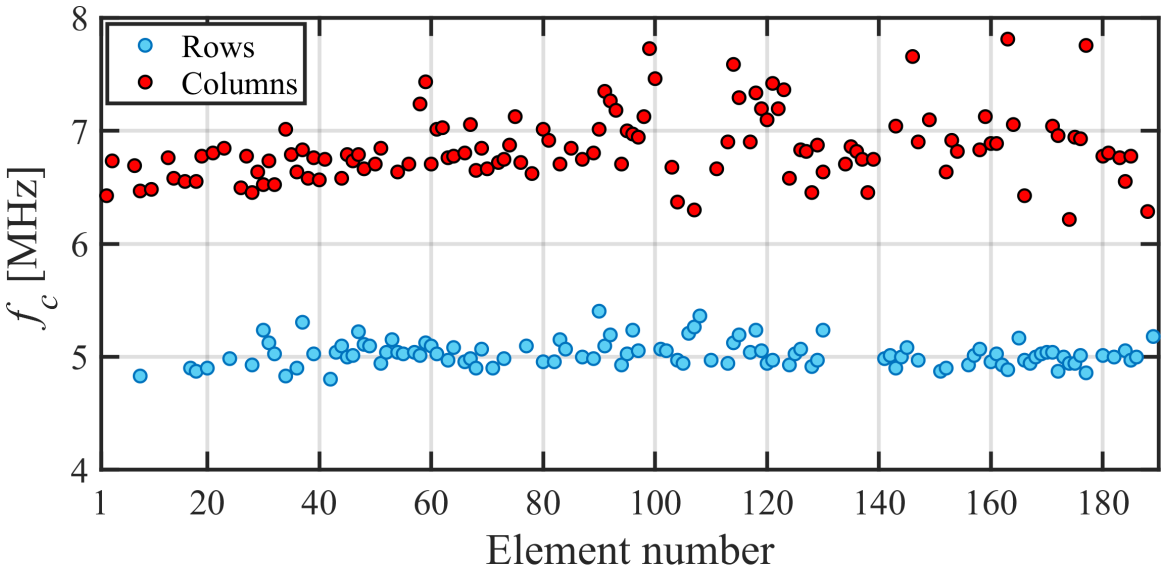
Referring to [78], the only other contribution to a parasitic capacitance should come from the post oxide when the top electrodes are probed. This will however also be present in the reverse configuration when columns are used for transmitting and can not be used to explain the lower amplitude. Since the capacitance and the relative change in capacitance of the elements with increasing bias were not measured before the encapsulation of the probe, the substrate coupling is not easily found.

The spectra shown in Fig. 6.19 shows a difference in the peak resonance frequency of the rows compared to the columns. The weighted center frequencies are plotted versus the element number, from 1 to 190, in Fig. 6.23(a), showing the uniformity across the array in transmit, and the values are listed in Table 6.3 together with the bandwidths. The extracted peak frequencies are also plotted in Fig. 6.24(a) and the average listed in Table 6.3. The average center frequencies of the functional row and column elements were $5.0 \pm 0.1\,\text{MHz}$ and $6.85 \pm 0.30\,\text{MHz}$, respectively, with the total average of rows and columns being $6.0 \pm 0.9\,\text{MHz}$ in transmit. This shift in center frequency of around $1.8 \pm 0.4\,\text{MHz}$ is currently not understood, as this would either mean a structural change in the CMUT which would affect both the rows and the columns, or that the resistor network or amplifiers for the rows were not working as intended and supplying a wrong DC or AC bias. A measurement performed on the same probe almost two years prior to the measurements presented here, showed an equal performance of the rows and columns in transmit.

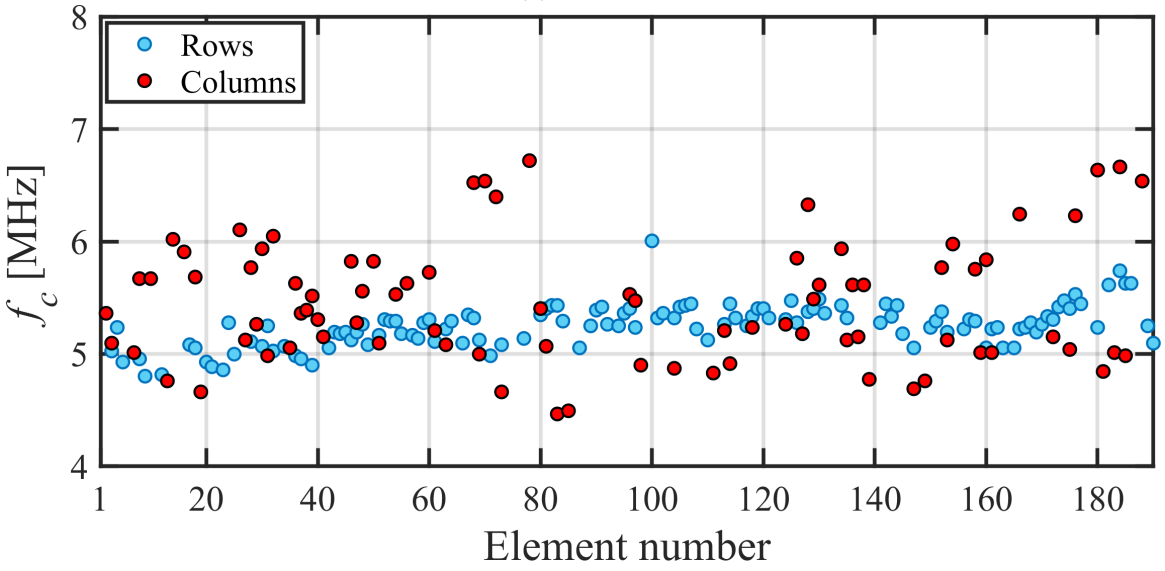
The total relative fractional bandwidth of both rows and columns is around $62 \pm 5\,\%$, which is a bit lower than previously fabricated arrays in this research group [86][82][83]. When comparing to the linear Tabla V-VI probes (192 elements) with peak and weighted center frequencies comparable to the TR2 probe, the bandwidth is between 61.7 % and 96.6 %, presented in the PhD thesis by Søren E. Diederichsen from this group [86, p. 138]. It is, however, not ideal comparing bandwidths across different probe generations and geometries, as the individual designs might be optimised for more output pressure by sacrificing bandwidth.

The peak frequency was also extracted, seen in Fig. 6.24a, from the spectral data and gave an average of $5.0 \pm 0.6\,\text{MHz}$. A difference of around $1.3 \pm 0.4\,\text{MHz}$ between the rows and columns is also seen here.

The earlier discussed Bragg frequencies and substrate ringing effect calculated in Section 2.1.7 are not clearly seen in the spectra in Fig. 6.19. No detectable dip in amplitude is observed around the center frequency at $\approx 5\,\text{MHz}$ as an effect of substrate ringing. A slight dip is observed at around 8.4 MHz and 9.4 MHz for the rows and columns, respectively, and for the columns at 11.2 MHz for almost $-2\,\text{dB}$ when compared to the lobe to the right. These are close in value to the expected Bragg frequencies, $f_{\text{B},1} = 9\,\text{MHz}$ and $f_{\text{B},2} = 11.46\,\text{MHz}$, presented in Section 4.2.

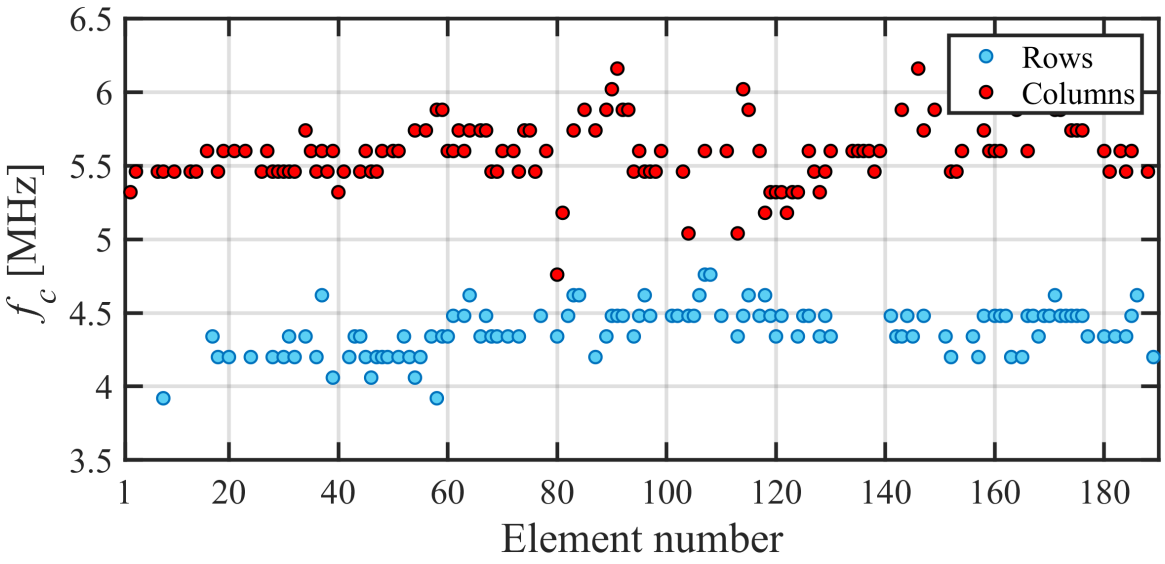


(a) Transmit

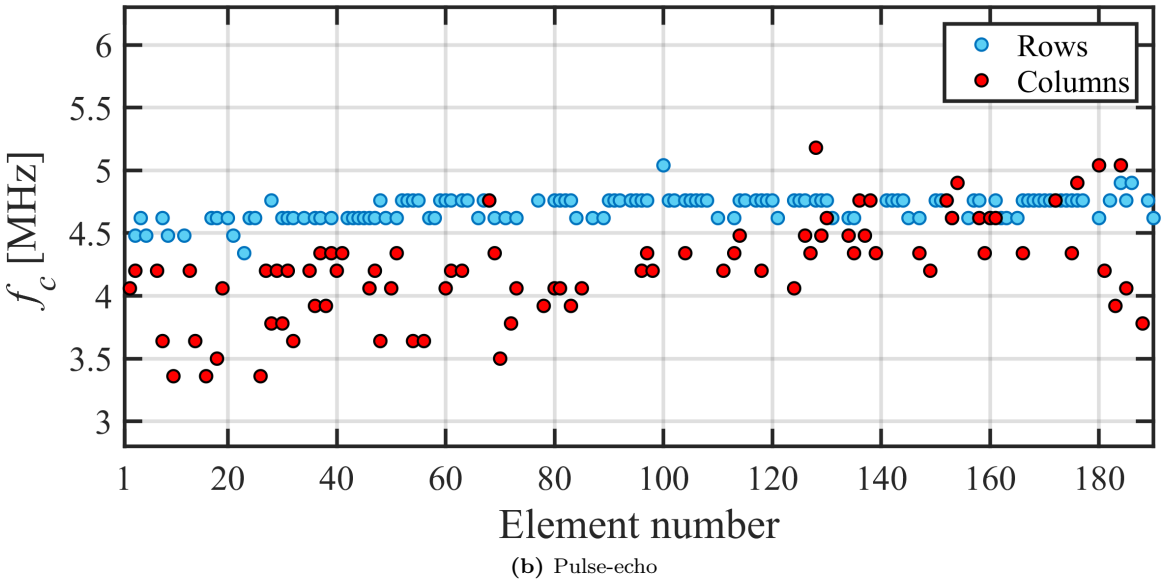


(b) Pulse-echo

Figure 6.23: Extracted center frequencies across the array for each element in transmit (a) and pulse-echo (b). The frequencies were found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses. The average center frequency of functional row and column elements in the probe is 6.0 ± 0.9 MHz in transmit and 5.3 ± 0.4 MHz in pulse-echo. From [1].



(a) Transmit



(b) Pulse-echo

Figure 6.24: Extracted peak frequencies across the array for each element in transmit (a) and pulse-echo (b). The frequencies were found by using a peak-finding algorithm in MATLAB. The average center frequency of functional row and column elements in the probe is 5.0 ± 0.6 MHz in transmit and 4.5 ± 0.4 MHz in pulse-echo.

Table 6.3: Results obtained from acoustical measurements of the probe in transmit and pulse-echo. From [1].

	Transmit			Pulse-echo		
Parameter	Row	Column	Total	Row	Column	Total
Center frequency [MHz]	5.03 ± 0.11	6.85 ± 0.30	5.99 ± 0.94	5.25 ± 0.19	5.45 ± 0.54	5.33 ± 0.38
Peak frequency [MHz]	4.38 ± 0.16	5.59 ± 0.25	5.02 ± 0.64	4.70 ± 0.09	4.21 ± 0.39	4.50 ± 0.35
Center frequency bandwidth [MHz]	3.28 ± 0.19	4.16 ± 0.37	3.74 ± 0.53	4.17 ± 0.13	5.27 ± 0.80	4.61 ± 0.74
Relative fractional bandwidth [%]	65.23 ± 3.69	60.68 ± 3.98	62.82 ± 4.47	79.47 ± 3.66	96.40 ± 8.77	86.23 ± 10.37
Sensitivity $[\mathrm{PaV^{-1}s^{-2}}]/10^{15}$	1.3 ± 0.1	2.4 ± 0.6	1.9 ± 0.7	—	—	—
Sensitivity $[\mu\mathrm{VV^{-1}}]$	—	—	—	380 ± 70	180 ± 20	300 ± 20

Pulse-echo

The averaged pulse-echo impulse response is shown in Fig. 6.21. In contrast to the impulse response transmit measurements it is now seen that the columns show a reduced receive sensitivity compared to the rows. The peak amplitude of the impulse response for the columns in Fig. 6.21 is decreased quite significantly by a factor of 2.4 (corresponding to $\approx 42\,\%$) compared to the rows in the same plot. As mentioned in the previous section, the sensitivities of the columns were expected to be close to the rows, with no silicon substrate to couple to, which has previously been the case. However, the low sensitivity could still be the result of element-to-element coupling or substrate coupling through the glass. Expanding on this explanation a few example calculations will be given below.

The sketch in [109] shows the probing configuration on a column element which has been fabricated with the SOI scheme, which is similar for the newer fusion-anodic scheme. The significant reduction in the impulse response amplitude of the columns can perhaps be found in the coupling present in the vacuum-filled kerf between the elements, $C_{\text{E-to-e}}$, sketched in Fig. 6.26, and in a coupling through the borosilicate glass wafer itself, C_{Boro}. The probed element is in this case element 1 with $C = C_{0,1}$ and the neighbouring element 2 has $C = C_{0,2}$. A simple estimate of the capacitance between two elements is

$$C_{\text{Element-to-element}} = \frac{\epsilon_0 L t}{d_{\text{kerf}}} = \frac{\epsilon_0 \cdot 20\,942.5\,\mu\text{m} \cdot 100\,\mu\text{m}}{2.5\,\mu\text{m}} = 7.4\,\text{pF} \tag{6.4}$$

with L being the element length, t the electrode thickness and d_{kerf} the kerf width. If an oxide with thickness, $t_{\text{kerf,ox}} = 716\,\text{nm}$, with the dielectric permittivity of ϵ_{ox}, grown on each sidewall of the kerf is included, the capacitance becomes

$$C_{\text{Element-to-element}} = \left(\left(\frac{\epsilon_0 L t}{d_{\text{kerf}}} \right)^{-1} + 2 \left(\frac{\epsilon_0 \epsilon_{\text{ox}} L t}{t_{\text{kerf,ox}}} \right)^{-1} \right)^{-1} = 6.5\,\text{pF}. \tag{6.5}$$

The coupling, if present, through the glass, will have a dielectric constant $\epsilon = \epsilon_{\text{boro}} \epsilon_0 = 4.6\epsilon_0$ times higher than if coupling through air or vacuum [110]. The capacitive contribution will, however, likely be reduced since it is a result of a fringing effect compared the parallel plate capacitance between the elements. One way such a fringe field capacitance between two flat electrodes through a substrate can be found is given in [123] as

$$C_{\text{Boro-fringe}} = \frac{4.6\epsilon_0}{\pi} \ln\left(1 + \frac{2W}{d_{\text{kerf}}}\right) L = 1.2\,\text{pF} \tag{6.6}$$

with W being the width of the electrode. This is also sketched in Fig. 6.25.

Referring to the circuit sketch in Fig. 6.26, calculating the right hand side capacitance, would be a contribution of

$$C_{\text{coupling}} = ((C_{\text{Element-to-element}} + C_{\text{Boro-fringe}})^{-1} + C_{0,2}^{-1})^{-1} \approx 5.8\,\text{pF} \tag{6.7}$$

for one nearest neighbouring element and the parasitic capacitances, considering that the theoretical element capacitance is 23.6 pF, found in Chapter 4. A contribution from both sides would be $C_{\text{couplingx2}} \approx 11.5\,\text{pF}$ which is 49 % of the element capacitance.
This will likely have a large impact on the receive sensitivity, as the relative change in capacitance due to plate deflection in receive mode, when compared to the static $C_{0,1}$ of the single element, will be smaller if a large portion of the static capacitance is parasitic. This will lower the effective coupling coefficient from the electrical to mechanical domain given by

$$k_{\text{eff,em}} = \frac{C_m}{C_m + C_{0,\text{total}}} = \frac{1}{1 + C_{0,\text{total}}/C_m} \tag{6.8}$$

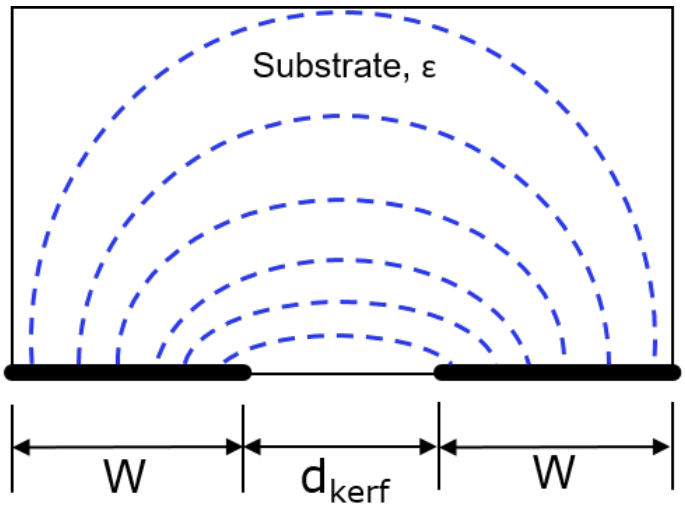


Figure 6.25: Sketch of the fringe electric field lines between the bottom of two electrodes with width, W, and the vacuum-filled kerf d_{kerf} separation. The structure is viewed upside down with the blue lines going through the substrate (indicated by the bounded box), with permittivity ϵ, creating a parasitic capacitance.

where $C_{0,\text{total}}$ is the total static element capacitance associated with a CMUT cell and C_m the lumped mechanical capacitance modelled in an equivalent circuit model, which incorporates the spring-softening effect. The coefficient describes the conversion of energy from one domain to another, and in this case from the electrical to the mechanical domain, also defined as

$$k_{\text{em}}^2 = \frac{E_{\text{mech}}}{E_{\text{total}}} = \frac{1}{1 + \frac{E_{\text{elec}}}{E_{\text{mech}}}} \tag{6.9}$$

and by including the plate deflection for a parallel plate model caused by a bias voltage, giving spring softening, it can be written as

$$k_{\text{em}}^2 = \frac{2\,x}{g_{\text{eff}} - x} \tag{6.10}$$

with g_{eff} being the effective CMUT gap distance and x the plate deflection different from no applied bias. Here it is seen that at collapse when $x = g_{\text{eff}}/3$ the coupling is maximised at 1. The parasitic capacitance from the coupling between the elements, either in the kerf or in the substrate, increases $C_{0,total}$ and reduces the coupling factor, the domain energy conversion and the sensitivity.

Previously fabricated 62+62 and 92+92 RCA CMUT probes [64], [82] in the group, which are based on an SOI wafer substrate with a 20 µm device layer, exhibited a reduction of the bottom electrode receive sensitivity by a factor of around 3 and 3.3, respectively. Even with the difference in receive sensitivity between the rows and the column of a factor of 2.4 for the TR2 probe, this shows a clear improvement in over the previous SOI wafer based fusion bonded design

The averaged spectra in Fig. 6.22 shows a smaller shift in the peak resonance frequency of the rows compared to the columns. The calculated center frequencies are plotted in Fig. 6.23(b). The extracted peak frequencies are plotted in Fig. 6.24(b) and the average listed in Table 6.3 The average center frequencies of the functional row- and column elements were 5.3 ± 0.2 MHz and 5.5 ± 0.5 MHz, respectively, with the total average of 5.3 ± 0.4 MHz in pulse-echo. The peak frequency was also extracted from the spectral data and gave an average of 4.7 ± 0.1 MHz and 4.2 ± 0.4 MHz in transmit and pulse-echo, respectively, with a total of 4.5 ± 0.4 MHz, also seen in Table 6.3.

The total relative fractional bandwidth (measured at -6 dB) was found to be 86 ± 10 %. These values are comparable to the measurements made with the Tabla V-VI probes. When compared to a linear test element from a similar 188+188 fusion-anodic bonded array presented in the PhD thesis

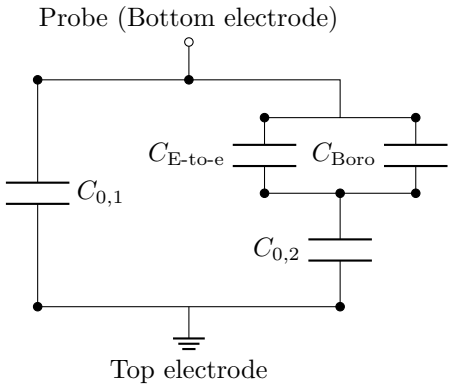


Figure 6.26: Circuit diagram of the neighbouring element coupling when probing column element 1, with $C = C_{0,1}$ and the signal on the bottom electrode pad and ground on the top electrode. The parasitic capacitances $C_{\text{E-to-e}}$ (short for element-to-element) and C_{Boro} (short for boro-fringe) as well as $C_{0,2}$, from the neighbouring element 2, couples into the probed element.

by Andreas Havreland [82], a bandwidth of $\leq 120\,\%$ was measured, though for a probe with a center frequency around 4.2 MHz biased at only 50 V (23 % of designed V_{pi}).

Furthermore, no substrate ringing is observed in these spectra in Fig. 6.22, which was calculated to be 5.07 MHz. However, a dip in amplitude is present at 8.8 MHz, which very well could correspond with the first Bragg frequency, $f_{\text{B},1} = 9\,\text{MHz}$.

6.3.3 Pressure uniformity

The electrode resistance discussed in Section 2.1.8 will be characterised for the TR2 probe in this section. As was found from the impulse responses in Fig. 6.21, the ratio of the peak impulse response amplitudes between the rows and the column was a factor of 2.4. The low measured amplitude of the impulse response for the columns can likely be explained by the signal drop caused by an higher than predicted electrode resistance. If the transmitted signal amplitude is attenuated along either the top or bottom elements, an uneven pressure field is generated with an averaged lower amplitude. The theoretical ωRC value as listed in Table 4.4 for the bottom electrodes is estimated to be 0.065 resulting in a signal loss of $\approx 0.04\,\%$, using the resistivity measured on a dummy silicon substrate wafer. This should in theory not affect the impulse response amplitude, but will nevertheless be characterised as unforeseen structural changes to the silicon electrode and current paths might have changed during the fabrication process.

As mentioned previously the electrode resistance was not measured on the finished array before encapsulation. If this was not the case, the top electrode resistance could easily have been measured by probing both ends of the metal contact. The bottom electrode resistance is more difficult to measure as it lies beneath the surface of the substrate, buried under layers of silicon and dielectrics. A test element would have had to be included in the design with access to the bottom electrode pad in both ends of an element. The effect of the electrode resistance is therefore estimated by instead measuring the pressure field along the top and bottom electrodes during transmit and from these gauge the uniformity and attenuation of the signal from one end to the other.

The pressure field was mapped in immersion using the Onda AIMS III by moving an Onda HGL-0400 hydrophone, connected to the experimental research ultrasound scanner SARUS, in the x-y plane in steps of 0.5 mm with a distance of 5 mm from the transducer surface. This creates a grid of 49×49 measurements with an area of 24.5 mm × 24.5 mm which completely captures the array. A 4-cycle sinusoidal 6.5 MHz pulse with an voltage amplitude of $V_{\text{AC,peak}} = \pm 75\,\text{V}$ has been used to excite three evenly spaced row elements and three column elements, specifically rows and columns with the same numbering (30, 96, 158). These were chosen based on the list of good/functional performing

elements from the impulse response measurements. At each grid point the three elements were excited and the impulse response traces logged and convolved with a Hamming window with the same length as the signal used for excitation.

The pressure maps shown in Fig. 6.27 are each an average of the peak pressure field of the three elements, after they have been aligned in space, and the plots have been normalised to their maximum value and log compressed. In Fig. 6.27(a) for the top electrodes, it is seen by inspection that the pressure distribution is even along the elements. A lengthwise cross-section along the element is plotted in Fig. 6.28. The mean value of the first and last 1/4 part of the element has been calculated as an estimate of the drop in signal and the pressure uniformity. The section near the contact ($\approx 5\,\text{mm}$) gives an average of $-2.4\,\text{dB}$ and near the end of the contact ($\approx 20\,\text{mm}$) an average value of $-2.9\,\text{dB}$ is calculated. This corresponds to a drop to 94 % of the initial amplitude, or an attenuation of 6 % going from one end to the other of the element. This is an acceptable and likely insignificant drop in signal amplitude, but larger than the expected value listed in Table 4.4. Fig. 6.27(b) likewise depicts the pressure of the bottom electrodes (columns) and the cross-section in Fig. 6.28(b) for which similar values have been calculated as $-1.9\,\text{dB}$ near the contact pads ($\approx 20\,\text{mm}$) and $-3.0\,\text{dB}$ near the end of the elements ($\approx 5\,\text{mm}$). This corresponds to a drop to 88 ± 16 % of the initial amplitude, or 12 % attenuation. This is more than the 1.17 % signal reduction predicted in Section 4.2 in Table 4.4 using 4.5 MHz and a 2.40 % reduction when using 6.5 MHz. This value can be compared to an attenuation of 74 % measured on a previously fabricated 92+92 RCA CMUT array with a center frequency of 4.5 MHz and a bottom electrode resistivity of $< 0.1\,\Omega\,\text{cm}$ [58].

It can be concluded that the new thicker bottom electrodes (100 µm) with a resistivity of $< 0.025\,\Omega\,\text{cm}$ is a large improvement in terms of electrode resistance and uniformity when compared to the previously fabricated 92+92 RCA probe.

The data depicted in Fig. 6.27 and Fig. 6.28, which is an average of three emitting row and column elements, exhibited large variations in the recorded pressures values. These variations are much higher than what was seen in [58] for a 92+92 RCA CMUT probe [82] and a 62+62 RCA CMUT probe [64], which both were plotted as an average of all the elements. This likely causes the large standard deviations of the attenuation and the fluctuations seen.

The element pressure uniformity results are more attenuating than expected if only the theoretical values of ωRC and $|H(L, \omega)|$ are considered. However, an improvement is shown in the conductivity and pressure uniformity when results are compared to the previously fabricated 92+92 RCA CMUT probe [58] with a thinner electrode. The 92+92 probe was fabricated with the LOCOS process on an SOI wafer with a 20 µm device layer used as electrode. The TR2 probe show similar uniform results compared to the 62+62 RCA CMUT probe [64] also with a 20 µm device layer.

6.4 Thermal characterisation

After the array has been mounted on the carrier board, encapsulated in RTV, RTV664, connected to the amplifier boards and the probe handle pieces assembled, the thermal performance of the probe needs to be characterised.

As shown in Section 6.2 the probe handle is fitted with an inlet and outlet tube for air cooling of the amplifier boards during scanning. Previous generation probes fabricated in this group have occasionally shown high surface temperatures, too high for safe use, and have shut down after prolonged scanning. This prompted the need for active cooling of the four internal amplifier boards, which is double the number required compared to the previous 62+62 or 92+92 RCA CMUT probes [64][82].

A simple thermal test was performed at BK Medical (Herlev, Denmark) on a hollow 3D-printed dummy probe seen in Fig. 6.29. A dummy load resistor was used to simulate the heat generated by the 4 amplifier boards, using the same power draw. An inlet and outlet was connected to a simple aquarium pump. The internal air temperature and ambient temperature was measured with

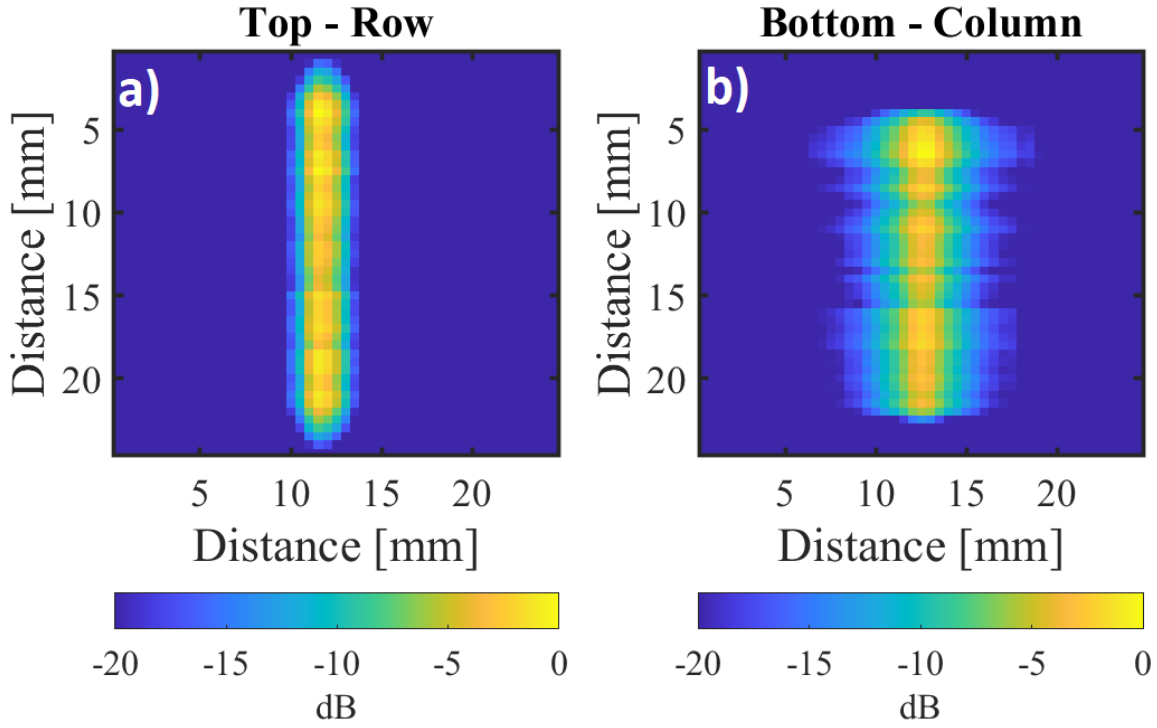


Figure 6.27: Average peak pressure field of elements excited at 6.5 MHz. The pressure is mapped for three different top and bottom electrodes using a hydrophone and an average is shown in (a) for top electrodes (rows) and in (b) the bottom electrodes (columns). The pressure is uniform along the top electrodes. The pressure measured along the bottom electrodes shows a clear maximum value in the top, near the contact pad of the element, but remains mostly uniform along the element. From [1].

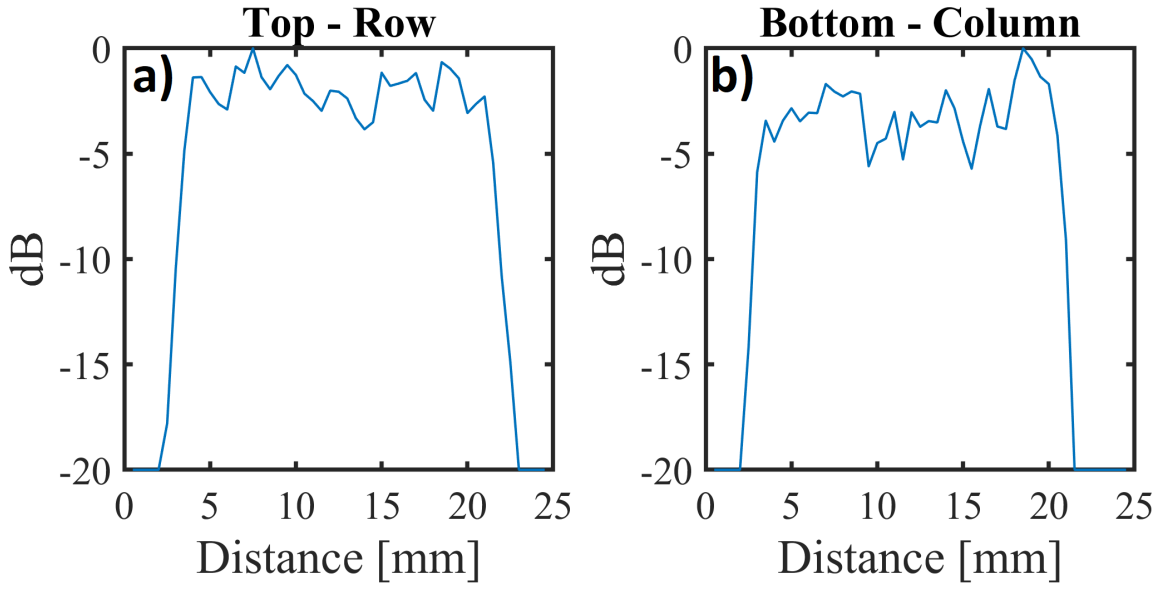


Figure 6.28: Average peak pressure field of elements excited at 6.5 MHz. The plots are lengthwise cross-sections of the maps shown in Fig. 6.27 depicting in (a) the top electrodes (rows) with the contact pad placed in the left hand side of the plot and in (b) the bottom electrodes (columns) with the contact pad in the right hand side. The pressure is uniform along the top electrodes. The pressure measured along the bottom electrodes shows a clear maximum value in the top of the contact but remains mostly uniform along the element.

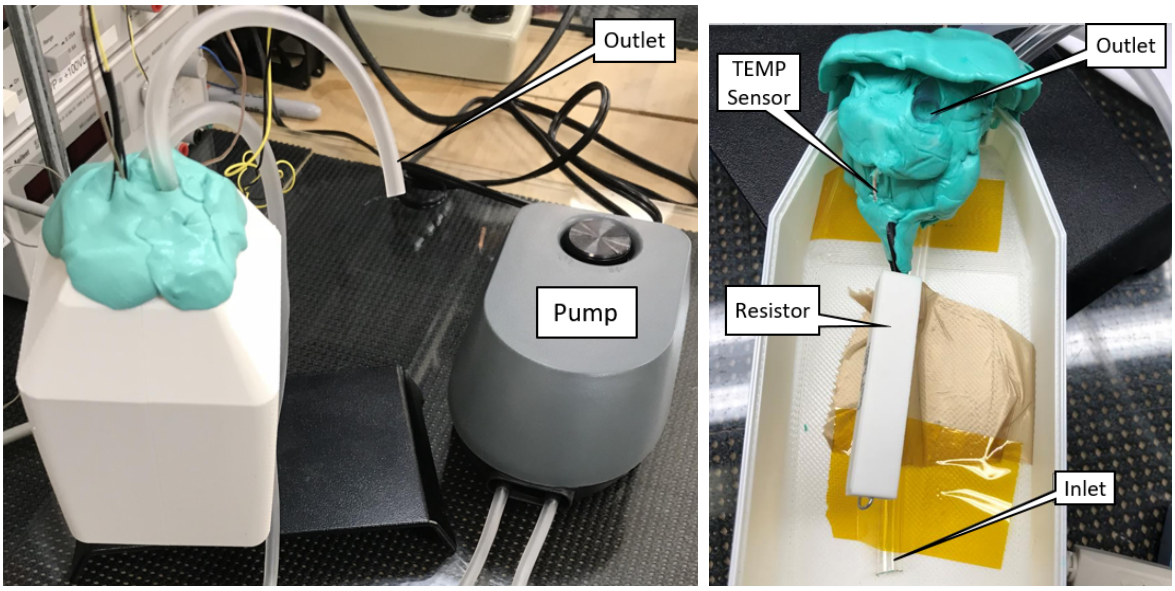
a thermocouple. The logged temperature with and without the pump turned on under load can be seen in Fig. 6.30. In these initial measurements, it is shown that the internal temperature is reduced by $\approx 26\,^{\circ}\mathrm{C}$ with the added cooling and that the maximum temperature reached was $\approx 39\,^{\circ}\mathrm{C}$. Based on this test, the same inlet and outlet tubes, fed by the pump, were incorporated into the TR2 probe shell.

After assembling the probe, an experiment was performed in air at CFU in 2020 to evaluate the cooling capability during idle mode and when emitting a suitable imaging sequence at two different pulse repetition frequencies (PRF). A setup similar to the one shown in Fig. 6.31 was used. Two FLIR C2 thermal imaging system cameras mounted on a frame was used; one camera pointing at the sole surface and another at the side (or top part) of the assembled probe body, near the electronic components of the preamplier boards. The temperature was logged from the cameras as a function of time and is plotted in Fig. 6.32. Data from the two views is plotted together with the shaded areas, which show the idle time period (gray), where just a DC bias voltage of 190 V is turned on, corresponding to 160 V at the chip level, and the areas where two sequences were turned on with a pulse repetition frequency (PRF) of 100 Hz (red) and 500 Hz (blue).

According to the standard specified in the FDA and DS/EN 60601-2-37 standard, measurement criteria 201.11.1.3 [124], either the test method in simulated use specified under 201.11.1.3.1.1 or in still air specified under 201.11.1.3.1.2 is used. The still air test criteria (without any applied gel) were used, which focuses on mainly the temperature rise, with the test method details specified in [124]. The main requirement is that the temperature rise shall not exceed $27\,^{\circ}\mathrm{C}$ and that the rise plus $23\,^{\circ}\mathrm{C}$ shall not exceed $50\,^{\circ}\mathrm{C}$. In simulated use (when a gel is applied to the transducer sole) the maximum surface temperature shall not exceed $43\,^{\circ}\mathrm{C}$.

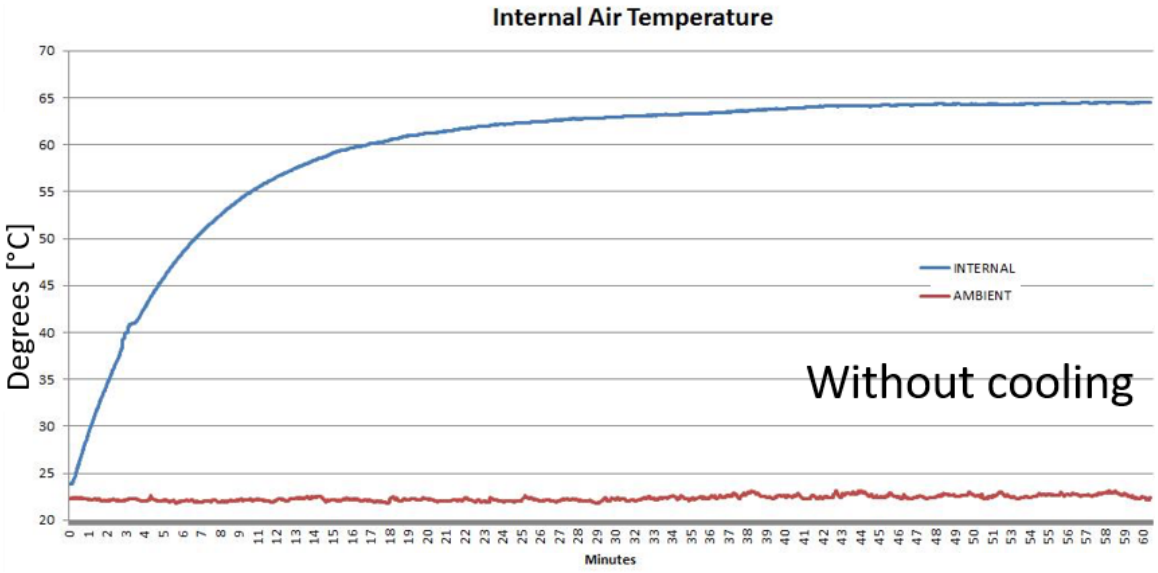
From the measured data in Fig. 6.32 it is seen that both the side surface temperature (top view) and the sole surface temperature reaches above $40\,^{\circ}\mathrm{C}$. The temperature even just exceeds $43\,^{\circ}\mathrm{C}$ on the sole and $46\,^{\circ}\mathrm{C}$ on the side. Before the idle temperature had stabilised, two test sequences (at an PRF of 100 Hz and 500 Hz) were turned on for only 2 min each. It was, however, surmised that they would likely reach $50\,^{\circ}\mathrm{C}$ with prolonged use. The last temperatures logged just when the probe is turned off show a maximum of $43.5\,^{\circ}\mathrm{C}$ on the sole and $46\,^{\circ}\mathrm{C}$ on the side, giving a rise of $24\,^{\circ}\mathrm{C}$ with the expectation that the probe will exceed this value.

This experiment was repeated in May 2022, with the setup in Fig. 6.32, where the pump was replaced with a tube connected to a compressed air laboratory tap for testing purposes. The pressure was regulated with a controlled pressure gauged set to 0.2 bar. These measurements plotted in Fig. 6.33 showed that the idling temperature of the probe when supplied with a DC voltage of 190 V, again corresponding to 160 V at the chip level, gives a stable average temperature at $\approx 31\,^{\circ}\mathrm{C}$ on the sole (blue) and $\approx 36.5\,^{\circ}\mathrm{C}$ on the side (red) after 25 min. A SA imaging sequence using 18 elements, 192 emissions, a pulse repetition frequency of 12 kHz, and ± 75 V peak voltage was then used as excitation signal. The surface temperature of the sole rose $\approx 2\,^{\circ}\mathrm{C}$ during the measurement, reaching a maximum average of $32.8\,^{\circ}\mathrm{C}$ (yellow) after 5 min. The probe side view had a stable surface temperature of $\approx 36.5\,^{\circ}\mathrm{C}$ (purple) throughout the measurement which is caused by the underlying voltage regulator on the amplifier boards. The temperature rise and surface temperature of the transducer body and sole when idling and imaging were both found acceptable for experimental external use below the FDA and DS/EN limits for scanning [124]. The airflow inside the current probe design is, however, likely restricted by the preamplifier boards and their shielding and the internal temperature is probably higher than what is measured on the surface. The internal environment can therefore also not be compared with the reduction in temperature achieved with the test performed at BK Medical. Unfortunately no temperature sensors were installed in the probe during assembly and the internal temperatures can not be monitored.

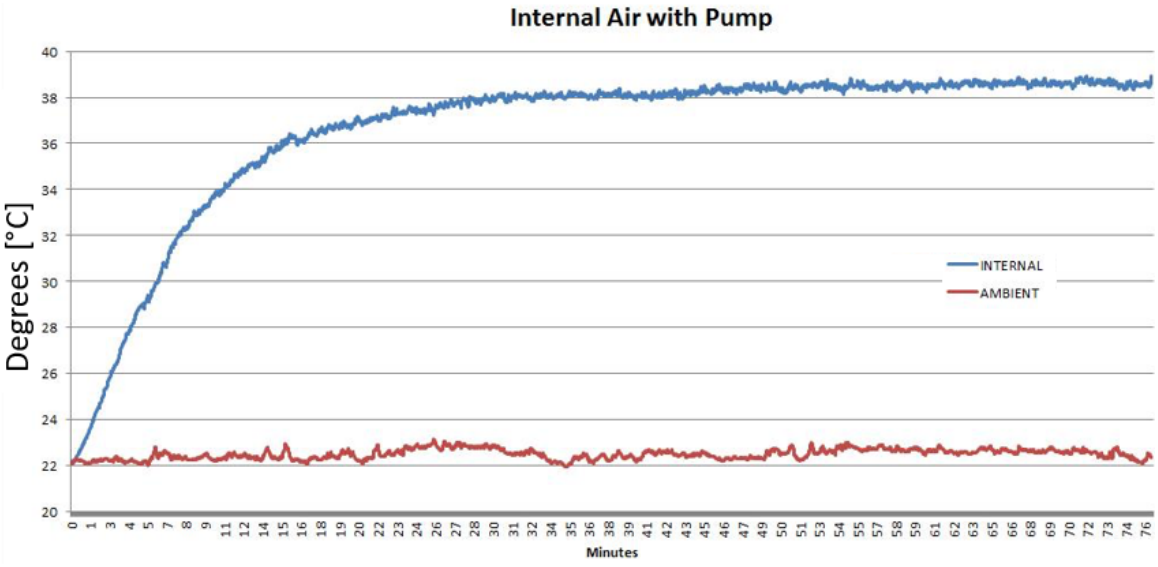


(a) (b)

Figure 6.29: A hollow 3D-printed probe with an internal dummy load resistor was used to simulate the heat generated by the 4 amplifier boards, using the same power draw. An inlet and outlet tube is seen connected to a simple aquarium pump, leading in and out of the probe which has been sealed up with a putty. The internal air temperature and ambient temperature was measured with a thermocouple.



(a)



(b)

Figure 6.30: Internal probe temperature measurements from the setup shown in Fig. 6.29 plotted together with the ambient temperature. Measured for 60 min (a) without the air pump turned on. Measured for 76 min (b) with the air pump turned on.

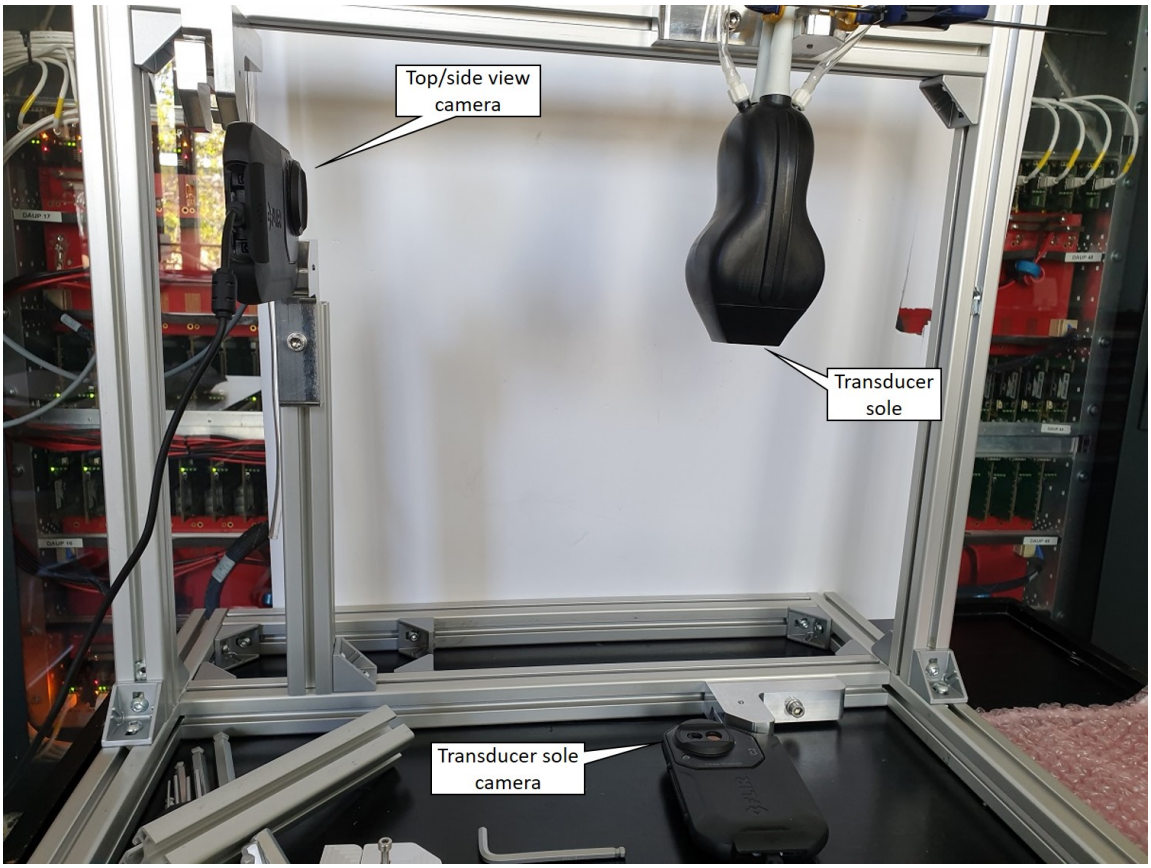


Figure 6.31: Thermal frame setup showing the fixed TR2 probe and two FLIR C2 thermal imaging system cameras; one camera is pointing at the sole surface and another at the side (or top part) of the assembled probe body.

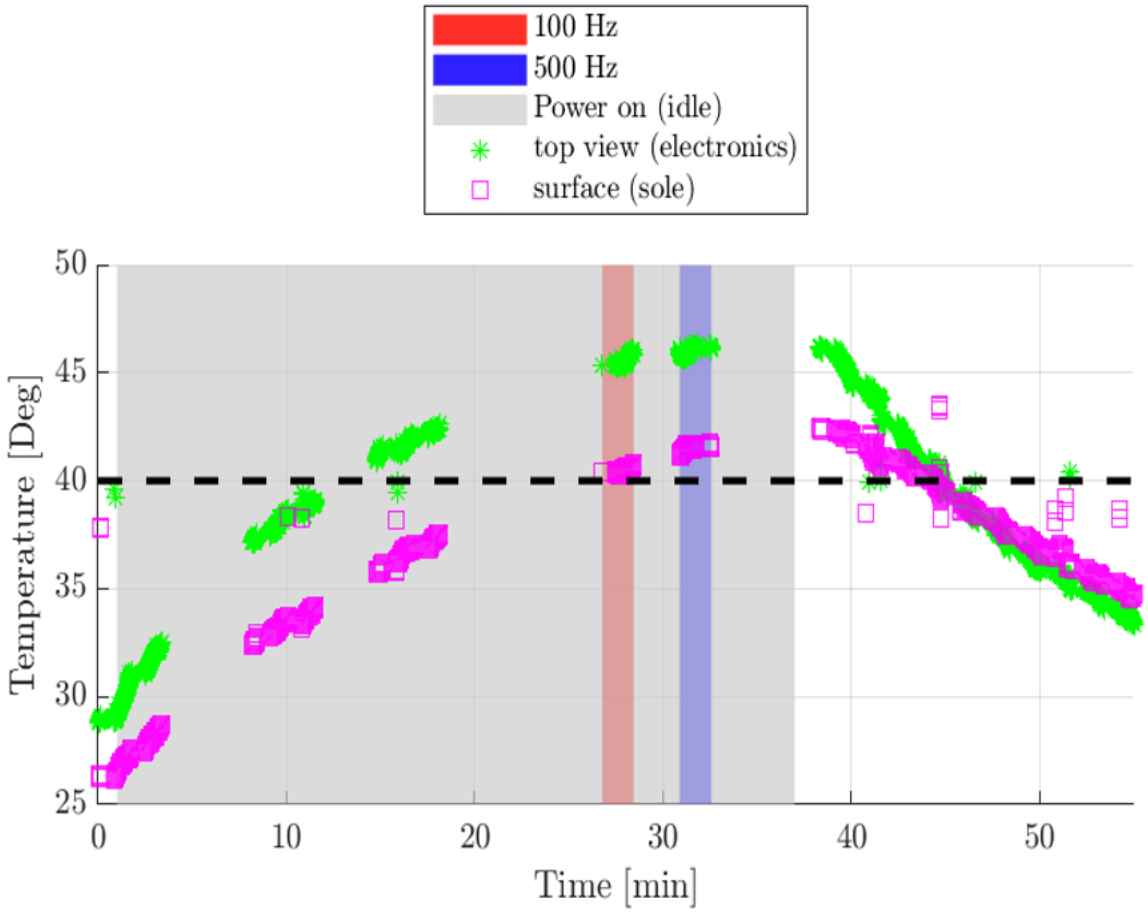


Figure 6.32: Thermal measurements performed on the assembled probe body using a setup with two FLIR C2 thermal imaging system cameras. These were mounted on a frame to measure the temperature on the probe from the side and the front. Measurements using two imaging sequences, with a pulse repetition frequency (PRF) of 100 Hz and 500 Hz, were performed with the probe in idle mode for 2 min each with an applied bias voltage of 190 V.

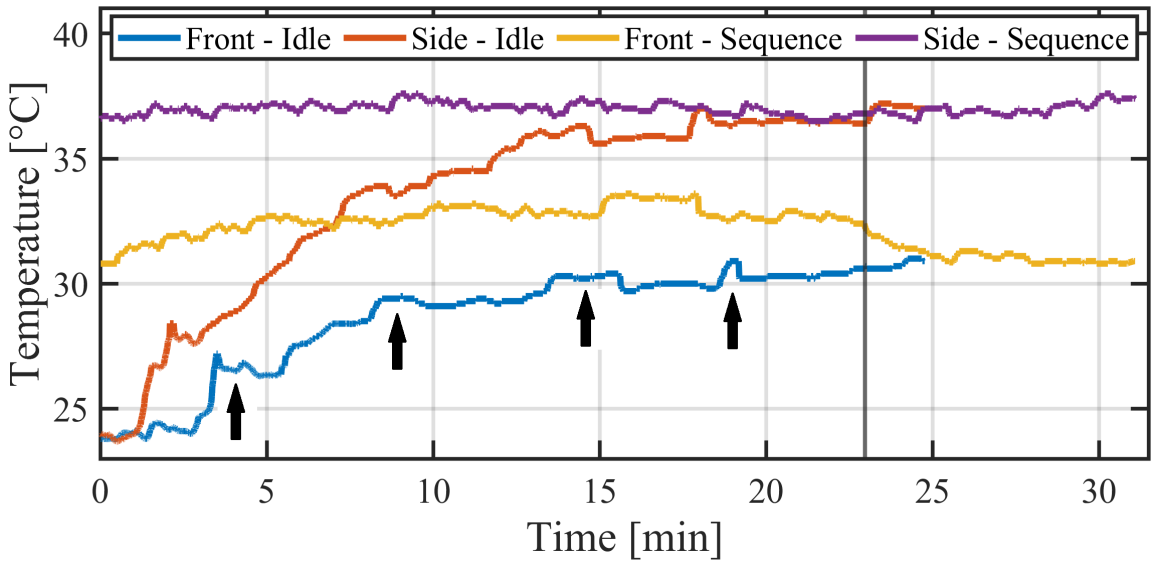
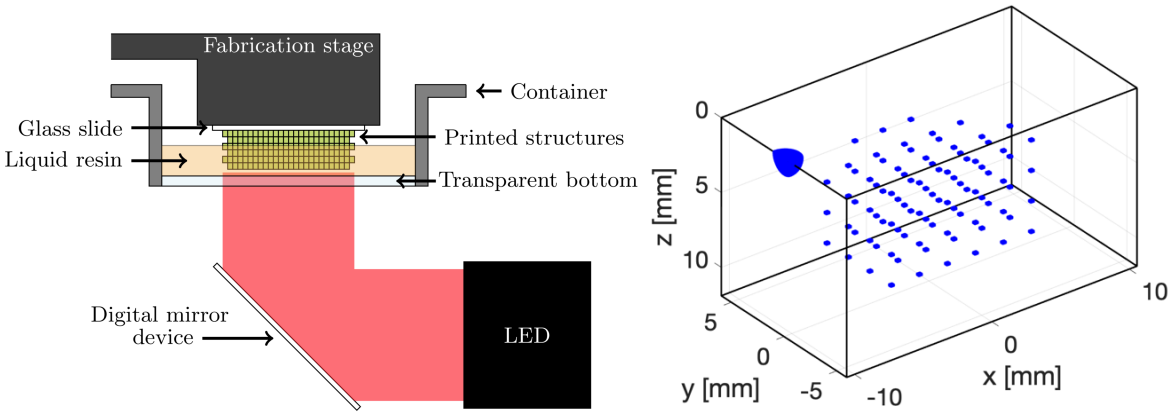


Figure 6.33: Thermal measurements performed on the assembled probe body using a setup with two FLIR C2 thermal imaging system cameras. These were mounted on a frame to measure the temperature on the probe from the side and the front. Measurements were performed in idle mode with an applied bias voltage and when using an imaging sequence. The vertical line at 23 min indicates when the sequence used for excitation is stopped. The slight variations in the dataset, illustrated by the black arrows for the blue curve, are caused by the thermal cameras performing automatic re-calibration during the measurements. From [1].



(a) A tiger **(b)** A mouse

Figure 6.34: A 3D resin printer, shown in (a), is equipped with a 365 nm high power LED (LZ1-00UV00, Ledengin) source and a digital mirror device (DMD) used to selectively illuminated a thin layer of resin through the transparent bottom of the resin vat [125]. A 3D MATLAB design of a scatter phantom, shown in (b), with a grid of $6 \times 4 \times 4$ isolated scatterer dots, spaced with a distance of 2.05 mm. This phantom has been designed by Martin Lind Ommen from this research group.

6.5 Imaging performance

6.5.1 B-mode performance of row-column array

The imaging capabilities of the probe was evaluated at CFU from B-mode images using the SARUS system by scanning a wire matrix phantom, a cyst phantom and a stereolithography 3D printed hydrogel phantom. The resolution obtained from volumetric scans can be estimated in the axial (z), the lateral (x) and azimuthal (y) directions as well as the penetration depth derived from the signal to noise ratio (SNR).

Scatter phantom

The custom built stereolithography printer used to print the soft hydrogel phantom has previously been presented in this research group in [125] and [126] by Martin Lind Ommen, where the functionality and materials used are explained. It works similar to a standard hobby based photopolymer resin based 3D printer in that it crosslinks the polymer exposed to a source matching the photoabsorber. The printer used reflects a 365 nm high power LED (LZ1-00UV00, Ledengin) source off a digital mirror device (DMD) into the transparent bottom of the a resin vat, as illustrated in Fig. 6.34a, and the stage is translated in the x-y plane to cover a larger print area. The ultimate printing resolution is $10 \times 10 \times 20\,\mu m^2$. The phantom used in this experiment (micro_flow_phantom_fp-v5_5_1) is designed with isolated $205 \times 205 \times 80\,\mu m^3$ embedded cavities, which function as point scatter targets. The scatterers were placed in a $6 \times 4 \times 4$ grid with a spacing of 2.05 mm, as shown in this 3D design drawing in Fig. 6.34b from MATLAB, which is also used to generate the image mask layers used for printing the phantoms. The printed phantom has the approximate dimensions $1 \times 1 \times 2\,cm^3$ and can be seen in Fig. 6.35.

3D volumetric imaging was performed using a SA sequence with 96 row and 96 column emissions, using a sinusoidal excitation signal with an AC transmit amplitude of $V_{peak} = \pm 75\,V$ and a frequency of 6.25 MHz. The three orthogonal B-mode imaging planes are shown in Fig. 6.36. From this the resolution of the PSF from the scatterers could be determined in the axial direction as $0.82\,\lambda$ (0.188 mm) and in the lateral direction as $1.72\,\lambda$ (0.394 mm). The side-to-main lobe level was fairly high at -11.90 dB, as seen in Fig. 6.38a, due to scattering from the phantom surrounding the point cavities.

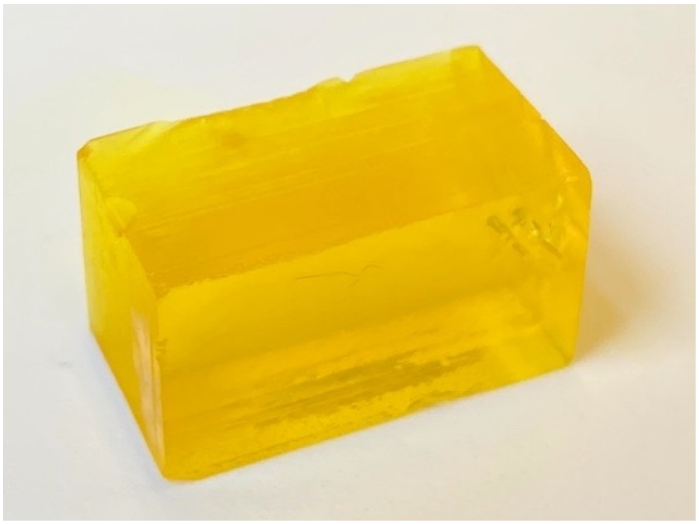


Figure 6.35: Stereolithography soft hydrogel phantom. The phantom dimensions are approximately $1 \times 1 \times 2\,\text{cm}^3$ and has a grid of $6 \times 4 \times 4$ isolated $205 \times 205 \times 80\,\mu\text{m}^3$ embedded cavities, spaced with a distance of 2.05 mm.

Wire and cyst phantoms

The wire phantom used for B-mode imaging is a box with a regularly spaced grid of wires in the x- and z-directions. The wires are 1 cm apart, and one column is intentionally missing to allow proper orientation of the transducers. The matrix of wires are immersed in water with little acoustic attenuation.

In this phantom the same imaging sequence used for the scatter phantom is utilised to scan a column of wires and produce three orthogonal B-mode imaging planes. The resolution of these are visualised in Fig. 6.37, which depicts three different planes from the volumetric scan of a wire phantom, measured to a depth of 80 mm with a dynamic range of 40 dB. The x-z (lateral) plane shows the wires as horizontal lines, the $y - z$ (azimuthal) plane shows two columns of wire cross-sections as dots, and the $x - y$ (transverse) plane depicts two horizontal wires; one barely visible at $(y) = (-8\,\text{mm})$ and one at $(y) = (2\,\text{mm})$. The resolution in this phantom was in the axial direction $1.16\,\lambda$ (0.265 mm) and in the lateral direction $1.56\,\lambda$ (0.356 mm), as seen in the PSF plotted in Fig. 6.38b. The contrast was found to be -16.90 dB due to the many missing elements.

The cyst phantom is a model DFS 571 (Dansk Fantom Service) with an attenuation 0.5 dB/[MHz cm], which is used as a tissue mimicking phantom for measuring imaging or penetration depth. This was measured at the point when the SNR attains a value of 0 dB, calculated as the average signal squared divided by the noise squared, shown in Fig. 6.39. A SA sequence with 96+96 emissions at 6.5 MHz was used. The transducer reaches a depth of $150\,\lambda$, where the wavelength λ in this phantom is 0.2375 mm. This corresponds to a penetration depth of 3.6 cm, again due to the many missing elements. A conventional is often have a $300\,\lambda$ to $400\,\lambda$ corresponding to 12 cm to 15 cm [89].

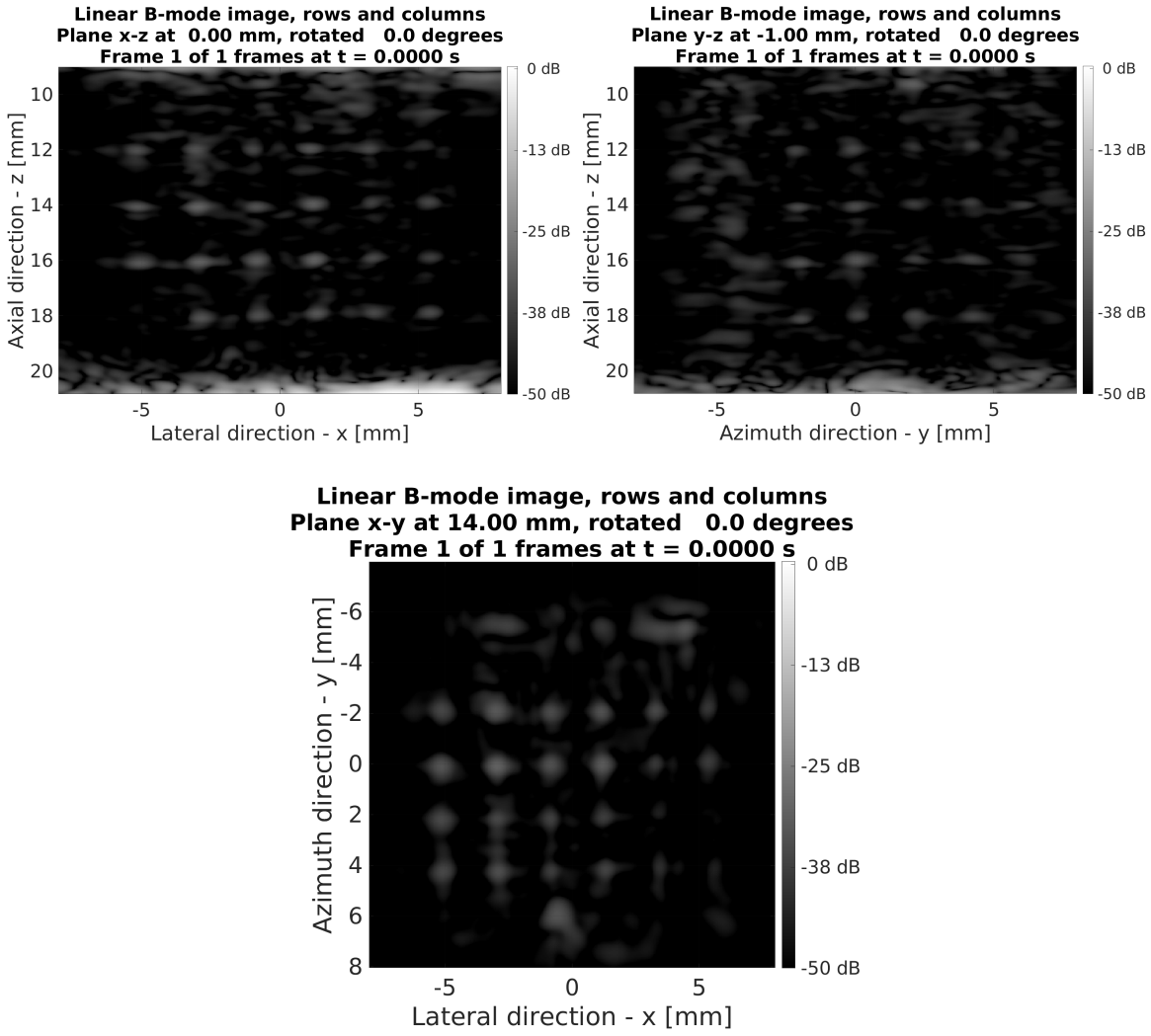


Figure 6.36: B-mode images of the point spread functions in three orthogonal planes obtained from a stereolithography 3D printed hydrogel phantom using the 190+190 TR2 transducer probe. The phantom has a grid of $6 \times 4 \times 4$ isolated $205 \times 205 \times 80\,\mu m^3$ embedded cavities, which function as scattering point targets. From [1].

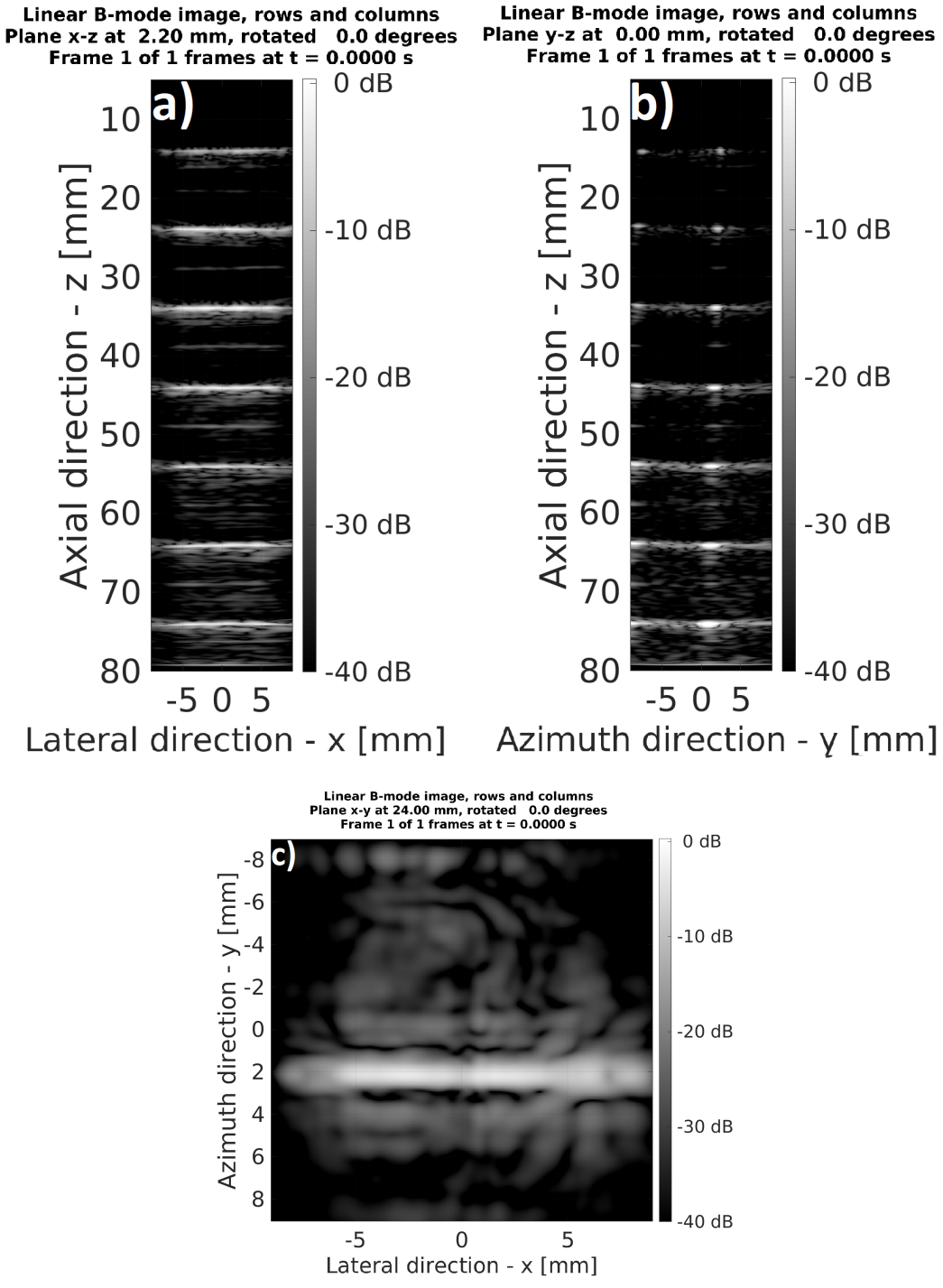
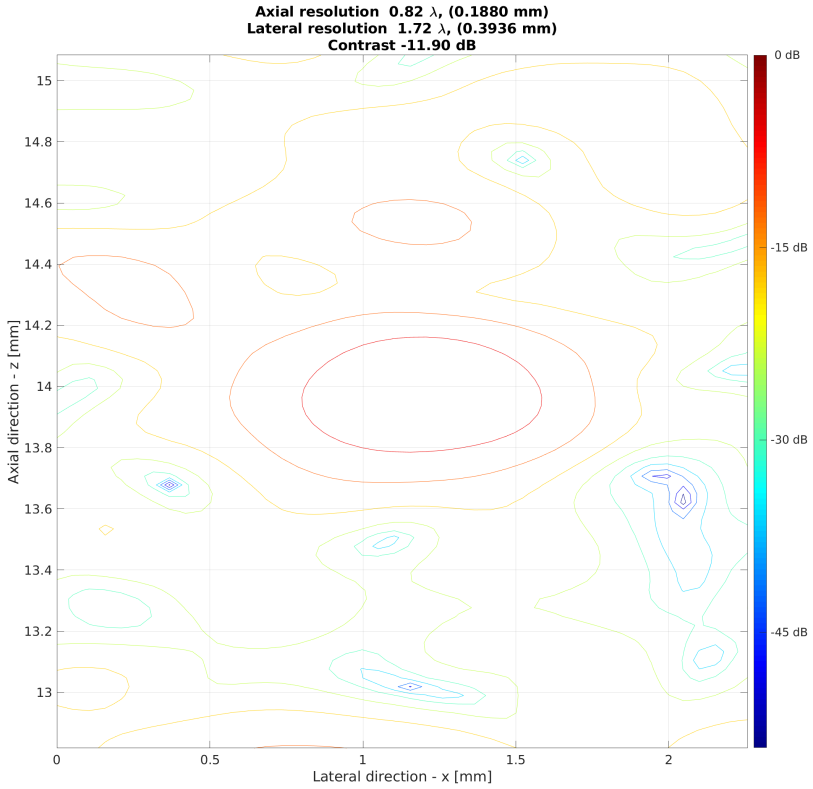
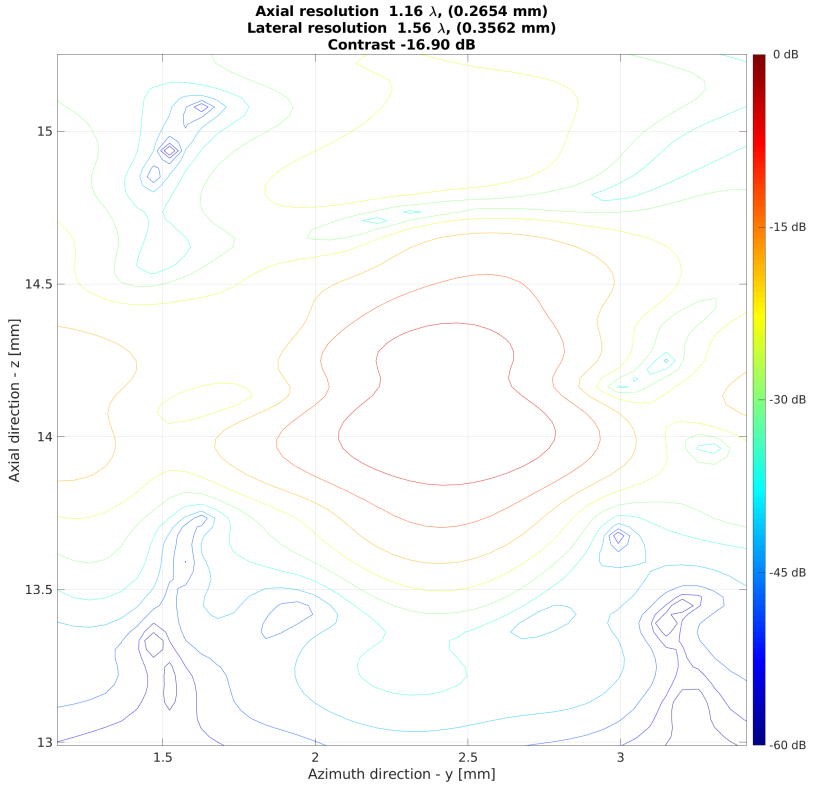


Figure 6.37: Imaging planes of a wire phantom obtained using the 190+190 TR2 transducer probe. The three different planes depict (a) the horizontal wires along in the x-direction (x-z plane), (b) two columns of wire cross-sections (y-z plane) and (c) the top of a single wire (x-y plane). From [1].



(a)



(b)

Figure 6.38: Point spread functions of the scatter phantom in the x-z plane (a) and of the wire phantom in the y-z plane (b).

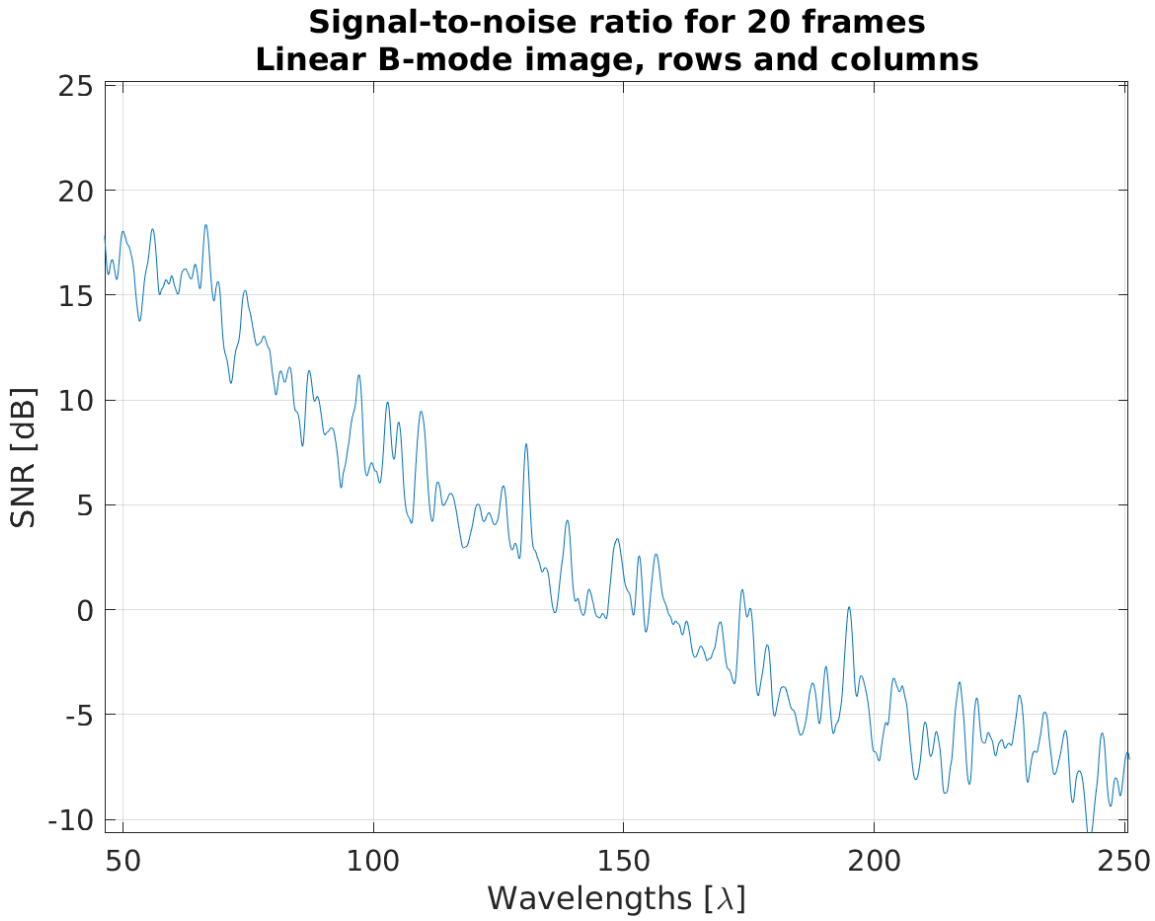


Figure 6.39: SNR of the 190+190 RCA probe for a tissue mimicking phantom phantom with an acoustical attenuation of 0.5 dB/[MHz cm]. The penetration depth is roughly 150 λ when the SNR reaches 0, corresponding to 3.6 cm as the wavelength in this phantom is 0.2375 mm when imaging with a frequency of 6.5 MHz. From [1].

6.6 Chapter summary

In this chapter the electrical and acoustical characterisation of the TR2 array before and after integration in the probe handle was presented. Impedance measurements were performed which showed a center frequency at 9.25 MHz in air matching the simulated value of 9.15 MHz from COMSOL well with an operational bias voltage at 150 V. The electromechanical coupling coefficient was calculated to be $k^2 \approx 7\,\%$.
Acoustical characterisation of the assembled probe in transmit and pulse-echo were performed and the impulse responses and spectra of the rows and columns of the probe was found. These showed a total functional element yield of the rows and columns in transmit as 61 % and in pulse-echo as 55 %. A discrepancy in the transmit and pulse-echo receive sensitivities between the rows and columns were found. In reason for this effect in transmit was discussed and is not currently understood. In pulse-echo the columns had a sensitivity 2.4 times lower than the rows and an explanation was discussed to be due to element-to-element capacitive coupling in the kerf between the bottom elements in the array.
The total averaged weighted center frequencies for the rows and columns in transmit and pulse-echo were 6.0 ± 0.9 MHz and 5.3 ± 0.4 MHz, respectively and the fractional bandwidth at $63 \pm 4\,\%$ and $86 \pm 10\,\%$, respectively. These values were around 3 MHz to 4 MHz lower than the predicted center frequency.
Furthermore, results from pressure uniformity measurements showed that the bottom electrodes had an attenuation of 12 %.

Thermal characterisation was presented. This showed that the probe exhibited little to no heating when imaging sequences were transmitted.
Lastly, the 3D volumetric imaging results of the probe were presented. These were performed on a 3D printed hydrogel phantom, a wire phantom and a cyst phantom. The resolution of the PSF for the hydrogel phantom was determined in the axial and lateral directions to be 0.82λ (0.188 mm) and 1.72λ (0.394 mm), respectively. The wire matrix phantom in wafer was measured to a depth of 80 mm. The resolution of the PSF was in the axial and lateral directions 1.16λ (0.265 mm) and 1.56λ (0.356 mm), respectively. The contrast was found to be -16.90 dB.
Results from SNR measurements showed a penetration depth of 3.6 cm.

Part II

Anodic bonding based CMUTs Transducer Human 1 (TH1)

Chapter 7

Design

In this Part II of the thesis, in the following design, the 2D RCA CMUT arrays which has been designated as *Transducer Human 1*, and will henceforth be referred to as TH1, will be presented.

Two generations of the TH1 arrays were fabricated in this thesis and they will be referred to as TH1-A and TH1-B. The TH1-A array design was a continuation of the 190+190 anodically bonded array presented in [55]. The following TH1-B array was fabricated in response to the electrical measurements of TH1-A, which showed a pull-in voltage approximately 100 V lower than the designed value. This was the result of an over-etch during the fabrication process, which led to a vacuum gap around 40 nm lower than designed. The array layout of TH1-B is identical to TH1-A, but the design parameters have been adjusted and the fabrication procedure has been changed and optimised slightly.

The design and the associated parameters of the arrays will be found based on the procedure in Chapter 2. Following this design chapter the fabrication process and its optimisation will be presented. Lastly the TH1-A array will be electrically characterised, the prototype probe will be assembled and its performance evaluated acoustically.

First the initial design of the TH1 array will be presented as the TH1-A array and then the updated design as the TH1-B array will be presented.

7.1 Specifications and requirements

The CMUT fabrication process of the TH1-A array utilising anodic bonding, as presented in Part I Section 5.1.2, is based on and further developed from a previous array fabricated in our group [83]–[85]. The idea behind this technique and resulting fabrication process is inspired by the anodically bonded CMUT arrays presented in 2014 by Bellaredj [116] and in 2015 by Yamaner et al [28] 1D linear array and in 2018 and 2021 by Sanders et al [56], [57] using RCA arrays.

In the figure shown in the introduction, Fig. 1.4, the general outline of the CMUT structure fabricated by the author of this PhD on a glass substrate using anodic bonding is shown. The RCA CMUT array presented in this chapter are made in the same manner and the fabrication process will be presented further down. The arrays were intended, like the finished TR2 probe, to be possible to interface and be used with a BK3000 scanner from BK Medical or the SARUS system with a maximum DC source bias of 190 V ($\pm$95 V), using a dual rail power amplifier. The platform, however, is different, and the finished array will instead of being encapsulated in a sealed probe handle be used in a newly developed prototype probe handle. This is presented later in Chapter 9 in Section 9.2. The design of the prototype probe will make it possible to freely interchange the nose piece of the probe, in which a chip is permanently mounted. In that way multiple chips can be tested using the

same probe, which will decrease the turn-around time for characterisation of the fabricated chips. The chip carrier board (CCB), mounted inside the nose piece, is developed in collaboration with our research group and BK Medical and sets the design and physical size limitations on the array. The pitch of the on-board 380 (190+190) element connectors on the CCB is 190 µm and the current maximum chip area is 2.94 mm × 2.94 mm. Four extra connectors for the apodization are also included, bringing the total connector count up to 384. This connector pitch restricts the array element pitch to 95 µm, since the odd and even rows and columns are interleaved with contacts on both side of the chip. If the $\lambda/2$ criterion is strictly followed this would, like the TR2 probe, result in an operational frequency of 8 MHz in immersion. If a much higher frequency is desired and $\lambda/2$ is kept, the current PCB board design will need to be changed, otherwise a slightly higher than $\lambda/2$ pitch is obtained.

7.2 Design parameters - TH1 design A

The TH1-A array was initially intended to have a designed center frequency in immersion of around 8 MHz with an element pitch of 95 µm. This pitch was kept the same as the TR2 array design presented in Part I in Chapter 4. The array likewise has the same element count of 190+190 rows and columns with four integrated apodization regions, two for the rows and two for the columns, situated around the periphery of the square array. This increases the interconnection count to 192+192.

The cell shape for this array was chosen to be square with a square inner electrode with a smaller diameter/side length. Adopted from the earlier TR2 and also the Tabla VI design, the element kerf was set to $d_{\text{elem-kerf}} = 2.5\,\mu\text{m}$. From here the cell size, number of cells across the element and cell distances can be found from Eq. (2.9) in Chapter 2

$$p_{\text{elem}} = n\,d_{\text{cell}} + d_{\text{elem-kerf}} + (n-1)\,d_{\text{cell-separation}} + 2\,d_{\text{cell-to-edge}} \tag{7.1}$$

$$95 = n\,d_{\text{cell}} + 2.5 + (n-1)\,d_{\text{cell-separation}} + 2\,d_{\text{cell-to-edge}}. \tag{7.2}$$

The distance between the cells in the element, $d_{\text{cell-separation}}$, was set to 8 µm, and by isolating the cell diameter this gives

$$d_{\text{cell}} = \frac{1}{n}(95 + 5.5 - 8\,n - 2\,d_{\text{cell-to-edge}}). \tag{7.3}$$

Now the effective clamping radius $a_{\text{eff}} = a + c\,h = a + 0.62\,h$, with a being the cell radius and h the plate thickness can included by setting $d_{\text{cell-to-edge}} = 0.62\,h$. This further limit values d_{cell} can take and the expression becomes

$$d_{\text{cell}} \leq \frac{100.5 - 8\,n - 1.24\,h}{n}. \tag{7.4}$$

The number of cells n, will be set to either one or two cells which gives the following restrictions on the cell diameter

$$d_{\text{cell}} \leq \begin{cases} 92.5 - 1.24\,h & \text{for } n = 1 \\ 42.25 - 0.62\,h & \text{for } n = 2. \end{cases} \tag{7.5}$$

The final plate thickness will be determined using FEM models in COMSOL, but h typically lies in the range from 1.5 µm to 5 µm, depending on the center frequency and pull-in voltage.

A two cell design using square cells with a cell side length of $d_{\text{cell}} = 37\,\mu\text{m}$ was chosen. This leaves

$$95 = 84.5 + 2\,d_{\text{cell-to-edge}} \Rightarrow d_{\text{cell-to-edge}} = 5.25. \tag{7.6}$$

where the plate thickness can be a maximum if $h = 8.46\,\mu\text{m}$.

By combining Eq. (2.15) and Eq. (2.16) the plate thickness can now be found from the cell size and resonance frequency as

$$\omega_r \sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}} = 10.328\sqrt{\frac{Y}{12\,(1-\nu^2)\,\rho_p}}\frac{h}{a^2} \tag{7.7}$$

with the same material parameters as used for TR2, except that the "radius" or half-diameter is now $a = 37\,\mu\text{m}/2 = 18.5\,\mu\text{m}$. By solving Eq. 7.7 analytically for h using 8 MHz, a plate thickness of 1.62 µm is obtained

The analytical unbiased resonance frequency in air will then be 18.1 MHz, given by the ratio between ω_r in immersion and ω_0 in vacuum from Eq. (2.15) , written below for convenience

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}}} = 0.44. \tag{7.8}$$

The operating voltage is for this array set to 150 V which if 80 % $V_{\text{pull-in}}$ is used gives us a pull-in of 187 V.

The effective gap can for $h = 1.62\,\mu\text{m}$ be found using Eq. (2.33)

$$g_{\text{eff}} = \sqrt[3]{\frac{12(1-\nu^2)V_{\text{pi,circ}}^2\,a^4\epsilon_0\pi}{89.4459Yh^3}} \tag{7.9}$$

$$= \sqrt[3]{\frac{12(1-0.177^2)(187\,\text{V})^2\,(18.5\,\mu\text{m})^4\,8.854\times10^{-12}\,\text{F}\,\pi}{89.4459\times148\,\text{GPa}(1.62\,\mu\text{m})^3}} = 287.4\,\text{nm}. \tag{7.10}$$

The expression from Eq. (2.33) is derived for circular plates, however, as it was mentioned in Chapter 2 and in [93] the error associated with using the circular model for square plates is minimal.

The structure for this array is built around the borosilicate glass wafer with etched cavities and metal electrodes. This would result in an effective gap equal to the actual vacuum gap, $g_{\text{eff}} = g_{\text{vac}}$, if the plate only consists of poly-Si and an Al layer.

If the CMUT devices were to go into pull-in and the membrane collapse, a direct short-circuit would occur between the applied signal source and ground. One could operate the CMUTs with a smaller bias voltage to have a larger safe margin, or design the array itself or electronics to have a failure more which does not result in short-circuiting the probe. The solution chosen, is to coat the poly-Si plate with silicon nitride before the wafers are bonded, as shown in Chapter 1 in Fig. 1.4(d).

Another issue that has been observed in earlier array designs prior to the TH1 generation was short circuits occurring between the top and bottom electrode at the bottom electrode contact pad. When the arrays were characterised using the tests described in Chapter 3, short circuits were seen already below 10 V. This was found to be due to electrical breakdown in air in the 400 nm gap between the metal top and bottom electrode near the contact pad. The problem was solved by extending the existing silicon nitride membrane to cover the borosilicate glass trench and thereby insulating the top and bottom electrodes, illustrated in Fig. 7.1. This made high voltage operation up to ±200 V DC bias possible.

The thickest layer of nitride we can deposit in a single deposition in the furnace is around 180 nm to 200 nm, which has a relative permittivity measured by the author of $\epsilon_{\text{ni}} = 6.86$. An oxidised nitride layer (oxynitride) has also been shown to facilitate more successful anodic bonding by increasing the bonding strength [127]. This is a method which has been used before in this group and will also be used for fabricating the TH1 chip generation.

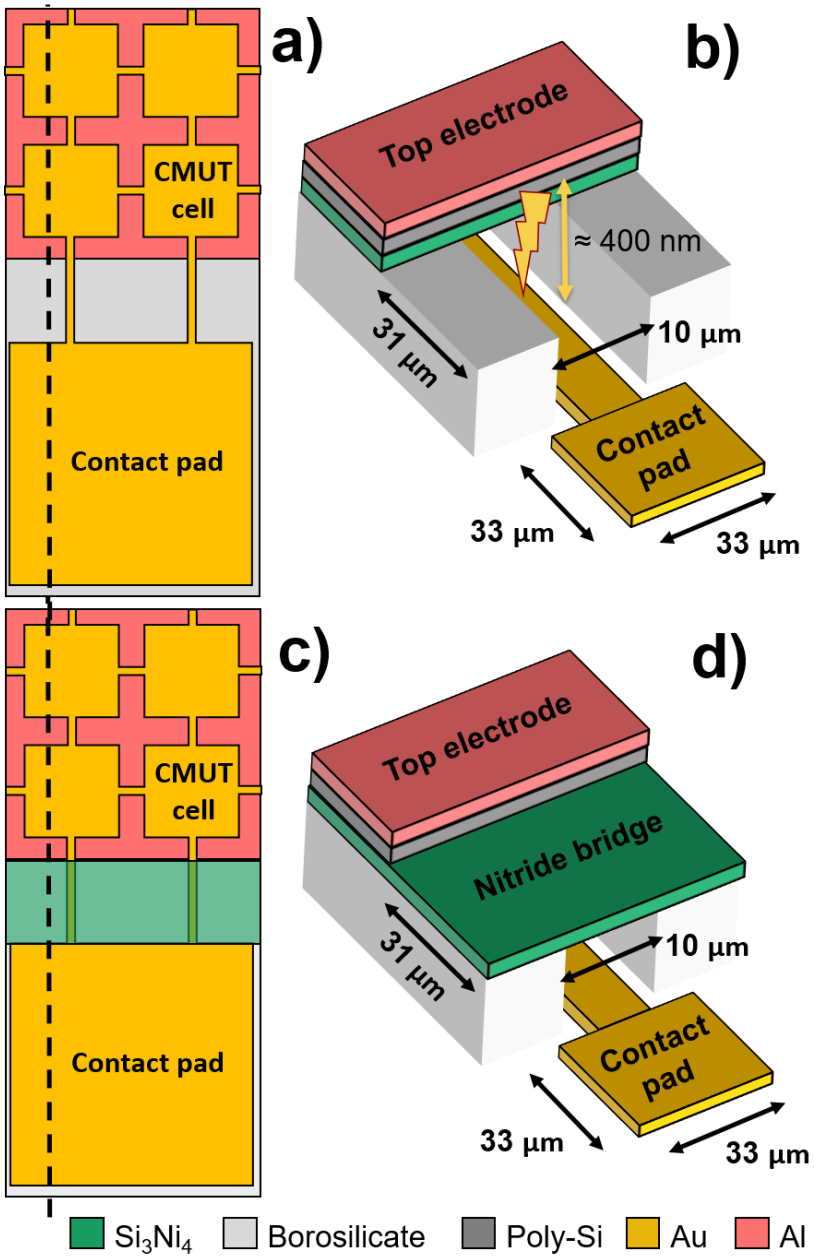


Figure 7.1: High voltage design overview. The previous and current design are (a) – (b) and (c) – (d), respectively. (a) Top down view through the top electrode of the CMUT cells, contact pad and interconnecting leads. The borosilicate glass substrate trench leading to the contact pad is uncovered. (b) The same structure near the bottom electrode pad shown in 3D. The 400 nm distance between top and bottom electrodes right at the edge of the top plate leads to an electrical breakdown in air. (c) Top down view through the top electrode. The borosilicate glass substrate trench with the chromium leads is here covered by a silicon nitride bridge design. (d) The 31 µm long borosilicate trench is seen covered by an insulting nitride membrane. The dotted cut-line corresponds to the cross-section presented in the process flow in Fig. 8.1, step 9). Adapted from [55].

The result is that the capacitive stack of media in the effective gap becomes vacuum and nitride, and the vacuum gap can by found from equation Eq. (2.21) as

$$g_{\text{eff}} = \sum_{n=1}^{N} \frac{t_n}{\epsilon_n} = g_{\text{vac}} + \frac{t_{\text{ni}}}{\epsilon_{\text{ni}}} \tag{7.11}$$

$$g_{\text{eff}} = 343.6\,\text{nm} = g_{\text{vac}} + \frac{200\,\text{nm}}{6.86} \tag{7.12}$$

$$g_{\text{vac}} = 258.2\,\text{nm}. \tag{7.13}$$

These values were used as starting guesses in the dedicated 2D CMUT COMSOL model, described in Chapter 2 Section 2.1.6. During the iterative optimisation of parameters, it was decided that a plate thickness of 2.5 µm would be used instead, which would match the device layer thickness on an already fabricated batch of PSOI wafers. The adjusted values for a square cell with side length 37 µm are listed in Table 7.1.

PSOI wafers are a type of SOI wafers previously presented in [76] and also used in the TR2 process, which are fabricated in the DTU Nanolab cleanroom facilities. The BOX thickness can be selected for each batch, and the poly-silicon device layer thickness controlled to within 100 nm to 200 nm through CMP with little thickness variation across the wafer. The average surface roughness of the poly-silicon, with and without oxynitride, can be brought to sub-nm values through polishing, which is crucial for fusion bonding. The anodic bonding process, as mentioned during the fabrication of TR2 in Section 5.1.2, is more forgiving in regards to the surface roughness. The polishing and cleaning procedures of these PSOI wafers are still continuously being developed in the group, also by the author, to increase yield and thickness precision.

Returning to the parameters, if the same calculation for the pull-in voltage is used to calculate the new effective gap and resulting vacuum gap, the following values are obtained

$$g_{\text{eff}} = 185.7\,\text{nm} = g_{\text{vac}} + \frac{200\,\text{nm}}{6.86} \tag{7.14}$$

$$g_{\text{vac}} = 156.5\,\text{nm}. \tag{7.15}$$

The vacuum gap is now closer to the one found from COMSOL at $g_{\text{vac}}135\,\text{nm}$.

The FEM model predicts a new biased center frequency in air at 23.6 MHz. A plate thickness of 2.5 µm gives a reduction in frequency from air to water (Eq. (2.15)) of $\omega_r/\omega_0 = 0.52$. This results in a frequency in immersion of 12.3 MHz, which has the $\lambda/2$ pitch of 62.6 µm. Compared to the current 95 µm pitch set in the design, the array would operate at a $3/4\lambda$ if used at 12.3 MHz and some degree of grating lobes can be expected during imaging. The array, however, is expected to have a relative fractional bandwidth of 60 % to 100 % and would be able to operate at 8 MHz if necessary.

The final array design is shown in Fig. 7.2 as a complete overview of the last lithographic mask of the fabrication process. All the masks and the design work has been carrier out in the CAD software L-Edit (Tanner Tools). The inset in the figure shows the integrated apodization region present in both ends of the rows and columns. This region is made up of 15 sub-elements with a varying cell count and rotation. The number of cells are gradually reduced from 3 to 1 cell over the length of the region to reduce the emitted amplitude at the edges of the array approximately according to a Hanning window function. This will reduce ghost echoes from the array edges when performing ultrasound imaging.

The mutual structural coupling between the cells, which was briefly introduced in Section 2.1.7, can also be calculated, like it as done for the TR2 probe array. The Bragg frequencies are found from

Table 7.1: Designed TH1 A transducer parameters

Design parameter		Unit
Array		
Number of elements	190+190	
Element pitch	95	µm
Element width	92.5	µm
Kerf	2.5	µm
Element length	18.05	mm
Element thickness	100	µm
Apodization length	1.43	mm
Apodization sub-element count	15	
Array side length	2.12	cm
Center frequency in air (biased)	23.6	MHz
Center frequency in air	27.5	MHz
Center frequency in immersion	12.3	MHz
CMUT cell		
Cell side length (square)	37	µm
Cell electrode side length (square)	33	µm
Number of cells in sub-element	4	
Distance to cell kerf	5.25	µm
Cell to cell distance in sub-element	8	µm
Distance to neighbouring element cell	13	µm
Plate thickness	2.5	µm
Al electrode thickness	1000	nm
Vacuum gap	135	nm
Electrode thickness (Cr|Au)	10|280	nm
Plate nitride thickness	200	nm
Pull-in voltage	187	V
Operating voltage	150	V

the first few repeating periodic cell distances in the cell design, shown in Fig. 7.3

$$
\begin{aligned}
d_1 &= 45 \\
d_2 &= 50 \\
d_3 &= \sqrt{45^2 + 45^2} = 63.64 \\
d_4 &= 95 \\
d_5 &= \sqrt{45^2 + 95^2} = 105.12 \\
d_6 &= 140 \\
d_7 &= \sqrt{95^2 + 140^2} = 147.05.
\end{aligned}
$$

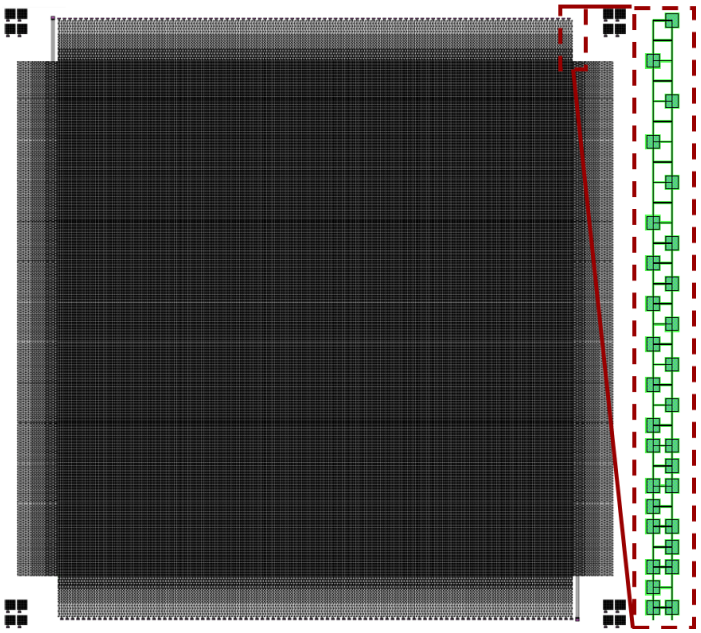


Figure 7.2: Design overview of the transducer human 1 (TH1-A) array design from L-Edit. The drawing shown is from the last mask layer for separating the deposited aluminium layer called *Top electrode*. A zoom-in inset is shown to the right of one end of an element, illustrating the apodization region of the 190+190 array. This is made up of 15 sub-elements with a varying cell count, and orientation, from 3 to 1 cells, which reduces the emitted amplitude approximately according to a Hanning window function. Four linear test elements can be seen in each corner of the array.

The corresponding Bragg frequencies are situated in the frequency spectrum at

$$f_{\mathrm{B},1} = \frac{1540\,\mathrm{m\,s^{-1}}}{45\,\mu\mathrm{m}} = 34.2\,\mathrm{MHz} \tag{7.16}$$

$$f_{\mathrm{B},2} = \frac{1540\,\mathrm{m\,s^{-1}}}{50\,\mu\mathrm{m}} = 30.8\,\mathrm{MHz} \tag{7.17}$$

$$f_{\mathrm{B},3} = \frac{1540\,\mathrm{m\,s^{-1}}}{63.64\,\mu\mathrm{m}} = 24.2\,\mathrm{MHz} \tag{7.18}$$

$$f_{\mathrm{B},4} = \frac{1540\,\mathrm{m\,s^{-1}}}{95\,\mu\mathrm{m}} = 16.2\,\mathrm{MHz} \tag{7.19}$$

$$f_{\mathrm{B},5} = \frac{1540\,\mathrm{m\,s^{-1}}}{105.12\,\mu\mathrm{m}} = 14.7\,\mathrm{MHz} \tag{7.20}$$

$$f_{\mathrm{B},6} = \frac{1540\,\mathrm{m\,s^{-1}}}{140\,\mu\mathrm{m}} = 11\,\mathrm{MHz} \tag{7.21}$$

$$f_{\mathrm{B},7} = \frac{1540\,\mathrm{m\,s^{-1}}}{147.05\,\mu\mathrm{m}} = 10.5\,\mathrm{MHz} \tag{7.22}$$

$$\tag{7.23}$$

where $f_{\mathrm{B},3}$ to $f_{\mathrm{B},7}$ will potentially appear inside the bandwidth of the 12 MHz center frequency if the bandwidth is assumed to be 100 %.

The substrate ringing introduced in the same section will be calculated from Eq. (2.45) using a borosilicate substrate with a thickness of 500 µm and a speed of sound at 5560 $\mathrm{m\,s^{-1}}$. The substrate ringing will appear in the frequency spectrum at

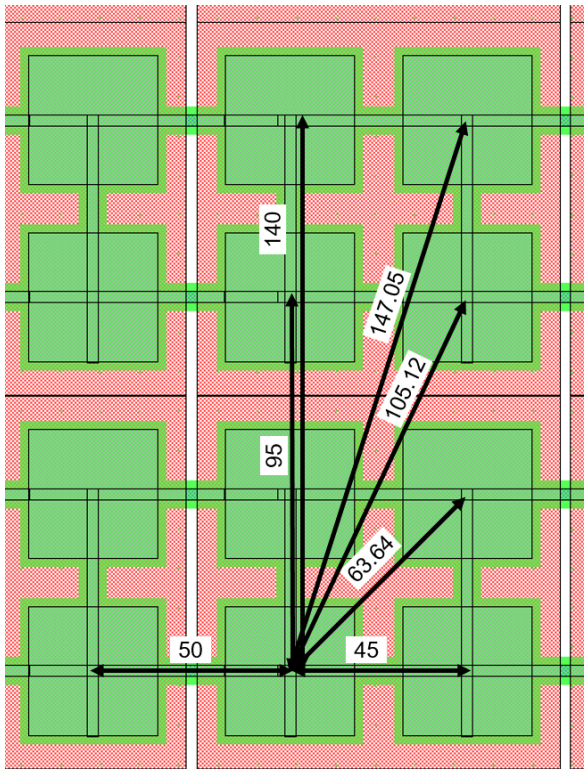


Figure 7.3: Seven nearest cell distances in the TH1 array design from L-Edit. The bottom electrodes and square cell cavities (green) are depicted going from left to right across the image and the top electrodes (peach red) in the orthogonal direction.

Table 7.2: Numerical values of ω_{nm} in [MHz]

m \ n	0	1	2	3
0	27.77	57.78	94.79	138.71
1	108.08	165.29	229.86	301.66
2	242.14	326.38	417.97	517.17
3	429.93	541.08	659.57	785.94

$$f_{\text{Sub}} = \frac{c_{\text{Boro}}}{2\,t_{\text{Boro}}} = \frac{5560\,\text{m}\,\text{s}^{-1}}{2\,500\,\mu\text{m}} = 5.56\,\text{MHz}. \tag{7.24}$$

Furthermore, the eigenfrequencies of the vibrational modes of the CMUT cell can also be found from using the numerical values for k_{nm} in Table 2.2 and Eq. 2.52. These have been calculated for the frequencies in vacuum and are given in Table 7.2. The first and second eigenfrequencies are $\omega_{00} = 27.77\,\text{MHz}$ and $\omega_{10} = 57.78\,\text{MHz}$, respectively, where it is seen that the former is close to the unbiased resonance frequency found from COMSOL in vacuum at 27.5 MHz with $h = 2.5\,\mu\text{m}$. The second mode be expected to lie at approximately double the resonance frequency at $f_{2\text{nd}} = 2 \times 12.3\,\text{MHz} = 24.3\,\text{MHz}$ when biased at 150 V.

Now that the dielectric layer thickness and the finalised gap height has been found, the element capacitance can be calculated. The capacitance is estimated from from the simple parallel plate capacitance at zero bias from Eq. (2.22)

$$C_0 = \left(\frac{g_{\text{vac}}}{\epsilon_0\, A_{\text{elem,-apo}}} + \frac{g_{\text{ni}}}{\epsilon_{\text{ni}}\epsilon_0\, A_{\text{elem,-apo}}} \right)^{-1} \tag{7.25}$$

$$= \left(\frac{135\,\text{nm}}{8.854 \times 10^{-12}\,\text{F}\,A_{\text{elem,-apo}}} + \frac{200\,\text{nm}}{6.86 \times 8.854 \times 10^{-12}\,\text{F}\,A_{\text{elem,-apo}}} \right)^{-1} = 47.2\,\text{pF} \tag{7.26}$$

where $A_{\text{elem,-apo}}$, at $874\,862\,\mu\text{m}^2$, is the area of the metal bottom electrodes of the main part of the element, excluding the apodization region which is not biased when performing the electrical characterisation. When fully biased during scanning, including the apodization regions, the element will instead have an expected capacitance of $C_0 = 51.6\,\text{pF}$.

In comparison, an element from a 16+16 RCA array, which will be included in the wafer layout, will have 36.2 pF.

An important advantage of utilising the anodic bonding technique, is that during fabrication of the CMUT cells the cavities can be etched directly in a glass substrate and metal can be used as the bottom electrodes. In Chapter 2, the resistivity of the gold deposited using e-beam deposition in the DTU Nanolab cleanroom facilities was compared in Table 2.4 to the highly doped silicon wafers used to fabricate the TR2 probe. The resistivity was measured to be three order of magnitude lower than silicon at $\rho_{\text{au}} = 3.15\,\Omega\,\text{cm}$.

To ensure a minimum amount of signal loss along a single element, the electrode thickness and size can be adjusted to reduced the resistance, ideally aiming for an ωRC product below < 35, which translates to a 1 % signal amplitude loss at the end of the element.

This process is also an iterative design process, as the anodically bonded array layout has multiple cell parameters which controls the electrode resistance. Each square cell has a side length, equalling the plate size, and a smaller square electrode placed inside the cell with a safety margin from the electrode to the cell wall. Wider and thicker electrodes are desirable, but can make mask alignment (both manual and automatic) more problematic and reduce the yield. The electrode leads connecting the individual CMUT cells, as seen as in Fig. 7.3, also have to be taken into account. These interconnects

account for most of the electrode resistance.
A sub-element with four square cells was chosen with a side length of 33 µm and a electrode to cell wall margin of 2 µm. This gives an interconnector width of 3 µm.

An estimate of the electrode resistance is now given. Based on the geometric model and illustrations from [58] the square electrodes connected with wires are modelled as trapezoidal resistor elements

$$R_{\text{square}} \approx \frac{\rho}{h}\sqrt{\frac{d+w}{d-w}}\ln\left(\frac{d}{w}\right) \tag{7.27}$$

where ρ is the electrode resistivity, h the thickness, d the electrode side length and w the interconnecting wire width. Two of these are in series in a sub-element with connecting wires of two length 12 µm and 17 µm. This segment is connected parallel with an identical set of cells and wires, simplified below as a left and a right side

$$R_{\text{sub-element}} = \left(R^{-1}_{\text{squares+wires,left}} + R^{-1}_{\text{squares+wires,right}}\right)^{-1}. \tag{7.28}$$

In an element there will be $190 \times R_{\text{sub-element}}$, not including the resistance from the two apodization regions. The apodization, which is shown in a closer look in Fig. 7.2, has fewer cells and longer connecting wires, significantly increasing the resistance. Be measuring the length of each of the wires and the number of cells and adding all the resistors for both sides of the element, an expression for the element resistance depending on the electrode thickness is found

$$R_{\text{element}} \approx \frac{54.33\,h + 0.21}{h^2}. \tag{7.29}$$

Using this together with the element capacitance and the resonance frequency of 12.3 MHz the following criterion can be set up

$$\omega RC = \omega_r\, C_0\, R_{\text{element}} = 2\,\pi \times 12.3\,\text{MHz} \times \left(\frac{54.33\,h + 0.21}{h^2}\right)\Omega \times 51.6\,\text{pF} < 0.35 \tag{7.30}$$

and by solving for h, a gold electrode thickness of 623 nm is found. This would in turn mean that the cell gap would have to be 623 nm + 135 nm = 758 nm. Achieving a cell depth or gap of 758 nm with wet etching of glass is possible, but has not been tested before in this group. It was decided for this fabrication process to keep the depth to around 400 nm, which is a typically used cavity depth in this group, to limit the number of unknowns. A gold electrode thickness of 280 nm was ultimately chosen. An adhesion layer of 10 nm chromium between gold and glass was used. The effect on the resistance from this layer is minimal and not included.

The new metal thickness gives a total electrode resistance of 196.7 Ω and an ωRC product of 0.78. The signal amplitude is then expected to drop to

$$|H(L,\omega)| = 95.2\,\% \tag{7.31}$$

equalling an attenuation of 4.8 % which is deemed acceptable.

In comparison the ωRC value of the top electrode, using the resistivity of Al of $\rho_{\text{Al}} = 2.7 \times 10^{-6}\,\Omega\,\text{cm}$ from Table 2.4, becomes

$$\omega RC = \omega_r\, C_0\, R_{\text{Top\_elec}} = 2\,\pi \times 12.3\,\text{MHz} \times \left(\frac{L_{\text{Top\_elec}}}{W_{\text{Elem}}\, t_{\text{Al}}}\rho_{\text{Al}}\right) \times 51.6\,\text{pF} = 0.02 \tag{7.32}$$

$$|H(L,\omega)| = 99.9\,\% \tag{7.33}$$

where $L_{\text{Top\_elec}} = 20\,900$ µm is the length of the top electrode, $W_{\text{Elem}}92.5$ µm is the width of the element, and $t_{\text{Al}} = 1000$ nm is the thickness of the metal top electrode. The signal amplitude is expected to attenuate by less than 0.1 %, even for frequencies up 50 MHz.

7.3 Array Overview

All the necessary design parameters of the CMUT array has now found and the design can be drawn in L-Edit. The array will be fabricated on a 4-inch (10 cm) borosilicate wafer. Multiple arrays other than the large 190+190 RCA array are also included for characterisation and destructive tests. Most of the available area on the wafer has been utilised in this way. Compared to the TR2 wafer layout in Fig. 4.5, only four 190+190 RCA arrays are included. The overview of the wafer is seen in Fig. 7.4 from the mask file *TH1_mask_October2020_ben1_V4*, which is annotated with all the included structures. These are

Total arrays & elements on wafers

Row-column:

- 4 x 1 RC 190+190
- 2 x 8 + 2 x 11 RC 16+16 = 38
- 2 + 4 x 3 RC 16+16 with a top frame = 14
- 2 + 4 x 3 RC 16+16 with a Bottom frame = 14

Linear:

- 4 x 12 Small test elements in the corners of the 190+190 arrays = 48
- 4 x 5 Long test element 190 = 20
- 4 x 25 Short test element 16 = 100
- 4 x 2 Linear element for deflection study = 8

Miscellaneous:

- 2 alignment marks resembling a cross which are used for conventional lithographic alignment using glass masks
- 4 alignment marks places in the north, south, east and west of the wafer for alignment when automatic computer-guided alignment is performed with the MLA machines

The long test elements 190, together with the small test elements in the corners of the 190+190 arrays, can be used for electrical characterisation of the larger arrays without probing these. The small test elements can be used to check the uniformity of the pull-in voltage across the 190+190 arrays. This could be beneficial if the contact pads of the 190+190 arrays are fragile from the processing steps or if destructive tests need be performed. The 16+16 arrays can be integrated and wire bonded to PCBs made specifically for acoustical characterisation in our MEMS lab. The groups of smaller RCA arrays also contain variations of the 16+16 arrays with frames. These are metal frames connecting either all the bottom electrodes (*bottom frame*) or all the top electrodes (*top frame*) together, as discussed in Chapter 3. This makes it possible to perform top electrode to bottom electrode measurements to find C_0 and short-circuits.

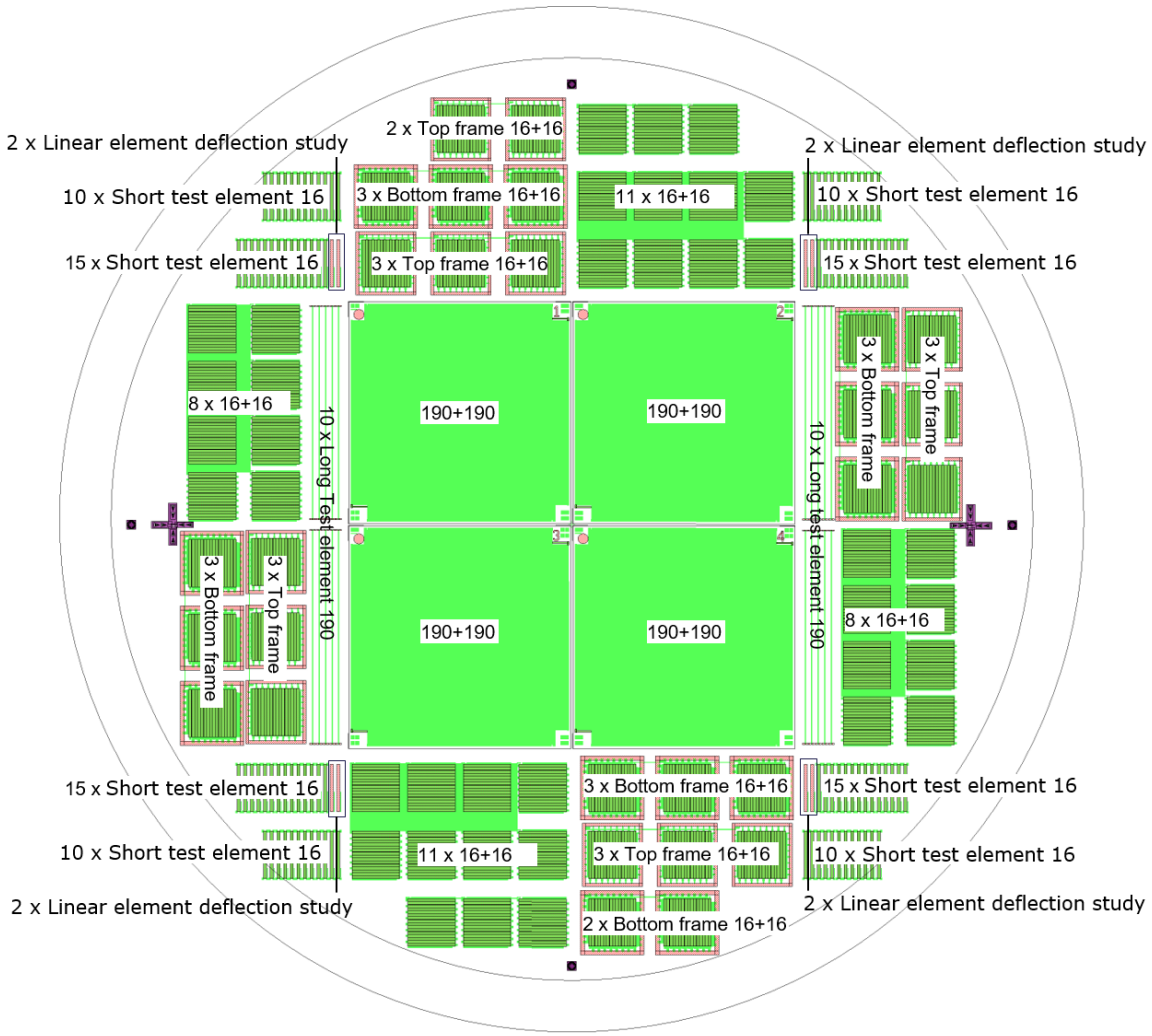


Figure 7.4: Overview of the wafer layout from L-Edit. In the centre region 4 large 190+190 RCA arrays, as depicted in Fig. 7.2, are placed. Beside all the main arrays, a section of 10 long test elements with the same amount of cells as the 190+190 elements is included. In the north, south, east and west sections are also included a number of 16+16 RCA arrays for acoustical characterisation. Some of these have a metal frame connected as discussed in Chapter 3, which either connects all the bottom electrodes (*bottom frame*) or all the top electrodes (*top frame*). In the corners of the wafer two rows of linear test elements with the same size as the 16+16 arrays are included.

7.4 Chapter summary

In this chapter, considerations regarding the design of the chip array were treated. The array presented was labelled TH1-A. Another TH1-B array was also designed based on the findings during the fabrication process and characterisation of TH1-A. This has been included in Appendix A. The geometrical parameters and properties of the CMUT cells were calculated using the procedure developed in the chapter on CMUT design. The initial design values were found from the resonance frequency in vacuum and adjusted using the COMSOL model developed in this group. Since these array design are based on a borosilicate glass substrate with metal electrodes, the electrode geometry was modelled and discussed. The metal electrode thickness was found based on the ωRC criterion, which was strictly upheld in favour of a conservative gap height. Only a small attenuation of the signal is expected. The Bragg and substrate ringing frequencies were found for the array and can potentially affect the later acoustic measurements and reduce the signal amplitude or bandwidth. The transducer frequency was furthermore increased during the design phase, from the initial 8 MHz in immersion to 12.3 MHz. This was a result based on the plate thickness available at the time of fabrication. Lastly the wafer layout was briefly presented with the various arrays fabricated.

Chapter 8

Fabrication

This chapter will describe the fabrication process used to make the glass-based TH1-A array, which utilises anodic bonding. The fabrication of both the TH1-A array and the TH1-B array along with several wafers for process optimisation was carried out in this PhD project. The focus in this part of the thesis was on the TH1-A design, which came to be used in the prototype probe, and it is therefore only the process for this array which will be presented.

In the end of this chapter the results from the fabrication and processes in need of optimising are presented briefly. The fabrication process for TH1-B will not be shown, but the optimised changes made to the process and the results are listed in Appendix A.2.

8.1 Process iterations of CMUT chips

A brief overview of the process flow is listed in Table 8.1 with a description of each step. Each step has a corresponding step in the illustrated process flow in Fig. 8.1.

8.2 Process chip A

Borosilicate glass

The wafer bonding technique used in this chip design is based on the anodic bonding process, as mentioned in Section 1.6, and for this a temperature stable glass wafer with easily movable alkali ion, such as sodium ions (Na^+), is necessary. The wafer base for the bottom substrate of this device will therefore be a borosilicate glass wafer (Borofloat 33 from SCHOTT), which was also used as the insulation layer in the TR2 arrays in Section 5.2. This thickness of the wafer is $500 \pm 20\,\mu m$. The electric volume resistivity of borosilicate glass is around $6.5\,\Omega\,cm$ at $350\,^\circ C$ [110], which is the temperature used for anodic bonding, and approximately $15\,\Omega\,cm$ at $25\,^\circ C$, which ensures excellent electrical insulation.

A common practice in the group before use is to perform a water bake-out in a $250\,^\circ C$ oven for an hour just prior to deposition to remove adsorbed water and reduce vacuum pump time.

Chromium deposition and etching

The next processing step 2) involves the definition of the mask used in etching the CMUT cell cavities. First the borosilicate glass wafers are deposited with a thin chromium layer of 50 nm in the Temescal FC-2000 e-beam evaporator. A photoresist is spin-coated on the metal surface and

Table 8.1: Overall fabrication steps of the array fabrication method based on anodic bonding. These are illustrated in the sketch in Fig. 8.1.

Step	Description
1	A borosilicate glass wafer is prepared for processing
2	Chromium is deposited, structured and used as an etching mask for an oxide etch
3	The chromium layer is removed
4	Gold is deposited and is etched through a photoresist mask using a physical sputter etch.
5	A structured PSOI wafer is anodically bonded to the bottom substrate wafer.
6	The PSOI handle and BOX layers are removed.
7	Wafer is metallised with aluminium.
8	The metal is structured through a photoresist mask.
9	An opening to the bottom electrode is made through poly-silicon
10	The bottom electrode is plugged with an aluminium deposition.
11	Finally the top electrode is structured (along the plane of the sketch) and separated.

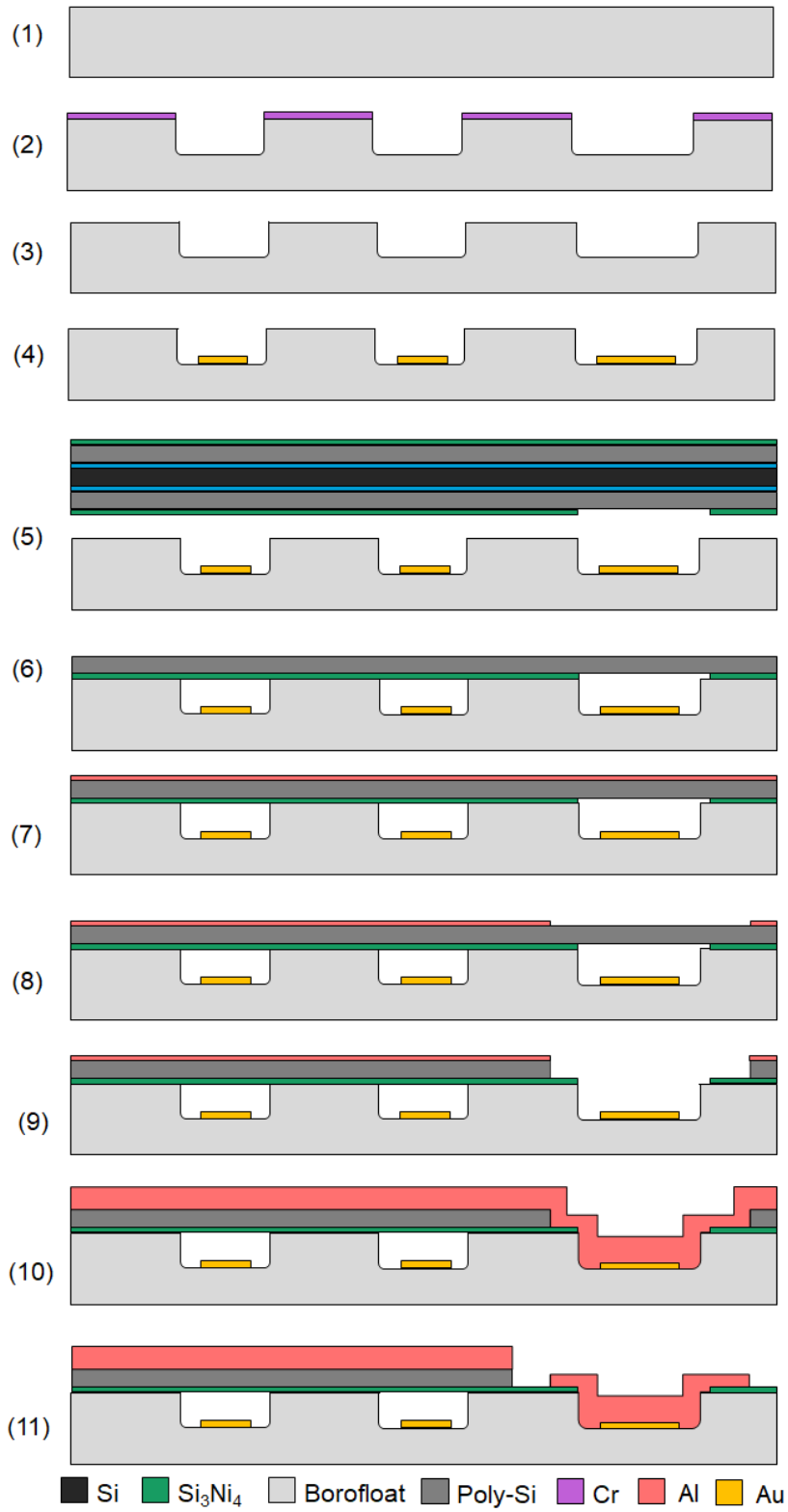


Figure 8.1: Fabrication process flow for the glass-based row-column CMUT array. The cross-section in step 9) corresponds to the cut-line in Fig. 7.1. The dimensions in the sketch are not to scale.

exposed through a mask named *Cavity* on the MLA 3 system, see Fig. 8.2, from the mask file *TH1_mask_October2020_ben1_V4*.

The chromium is then etched in a wet etchant, Chrome Etch 18 [128], which main component diammonium cerium hexanitrate ($Ce(NH_4)_2(NO_3)_6$:$HClO_4$:HCL:H_2O = 25% : 5% : 2.5% : 67.5%) converts chromium to soluble chromium nitrate

$$3\,Ce(NH_4)_2(NO_3)_6 + Cr \rightarrow {}_3Cr(NO_3)_3 + 3\,Ce(NH_4)_2(NO_3)_5. \tag{8.1}$$

The etching rate is on the order of 60 nm/min without agitation at room temperature.

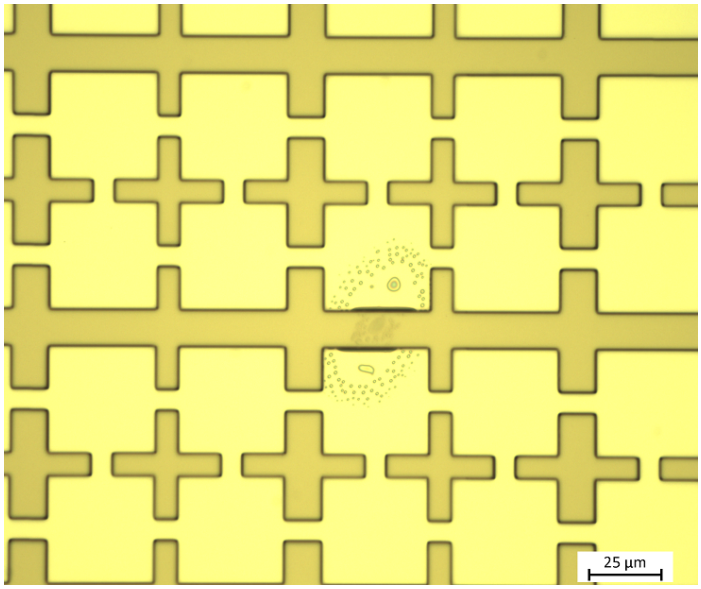


Figure 8.2: Microscope image of the *Cavity* resist mask on top of Cr metal.

Glass substrate etching

The etched chromium layer now functions as a hard mask when transferring the cavity patterns into the glass substrate. This etching of the borosilicate glass is done using the toxic and highly corrosive 12.5 % ammoniumflouride BHF, which at the used concentrations has an oxide etch rate of ≈ 25 nm/min in patterned bulk glass substrates. The simplified etching reaction is as following

$$SiO_2 + 6\,HF \rightarrow H_2SiF_6 + 2\,H_2O. \tag{8.2}$$

The photoresist mask is stripped in NMP (Remover 1165) and the chromium masking layer is removed in Chrome Etch 18. To remove trace impurites of metal and resist the substrate is cleaned in a piranha solution (H_2SO_4:H_2O_2 in 4:1) for 10 min before deposition of the bottom electrode metal. Another water bake-out is sometimes performed before further processing.

Bottom gold electrode deposition

The choice of metal used for the bottom electrodes is gold which has a resistivity around $3.15 \times 10^{-6}\,\Omega\,cm$, which was measured in the cleanroom and listed in Table 2.4. This is deposited in the Temescal e-beam system. The thickness together with the cavity depth is what defines the vacuum gap of the CMUT cells. For this particular design, a total vacuum gap of ≈ 135 nm is desired, as found in Chapter 7. The cavity depth from the previous BHF etch was 425 nm which necessitates

a metal thickness of 290 nm. However, for e-beam deposited gold to adhere to the glass substrate an intermediate adhesion layer is needed. The two most used materials are the transition metals, chromium or titanium. Both are more chemically reactive than the noble metal gold and can facilitate a chemical bond to the surface. The advantages of using Cr or Ti for this process is, however, not fully understood. Both of these metals have been used in separate processes for the TH1-A and TH1-B arrays and is discussed in Section 8.3. The choice for TH1-A was to use a chromium layer as adhesion as the metal is easily etched using the existing Chrome Etch 18.

First a 10 nm Cr layer is deposited. Then a 280 nm gold layer is deposited without breaking the vacuum, to minimise oxidation of the Cr surface and promote adhesion.

Bottom electrode sputter etching

In step 4), the electrode metal is defined using sputter etching. First a mask named *Bottom electrode* is defined in a different type of photoresist called AZ 5214E and exposed on the MLA3 system. This type is a resist for which the polarity can be changed depending on the post-exposure baking step. This has been chosen and optimised due to certain requirements on the design, which can be found in a later Section 8.3. The process step is shown in Fig. 8.3.

Next the resist and gold covered glass wafer is mounted on a chuck with six securing clamps. It is important to note that due to the poor thermal conductivity of the glass substrate, the wafer may heat up and locally damage the resist mask and underlying metal layer if the backside cooling is not distributed evenly across the layer. This is caused by an unclean chuck or due to not correctly securing that the clamps have proper contact with the wafer. The etching of gold and the underlying Ti adhesion layer is performed on the ion-beam etcher (IBE) Ionfab 300, which utilises sputtering of Ar ions to bombard and thereby etch the metal. For the process recipe called *Au acceptance -angle* an etch rate of around 40 nm/min was found.

An example of etched bottom electrodes is shown in Fig. 8.4. The gold border or halo effect seen in the figure likely comes from a shadowing effect and a re-deposition during etching. In all fabricated samples, the gold border does not extend to the edge of the cavity and interfere with the bonding process. This effect has also been studied with SEM and can be seen in detail in Fig. 8.5a and in Fig. 8.5b.

The resist, which at this point has taken surface damage from the ion bombardment, is removed in a series of plasma ashing and wet resist strip steps, all of which have been partially optimised in the process for TH1-B later, and can be found in Appendix A.2.

After the etching process the vacuum gap was checked using a profilometer. This was found to be only $g_{\mathrm{vac}} \approx 96\,\mathrm{nm}$, which would indicate that an over-etch has occurred during the IBE etching process. A further study to ensure that future batches are not over-etched was made for the following TH1-B process.

Anodic alignment bonding

The bottom and top substrates are now cleaned and made ready for bonding. The borosilicate glass wafer is cleaned in a piranha solution for 5 min to 10 min.
The solution consists of H_2SO_4, which is added first, and then H_2O_2 which makes the solution self-heat to 70 °C to 80 °C within a couple of seconds.

This is done mainly to remove any surface contaminations which include traces of resist and organic residue that are left over from the previous step. Traces of metal ions are also removed.

Before the bonding process the nitride layer on the polished surface of the PSOI wafers was structured through a resist mask called *Opening to bottom - SiN*. This is done to pre-open the nitride membrane above the bottom electrode opening, which makes the later bottom electrode etch easier to perform. During this nitride etching process, the polished poly-Si thickness was checked on a test wafer.

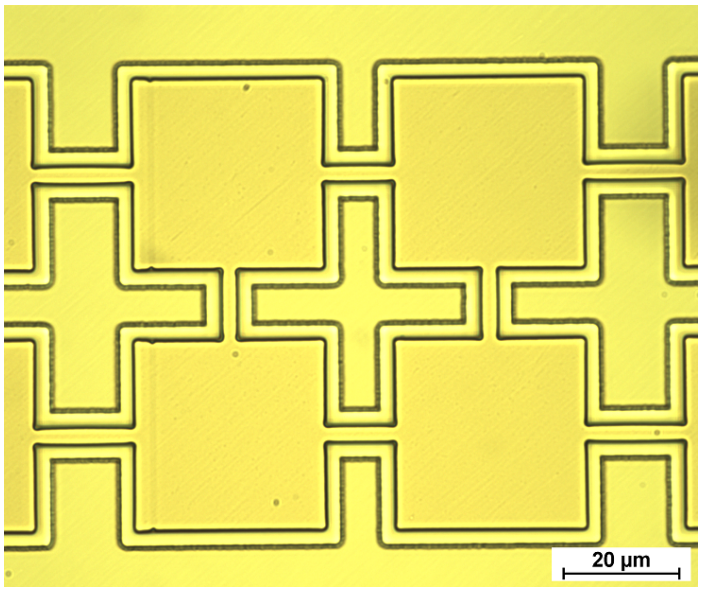


Figure 8.3: Microscope image of the *Bottom electrode* resist mask in the CMUT glass cavities on top of the Au electrode layer.

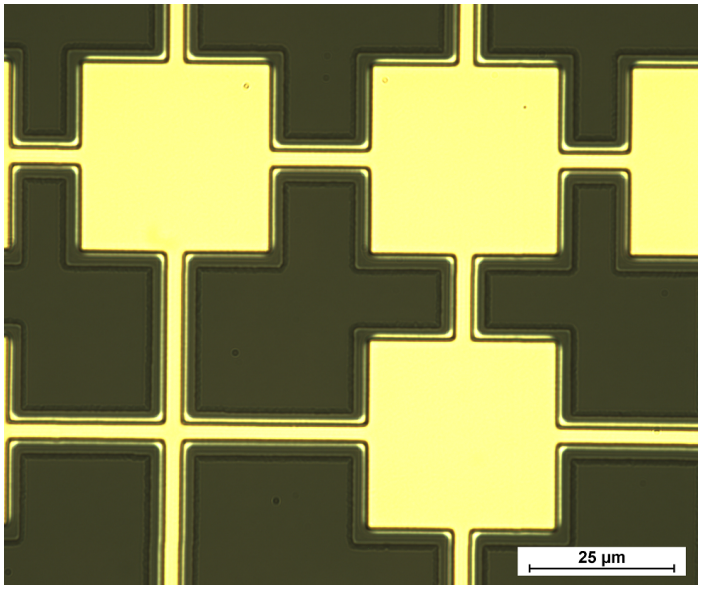
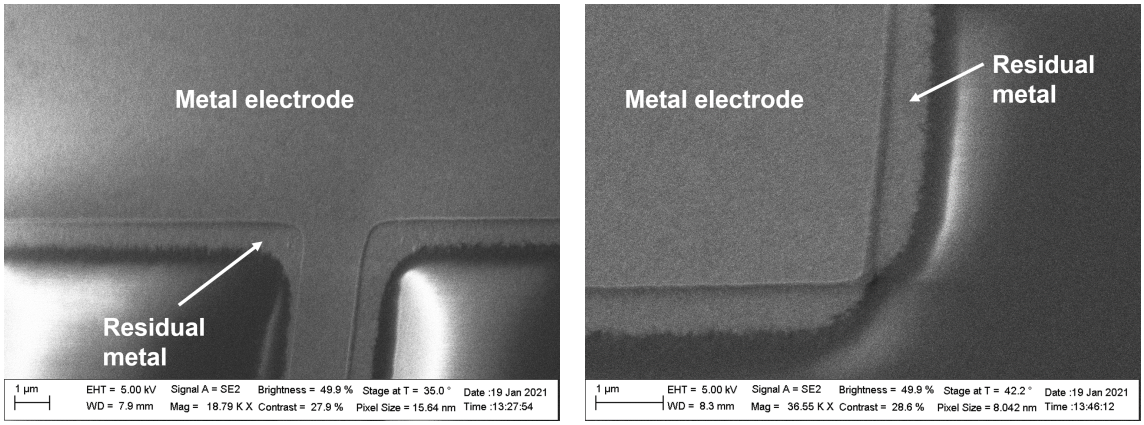


Figure 8.4: Microscope image of the *Bottom electrode* resist mask in the CMUT glass cavities on top of the Au electrode layer after IBE etching. The Au electrodes are now confined to the glass cavities. A halo effect likely caused by re-deposition is visible along the resist mask edge.



(a) **(b)**

Figure 8.5: Images taken with a SEM of the bottom electrodes on test wafers without the glass cavities etched. A residual layer of gold is seen along the edges of the gold contact from the IBE etch.

This was done by etching through the poly-Si and measuring the thickness using a profilometer. The thickness of the poly-Si plate was found an average of around 2.1 µm to 2.2 µm instead of the designed 2.5 µm. This will change the resonance frequency measured during characterisation. The nitride layer was likewise found to be 180 nm.

The PSOI is cleaned with the RCA cleaning mixture. It is only the first RCA-1 solution which is used. Since the fabrication of the TR2 chip presented in Part I, particle contamination studies of the RCA baths had been made in the MEMS-Applied Sensors group, which indicated that only cleaning with RCA-1 produced the least amount of particles. The HF dip after RCA-1 is also avoided for PSOI wafers made for this process. This is to avoid etching the silicon nitride layer has been deposited and subsequently oxidised to oxynitride on the PSOI wafers to strength the anodic bond [127].

The bonding itself is performed in a two-step process, where the wafer stack is first aligned with respect to the supplied alignment marks and then transferred to the bonder. The alignment is performed on the MA6-2, which is normally used for chromium glass mask alignment and flood-exposure, but it can be converted into an alignment bonder by exchanging the frame to one capable of interfacing with the bonding fixture used for the SB6 wafer bonder. The alignment is necessary to align the openings in the nitride layer on the PSOI to the bottom electrode pads, seen in Fig. 8.1 step 5).

When set-up is complete, the wafers are loaded by first mounting the PSOI wafer with the polished and structured front surface facing away from the fixture. Then the structured bottom glass substrate is loaded with the frontside facing towards the PSOI. The order in which the wafers are mounted serves two purposes: the first reason is explained in section 5.1.2 and is due to the polarity necessary to bond the wafer stack and not fuse the glass wafer to the bonding fixture; the second reason is so that the backside cameras equipped on the MA6-2 aligner can be used to align the two wafers through the transparent glass wafer.

The two wafers are kept separated by around 100 µm to 130 µm during alignment. This distance is necessary to avoid the wafers touching each other and forming Newton's rings. A typical alignment distance when using glass masks in combination with resist-coated wafers can be as low as a few micrometers. However, wafer bow of the substrates, and possibly also particles on the wafer surfaces, can restrict the minimum distance. The increased distance can complicate alignment and several attempts are often needed as the wafers can shift when contacting. When the wafers have been aligned, they are brought into contact and held in place by clamps, as is also done in the fusion bonding process, while the bonding fixture is transferred to the SB6 wafer bonder. This step is a

pre-bonding process.

The wafer stack is then anodically bonded, at an elevated temperature of 375 °C with a four step voltage ramp (200 V/400 V/600 V/800 V) achieving an accumulated charge of approximately 3000 mC which is an indicator for a good quality bond. The whole bonding procedure lasts around 50 min including wafer cooldown time.

Due to the transparent nature of the glass substrate, the wafer stack can immediately be inspected for voids by eye from the backside. A backside overview photo and a microscope image from one of the center arrays are shown in Fig. 8.6 and in Fig. 8.7. The voids are clearly seen along the right edge of the wafer as oblong spots with Newton's rings. An example of the openings in the PSOI nitride to the bottom electrode pads is seen in Fig. 8.7a. The slightly misaligned alignment marks used during alignment bonding are seen in Fig. 8.8.

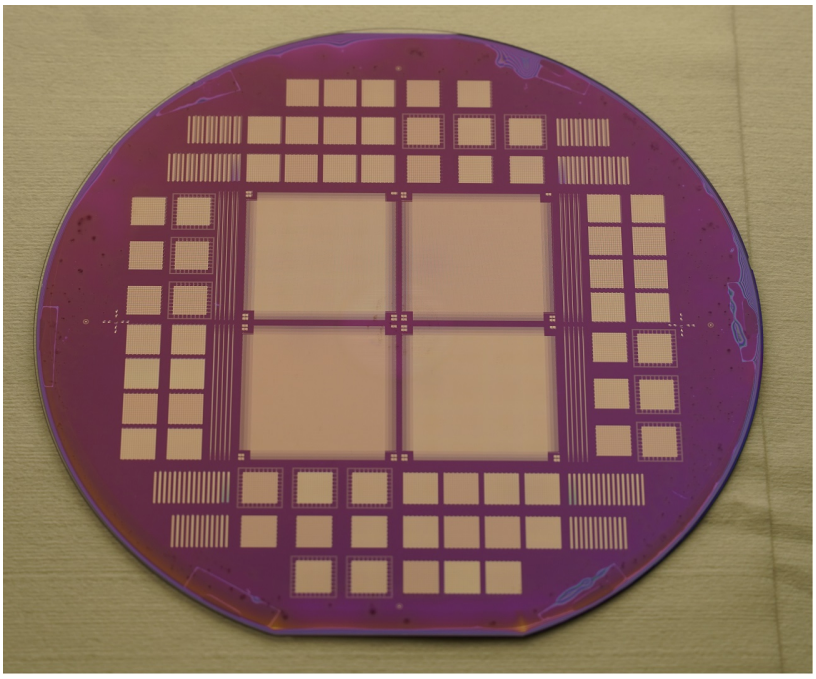


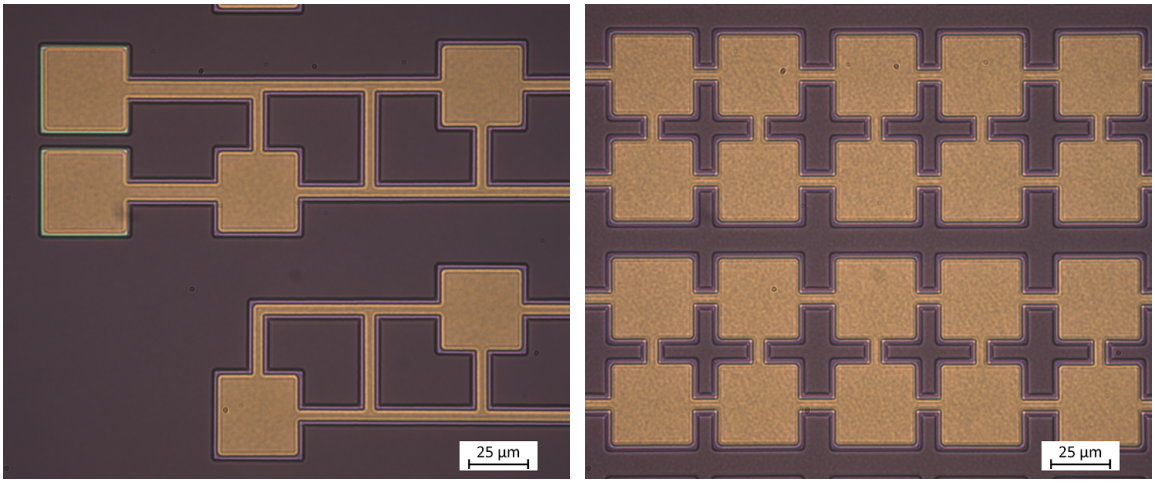
Figure 8.6: Backside of the anodically bonded wafer stack. Voids are seen in the wafer periphery in the top of the image.

PSOI handle and BOX layer removal

The next step 6) involves the removal of the PSOI wafer handle layers which are not desired in the final structure. These layers, from the top of the stack, are the silicon nitride layer, the poly-silicon layer, the first BOX layer, the silicon handle layer and the final BOX layer. With the exception of the nitride layer, which was not present in Part I, all the other layers are removed in the same way as presented in Chapter 5 Section 5.2. The etching process of the silicon nitride is performed in the ASE tool using the recipe *maengsin*, which was based on the *1SiO2_02* recipe, shown in Table 8.2.

During the silicon handle etch in KOH, any voids present will most likely result in the plate breaking off, exposing the underlying electrodes and slightly over-etch the poly-Si plate. As a result of the strong anodic bond, which has a higher tolerance for particles, the plate does not peel off the bottom substrate. This has previously been seen in this group for some wafers based on the fusion bonding technique. Voids are usually abundant around the edge of the wafer due to particles from handling the wafer.

After removing the BOX in BHF in a beaker, only the around 2.16 µm thick poly-Si plate with a



(a) (b)

Figure 8.7: Microscope image of the metal bottom electrodes inside the glass cavities. The image is taken from the backside of the bonded wafer through the 500 µm thick glass substrate.

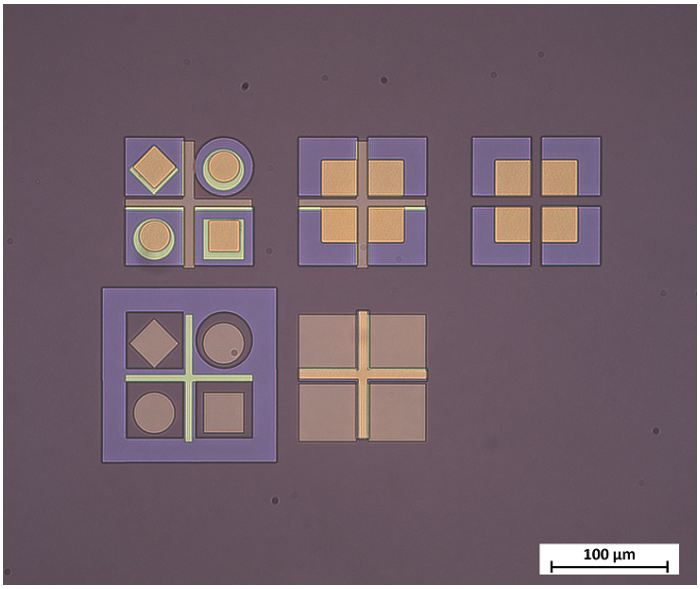
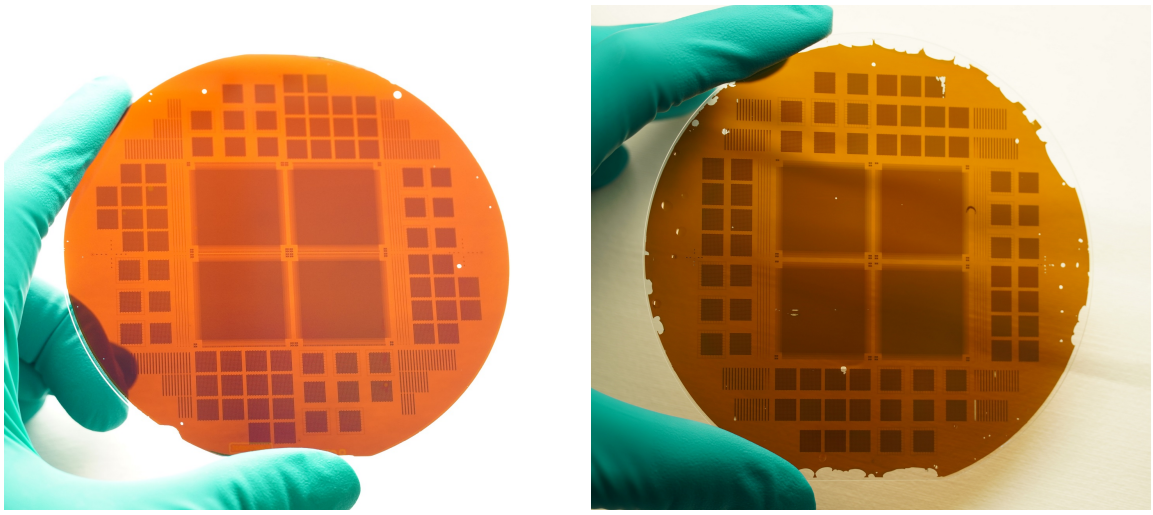


Figure 8.8: Microscope image of the alignment marks used during alignment bonding, taken from the backside of the bonded wafer stack. The marks are slightly misaligned, seen by non-concentric squares and circles in the upper left corner and by off-center cross in the lower left corner.

Table 8.2: Etching parameters for the *maengsin* nitride etching recipe on the ASE tool.

Parameter	maengsin
Coil Power [W]	150
Platen Power [W]	25
Platen Temperature [°C]	20
C_4F_8 flow [sccm]	20
H_2 flow [sccm]	0
He flow [sccm]	100
Pressure [mTorr]	2.5

180 nm silicon nitride layer remains. During this etch, or just before the wafers are rinsed, large voids which have not burst by themselves are poked with metal cleanroom tweezers. This is done to ensure that they do not burst during vacuum in later process steps and scatter plate flakes across the array or in the tool used. When manually bursting voids, there is, however, a risk that this will also create flakes which can adhere to the wafer surface. A comparison can be seen in the in Fig. 8.9a and in Fig. 8.9b, of a near perfect wafer bond, with no voids affecting the large arrays, and a bond with many edge voids and small particle resulting in etching of the large center arrays.



(a) **(b)**

Figure 8.9: Photo of two wafers with a slightly different wafer layout and their handle layers removed. (a) can be seen to have very little voids not affecting any of the large arrays or smaller test arrays. (b) can be seen to have multiple small voids in the periphery and in the large center arrays, which will result in some unusable elements.

Initial metallisation

In the following step 7) the poly-Si plate is metallised with a layer of 200 nm aluminium. This is also performed in the Temescal e-beam evaporator. This layer is thinner than the typical thickness of 400 nm used because the aluminium is primarily used as an etching mask. The surface is spin-coated with a positive resist (2 µm AZ MIR 701) and the mask called *Opening to bottom - Poly* is used to pattern wafer and make openings over the bottom electrode pads.

Bottom electrode access through metal

The aluminium is then etched in a batch process using the etchant PES (PES-77-19-04) [117] in a beaker for about 5 min, with an etch rate at ≈ 40 nm/min, or until visual feedback is observed. The resulting structure is depicted in step 8), Fig. 8.10, after the resist has been removed in a plasma ashing process.

Bottom electrode access through poly-silicon

In step 9), the same aluminium mask is used for etching through the poly-silicon covering the bottom electrode pads. This procedure is performed using the ASE tool and the recipe *shallolr*. Recipe parameters in Table 8.3. This process is timed so that only one or two cycles of over etch is done. This is to minimise under-etching of the plate and to avoid potentially damaging the electrodes themselves. The openings can be seen in Fig. 8.11, where the etch is stopped on the silicon nitride layer bonded to the glass substrate.

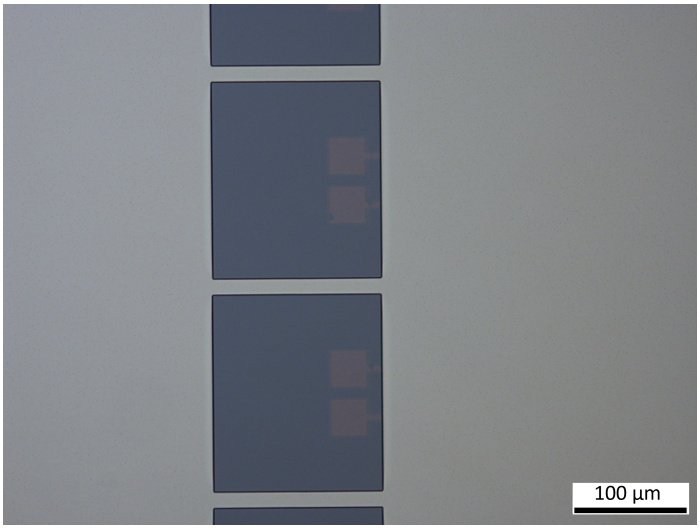
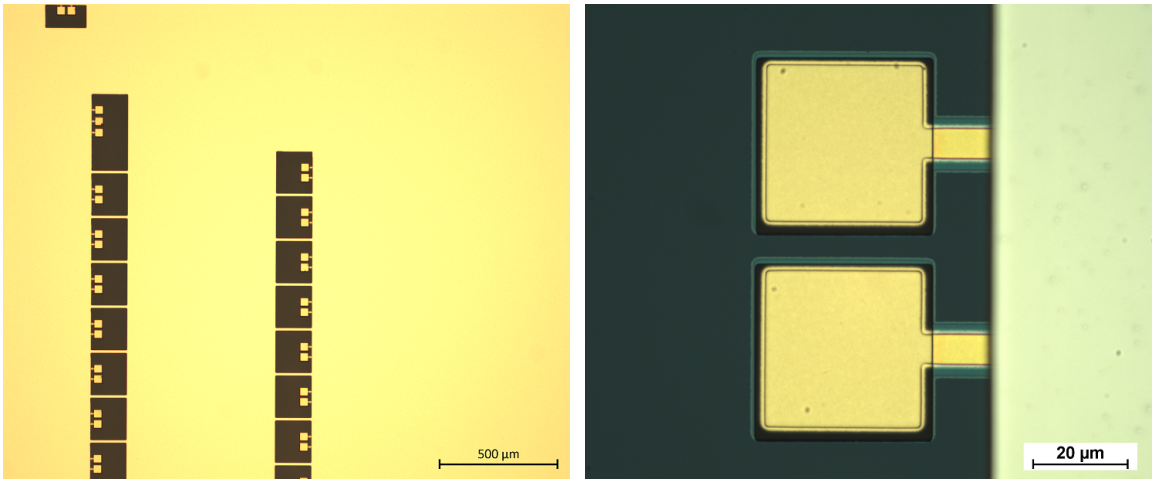


Figure 8.10: Microscope image of the opening in the aluminium to the poly-Si plate covering the bottom electrodes. The mask used is *Opening to bottom - Poly*.

Table 8.3: Parameters for the shallolr bosch etching process used in the ASE tool. 1 min and 9 s corresponds to 6 etching cycles.

Common paramters		Multiplexed parameters		
Parameter	Setting	Parameter	Etch	Passivation
Platen Temperature [°C]	10	SF_6 flow [sccm]	260	0
No. of cycles	5	O_2 flow [sccm]	26	0
Process time [min:s]	01:09	C_4F_8 flow [sccm]	0	120
APC mode	manual	Coil Power [W]	2800	1000
APC [%]	86.8	Platen Power [W]	16	0
		Cycle time [s]	6.5	5



(a) **(b)**

Figure 8.11: Microscope images showing the completed poly-Si etch with the opening to the bottom electrode pads. No nitride is present on top of the Au gold pads because of the openings made in the nitride on the PSOI wafer using the *Opening to bottom - SiN* photo mask.

Plugging of bottom electrodes

The cavities with the bottom electrode contact pads are filled up with another layer of aluminium, and the cells are plugged. This step is also necessary in order to metallise and expand the contact pad size to dimensions similar to the top electrode pads (175 µm × 150 µm). A large contact pads is necessary for wire bonding and to access the element with probes. In the same process, the open glass trenches covered by a silicon nitride membrane are plugged with aluminium. This creates a vacuum seal inside the cells in the element.

For both of these methods to work, the deposition process needs to deliver a sufficient step coverage so that the small contact pads (37 µm × 37 µm) are connected to the larger pad, and so that the glass channel is sealed. The deposition is performed with the Temescal tool. As mentioned, this is an e-beam evaporator which are not normally used when good step coverage is required. The system is however equipped with rotating planetary wafer holders, which improves coverage compared to stationary flat or dome-shaped deposition systems. To further improve the process, the layer thickness is set between 800 nm to 1000 nm, see Fig. 8.12, which is approximately twice the cavity depth. This brings the total top electrode metal thickness to around 1000 nm. The plugged cavities and larger electrode pad are shown in Fig. 8.13.

The quality of the aluminium plug was investigated using SEM. The entrance to the glass trench, shown in the sketch in Fig. 8.12, has been imaged and can be seen in the two figures in Fig. 8.14. The images have been taken at two different contact pad locations with a tilt of 10.5° and 20°, respectively. Fig. 8.14a shows a pile-up of aluminium right at the edge of the cavity, where the nitride layer is terminated. Two smaller bumps of metal on both sides of the main pile corresponds with the corners of the trench opening. In contrast, Fig. 8.14b depicts a flatter topology and also a smaller distance between the metal and the outline of the eletrode pad. This indicates that there is a larger overhang of the nitride layer due to misalignment during alignment bonding. Both images illustrates plugged cavities and sealed trenches.

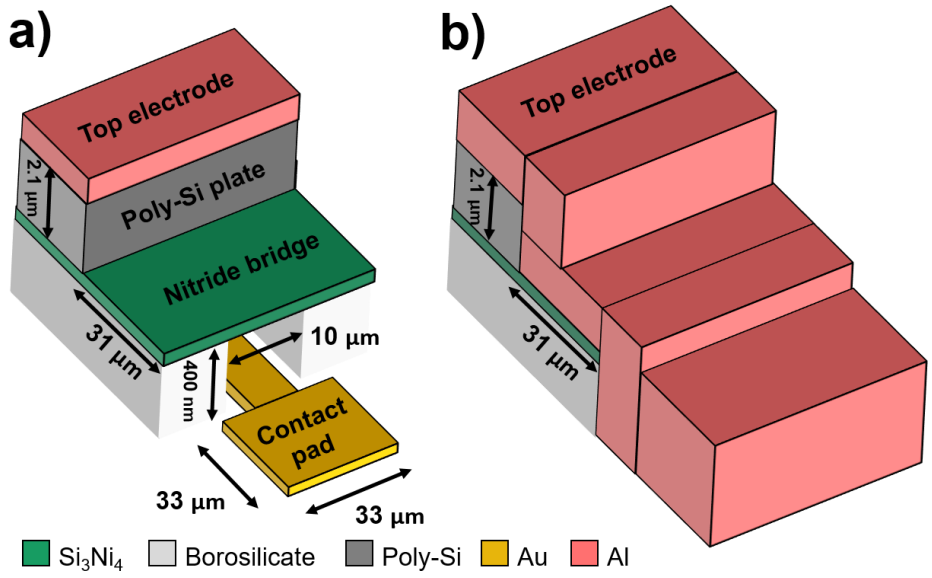


Figure 8.12: (a) Sketch of the borosilicate glass trench near the contact pad, covered by a silicon nitride bridge layer. A single 200 nm aluminium layer is on top of the plate. (b) the contact pad cavity plugged with 800 nm aluminium, which also seals the trench leading into the cells. The sketches are not to scale.

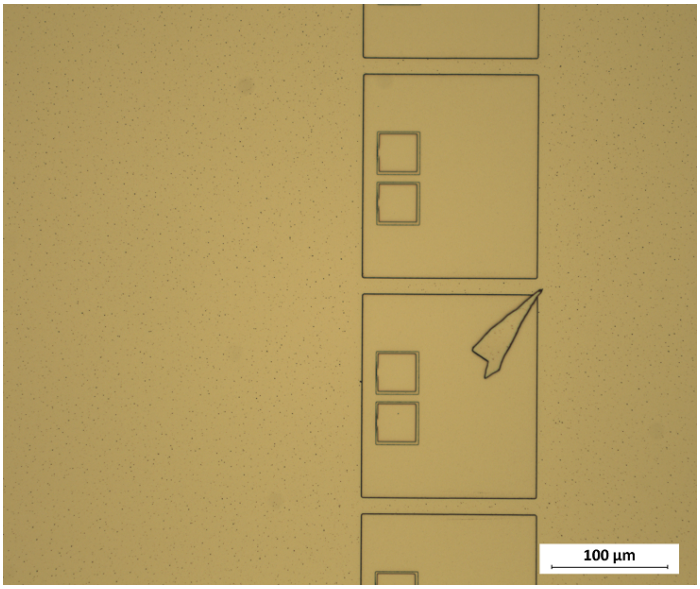


Figure 8.13: Microscope image of the Al-plugged contact pads and the larger rectangular electrode before top electrode separation. A poly-Si flake from the plate is seen partially covering one of the large contact pads.

Top electrode structuring and bottom electrode separation

The last step 11) in the process flow is separating the top electrodes by etching through the metal and poly-silicon plate. The wafer is first patterned with a positive resist and exposed using the mask called *Top electrode*. This mask outlines and separates the top electrodes and leaves a metal layer over the bottom electrode contact pads.

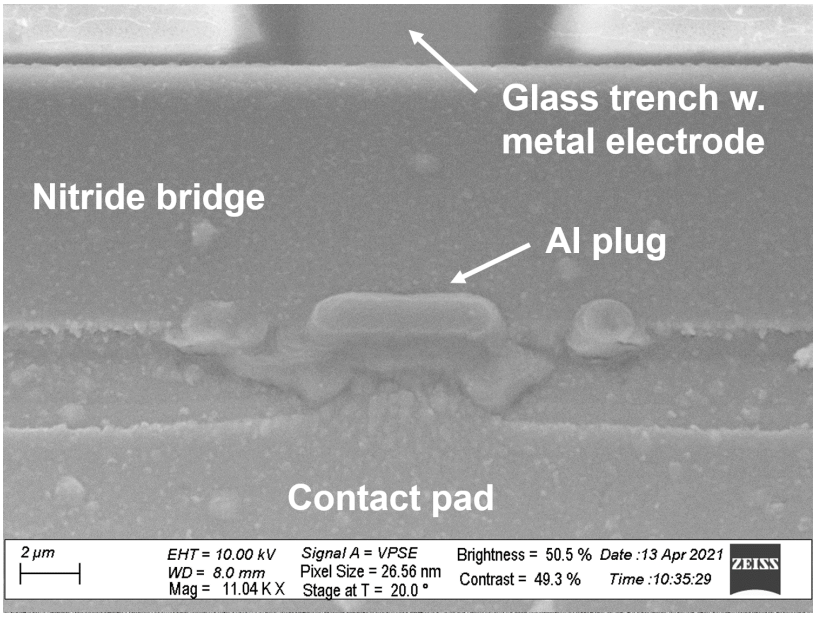
The etching process is also performed in the IBE tool using the recipe *Al etch with resist*, which in the bulk area of the wafer has an etch rate of approximately 25 nm/min. Because the tool uses physical sputter etching, an over-etch is necessary to remove metal in the trenches between the elements. The trenches in this design are only 2.5 µm wide and the corners will create a shadow effect, lowering the etch rate.

Without removing the resist the poly-silicon electrodes are subsequently etched in the ASE tool, repeating the *shallolr* recipe from step 9), which will stop on the silicon nitride layer. In this process two extra cycles are used to help ensure that the narrow trenches are completely separated.

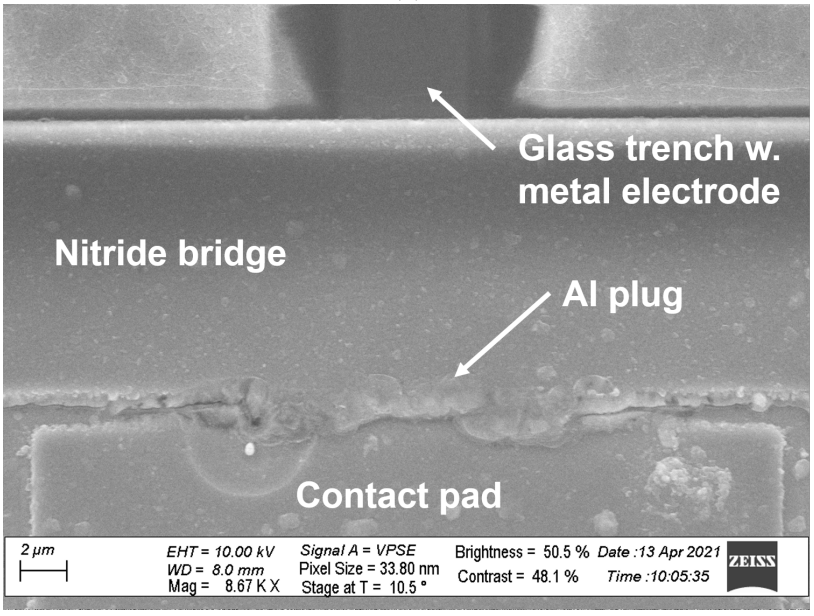
The separated top electrodes and bottom electrodes pads can be seen in Fig. 8.15a and in Fig. 8.15b, respectively. The resist mask is then removed in a plasma ashing process and the finished wafer is presented in Fig. 8.16 and the final step will be dicing the individual arrays on the wafer using the dicing saw (DISCO-DAD-321).

8.3 Process Optimisation

The fabrication of the TH1-A array wafer initially started with a batch of four substrates, each with four large 190+190 RCA CMUT arrays. Out of these four wafers, two of them were anodically alignment bonded with a PSOI wafer. The remaining two experienced problems during processing, due to the formation of ribbons, as will be explained below, and any further fabrication was stopped. One of the two bonded wafers had their wafer stack shift during bonded, which meant the openings in the silicon nitride on the PSOI wafer did not match the bottom electrode contact pad and processing was stopped.

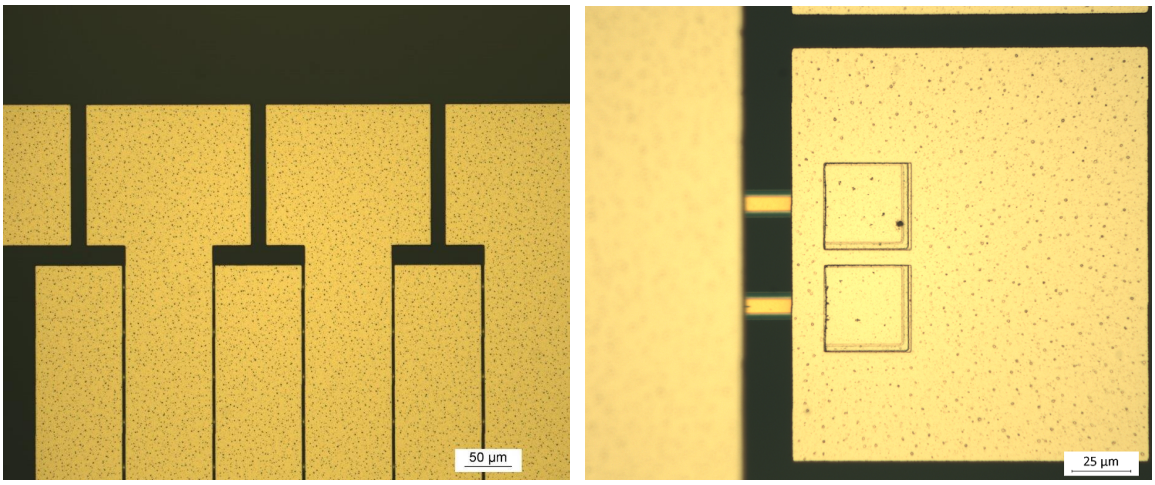


(a)



(b)

Figure 8.14: Images taken with a SEM of the bottom electrode pads after plugging them with aluminium. On (a) a large pile-up of metal is seen at the entrance to the trench. On (b) a smaller pile-up is seen and the nitride bridge layer is seen to be closer to the electrode pads in the bottom of the image, showing some misalignment during bonding.



(a) (b)

Figure 8.15: Microscope image of the to electrodes after the poly-Si etch in the ASE tool. (a) shows an overview of the the separated top electrodes. (b) show a bottom electrode pad separated from the top electrodes. The connecting leads covered by the nitride bridges are seen.

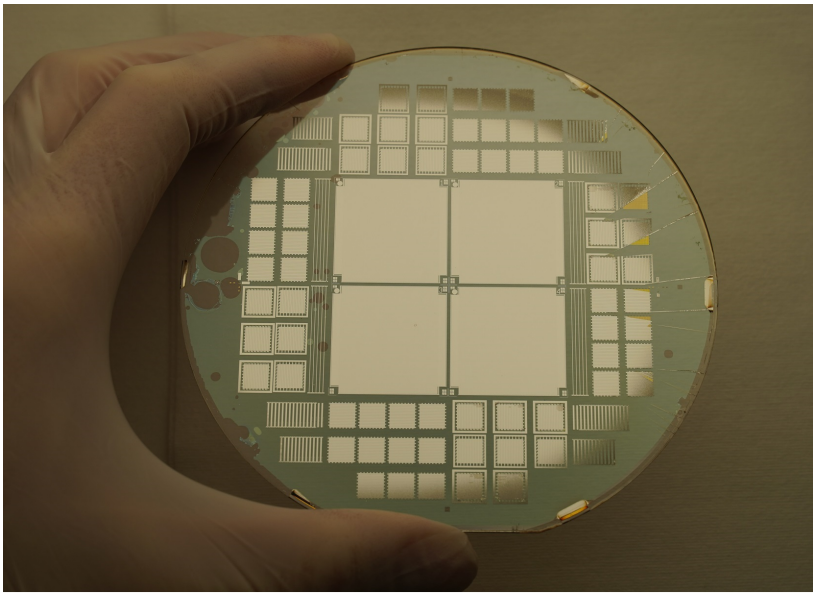


Figure 8.16: Photo of the finished TH1-A wafer after fabrication. Multiple voids in the left hand side, away from the 190+190 arrays are seen. In the south-east corner the been resist mask has burner slightly during the IBE etching process, which gives the metal a discolouration.

Processing was continued on the remaining successfully bonded wafer, which resulted in a single usable TH1-A chip.

Some of the processing steps potentially causing trouble and either altering the design parameters or making the arrays unusable are described below

- Over-etching in the IBE process
- PSOI plate polishing
- Gold ribbon formation in the IBE process
- Incomplete aluminium plugging of electrodes

8.3.1 Over-etching in the IBE process

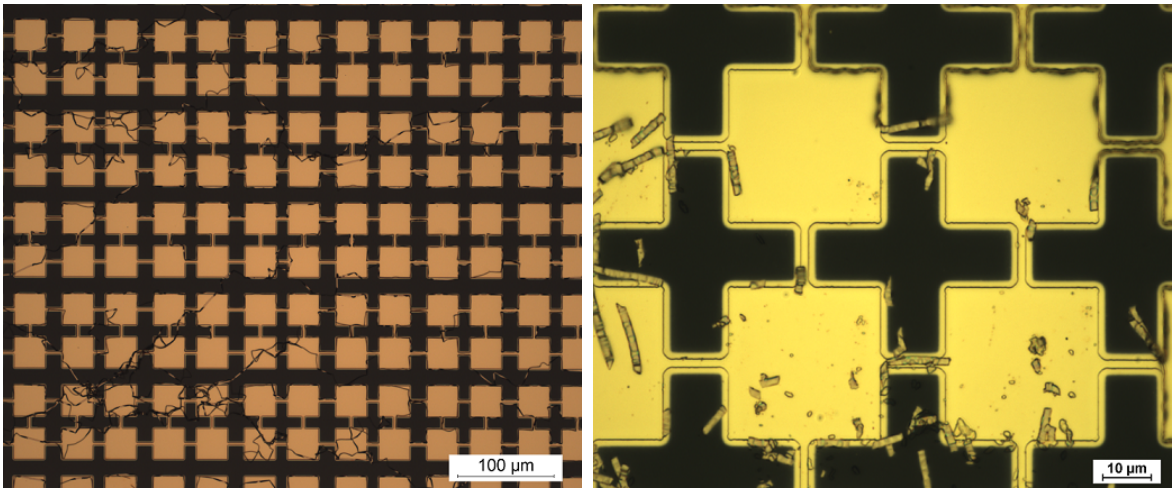
In step 4) the gold bottom electrodes are defined with a physical sputtering etch using the IBE tool. An over-etch was seen after the photoresist had been stripped and the vacuum gap was measured on a profilometer. The gaps was found to be $g_{\text{vac}} \approx 96\,\text{nm}$, indicating an over-etch of $\approx 40\,\text{nm}$. This was caused by the sputtering of the surrounding glass wafer surface, which was not taken into account during processing. The etch rate in the glass substrate is process dependent and was found to be around 22 nm/min, which can quickly have a high impact on the vacuum gap if the etch is not timed appropriately.

8.3.2 PSOI plate polishing

The PSOI wafers used in both the TR2 process and in the anodically bonded TH1 process is an important tool in the fabrication of CMUT wafers. This is due to the fact that we can fabricate the PSOI in the DTU Nanolab cleanroom and tune the plate thickness to our specifications. The fabrication process is not treated in this thesis but can be seen in Appendix B.1.3. The plate thickness is controlled by depositing poly-silicon in an LPCVD furnace and the layer thickness inspected using an ellipsometer. The wafers are subsequently polished to sub-nanometer roughness. At the time of fabrication of the TH1-A wafers, a reliable model for fitting the plate thickness using the ellipsometer had not been found, and the polishing recipe had not been optimised for minimal removal of material. This resulted in an unreliable poly-silicon plate thickness before polishing and a thickness after polishing to be different from the designed value by an average $302 \pm 51\,\text{nm}$. This was obtained using the *hm_soi_cmut_1.5min* recipe on the CMP polishing machine for 1.5 min.

8.3.3 Gold ribbon formation in the IBE process

In step 4), during the IBE etching process of the 10 nm chromium layer and the 280 nm gold layer a re-deposition or backsputtering of the metal onto the resist mask occurs. This covers the side-walls of the resist in a thin layer of metal [129]. When the resist is removed afterwards, with either a wet resist strip or plasma ashing, thin ridges or ribbons of metal are revealed. If a wet strip is used, most of these ribbons are torn off with ultrasonic cleaning and removed when the resist is dissolved. They may however re-deposit and adhere to the surface, as shown in Fig. 8.17a, which short-circuit electrodes and also prevent bonding. If a plasma ashing process is used instead, the ribbons, which are approximately the height of the resist (1.5 µm to 2.0 µm), are left free-standing and will break off, seen in Fig. 8.17b. Furthermore, the resist will take surface damage from ion-bombardment and heating, and the top layer of resist will be difficult to remove in resist strips. A small design of experiments (DOE) study was run to find the optimal resist removal procedure without causing ribbons, included in Appendix A.3. The study was not conclusive, but it was found that a combination of softening the resist with plasma ashing followed by multiple wet resist strips gave the least amount of remaining resist and ribbons.
However, repeated wet resist strips and plasma ashing can also cause electrode damage and delamination, as the Cr adhesion layer and gold layer was shown to be eroded in the plasma asher.



(a) (b)

Figure 8.17: (a) shows gold ribbons from the IBE etching process adhering to the wafer surface after a wet resist strip. (b) shows the gold ribbons breaking of the electrodes and falling onto the surface after a resist strip using plasma ashing.

This cleaning process is still currently in development in this group and several solutions have been proposed.

8.3.4 Incomplete aluminium plugging of electrodes

In step 10), the plugging of the contact pad cavities and sealing of the glass trench was occasionally found to be incomplete. This lead to a loss of vacuum inside the elements, which could affect the acoustical performance. The open glass trench also makes the CMUT cells vulnerable to plate stiction from water in the cell cavities and also metal electrode damage during etching processes or plasma ashing.

8.4 Chapter summary

In this chapter the fabrication process for the anodically bonded TH1-A chip array was presented, which was carried out in the DTU Nanolab cleanroom facilities. All the main steps of the fabrication were shown and details were provided for each of them. The resulting wafer with the TH1-A arrays chips were shown in the end. The results from the fabrication and some of the processes in need of optimising were presented briefly. The fabrication process for TH1-B was not shown, but an overview of the results are shown in Appendix A.2.
The next chapter will go into details about the electrical and acoustical characterisation of the TH1-A chip and the assembly of the modular prototype probe.

Chapter 9

Transducer Characterisation

In this chapter the first of the new generation of anodic bonded chips, the Transducer Human 1 A (TH1-A) is characterised before and after encapsulation, using some of the same setups used for the TR2 probe. A difference is here that a more thorough electrical characterisation has been performed before the chip was mounted in the prototype probe. The TH1-B array has also been electrically characterised, but since the focus of this PhD project was on the TH1-A array used in the prototype probe these measurements are not included.

The wafer layout has included many test elements and smaller 16+16 row-column arrays both with and without frames for connecting the top or bottom electrodes together. The first part of this characterisation chapter covers the electrical measurements in which many of the various test elements and smaller arrays are analysed. The focus, however, was fully characterising the south-eastern placed TH1-A chip, with the chip number 4 (*RC4SI3N4*), mounted in the prototype probe, and that is what will be presented in the following sections.
Following the pre-probe measurements, the encapsulation of the chip in the modular prototype probe will briefly be presented. Afterwards the acoustical characterisation on the probe with transmit and pulse-echo measurements will be presented and the uniformity and amplitude of the rows and column elements will be compared. Finally a pressure uniformity map will be presented as a method for evaluating the signal attenuation of the elements.

The measurements presented in the acoustical characterisation are the first transmit and pulse-echo measurements performed using the prototype probe modular platform since it was built. The TH1-A chip array is also the first chip to be installed in the probe. The acoustical results are therefore preliminary and not fully understood in the at the time of writing. Further characterisation of the prototype probe as a platform for characterising RCA chips will be necessary.

9.1 Electrical Characterisation

Electrical characterisation was performed before the wafer was diced into individual chips and wire bonded. Initial measurements are made using the B1500A Semiconductor Device Parameter Analyzer (Keysight Technologies, Santa Rosa, California, USA), seen in Fig. 9.1. These are Z-f (up to 1 MHz), IV and CV measurements, as described in Chapter 3, up to ±100 V. Impedance measurements are made using the Agilent E4990A Precision Impedance Analyzer (Agilent Technologies, Inc., Santa Clara, California, USA) together with the Agilent impedance probe kit which is connected to the Keithley 2410 Sourcemeter and a MATLAB GUI on a lab computer through GPIB. Both are used in conjunction with the Cascade Summit 12K Probe Station, which makes the characterisation using the B1500A semi-automatic and makes it possible to probe each of the 95 elements on each side of the array in one measuring sequence. This is done by controlling the probe station through GPIB

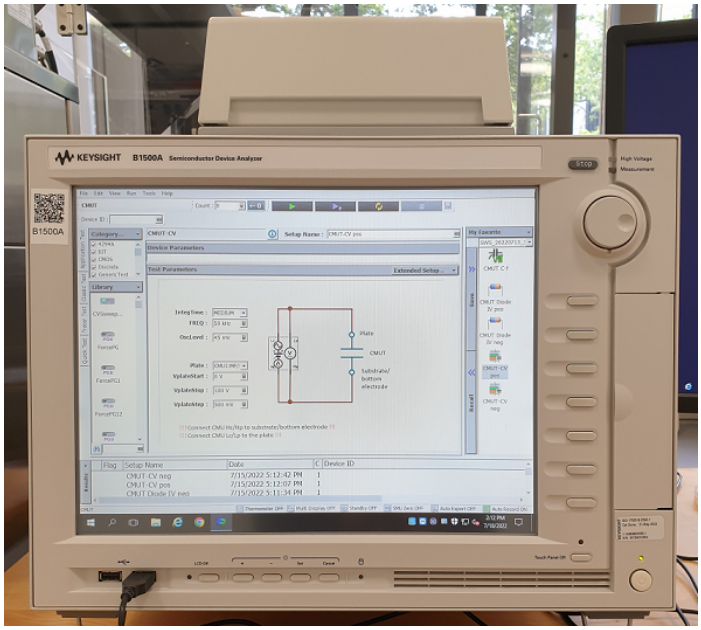


Figure 9.1: The B1500A Semiconductor Device Parameter Analyzer from Keysight used to perform Z-f, IV and CV measurements.

from the B1500A. The probe station has a wafer map with x and y coordinates of predefined chip and contact pad positions in a list, which it runs through when it receives probe move commands from the B1500A. Each set of data is measured and saved to the B1500A before a new position is probed.

9.1.1 IV, Z-f and CV measurements

The first type of measurements performed on the wafer, with chip design A, were IV, Z-f and CV on the long 190 sub-element test elements and 16+16 framed arrays, described in the Chapter 7. These are performed to quickly gauge the general performance of the CMUTs without touching the large 190+190 RCA arrays. In Chapter 3 it was mentioned that the initial Z-f measurements performed using the B1500A are used to determine if the phase angle and magnitude of the impedance has the characteristics of a capacitor, and also at which frequency the CV measurement should be made. These are low frequency studies, 10 kHz to 1 MHz, far from the resonance of the CMUT.

As a part of the initial tests, CV characteristics was tested on a few north-eastern single long 190 elements from −100 V to 100 V as described in Chapter 3, and one such CV curve is plotted in Fig. 9.2. See the wafer layout in Fig. 7.4 for the element locations. The predicted operating voltage and pull-in voltage are 150 V and 187 V as stated in Table 7.1.
It is in the figure observed that from 0 V to approximately ±60 V or ±65 V the capacitance follows a parabolic behaviour until the slope changes rapidly, which is usually seen when the CMUTs are near pull-in. The capacitive response then takes on an unusual uneven shape. Decreasing the voltage from ±100 V to 0 V, shows a sharp decline in the capacitance, descending into the the parabolic shape around ±60 V.

This clearly indicates that the pull-in occurs at voltages much lower than the designed V_{pi} voltage, and it also confirms that it lies lower than expected due to the reduced vacuum gap from 135 nm to around 95 nm to 100 nm, which was found in Chapter 8. It is estimated that the collapse happens at the first peak in capacitance, when the slope is maximum, at approximately 65 V to 70 V. This was observed on several, but not all, test elements. The operating voltage was as a result unfortunately reduced to maximum of 50 V (76 %$V_{\text{pull-in}}$) or lower, to avoid pull-in occurring in the larger 190+190

Table 9.1: TH1-A transducer parameters simulated and measured.

Updated design parameter		Unit
Array simulated		
Center frequency in air (biased)	21.61	MHz
Center frequency in air	25.16	MHz
Center frequency in immersion	10.7	MHz
190+190 element capacitance w. apodization	69.3	pF
190+190 element capacitance w.o. apodization	63.4	pF
Pull-in voltage (for a 96 nm gap)	103	V
CMUT cell measured		
Plate thickness	2.156	µm
Al electrode thickness	1000	nm
Vacuum gap	≈ 96	nm
Electrode thickness (Cr|Au)	10|280	nm
Plate nitride thickness	180	nm
Pull-in voltage (estimated from measurements)	65	V
Operating voltage	50	V

arrays.

The value of $V_{\text{pull-in}}$ simulated from COMSOL with the adjusted parameters during fabrication is 103 V as can be seen in Table 9.1.

The expected capacitance of the 190+190 arrays, without and with bias applied to the apodization region is as follows

$$C_{0,\text{-apo}} = 63.4\,\text{pF} \tag{9.1}$$

$$C_{0,\text{apo}} = 69.3\,\text{pF} \tag{9.2}$$

and the 16+16 test elements will have

$$C_{0,16+16} = 48.6\,\text{pF}. \tag{9.3}$$

In Fig. 9.3 is seen the Z-f, C-f and CV curves of a smaller element made in the same size as the 16+16 arrays. The impedance plot, Fig. 9.3c(a) shows an exemplary linear tendency with a phase angle at a constant $-90°$. The capacitance is also seen to be constant in the total frequency range in Fig. 9.3(b). The capacitance measured up to ± 50 V shows a parabolic CMUT behaviour, with a good fit as seen in Fig. 9.3(c). The extracted V_{offset} is very low at 0.27 V and $C_0 = 48.66$ pF matches quite well with what was found in Eq. (9.3).

Based on the findings of the test elements, the TH1-A chip was characterised, as described in Chapter 3, by placing the probes connected to the B1500A analyser between two adjacent top or two adjacent bottom electrodes. First either all the odd or even row or column elements are measured with the following test sequence

- Z-f - 50 mV at medium integration time
- IV positive - Sweeping up 50 V in 0.5 V steps
- IV negative - Sweeping up -50 V in 0.5 V steps
- CV positive - Sweeping up 50 V in 0.5 V steps at 10 kHz
- CV negative - Sweeping up -50 V in 0.5 V steps at 10 kHz

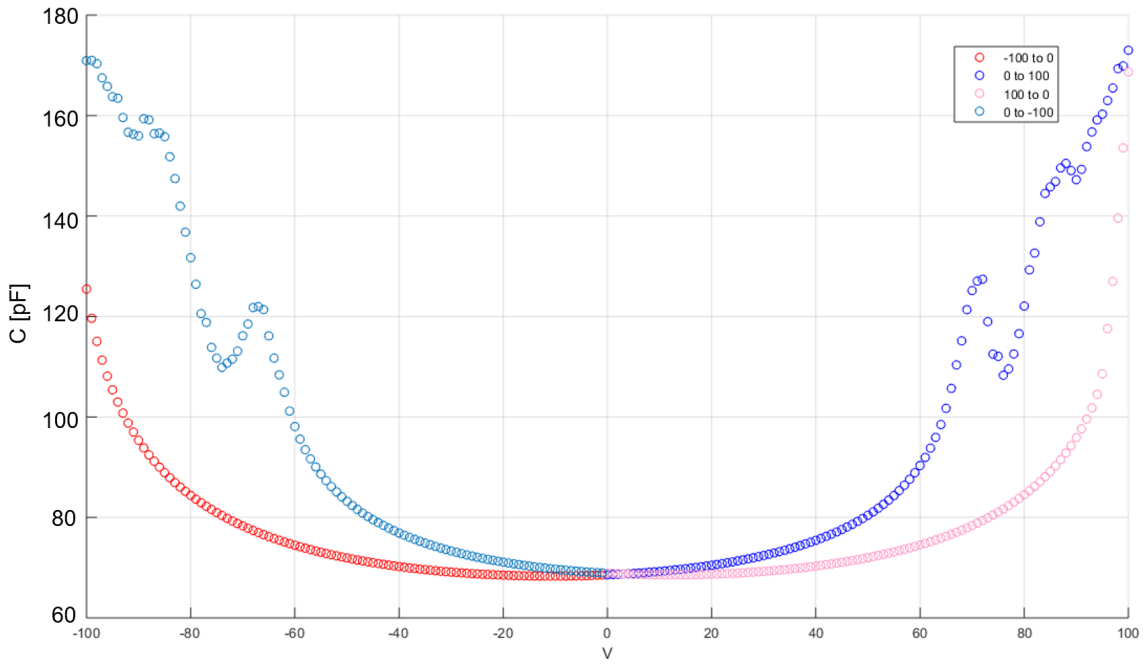


Figure 9.2: CV curve from a north-eastern long test element 190. This has been from $-100\,\mathrm{V}$ to $100\,\mathrm{V}$. The voltage has been increased past with is estimated to be the pull-in voltage at around $65\,\mathrm{V}$.

then the data is appended and sorted according the the maximum and minimum current acquired during IV test. The voltage is only set to a maximum of $\pm 50\,\mathrm{V}$, corresponding to an effective $25\,\mathrm{V}$ on each element due to the voltage division. In this way the characteristics of the array elements can be fully mapped and poor performing or short-circuited elements sorted without potentially damaging the elements or shifting the values due to early pull-in.
From here on, since the neighbouring element pairs are probed, and all data, both IV and CV curves, are plotted for top-to-top or bottom-to-bottom, the fitted C_0 value will refer to the capacitance of multiple elements. The originally calculated $C_{0,\text{-apo}}$ or $C_{0,+\text{apo}}$ from Eq. 9.1 and Eq. 9.2 still are the only values referring to the capacitance in a single element measured between the top and bottom electrode.

The IV data set for the bottom elements (the columns) is plotted in Fig. 9.4 as a bar plot and the top elements (the rows) are shown in Fig. 9.5. From the plot of the bottom elements it is seen that most of the elements are working (coloured blue), with only two short circuits between elements 141-142 and 145-146 (coloured red). Four elements have a current below the lower limit at $0.5\,\mathrm{pA}$ and are sorted as not connected (coloured green). These are elements 25, 31, 39 and 49, confirmed in microscope images in Fig. 9.6, which show that the contact pads have no aluminium and therefore have a low measured current due to poor probe contact. It is unknown why the IV test only measured a low current when the even elements 24, 30, 38 and 48 are probed, as seen in Fig. 9.4. The same low current should be seen for the neighbouring measurements. This is due to the fact that e.g. the element 25 is contacted twice during the odd and even tests, between E24-E25 and E25-E26.
Nothing unusual was found at the bottom electrode contact pads of the short-circuited elements which would indicate any bridging connection. The mean current value is $7.4 \pm 97.9 \times 10^3\,\mathrm{pA}$ and the data is summarised in Table 9.3 further below.

The plot of the maximum current of the top elements in Fig. 9.5 show that quite many of the elements have a current higher than the $100\,\mu\mathrm{A}$ limit, which indicates that these are short-circuited. Out of all the 46 shorted elements, four were picked out (9, 11, 153 and 187) and checked under a

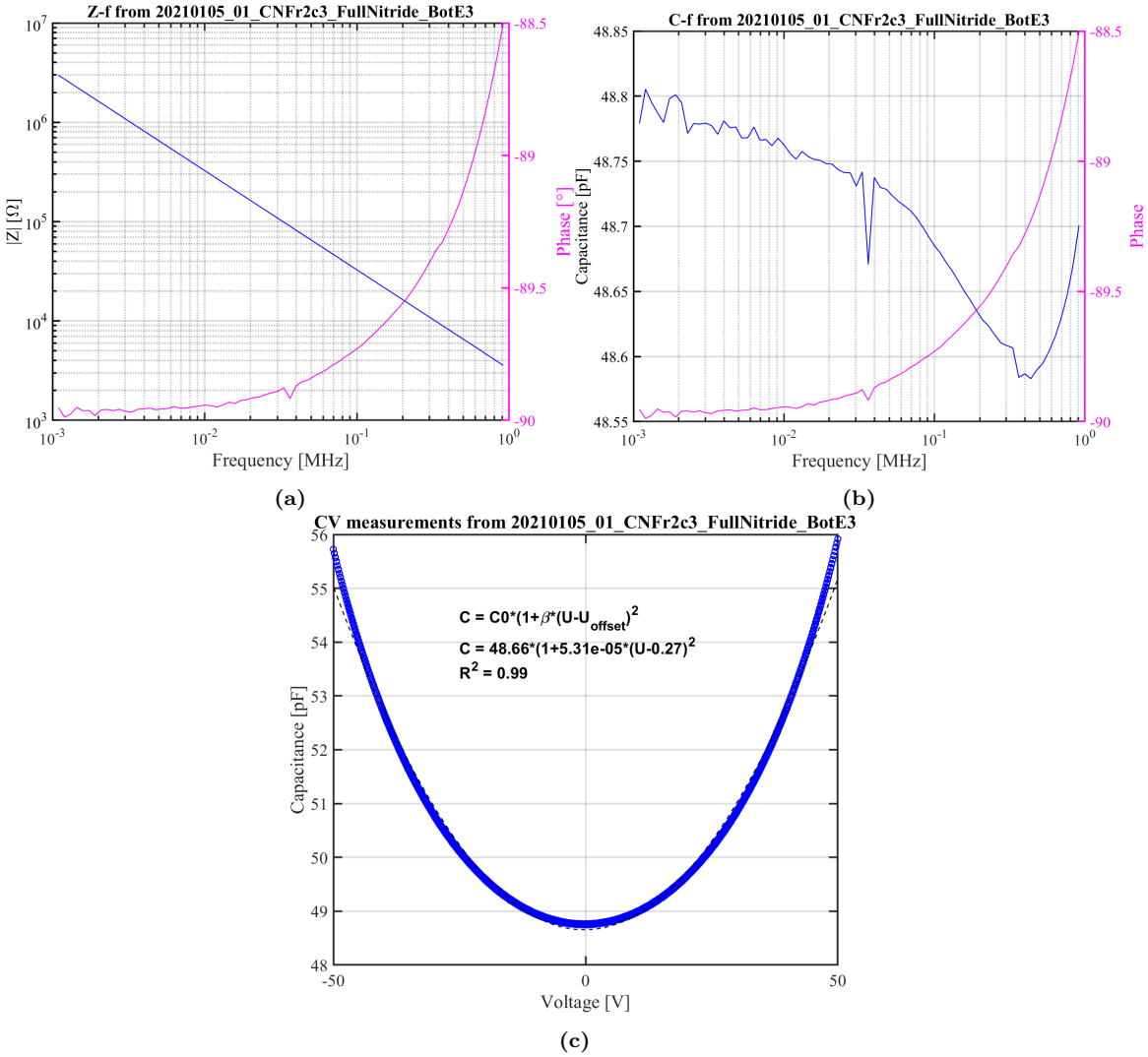


Figure 9.3: Northern 16+16 row-column array with a top frame. A bottom element has been probed up to ±50 V while the all the top electrodes are connected. A parabolic fit from Eq. 3.10 is included in the CV curve.

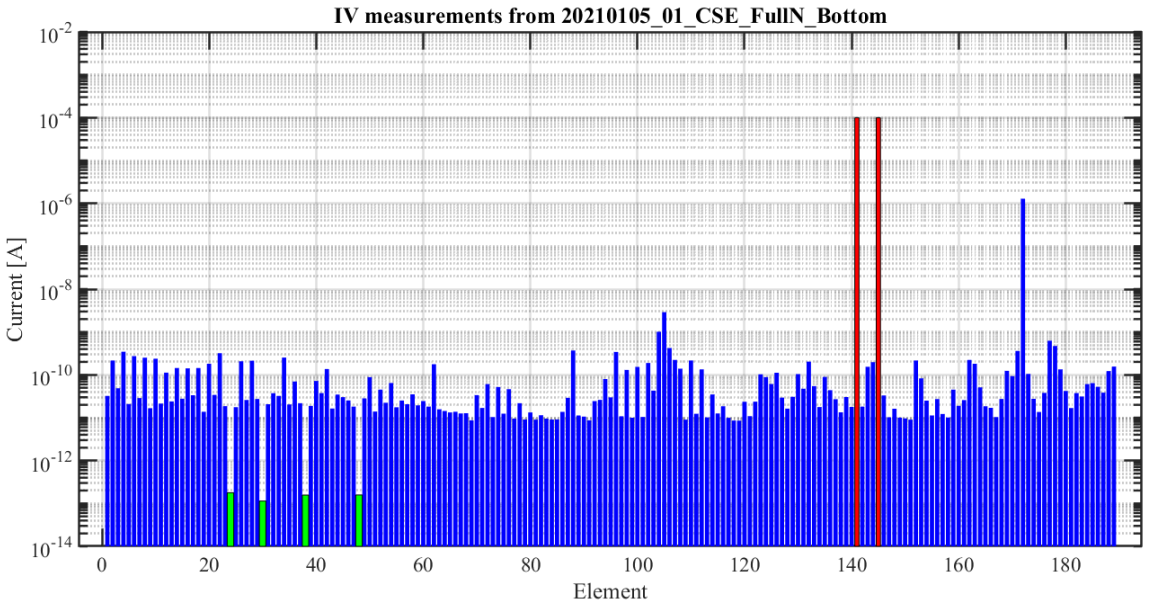


Figure 9.4: The maximum currents measured in the IV tests (on the y-axis) for each bottom element (on the x-axis) collected in a bar plot. A consistent low current from $\sim$ 50 pA to 100 pA, with a mean of $7.4 \pm 97.9 \times 10^3$ pA, is measured for most of the elements categorised as working (blue). The elements numbering 24, 30, 38 and 48 all have a current below 0.5 pA and are sorted as not being connected (green). The two elements, 141 and 145 have a current above the short circuit limit 100 µA (red).

microscope along the length of the kerf to the neighbouring element. Multiple small particles and longer strand-like defects were found all across the top electrode surface and are believed to have acted as masks during the top electrode separation etch. In Fig. 9.7 these are seen to bridge two electrodes and create a short circuit. These are likely also the cause of all the other short circuits, but was not individually checked. However, one element marked as shorted, E10, was checked extensively in the microscope and no visible bridge to its neighbour was found. The current is 163.6 ± 626.9 pA and the data is summarised in Table 9.3.

The minimum of the measured capacitances from the CV tests are plotted for the bottom and top electrodes in Fig. 9.11 and Fig. 9.12, respectively, for each element. The elements which were categorised as short-circuited in the IV tests have been marked similarly with a red colour in the plots. An overview plot of the measurement series showing a working element is shown in Fig. 9.13. In Fig. 9.11 most of the bottom elements have the same capacitance at around 30 pF to 31.5 pF but are grouped into two to three levels, with the second level value at around 43.5 pF and the third at 57.5 pF, which can also be seen from Fig. 9.14a. The first level value corresponds well with the predicted capacitance from equation Eq. (9.1)

$$C_{\text{bot-to-bot}} \times 2 = 31.5\,\text{pF} \times 2 = 63\,\text{pF} \tag{9.4}$$

$$C_{0,\text{-apo}} = 63.4\,\text{pF}. \tag{9.5}$$

The value of the second level would also correspond well with a measurement between two electrodes, with one shorted to its neighbour from Eq. (3.3) given as

$$C = \frac{(m+1)(n+1)}{m+n+2} = \frac{1 \times 2}{1+2}\,63.4\,\text{pF} = 42.3\,\text{pF}. \tag{9.6}$$

However, this argument would only make sense when the value is measured on the electrodes neighbouring the actual short-circuited elements E141-E142 and E145-E146 and not on the other observed element clusters near element 100, 130 or above 160. The reason for this higher capacitance is not yet known.

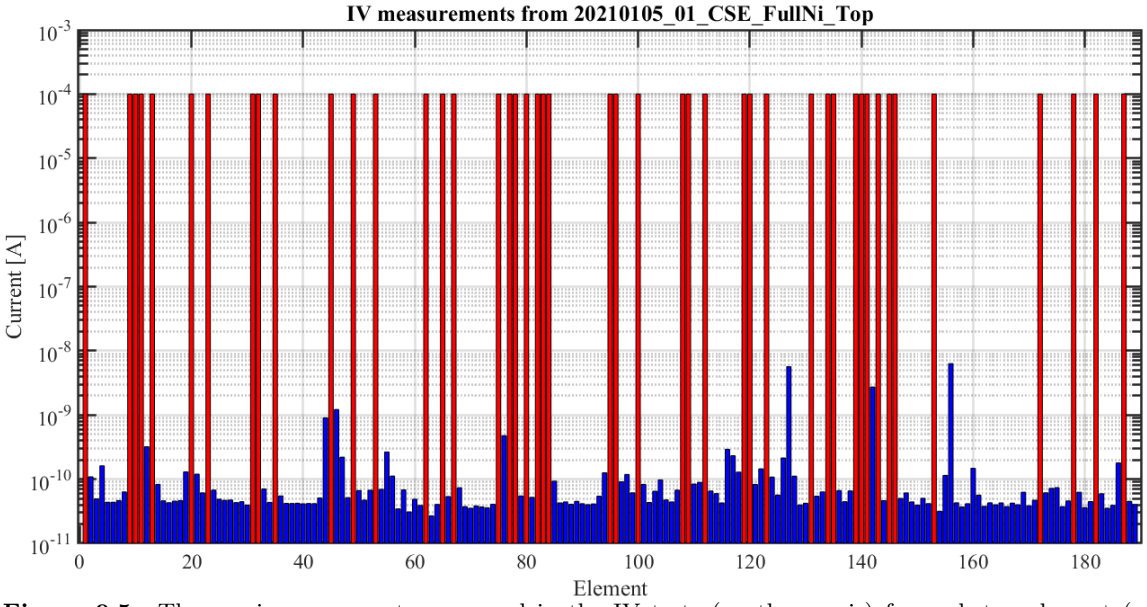


Figure 9.5: The maximum currents measured in the IV tests (on the y-axis) for each top element (on the x-axis) collected in a bar plot. A consistent low current from $\sim$ 40 pA to 110 pA, with a mean of 163.6 ± 626.9 pA, is measured for the working elements (blue). Quite a few element are short-circuited above the current limit 100 µA (red).

The value of the third level corresponds to around 9 neighbouring short-circuits seen by

$$C = \frac{1 \times 9}{9 + 2} 63.4\,\text{pF} = 57.6\,\text{pF}. \tag{9.7}$$

Whether or not it is caused by shorted elements, it is an effect of the surrounding elements with a higher capacitance at around 43.5 pF. A hysteretic behaviour has been seen in elements with both high and low capacitance, see Fig. 9.8, which indicates a dielectric charging effect. This is believed to be a different effect from the built-in V_offset charge. This discrepancy in capacitance on upward and downward sweeps in DC bias voltage is not always reflected in the fitted parabolic parameters, e.g. the fitted V_{offset} values are smaller than they appear visually on the plots due to the symmetry of the plotted data. The average fitted V_{offset} is -0.04 ± 1.45 V for the bottom electrodes and 0.23 ± 0.73 V for the top electrodes, and the data for C_{min}, C_0 and I_{max} is listed in Table 9.3.

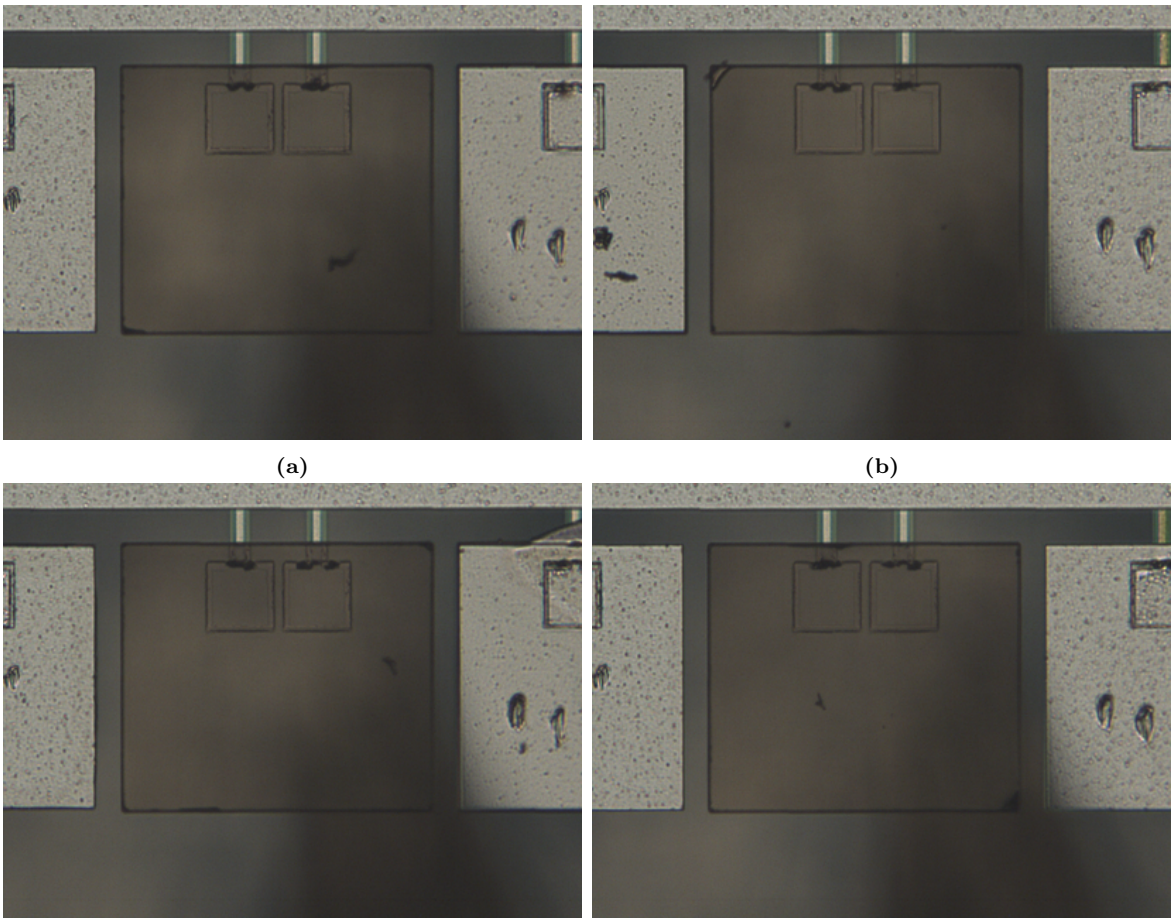
A single value to measure the difference in capacitance between 0 V to $\pm$ 50 V, $C_{(0\,\text{V}\to\pm50\,\text{V})}$, and $\pm$50 V to 0 V, $C_{(\pm50\,\text{V}\to0\,\text{V})}$, has been proposed as

$$\frac{\Delta C_{\pm\text{sweep}}}{C_0} = \left(\left| \frac{C_{(0\,\text{V}\to\pm50\,\text{V})} - C_{(\pm50\,\text{V}\to0\,\text{V})}}{C_0} \right| \right) \tag{9.8}$$

$$\Delta C_{\pm\text{hyst}} = \sum^{N_C} \frac{\Delta C_{\pm\text{sweep}}}{C_0} / N_C \tag{9.9}$$

where $\Delta C_{\pm\text{sweep}}/C_0$ is a vector containing the ΔC values for either the positive or negative sweep, normalised by C_0 obtained from that CV curve fit. The value of $\Delta C_{\pm\text{hyst}}$ is calculated as the mean of the vector and is a single dimensionless value for either sweep, measuring how much hysteresis is present in the CV data.
The value of $\Delta C_{\pm\text{hyst}} \times N_C = \sum^{N_C} \frac{\Delta C_{\pm\text{sweep}}}{C_0}$ can be understood as the area between the two curves for either the positive or negative side of the plots.

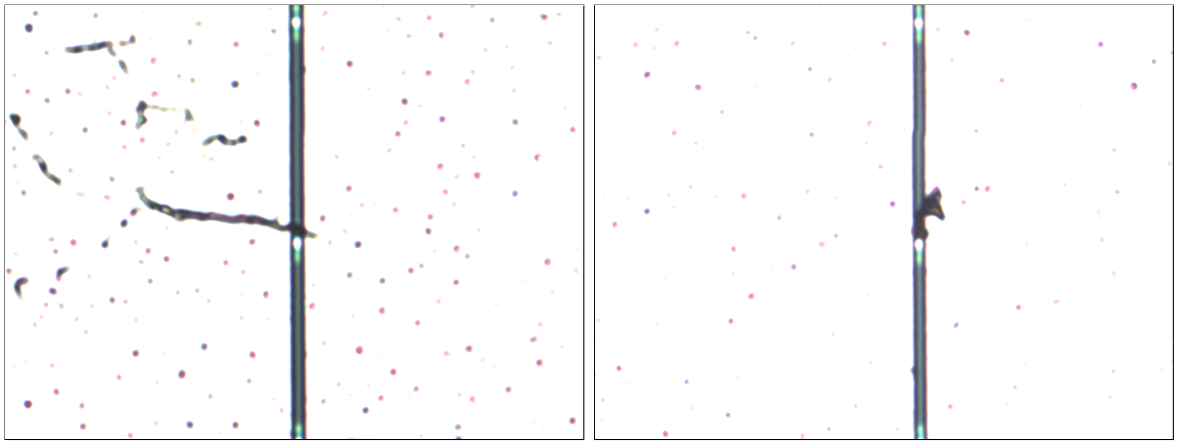
For the two example CV curves in Fig. 9.8, and element E47 from Fig. 9.13, the $\Delta C_{\pm\text{hyst}}$ values are presented in Table 9.2. The values in the table clearly indicate that CV curves can be grouped



(a) **(b)**

(c) **(d)**

Figure 9.6: Four bottom electrode pads with missing aluminium metal: E25, E31, E39 and E49. This is due by a problem during spin-coating of the photoresist layer for the *Top electrode* mask. Incomplete mask coverage causes the IBE and ASE etching processes to remove the contact pads.

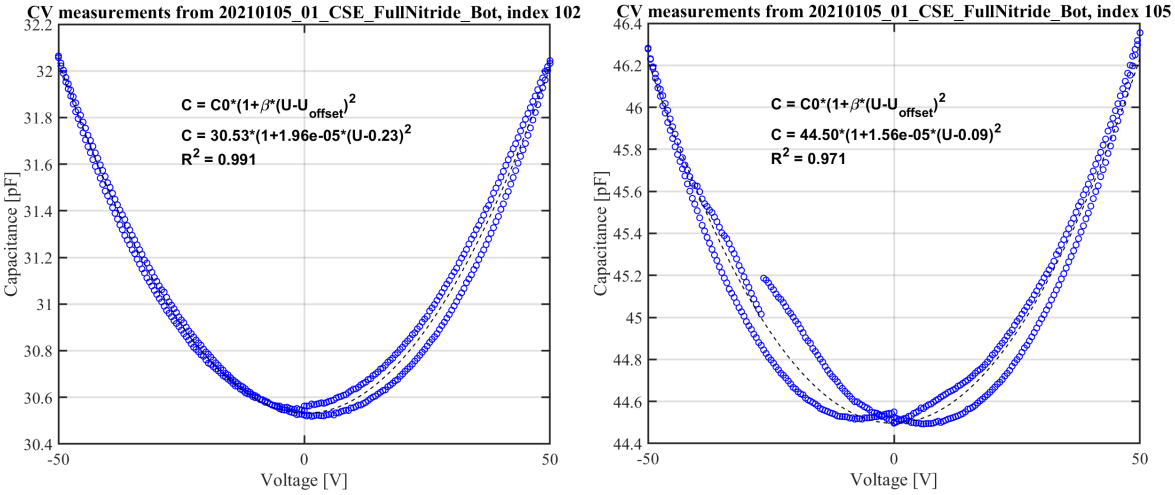


(a) **(b)**

Figure 9.7: Microscope images of particles found on the wafer, which are believed to have acted as masks during the top electrode separation etch and are short-circuiting the two adjacent electrodes. (a) shows a particle strand between the shorted elements E9-E10 and similarly in (b) a particle is found in the kerf between the shorted elements E187-E188.

Table 9.2: Calculated value of $\Delta C_{\pm\text{hyst}}$ from Eq. 9.9, based on the measured discrepancies of the capacitances found in the CV tests performed on elements E102, E105 Fig. 9.8 and E47 Fig. 9.13.

Element-to-element	$\Delta C_{\pm\text{hyst}}$		Hysteresis
	Pos	Neg	
47-48	2.50×10^{-4}	2.15×10^{-4}	No hysteresis
102-103	33.37×10^{-4}	11.38×10^{-4}	Positive sweep hysteresis
105-106	27.43×10^{-4}	35.25×10^{-4}	Both direction sweep hysteresis



(a) (b)

Figure 9.8: Data from CV tests for two bottom electrode neighbour to neighbour measurements. (a) measured between elements E102-E103 show hysteresis most prominently in the positive voltage sweep. This also affects the V_{offset} and is not reflected in the parabolic fit. (b) measured between elements E105-E106 shows hysteresis in both positive and negative voltage sweep, which is also not reflected in the fitted parameters but lowers the R^2 value.

according to their degree of hysteresis, seen e.g. by the increase in $\Delta C_{+\text{hyst}}$ by ≈ 16 times for element E105 compared to E47. A histogram showing the hysteresis, $\Delta C_{\pm\text{hyst}}$, for the bottom electrodes can be seen in Fig. 9.9 and for the top electrodes in Fig. 9.10. A cut-off value of $\Delta C_{\pm\text{hyst}} = 0.95 \times 10^{-3}$ to determine which of the elements have an acceptably low hysteresis was chosen from the data in Fig. 9.9 and in Fig. 9.10. Several groups of elements with different amounts of hysteresis are seen in the figure, and the two group with a value $\leq 0.95 \times 10^{-3}$ were found to have minimal hysteresis. The number of elements with a higher $\Delta C_{\pm\text{hyst}}$ than the cut-off was found to be 54 for the bottom electrodes and 19 for the top electrodes and the data is summarised in Table 9.4, together with the element yield.

The minimum capacitances measured from the CV curves of the top electrodes, in Fig. 9.12, are grouped into four levels as seen in Fig. 9.14b, and the average listed in Table 9.3. The lowest peak in the histogram are elements with capacitances from ≈ 0.1 pF to 5 pF, which are not performing as CMUT capacitors. The next three levels are elements with capacitances at around 31.5 pF, 44.5 pF and 51.7 pF.

Again the values 31.5 pF and 42.3 pF correspond well with a measurement between two neighbours ($\frac{1}{2} C_{0,\text{-apo}}$) and three neighbours with one shorted connection ($\frac{2}{3} C_{0,\text{-apo}}$), respectively. Three or four shorted neighbouring elements ($\frac{4}{5} C_{0,\text{-apo}}$) would give a value of 52.8 pF, which is close to the measured 51.7 pF. Contrary to the bottom elements, most of the higher capacitances are observed adjacent to short-circuited elements and can be explained by Eq. (9.1). Higher values than $C_{0,\text{-apo}}$, even above 100 pF are seen in both plots for the top and bottom electrodes and can not be explained

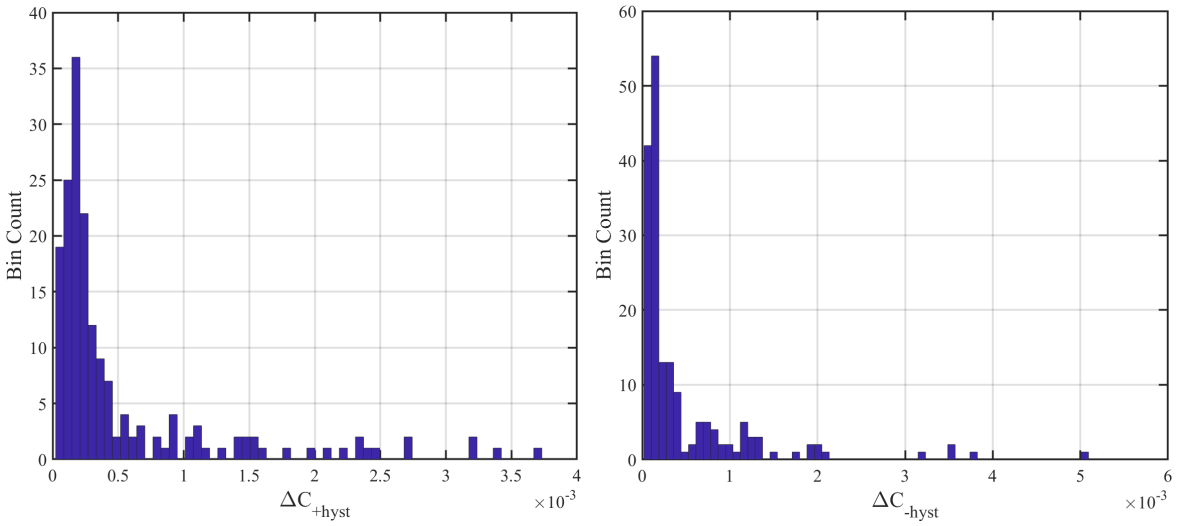


Figure 9.9: Histogram of capacitive hysteresis calculated as $\Delta C_{\pm\text{hyst}}$ from Eq. 9.9. Data is obtained from CV tests for the bottom electrode neighbour to neighbour measurements by sweeping the DC bias ±50 V. (a) depicts the histogram of $\Delta C_{+\text{hyst}}$ for the positive CV sweep from 0 V → 50 V → 0 V. (b) depicts the histogram of $\Delta C_{-\text{hyst}}$ for the negative CV sweep from 0 V → −50 V → 0 V.

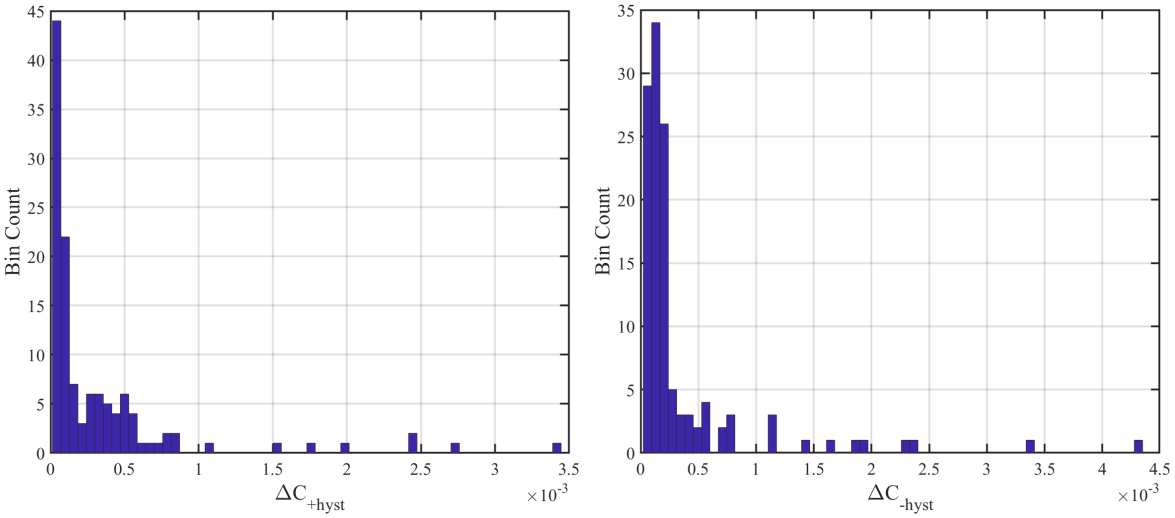
easily by just considering the shorted neighbouring elements. The fitted values of C_0 and V_{offset} are listed in Table 9.3.

The final element yield of the array comes to 64.55 % for the bottom electrodes and 54.50 % for the top electrodes, which is considerably reduced by removing the elements exhibiting hysteresis at the measured bias voltages. Dielectric charging of the CMUT indicated by hysteresis in the CV tests is is an unwanted effect as it can cause stability issues and a reduction in the imaging performance. The method of categorising and excluding elements based on hysteresis and other unwanted phenomena is under development in our group. If the elements with a hysteretic behaviour are not excluded from the number of accepted elements, the yield would be 93 % for the bottom electrodes and 65 % for the top electrodes.

9.1.2 Impedance

Impedance measurements were performed between top and bottom electrodes on 190 long test elements, 16+16 small arrays with frames placed in the north and south section of the wafer, and on short test elements corresponding to elements from the 16+16 arrays. This was done to get an estimate of the pull-in voltage for the TH1-A chip array and to find the resonance frequency close to the operating bias voltage. The bias voltage was varied in the range from 0 V to 100 V in steps of 1 V for the first measurements and then with larger steps of 5 V to 10 V in subsequent tests.

The first set of measurements performed was on a south-eastern 190 long test element in the frequency range from 10 MHz to 30 MHz but plotted in Fig. 9.15 and in Fig. 9.16 from 13 MHz to 20 MHz. The spectra in the two figures show a selected voltage range from 25 V to 50 V and 55 V to 75 V, respectively, to more clearly show the voltage dependent behaviour of the impedance and phase. In Fig. 9.15 it is seen that identifying resonance and anti-resonant peaks in the impedance plot is difficult as multiple peaks are present. This is also reflected in the phase plot underneath. If focus is drawn to the group of peaks at just around 17.3 MHz in both plots, a clear down-shift in the peak frequency and an increase in the peak amplitudes for an increasing applied bias voltage is seen. This is indicative of the spring softening effect observed in CMUTs.



(a) (b)

Figure 9.10: Histogram of capacitive hysteresis calculated as $\Delta C_{\pm\text{hyst}}$ from Eq. 9.9. Data is obtained from CV tests for the top electrode neighbour to neighbour measurements by sweeping the DC bias $\pm 50\,\text{V}$. (a) depicts the histogram of $\Delta C_{+\text{hyst}}$ for the positive CV sweep from $0\,\text{V} \rightarrow 50\,\text{V} \rightarrow 0\,\text{V}$. (b) depicts the histogram of $\Delta C_{-\text{hyst}}$ for the negative CV sweep from $0\,\text{V} \rightarrow -50\,\text{V} \rightarrow 0\,\text{V}$.

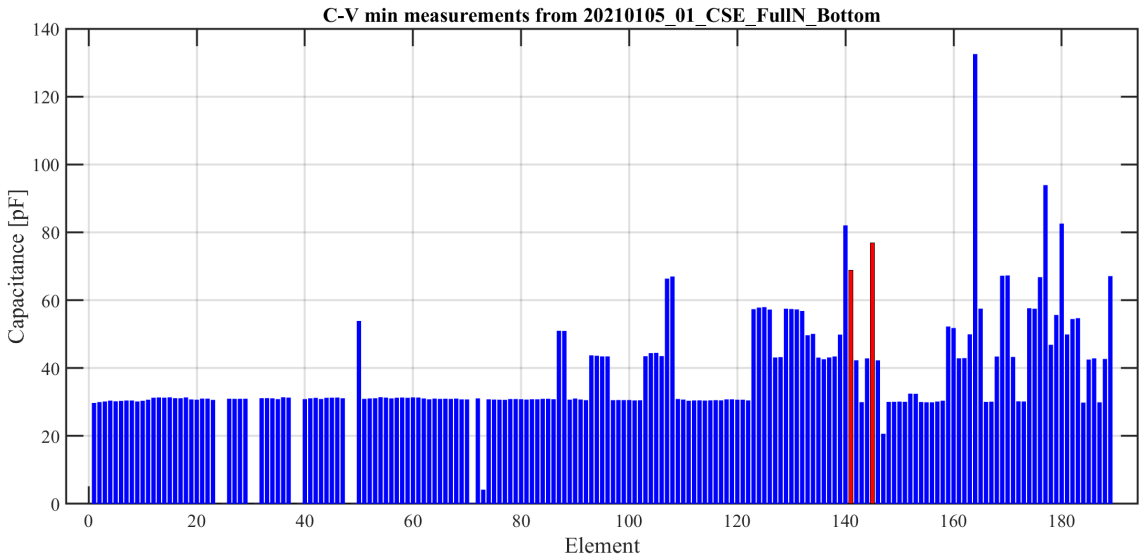


Figure 9.11: The minimum capacitance measured in the bottom electrode CV tests (on the y-axis) for each element (on the x-axis) collected in a bar plot. The short-circuited and missing elements are removed. A large number of the elements have a capacitance close around 31.5 pF, which corresponds well with the predicted capacitance. Groups of elements with higher capacitive values, 44.5 pF and 51.7 pF, placed not only around short-circuited are observed. A few elements exhibit capacitances much higher than the predicted $C_{0,\text{-apo}}$ and can not be explained solely by their neighbouring elements.

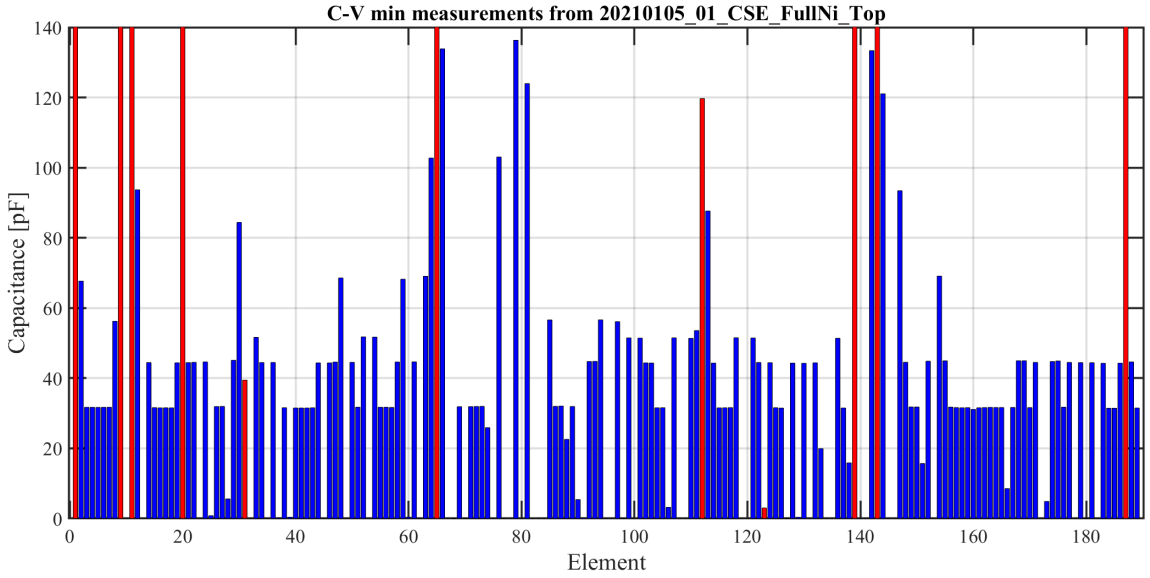


Figure 9.12: The minimum capacitance measured in the top electrode CV tests (on the y-axis) for each element (on the x-axis) collected in a bar plot. The short-circuited and missing elements are removed. A large number of the elements have a capacitance close around 31.5 pF, which corresponds well with the predicted capacitance. Groups of elements with higher capacitive values, 44.5 pF and 51.7 pF, placed not only around short-circuited are observed. A few elements exhibit capacitances much higher than the predicted $C_{0,\text{-apo}}$ and can not be explained solely by their neighbouring elements.

Table 9.3: Measured and fitted values from the IV and CV tests. The measured $I_{\max}$ and $C_{\min}$ and fitted V_{offset} and C_0 are based on the elements, which were non-shorted, with a $R^2 > 0.90$ and a $C > 5\,\text{pF}$. The average $I_{\max}$ is seen to be very high for the bottom electrodes, as some of the elements with a high C_{min} and hysteresis also exhibited a large $I_{\max}$.

Array statistics	Bottom electrode	Top electrode	Unit
Measured parameters			
$I_{\max}$	$7.4 \pm 97.9 \times 10^3$	163.6 ± 626.9	pA
Min $I_{\max}$	8.55	31.10	pF
Max $I_{\max}$	1.3×10^6	136.31	pF
$C_{\min}$	38.53 ± 14.05	46.90 ± 22.93	pF
Min $C_{\min}$	29.73	31.10	pF
Max $C_{\min}$	132.50	136.31	pF
Fitted parameters			
V_{offset}	-0.04 ± 1.45	0.23 ± 0.73	V
C_0	38.52 ± 14.04	46.89 ± 22.92	pF
Min C_0	29.73	31.20	pF
Max C_0	132.48	136.27	pF

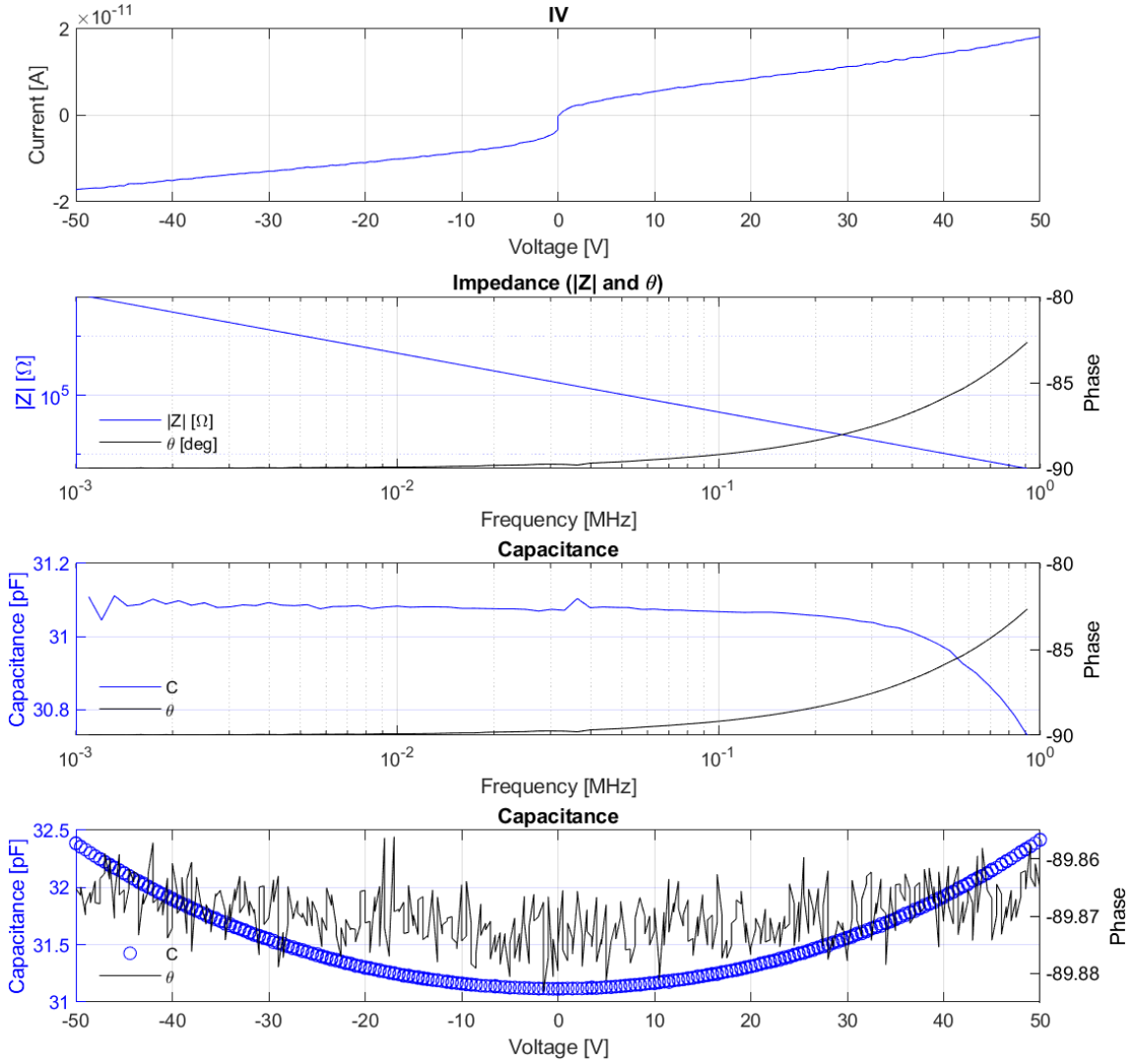
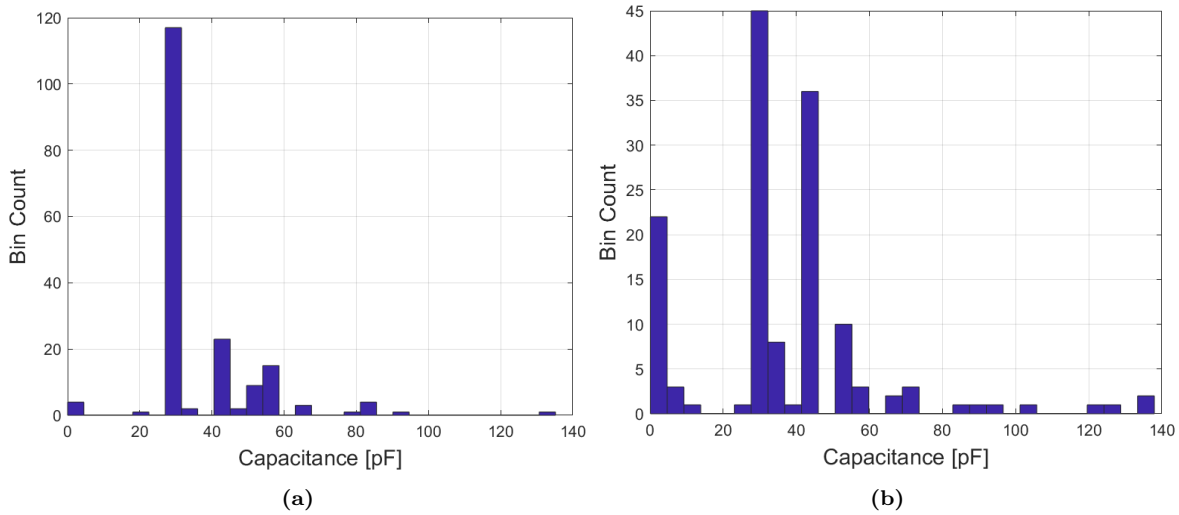


Figure 9.13: Overview of the IV, Z-f, C-f and CV tests performed on the bottom (column) element E47.



(a) **(b)**

Figure 9.14: Histogram of the minimum capacitance measured on the (a) bottom and (b) top electrodes.

Table 9.4: Array statistics from the IV and CV tests showing the total number of accepted elements and the yield. The number of short-circuited and not connected elements, as shown in the previous IV plots, is shown. The remaining elements have been analysed and removed according to the listed criteria. The non-functioning elements are listed, with a low capacitance and a poor CV fit. The elements showing hysteresis in either or in both the positive or negative CV sweep are also grouped. The final yield with and without the removal of the elements showcasing hysteresis is given.

Array statistics	Bottom electrode	Top electrode	Unit
Total accepted	122	103	Elements
Short circuits	2	46	Elements
Not connected (NC)	4	0	Elements
Beside short circuits and NC			
Low C ($C_{\text{min}} < 5\,\text{pF}$)	6	13	Elements
Bad elements ($R^2 < 0.90$)	1	8	Elements
Hysteresis ($\Delta C_{\pm\text{hyst}} > 0.95 \times 10^{-3}$)	54	19	Elements
Yield	93.12	64.58	%
Yield including elements w. hysteresis	64.55	54.50	%

From the previous CV measurements it was estimated that pull-in would occur around 65 V DC. In Fig. 9.16 in the impedance plot, a large frequency shift occurs for the peak initially located at 16.5 MHz to 15.5 MHz, when the bias is changed from 55 V through 65 V to 70 V. This typically indicates that the bias voltage is near pull-in voltage of the CMUTs. At 75 V bias the peak shifts up again in frequency to the same position as when biased at 65 V. Further increasing the bias to 100 V decreases the peak amplitude and does not further shift it downwards in frequency. The is likely due a hysteretic charging effect in the CMUT capacitors, which was also illustrated in the CV plots in Fig. 9.8. The measured center frequency at the estimated 50 V (80 % $V_{\text{pull-in}}$) bias was 16 MHz to 17 MHz which is about 4 MHz to 5 MHz, lower than the COMSOL simulated value of 21.6 MHz in air. However, this would result the center frequency in immersion to be ≈8 MHz.

The precise mechanisms of dielectric charging in CMUTs are still not fully understood in the field [73] but is topic for further research. However, if we assume the effect to be coupled with the presence of movable charges in the dielectric layers of the CMUT, electric fields opposing the bias fields are set up inside the device. This can prevent the devices from reaching pull-in at the expected $V_{\text{pull-in}}$ voltage. Compared to the clear indication of pull-in observed in the impedance plots of the TR2 CMUT chips, in Fig. 6.3, a definite pull-in voltage was not measured on the TH1-A chip or its test elements.

9.1.3 Long term stability

Long term assessment of the stability of the CMUT elements was also performed. The setup described in Chapter 3 with the Agilent E4990A impedance analyser and Keithley 2410 Sourcemeter was utilised and controlled by a GUI from MATLAB.

The results are shown in Fig. 9.17 and in Fig. 9.18 for a two similarly performing elements, a short 16 test element and an element from a 16+16 array with a *bottom frame*, respectively. In Fig. 9.17 the test element is supplied with a ±100 V to demonstrate the unstable performance well-above the estimated pull-in at 65 V to 70 V. Each voltage step is held for 10 min and the peak phase angle and fitted slope capacitance, found from the impedance magnitude, are decreasing rapidly over the course of each bias cycle. It is observed that a slightly larger drop in phase and capacitance occurs for the positive bias, and that a remnant bias is present at the 0 V steps. These effects can likely be explained by the surmised charging (or de-charging) phenomenon, which also causes the hysteretic behaviour of some of the CV tests and prevents the CMUTs from properly reaching pull-in collapse.

In Fig. 9.18 the element from the 16+16 array was supplied with a ±50 V. Contrary to Fig. 9.17,

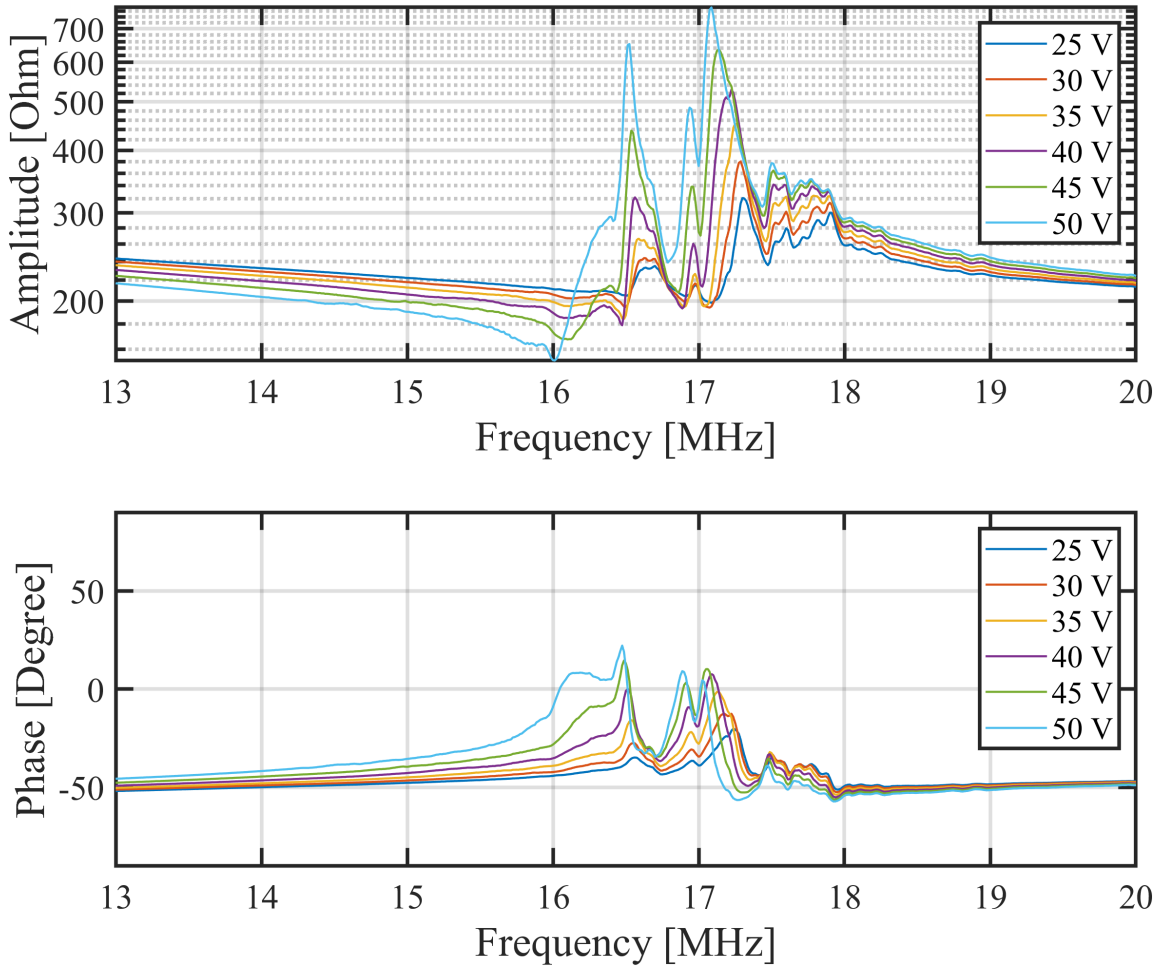


Figure 9.15: Impedance measurements of a long CMUT element corresponding to an element of the 190+190 RCA array. The impedance has been measured with a DC bias from 25 V to 50 V and a 50 mV AC. This demonstrates the CMUT element far from pull-in and at ≈80 % $V_{\text{pull-in}}$ at 50 V.

this element shows a very stable performance for each bias step held for 60 min. A slight difference in peak phase and slope capacitance is observed between the positive and negative bias, and no remnant bias is seen in the 0 V step. This demonstrates that operating the arrays at a bias of ±50 V will result in a stable pressure output.

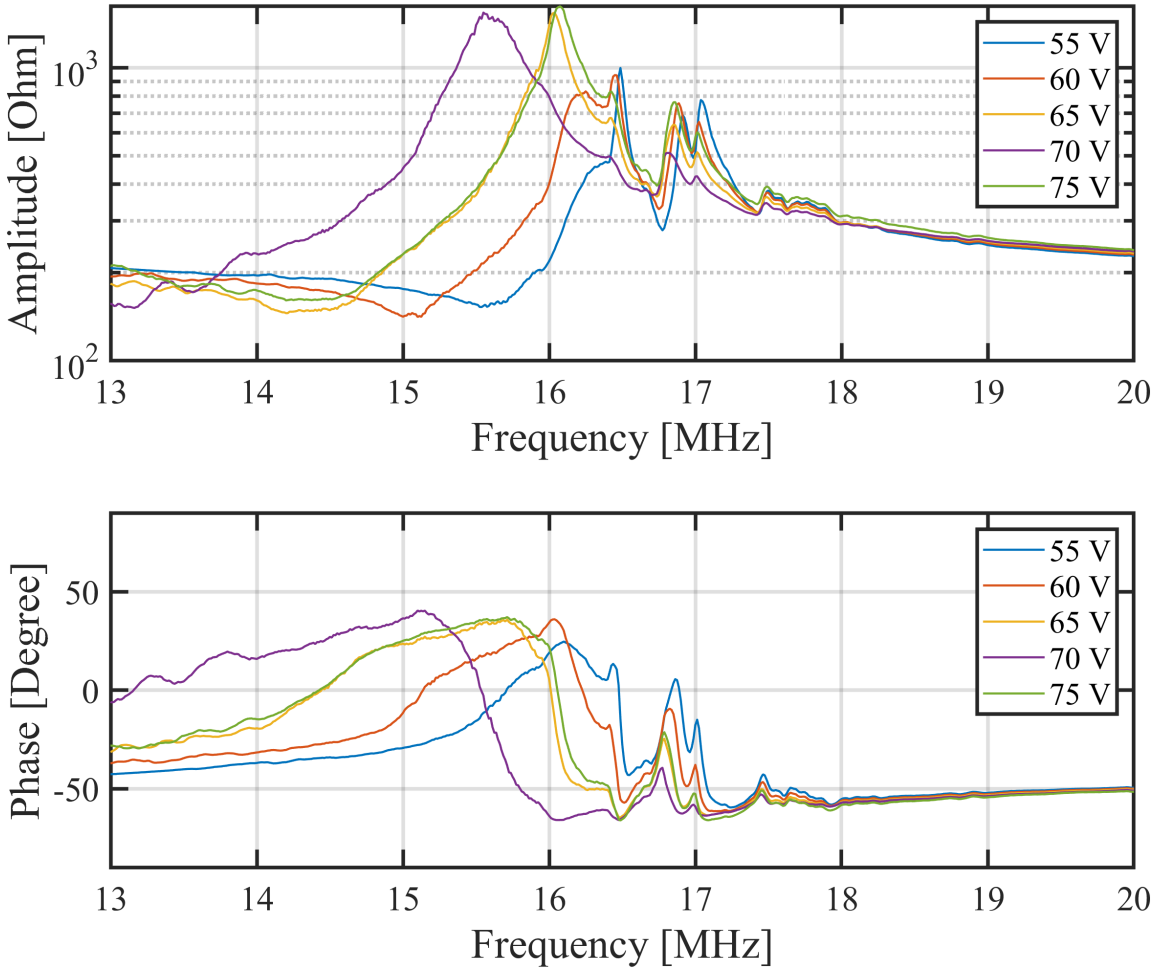


Figure 9.16: Impedance measurements of a long CMUT element corresponding to an element of the 190+190 RCA array. The impedance has been measured with a DC bias from 55 V to 75 V and a 50 mV AC. This demonstrates the CMUT element close to pull-in, estimated to be close to at 65 V. No clear indication of pull-in is seen, as the impedance amplitude peaks and phase angle peaks do not shift further down in frequency when the DC bias voltage is increased above 70 V.

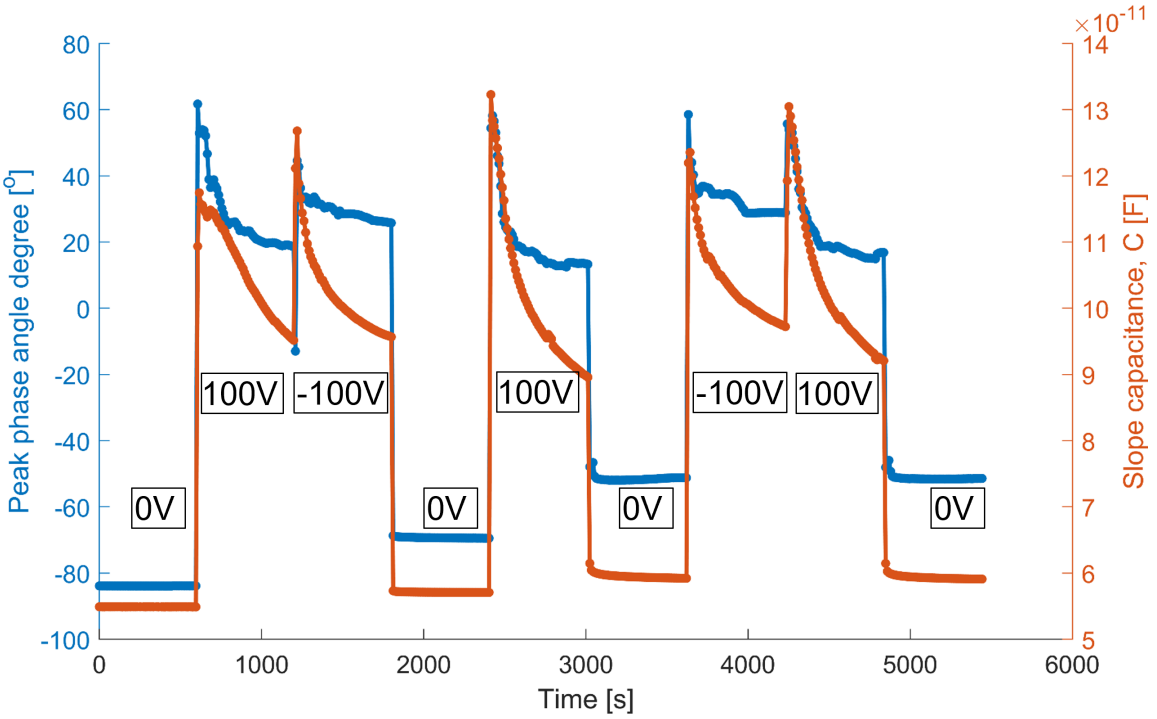


Figure 9.17: Stability measurement performed on a short 16 test element using the Agilent E4990A impedance analyser. The figure shows the peak phase angle in ° and the slope capacitance as a function of time at different bias voltages from −100 V to 100 V. A clear decay of both values are seen for each of the 10 min steps.

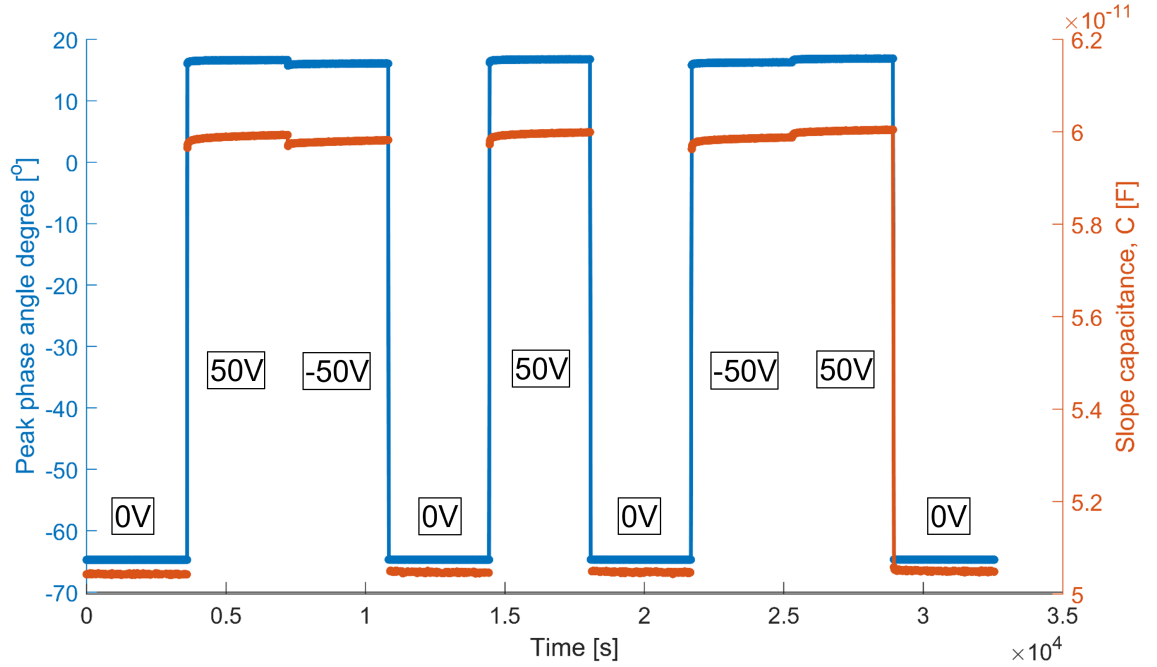


Figure 9.18: Stability measurement performed on an element from a 16+16 array with a *bottom frame* using the Agilent E4990A impedance analyser. The figure shows the peak phase angle in ° and the slope capacitance as a function of time at different bias voltages from −50 V to 50 V. Stable values are seen throughout the 60 min steps.

9.2 Probe Assembly

The author of this thesis has not participated in the assembly of the probe housing the TH1-A chip, and has only to a small degree been involved in the design and development of the probe. However, in preparation for the assembly of newer generations of chips, such as the TH1-B chip, the author has gone through all of the following steps using dummy chips. The following section will therefore give brief overview of the steps involved, where further details are given included when available. The mounting and wire bonding was performed at TPT Wire Bonder GmbH & Co KG (Munich, Germany). The design and process development for assembly of the acoustic stack for the nose piece was done by Ph.D. student Kasper Fløng Pedersen that also assembled the nose piece containing the TH1-A chip. For completeness and to allow the reader to fully understand how the probe is assembled, results from the assembly are presented with permission from Kasper Fløng Pedersen as much of this is unpublished at the time of writing.

9.2.1 Prototype Probe

The probe is a modular probe for rapid prototyping of ultrasonic CMUT arrays. It was developed in a collaboration between our research group and BK Medical (Herlev, Denmark) and presented in [130] by Kasper Fløng Pedersen. It is also designed with the purpose of being used for human clinical scans using the human transducer 1 (TH1) generation of chips as the transducer arrays. The approval of the probe for clinical trials requires that the probe adheres to a list of medical compliances. These can be e.g. standards regarding general safety of electromedical devices (DS/EN 60601-1:2006) and thermal safety under test (DS/EN 60601-2-37), which will not be treated in this PhD report. A thermal characterisation test of the probe was planned but not performed.

The modular aspect of the probe comes from the ability to freely interchange self-contained nose pieces and to take apart the probe body for inspection of the electronics. The nose piece contains the encapsulated chip mounted on a PCB and is simply connected to the main body with four connectors and screws, forming a water-tight seal for measurements in immersion.

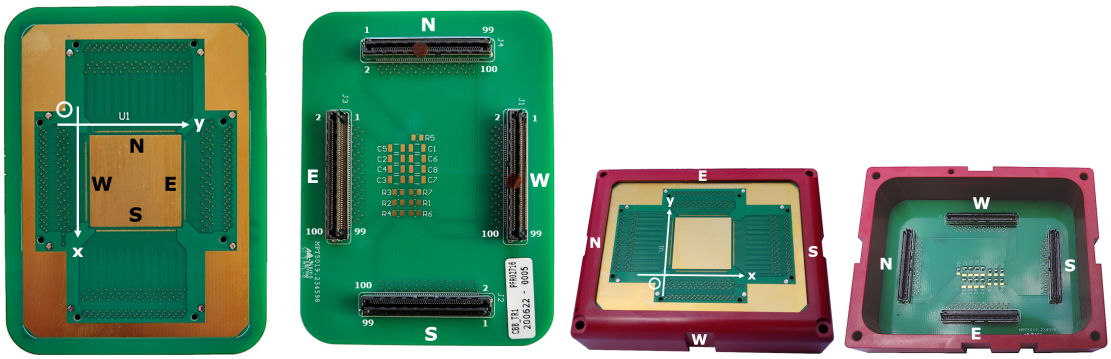
An overview of the components of the prototype probe is shown in Fig. 9.19 and in Fig. 9.20. In Fig. 9.19a and Fig. 9.19b is shown the PCB chip carrier board (CCB) which the chip will be glued and mounted to. The CCB is glued to a medical grade PPSU-polymer milled nose piece frame, seen in Fig. 9.19c and Fig. 9.19d. The CCB has a metal center square pad used for bonding the chip with an area of 2.94 mm × 2.94 mm. The bonding pads lining each side of the chip area has a pitch of 190 µm, which limits the chip designs to an element pitch of 95 µm.

The finished nose piece (shown here without encapsulating silicone layers) is connected to the main body. This consists of the four preamplifier boards of the same type as used for the TR2 probe (and originally for the Tabla-V probe), fixed to a 3D-printed PCB-carrier, seen in Fig. 9.20a. The PCB-carrier is connected to the interposer PCBin the cassette, Fig. 9.19b, inserted into a PPSU-polymer milled body and connected to the nose with a water-tight seal, see Fig. 9.19d. Further details pertaining to the design can be found in [130].

9.2.2 Chip mounting and wire bonding

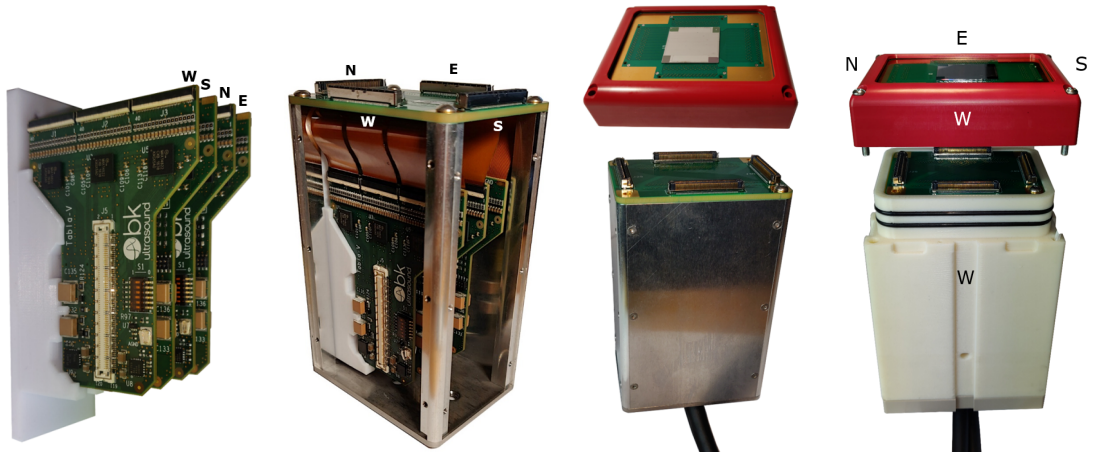
When the chip has been electrically characterised on wafer level, using the semi-automatic probe station, the arrays are diced into chips on the DISCO saw mentioned in Chapter 8. Even though the TH1-A chip was not mounted and glued to the CCB in our laboratory, this method will be briefly shown below.

The first step is soldering a PCB electromagnetic interference (EMI) frame to the CCB for contacting the EMI shield mounted in a later step. The CCB is then mounted in a Metcal rework station and thermocouples connected to the station is taped to the front and backside of the board. The chip is then placed on the CCB, aligned with the center metal square and picked up with a vacuum suction cup. A stencil with 0.2 mm holes in a square grid is placed on the center square on the CCB and



(a) (b) (c) (d)

Figure 9.19: Photos [130] of:(a) Chip carrier board (CCB) and (b) CCB underside. (c) CCB in nose piece. (d) Backside of nose piece.

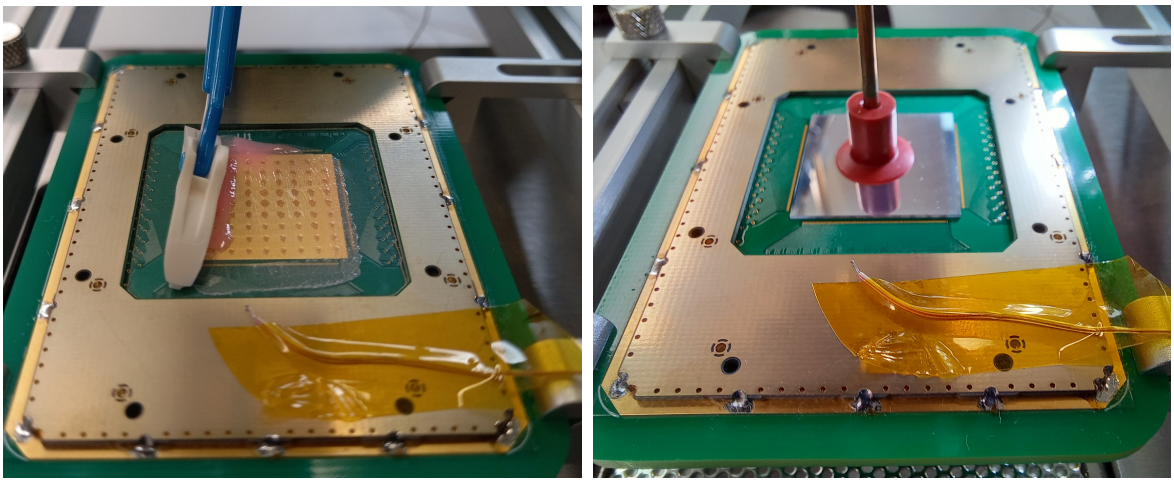


(a) (b) (c) (d)

Figure 9.20: Photos [130] of: (a) PCB-carrier and (b) probe electronics. (c) Casette and nose piece. (d) Body and nose piece.

a thermal curable adhesive, Structalit 5605 (Panacol), is applied through the stencil mask with a scraper or squeegee tool, as demonstrated in Fig. 9.21a. The chip is then lowered onto the the board and the glue is cured at 105 °C for 50 min, see Fig. 9.21b.

With the chip securely mounted, the CCB can be sent to TPT for wire bonding. As mentioned, both the mounting and wire bonding was performed at TPT Wire Bonder. The glued and wire bonded chip can be seen in Fig. 9.22 and Fig. 9.23. As seen in Fig. 9.23b there might be potential reliability problems with some of the wire bonds as they are off center of the bonding, some wires are tilting to either side, and some damage to the electrodes occurred during bonding. Our MEMS research lab is also equipped with a TPT HB100 wire bonder, which had not been acquired at the time of probe assembly for the TH1-A chip. This semi-automatic wire bonder is fully capable of wire bonding all of the 384 contact pads (including the apodization contacts) within 20 min to 60 min, when wafer maps have been created. This will enable us to fully integrate the chips fabricated in the DTU Nanolab cleanroom into probes at our own facilities and perform electrical and acoustical characterisation.



(a) **(b)**

Figure 9.21: (a) Applying glue and (b) gluing the chip at an elevated temperature of 105 °C.

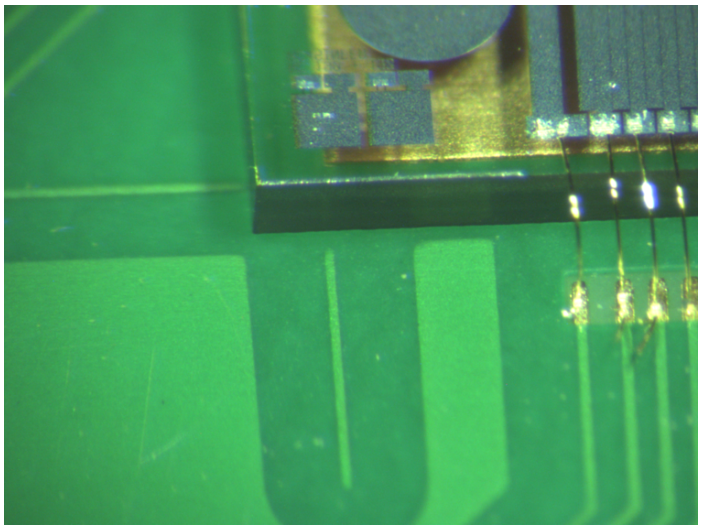
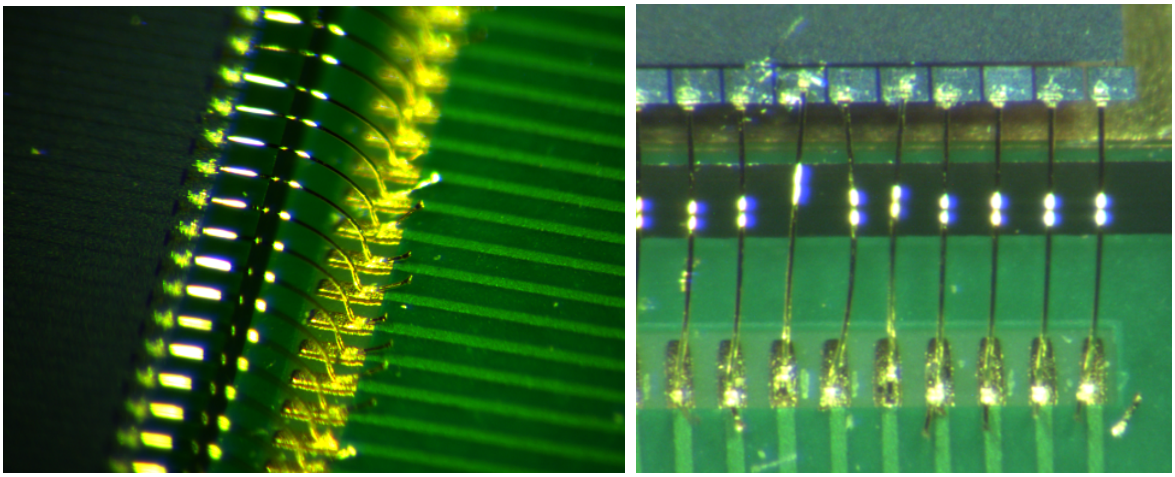


Figure 9.22: The north-west corner of the TH1-A chip showing the alignment to the CCB and the first few wire bonds to the apodization and the row element contact pads.



(a) (b)

Figure 9.23: Microscope images showing wire bonds (a) to the top electrode contact pads (rows) and (b) to the bottom electrode contact pads (columns).

9.2.3 Encapsulation and shielding

The chip and wire bonds will just like the TR2 probe be encapsulated in a silicone elastomer suited for medical use. This will protect the array from mechanical damage and ensure patient safety during high voltage use.

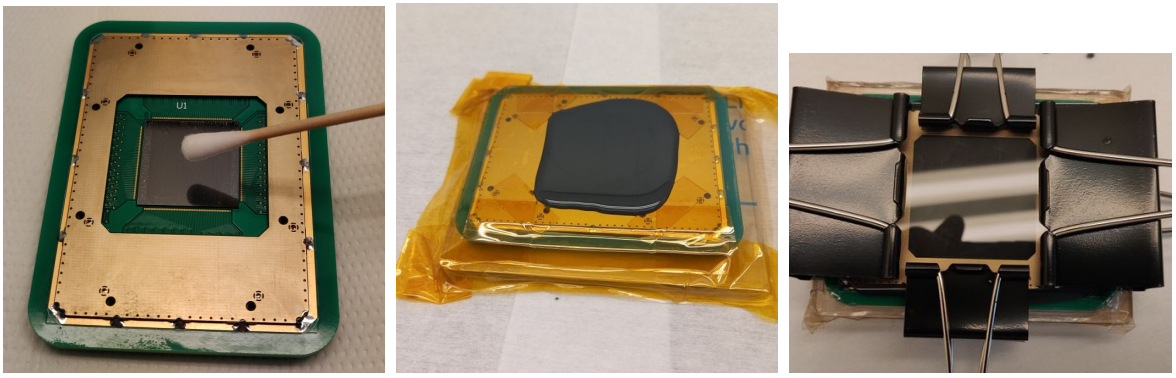
In preparation the CCB is covered in Kapton or TPFE tape exposing the center of the frame with the chip. The center is cleaned with IPA and a Dowsil 1200 primer (The Dow Chemical Company, USA) is applied for better adhesion to the following silicone and it is then cured under high humidity, see Fig. 9.24a.

The 2-part polydimethylsiloxane (PDMS) silicone polymer, a SYLGARD-170 Silicone Elastomer (The Dow Chemical Company, USA), is mixed in equal parts per volume and the mixture centrifuged in a container taken from a freezer. In Fig. 9.24b the PDMS is then poured into the frame and overfilled and the CCB is degassed in a vacuum chamber for 5 min to 10 min to remove air bubbles, which would otherwise be detrimental during acoustic imaging. The PDMS also ensures good acoustical matching from the CMUT to the scanned medium. The PDMS is planarized with a thick PMMA acrylic sheet held in place with clamps, demonstrated in Fig. 9.24c, and the polymer is cured overnight 45 °C approximately 12 hours.

After removing the PMMA and excess PDMS from the frame, a new Kapton tape mask is applied which exposes part of the frame around the center, see Fig. 9.25a. The primer is applied over the cured PDMS and frame and it itself is cured. Afterwards the mask is removed. A new batch of PDMS is mixed and a small amount poured on top of the frame to serve as a binder to the EMI shield, see Fig. 9.25b, which is an aluminised polymer film (12.5 µm polypropylene with a sub-micron thick aluminium layer) of the same type as used for the TR2 probe. The film sold as Torayfan PC3 (Toray Plastics (America), Inc., North Kingstown, USA). This film is applied carefully to avoid wrinkles or bubble entrapment and the layer is planarized again with the PMMA sheet and cured at 45 °C, see Fig. 9.25c.

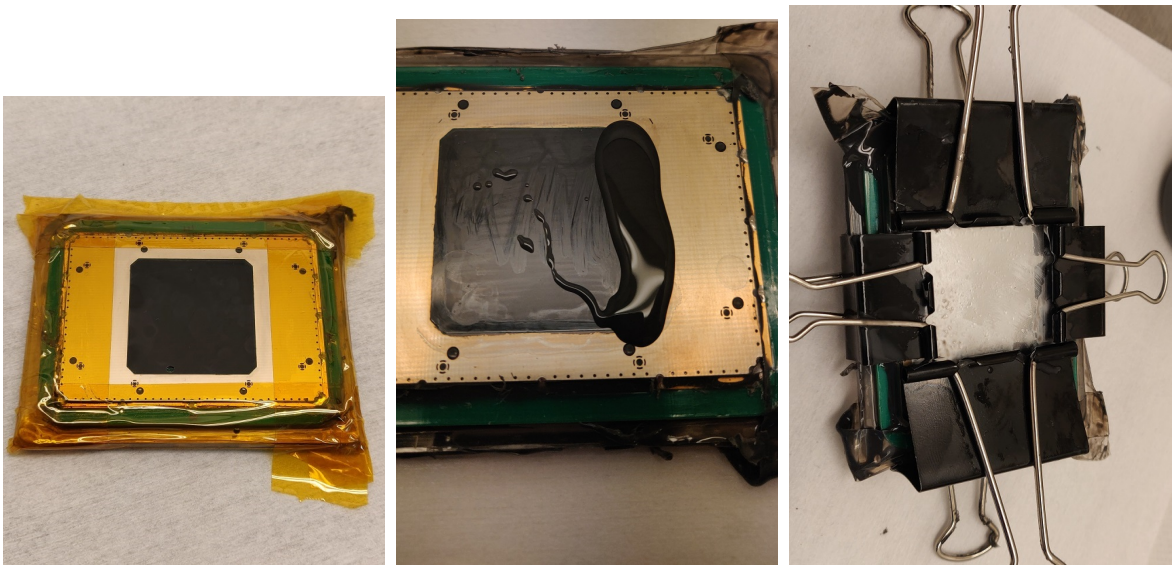
After the curing process the CCB frame is cleaned using IPA the EMI shielding film is cut to a square shape with a scalpel, see Fig. 9.26a. An electrically conductive adhesive, Loctite 3863 (Loctite, USA) is applied to the film and the frame in Fig. 9.26b to ensure electrical contact to the grounding plane.

The CCB is now ready to be mounted in the red-coloured 3D milled PPSU plastic shell from Fig. 9.19c. The protruding lip on the inside of the frame is abraded and a Loctite 480 glue is



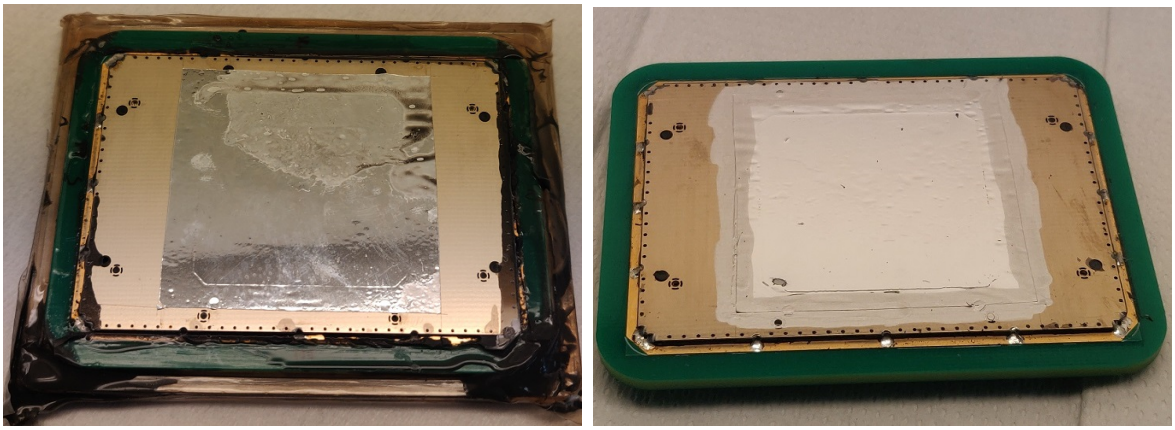
(a) **(b)** **(c)**

Figure 9.24: (a) First PDMS priming inside the frame and (b) PDMS pouring with overfill. (c) PDMS layer planarizing with a PMMA sheet held in place with clamps.



(a) **(b)** **(c)**

Figure 9.25: (a) Masking with Kapton tape and applying primer for EMI shield PDMS layer. (b) Pouring PDMS for adhesion of the EMI shield to the first layer of cast PDMS. (c) Attaching and planarizing the EMI shield with a PMMA sheet.



(a) **(b)**

Figure 9.26: (a) Cutting the EMI shield to size and (b) gluing it to the frame with conducting glue (illustrated here with an Al film instead of the Torayfan PC3 film).

applied, seen in Fig. 9.27a. The CCB is then quickly inserted before the glue is cured. Additional PMMA fixture plates are inserted on the backside of the CCB in the PPSU shell to apply pressure while gluing. Additional glue is applied along the edge of the shell on the front-side as a preventive measure against water ingress during ultrasonic scans in immersion.

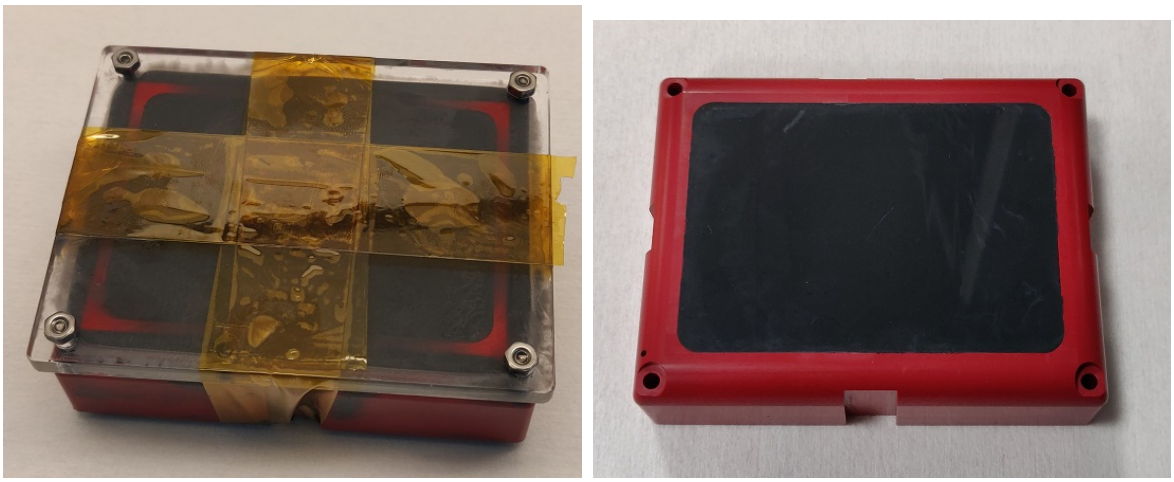
The last steps involve priming of the surface and pouring the final PDMS layer. First the PPSU plastic nose piece is masked with Kapton tape and a bowl-shaped dam is then made from Kapton tape to prevent spillage of silicone during pouring, shown in Fig. 9.27b. The open backside of the CCB is also covered in tape. Primer is then applied on every surface inside the front part of the PPSU frame. Another batch of PDMS silicone is mixed and poured, overflowing the cavity, and subsequently degassed in a vacuum chamber. The dam of Kapton tape is carefully removed and the PDMS is planarized with a PMMA sheet held down with four screws through the plastic frame, demonstrated in Fig. 9.28a. To prevent warping of the clamped PMMA sheet during, the whole nose piece is wrapped tightly in tape. It is then cured at 45 °C for 12 hours and the PMMA sheet removed. After cleaning up the plastic with IPA and removing excess polymer from front and backside, the nose is completed and can be seen in Fig. 9.28b.

9.2.4 Electronics

The four preamplifier boards used in the prototype probe, seen in Fig. 9.20a, is the same boards supplied for the TR2 probe. They are labelled *Tabla-V* and developed by BK Medical. Each board is equipped with six MAX14822 16-channel high voltage (HV)-protected low noise operational amplifier ICs with a bandwidth of 45 MHz. They have support for 96 channels adding up to a total of 384 channels, which supports the 380 elements and 4 apodization regions in total. As was shown in Fig. 9.20a, the boards are held securely by a 3D-printed PCB carrier, connected pairwise with on-board connectors. In Fig. 9.29 the interposer board is shown. The backside of this, shown in Fig. 9.29b, has 12 sockets for connecting three flex cables from each board to the corresponding N, S, W, E connectors on the front side.
The self-contained shielded cassette and probe body was seen in Fig. 9.20, with the attached odd and even coaxial scanner cables from BK Medical. The cassette backside has integrated inlet and outlet tube fittings for attaching cooling hoses.

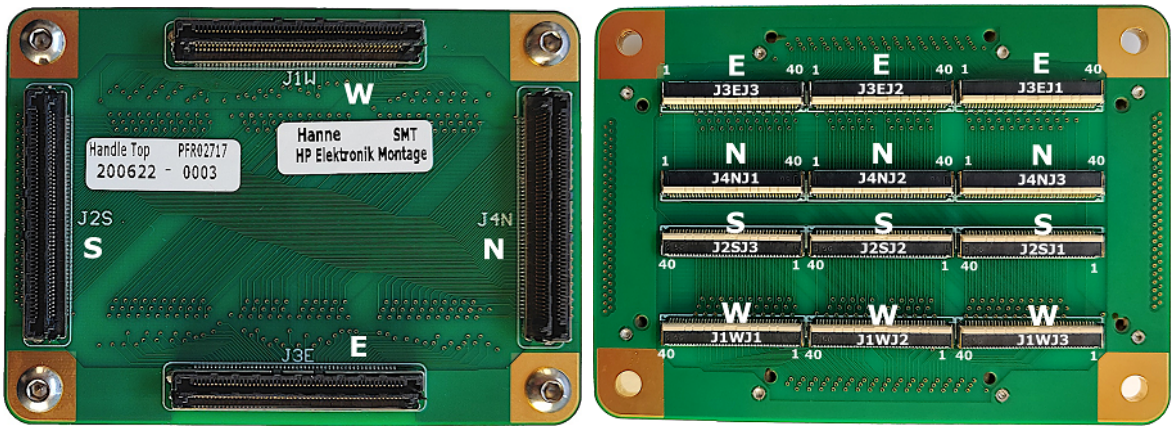
(a) **(b)**

Figure 9.27: (a) Applying glue to the inside rim of the PPSU frame. (b) Inserting and gluing the CCB to the PPSU frame and forming Kapton tape dam for PDMS casting (illustrated here with an Al film as EMI shield instead of the Torayfan PC3 film).



(a) **(b)**

Figure 9.28: (a) Pouring and planarizing the final PDMS layer. (b) Finished nose piece after cleaning.



(a) **(b)**

Figure 9.29: (a) Interposer board seen from the front with sockets for connecting the the CCB and (b) the same board seen from the back with sockets for connecting flex cables to the TABLA V preamplifier boards.

9.3 Acoustic Characterisation

The prototype probe with the attached nose piece containing the TH1-A chip was acoustically characterised at the CFU at DTU. The exact same research SARUS scanner used during characterisation of the TR2 probe in Chapter 6, was also used to perform a series of experiments to evaluate the performance of the probe. All of the measurements were performed in immersion in a water-filled tank controlled by the AIMS stage capable of translating the probes in an x-y-z coordinate system.

The characterisation of the prototype probe will in this chapter be based on the following conducted experiments:

- A hydrophone will be submerged in deionised (DI) water and used as a receiver to perform one-way impulse transmission measurements.
- A PMMA reflector plate is placed in the water 30 mm from the transducer surface to perform two-way pulse-echo receive measurements.
- The hydrophone is used to generate pressure maps of the transmitting elements by scanning in a plane in front of and parallel to the probe surface.

The prototype probe, as the name implies, is meant for rapid prototyping of CMUT based row-column, or linear, arrays fabricated at the cleanroom facilities at DTU Nanolab to reduce turn-around time. It is also designed with the purpose of ultrasonic scanning of humans. This will be realised in the immediate future when more extensive testing of the electronics and performance has been conducted. Contrary to the TR2 probe there has not yet been performed any thermal characterisation of the prototype probe yet in accordance with the DS/EN 60601-2-37 standard [124]. This is also necessary before the probe can be used for clinical test. The initial thermal and electrical tests were planned but unfortunately other scheduled measurements were delayed, and the author did not have the time to perform the tests before the hand-in date of this PhD thesis.

The first two experiment types are presented in the following Section 9.3.1, and the last in Section 9.3.3. In Section 9.3.1, first a presentation of the results for the probe measured in transmit and in pulse-echo is given and then a discussion for each of the two.

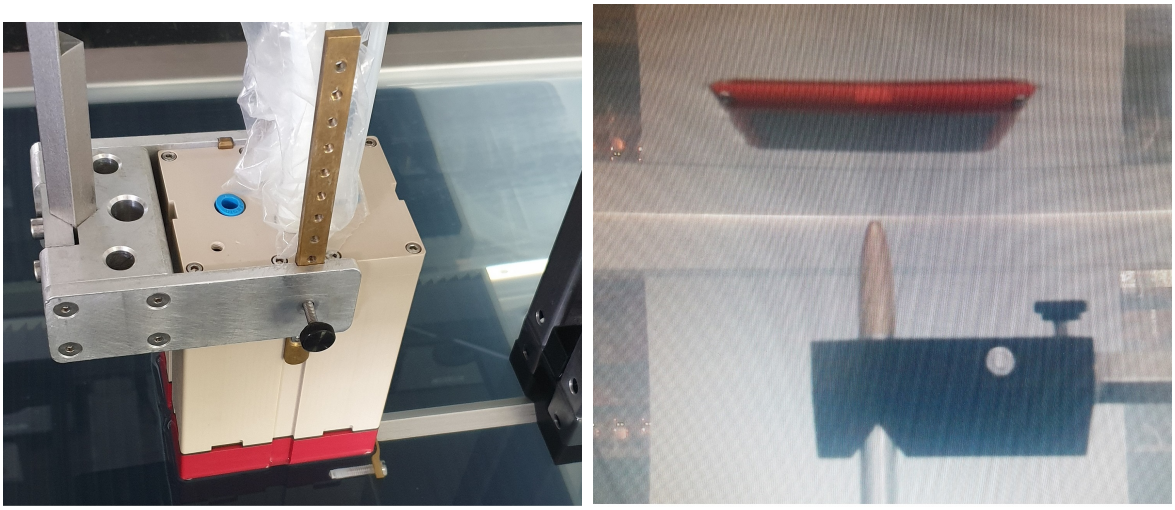
9.3.1 Impulse response

Both transmitting and receiving was done with one element at a time for all rows and columns, respectively. The DC bias to the probe was set to 50 V (±25 V) using two power supplies and the AC excitation voltage set to 80 V peak-to-peak (±40 V). Due to the nature of the amplifiers used in SARUS if the excitation voltage is below ±15 V it is clipped and no voltage is applied. Above ±15 V the amplifiers will ideally perform linearly. The actual AC voltage on the probe is therefore 50 V peak-to-peak (±25 V). The voltage levels were set to reflect the measured pull-in voltage mentioned in Section 9.1.1 and in Section 9.1.2.

Transmit

The impulse response functions measured using the prototype probe for transmitting signals (TX) are acquired using SARUS. The transducer probe has no need for a formfitting adapter to be mounted to the fixed arm connected to the Onda AIMS system, illustrated back in Fig. 6.16. Instead brass rails are used to fix it to the arm, as seen in Fig. 9.30a. The Onda HGL-0400 hydrophone connected to an Onda AH-2010 amplifier is attached to the movable arm and submerged in the water tank. The probe is lowered so the transducer surface is just below the water surface and the probe is manually centred using cameras attached to the tank, see Fig. 9.30b.

For this prototype probe, the excitation will be the same coded stochastic white noise signal as was used for the characterisation of the TR2 probe, though instead at ±40 V. The signal is recorded by the hydrophone and decoded to find the transmit impulse response.



(a) **(b)**

Figure 9.30: Photos of the acoustic measuring setup. (a) The prototype probe mounted to the AIMS III probe fixture with brass rails. (b) The hydrophone used during transmission measurements. This is mounted to a holder capable of moving in an x-y-z coordinate system.

The results from the averaged impulse response functions measured in transmit can be seen in Fig. 9.31 for the rows and columns, where the x-axis shows a cropped section view of the much larger recorded time signal and a 1 µs window is shown for illustrative purpose. The y-axis is in the units $\mathrm{Pa\,V^{-1}\,s^{-2}}$, as explained in [120], [122], where the area and distance to the hydrophone is factored out to measure the relative impulse response or sensitivity. The averaged responses have been found by cross-correlating and averaging all of the signal from the rows and columns separately to a reference row and column element with a large response. This is typically the middle element. They are plotted together with their envelopes, normalised to the peak amplitude of the averaged signals.

The measured impulse response functions for each element has been analysed and grouped in the histograms shown in Fig. 9.32 according to the the peak impulse amplitude. The impulse amplitude data on each plot can be seen to be grouped into three categories for which the cut-off value for each group is chosen heuristically. The elements which a peak impulse response value or sensitivity above $> 6.94 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the rows and $> 5.18 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the columns are designated good or functional elements, which amount 127 rows and 128 columns, respectively. The elements with a peak sensitivity in the range from $3.98 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ to $6.94 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (rows) and in the range from $2.96 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ to $5.18 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ are less good semi-functional elements, which amount to 32 rows and 5 columns, respectively. The number of bad or not connected elements with a peak sensitivity below $2.96 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (rows) and $3.98 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ are 31 rows and 57 columns. The number of elements in each category and the yield are listed in Table 9.5.

The spectra of the averaged impulse responses have also been calculated by truncating the data around the pulse and using fast Fourier transform (FFT) and plotted in Fig. 9.33. This y-axis in dB has been normalised to the maximum impulse response values $4.99 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the rows and $2.6 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the columns.

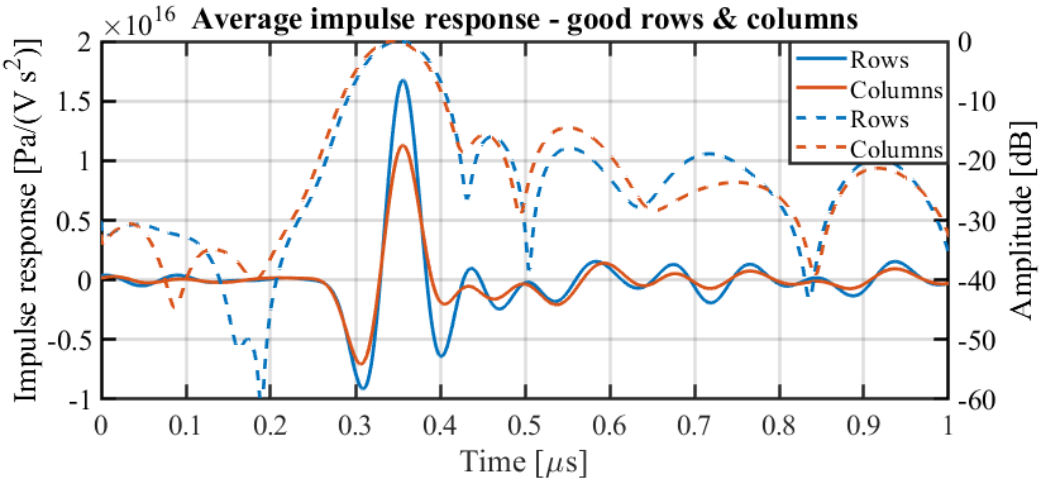


Figure 9.31: Average transmit impulse response in transmit (TX), as solid lines, and the normalised envelope (in dB), as dashed lines, of the functional row and column elements with amplitudes above $6.94 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for rows and above $5.18 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for columns.

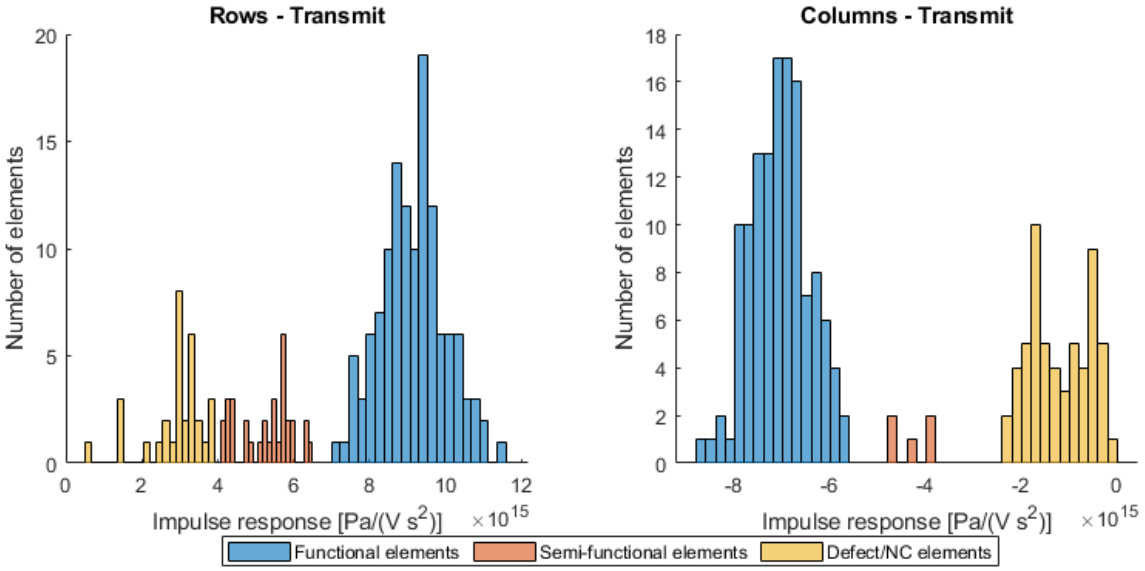


Figure 9.32: Histogram of the maximum impulse response values for all the rows and columns in transmit. These are grouped into three categories depending on their maximum impulse response values.

Table 9.5: Overview of the transmit yield and associated impulse response amplitude cut-off values for each of the three element categories; functional, semi-functional and bad/NC.

Element category	Cut-off value $[\mathrm{Pa\,V^{-1}\,s^{-2}}]/10^{15}$		Amount (% yield of 190)		Total yield (of 380)
	Rows	Columns	Rows	Columns	
Functional	>6.94	>5.18	127 (66.8%)	128 (67.4%)	(67.11%)
Semi-functional	3.98<i<6.94	2.96<i<5.18	32 (16.8%)	5 (2.6%)	9.7%
Bad/NC	<3.98	<2.96	31 (16.3%)	57 (30%)	23.2%

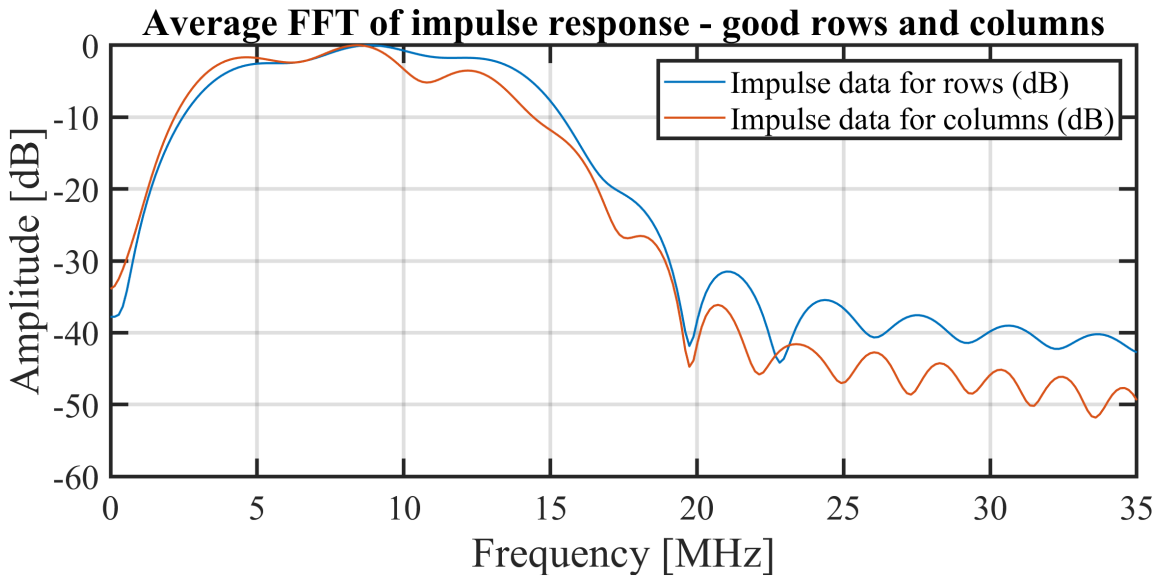


Figure 9.33: Average FFT spectra of the impulse response in transmit (TX) of the functional row and column elements with impulse response amplitudes above $6.94 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the rows and $5.18 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the columns. The spectra for the rows and columns are normalised to the maximum of the average impulse responses with the values $4.99 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $2.6 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$, respectively.

Pulse-echo

For measuring the impulse response of the transducer in pulse-echo (PE) a PMMA reflector plate was placed with a distance of 30 mm from the transducer surface. This is see in Fig. 9.34. This distance is measured and adjusted by inspecting the pulse-echo signal of selected elements of the probe. The same coded excitation signal used in the transmit measurements is repeated here.

The measured pulse-echo impulse response functions are aligned and averaged, and their plots are shown in Fig. 9.35 together with the envelopes dB. The y-axis is expressed in the units $\mathrm{V\,V^{-1}}$ as the value recorded by the transducer probe is relative to the amplitude of the transmitted pulse. The averaged response of the row elements is seen to significantly reduced compared to the response of the columns.

The elements are also for the pulse-echo measurements grouped according to their peak receive sensitivity values in $\mathrm{V\,V^{-1}}$, as seen in Fig. 9.36. It is here more difficult, compared to the TX results, to determine what cut-off threshold value for each element category should be as the elements take a wide range of sensitivity values. The peak impulse response threshold value for the good or functional elements is estimated to be $0.11\,\mathrm{V\,V^{-1}}$ for rows and $0.50\,\mathrm{V\,V^{-1}}$ for columns, giving 108 rows and 123 columns. The less good or semi-functional elements are in the range from $0.06\,\mathrm{V\,V^{-1}}$ to $0.11\,\mathrm{V\,V^{-1}}$ for rows and $0.13\,\mathrm{V\,V^{-1}}$ to $0.50\,\mathrm{V\,V^{-1}}$ for columns, giving 27 rows and 12 columns. The bad or NC elements are below $0.06\,\mathrm{V\,V^{-1}}$ for rows and $0.13\,\mathrm{V\,V^{-1}}$ for columns, which amounts to 55 rows and

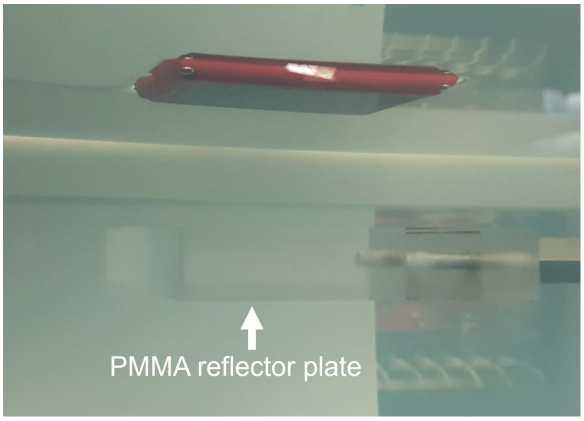


Figure 9.34: Photo of the setup used for pulse-echo measurements. A PMMA reflector plate is seen in the image, placed at 30 mm from the transducer surface.

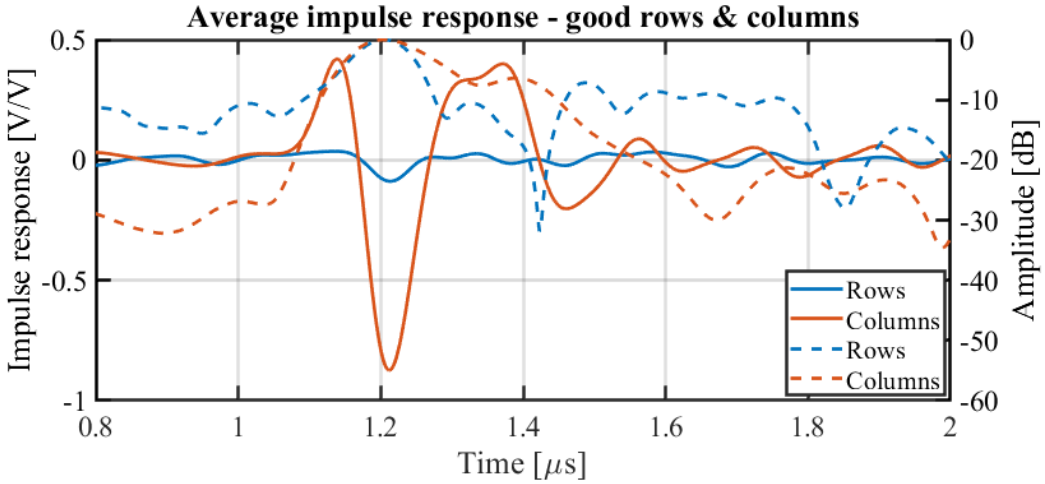


Figure 9.35: Average pulse-echo impulse response in transmit (PE), as solid lines, and the normalised envelope (in dB), as dashed lines, of the functional row and column elements with amplitudes above $0.11 \times 10^{15}\,\mathrm{V\,V^{-1}}$ for rows and above $0.50 \times 10^{15}\,\mathrm{V\,V^{-1}}$ for columns.

Table 9.6: Overview of the pulse-echo yield and associated impulse response amplitude cut-off values for each of the three element categories; functional, semi-functional and bad/NC.

Element category	Cut-off value [V V^{-1}]		Amount (% yield of 190)		Total yield (of 380)
	Rows	Columns	Rows	Columns	
Functional	>0.11	>0.50	108 (56.8%)	123 (64.7%)	60.8%
Semi-functional	0.06<i<0.11	0.13<i<0.50	27 (14.2%)	12 (6.3%)	10.3%
Bad/NC	<0.06	<0.13	55 (28.95%)	55 (28.95%)	28.95%

55 columns. The grouped element numbers and yields are listed in Table 9.6.

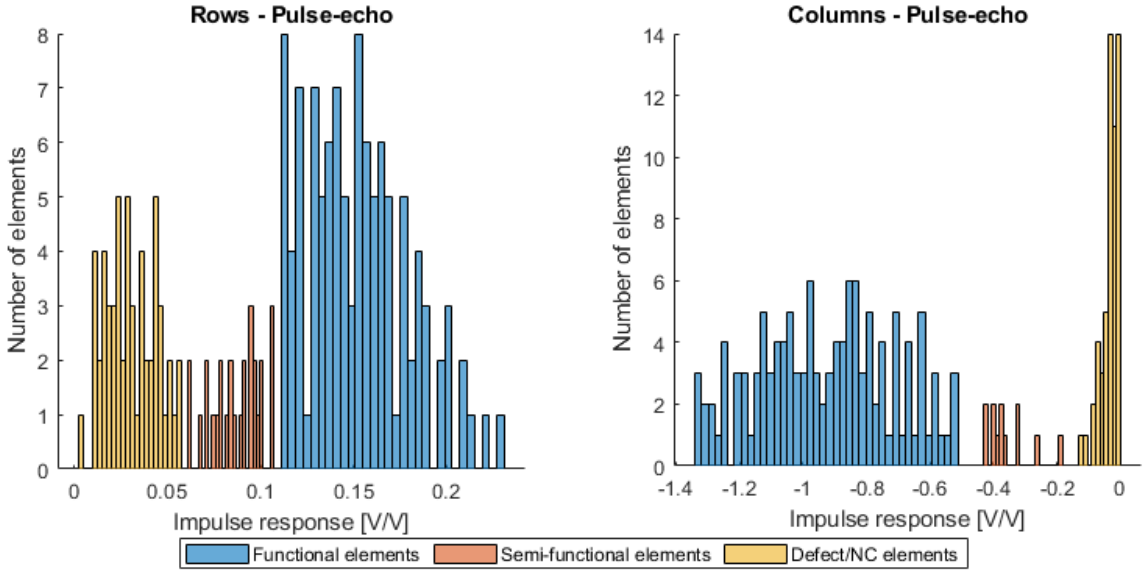


Figure 9.36: Histogram of the maximum impulse response values for all the rows and columns in pulse-echo. These are grouped into three categories depending on their maximum impulse response values.

The spectra of the averaged impulse responses are plotted in Fig. 9.37 for rows and columns, which have been normalised to their maximum impulse response values $34.9 \times 10^{-3}\,\mathrm{V\,V^{-1}}$ and $402 \times 10^{-3}\,\mathrm{V\,V^{-1}}$, respectively.

9.3.2 Results analysis and discussion

The results from the measurements in transmit and pulse-echo will be discussed and compared.

The center frequencies from the two spectra can be found using the same formula as Eq. 6.2, repeated here for convenience:

$$f_c = \frac{\sum_{i=0}^{N/2} S(i\,f_s/N) \cdot i\,f_s/N}{\sum_{i=0}^{N/2} S(i\,f_s/N)} \tag{9.10}$$

where f_s is the sampling frequency which was 70 MHz and N is the number of frequency bins in the spectrum S. The sum is made up until 35 MHz (the Nyquist frequency at $f_s/2$), multiplying and weighing the amplitudes contained in S with the corresponding frequency and normalising with the sum of the components of S.

The transducer bandwidth is found by normalising the spectra to their respective weighted center frequencies and finding the upper and lower frequency values corresponding to the -3 dB cut-off for

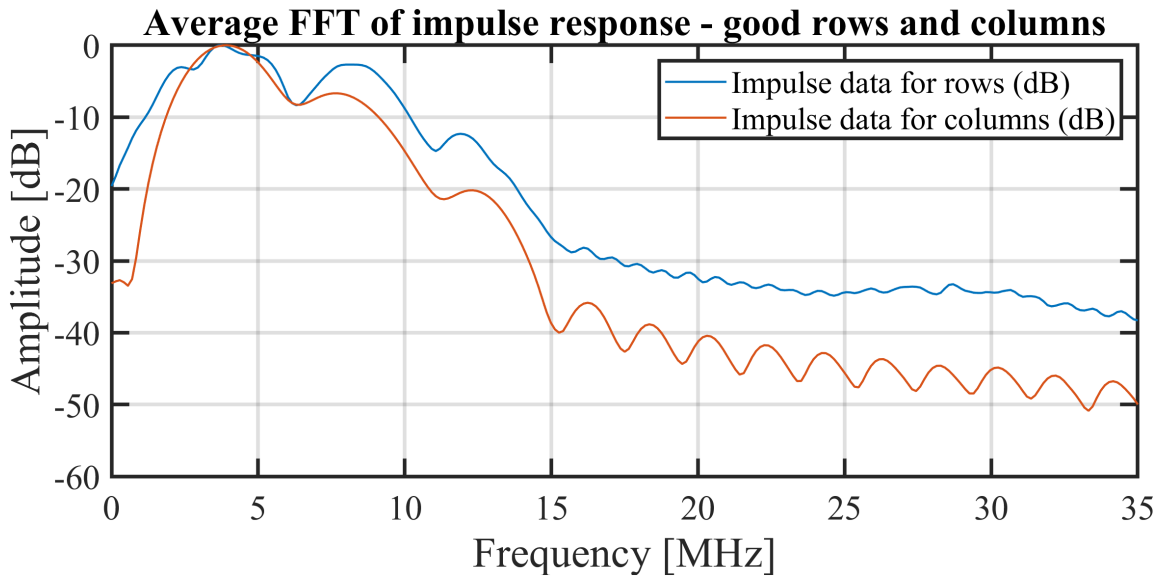


Figure 9.37: Average FFT spectra of the impulse response in pulse-echo (PE) of the functional row and column elements with impulse response amplitudes above $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$. The spectra for the rows and columns are normalised to the maximum of the average impulse responses with the values $2.11 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ and $7.63 \times 10^{-5}\,\mathrm{V\,V^{-1}}$, respectively.

the transmit measurements and similarly the upper and lower frequency values corresponding to the $-6\,\mathrm{dB}$ cut-off for the pulse-echo measurements. The formula used is

$$f_{\mathrm{rel.BW}} = \frac{f_{\text{-3dB,1}} - f_{\text{-3dB,2}}}{f_c} \times 100\,\% \tag{9.11}$$

where $f_{\text{-3dB,1}}$ and $f_{\text{-3dB,2}}$ are the two points on the frequency axis corresponding to $-3\,\mathrm{db}$.

The peak frequency is also extracted from the FFT spectra in Fig. 9.33 and Fig. 9.37, by taking the frequency on the x-axis associated with the maximum amplitude.

Transmit

The averaged transmit impulse responses in Fig. 9.31 show that the shape of pulses and envelopes of rows and columns are they same. The peak sensitivity value of the rows and columns are measured to be $1.67 \times 10^{16}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.13 \times 10^{16}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$, respectively. This shows that the columns has around 67 % (or a factor 1.48) of the transmit sensitivity when compared to the rows.

This tendency is opposite of the performance of the measured transmit signal of the TR2 probe, where the rows had a smaller amplitude than the columns with a factor of 1.8. The plotted impulses in Fig. 9.31, are generated from cross-correlated and aligned functional elements with amplitudes $> 6.94 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the rows and $> 5.18 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ for the columns. Elements with an impulse response amplitude above the threshold but with a different pulse shape, length and phase compared to the other functional elements, are sometimes not aligned correctly to the reference pulse. This results in the averaged impulse response function broadening and decreasing in amplitude, which can explain some of the discrepancy seen between rows and columns.

Another more plausible reason for the difference in rows and columns in transmit might be explained by focusing on the electrical measurements shown in Section 9.1.1. For the IV and CV measurements shown in Fig. 9.4 and Fig. 9.11, respectively, only two short-circuits between neighbouring elements are found, and most of the minimum capacitances are at the same level around 31.5 pF.
For the top electrodes seen in Fig. 9.5, a total of 46 neighbour to neighbour measurements are short-circuited. Most of these elements in Fig. 9.12 also have corresponding low capacitances, but the

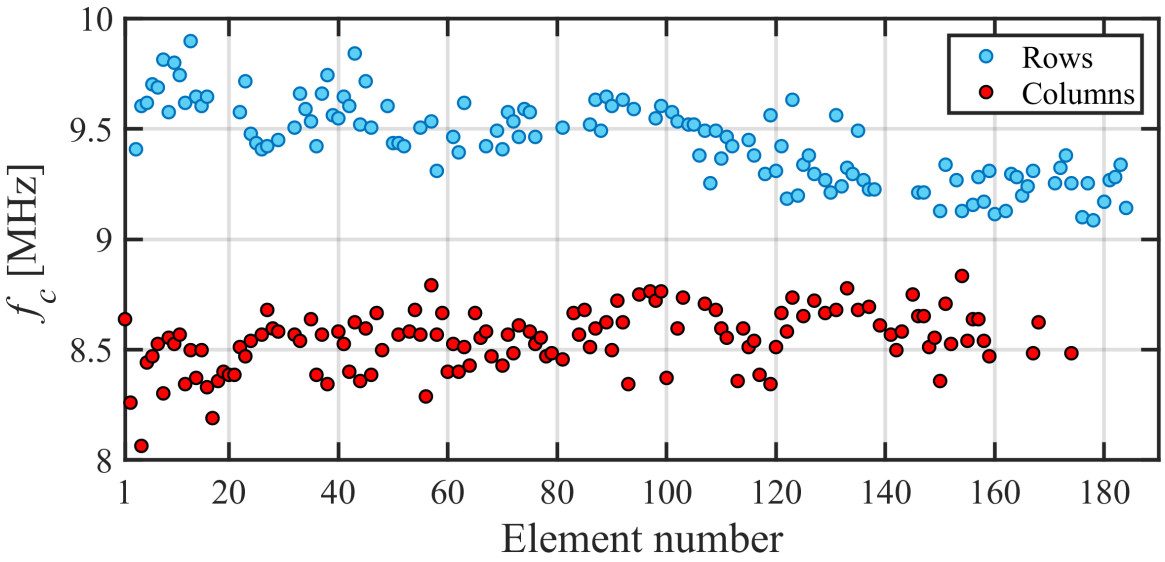
elements adjacent to the shorted neighbours have higher capacitive values, as discussed previously. When acoustical characterisation is performed on all the elements, both working and short-circuited-to-neighbour elements, the short-circuited elements will potentially emit a pressure with double amplitude or larger. Since many of the top electrodes are connected in pairs, the emitted pressure will in general be larger for the rows than the columns for this array, which is seen in Fig. 9.31.

The weighted center frequencies are calculated using Eq. 9.10 with data from the spectra in Fig. 9.33. The values are plotted in Fig. 9.38a for each functional row and column element in the range from 1 to 190, and are used to gauge to uniformity of the center frequencies across the array in transmit. The results are listed in Table 9.7, along with the bandwidths. The average center frequencies of the rows and columns are 9.44 ± 0.18 MHz and 8.54 ± 0.13 MHz, respectively, with the total average of both rows and columns at 8.99 ± 0.48 MHz. This center frequency is around 3.3 MHz lower than the designed at 12.3 MHz. A reduction in frequency is expected as the plate thickness of 2.156 µm was lowered during fabrication from the designed value of 2.5 µm, and the broad bandwidth found further below can accommodate using the transducer at 8 MHz and 12.3 MHz. This frequency in immersion was, however, expected to be around 10.7 MHz as listed in Table 9.1. The standard deviation of the measurements is relatively small but a difference between rows and columns of 0.90 ± 0.30 MHz is observed, similar to the TR2 probe, at 1.8 ± 0.4 MHz. It is seen from Fig. 9.38a that the row elements in the range from around 120 to 190 have a lower center frequency than the rest of the rows. This can possibly be explained by comparing an impulse response from row element E40 and E160, where the pulses are different and the center weight is shifted to a lower frequency. The shift in center frequency between rows and columns is currently not fully understood, as this would mean that they are either structurally different, or that the bias supplied is not at the intended level, which could be caused by impedance mismatch in the probe.

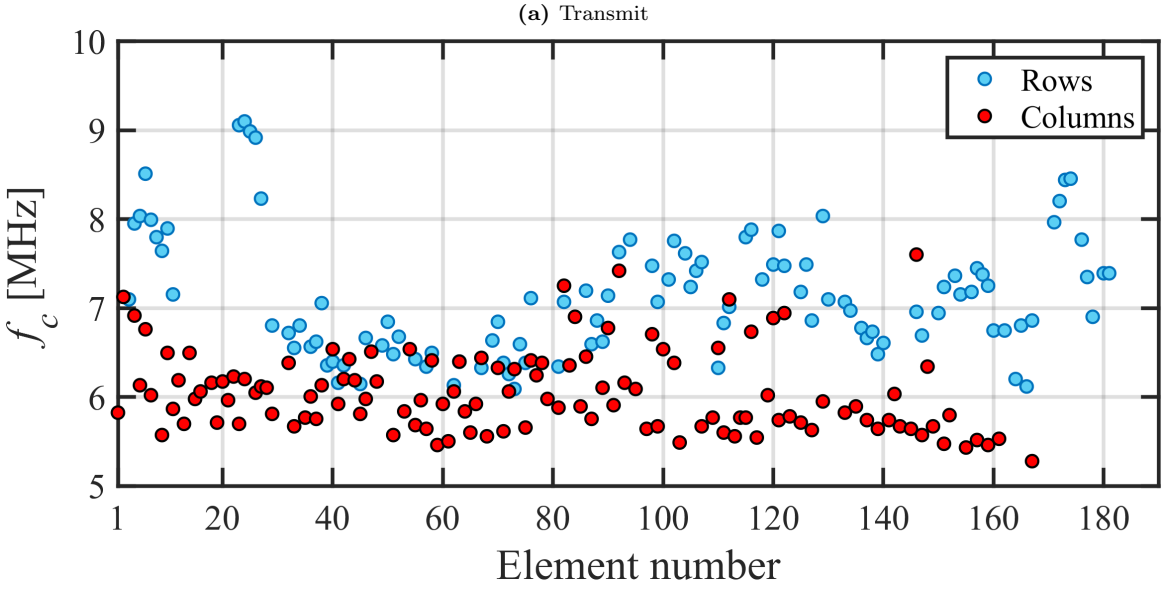
The mismatch between center frequencies are however not crucial for operating the transducer as the relative fractional bandwidth is high for both rows and columns. The average fractional bandwidth is 96.3 ± 10.8 % for rows and 81.5 ± 14.3 % for columns, where the total average bandwidth of both of rows and column is 88.9 ± 14.7 %.

The peak frequencies were also extracted from the spectra and plotted in Fig. 9.39a. The total average peak frequency of both rows and columns was found to be 8.64 ± 0.52 MHz. The results are listed in Table 9.7.

By observing the spectra in Fig. 9.33, two distinct dips in around the center frequencies are seen at 6.16 MHz and 10.78 MHz. These appear quite close in value to the substrate ringing, $f_{\mathrm{Sub}} = 5.56$ MHz, calculated in Section 7.2 and the Bragg frequencies, $f_{\mathrm{B},6} = 11$ MHz and $f_{\mathrm{B},7} = 10.5$ MHz and could very well correspond to these. The substrate ringing was surprisingly not observed in the TR2 probe, which utilised a different substrate as combination of silicon and borosilicate.

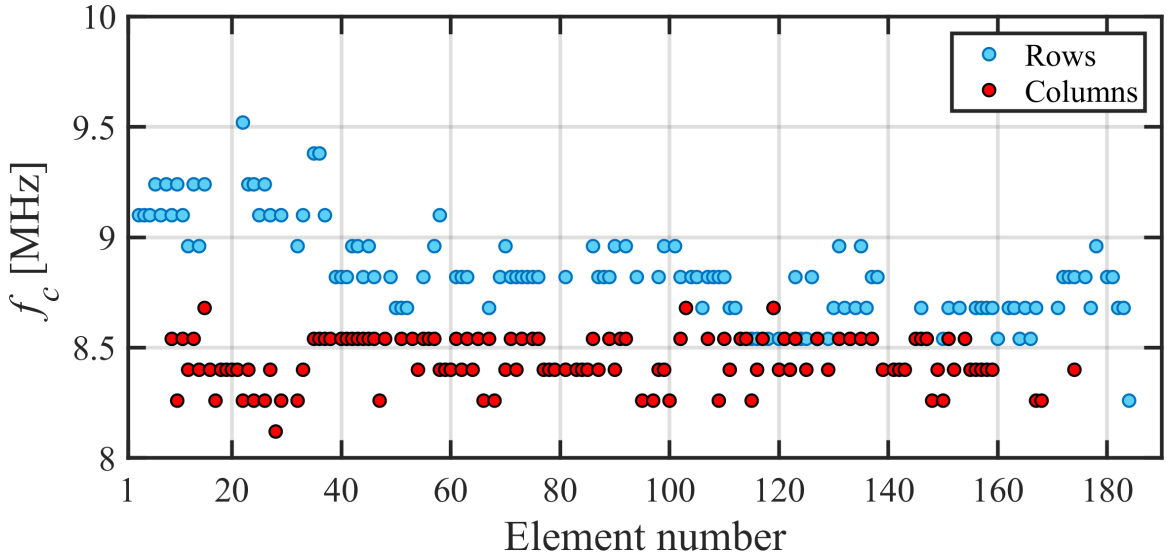


(a) Transmit

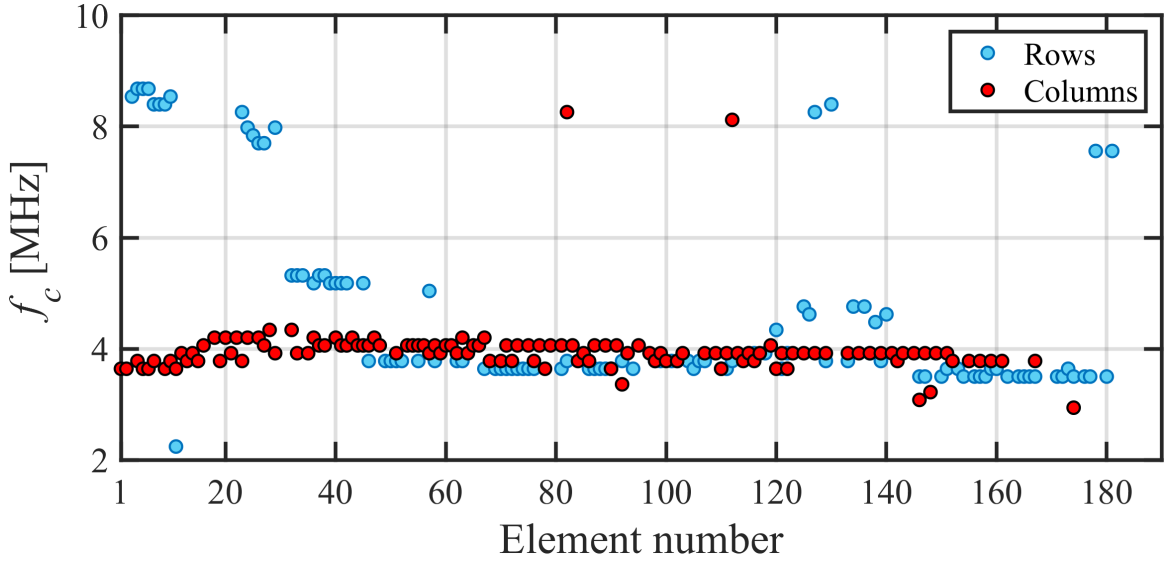


(b) Pulse-echo

Figure 9.38: Extracted center frequencies across the array for each element in transmit (a) and pulse-echo (b). The frequencies were found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses. The average center frequency of functional row and column elements in the probe is 9.0 ± 0.5 MHz in transmit and 6.6 ± 0.8 MHz in pulse-echo.



(a) Transmit



(b) Pulse-echo

Figure 9.39: Extracted peak frequencies across the array for each element in transmit (a) and pulse-echo (b). The frequencies were found by using a peak-finding algorithm in MATLAB. The average center frequency of functional row and column elements in the probe is 8.6 ± 0.5 MHz in transmit and 4.3 ± 1.3 MHz in pulse-echo.

Table 9.7: Results obtained from acoustical measurements of the probe in transmit and pulse-echo.

	Transmit			Pulse-echo		
Parameter	Row	Column	Total	Row	Column	Total
Center frequency [MHz]	9.44 ± 0.18	9.09 ± 0.13	8.99 ± 0.48	7.13 ± 0.69	6.08 ± 0.55	6.57 ± 0.81
Peak frequency [MHz]	8.91 ± 0.56	8.38 ± 0.28	8.64 ± 0.52	4.64 ± 1.70	3.98 ± 0.58	4.29 ± 1.28
Center frequency bandwidth [MHz]	9.09 ± 1.02	6.97 ± 1.26	8.02 ± 1.56	10.65 ± 3.66	8.27 ± 1.88	9.38 ± 3.09
Relative fractional bandwidth [%]	96.27 ± 10.79	81.49 ± 14.30	88.85 ± 14.66	152.81 ± 64.21	135.31 ± 23.70	143.49 ± 47.88
Sensitivity $[\mathrm{PaV^{-1}s^{-2}}]/10^{16}$	1.67	1.13	1.4	-	-	-
Sensitivity [mV/V]	-	-	-	88.6	873.6	481.1

Pulse-echo

The averaged pulse-echo impulse responses are shown in Fig. 9.35. Contrary to the previous transmit measurements the amplitude of the rows are now significantly reduced. The absolute peak sensitivity value of the rows and columns are measured to be $0.0886\,\mathrm{V\,V^{-1}}$ and $0.8736\,\mathrm{V\,V^{-1}}$, respectively. This shows that the rows surprisingly only have around 10 % (or a factor 9.86) of the pulse-echo sensitivity when compared to the columns. This large reduction is not expected as the yield of the functional rows at 56.8 % is comparable to the columns at 64.7 %.

To verify this receive sensitivity of the probe, another small measurement was made using a linear BK Medical commercial probe. This was placed beneath the prototype probe in place of the PMMA sheet and used to transmit, while the prototype probe was used for receiving. The received signal was recorded with the BK probe in two orientations perpendicular to the rows, and the columns. A few of the well-performing elements with a good impulse response were compared for the rows and columns. It was found that the rows had a peak sensitivity in receive of around 69 % to 77 % compared to the columns, or a factor of 1.44 for the former number, which is comparable to performance in transmit. The reason for the large difference between the recorded pulse-echo measurements and the receive measurements is at the time of writing this thesis is presently not understood. This results will, however, still be discussed in this section.

Previously fabricated 62+62 and 92+92 RCA CMUT probes [64], [82], which are based on an SOI wafer substrate with a 20 um device layer, exhibited a reduction of the column receive sensitivity by a factor of around 3 and 3.3, respectively. The TR2 probe in Part I in comparison showed a factor of 2.4. The tendencies exhibited by these probes are opposite when compared to the TH1 probe, as the rows show a lower receive sensitivity compared to the columns. If the values are compared to the factor of 1.44 from above, the TH1 probe show a clear improvement in the relative difference in receive sensitivity between rows and columns.

As previously discussed in Section 1.4.2 and for the TR2 probe, the substrate coupling is an important parameter which affects the sensitivity of the device. The substrate coupling has, as mentioned in [78], previously been most prominent when the bottom electrode are used in receive. When the top electrodes are probed and used for receiving they are grounded to the bottom electrodes and no capacitive substrate coupling is present.

Since the pulse-echo sensitivity of the rows is 10 % of the columns, it is difficult to determine if the columns are affected by any capacitive substrate coupling affects compared to the rows.

The substrate coupling between neighbouring elements was measured for the 190+190 bottom electrodes. This was performed by probing the electrodes in the glass cavities directly on a structure without a bonded top plate. The 1st nearest neighbour pair gave a value of 0.85 pF, the 2nd nearest neighbour a value of 0.47 pF and the 3rd a value of 0.32 pF. A simple estimate of the substrate coupling due to the fringe field in the borosilicate substrate can be given by the formula Eq. 6.6 in [123] as

$$C_{\text{Boro-fringe}} = \frac{4.6\epsilon_0}{\pi} \ln\left(1 + \frac{2W}{d}\right) L = 0.26\,\text{pF} \tag{9.12}$$

where the width of the square CMUT electrode is $W = 33\,\mu\text{m}$ and the nearest distance between neighbouring element electrodes is $d = 17\,\mu\text{m}$. The length $L = 33\,\mu\text{m} \times 2 \times 190 = 12\,540\,\mu\text{m}$ is taken as the width of the electrode multiplied by two, since there are two CMUT cells in a sub-element, times the number of sub-elements, 190. Both the measured and calculated substrate coupling capacitance is small compared to the value of a single element, $C_{0,\text{1-apo}} = 63.4\,\text{pF}$, and are likely not causing any reduction in the sensitivity. Referring to the sketch in Fig. 9.40 (a simplified version of Fig. 6.26), the contribution from the measured parasitic coupling capacitance $C_{\text{meas, coupling}}$ and the neighbouring element $C_{0,\text{2-apo}}$ is calculated

$$C_{\text{coupling}} = ((C_{\text{meas, coupling}})^{-1} + (C_{0,\text{2-apo}})^{-1})^{-}1 = 0.84\,\text{pF}. \tag{9.13}$$

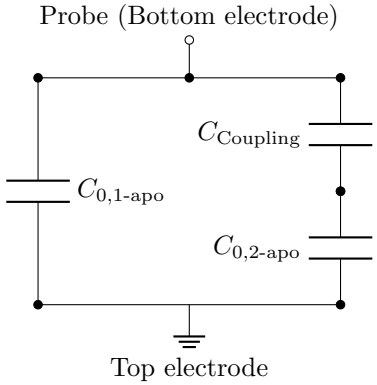


Figure 9.40: Circuit diagram of the neighbouring element coupling when probing column element 1, with $C = C_{0,1-apo}$ and the signal on the bottom electrode pad and ground on the top electrode. The measured parasitic capacitance C_{Coupling} as well as $C_{0,2\text{-apo}}$, from the neighbouring element 2, couples into the probed element.

Even when the contributions from both nearest neighbours on each side of the element are included, $C_{\text{Couplingx2}} = 1.67\,\text{pF}$, the effect is only around 2.6 % of the element capacitance.

The weighted center frequencies are calculated using Eq. 9.10 and are listed in Table 9.7. The values are plotted in Fig. 9.38b for each functional row and column element. The average center frequencies of the rows and columns are $7.13 \pm 0.69\,\text{MHz}$ and $6.08 \pm 0.55\,\text{MHz}$, respectively, with the total average of both rows and columns at $6.57 \pm 0.81\,\text{MHz}$. The standard deviation of the measurements is larger than for transmit data. It is currently not understood why the rows and columns in pulse-echo are 1 MHz to 2 MHz lower than during transmit. This average center frequency at $6.57 \pm 0.81\,\text{MHz}$ is even further from the designed 12.3 MHz and the expected frequency of 10.7 MHz due to the lower plate thickness. This large deviation is at the time of writing not currently understood. It is seen from Fig. 9.38b that some of the row elements at around E7, E25 and E175 have a higher center frequency than the rest of the rows. By inspection of the impulse response of these, it was seen that the pulse shape varied between the three (E7, E25 and E175) and a reference element, which can explain the shift in frequency.
The extracted peak frequencies show the same tendency, but the frequencies are naturally lower since the peak amplitude is detected at $\approx 60\,\%$ of the weighted center frequencies.

The relative fractional bandwidth (extracted from the spectra at the $-6\,\text{dB}$ points) was found to be $151 \pm 64\,\%$ for the rows and $135 \pm 24\,\%$ for the columns, with the total average for both at $144 \pm 48\,\%$. This broadband behaviour makes it possible to use the probe at multiple frequencies, but as it can be seen from Fig. 9.37, it will likely perform sub-optimal at 12.3 MHz, where the amplitude has decreased to $\approx -15\,\text{dB}$. The probe has the highest amplitude at $\approx 4\,\text{MHz}$ and $\approx 8\,\text{MHz}$, where in the latter the transducer pitch at 95 µm will correspond to $\lambda/2$.

Furthermore, the same dips in the spectra at 6.44 MHz and at 11 MHz are seen, which again likely corresponds to the substrate ringing $f_{\text{Sub}} = 5.56\,\text{MHz}$, calculated in Section 7.2 and the Bragg frequencies, $f_{\text{B},6} = 11\,\text{MHz}$ and $f_{\text{B},7} = 10.5\,\text{MHz}$.

9.3.3 Pressure uniformity

The electrode resistance discussed in Section 2.1.8 will be characterised for the TH1-A prototype probe in this section.

The theoretical ωRC product was estimated in Section 7.2 to be 0.78, using the calculated $C_{0,\text{apo}} = 51.6\,\text{pF}$ (including apodization), the resistance $R = 196.7\,\Omega$ and the frequency $f = 12.3\,\text{MHz}$. During the electrical characterisation the resistance of one long test element was measured, corresponding to

one element from the 190+190 array. Instead of the predicted 196.7 Ω it was found to be 512.82 Ω, which is likely caused during either the bottom electrode etching process, a cleaning step or the anodic bonding process itself. The cleaning or etching solution piranha was found to etch the Ti adhesion layer for the gold electrodes if it is not stirred constantly, as described in Chapter 8. This in combination with the anodic bonding process at high voltage steps can cause electrode damages. This is a topic under investigation in this research group but has not been further pursued in this PhD thesis.

The high resistance will lead to a higher attenuation than expected seen from the following example calculations using newly found center frequency in transmit and pulse-echo

$$\omega RC_{\text{transmit}} = 2\pi\, 8.99\,\text{MHz} \times 512.82\,\Omega \times 63\,\text{pF} = 1.82 \tag{9.14}$$

$$|H(L,\omega)|_{\text{transmit}} = 80.1\,\% \tag{9.15}$$

$$\omega RC_{\text{pulse-echo}} = 2\pi\, 6.57\,\text{MHz} \times 512.82\,\Omega \times 63\,\text{pF} = 1.33 \tag{9.16}$$

$$|H(L,\omega)|_{\text{pulse-echo}} = 87.8\,\%. \tag{9.17}$$

The pressure field was mapped in immersion using the Onda AIMS III by moving an Onda HGL-0400 hydrophone, connected to the experimental research ultrasound scanner SARUS, in the x-y plane in steps of 0.5 mm with a distance of 5 mm from the transducer surface. This creates a grid of 41×41 measurements with an area of 20.5 mm × 20.5 mm which will completely capture the footprint of the array is the apodization region is discounted. The elements with the apodization are only 18.05 mm long. A 4-cycle sinusoidal 9.5 MHz pulse with a voltage amplitude of $V_{\text{AC,peak}} = 40\,\text{V}$ was used to excite all the row and column elements sequentially for each position of the hydrophone in the grid. At each grid point the impulse response traces logged and convolved with a Hamming window with the same length as the signal used for excitation.

The pressure maps shown in Fig. 9.41 depict the average of the peak pressure field of the top element, row E127, and the bottom element, column E70. These elements were selected based on the list of functional good performing elements from the impulse response measurements. The pressure maps have been normalised by their maximum value, which for row E127 was 562.5607 and for column E70 was 358.5603. From both maps, it is seen by inspection that the pressure looks evenly distributed along the length of the elements, except for sudden decrease in pressure a lower part of the top electrode in Fig. 9.41(a), as if a section of element is missing. It is also seen that full extent of the pressure map is not captured by a 41 × 41 grid, as the top electrode extends out of the bounds of the plot. The hydrophone also appears to not have been fully aligned with the array, as the bottom electrode is shifted toward the bottom of the plot in Fig. 9.41(b). The lengthwise cross-sections along the elements are plotted in Fig. 9.42. The sudden drop in amplitude is seen clearly in Fig. 9.42(a). The mean value of the first and last 1/4 part of the top electrode has been calculated as an estimate of the drop in signal and the pressure uniformity. The section near the contact (near 0 mm in the plot) gives an average of −1.1 dB and near the end of the contact (near 20 mm) an average value of −2.4 dB is calculated. This corresponds to a drop to $85.6 \pm 21.8\,\%$ of the initial amplitude, or an attenuation of 15 % going from one end to the other of the element. This is much larger than the predicted $< 0.1\,\%$ for the top electrodes in Chapter 7, but can still be considered an acceptable value. A possible explanation for this can be found in from the formation of gold ribbons during the IBE etching process in Chapter 8. Repeated wet resist strips and plasma ashing was necessary to remove damaged resist and the gold ribbons, which damages the Cr adhesion and can damage the gold electrodes.
The sudden decreases in amplitude could be caused by the performance of the orthogonal elements, which provide the grounding during the measurements. If a bottom electrodes provides poor grounding or if a short-circuit exists between top and bottom electrodes, a decrease in pressure will likely be seen.

A peculiar example of such a short-circuit can be seen in Fig. 9.43 for row E47, where a decrease in amplitude is seen along the element length. At $\approx 17\,\text{mm}$ along the vertical row (top) element, the orthogonal bottom electrode is actuated, biased and is outputting pressure. These pressure maps have the potential to be used as a array diagnostic tool to confirm that only the expected elements are emitting pressure, and where potential defects can found and compared to previous electrical measurements.

From the cross-section in Fig. 9.42(b) the same calculations are performed on the column element E70. The section near the contact (near 16 mm in the plot) gives an average of $-1.7\,\text{dB}$ and near the end of the element (near 0 mm) an average value of $-3.1\,\text{dB}$ is calculated. This corresponds to a drop to $85 \pm 18\,\%$ of the initial amplitude, or an attenuation of $15\,\%$ going from one end to the other of the element. This attenuation is surprisingly lower than the calculated value in Eq. 9.15. The frequency of the excitation signal used was $9.5\,\text{MHz}$ giving instead an ωRC value and $|H(L,\omega)|_{\text{transmit}}$ of

$$\omega RC_{\text{transmit}} = 2\pi\, 9.5\,\text{MHz} \times 512.82\,\Omega \times 63\,\text{pF} = 1.93 \tag{9.18}$$

$$|H(L,\omega)|_{\text{transmit}} = 78\,\% \tag{9.19}$$

which is lower than or comparable to $85.6 \pm 21.8\,\%$, when the standard deviation is taking into consideration.

The unfortunate increase in bottom electrode resistance resulted in a reduction of $\approx 15\,\%$ of the transmitted signal amplitude along the element. This attenuation problem can be solved by simply increasing the bottom electrode thickness or increasing the electrode width, as long as the cell design permits it. It can therefore be concluded that using gold as the basis for metal electrodes is a viable strategy for obtaining uniform element pressure.

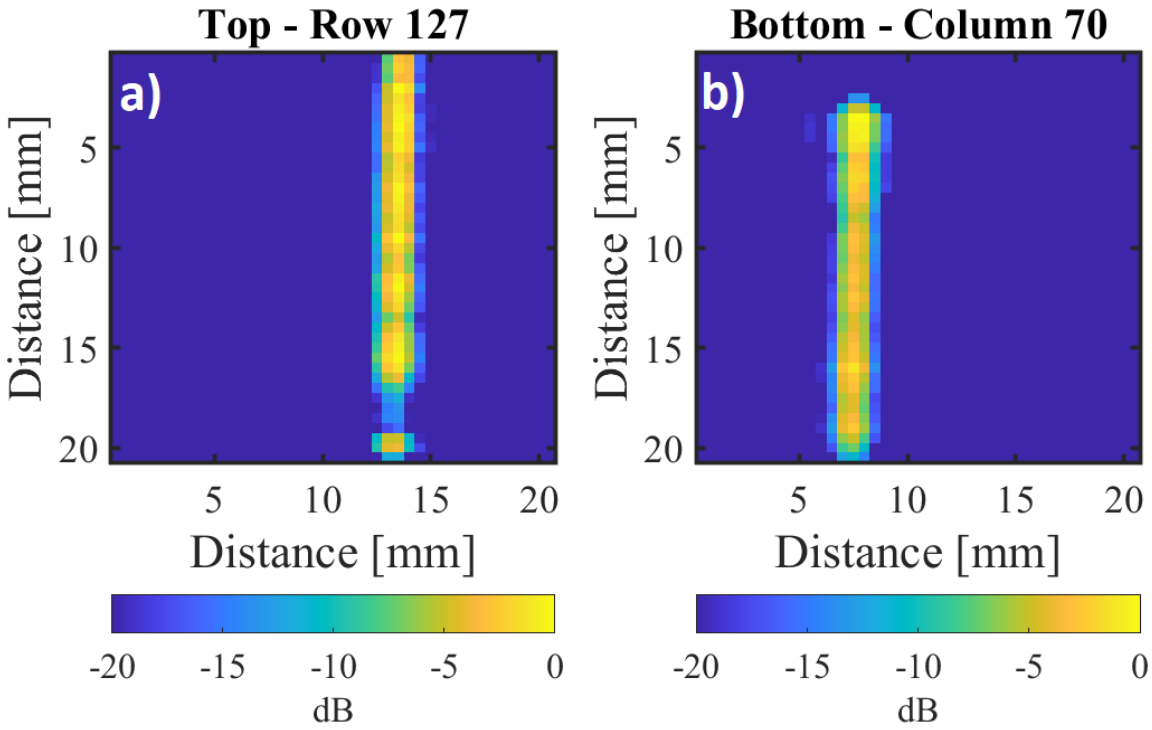


Figure 9.41: Average peak pressure field of elements excited at 9.5 MHz. The pressure is mapped for all top and bottom electrodes using a hydrophone and an average is shown in (a) for a single top electrode (row 127) and in (b) for a single bottom electrode (column 70), which has been rotated 90° for better comparison. The pressure is uniform along both electrodes. The pressure measured along the bottom electrodes shows a clear maximum value in the top of the image, near the contact pad of the element, but remains mostly uniform along the element.

9.4 Chapter summary

In this chapter the electrical and acoustical characterisation of the TH1-A array before and after integration in the prototype probe was presented. IV, CV, impedance and stability measurements were performed which showed a lower than expected center frequency in air at between 16 MHz to 17 MHz and a reduced pull-in at around 65 V due to a reduced vacuum from the fabrication process. The element capacitances were found to be in good agreement with the predicted value at 63.4 pF but with a large variation and many elements showed hysteretic charging behaviour. The yield from the electrical measurements was found to be 65 % and 55 % for the bottom and top electrodes, respectively.
Acoustical characterisation of the assembled probe in transmit and pulse-echo showed good performance of the elements, but with a low functional element yield at 67 % and 61 %, respectively. A discrepancy in the transmit and pulse-echo receive sensitivities between the rows and columns were found. In transmit this effect was discussed to be due to the many neighbour-to-neighbour short-circuits. The total averaged center frequencies for rows and columns was found to be lower than the predicted 10.7 MHz in immersion by around 2 MHz to 3 MHz. The total averaged fractional bandwidths of the rows and columns were calculated in transmit to be 89 ± 15 % and in pulse-echo to be 144 ± 48 %. Finally, signal attenuation was evaluated for the top and bottom electrodes and found to be 15 % for both.

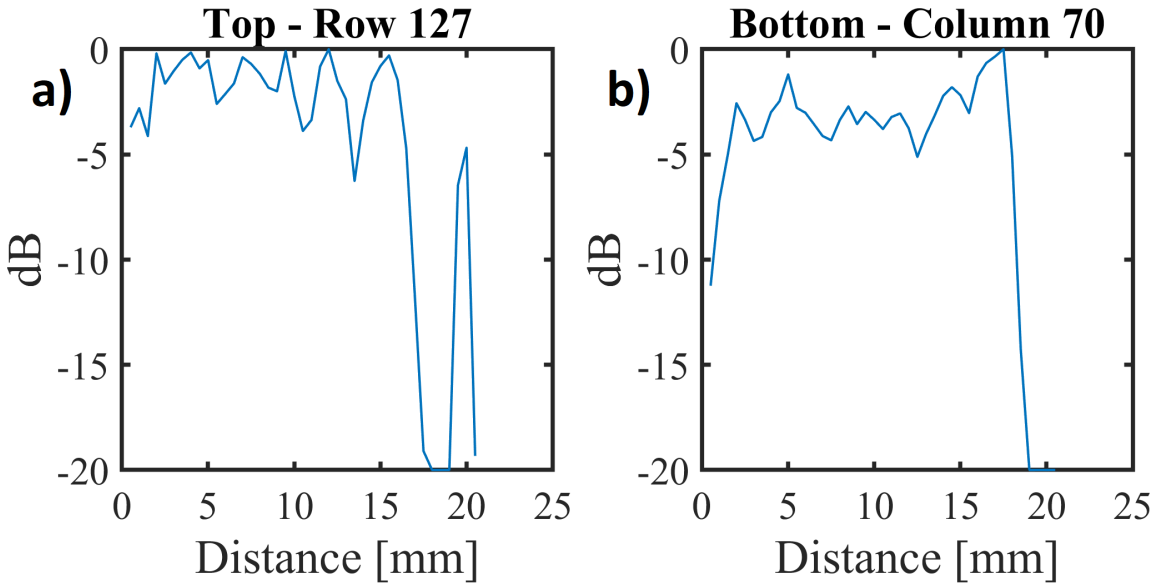


Figure 9.42: Average peak pressure field of elements excited at 6.5 MHz. The plots are lengthwise cross-sections of the maps shown in Fig. 9.41 depicting in (a) the top electrodes (rows) with the contact pad placed in the left hand side of the plot and in (b) the bottom electrodes (columns) with the contact pad in the right hand side. The pressure is mostly uniform along the top electrodes, except for the drop at 180 mm, which is likely caused by the performance of the orthogonal element, which provide the grounding during the measurements. The pressure measured along the bottom electrodes shows a clear maximum value in the top of the contact but remains mostly uniform along the element.

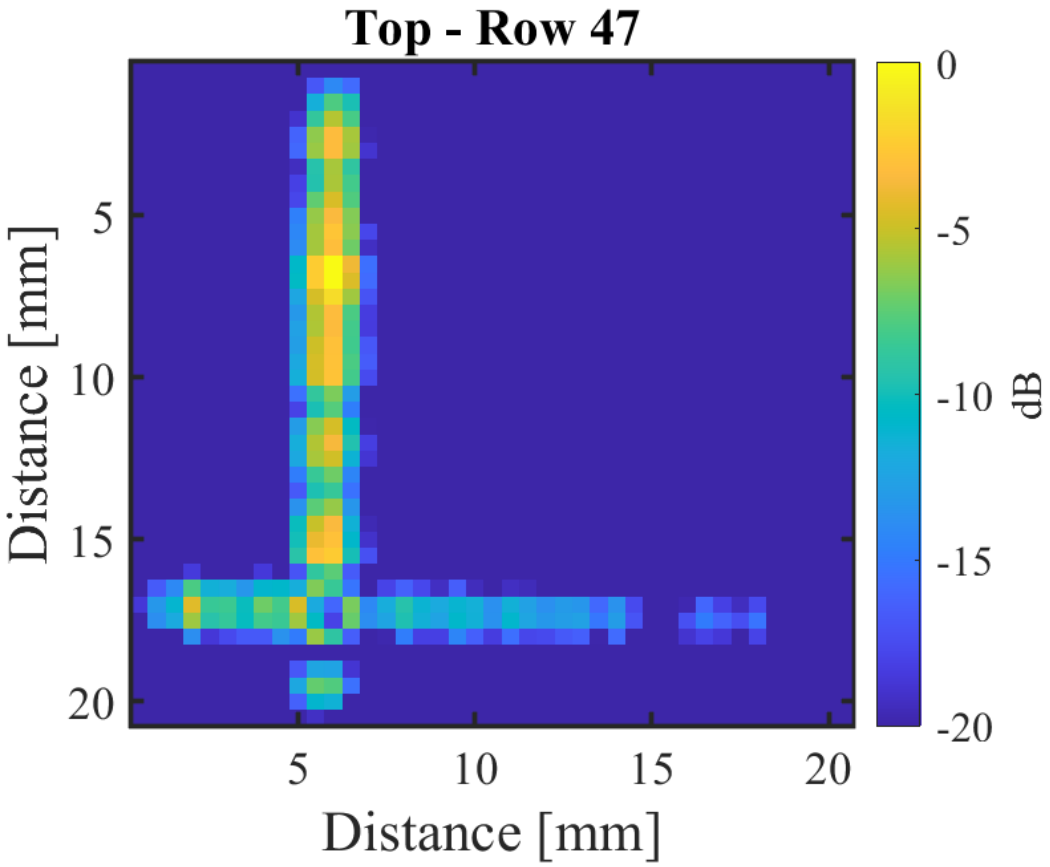


Figure 9.43: Average peak pressure map of row element E47 excited at 9.5 MHz, showing a short circuit with orthogonal bottom elements at ≈ 17 mm and thereby the actuation of these.

Chapter 10

Conclusion and outlook

This thesis has described the work of the PhD project with the title Micromachined Integrated 2D Transducers for Resolution Ultrasound Imaging. The main goal of this project has to develop large scale 2D 190+190 row-column-addressed (RCA) capacitive micromachined ultrasonic transducer (CMUT) arrays for the use in three dimensional volumetric imaging. This has been achieved through the fabrication of two chip designs, based on two different fabrication techniques, which have been compared throughout the thesis. The techniques are using the local oxidation of silicon (LOCOS) based process combining fusion and anodic bonding with highly doped silicon as bottom electrodes, and using a purely anodic bonding process with metal bottom electrodes. They each have their advantages as CMUT platforms for building arrays with a uniform pressure output for all elements. These chips were integrated in 3D milled hand-held probes, designed and built through a collaboration in this project between the company BK Medical and DTU Health Technology. One of these probes were made as a modular prototype probe capable of interchanging the CMUT arrays for use in rapid prototyping.

In Chapter 2 a method for use in designing CMUT devices was developed. This uses a combination of analytical expressions and simulations using finite element method (FEM) software to derive the geometric parameters of the CMUT cells, as well as the capacitance and operation voltage for the required center frequency. The final parameters are found through an iterative process with the theoretical values used as input for the simulation. An acoustical coupling phenomenon between periodic CMUT cells and the substrate ringing were also discussed as potential detrimental effects when acoustical characterisation is to be performed. A model for predicting the acoustical attenuation of the signal along the array elements was developed as a delay line model, based on the dimensionless ωRC product. This was previously developed in the group, and can be used as a tool for selecting appropriate top and bottom electrode material and dimensions for large scale arrays.

In Chapter 3 the methodology used when performing electrical characterisation of the chips before the probe assembly was presented. Due to limitations of the automatic wafer probing station used, it was not possible to perform electrical test by measuring between the top and bottom electrodes of the large 190+190 arrays. These tests would require all rows or columns to be connected and was not possible in our current setup. To evaluate the performance of each element, a different measuring technique was developed to perform the measurements and test analysis with probes placed on neighbouring elements. This method allows for determination of the capacitance between two elements which was shown to be half of the capacitance of a single element. This method also allows one to deduce how many neighbouring elements are short-circuited.

In Part I Chapter 4 the focus was set on the development of the TR2 array. The design parameters were partially found based on the procedure from Chapter 2, and the choice of bottom electrode thickness was discussed based on the estimated electrode resistance, which ultimately predicted a signal attenuation of 0.04 %. The center frequency in immersion was chosen as 4.5 MHz with a smaller than $\lambda/2$ element pitch, different from the originally designed 8 MHz frequency. This was

explained as to be due to an error in the initial 3D model used in OnScale to simulate the frequency. The single round cell design was settled on a 70 µm diameter, with a 4 µm plate and a 100 µm thick silicon electrode with a resistivity of $\rho_{Si} < 0.025\,\Omega\,cm$.

In Chapter 5 the novel microfabrication process of the TR2 array is described, using the design developed in this group. This was based on the LOCOS process for fabricating the cell cavities. The TR2 array was successfully fabricated and presented as a diced chip in the final part of the chapter. However, damage was observed on 40 % of the elements, which was caused by the formation of a sulphur compound during a bottom electrode etching process. This was found to cause yield problems during later characterisation.

The following Chapter 6 presented all the various electrical, thermal and acoustical characterisation of the TR2 array. The TR2 array was successfully assembled into an ultrasound probe. A pull-in voltage at around 185 V, and the operational bias was set to 150 V. The electromechanical coupling coefficient was $k^2 \approx 7\,\%$. A center frequency of 9.25 MHz was found to match the designed value when biased at 150 V. Acoustical measurements of the assembled probe in transmit and pulse-echo were performed and the impulse responses and frequency spectra of the rows and columns of the probe were found. These showed a total functional element yield of the rows and columns in transmit as 61 % and in pulse-echo as 55 %, respectively. The sensitivity of the rows, or top electrodes, were found to be a factor of 1.8 lower than for the columns, or bottom electrodes, in transmit.
In pulse-echo the sensitivity of the columns were measured to be 2.4 times lower than the rows. An explanation for the effect in transmit was not found, but was discussed for the pulse-echo measurements to be due to element-to-element capacitive coupling in the kerf between the bottom elements in the array. Even with a 2.4 times reduction in column receive sensitivity, the probe was found to perform better in terms of relative sensitivity of rows and columns when compared to previous silicon-on-insulator (SOI) substrate based RCA probes fabricated in this group.
The average weighted center frequencies for the rows and columns in transmit were 5.0 ± 0.1 MHz and 6.9 ± 0.3 MHz, respectively and the fractional bandwidth at $65 \pm 4\,\%$ and $61 \pm 4\,\%$, respectively. The difference in frequency between rows and columns of $\approx$2 MHz is likewise not currently understood. In pulse-echo, these same parameters for the rows and columns were 5.3 ± 0.2 MHz and 5.5 ± 0.5 MHz, respectively and the fractional bandwidth at $80 \pm 4\,\%$ and $96 \pm 9\,\%$, respectively. The total element yield in transmit was 61 % and 55 % in pulse-echo.
Furthermore, results from pressure uniformity measurements showed that the bottom electrodes had an attenuation of 12 %. This result is an improvement over a previous smaller 92+92 RCA CMUT probe with a high electrode resistivity, and is comparable to another 62+62 RCA CMUT probe. This shows that the highly doped silicon substrate used for the TR2 probe is a viable platform for fabricating large RCA arrays.
Thermal characterisation was presented and showed that the probe exhibited little to no heating when imaging sequences were transmitted, and this can potentially lead to much higher output pressure and lower signal to noise ratio (SNR) if a higher pulse repetition frequency (PRF) can be used with coded excitation.
Lastly, the 3D volumetric imaging results of the probe were presented in the last part of the chapter. When imaging was performed on 3D printed hydrogel phantoms, the resolution of the point spread function (PSF) was determined in the axial direction to be 0.82λ (0.188 mm) and in the lateral direction to be 1.72λ (0.394 mm). A wire matrix phantom in wafer was measured to a depth of 80 mm. The resolution of the PSF was in the axial direction 1.16λ (0.265 mm) and in the lateral direction 1.56λ (0.356 mm). The contrast was found to be -16.90 dB. Results from SNR measurements showed a penetration depth of 3.6 cm as a result of the many missing elements.

In Part II Chapter 7 the focus was set on the development of the TH1-A array. The design parameters were also based on the procedure from Chapter 2. The choice of metal bottom electrode thickness was based on the estimated electrode resistance, which predicted a signal attenuation of 4.8 %. The center frequency in immersion was chosen as 12.3 MHz with a slightly higher than $\lambda/2$ element pitch at $3/4\lambda$, due to the availability of the plate thickness at this time. The two-cell square design was settled on a 37 µm side length, with 33 µm square metal electrodes. The plate thickness was 2.5 µm, the gap was 135 nm and a 280 nm thick Au electrode with a resistivity of

$\rho_{Au} = 3.15 \times 10^{-6}\,\Omega\,\mathrm{cm}$ was used.

In Chapter 8 the microfabrication process of the TH1 array is described, using the anodic row-column design developed in this group. This was based on wet etching the cell cavities in borosilicate glass and anodically bonding the substrate to a top plate. The TH1 array was successfully fabricated. However, only one functional chip was successfully fabricated due to multiple problems affecting the yield. During the definition of the metal bottom electrodes, it was found that the sputter etching process produced ribbon-like strips of metal from re-deposition, which were challenging to prevent from occurring and to remove from the wafer surface. Furthermore, it was found that over etching in the sputter etching process had reduced the cell gap height to 96 nm, and that the poly-silicon-on-insulator (PSOI) used had a reduced plate thickness of $\approx 2.1\,\mu\mathrm{m}$ to $2.2\,\mu\mathrm{m}$ instead of $2.5\,\mu\mathrm{m}$. This reduced the expected resonance frequency to 10.7 MHz

The following Chapter 9 presented all the various electrical and acoustical characterisation of the TH1-A array. The fabricated TH1-A array was successfully integrated in an ultrasound prototype probe.

IV, CV, and impedance measurements were made using the method described in Chapter 3 by measuring between neighbouring elements. IV measurements showed only two short-circuited elements for the bottom electrodes, whereas 46 were seen for the top electrodes. CV measurements showed that the elements exhibited capacitances close to the expected value of 63.4 pF. Criteria for sorting the elements were used, based on short-circuits, missing connections, low capacitance, poor parabolic fit to the CV curve and if the elements exhibited charging hysteresis. This resulted in an element yield of 65 % for the top electrodes and 55 % for the bottom electrodes, respectively.

The impedance measurements did not result in a clearly defined pull-in as elements were shown to exhibit charging and unstable performance voltages around $V_{\text{pull-in}}$. Nevertheless, a pull-in was estimated at around 65 V, giving an operational DC bias at 50 V. The center frequency was found to lie lower at 16.5 MHz to 17 MHz than the simulated value at 21.6 MHz when biased at 50 V.

Acoustical measurements of the assembled probe in transmit and pulse-echo were performed and the impulse responses and frequency spectra of the rows and columns of the probe were found. These showed a total functional element yield of the rows and columns in transmit as 67 % and in pulse-echo as 61 %. The sensitivity of the columns, were found to be a factor of 1.48 lower than for the rows in transmit, which was the opposite behaviour of the TR2 probe. This was discussed to be the result of the many shorted top electrode pairs (rows), which meant that many elements would emit higher pressure than the bottom electrodes (columns).

In pulse-echo the rows had a sensitivity of 9.86 times lower than the columns. The reason for this effect is not yet understood, as the substrate coupling between elements was measured to be insignificant at ≈1 pF. Another separate test was performed using another transducer for transmitting while the TH1 was receiving. This showed that the that the sensitivity of the rows was a factor of 1.44 lower than the columns. It was therefore speculated that problems might have occurred during the pulse-echo tests. However, re-measuring had at the time of hand-in of this thesis not yet been done. Even with a 1.44 times reduction in row receive sensitivity, the probe was found to perform better in terms of relative sensitivity of rows and columns when compared to previous SOI substrate based RCA probes fabricated in this group.

The average weighted center frequencies for the rows and columns in transmit were 9.4 ± 0.2 MHz and 8.5 ± 0.1 MHz, and the fractional bandwidth was 96 ± 11 % and 81 ± 14 %, respectively. In pulse-echo, these same parameters for the rows and columns were 7.1 ± 0.7 MHz and 6.1 ± 0.6 MHz, and the fractional bandwidth was 80 ± 4 % and 96 ± 9 %, respectively. The reason for the difference in frequency between rows and columns of 1 MHz to 2 MHz is not known yet. The total element yield in transmit was 67 % and 61 % in pulse-echo.

Furthermore, results from pressure uniformity measurements showed that both the top and bottom electrodes had an attenuation of ≈ 15 %, much higher than anticipated. An explanation for the increased bottom electrode attenuation was given as poor grounding to the orthogonal elements and electrode damages during fabrication. This uniformity result is still an improvement over a previous smaller 92+92 RCA CMUT probe with a high electrode resistivity, and the resistance can be further decreased by increasing the metal electrode thickness. This shows that using metal electrodes for

fabricating large RCA arrays is a viable method.

In conclusion, the work of this PhD project has addressed the design and fabrication of two large scale 2D 190+190 RCA CMUT probes. Both of these were fabricated successfully but also demonstrated problems with electrical and acoustical performance differences between rows and columns. These also showed a reduced yield. The anodically bonded TH1-A array was predicted to exhibit low substrate coupling, low signal amplitude attenuation and high fabrication yield. It showed a very low substrate coupling, a low attenuation, but also a relatively low yield affected by short-circuited top electrodes and charging effects. In spite of this, initial acoustical probe measurements showed many functional elements with a high relative bandwidth. The fusion-anodic bonded TR2 array exhibited a large bottom electrode capacitive coupling and a relatively low element yield, which affected its acoustical performance and imaging depth. It did, however, show a low signal amplitude attenuation along the bottom electrodes.

This shows that these are both viably fabrication methods for making increasingly larger 2D arrays. Future work in this area should focus on optimisation of the fabrication yield and process reliability. This work is currently in progress.

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Chapter **A**

Design parameters and fabrication results

A.1 TH1-B design

The TH1-B array was built upon the design of the TH1-A array, and its parameters reflect some of the discoveries made during the fabrication process and electrical characterisation of TH1-A.

The array was initially intended to have a designed center frequency in immersion of around 8 MHz with an element pitch of 95 µm. The lateral dimensions of the TH1-B array is identical to TH1-1 design and will therefore not be repeated but can be found summarised in Table A.2. The same plate thickness of 1.62 µm and the ratio of the resonance frequency in immersion to the resonance frequency in air will be $\omega_r/\omega_0 = 0.44$ using Eq. 2.15 and Eq. 2.16. This will give a predicted resonance frequency in air/vacuum of 18.1 MHz. The effective CMUT gap calculated using Eq. (2.33) will, however, be different as another pull-in voltage is used.

The operating voltage for this TH1-B array will be 200 V which will result in a pull-in voltage of 250 V if a DC bias of 80 % V_{pi} is presumed.

The effective gap can for $h = 1.62\,\mu\text{m}$ be found using Eq. (2.33) with a $V_{\text{pi}} = 250\,\text{V}$

$$g_{\text{eff}} = \sqrt[3]{\frac{12(1-\nu^2)V_{pi,circ}^2\, a^4 \epsilon_0 \pi}{89.4459 Y h^3}} \tag{A.1}$$

$$= \sqrt[3]{\frac{12(1-0.177^2)(250\,\text{V})^2\,(18.5\,\mu\text{m})^4\, 8.854\times10^{-12}\,\text{F}\,\pi}{89.4459\cdot 148\,\text{GPa}(3.20\,\mu\text{m})^3}} = 348.8\,\text{nm}. \tag{A.2}$$

The plate used for this array will also a nitride layer facing inside the cavity. The vacuum gap is then found to be

$$g_{\text{eff}} = 343.6\,\text{nm} = g_{\text{vac}} + \frac{190\,\text{nm}}{6.86} \tag{A.3}$$

$$g_{\text{vac}} = 314.5\,\text{nm}. \tag{A.4}$$

These value were used as starting guesses in the 2D CMUT COMSOL model. From the fabrication of the previous TH1-A, it was found, see section polishing test if I write it, that the standard batch of PSOI wafers with a device (plate) thickness of 2.5 µm was instead an average of around

Table A.1: Numerical values of ω_{nm} in [MHz]

m \ n	0	1	2	3
0	23.95	49.83	81.75	119.62
1	93.21	142.54	198.23	260.15
2	208.82	281.48	360.46	446.000
3	370.77	466.63	568.81	677.79

2.1 µm to 2.2 µm. The nitride thickness from the previous fabrication was also found to be 190 nm instead of 200 nm, if the maximum run time for one deposition in the furnace is used. It was thus these value that were used in COMSOL. The adjusted values obtained from simulations are shown in Table A.2. Using the same equation for the pull-in voltage as a function of the gap height (Eq. (2.33)), the new effective gap and vacuum gap would be

$$g_{\text{eff}} = 261.3\,\text{nm} = g_{\text{vac}} + \frac{190\,\text{nm}}{6.86} \tag{A.5}$$

$$g_{\text{vac}} = 233.6\,\text{nm} \tag{A.6}$$

which is now closer to the value used in the simulations of 200 nm.

With the new plate thickness COMSOL model predicts a unbiased center frequency in air at 25.1 MHz and an biased center frequency at 22.18 MHz. The theoretical reduction in frequency from air to water will now be $\omega_r/\omega_0 = 0.49$. This results in a biased frequency in immersion of 10.95 MHz, which corresponds to a $\lambda/2$ pitch of 70.3 MHz. By the same argument as for the TH1-A array, this array would have a pitch of around $3/4\lambda$ if it is used at 10.95 MHz. It is, however, expected to have a relative fractional bandwidth of 60 % to 100 % and would be able to operate at 8 MHz if necessary.

The TH1-B array design, being identical to the TH1-A, can be seen in Fig. 7.2.

The Bragg and substrate ringing frequencies will, due an same lateral geometry and substrate thickness, lie at same frequencies as the TH1-A array.

The eigenfrequencies are found for the array using the numerical values for k_{nm} in Table 2.2 and Eq. 2.52. These have been calculated for the frequencies in vacuum and are given in Table A.1. The first and second eigenfrequencies are $\omega_{00} = 23.95\,\text{MHz}$ and $\omega_{10} = 49.83\,\text{MHz}$, respectively. It is seen that the first eigenfrequency is relative close to the unbiased resonance frequency found from COMSOL in vacuum at 25.1 MHz.

Now that final gap height has been found, the element capacitance can be calculated. The capacitance is estimated from from the simple parallel plate capacitance at zero bias from Eq. (2.22)

$$C_0 = \left(\frac{g_{\text{vac}}}{\epsilon_0\, A_{\text{elem,-apo}}} + \frac{g_{\text{ni}}}{\epsilon_{\text{ni}}\epsilon_0\, A_{\text{elem,-apo}}} \right)^{-1} \tag{A.7}$$

$$= \left(\frac{135\,\text{nm}}{8.854 \times 10^{-12}\,\text{F}\, A_{\text{elem,-apo}}} + \frac{200\,\text{nm}}{6.86 \times 8.854 \times 10^{-12}\,\text{F}\, A_{\text{elem,-apo}}} \right)^{-1} = 34\,\text{pF} \tag{A.8}$$

where $A_{\text{elem,-apo}}$, at $874\,862\,\mu\text{m}^2$, is the area of the metal bottom electrodes of the main part of the element, excluding the apodization region which is not biased when performing the electrical characterisation. When fully biased during scanning, including the apodization regions, the element will instead have an expected capacitance of $C_0 = 37.2\,\text{pF}$.

An estimate of the electrode resistance can now be given using the same geometric considerations and electrode width as in Section 7.2. This results in the following criterion

Table A.2: Designed TH1 B transducer parameters

Design parameter		Unit
Array		
Number of elements	190+190	
Element pitch	95	µm
Element width	92.5	µm
Kerf	2.5	µm
Element length	18.05	mm
Element thickness	100	µm
Apodization length	1.43	mm
Apodization sub-element count	15	
Array side length	2.12	cm
Center frequency in air (biased)	22.18	MHz
Center frequency in air	25.1	MHz
Center frequency in immersion	10.95	MHz
CMUT cell		
Cell side length (square)	37	µm
Cell electrode side length (square)	33	µm
Number of cells in sub-element	4	
Distance to cell kerf	5.25	µm
Cell to cell distance in sub-element	8	µm
Distance to neighbouring element cell	13	µm
Plate thickness	2.156	µm
Al electrode thickness	1000	nm
Vacuum gap	200	nm
Electrode thickness (Ti|Au)	10|210	nm
Plate nitride thickness	190	nm
Pull-in voltage	250	V
Operating voltage	200	V

$$\omega RC = \omega_r \, C_0 \, R_{\text{element}} = 2\,\pi \times 10.95\,\text{MHz} \times \left(\frac{54.33\,h + 0.21}{h^2}\right)\Omega \times 37.2\,\text{pF} < 0.35. \tag{A.9}$$

If this is solved for h, a gold electrode thickness of 401 nm is found. This would in turn mean that the cell cavity gap would have to be 401 nm + 200 nm = 601 nm. Instead a cavity gap of around 400 nm is used. A gold electrode thickness of 210 nm was ultimately chosen. An adhesion layer of 10 nm titanium between gold and glass was used. The effect on the resistance from this layer is minimal and not included.

This metal thickness gives an electrode resistance of 263.4 Ω and an ωRC product of 0.67. The signal amplitude is then expected to drop to

$$|H(L,\omega)| = 96.4\,\% \tag{A.10}$$

equalling an attenuation of 3.6 % which is deemed acceptable.

A.2 TH1-B processing results

For the fabrication of the TH1-B chip, a few processing parameters were changed. These are briefly described in the list below together with some of the results.

Ti adhesion layer Due to some observed electrode damage of the Cr adhesion layer in the fabrication of TH1-A, the adhesion layer was changed to Ti instead, which is not affected by plasma ashing steps or the etches performed in the advanced silicon etcher (ASE). However, it was found that Ti was etched in the piranha cleaning solution used before bonding. Therefore only a very short cleaning step is necessary coupled with continuous stirring of the solution in a beaker. Piranha has been found to have a moderate etch rate in sputtered bulk titanium film at 240 nm/min by Williams et al. [131], however the chemical ratio used was ≈ 50 parts 96% H_2SO_4 : 1 parts 30% H_2O_2 at 120 °C, so a direct comparison between our cleaning solution cannot be made.

Both chemical components of piranha aid in the etching process, but the exact combined reaction does not seem to have been studied in detail. The acid, H_2SO_4, by itself at a 46 % concentration at 80 °C, was found to have an etch rate of 63.2 nm/min [132], and the base, pure H_2O_2, an etch rate of 180 nm/min at 50 °C [133]. Due to concerns of under etching the Au electrode and the fact that the specific etch rate of Ti when used as an adhesion layer was unknown, wafers should only be immersed for a few tens of seconds or a minute.

IBE etching process The IBE etching process for defining the metal bottom electrodes was times carefully before each wafer batch was etched to ensure minimal over etch. This gave for the TH1-B arrays a vacuum gap between 196 nm to 201 nm, close to the designed value of 200 nm. Furthermore, a combination of a plasma ashing step for around 10 min and then repeated wet resist strips proved useful for removing the formed gold ribbons. This is however still under investigation.

KOH handle thinning A new problem concerning the silicon handle etch in the KOH etching bath was observed. Several small holes in the silicon dioxide etch stop layer was found after handle thinning. These are thought to either be the result of pinholes in the oxide or defects in the silicon handle wafer, causing some area to etch faster than others. This is still a topic for investigation. This resulted in holes in the top plate of many of the 190+190 arrays, which when coupled with particles present during the element separation etch caused many problems with yield.

A.3 Gold ribbons design of experiment

	Resist thickness	150°C Hard Bake	60° Etch	Resist Strip
1	~600 nm	No	No	Plasma
2	2 µm	Yes	No	Plasma
3	2 µm	No	Yes	Plasma
4	~600 nm	Yes	Yes	Plasma
5	2 µm	No	No	Wet
6	~600 nm	Yes	No	Wet
7	~600 nm	No	Yes	Wet
8	2 µm	Yes	Yes	Wet

Figure A.1: Table with DOE design, testing for four different process parameters in a two level fractional factorial design using 8 runs. This is run to test the presence of ribbons.

Chapter B

Process flows

B.1 Main fabrication process flows

B.1.1 Fusion anodic bonding process flow

Process flow title			Revision
RC CMUTs 2xLOCOS			**1.0**
DTU Danchip National Center for Micro- and Nanofabrication	Contact email ahav@nanotech.dtu.dk rungra@dtu.dk	Contact person Andreas Havreland Rune Sixten Grass	Contact phone 81711536 42280068
	Labmanager group MEMS(3313)	Batch name 2D CMUT LOCOS	Date of creation 13-Sep-19	Date of revision 8-Mar-22

Objective

Batch name: **Error! Reference source not found.**

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Substrates

Substrate	**Orient.**	**Size**	**Doping/type**	**Polish**	**Thickness**	**Box**	**Device layer thicknes**	**Purpose**	**#**	**Sample ID**
Si	<100>	4”	n (Phos.) <0.025 Ω cm	DSP	525±25µm		20 µm	Bottom electrode		
SOI	<100>	4”	n (Phos.)	SSP	525±25µm		3 µm	Top electrode 400 nm box		

Comments: Number of wafers is for illustration only

Step	Heading	Equipment	Procedure	Comments
1	Preparation			**Bottom electrode wafer**
1.1	Wafer selection	Wafer box		20 µm device layer
2	Oxidation – Insulation oxide			**Bottom electrode wafer**
2.1	RCA	RCA bench		All wafers
3	Oxidation – 2nd Insulation oxide			**Bottom electrode wafer**
3.1	RCA	RCA bench		All wafers
3.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and test wafers for equally distributed on each side of the test wafer. No spacing between wafers. Remember test wafers for later in the process LOCOS process 4.5 MHz **Recipe**: Dry1100, time:8h30min **Target thickness**: 400±10nm **Annealing time**: 20min	1-3 dummies Note time in logbook
3.3	Thickness measure	Filmtek/Ellipsometer	Measure oxide thickness on dummy wafer	Dummy wafer
3.4	Break down voltage		Out of clean room	Dummy
4	Nitride deposition – 2nd LOCOS nitride			**Bottom electrode wafer**
4.1	Si3N4 deposition	Nitride furnace (4'')	Deposit nitride **Recipe**: Nitride4 **Time**: 14 min (@ 3.4 nm/min) **Target thickness**: 55 nm ±5nm	
5	Polysilicon deposition – Nitride etch mask			**Bottom electrode wafer**
5.1	Polysilicon deposition	Polysilicon furnace (4'')	**Recipe**:Poly620 **Time**: 11 min (@8.7 nm/min) **Target thickness**: 100nm	
6	Lithography 1.5 µm – polysilicon etch/nitrid etch			**Bottom electrode wafer**
6.1	Coat wafer	Spin coater: Gamma UV	**Resist:** nLOF (negative resist) **Recipe:** 2411 DCH 100mm nLOF 2020 1.5um HMDS **Thickness:** 1.5 um	
6.2	Exposure	Aligner: MA6	Align to flat. Hard contact **Exposure time**: 10 sec **Intensity**: 11 mW/cm^2 **Mask**: Cavity (Darkfield)	
6.3	Develop	TMAH UV developer	**Recipe**: 3001 DCH 100mm PEB60s@110C SP60s PEB 110C	
6.4	Inspection	Optical microscope	Check pattern and alignment marks	
7	Polysilicon etch			**Bottom electrode wafer**
7.1	Polysilicon etch	Wet Poly Etch	Strip Poly-Si for 5 min	Might require 1 silicon wafer in the bath for conditioning

7.2	Strip resist	Plasma Asher 2	**Process time:** 10-15 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
7.3	Inspection	Optical microscope	Check pattern and alignment marks	
8	Nitride wet etch – 2nd LOCOS nitride			**Bottom electrode wafer**
8.1	Nitride etch	Wet bench	Wet silicon nitride etch H3PO4 @ 160 C (2.3 nm/min) **Time**: ~20 min	
8.2	7up	7up	Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH	
8.3	Inspection	Optical microscope	Check pattern and alignment marks	
8.4	Strip polysilicon mask	DRIE Pegasus	**Recipe**: 100nmPoly_SOI **Process time:** 12s (2 cycles)	
9	Lithography 1.5 µm – oxide/Si etch			**Bottom electrode wafer**
9.1	Coat wafer	Spin coater: Gamma UV	**Resist:** MiR 701 (positive resist) **Recipe**: 1411 DCH 100mm MiR 701 1.5um HMDS	
9.2	Exposure	Aligner: MA6	Align to flat. Hard contact **Exposure time**: 18 sec **Intensity**: 11 mW/cm^2 **Mask**: Bottom electrode	
9.3	Develop	TMAH UV developer	**Recipe**: 3001 DCH 100mm PEB60s@110C SP60s PEB 110C	
9.4	Inspection	Optical microscope	Check pattern and alignment marks	
10	Oxide etch – insulation layer			**Bottom electrode wafer**
10.1	Oxide etch	AOE	**Recipe:** SiO2_res **Time:** 2 min (@400nm oxide) **Temp:** 0C(or -5C to -10C)	Wait 30 min for temp to stabilize
10.2	Inspection	Optical microscope	Visual Inspection	Can you see silicon in the alignment marks?
11	Silicon etch –			**Bottom electrode wafer**
11.1	Etching Si	Pegasus	Etch 100 µm silicon from the top **Recipe**: Prototype/mae/DREM **Time**: approx. 36 min **Temp**: -19C	Check etch is all the way through the Si and you can see Oxide in the alignment marks
11.2	Strip resist	Plasma Asher 2	**Process time**: 45 min **O_2**: 400 ml/min **N**: 70 ml/min **Power**: 1000W	
12	Oxidation – 2nd LOCOS			**Bottom electrode wafer**
12.1	RCA	RCA bench	Only first HF for half the time (10 sec)	
12.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally	1-3 dummies Note time in logbook

		distributed on each side of the test wafer. No spacing between wafers. 4.5 MHz Recipe: Wet1100, time: 1 Hour 35 Min Target thickness: 840 nm Total on dummy: 750 nm	
12.3 Break down voltage		Out of clean room	Dummy
13 Wafer bonding – PSOI Top electrode			**All wafers**
13.1 RCA	RCA bench	RCA of wafers including new 3um (P)SOI wafers	
13.2 Fusion bonding	Wafer bonder 02	**Recipe**: CMUT Transport wafers in dedicated box from RCA, after hand bonding. Minimize ambient exposure and handling time. Use RCA cleaned tweezers	
13.3 Annealing	Anneal-bond furnace	**Recipe**: Ann1100 **Time**: 1h 10min	
13.4 Inspection	Pl mapper	Inspect post anneal voids **Detector**: Si + InGaAs **Gain**: x10 (corr.) **Filter**: 1100nm HP	
13.5 Oxide etch 2: BHF Clean	BHF	Etch through to silicon on both sides. **Time:** 6 min	Only if there is oxide on the back of SOI wafer
14 Device layer etch from backside			**Bonded**
14.1 Si etch	ASE/Grinding	Etch device layer until grooves/patterns are visible **Recipe**: etchaway (etchacar, use carrier if no clamping), ~1 hour to etch ~400µm (~6µm/min) 2 x 30 min + 1-5 x 5 min	(Etch until the oxide become visible at the circumference of the wafer, couple of mm. Then abort the process.)
14.2 Polish	Polisher/CMP	Polish backside of wafer prior to bonding Roughness 40 nm -> 0,5 nm 5 min CMUT Trench	
15 Wafer bonding – Borofloat/Pyrex Insulation wafer			**Bonded wafers and borofloat wafer**
15.1 RCA	RCA bench	RCA of wafers including cleaning borofloat wafers in Piranha solution for 10 min in separate beaker	
15.2 Anodic bonding	Wafer bonder 02	**Recipe**: CMUT (800V) Transport wafers in dedicated box from RCA, after hand bonding. Minimize ambient exposure and handling time. Use RCA cleaned tweezers	
15.3 Annealing	Anneal-bond furnace	**Recipe**: Ann1100 **Time**: 1h 10min	
15.4 Inspection	Pl mapper	Inspect post anneal voids **Detector**: Si + InGaAs **Gain**: x10 (corr.) **Filter**: 1100nm HP	
16 Handle layer and box oxide etch			**Bonded wafers**
16.1 Polysilicon or amorphous deposition	PECVD 3 or IBE/IBSD Ionfab 300	Deposits clampable a-Si or Poly-Si layer on glass side **Time:** approx. 35 min for 220 nm (PECVD3), or approx. 50 min for 200 nm (IBSD)	

16.2 Si etch	ASE	Etch handle layer away, **Recipe:** etchaway, ~1 hour to etch 360 µm (~6µm/min)	Etch until the oxide become visible at the circumference of the wafer. Then abort the process.
16.3 KOH	Si Etch 3: KOH	Etch the remaining of the device layer. **Process time**: (~10-15min)	If voids have been detected in the PL mapper, then make sure to puncture them with a tweezer. Then dip the wafers in the KOH again peel of the membrane.
16.4 Oxide etch	BHF	Etch box oxide away, Time: 7 min, check oxide is gone.	
16.5 Piranha	Fumehood	Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH	Don't use dirty single spin drier to dry
17 Lithography - Access to bottom electrodes			**Bonded wafers**
17.1 Deposit Al	Wordentec or Temescal	Target Al thickness: 100nm	
17.2 Coat wafer	Spin coater: Gamma UV	Mir 701 positive resist **Recipe**: 1411 DCH 100mm MiR 701 1.5um HMDS	
17.3 Exposure	Aligner: MA6	Align to flat. Hard contact **Exposure time**: 13 sec **Mask**: Access to bottom electrode (Darkfield Mask)	
17.4 Develop	TMAH UV developer	**Recipe**: PEB 110C 60s puddle develop	
17.5 Inspection	Optical microscope	Check pattern and alignment marks	
18 Etch - Access to bottom electrodes			**Bonded wafers**
18.1 Al etch	Wet bench 05: Al etch	**Etch rate:** ~60-100nm/min **Time:** 1.5 min	
18.2 Si etch	ASE	Etch through top plate layer, **Recipe:** prototype/shalolrc, 5 cycles, **Time:** 57 sec **Temp:** 20C	
18.3 Oxide etch	ASE	Etch through post oxide layer **Recipe:** SIO2IPCc **Time:** 3 x 4 min (@1356nm oxide) **Temp:** 20C	Wait 30 min for temp to stabilize
18.4 Strip resist	Plasma Asher 2	**Process time:** 45 min **O_2:** 400 ml/min **N:** 70 ml/min **Power:** 1000W	
18.5 Al etch	Wet bench 05: Al etch	**Etch rate:** ~60-100nm/min **Time:** 1.5 min	
19 Metallization			**Bonded wafers**
19.1 Deposit Ti+Al	Wordentec or Temescal	Target Ti thickness: 20nm Target Al thickness: 400nm	
20 Lithography – Top electrode			**Bonded wafers**
20.1 Coat wafer	Spin coater: Gamma UV	Mir 701 positive resist **Recipe**: 1411 DCH 100mm MiR 701 1.5um HMDS	

20.2 Exposure	Aligner: MA6	Align to flat. Hard contact **Exposure time**: 5.5 sec **Mask**: Top electrode	
20.3 Develop	TMAH UV developer	**Recipe:** DCH 100nm SP 60s	
20.4 Inspection	Optical microscope	Check pattern and alignment marks	
21 Etch top electrode			**Bonded wafers**
21.1 Al etch	Wet bench 05: Al etch	**Etch rate:** ~60-100nm/min **Time:** 1.5 min	
21.2 Si etch	ASE	Etch top plate (3 µm) to separate elements **Recipe:** prototype/shalolrc, 5 cycles, **Time:** 57 sec **Temp:** 20C	
21.3 Strip resist	Plasma Asher 1	**Process time:** 45 min **O_2:** 400 ml/min **N:** 70 ml/min **Power:** 1000W	If cannot clamp do Si etch
22 Dicing			**Bonded wafers**
22.1 Coat wafers	Spin coater: Gamma UV	Recipe: 3441 DCH100 5214E 4.2 µm	Protecting resist for the dicing process. Potentially use a mask to expose contacts.
22.2 Dicing out chips	Disco Saw	Dicing out chips	Disco Saw

B.1.2 Anodic bonding process flow

Process flow title			Revision
Anodic bonded CMUT with insulating nitride			**V2**
	Contact email rungra@dtu.dk	Contact person Rune Sixten Grass	Contact phone +4542280068
	Labmanager group	Batch name RCABCMUT 1	Date of creation	Date of revision 07-09-2021

Objective

Batch name: RCABCMUT

The purpose of the project is to fabricate Capacitive Ultrasonic Transducers using an anodic bonding process via a homemade SOI wafer, with addition of a nitride membrane.

Substrates

Substrate	**Orient.**	**Size**	**Doping/type**	**Polish**	**thickness**	**Box**	**Purpose**	**#**	**Sample ID**
Silicon	<100>	4”	n (Phos.)	DSP	350±15µm		Top plate	25	ON538-1
Boron glass		4”	p (Boron.)	DSP	500±10µm		Bottom plate	25	IB548

Comments:

Fabrication process for bottom plate:

Step	Heading	Equipment	Procedure	Comments
1	Preparation for Bottom electrode fabrication			**Bottom electrode wafers**
1.1	Wafer selection	Wafer box	Use the dedicated vacuum tweezer across the A-furnace stack	IB548 – All further handling of the wafers should be limited to only vacuum-tweezers unless otherwise unavoidable
1.2	Dehydration	Oven 250C	Place borofloat wafers in a metallic cassettes. **Time:** ≈2-3h	All borofloat wafers used for Bottom. Done to decrease the pump-down time for Temescal
2	Cr deposition as masking layer for cavity etch			**All Bottom electrode wafers**
2.1	Cr deposition by E-beam evaporation	Temescal	**Recipe:** Cr **Deposition rate:** 10 Å/s **Final thickness:** 50nm	All borofloat wafers.
3	Lithography process 1 – Cavities pattern			**All Bottom electrode wafers**
3.1	Spin coating	Gamma UV	AZ MiR 701 positive resist 2 µm with HMDS **Recipe:** 1421 - DCH 100mm MiR 701 2um HMDs **Cleaning wafer:** 0400 100mm Coater Clean	Clean spinner nozzle and run the dummy wafers – inspect dummy wafer in white light Stop: Large comets & particles
3.2	Exposure	MLA-3 aligner	**Mask:** CAV **Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm	See PP Mask Polarity This is a positive mask used as is.
3.3	Develop	TMAH UV developer	**Recipe:** 3008 DCH 100mm PEB120s@110C SP60s	
3.4	Inspection	Optical microscope	Check pattern	Stop: Delamination, defects in the center, resist on mask. Mask cleaning might be necessary.
3.5	Inspection	Dektak XT	Check height, write it down	Optional – indicator – we suggest to skip this, use time for optical inspection instead
4	Cr mask etch			**All Bottom electrode wafers**
4.1	Cr etch	Cr etch 18 in beaker	Cr etch 18 **Time:** 1:00 min	Easy to see when etch is finished as glass will be clear. Re-use Cr etch 18
4.2	Inspection	Optical Microscope	Ensure no under etch	Stop: Ref Kitty picture – underetch looks like blooming flowers at the corners
4.3	Inspection	Dektak XT	Check height, write it down	Optional – indicator– we suggest to skip this, use time for optical inspection instead
5	Cavity etching			**All Bottom electrode wafers**

5.1	Cavity etch	BHF plastic beaker	**Etch rate:** ≈24nm/min **Etch time:** 16.5 min **Target depth:** 400 nm	Preferable to batch etch to keep cavity depths the same
5.2	Inspection	Optical microscope	Check for defects	Stop: Check that there is no under-etch and that is no metal residue in cavities
5.3	Inspection	Dektak XT	Measure depth of the cavities	This measurement is not precise due to variation in thickness of resist. It does provide an indication.
6	Removal of masking layers			**All Bottom electrode wafers**
6.1	Resist strip	Resist strip wet bench	**Time:** 10 min with ultrasonic agitation	
6.2	Inspection	Dektak XT	Measure depth of cavities	
6.3	Cr removal	Cr etch 18 in beaker	**Etch time:** 1-2 minutes **Etch rate:** ~50-100 nm/min	Wafers need to be completely transparent when done
6.4	Cleaning-Piranha	Piranha in a beaker	Sulfuric acid H_2SO_4 (98%) and peroxide H_2O_2 (30%) in the ratio 4:1 **Temp:** 70-80C **Time:** 10 min	First add H_2SO_4 into a glass beaker then add H_2O_2.
6.5	Inspection	Optical microscope		See if pattern is good, and see whether all Cr is gone Stop: If the cavities are not well-defined squares - see Kitty picture
6.6	Inspection	Dektak XT		Final measurement of depth **Important** **Preferable measure on all wafers in the same spot.** **Contact pads in the wafer center**
7	Bottom electrode metal			
7.1	Dehydration	250C Oven	**Time:** 5 hours	
7.2	Deposit Ti/Au	Temescal	**Recipe:** Ti/Au **Final thickness Ti/Au:** 220 nm **Ti deposition rate:** 5 Å/s **Au deposition rate:** 2-3 Å/s	In this step, the Au thickness can be adjusted to fit a specific gap height. Low deposition rate to minimize particles
7.3	Inspection	Optical microscope	Darkfield inspection look for particles	Stop: If you see many large Au particles all over the wafer
8	Lithography process 2 – Bottom electrode			
8.1	Spin coating	Gamma-UV	**Recipe:** 3411 - DCH 100mm 5214E 1,5um HDMS	Clean spinner nozzle and run 2-3 dummy wafers – inspect dummy wafer in white light Stop: Large comets & particles
8.2	Exposure	MLA-3 aligner	**Mask:** BOT **Exposure dose:** 45 mJ/cm^2 **Defocus:** -2 **Laser:** 405 nm	See PP Mask Polarity This is a positive mask used as is. The polarity is reversed during bake and flood

				exposure to protect the metal in the cavities. Might be a good idea to do a dose test
8.3	Develop	TMAH UV developer	**Recipe:** 2002 DCH PEB 110 C 120 s	
8.4	Exposure	Aligner: MA6-2	**Exposure dose:** ≈198 mJ/cm^2 **Time:** 18 @ 11 mW/ cm^2	Flood exposure of wafer
8.5	Develop	TMAH UV developer	**Recipe:** 1002 DCH 100 mm SP 60 s	
8.6	Inspection	Optical microscope		Check that resist pattern is well defined inside cavities. Use dark field to make edges more visible.
9	Dry etching – Bottom electrode			
9.1	Etching Au	IBE/IBSD Ionfab 300	**Recipe:** Au acceptance –angle **Etch time:** 5:15 min for 10nm/210nm Ti/Au	Etch time will depend on the metal thickness. You don't want to much overetch. Time it with a dummy wafer.
9.2	Resist strip	Resist strip wet bench	**Time:** 15+ min with ultrasonic agitation This step might be necessary to repeat several times to remove resist (x3-5). Preferable keep the wafers submerged (and wet) as long as possible to avoid sticktion and redeposition of particles.	Resist will likely be stuck and take long time for some of the wafers. A short plasma ashing step before to soften the resist will likely also help
9.3	Inspection	Optical microscope		Check that pattern is well defined inside cavities. Use dark field to make edges more visible. Check that there is no resist (residue) left. Stop: If you see metal ribbon/filaments short-circuiting the bottom electrodes
9.4	Inspection	Dektak XT		Final measurement of gap height – preferably done on all wafers at the same point on the wafer: at the contact pad in the center Stop: Large particles within cavities

Fabrication process for anodic bonding of top and bottom plate:

Step	Heading	Equipment	Procedure	Comments
10	Cleaning before wafer bonding			**Top wafers**
10.1	Cleaning-RCA	RCA bench	Only RCA1	All top plates Flush both bath (x2) and cannisters with water and dump it immediately

			RCA1 is only used at the moment due to particle concern. Without HF dip, so oxynitride is not etched.
10.2 Cleaning-Piranha	Piranha in a beaker	Sulfuric acid H2SO4 (98%) and peroxide H2O2 (30%) in the ratio 4:1 **Temp:** 70-80C **Time:** 10-20 sec We are currently unsure if this step is needed at all. Underetch of electrodes is a risk factor.	All bottom plates. First add H2SO4 into a glass beaker then add H2O2. Consider if this step is necessary as the piranha might etch the Ti adhesion layer. If used, the solution should be stirred either with a hotplate or by hand. Only a short clean is likely needed. Alternatively acetone (maybe with US), IPA and water might be enough to remove residue.
11 Wafer bonding			**All wafers**
11.1 Alignment bonding	Aligner: MA6-2	MA6-2 is converted to alignment pre-bonder and the procedure in the manual is followed. PSOI silicon top wafer is loaded first, then the bottom glass substrate. **Alignment distance:** ≈100-150 µm	Put on a new pair of gloves on top of your others and wear a mask. If possible, pre-orientate wafer flats of both top and bottom in boxes. Take wafers out under HEPA filters to avoid particles. Smallest alignment distance depends on wafer bow and particles.
11.2 Anodic bonding	Wafer bonder 2	**Recipe:** CMUT/anodic bond 4 inch 600V align **Voltage steps:** -150V -300V, -600V, at 350°C Note down total charge	Bottom and top plate directly from the cleaning process. Stop: Major voids at the edges or on arrays. Surface should preferable be free from voids.
11.3 Inspection	Optical microscope		Look for defects, also near edges Stop: Major voids at the edge + center
12 Handle and box layer etching			**All bonded wafers**
12.1 Crystal bond	Hotplate: 90-110C	Dummy wafer is put facing up on tissue paper on hotplate. Crystal bond is applied from the center and out in a circular motion. Bonded wafer is placed on top with glass-side facing down. Stack is removed from hotplate and cooled down. **Recipe:** Standby, Pins down	Spread crystal bond evenly and do not apply too much, so that it spills out. After cooling, check that wafer stack is bonded.
12.2 Nitride etch	ASE	Etch nitride layer away from top **Recipe:** MEMS/MAENGSiN **Etch time:** 12 to 17 min at 20 °C, with 200 nm nitride	Visible color change is seen when etch is completed. Color should resemble Si
12.3 Crystal de-bond	Hotplate: 90-110C	Bonded stack is placed on hotplate and device wafer is slid off dummy wafer using a tweezer (or by pushing the edge with your finger).	

		Both wafers are wiped with wet napkins and sprayed with a water gun to remove wax. **Recipe:** Standby, Pins down	
12.4 Oxide etch	BHF	Plastic beaker inside fumehood Etch of thin oxide buffer layer. **Etch rate:** 75 nm/min. **Etch time:** approx. 2-5 minutes	Surface is hydrophobic when etch is done Re-use for step 12.6 and 12.8
12.5 Poly-Si layer	Si KOH etch 3	Etch top (not useable) device layer away. **Process 4:** 90C **Etch time:** 5-10 min for a thickness of 3 µm	Time depends on the thickness of the poly-Si on the PSOI wafer. Will stop bubbling. Remember 40 min heat-up time
12.6 Oxide etch	BHF	Plastic beaker inside fume hood Etch of non-useable box layer. **Etch rate:** 75 nm/min. **Etch time:** 6 minutes for a thickness of 400 nm	Time depends on the thickness of the oxide on the PSOI wafer. Surface is hydrophobic when etch is done
12.7 Si etch	Si KOH etch 3	Etch handle layer away **Process 4:** 90C **Etch rate:** 1.7µm/min **Etch time:** 3 hours 15 minutes for a thickness of 350 µm If concentration is adjusted at the start of the process the etch might take longer time and running at 90 °C for longer is preferred.	This is a critical step of the process flow. It is recommended to check how the wafers look regularly during the step, also removing it from the bath to check. Keep an eye on the wafer in the last 30 min. Alternatively use process 3: 80C after 2 h 30 min. The concentration might change during the long etch and increase etching time needed Stop: If plate defects occur. Assess whether the main arrays are salvageable.
12.8 Oxide etch	BHF	Plastic beaker inside fumehood Etch of not useable box layer. **Etch rate:** 75 nm/min. **Etch time:** 6 minutes for a thickness of 400 nm	Time depends on the thickness of the oxide on the PSOI wafer. Surface is hydrophobic when etch is done
12.9 Cleaning-Piranha	Piranha in a beaker	Sulfuric acid H_2SO_4 (98%) and peroxide H_2O_2 (30%) in the ratio 4:1. **Temp:** 70-80C	First add H2SO4 into a glass beaker then add H2O2. To remove potassium ions and more.
13 Lithography – Alignment mark access			**All bonded wafers**
13.1 Coat wafer	Gamma UV	**Resist:** AZ MiR 701 positive resist **Recipe:** 1411- DCH 100mm MiR 701 1.5 um HMDS	Clean spinner nozzle and run 1-2 dummy wafers. Stop: Large comets & particles
13.2 Exposure	MLA-3 aligner	**Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm **Mask:** Draw mode	Contrast is not very good in this step. Squares or circles can be drawn using the overhead camera in MLA.

13.3 Develop	TMAH UV developer	**Recipe:** 3001 DCH 100mm PEB60s@110C+SP60s	
13.4 Inspection	Optical microscope	Check pattern and alignment marks.	Ensure that resist covers electrodes uniformly
14 Etch - Alignment mark access			**All bonded wafers**
14.1 Crystal bond	Hotplate: 90-110C	Dummy wafer is bonded to glass-side of device wafer. **Recipe:** Standby, Pins down	After cooling, check that wafer stack is bonded. It might not be necessary at this step to do crystal bonding. The ASE might clamp the wafers fine.
14.2 Device layer etch	ASE	Dry etching through Poly Si stopping on nitride. 4-5 cycles, **Recipe:** shallolr	
14.3 Crystal de-bond	Hotplate: 90-110C	Bonded stack separated on hotplate and cleaned with water. **Recipe:** Standby, Pins down	Remaining wax is likely removed in plasma asher 1
14.4 Resist strip	Plasma asher 1	Photoresist stripping **Pressure:** 0.8-1.0mbar. **Gas:** Mixture of O2 and N2. **Power:** 1000watts. **Time:** 30-45 min	
15 Top electrode deposition 1			**All bonded wafers**
15.1 Deposition Al	Temescal	**Recipe:** Al **Final thickness Al:** 200nm **Deposition rate Al:** 10 Å/s	The deposition rate looks to be fluctuating during deposition, however, the metal layer looks fine.
16 Lithography – Top electrode			**All bonded wafers**
16.1 Coat wafer	Gamma UV	**Resist:** AZ MiR 701 positive resist **Recipe:** 1421 - DCH 100mm MiR 701 2um HMDS	Clean spinner nozzle and run 1-2 dummy wafers. Spin coat as soon as possible after metal deposition Stop: Large comets & particles
16.2 Exposure	MLA-3 aligner	**Mask:** OPE-Poly **Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm	See PP Mask Polarity This is a positive mask used as is.
16.3 Develop	TMAH UV developer	**Recipe:** 3008 DCH 100mm PEB120s@110C SP60s	
16.4 Inspection	Optical microscope	Check pattern and alignment marks.	Stop: If bottom electrode pad openings are not well-defined
17 Etch – Opening to bottom electrode			**All bonded wafers**
17.1 Al wet etch	PES solution in beaker	Etch of pure aluminum. **Etch rate:** ≈45-60nm/min. **Etch time:** ≈6 min.	Mix the solution with the wafer holder when starting the etch, as it is quite viscous. Visual feedback when done etching

17.2 Inspection	Optical microscope	Inspection of aluminum etch.	Stop: If metal is not etched. Check in microscope and continue etch is necessary. A bit of underetch is okay
17.3 Resist strip	Plasma asher 1	Photoresist stripping **Pressure:** 0.8-1.0mbar. **Gas:** 400 O2 and 70 N2. **Power:** 1000watts. **Time:** 45 min	
17.4 Crystal bond	Hotplate: 90-110C	Dummy wafer is bonded to glass-side of device wafer. **Recipe:** Standby, Pins down	After cooling, check that wafer stack is bonded.
17.5 Device layer etch	ASE	Dry etching through Poly Si. 5 cycles, **Recipe:** shallolr	
17.6 Crystal de-bond	Hotplate: 90-110C	Bonded stack separated on hotplate and cleaned with wet tissue paper. **Recipe:** Standby, Pins down	Careful not to get water of the front-side. Remaining wax is removed in plasma asher 1
18 Top electrode metal			**All bonded wafers**
18.1 Deposit Al	Temescal	**Recipe:** Al **Final thickness Cr:** 800 nm **Al deposition rate:** 10 Å/s	The bottom electrode cavities are plugged with aluminium in this step. Clean the wafers with a nitrogen airgun before this step
18.2 Inspection	Optical microscope	Inspection of plugged cavities	
19 Lithography – Separation of top electrodes			**All bonded wafers**
19.1 Coat wafer	Gamma UV	**Resist:** AZ MiR 701 positive resist **Recipe:** 1411- DCH 100mm MiR 701 2 um HMDS	Clean wafers with a nitrogen airgun before this step. Clean spinner nozzle and run 1-2 dummy wafers. Stop: Large comets & particles.
19.2 Exposure	MLA-3 aligner	**Exposure dose:** 320 mJ/cm^2 **Laser:** 405 nm **Defocus:** 0 **Mask:** TOP	See PP Mask Polarity This mask needs to be reversed, so the metal can be exposed and etched to separate top from bottom electrodes.
19.3 Develop	TMAH UV developer	**Recipe:** 3008 DCH 100mm PEB120s@110C SP60s	
19.4 Inspection	Optical microscope	Check pattern and alignment marks for particles.	Stop: Large comets & particles.
20 Etch – Top electrode metal			**All bonded wafers**
20.1 Etching Au	IBE/IBSD Ionfab 300	**Recipe:** Al etch with resist **Etch time:** ≈50 min for 1000 nm Al Split the etch up in 2-3 steps and let the wafer cool just a bit between etches.	You can time the etch with a dummy wafer. Bulk area might be etched fine after 40 min, but in-between electrodes still have metal requiring 10 min extra.

20.2 Inspection	Optical microscope	Inspect that the top electrodes are separated	
20.3 Crystal bond	Hotplate: 90-110C	Dummy wafer is bonded to glass-side of device wafer. **Recipe:** Standby, Pins down	After cooling, check that wafer stack is bonded.
20.4 Plate etch	ASE	Dry etching through Poly Si. 5 cycles, **Recipe:** shallolr	
20.5 Inspection	Optical microscope	Inspect that the top electrodes are separated down to the underlying nitride layer/glass	
20.6 Crystal de-bond	Hotplate: 90-110C	Bonded stack separated on hotplate and cleaned with wet tissue paper and water gun. **Recipe:** Standby, Pins down	Careful not to too much water of the front-side. Remaining wax is removed in plasma asher 1
20.7 Resist strip	Plasma asher 1	Photoresist stripping **Pressure:** 0.8-1.0mbar. **Gas:** 400 O2 and 70 N2. **Power:** 1000watts. **Time:** 30-45 min	
20.8 Inspection	Optical microscope	Final inspection (particles and short-circuits) before taking wafers out of cleanroom	

B.1.3 PSOI process flow

Process flow title			Revision
Poly-silicon-on-insulator (PSOI) fabrication process			**1.0**
	Contact email kitste@dtu.dk	Contact person Kitty Steenberg	Contact phone Click here to enter text.
	Group MEMS Applied-Sensors	Batch name PSOI	Date of creation 01-02-2022	Date of revision 01-02-2022

Objective

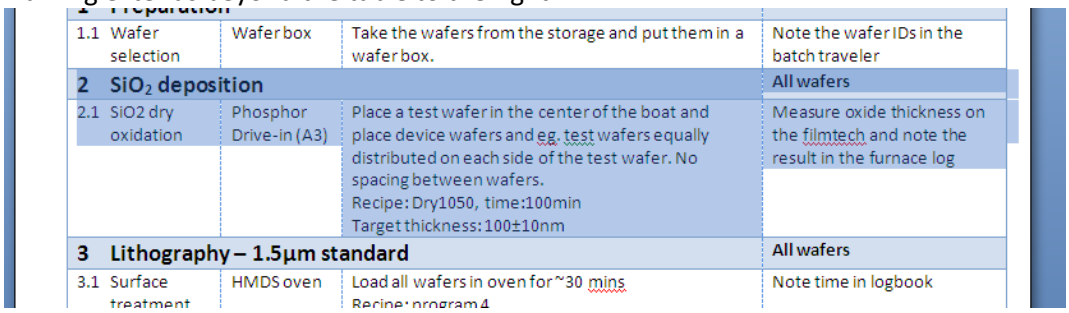
Batch name: **Error! Reference source not found.**

This is an example process flow to be used as a template. It should contain

- The objective of the process.
- Substrates/samples used in the flow. Both actual samples to be processed (device wafers) and monitor samples for the different process steps
- The Process flow main processes and steps
- Recommended: Figures illustrating the sample before and after each main process step.

How to use this template (works only with the .dotx template file)**:**

- Fill out the fields in the heading!
- Add process steps in the following way:
  1. Select a process step header and one or more detail steps. Make sure to select the whole line so that the marking extends beyond the table to the right.



1.1	Wafer selection	Wafer box	Take the wafers from the storage and put them in a wafer box.	Note the wafer IDs in the batch traveler
2	**SiO_2 deposition**			**All wafers**
2.1	SiO2 dry oxidation	Phosphor Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Dry1050, time:100min Target thickness: 100±10nm	Measure oxide thickness on the filmtech and note the result in the furnace log
3	**Lithography – 1.5µm standard**			**All wafers**
3.1	Surface treatment	HMDS oven	Load all wafers in oven for ~30 mins Recipe: program 4	Note time in logbook

  2. Press <crtl> C to copy the part.
  3. Select the step header where you want to insert the new step. Again make sure to select the whole line.
  4. Press <ctrl> V to insert to new step.
- The Content (TOC) on the last page is an option, but can give a nice overview for very long process flows.

Substrates

Substrate	**Orient.**	**Size**	**Doping/type**	**Polish**	**thickness**	**Box**	**Purpose**	**#**	**Sample ID**
Silicon	<100>	4”	n (Phos.)	DSP	350±15µm		Top plate	25	ON538-1

Comments: Number of wafers is for illustration only

Step	Heading	Equipment	Procedure	Comments
1	Preparation			**All wafers**
1.1	Wafer selection	Wafer box	Take the wafers from the storage and put them in a wafer box.	Note the wafer IDs and box: WAFR_YYYYMMDD_PSOI_XX
2	Deposition SOI			**All wafers**
2.1	RCA clean	RCA (4",6")	All wafers including test wafers should be RCA cleaned	
2.2	SiO2 dry oxidation – BOX layer	Phosphor Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Dry1100, time:12 h 30 min Target thickness: 500 nm	Approximately 500 nm or approximately 12 hours and 30 minutes. The 500 nm is a thickness that previously has been sufficient for many fabrications. However, if the handle wafer is removed entirely by dry etching, it might be a good idea to use a thicker (wet) oxide on the order of 1 µm, to ensure acceptable etch stopping properties
2.3	Measure thickness	Filmtek and VASE	Measure thickness on the Filmtek and VASE and note the result with MSE/RSME and recipe used Only test wafer!	Save this data so that it can be fitted for the model when measuring Poly-Si
2.4	Poly-Si deposition – Device layer	LPCVD Poly-Si (4") (B4)	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Fill up with dummy wafers for boron doped poly. Recipe: POLYBOR, time: 1 h 40 min Target thickness: 1 µm	Deposition of device layer. Remember, you are not allowed to deposit continuously for more than 3 hours (corresponding to approximately 2 µm). Hence, if you want 3 µm poly it is advantageous deposit 2×1.5 µm rather than first 2 µm and then add 1 µm on top. The reason being the thin film measuring equipment (FilmTek, Ellipsometer) becomes less precise for large film thicknesses
2.5	Measure thickness	Filmtek and VASE	Measure thickness on the Filmtek and VASE and note the result with MSE/RSME and recipe used Filmtek recipe: PolySi(3my) on SiO2 thick PSD2 Vase recipe: PSOI_model	Use the SiO2 data to fit the BOX layer
3	Chemical Mechanical polishing (CMP)			**All wafers**
3.1	Storage during CMP	Plastic Beaker	Put wafers in a plastic beaker filled with water and use a holder that fits all wafers you want to polish in the subsequent step. Transport the beaker to the Polisher/CMP	Make a chemical note stating water
3.2	Polishing	CMP	Recipe: cmut_kitste Time: 1 min 30 s or 3 min – this is adjusted in step 2 which has a 13 s off set for the carrier to reach to	Insert shim's and napcon to approx. + 30 µm and measure CNESW note down

		plate. Therefore, 1 min and 30 s polishing is set to be 1 min 43 s in step 2	and comment concave/convex Brush conditioning should be done right before polishing Take the wafers from the water filled beaker into the CMP, and afterwards put the now polished wafer back into the water filled beaker. Repeat this process for all the wafers in your holder. Be aware of different hydrophilic properties on the surface after the polishing, such variation can imply particle contamination. Hence, check the wetting properties after the clean, and verify these properties are uniform across the wafer surface.
3.3 Piranha	Beaker 1	Recipe: H2SO4:H2O2 in the ratio 4:1. Time: 10 min	First Sulfuric acid (H2SO4) and then hydrogen peroxide (H2O2) in the ratio 4:1. We have our own beaker for this on our shelf called Piranha 1.
3.4 Rinse	QDR	Recipe: 1	Use the rinse program with spray cycles. Do not dry the wafers, transport them to Oxide etch 2: BHF while they are wet
3.5 Oxide etch	BOE in beaker/ Wetbench	Time: 5 min for Poly-Si	Use the beaker used for storage
3.6 Rinse	QDR	Recipe: 1	Use the rinse program with spray cycles. Do not dry the wafers.
3.7 Piranha	Beaker 2	Recipe: H2SO4:H2O2 in the ratio 3:1. Time: 10 min	First Sulfuric acid (H2SO4) and then hydrogen peroxide (H2O2) in the ratio 3:1. We have our own beaker for this on our shelf called Piranha 2.
3.8 Rinse	QDR	Recipe: 1	Use the rinse program with spray cycles.
3.9 Spin dry	Spin dryer		Leave in for 30 s when program is stopped to dry completely.
4 Characterization			**All wafers**
4.1 Particle Scan	KLA Tencor SurfScan 6420	Recipe: 4IN_POLY_SI	Ask Patama or Kitty to do this

4.2	Measure thickness	Filmtek and VASE	Measure thickness on the Filmtek and VASE and note the result with MSE/RSME and recipe used Filmtek recipe: PolySi(3my) on SiO2 thick PSD2 Vase recipe: PSOI_model	Try to get the MSE down to 60-70, save the data to optimize the model fit later
4.3	Measure roughness	AFM Icon-1	QNM tapping mode Scan size: 1-2 µm, 1 Hz Rq < 1 nm Rmax < 5-10 nm	Note down: material and CMP process along with Rq XX nm, Ra XX nm, Rmax XX nm Measure at least C and N/S/E/W Valleys are ok, peak no-go
5	Oxy nitride			
5.1	RCA clean	RCA (4",6")	All wafers including test wafers should be RCA cleaned	
5.2	SiO2 dry oxidation	Furnace (C1) - Anneal-oxide	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Recipe: DRY1000, Ox time: 15 min, anneal 20 min Target thickness: 20 nm	
5.3	Nitride deposition	Furnace (B2) - LPCVD Nitride 4"	Recipe: Nitride4, Time: 60 min Target thickness: 200 nm	
5.4	SiO2 wet oxidation	Furnace (C1) - Anneal-oxide	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Recipe: WET1100, Ox time: 3 hours, anneal 20 min Target thickness: 920 nm	
6	Structuring the nitride			
6.1	Spin coat	Gamma UV	1421 - DCH 100mm MiR 701 2um HMDS	
6.2	Exposure	MLA3	Dose 320, Defoc 0, Exp time 7 min	
6.3	Developer	TMAH UV-Lithography	3001 DCH 100mm PEB60s@110C SP60s	
6.4	Dry etch Nitride	AOE	Recipe: SiO2_res Time: 3 min Temp: 0 C	
6.5	Resist strip	Plasma asher 2	45 min, O2 400 ml/min, N2 70 ml/min, 1000 W	

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Chapter **C**

Paper A - 188+188 Row-Column Addressed CMUT Transducer for Super Resolution Imaging

188+188 Row–Column Addressed CMUT Transducer for Super Resolution Imaging

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Published in:
Proceedings of the IEEE International Ultrasonic Symposium 2019

Link to article, DOI:
10.1109/ULTSYM.2019.8925940

Publication date:
2019

Document Version
Peer reviewed version

188+188 Row–Column Addressed CMUT Transducer for Super Resolution Imaging

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***Abstract*—A capacitive micromachined ultrasonic transducer (CMUT), 8 MHz resonance frequency, $\lambda/2$ cell pitch 188+188 row-column addressed (RCA) array for super resolution imaging is presented. The top- and bottom electrode design features a zig-zag shaped pattern to increase the active cell area for fixed plate thicknesses. The RCA CMUT has been fabricated utilising a deposit, remove, etch, multistep (DREM) process to fully separate the bottom electrodes electrically as well as anodic bonding the array to an insulating borosilicate glass wafer. Linear test elements have been characterized. Electrical measurements show a center frequency of approximately 5.5 MHz and a coupling coefficient of 7.8% for -80 V DC bias and 50 mV AC. Acoustic measurements made in immersion with a single cycle 4 MHz pulse with a -90 V DC bias demonstrate that the fabricated CMUT arrays can emit broadband ultrasound pulses.**

I. Introduction

The number of interconnections required to perform 3D ultrasound imaging can be greatly reduced by applying a row-column addressed (RCA) scheme compared to a conventional fully populated matrix (FPM) array [1]–[6]. Conventional FPM arrays require N^2 interconnects, where N is the number of elements in the elevation and azimuth direction. By applying a RCA scheme the same number of channels can be obtained by only $2N$ interconnections. However, the resolution capability is proportional with N, and it is therefore desirable to design 3D transducers with as many channels as possible. The linear scaling law of RCA arrays facilitates 3D transducers with a high number of channels, that otherwise would be exceedingly impractical for FPM arrays. The high achievable resolution with the RCA scheme can be utilized in super resolution imaging to more precisely determine the positions of injected micro bubbles in vascular structures.

This work presents the development of a $188 + 188$ element RCA transducer array based on the capacitive micromachined ultrasonic transducer (CMUT) technology. The CMUT cavities are defined by a local oxidation of silicon (LOCOS) [7] process and a deep silicon etch combined with a silicon etch back and an anodic bonding of a glass wafer are utilized to define the bottom electrodes. This process therefore only utilizes one SOI (Silicon On Insulator) wafer for the top plate, and a standard silicon wafer for the bottom electrode. The LOCOS process allows for tightly controlled CMUT cell dimensions and well-defined cavity depths due to the predictability of the grown oxide thicknesses. This technique combined with the advantage from a deposit, remove, etch, multistep (DREM) process and anodic bonding results in that the substrate coupling, which would otherwise lower the receive sensitivity of the bottom electrodes, are avoided as the glass wafer is insulating [8].

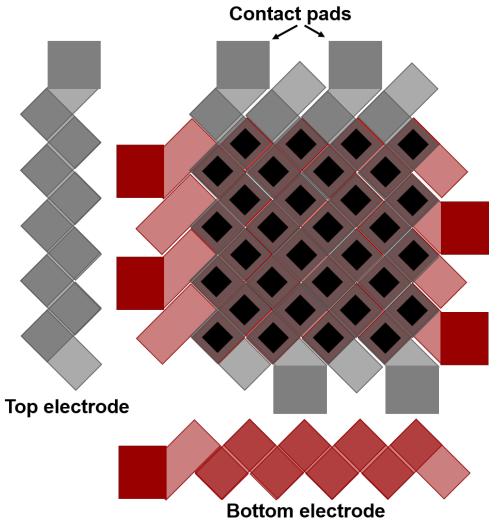


Fig. 1: Sketch of a 4+4 row-column CMUT array structure where both the bottom and top electrodes are designed with a zig-zag shaped pattern, with the cells positioned in the overlapping segments.

II. Design & Fabrication

A. Design

The RCA CMUT array is designed having 188+188 elements with a pitch of $\lambda/2$ ($95\,\mu\mathrm{m}$), an operating frequency of $8\,\mathrm{MHz}$, and a plate thickness of $3\,\mu\mathrm{m}$. The wafer layout also includes linear CMUT arrays for testing with a slightly different pitch and radii compared to the RCA CMUT arrays. The CMUT cells are designed to be $50\,\mu\mathrm{m}$ wide whereas the linear test elements used in this work are $70\,\mu\mathrm{m}$ wide. The pull-in voltage is designed to be at $220\,\mathrm{V}$. The row and column design for this chip has a zig-zag pattern (illustrated in Fig. 1) to increase the active area of cells for a fixed plate thickness with a factor two compared with a typical straight row-column design [9].

B. Fabrication

The fabrication of the CMUT array is based on the LOCOS process, a DREM trench etch process and two bonding steps (fusion and anodic bonding). The LOCOS process is a well known method where a silicon substrate is masked off, blocking the diffusion of oxygen, and selectively oxidized. The masking material used is silicon nitride, Si_3N_4.

In this work, a combination of a long DREM etch, a backside etch of silicon, and an anodic bonding of a borosilicate glass wafer is performed to separate the bottom elements electrically and to avoid capacitive substrate coupling. The DREM etch is similar to a conventional Bosch process but consists of three finely tuned steps which to a higher degree preserves the deposited fluorocarbon layer everywhere except in the bottom of etched trenches. This process protects the masking material resulting in an infinite selectivity, creating uniform etching scallops of the sidewalls and facilitates deeper etches [10].

The fabrication process for the RCA CMUT array is similar to previous presented processes [11] and all the steps are carried out in the cleanroom at DTU Nanolab. The main steps which are in focus in this work are illustrated in Fig. 2.
The starting point to arrive at step 1, is a silicon wafer with a resistivity of $<0.025\,\Omega\,\mathrm{cm}$, which is thermally oxidised at $1100\,^{\circ}\mathrm{C}$ under dry conditions to grow a $400\,\mathrm{nm}$ SiO_2 layer. This is followed by a deposition of a $55\,\mathrm{nm}$ stoichiometric Si_3N_4 layer and a $100\,\mathrm{nm}$ polycrystalline silicon layer in LPCVD (Low Pressure Chemical Vapour Deposition) furnaces. The polysilicon layer and subsequently the silicon nitride layer are patterned with a photolithographic process combined with dry and wet etching, leaving silicon nitride as masking pads on silicon oxide where the CMUT cavities will be formed.

From this step the wafer is again patterned to open up the silicon oxide, exposing the silicon substrate. The DREM etch is then performed at a temperature of $-19\,^{\circ}\mathrm{C}$ using a reactive deep ion etching (DRIE) tool, capable of performing this modified Bosch process, for a final depth of $110\,\mu\mathrm{m}$.

The result is a structure similar to step 1 in Fig. 2, where a 45° cross-section of the structure illustrated in Fig. 1 is shown. Depicted are four (black) silicon nitride pads used in the LOCOS process which have been structured on (dark gray) silicon oxide on (gray) silicon. The $110\,\mu\mathrm{m}$ deep DREM etch into the silicon is separating the cells into groups of two. Fig. 3 shows a cross-sectional scanning electron microscope (SEM) image of two etched DREM trenches in silicon, with a depth of $113\,\mu\mathrm{m}$.

A thermal oxidation is performed under wet conditions at $1100\,^{\circ}\mathrm{C}$ for a total post SiO_2 thickness of around $840\,\mathrm{nm}$, forming the CMUT cavities (step 2). A SOI wafer is direct bonded by fusion bonding to the structure in step 2 to enclose the cavities (step 3).

To fully separate the bottom electrodes, the wafer stack is flipped and dry etched by a RIE process from the backside, thinning down the substrate by $\approx 400\,\mu\mathrm{m}$. The wafer backside after etching can be seen in the microscope and SEM image in Fig. 4 and 5a respectively. It can be seen from the image,

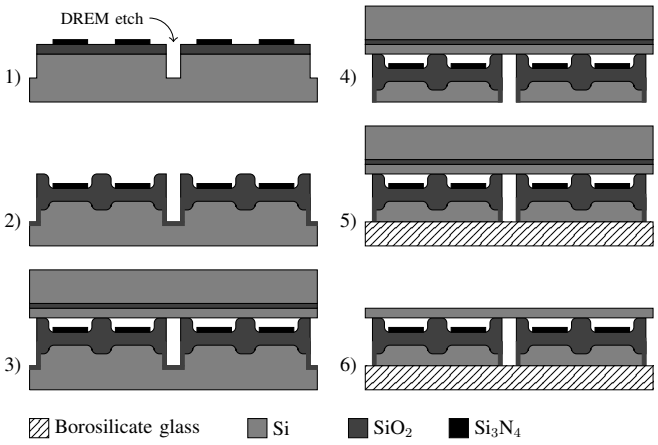


Fig. 2: Cleanroom fabrication process for the row-column CMUT array. Only the processes comprising the DREM etch, LOCOS oxidation and fusion- and anodic bonding are depicted.

that the dry etching process has etched past the extend of the original $113\,\mu\mathrm{m}$ trench, exposing the oxide covering the inside of the trench. These zig-zag oxide structures are left standing due to the high selectivity of silicon to silicon oxide.

To reduce the roughness of the backside surface for anodic bonding and remove the SiO_2 structures present in Fig. 4, the wafer is polished using a Logitech CM62 Orbis CMP (Chemical Mechanical Polishing) machine [12], the result is shown in Fig. 5b.

A borosilicate glass wafer is then bonded by anodic bonding to the backside at a temperature of $350\,^{\circ}\mathrm{C}$ using a three step voltage ramp (300 V/600 V/800 V). The handle- and BOX layers are then removed from the SOI wafer by dry etching (step 6) leaving the top plate bonded to the cavities. To finalise the CMUTs, first, access to the bottom substrate electrodes are etched through the plate and post SiO_2 by using a patterned hard $100\,\mathrm{nm}$ thick aluminium mask. Then, after removing the mask, the top- and bottom electrode contact pads are metallised by depositing and patterning $400\,\mathrm{nm}$ aluminium, as well as the underlying silicon by a RIE process. The RCA CMUT arrays are then diced from the wafer.

III. Characterization

A. Electrical

The electrical response of the CMUT array has been tested by performing impedance measurements on a linear test element. The measurements were made using an Agilent 4294A Precision Impedance Analyzer with a varying DC voltage and an AC voltage of $50\,\mathrm{mV}$.

Fig. 6 shows the measured magnitude and phase of impedance for frequencies up to $10\,\mathrm{MHz}$. The applied DC bias voltage has been varied between $-60\,\mathrm{V}$ and $-80\,\mathrm{V}$, where the latter value correspond to approximately 90% of the CMUT pull-in voltage ($-90\,\mathrm{V}$).

In the magnitude plot four clear resonant peaks are seen for the corresponding voltage values. The spring-softening effect

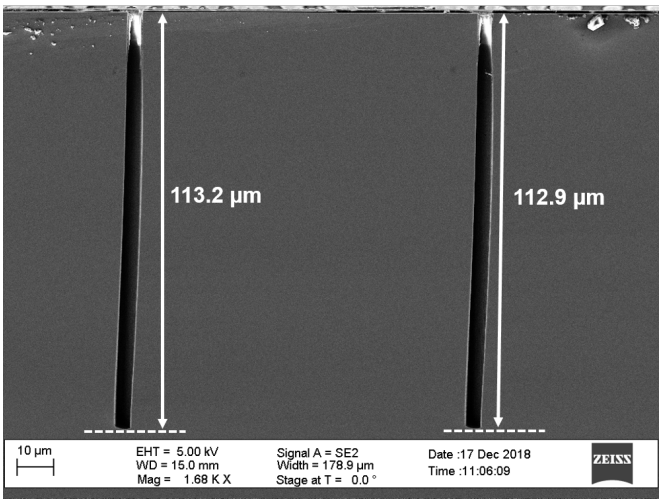


Fig. 3: Scanning electron microscope cross-sectional image of silicon wafer from step 1 in the fabrication process (Fig. 3). The etch depth of $113\,\mu\mathrm{m}$ is acquired after performing multiple deposit and removal cycles.

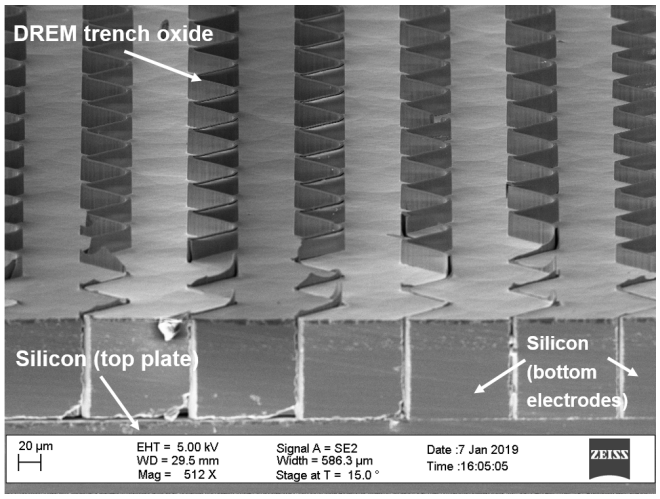
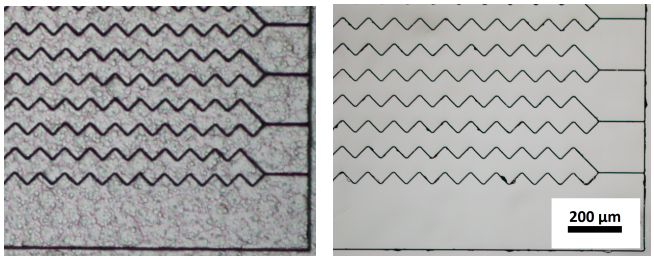


Fig. 4: Scanning electron microscope cross-sectional image of wafer backside from step 4 in the fabrication process (Fig. 2) before polishing. The bottom electrodes are seen as zig-zag shaped DREM etch separated silicon segments.

is also observed by the shift to lower resonance frequencies in the range from $\approx 6.3\,\mathrm{MHz}$ to $\approx 5.5\,\mathrm{MHz}$, by increasing the DC bias. Since these test elements have wider cell diameters the resonance frequency is also lower than the expected $8\,\mathrm{MHz}$ for the RCA CMUT array. The electromechanical coupling coefficients given by equation $k^2 = (1-(f_{res}/f_{ares})^2)\times 100\%$, are estimated to be 3.7%, 3.8%, 3.9%, 4.4%, and 7.8%, where f_{res} and f_{ares} are the resonance and anti-resonance frequencies respectively. The phase angle is also constant at $-90°$ except for around the resonant frequency in correspondence with



(a) (b)

Fig. 5: Optical images of the wafer backside from step 4 in the fabrication process before anodic bonding is carried out (Fig. 2). (a): After the backside RIE process has separated the bottom electrodes. (b): After polishing the backside using a CMP process.

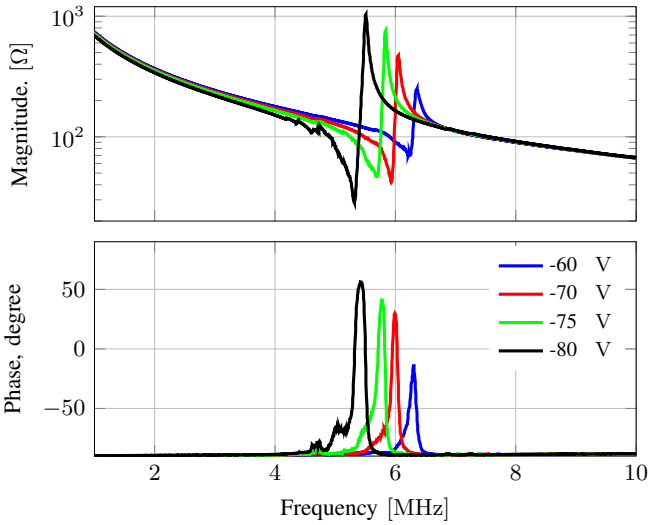


Fig. 6: Impedance measurements of the fabricated linear CMUT test array at four different DC biases with a $50\,\mathrm{mV}$ AC bias. The expected spring softening effect is observed for increased DC magnitude.

typical CMUT capacitance behaviour.

B. Acoustic

To acoustically verify the CMUTs' ability to transmit pressure, the array is mounted on a printed circuit board (PCB) and the contact pads are wire-bonded to the board. A dam of acrylic glass is then glued onto the PCB around the array and filled with a polydimethylsiloxane (PDMS) with an approximate thickness of $2\,\mathrm{mm}$. This serves to electrically insulate the elements from the water. The encapsulation procedure is described in [13].

The acoustic signal from the linear CMUT test array has been measured using a HGL-0400 hydrophone connected to a AC-2010 pre-amplifier (Onda Corporation, CA, USA) in immersion aligned $4\,\mathrm{cm}$ from the transmitting CMUT array. The elements were actuated with a single cycle $10\,\mathrm{V}$ peak-to-peak $4\,\mathrm{MHz}$

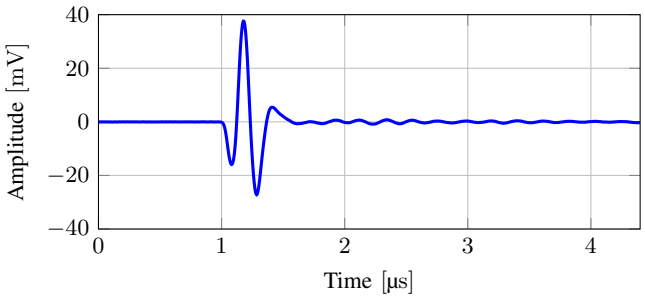


Fig. 7: Hydrophone signal from for linear CMUT test array. A single-period, 4 MHz sinusoidal pulse is used to excite the array.

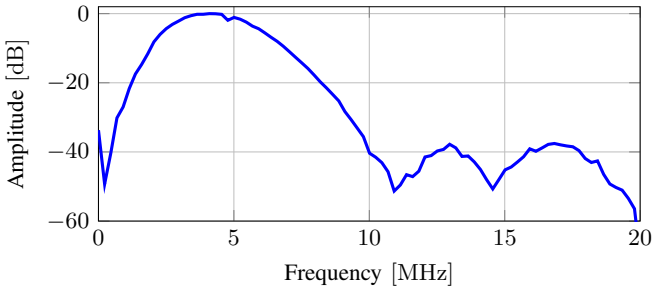


Fig. 8: The amplitude spectrum of the received hydrophone signal for the linear CMUT test array.

sinusoidal pulse with a DC bias of $-90\,\mathrm{V}$ and the signal from the hydrophone is sampled by a 5442D oscilloscope from PicoScope using 12 bit resolution and a sampling frequency of 62.5 MHz.

Fig. 7 shows the measured hydrophone signal as a function of time and Fig. 8 the amplitude spectrum of the signal. Both show expected typical CMUT characteristics. The bandwidth read off at $-3\,\mathrm{dB}$ is determined to be 68% and is limited by the bandwidth of the pulse.

The substrate ringing due to the silicon substrate and bonded glass wafer is observed in the spectrum at $\approx 5\,\mathrm{MHz}$ which is in agreement with the expected frequency.

IV. Conclusion

This paper presented an alternative fabrication method of RCA CMUTs. The method utilises a DREM process combined with an anodicly bonded glass wafer to fully separate the bottom electrodes of the arrays electrically. This ultimately leads to a reduced substrate coupling. Characterization during the fabrication process shows the expected mechanical separation of the elements by etching and backside polishing in preparation for bonding. Electrical and acoustical characterization shows typical CMUT behaviour. Resonant frequencies were measured between $6.3\,\mathrm{MHz}$ and $5.5\,\mathrm{MHz}$ with DC biases from $-60\,\mathrm{V}$ to $-80\,\mathrm{V}$ with corresponding electromechanical coupling coefficients from 3.7% to 7.8%.

From the hydrophone measurements in immersion substrate ringing is observed at $5\,\mathrm{MHz}$ and a pulse bandwidth is estimated to be 67.7%.

In conclusion, the fabrication methods and row-column design used, which combines tight control of cavity dimensions by LOCOS and electrical insulation by anodic bonding and DREM, results in a functioning CMUT with a good electrical and acoustical response. The next step will be measuring on a RCA CMUT. A device with these specifications will by a possible candidate for the use in super resolution imaging.

Acknowledgment

The authors would like to thank Chantal Silvestre for her help with the DREM process. This work is financially supported by Innovation Fund Denmark (7050-00004B) and by BK Medical, Herlev, Denmark.

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Chapter **D**

Paper B - Wafer Level Characterization of Row-Column Addressed CMUT Arrays

2019 IEEE International Ultrasonics Symposium (IUS)
Glasgow, Scotland, October 6-9, 2019

Wafer Level Characterization of Row-Column Addressed CMUT Arrays

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***Abstract*—This paper presents a measurement methodology for wafer level characterization of row-column addressed (RCA) capacitative micromachined ultrasound transducers (CMUT). Characterization of a 62+62 element RCA CMUT is presented. To facilitate wafer level electrical characterization measurements between adjacent electrodes can be used to characterize the device. This allows for determination of the individual element capacitance. Current-voltage measurements between adjacent top or bottom electrodes provides valuable information about process yield.**

I. Introduction

Row-Column Addressed (RCA) capacitive micromachined ultrasonic transducers (CMUTs) are an attractive alternative to fully-populated matrix arrays, as they provide volumetric imaging with a greatly reduced number of electrical connections [1], [2]. Furthermore, they can be mass-produced on wafer scale using silicon process technology which allows for tight control of the dimensions. RCA CMUTs have been fabricated using various fabrication techniques including fusion bonding, anodic bonding and surface micromachining. Several devices have been presented including a 32+32 RCA CMUT chip based on a fusion bonding process with silicon nitride [3], a RCA CMUT chip fabricated using a surface micromachining process [4], a 32+32 anodically bonded RCA CMUT chip [5], a BCB based RCA CMUT chip [6], a 62+62 fusion bonded RCA CMUT probe [7], and a 120+120 element RCA CMUT probe fabricated using sacrificial release microfabrication [8]. As the resolution of the RCA transducer scales linearly with the number of elements the current trend is to increase the number of elements and fabricate large area chips.

In this work we present wafer level characterization of a local oxidation of silicon (LOCOS, origanally used by [9] for CMUTs) based 62+62 element RCA CMUT transducer as shown in Fig. 1. Manual electrical characterization of a transducer having 124 element becomes a tedious job and automated tests need to be implemented on wafer scale, i.e. electrical wafer level test can be used to ensure that only fully functional arrays are used for probe manufacturing and to provide valuable information during process optimization.

Conventional linear arrays are easily characterized electrically using the two terminals on the device, e.g. the capacitance of an element can be measured directly using the two terminals of the element. However, RCA arrays cannot be measured in the same way as e.g. a measurement of the capacitance of a row-element will require that all columns are shorted and vice versa. This is not easily done on commercial wafer probers where micro manipulators are used to place probe needles or a probe card in fixed positions. During wafer level characterization the probe needles remain fixed and the wafer is automatically moved to perform the measurements needed. The objective of this work is therefore to present a methodology for characterization of RCA CMUT arrays with the aim of providing an automated and non-destructive wafer level test to determine if an array is fully functional or not.

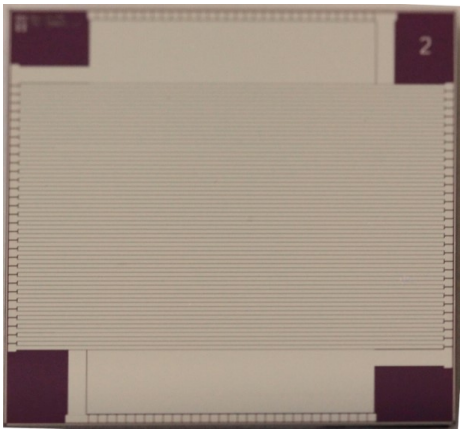

Fig. 1. Image of the 62+62 RCA CMUT chip

The article is organized as follows: First, the measurement methodology is described. Then, the experimental details of the wafer level electrical characterization is given. Finally, the article ends with conclusions.

II. CMUT characterization methodology

The characterization methodology is illustrated in Fig. 2. Two fixed probes, $P1$ and $P2$, are used to connect two neighboring top electrodes (e.g. rows $R2$ and $R3$) to the measurement equipment.

In a typical situation a range of electrical measurements are performed:

1) Current voltage (IV) measurements are made to determine if adjacent top or bottom electrodes are short circuited due to e.g. problems during fabrication.
2) Impedance frequency (Z-f) measurements are performed to determine the frequency for capacitance voltage (CV) measurements and investigate the characteristics of the transmission line.

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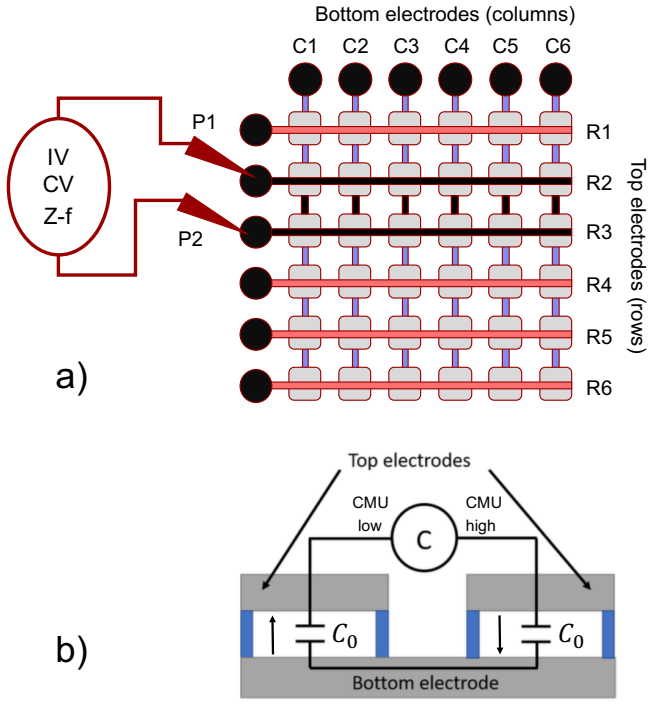

Fig. 2. a) Illustration of the measurement of the capacitance between two neighboring top electrodes, $R2$ and $R3$ using two probes, $P1$ and $P2$. b) The bottom electrodes, $C1$ to $C6$, effectively connect the CMUT cell capacitors in $R2$ in series with the cell capacitors in $R3$. The measured capacitance is therefore $C = C_0/2$. The arrows show the direction of the electric field in the CMUT cavities. The electric field points in opposite directions.

3) CV measurements are used to verify the electro mechanical behavior of the elements which is seen as a parabolic CV curve.

Once the measurement is completed the wafer is moved to allow the fixed probes to connect to e.g. $R3$ and $R4$ and this procedure is then repeated until all elements have been measured. When all rows have been characterized the procedure is repeated on the columns. This allows to determine the electrical characteristics of the array and identify defective elements.

During impedance measurements, the bottom electrodes, columns $C1$ to $C6$, effectively connect the CMUT cell capacitors in $R2$ in series with the cell capacitors in $R3$ as illustrated in Fig. 2b). Ignoring electrode resistance [10] and substrate coupling [11] the measured capacitance, C, is therefore

$$C = \frac{C_0}{2}, \tag{1}$$

where C_0 is the capacitance of a single row element. In this way the element capacitance can be estimated on wafer scale.

The electrical measurements allow to determine if the elements of the array perform as expected and process errors can be detected as abnormal electrical behavior indicating a faulty element. For example, if two neighboring rows are not completely separated during element etching, as illustrated on Fig. 3, the IV measurement will show that the elements are

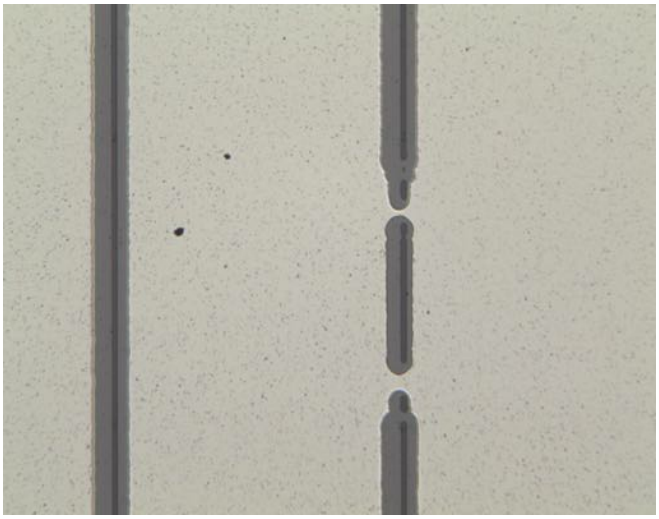

Fig. 3. Short circuit between two adjacent top electrodes (rows).

short circuited and impedance measurements, used to calculate the capacitance, will show both a small resistance and phase angle. Likewise, the capacitance between the short circuited elements and a neighboring element will represent a series coupling of $2C_0$ and C_0, i.e. the measured capacitance is (again ignoring substrate coupling) $C = 2C_0/3$. In general, the capacitance between m short circuited elements and n short circuited elements will be

$$C = \frac{mn}{m+n} C_0. \tag{2}$$

Thus, also the capacitance between two neighboring elements can reveal structural defects.

III. Experimental

The methodology for wafer level characterization of CMUTs relies on a semi-automatic wafer prober and IV, CV and Z-f are the basic tests performed. These measurements were performed on a 62+62 RCA CMUT array from the same wafer as the array described in [12], however, a chip with lithographic errors possessing dielectric charging was selected to demonstrate the possibilities of wafer level test. A Cascade 12K Summit semi-automatic wafer prober and a KEYSIGHT B1500A Semiconductor Device Parameter Analyzer equipped with a B1520A multi frequency capacitance measurement unit (CMU) and six source measurement units (SMU) for IV measurements were used. The KEYSIGHT B1500A is connected to the probe manipulators using a SMU-CMU unify unit (SCUU) which allows to automatically switch between current-voltage and capacitance measurements. The measurement system is also equipped with a guard switch unit (GSWU) which is used for an accurate impedance measurement by connecting the guard lines between CMU high and low near the CMUT. The electrical measurements were performed between neighboring bottom or top electrodes.

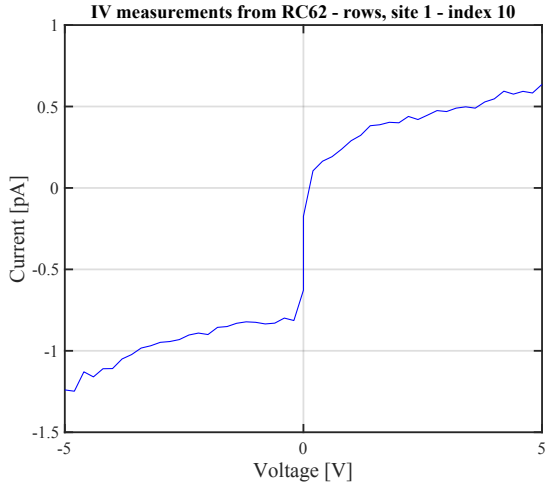

Fig. 4. Typical current-voltage measurement between adjacent row elements show a leakage current in the pA range.

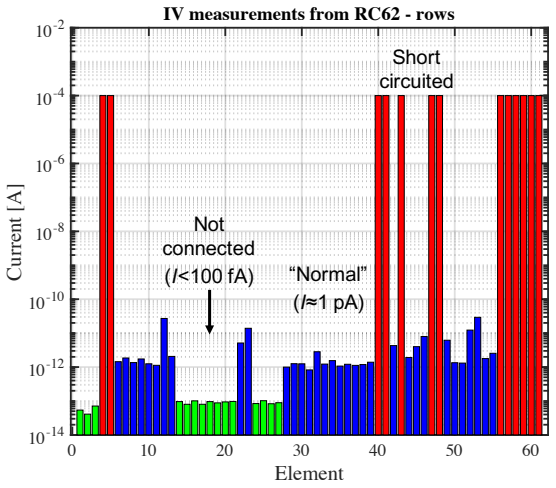

Fig. 5. Plot of the maximum current for each adjacent row elements determined from IV measurements as shown on Fig. 4. The blue bars show normal functioning elements. The red bars indicate elements that are shorted, and the green bars show elements that are not connected.

A. IV characterization

Fig. 4 shows the IV curve measured between two adjacent row elements on the 62+62 RCA CMUT array. The currents is as expected very low, in the pA range, corresponding to a large electrical resistance of around 10 TΩ. Such IV measurements were performed between all adjacent elements in the array and the maximum current was extracted and the result is shown on Fig. 4. The plot reveals three categories of elements. The blue bars show normal functioning elements where the current between adjacent rows is around 1 pA. The red bars indicate elements that are shorted leading to a high current. The reason for the short circuited elements were found to be errors in the

Fig. 6. Bond pad and row element not connected due to errors in the lithographic process.

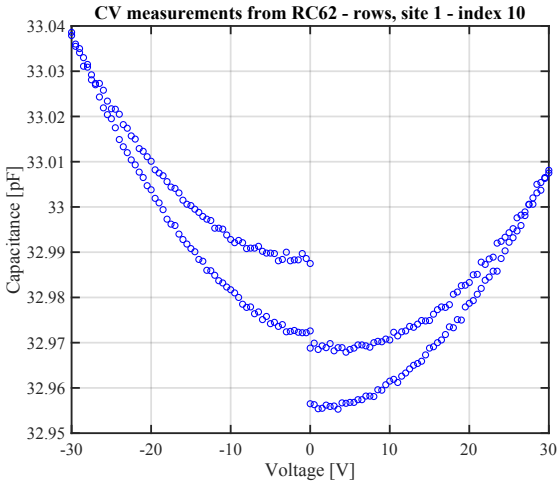

Fig. 7. Capacitance-voltage measurement between adjacent row elements. The CV curve reveals dielectric charging.

definition of the top electrodes as show on Fig. 3. Finally, the green bars show elements that are not connected leading to a very low current on the order of fA. The reason for this error was in all cases found to be an over etch of the aluminum electrode close to the bonding pad leaving the element without connection to the bond pad as illustrated in Fig. 6. Thus, IV measurements are very well suited for process control and can be performed on both top (row) and bottom (columns) electrodes.

B. CV characterization

Fig. 7 shows a typical CV curve as measured on the RCA CMUT chip shown on Fig. 1. The CV curve is parabolic as expected for a CMUT where the applied voltage decreases the gap in the CMUT cells leading to an increasing capacitance. It is noted that the CV curve has hysteresis indicating dielectric charging. Measurements on linear test elements has shown

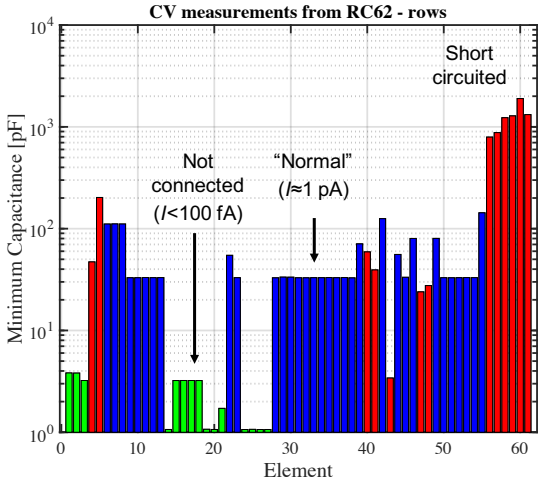

Fig. 8. Plot of the minimum capacitance for each adjacent row elements determined from CV measurements as shown on Fig. 7. The blue bars show normal functioning elements having a capacitance around 30 pF. The red bars indicate elements that are shorted so the capacitance cannot be determined. The green bars show elements that are not connected where the capacitance is around 1 pF.

that the device is electrically stable for one bias polarity. That the charging behavior is observed for *both* voltage polarities is because that measuring between adjacent electrodes means that the electric field in the CMUT cavities of the two elements always points in opposite directions as illustrated in Fig. 2. CV measurements were performed between all adjacent elements in the array and the minimum in capacitance was extracted and the result is shown on Fig. 7. The capacitance of the normal functioning elements is around 33 pF. The capacitance measured between elements which are shorted to neighboring elements is higher as the area of the elements are larger. CV measurements can also be performed between adjacent bottom electrodes.

IV. Conclusion

This paper presented a measurement methodology for wafer level characterization of RCA CMUTs. To facilitate automated wafer level tests, electrical measurements were performed between adjacent top (rows) or bottom electrodes (columns). IV measurements between fully functioning elements showed a maximum current in the pA range. It was found that short circuited elements and elements that are not connected to the bond pads can be be identified electrically. The reason for the errors was found to be related to the etching process used for definition of the top electrodes. CV measurements allowed to determine the element capacitance as this is approximately twice the measured capacitance. When CV measurements are performed between adjacent electrodes the electric field has opposite directions in the two elements and if dielectric charging is present it will show up in the CV curve for both polarities even if the device is stable in one voltage polarity. In conclusion, wafer level characterization of RCA CMUT devices is a valuable tool for selecting the best performing chips and to assist in process optimization.

V. Acknowledgement

This work was financially supported by grant 7050-00004B from Innovation Fund Denmark, and from BK Medical, Herlev, Denmark.

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Chapter **E**

Paper C - Wafer bonded CMUT technology utilizing Poly-Silicon-on-Insulator wafers

Wafer bonded CMUT technology utilizing a Poly-Silicon-on-Insulator wafer

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Published in:
Proceedings of the 2019 IEEE International Ultrasonics Symposium

Link to article, DOI:
10.1109/ULTSYM.2019.8925931

Publication date:
2019

Document Version
Peer reviewed version

Wafer bonded CMUT technology utilizing a Poly-Silicon-on-Insulator wafer

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***Abstract*—This paper presents a fabrication process of a Poly-Silicon-On-Insulator (PSOI) wafer that can be used as an alternative to conventional Silicon-On-Insulator (SOI) wafers for fabrication of Capacitative Micromachined Ultrasound Transducers (CMUT). The fabrication of PSOI wafers does, unlike the conventional SOI fabrication, not involve any bonding steps. A batch of PSOI wafers having a 400 nm BOX layer and a 2.6 µm ± 0.04 µm (1σ) device layer is fabricated and characterized. A surface roughness of 0.47 nm is measured for the PSOI device layer, and successful fusion bonds (direct bonds) are demonstrated between PSOI wafers and oxidized silicon wafers. A wafer-bonded CMUT using a PSOI wafer is fabricated and electrically characterized, and the expected CMUT performance is observed. Impedance spectra are demonstrated at five different DC biases, the expected spring softening effect is observed when the magnitude of the DC bias is increased.**

I. Introduction

Silicon-On-Insulator (SOI) wafers are today routinely used in the semiconductor industry and have been applied for numerous applications ranging from P/N junctions [1], Optical applications [2], and in particular for applications in the industry of Micro Electrical Mechanical Systems (MEMS) [3]. The target application for this paper is the Capacitive Micromachined Ultrasound Transducer (CMUT), a technology developed in the 1990's [4] that falls into the category of MEMS devices where SOI wafers are commonly used. The basic structure of a SOI wafer consists of a device layer, a buried oxide layer (BOX), and a handle wafer (substrate). The device layer of the SOI wafer is used in CMUT applications as the vibrating plate or membrane. The device layer of SOI wafers used for wafer bonded CMUTs are required to have bondable surfaces, low electrical resisitvity, predictable mechanical stiffness, and preferably a uniform device layer thickness, h. Monocrystallinity of the device layer is not important for CMUT applications, but, it is essential for other SOI based applications. The ability to customize the thickness and resistivity of the individual layer provides great freedom in a MEMS design. The fabrication processes of CMUTs are either based on a sacrificial release [5] and wafer bonding step, where the latter is the main focus of this work. Several wafer bonding techniques have been demonstrated for CMUT applications [6]–[8]. The device layer thickness, of conventional SOI wafers, can be specified from hundreds of microns down to $2\,\mu\mathrm{m}$ with a uncertainty of $0.3\,\mu\mathrm{m}$. The SOI wafers used for CMUT applications are typically close to the lower limit, and have typically device layers less than $10\,\mu\mathrm{m}$. However, CMUT plates (device layer) thinner than $2\,\mu\mathrm{m}$ plate are highly desirable in some CMUT designs, especially for high frequency or high bandwidth applications. Hence, it becomes challenging for such applications to get the desired wafer specification when conventional SOI wafers are used. A thinner device layer can be obtained by thermally oxidize the SOI wafers and remove the grown oxide subsequently. This process can be controlled with high precision, but, the relative thickness variation increases, since, the uncertainty of the device layer thickness is unaffected by the oxidation process. Variations of the plate thickness, h, across a CMUT array influence important characteristic CMUT parameters such as resonance frequency and pull-in voltage, which scales with h and as $h^{3/2}$, respectively. Thus, tight control of the plate thickness is necessary for having equal performance of all CMUT in an array. The objective of this paper is to demonstrate the Poly-silicon-On-Insulator wafer as a rapid prototyping tool for CMUT fabrication. The PSOI technology is required to be non-inferior to the already existing SOI technology measured by important CMUT characteristics, such as reliable bonding properties, sufficient electrical properties and uniform device layer thickness across the wafer. Fusion bonded CMUTs must be demonstrated to verify non-inferiority of the PSOI technology, since fusion bonding is more sensitive in terms of surface roughness and cleanliness compared to other techniques such as anodic bonding and polymer bonding. The majority of the CMUTs demonstrated found in the literature have plate thicknesses less than $5\,\mu\mathrm{m}$ and it will therefore be considered as the upper bound of the device layer. In addition, the device layer resistivity should be less than $1\,\Omega\,\mathrm{cm}$ to be interesting for CMUT applications.

II. Fabrication

A. Fabrication of PSOI wafers

The fabrication process of conventional SOI wafers consists of few steps, first an oxide is grown on a silicon substrate (wafer A) and the oxide surface is thereafter fusion bonded to a new silicon wafer (wafer B). The oxide defines the BOX layer and wafer A defines the handle layer. The device layer is made by wafer B, the thickness is adjusted to match the desired specifications by removing silicon in a grinding process. Finally, a chemical mechanical polishing (CMP) is carried out to obtain the same surface standard as conventional silicon wafers [9]. The fabrication process of PSOI wafers is similar to the fabrication of conventional SOI. However, the

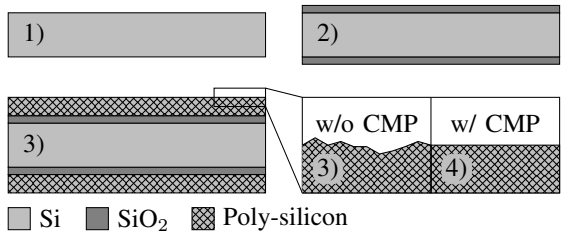

Fig. 1. Fabrication process of PSOI wafers. 1) A standard silicon wafer is RCA cleaned. 2) A thermal oxide is grown. 3) Poly-silicon is deposited in an LPCVD process. 4) The poly-silicon layer is polished (CMP) to reduce surface roughness. Figure is not to scale.

device layer is deposited using a Low Pressure Chemical Vapor Deposition (LPCVD) process instead of being bonded to the oxide surface. The fabrication of PSOI wafers consists of four steps as shown in Fig. 1.

The first step in the PSOI fabrication is a RCA clean of a silicon wafer. This wafer will end up as the handle layer and electrical properties, doping type, and wafer thickness should therefore match desired specifications. In step 2, an oxide is thermally grown that constitutes the BOX layer. A $400\,\mathrm{nm}$ dry oxide grown at $1100\,^{\circ}\mathrm{C}$ is used for the PSOI wafers fabrication in this work. The device layer is created in step 3, where a boron doped poly-silicon is deposited using a LPCVD process. The equivalent could be obtained by a phosphor doped poly-silicon, but the deposition rate is substantially lower.

Finally, in step 4, the poly-silicon surface is polished using a Logitech CM62 Orbis Chemical Mechanical Polishing (CMP) machine. The final poly-silicon thickness of a fabricated PSOI has been measured across the wafer using multi-angle reflectometry measurements, the resulting thickness map is shown in Fig. 2. A mean thickness of $2.60\,\mu\mathrm{m}$ with a standard deviation of $0.04\,\mu\mathrm{m}$ has been measured. Additionally, the difference between minimum and maximum thickness is measured to be $0.26\,\mu\mathrm{m}$, hence, in full compliance with the non-inferior constraint. The surface roughness, of the deposited LPCVD poly-silicon, has been measured using a PLu neox Optical Profiler (confocal microscope) to $6.98\,\mathrm{nm}$ prior to the CMP process and $0.47\,\mathrm{nm}$ after the CMP process. The true surface roughness could be lower, since these measurements are at the resolution limitation of the confocal microscope. A surface roughness of approximately $0.5\,\mathrm{nm}$ has also been measured on a reference silicon wafer. A surface roughness of less than $1\,\mathrm{nm}$ is required to achieve successful fusion bond and preferably even lower [10]. The CMP process is therefore essential for fusion bonding to be successful.

The mechanical and electrical properties of a LPCVD poly-silicon are influenced by multiple parameters, including deposition temperature, deposition time, gas composition, tube pressure, and flow conditions among other. The deposition rate of the LPCVD poly-silicon should be high enough to produce $5\,\mu\mathrm{m}$ poly-silicon layer within a reasonable time. At the same time the built-in stress should preferably be tensile and the resistivity should be low. A tensile stress in the poly-

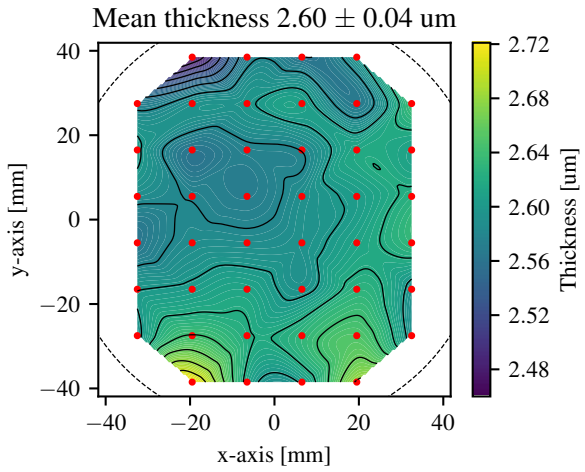

Fig. 2. Interpolated thickness map of a PSOI device layer measured using multi-angle reflectometry. The circumference of the wafer is indicated by the dashed black line, and the 44 red dots indicate the spatial positions of the data points used to generate the thickness map.

silicon prohibits buckling effects in the final CMUT structure. An acceptable resistivity parameter space depends on the CMUT application, and a criterion that describes when the resistivity is low enough for acceptable CMUT performance can be found in [11]. Four point probe measurements of 19 PSOI wafers have been conducted to estimate the resistivity of the device layer, the mean and standard deviation were $0.036\,\Omega\,\mathrm{cm} \pm 0.019\,\Omega\,\mathrm{cm}$, and the highest measured resistivity was $0.062\,\Omega\,\mathrm{cm}$. Depositing rate, thin film stress, and resistivity do all depend on the deposition temperature [12]–[17], and quantitative values of these parameters are plotted in Fig. 3.

The material properties of the deposited poly-silicon vary from lab to lab, and the data should be interpreted as tendencies and not absolute values. The deposition rate is seen, in Fig. 3 a), to increase as the deposition temperature increases, whereas a reduction in the resistivity is observed in Fig. 3 b) (notice the log y-scale). Hence, rapid fabrication time and low resitivity are obtained by an increased deposition temperature. However, the temperature dependency of the stress is not unambiguous as the deposition rate and resistivity, and extrapolation is therefore difficult. Fusion bonded CMUTs require an annealing step at temperatures on the order of $1000\,^{\circ}\mathrm{C}$, and annealing time and temperature do also influence the stress and resistivity. The highest process temperature is, however, significantly lower for other CMUT fabrication methods such as anodically bonded CMUTs, where the highest process temperature is on the order of $350\,^{\circ}\mathrm{C}$ [7]. The resistivity and stress values from Fig. 3 b) and c) are therefore directly applicable for anodically bonded CMUTs, but are perturbed during annealing for fusion bonded CMUTs. The minimum device layer thickness for conventional SOI wafers are limited to $2\,\mu\mathrm{m}$, but, the PSOI technology can provide a device layer ranging from approximately $10\,\mathrm{nm}$

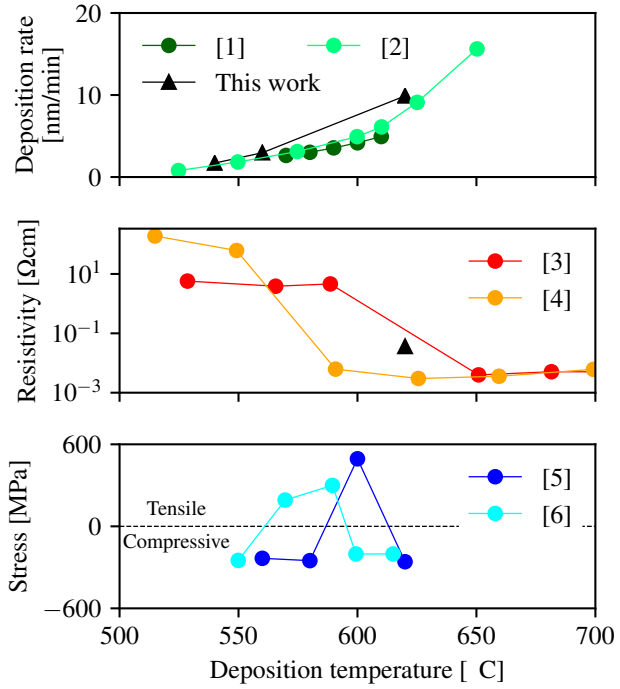

Fig. 3. The deposition rate, resistivity, and stress as function of deposition temperature. The circular markers are from the literature and represents either boron doped or undoped LPCVD poly-silicon and triangular markers indicate measurements of LPCVD boron doped poly-silicon from this work.

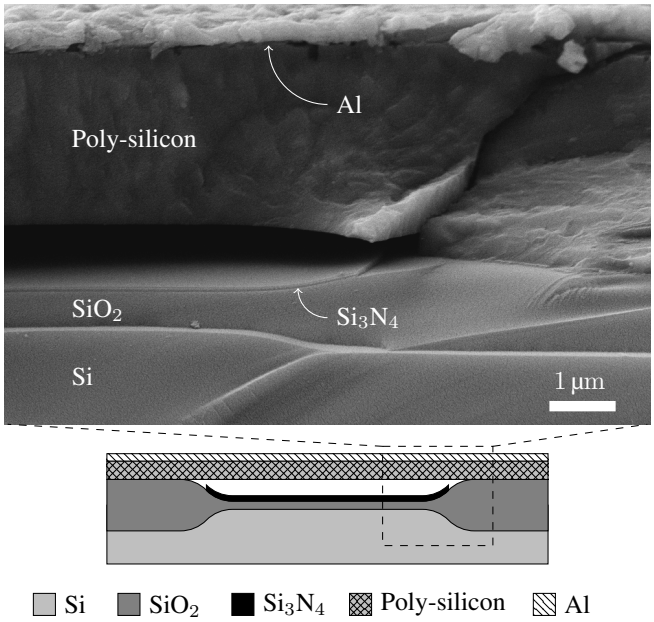

Fig. 4. Cross sectional SEM image of a CMUT fabricated using a PSOI wafer. A thin gold layer of a few nanometer has been sputter to reduce charging effects in the dielectric layers. A sketch of the designed LOCOS CMUT is inserted below the SEM image.

TABLE I
VARIOUS MEASURED PSOI PARAMETERS

Parameter	Samples [#]	Upper bound
Device layer thickness variations	2	$<0.3\,\mu m$
Surface roughness	1	$0.47\,nm$
Wafer bow	10	$<20\,\mu m$
Device layer resistivity	19	$<0.062\,\Omega\,cm$

to $5\,\mu m$, and is limited by how thin or how thick layers the LPCVD system can deposit. But, the PSOI technology is also applicable for applications that require device layers of less than $2\,\mu m$. The fabrication time of PSOI wafers is two-three days under the assumption of availability of an oxidation furnace, a LPCVD poly-furnace and a CMP machine. The PSOI technology provides a rapid and flexible technology platform for CMUT research and development, as an alternative to the conventional SOI wafers where the delivery time (months) can limit the iteration process of various CMUT designs.

An overview of various measured PSOI parameters can be found in Table I.

B. Fabrication of CMUTs

The CMUTs in this work have been fabricated using a LOCal Oxidation of Silicon (LOCOS) process, first demonstrated in 2008 by [18] and described further in [19]. The LOCOS process has numerous beneficial properties for CMUT fabrication such as high dielectric strength, reduced parasitic capacitance, good uniformity, and the gap height can be controlled with nanometer precision. The PSOI wafer and the processed LOCOS substrate wafer were both RCA cleaned prior to the fusion bonding process, and pre-bonded using a Süss SB6 wafer bonder, followed by an annealing step at $1100\,°C$ for $70\,min$. A cross sectional image of a fabricated CMUT has been acquired by a Scanning Electron Microscope (SEM) and shown in Fig. 4. A sketch of the structure has been inserted below the SEM image to illustrate the designed LOCOS structure. The CMUT plate is as expected composed of a polycrystalline material separated from the bottom of the CMUT cavity by the LOCOS bird's beak structure. The CMUT has been diced by an automatic dicing saw and the surface is observed to be frayed as a result of the dicing process.

III. CMUT CHARACTERIZATION

The fabricated CMUTs have been electrically characterized by impedance measurements. The measurements were performed using an Agilent 4294A Precision Impedance Analyzer with five different DC biases and an AC voltage of $100\,mV$. The impedance magnitude and phase are plotted in Fig. 5 a) and b), respectively, where the expected CMUT behaviour is observed. A distinct resonance frequency is observed in the frequency range between $5\,MHz$ and $6.5\,MHz$, and the spring softening effect is confirmed by the frequency shift towards lower frequencies as the magnitude of the DC bias is increased. In addition the phase is approximately, in Fig. 5 b), $-90°$ for all off-resonance frequencies up to $10\,MHz$, which verifies the expected capacitive properties for the CMUT. The impedance

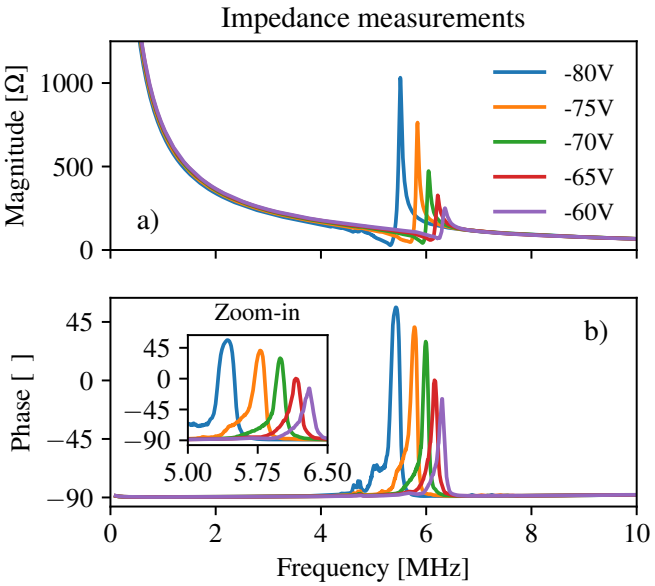

Fig. 5. Impedance measurements of a fabricated CMUT at five different DC biases. The expected spring softening effect is observed for an increased DC magnitude. The applied bias ramp corresponds to 72.2%, 77.8%, 83.3%, 88.9%, 94.4% of the pull-in voltage.

measurements demonstrate the technological potential of PSOI wafers as an alternative to conventional SOI wafer for MEMS devices.

IV. Conclusion

This paper presented a fabrication method of a Poly-Silicon-On-Insulator (PSOI) wafer. A PSOI wafer was demonstrated applicable for CMUT applications as an alternative to conventional Silicon-On-Insulator (SOI) wafers. Fabrication of PSOI wafers can reduce iteration time for wafer bonded CMUTs, and the device layer of a PSOI wafer can be fabricated thinner than a conventional SOI. The device layer thickness of a fabricated PSOI wafer was measured using multi-angle reflectometry and yielded a mean thickness of $2.60\,\mu\mathrm{m}$ with a standard deviation of $0.04\,\mu\mathrm{m}$. A mean resistivity of 19 PSOI wafers were characterized by four point probe measurements and measured to $0.36\,\Omega\,\mathrm{cm} \pm 0.19\,\Omega\,\mathrm{cm}$ (1σ). A surface roughness of $0.47\,\mathrm{nm}$ was determined by confocal microscopy, and a bondable surface properties was demonstrated by fabrication of a functional fusion bonded CMUT. An impedance analysis of the fabricated CMUT showed the expected CMUT behaviour. A distinct resonance frequency was observed for five different DC biases, and the spring softening effect was confirmed by a frequency shift as the magnitude of the applied DC bias was increased.

V. Acknowledgement

We would like to thank the Danish Innovation Fund and BK Medical for funding this research.

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Chapter **F**

Paper D - Large Scale High Voltage 192+192 Row-Column Addressed CMUTs Made with Anodic Bonding

Large Scale High Voltage 192+192 Row-Column Addressed CMUTs Made with Anodic Bonding

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***Abstract*—This work presents the fabrication process of anodically bonded 192+192 2D row-column addressed (RCA) capacitive micromachined ultrasonic transducer (CMUT) arrays.**
Four large 2.1 by 2.1 cm^2 arrays with a resonance frequency of 7.5 MHz in water and $\lambda/2$ element pitch at $95\,\mu\mathrm{m}$ are shown successfully fabricated. The arrays exhibit a $100\,\%$ bond yield by anodically bonding an SOI wafer to a borosilicate glass wafer structured with CMUT cavities. A silicon nitride layer has been used at the wafer bonding interface to insulate the top and bottom electrodes for high voltage operation to at least $\pm 200\mathrm{V}$ DC bias. Electrical measurements have been performed on 192+192 RCA arrays and smaller 16+16 RCA arrays. These showed a resonance frequency of approximately $18\,\mathrm{MHz}$ in air at a bias of $-200\,\mathrm{V}$, corresponding to $80\,\%$ of the pull-in voltage and 50 mV AC, with a coupling coefficient of $26.8\,\%$.

I. Introduction

The image quality of medical ultrasound images improves as the number of elements is increased. Unfortunately, having a large number of elements poses a challenge for 3D ultrasound imaging, where the scaling properties of the number of interconnections depend highly on the addressing scheme. By employing a row-column addressing (RCA) scheme [1], the number of interconnections, N, scales as $2N$ compared to N^2 for conventional fully populated matrix (FPM) arrays [2]. The capacitive micromachined ultrasonic transducer (CMUT) technology is in this work used to realize 2D row-column addressed (RCA) arrays, since the technology enables a convenient design flexibility. In addition, the RCA arrays also offer broad bandwidth [3], high coupling coefficient [4], and reduced self-heating [5]. 2D CMUT arrays have already been demonstrated in the literature both for FPM [6] and row-column [7] arrays.

The large area needed for RCA arrays with a high channel count sets strict requirements for the yield and robustness of the fabrication process, which is the focus of this work. Especially the ability to bond the top plate to the bottom substrate without voids or complications due to particles is a critical step.

A large RCA array area does also produce a high transmit pressure, which is needed for deep tissue penetration. The stored electrostatic energy in the CMUT scales with the applied bias voltage squared, hence, more energy can be converted into the mechanical domain as the bias is increased.

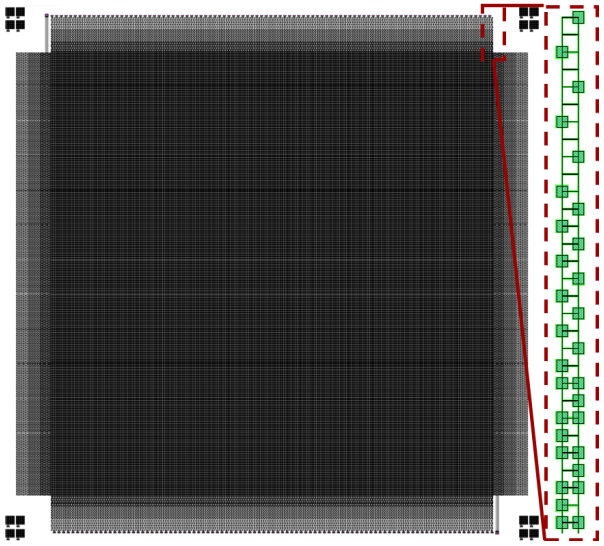

Figure 1. Design overview of the 192+192 row-column CMUT array. The integrated apodization scheme for one element is seen in the inset.

This work presents the development of a high voltage 192+192 element RCA transducer array based on CMUT technology using anodic bonding. This has earlier been demonstrated for a linear array in [8] and later for a 32+32 RCA array [9]. Both of these CMUT arrays were characterized at bias voltage lower than $75\,\mathrm{V}$, whereas the aim of this work is to operate the CMUT at bias voltages up to $200\,\mathrm{V}$. Other techniques have been presented for RCA CMUT fabrication such as sacrificial release cavity formation and polymer based devices [10], [11].

The anodic bonding technique involves the bonding of a silicon-on-insulator (SOI) top plate wafer to a borosilicate glass (Borofloat 33) substrate and gives several advantages during fabrication and for device performance.

The insulating glass lowers substrate coupling between the bottom electrodes (column elements), which gives the same receive sensitivity on rows and columns [12]. Utilizing glass as a substrate makes it possible to define cavities directly by etching instead of using e.g. sacrificial release methods [13] or performing local oxidation of silicon (LOCOS) [14]. The anodic bonding process is less sensitive to particle contamination

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and easily gives strong bonds, which allows us to make large arrays with high yield.

Furthermore, low resistivity metal electrodes are advantageous for large RCA arrays, since the electrode resistance can result in significant attenuation along the elements [15]. A low attenuation along the bottom electrodes and thereby uniform transmit pressure is achieved by lowering the dimensionless product ωRC, where, ω, is angular frequency, R, is the resistance, and C, is the capacitance of an element.

II. Design & Fabrication

A. Design

Fig. 1 shows the design of the CMUT array.

The RCA CMUT arrays presented are designed with 192+192 row and column elements having a 7.5 MHz center frequency in immersion. The CMUT cells have a square geometry with a side length of 37 µm, a $\lambda/2$ element pitch at 95 µm and a plate thickness of 3 µm. The design includes an integrated apodization scheme [16] at the edge of the array extended over 15 sub cells to reduce edge wave effects. The whole wafer design, seen in Fig. 2, features four large 192+192 RCAs measuring $2.1 \times 2.1\,\mathrm{cm}^2$ and 76 smaller 16+16 RCA test arrays. The 16+16 arrays feature structures with either shorted top or bottom electrodes for ease of characterization.

To realize the high voltage aspect of the design mentioned above, a silicon nitride layer is incorporated as an intermediate dielectric layer between the plate and glass substrate in two different designs shown on Fig. 3. The first design Fig. 3 a) and b), utilized the nitride membrane as pull-in isolation inside the cells. This gave rise to short circuits in the 400 nm gap between the aluminium top electrode and the chromium leading from the cell to the contact pad due to electrical breakdown in air. This breakdown occurs already below 10 V bias.

The second design, seen in Fig. 3 c) and d), uses another lithography mask when opening to the bottom electrode. In this design the silicon nitride membrane is instead extended to the bottom electrode contact pad. The silicon nitride membrane covering the Borofloat trench insulates the top and bottom electrodes and allows for high voltage operation up to at least ±200 V DC bias.

B. Fabrication

The process flow is shown in Fig. 4. The material used as substrate is a borosilicate glass wafer with a thickness of 525 µm (Borofloat 33). First a 50 nm chromium metal layer is deposited and structured using a photolithographic process and wet etching, thereby forming a mask for etching the cell cavities. A buffered hydrofloric acid (BHF) is used to isotropically etch the CMUT cavities to a depth of 410 nm and the chromium mask is removed. In the next step a new 230 nm chromium layer is deposited and wet etched through a photoresist mask to structure the bottom electrode in the cell cavities and interconnecting leads. These steps are illustrated in Fig. 4, steps a) through d), where the cross-section corresponds to the cut-line shown in Fig. 3.

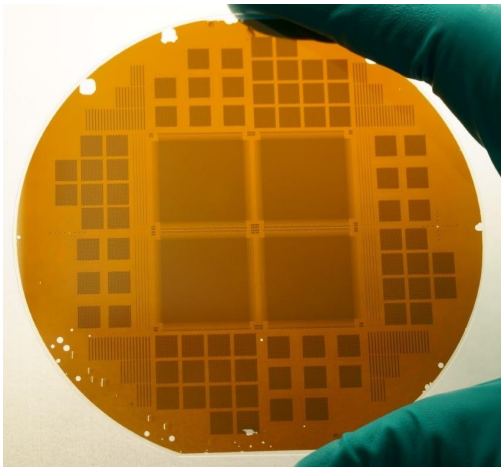

Figure 2. Photograph of the borosilicate glass wafer from step 6 in the fabrication process. The four 192+192 RCAs, the smaller 16+16 RCAs and the linear test elements are shown.

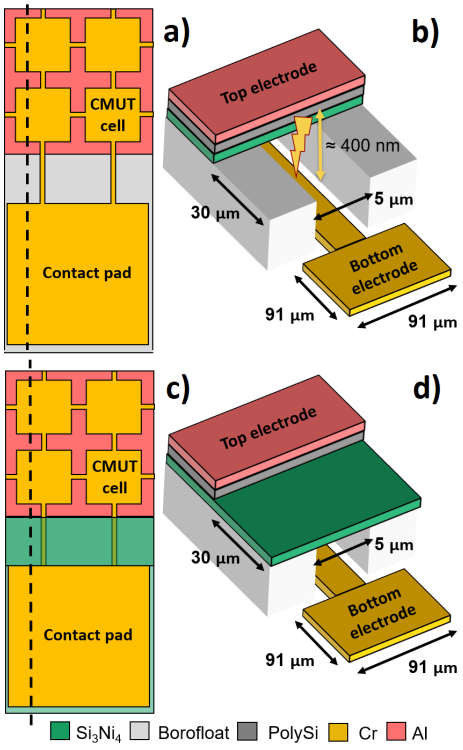

Figure 3. High voltage design overview. First and second design are a) – b) and c) – d), respectively. a) Top down view through the top electrode of the CMUT cells, contact pad and interconnecting leads. The borofloat substrate trench leading to the contact pad is uncovered. b) The same structure near the bottom electrode pad shown in 3D. The 400 nm distance between top and bottom electrodes right at the edge of the top plate leads to an electrical breakdown in air. c) Top down view through the top electrode. The borofloat substrate trench with the chromium leads is here covered by a silicon nitride bridge design. d) The 30 µm long borofloat trench is seen covered by an insulting nitride membrane. The dotted cut-line corresponds to the cross-section presented in the process flow in Fig. 4

A poly-silicon-on-insulator (PSOI) wafer is used [17], as an alternative to the conventional SOI wafer. The thickness of the poly silicon device layer is $3\,\mu\mathrm{m}$. A $200\,\mathrm{nm}$ stoichiometric silicon nitride layer is deposited on the PSOI wafer to obtain protective electrical insulation. The nitride covered PSOI wafer is then subsequently thermally oxidized for three hours at $1100\,^{\circ}\mathrm{C}$ in an H_2O environment to improve the anodic bonding conditions [18].

The PSOI and the glass substrate are then cleaned in an RCA-1 cleaning solution (H_2O, NH_4OH and H_2O_2 (5:1:1)) and a piranha solution (4:1) respectively. They are then anodically bonded in vacuum at an elevated temperature of $375\,^{\circ}\mathrm{C}$ through a four step voltage ramp (200 V/ 400 V/ 600 V/ 800 V) achieving an accumulated charge of approximately 3000 mC, step e).

Due to the transparency of the glass substrate the bond can be inspected for voids before the process is continued, without the need for infrared wafer mapping.

The silicon nitride, poly-silicon, BOX and handle layers are then removed from the backside of the PSOI wafer using dry and wet etching, leaving the $200\,\mathrm{nm}$ silicon nitride and $3\,\mu\mathrm{m}$ poly-silicon plate covering the cavities (step 6). Using a microscope for inspection, this critical etching process step shows a $100\,\%$ bond yield for the four large centre arrays and $98.8\,\%$ yield for the 16+16 arrays, seen in Fig. 2.

A $400\,\mathrm{nm}$ aluminium metal layer is then deposited and patterned by wet etching to create the top electrode contacts. This layer is subsequently used as a dry etching mask for separating the poly-silicon row elements using reactive ion etching (RIE). Finally, a new photoresist mask is made for opening the nitride covering the bottom electrode contact pads using a RIE process. These steps are illustrated in Fig. 4, steps g) through i).

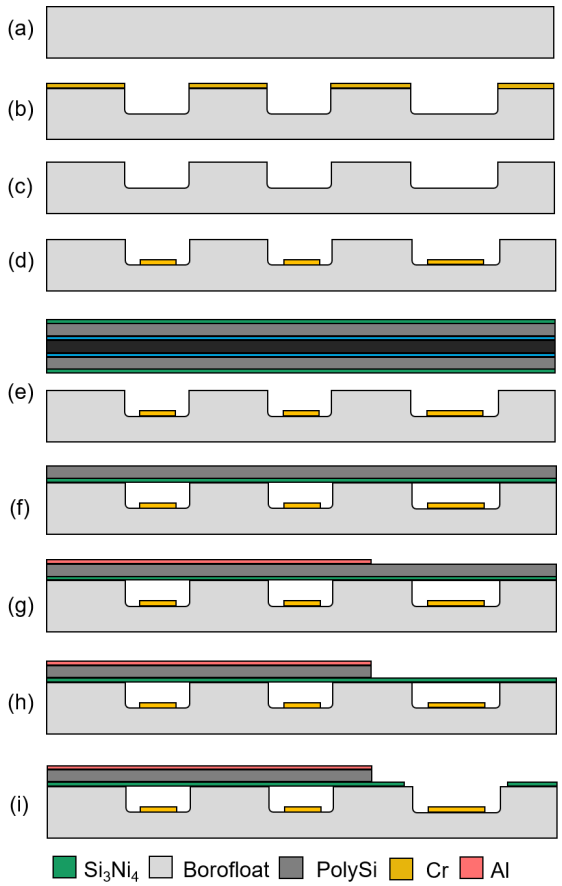

Figure 4. Fabrication process flow for the glass-based row-column CMUT array. The cross-section corresponds to the cut-line in Fig. 3

III. Characterization

A. Electrical

The electrical behavior of the 192+192 CMUT arrays has been characterized in air by performing current-voltage (IV), capacitance-voltage (CV) and impedance (Z-f) measurements pair wise between adjacent rows (top electrodes) of the 192+192 arrays. The 16+16 arrays were also characterized and measured between top and bottom electrodes by shorting either all top or bottom elements [19]. The measurements were made with an automated wafer prober (Cascade Summit 12K probe station), a parameter analyzer (Keysight B1500A Semiconductor Parameter Analyzer), and a dedicated impedance analyzer (Agilent 4294A Precision Impedance Analyzer) with a varying DC voltage and an AC voltage of $50\,\mathrm{mV}$ connected through a bias tee.

The capacitance vs. voltage characteristic, seen in Fig. 5, is shown for a voltage sweep from $-100\,\mathrm{V}$ to $100\,\mathrm{V}$ on a 16+16 array element. The minimum capacitance is measured to be $2.84\,\mathrm{pF}$ at $0\,\mathrm{V}$, and the CV curve exhibits the expected parabolic CMUT behaviour and no noticeable dielectric charging is seen. The impedance magnitude and corresponding $-90°$ phase of a test element has been measured, Fig. 6, for frequencies up to $25\,\mathrm{MHz}$ with an applied DC bias voltage of $-200\,\mathrm{V}$ and $50\,\mathrm{mV}$ AC corresponding to $80\,\%$ of the designed pull-in voltage of $250\,\mathrm{V}$.

Resonance and anti-resonance peaks, f_{res} and f_{ares}, are seen at the frequencies $16.6\,\mathrm{MHz}$ and $19.4\,\mathrm{MHz}$, respectively. The electromechanical coupling coefficient has been estimated using

$$k^2 = (1 - (f_{res}/f_{ares})^2) \times 100\,\% \quad (1)$$

to be $26.8\,\%$.

All elements measured could support a DC bias of at least $\pm 200\,\mathrm{V}$ if the designed silicon nitride bridge was intact after etching. Elements which had their nitride bridge partially fractured in the final fabrication steps still experienced breakdown at lower voltages, i.e. around $150\,\mathrm{V}$ to $180\,\mathrm{V}$ DC.

IV. Conclusion

In this paper the fabrication process and initial electrical characterization of a row-column CMUT array based on a anodically bonded borosilicate glass substrate has been presented. Incorporation of a silicon nitride membrane between the top and bottom electrode has eliminated previously observed breakdown in air near the electrode pads and allowed for high voltage

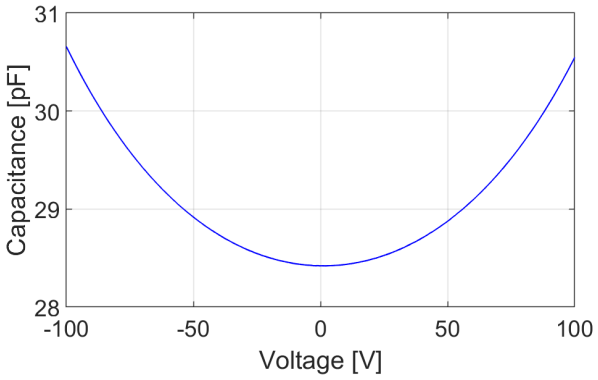

Figure 5. Capacitance vs. voltage (CV) measurement between top and bottom electrode on a an element from a 16+16 row-column CMUT array.

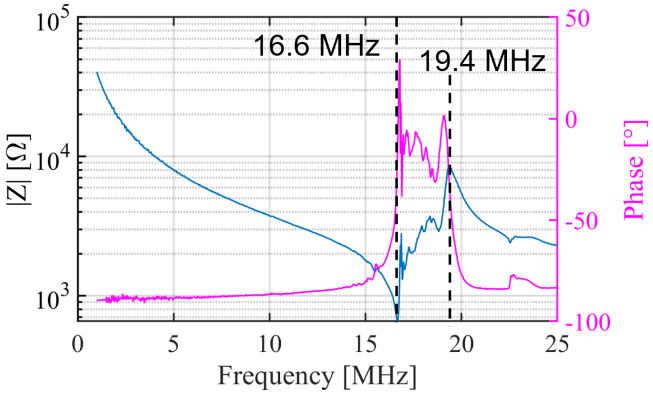

Figure 6. Impedance measurement of a CMUT test element at $-200\,\mathrm{V}$ DC bias and $50\,\mathrm{mV}$ AC. The resonance and anti-resonance peaks are seen at 16.6 MHz and 19.4 MHz, respectively.

operation at a bias of $\pm 200\,\mathrm{V}$. Electrical characterization of the CMUTs has shown the expected parabolic CV behaviour and a resonance frequency at $17\,\mathrm{MHz}$ in air. The fabrication process presented a $100\,\%$ and $98.8\,\%$ bond yield for the 192+192 and 16+16 arrays respectively. This demonstrated that anodic bonding is a viable fabrication platform for the fabrication of large defect free 2D RCA arrays.

The next step will be improving the quality of the silicon nitride etching process and performing a full electrical and acoustical characterization of transmit and receive properties of the RCA arrays.

Acknowledgment

This work is financially supported by Innovation Fund Denmark (7050-00004B).

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Chapter **G**

Paper E - A Hand-Held 190+190 Row–Column Addressed CMUT Probe for Volumetric Imaging

A Hand-Held 190+190 Row–Column Addressed CMUT Probe for Volumetric Imaging

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***Abstract*—This paper presents the design, fabrication, and characterization of a 190+190 row-column addressed (RCA) capacitive micromachined ultrasonic transducer (CMUT) array integrated in a custom hand-held probe handle. The array has a designed 4.5 MHz center frequency in immersion and a pitch of 95 µm which corresponds to $\approx \lambda/4$. The array has a 2.14 $\times$ 2.14 cm^2 footprint including an integrated apodization scheme to reduce ghost echoes when performing ultrasound imaging. The array was fabricated using a combination of fusion and anodic bonding, and a deposit, remove, etch, multistep (DREM) etch to reduce substrate coupling and improve electrode conductivity. The transducer array was wire-bonded to a rigid-flex printed circuit board (PCB), encapsulated in room temperature vulcanizing (RTV) silicone polymer, electromagnetic interference (EMI) shielded, and mounted in a 3D-milled PPSU probe handle. The probe was characterized using the SARUS experimental scanner and 3D volumetric imaging was demonstrated on scatter and wire phantoms. The imaging depth was derived from tissue mimicking phantom measurements (0.5 dB MHz^{-1} cm^{-1} attenuation) by estimating the SNR at varying depths. For a synthetic aperture imaging sequence with 96+96 emissions the imaging depth was 3.6 cm. The center frequency measured from the impulse response spectra in transmit and pulse-echo was 6.0 $\pm$ 0.9 MHz and 5.3 $\pm$ 0.4 MHz, and the corresponding relative bandwidths were 62.8 $\pm$ 4.5 % and 86.2 $\pm$ 10.4 %. The fabrication process showed clear improvement in relative receive sensitivity and transmit pressure uniformity compared to earlier silicon-on-insulator (SOI) based designs. However, at the same time it presented yield problems resulting in only around 55 % elements with a good response.**

I. Introduction

In the recent years, there has been a growing interest in developing 2D ultrasonic transducer arrays for performing 3D volumetric imaging with resolution comparable to conventional 2D imaging made with linear 1D arrays.

For good focusing and high resolution 3D ultrasound imaging a large probe with a significant number of elements, N, is needed. 2D arrays with elements in both the azimuthal and elevation direction are typically fabricated as fully populated matrix (FPM) arrays, where the number of elements and therefore also the number of individual connections each scale with N^2. A linear probe might have 190 elements, which for a matrix array having the same resolution in both directions would result in $190 \times 190 = 36{,}100$ connections. This would require highly impractical bulky cables connecting the probe to the scanner in addition to electronics capable of handling the data rates, which would be several terabytes per second for such an array.

The focusing ability of ultrasound probes is proportional to the wavelength and the ratio of the imaging depth to the width of the probe. The width is equal to the pitch times the number of elements N. Maintaining the same resolution in both dimensions necessitates the same number of elements, hence N^2 connectors. Also maintaining a good resolution demands large probes to maintain the ratio between depth and width.

State-of-the-art FPM array probes based on lead zirconium titanate (PZT) crystal materials can already be acquired commercially from e.g., Philips (X6-1 xMATRIX array transducer with 9212 elements) and for research solutions through Verasonics (Matrix Array Transducer with 1024 elements (32×32)). To achieve a higher channel count an effort has been made to design electronics performing pre-beamforming that fit inside the probe handle [1]–[3], which has also been made possible in the Philips X6-1 xMATRIX probe. Integrated electronics and the use of PZT materials, however, still have problems concerning probe heating under continuous use [4], [5].

A. Row-column arrays

Recently, a new type of array scheme has been developed which can reduce the number of channels needed for imaging and keep the same array footprint without resorting to e.g., using sparse arrays [6], [7]. This is the so-called row-column addressed (RCA) array which was proposed by Morton and Lockwood in 2003 [8] and reiterated by Démoré et al in 2009 [9]. An RCA transducer is composed of two 1D arrays placed orthogonal to each other, with sub-elements in overlapping segments. Imaging sequences are likewise different, in the sense that instead of actuating each single sub-element and selecting sub apertures in the matrix array, entire row or column elements encompassing potentially hundred of sound emitting sub-

elements are excited simultaneously. Row or column elements are used for transmitting a line focus, while the orthogonal elements are grounded. For receiving, opposite elements are often used to focus in a perpendicular line while the previously transmitting elements are grounded. This creates a focus point in the volume where the two lines overlap, which can be used for volumetric imaging. Since only $2 \times N$ elements are used this significantly reduces the number of connections needed. Morton and Lockwood [8] state that beamforming two perpendicular planes with an RCA array results in a loss of signal strength compared to an $N \times N$ FPM array, and that $4 \times N$ elements are needed to get a comparable resolution. It has, however, been shown by Rasmussen and Jensen [10] that RCA arrays always have a higher resolution than FPM arrays for the same number of matrix elements ($32+32$ rows and columns compared to 8×8 matrix elements). More details about the imaging abilities of RCA arrays can be found in [11].

Row-column arrays have been fabricated using PZT or other piezoelectric materials, including a 1-3 ceramic RCA 64×64 array [12], an RCA 256×256 array [13], and a $7.5\,\mathrm{MHz}$ dual-layer transducer with 256 PZT elements used for transmit combined with 256 orthogonal P[VDF-TrFE] copolymer elements for receive [14]. An alternative version of the row-column scheme named top-orthogonal-to-bottom electrode (TOBE) using an electrostrictive ceramic PNM-PT was presented in [15]. Recently, a 62+62 PZT row-column array integrated in a hand-held probe was demonstrated [16]. Commercial row-column probes using PZT are available from Vermon and Verasonics (RC6gV Row-Column Array Transducer), using 128+128 rows and columns with a $6\,\mathrm{MHz}$ center frequency. A similar prototype probe with 128+128 rows and columns with a $12\,\mathrm{MHz}$ center frequency was introduced by Daxsonics.

PZT probes are often fabricated using the dice-and-fill method [17], where the kerf is limited by the width of the dicing blade to around $15\,\mu\mathrm{m}$ [18]. This imposes restrictions on the transducer design, especially at higher frequencies where the element width becomes comparable to the kerf for small pitch probes. Furthermore, high frequency probes require a small thickness of the PZT material, which makes such probes increasingly difficult to fabricate. Therefore, alternatives to fabricating probes using PZT are needed.

B. Capacitive micromachined ultrasonic transducers

One alternative to the piezoelectric transducer is the capacitive micromachined ultrasonic transducer (CMUT) based on silicon microfabrication. It was first demonstrated using sacrificial release methods [19], and later with fusion bonding (also called direct bonding) [20]. This structure uses a thin vibrating plate or membrane for transmit and receive. CMUTs, when compared to conventional PZT based transducers, do not have any significant self-heating due to low internal loss and high thermal conductivity [21], [22] and also provides higher frequency bandwidth [23]. These transducers can be made with microfabrication and the single CMUT units, referred to as cells, can be defined through the use of simple lithographic processes. The devices can therefore be made smaller, and the pitch can more easily be controlled than what is usually possible with dicing for piezoelectric transducers. This allows a pitch of $\lambda/2$, which minimises grating lobes [24], to be more easily kept for higher center frequencies, and easier integration with integrated circuits on chip.

Since the first use for imaging [25] CMUTs have been successfully used for 1D linear array probes by several academic and industrial research groups [26]–[36] and more recently such probes have become commercially available. The first 2D array using CMUTs based on the row-column addressing scheme had 32+32 elements fabricated using wafer fusion bonding, where the cavities and membranes were both made with silicon nitride. Since then several row-column CMUTs have been designed and fabricated with a variety of different methods, such as sacrificial release [37], [38] using a TOBE array architecture, adhesive wafer bonding [39], [40], fusion bonding [16], [41]–[44] and anodic bonding [45]–[47]. Some of these arrays have been integrated in hand-held probes, presented in [16] as a 62+62 RCA 2D CMUT probe together with a corresponding PZT probe for comparison, and in [44] where two 92+92 RCA 2D CMUT probes with and without integrated diverging lenses are presented. These probes showed the potential for using CMUTs for RCA arrays and demonstrated that such probes can attain similar performances as a PZT probe made using the same dimensions. However, it was found that capacitive substrate coupling [48] and the resistance of the electrodes [49] used for the CMUT devices is important for the performance of large CMUT arrays and needs to be optimized.

C. Requirements for large array designs

When designing large RCA arrays there are a number of important criteria to ensure optimal performance. The pressure emitted along each element, rows and columns, and across neighbouring elements should be uniform. If this is not the case, the pressure field of the array when performing imaging will not match simulated fields and can be detrimental to the image quality. Likewise, the receive sensitivity of both rows and columns should be equal to ensure even performance.

Considering the first requirement, the distribution of the electric potential along the CMUT elements becomes important. When a high frequency excitation (AC) signal is applied on a long element the electrode resistance can have significant influence on the transmit pressure uniformity. If the resistance is too high the system will behave as a low-pass filter and attenuate the applied signal along the element. This effect can be modelled as a delay line [49]. The value of the dimensionless product ωRC, being a combination of the angular excitation frequency, ω, the element electrode resistance, R, and the total capacitance of the element, C, can be used as a criterion to minimise adverse attenuation. To keep a uniform pressure distribution, the potential drop along the element is set to a maximum of 1 %. This corresponds to an ωRC value of

$$\omega RC \leq 0.35. \tag{1}$$

This can also be expressed in terms of the the sheet resistance, $R_\square$, the element or electrode length, L, and the capacitance per area, C'

$$\omega R_\square C' L^2 \leq 0.35. \quad (2)$$

This allows one to predict the signal drop and adjust the design parameters without the need to directly measure the electrode resistance. It furthermore shows that the choice of $R_\square = \rho/t$, which depends on the electrode resistivity, ρ, and thickness, t, becomes much more crucial for larger arrays as the effect scales with the area, L^2.

The second requirement regarding the sensitivity depends on how well the substrate coupling or cross-talk between elements [48] can be suppressed. CMUT elements which are fabricated with a silicon substrate often utilise a silicon-on-insulator (SOI) wafer during fabrication with an insulating layer to separate bottom electrodes from the handling substrate [37], [42], [50], [51]. This allows the elements to capacitively couple to each other through the substrate, giving rise to parasitic capacitance which will lower the receive sensitivity of the array [52]. A way to mitigate this could be to use increase the signal path length between the elements partially separating them with an etching process [53]. An alternative solution could be removing the electrical path through the substrate completely [39], [54], which can be realized by utilising an insulating handling substrate as an alternative to silicon.

For the first effect, the ωRC criterion sets requirements for the resistivity and thickness of the material used to fabricate the top and bottom electrodes and the fabrication techniques needed. Two main types of electrodes determines which techniques that can be used; metal electrodes, which will require processes with a low processing temperature or thermal budget, and silicon-based electrodes allowing for a higher thermal budget.

If silicon is used as bottom electrode material, a limit of around $10^{21}\,\mathrm{cm}^{-3}$ is set as the highest doping level, which can be achieved, corresponding to a resistivity of $10^{-4}\,\Omega\,\mathrm{cm}$ [55]. This can prove problematic for long arrays when considering ωRC. CMUTs fabricated with a silicon substrate using fusion/direct bonding process [56], [57] requires a high temperature post annealing step at $> 1000\,^\circ\mathrm{C}$ to fuse the dielectric insulation layer with a top plate. Such a device is illustrated in Fig. 1(a) fabricated on an SOI wafer. The temperature step makes this technique incompatible with metal bottom electrodes, and one has to rely on the low resistivity of doped silicon for the bottom electrodes and increase the electrode thickness to keep the resistance sufficiently low.

Bottom electrodes made of metal are typically fashioned e.g., in Al, Cr, or Au. In comparison to doped silicon, metal electrodes have a resistivity on the order of $10^{-6}\,\Omega\,\mathrm{cm}$ [58], which being two magnitudes lower than doped silicon, will reduce resistance problems and be sufficient for most applications, depending on the electrode shape. The low thermal budget limits the number of techniques which can be used for CMUTs to mainly three types. 1) Adhesive polymer bonding [59] using e.g., BCB [39], see Fig. 1(b). This is a versatile method for joining different types of substrates and top plates with a polymer spacer, which can be patterned as a standard UV-sensitive resist and used with both silicon and metal bottom electrodes. 2) Sacrificial release methods [60], which can be used with both metal and silicon electrodes, see Fig. 1(c). For this technique an intermediate sacrificial layer between the substrate and a dielectric layer is dissolved, leaving CMUT cavities covered by a dielectric plate. 3) Finally, anodic bonding [61] can be used, where bottom electrodes are made by etching CMUT cavities into a glass substrate, metal electrodes are deposited, and the substrate is bonded to a silicon top plate, see Fig. 1(d). This has a maximum processing temperature of $375\,^\circ\mathrm{C}$.

In contrast, CMUT top electrodes are typically made using a wafer-bonded plate of silicon, which is then covered with a thick metal layer of low resistivity. For typical electrode designs the electrode resistance will not affect the pressure field [53]. The metal deposition happens as one of the last process steps and is not affected by previous high temperature processes. It can therefore be used in combination with various types of CMUTs.

Ideal structures for low resistance signalling would be combining a glass wafer patterned with CMUT cells, using a metal bottom electrode [45], [47], [61]. Such devices using dielectrics for the membrane or etching for structuring cell cavities can, however, display stability issues and dielectric charging of the device [62]–[64]. However, a fabrication process based on an SOI substrate together with the local oxidation of silicon (LOCOS) technique [57] and fusion bonding have been shown to exhibit little to no charging [51]. The structure is illustrated in Fig. 1(a). The LOCOS process, when used for CMUT fabrication, allows for reduced parasitic capacitance, high dielectric strength, good uniformity and tightly controllable CMUT dimensions and vacuum gap height down to under 10 nm precision due to the predictability of the oxide thickness [65].

D. New CMUT design

In this paper, we present a hand-held RCA CMUT based probe for volumetric imaging with a potential use in medical applications. This device is based on a LOCOS process fabricated on a doped silicon wafer, in combination with fusion bonding to an SOI wafer and a physical separation of the bottom electrodes to reduce cross-talk between the elements [54]. This is realised using a deep reactive-ion etching (RIE) based process. For improved mechanical stability, while also providing element-to-element insulation and low capacitive substrate coupling, a borofloat glass wafer is anodically bonded to the backside of the elements after the separation process. The separated electrodes have a cross-section of almost $100 \times 100\,\mu\mathrm{m}^2$ which combined with a highly doped silicon substrate will mitigate delay-line effects.

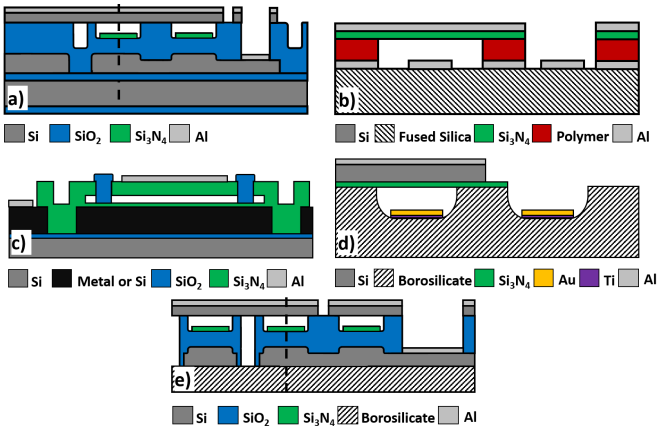

Figure 1. Cross-sectional view of five different RCA CMUT fabrication technologies. (a) Fusion bonding of a silicon top plate to a LOCOS structure grown on a doped SOI substrate. Figure is adapted from [51]. (b) Adhesive polymer bonding of a silicon nitride membrane to a fused silica wafer with metal electrodes using polymer [39]. (c) Sacrificial release method using a metal or doped silicon bottom electrode, where cavities are formed by etching of a sacrificial layer encapsulated in silicon nitride. (d) Anodic bonding of an insulated top plate to a structured borosilicate glass substrate with metal electrodes [45]. (e) A combination of a silicon top plate fusion bonded to a LOCOS structure and a borosilicate glass plate anodically bonded to the backside. A doped silicon substrate separated with a trench etch is utilised as bottom electrodes.

The fusion-anodic double bonded structure is illustrated in Fig. 1(e) and as a cross-sectioned 3D sketch in Fig. 2. This device should benefit from stable high-performing CMUTs while also exhibiting low element-to-element coupling and high transmit pressure uniformity.

The paper is organized as follows: Section II is divided into a part *A* and *B*. The first part introduces the general design parameters of the presented CMUT array. The second part describes in detail the cleanroom fabrication of the device. Section III describes the assembly of the transducer probe. Results from the thermal, electrical and acoustical characterizations are presented in Section IV and discussed in Section V. Ultrasound imaging and measurements of sensitivity and penetration depth performed with the probe is described in Section VI. Finally, a conclusion is drawn in Section VII.

II. Design & Fabrication

A. Design

The RCA array design is a symmetrical square with 190 row elements and 190 column elements used for beamforming, divided into rectangular segments of 95 odd and even elements of alternating pad numbering on each side of the array.

A 3D sketch of the corner of an array is shown in Fig. 2. This cut-off of the array shows four orthogonal top and bottom electrodes highlighted in orange and blue, respectively, as well as the underlying cells and element separation. Bordering the central region of the array are four apodization regions as shown in the boxed section in Fig. 3, which each are accessible from a single contact pad in the corners of the array not shown in

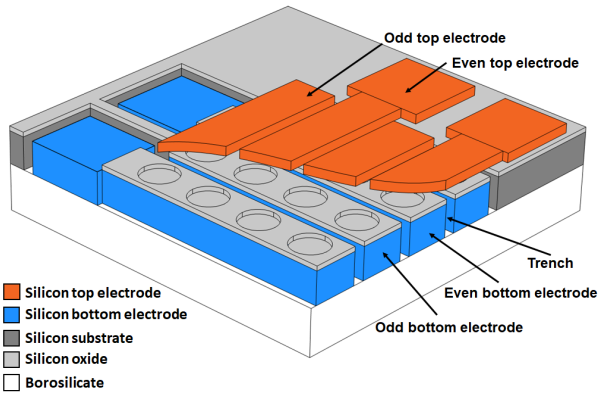

Figure 2. A 3D sketch of the corner of an RCA array. The orthogonal blue bottom electrodes and orange top electrodes, made of silicon, are shown encapsulating the structured oxide layer with the circular CMUT cells. A wide trench is shown separating the bottom electrodes laterally, and a glass substrate (borosilicate) is shown bonded to the backside of the structure.

Fig. 2. This raises the total channel count to 192+192. The apodization is incorporated into the design to round off the signal towards the edges of the array with a Hann window function. This reduces the relative signal amplitude from 1 to 0 at the edge of the apodization region and thereby suppresses side lobes and ghost echoes. The signal is decreased over nine cells with an increasing inter-cell distance. The RCA CMUT array is designed with an element pitch of $95\,\mu\mathrm{m}$. The elements are $92.5\,\mu\mathrm{m}$ wide and contains a single row of circular cells which are $70\,\mu\mathrm{m}$ in diameter. If the plate thickness is chosen as $4.0\,\mu\mathrm{m}$ and the vacuum gap height is $196\,\mathrm{nm}$ this will give a center frequency of $9.15\,\mathrm{MHz}$ in air and $\approx 4.5\,\mathrm{MHz}$ in immersion using a pull-in voltage of $190\,\mathrm{V}$. The center frequency in immersion was found using the following equation

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1+\beta}} = \frac{1}{\sqrt{1+\Gamma\dfrac{\rho_m}{\rho_p}\dfrac{a}{h}}} \tag{3}$$

obtained by Lamb [66] and revisited by Amabili and Kwak [67]. Here, ω_r/ω_0 is the ratio between the resonant frequency in water and vacuum, β is the added virtual mass incremental factor (AVMI) consisting of the medium to plate density ratio, ρ_m/ρ_p, the radius, a, and the thickness of the plate, h. Γ is the non-dimensionalised added virtual mass incremental (NAVMI) factor which can take multiple values depending on the clamping conditions. The value stated by Lamb [66] of $\Gamma = 0.6689$ is chosen. The center frequency in immersion is predicted to be around $49\,\%$ of the center frequency in air ($9.15\,\mathrm{MHz}$ at $80\,\%$ of $V_{\text{pull-in}}$).

The center frequency, gap height, and plate thickness were determined using the finite element method (FEM) simulators OnScale and COMSOL.

The remaining design parameters are stated in Table I. The previously discussed delay-line effect above in Section I, will theoretically for one element of the 190+190 RC array, using $C = 23.6\,\mathrm{pF}$ and $R = 556\,\Omega$, approximately equal

$$\omega RC \approx 0.38 \tag{4}$$

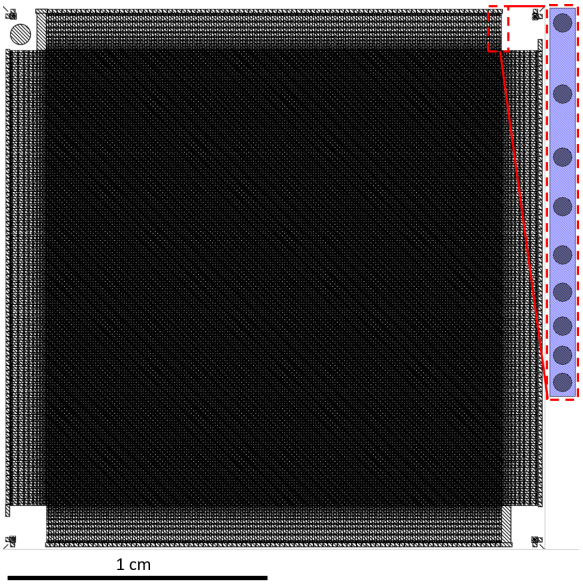

Figure 3. Design overview of the 190+190 RCA CMUT array. The integrated apodization region designed to roll-off the signal towards the edge is seen in the inset.

Table I
DESIGNED TRANSDUCER PARAMETERS

Design parameter		Unit
Array		
Number of elements	190+190	
Element pitch	95	µm
Element width	92.5	µm
Kerf	2.5	µm
Element length	20.95	mm
Element thickness	100	µm
Apodization length	1.45	mm
Apodization cell length	9	
Array side length	2.14	cm
Center frequency in air	9.15	MHz
Center frequency in immersion	4.5	MHz
CMUT cell		
Cell diameter (round)	70	µm
Distance to cell kerf	11.25	µm
Plate thickness	4.0	µm
Al electrode thickness	400	nm
Vacuum gap	196	nm
Nitride thickness	55.6	nm
Insulation oxide thickness	375	nm
Post oxide thickness	825	nm
Pull-in voltage	190	V

at a frequency of $4.5\,\mathrm{MHz}$. This corresponds to a drop in signal along the element of approximately $1.2\,\%$. This is deemed an acceptable loss considering that the silicon substrate used for fabrication has a resistivity of $0.025\,\Omega\,\mathrm{cm}$ or less. For the top electrodes, the resistance is $R = 15\,\Omega$ and an ωRC value of less than 0.01 is found showing that metal electrodes are efficient in suppressing this effect.

The four inch wafer design features eight RCA arrays each with a footprint measuring $2.14 \times 2.14\,\mathrm{cm}^2$. Furthermore, 16 smaller 16+16 RCA arrays as well as linear arrays are included for electrical and acoustical testing.

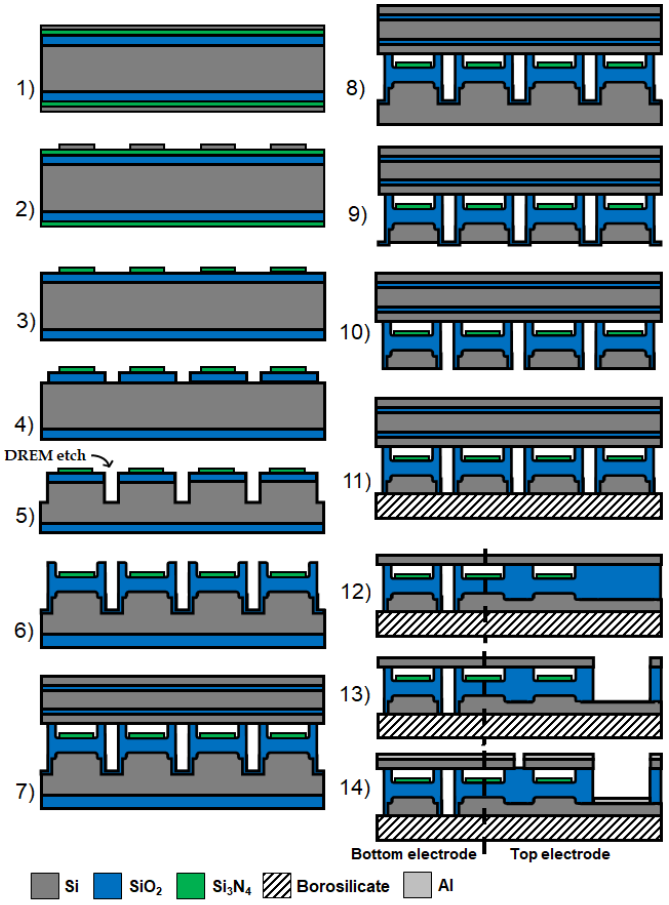

Figure 4. Fabrication process flow for the row-column CMUT array. The dashed line in drawings 12) through 14) represents a shift in perspective between a cross-section of the bottom electrode (to the left) and the top electrode (to the right).

B. Fabrication

The fabrication of the CMUT array was based primarily on the LOCOS process [57] for structuring the cells and fusion bonding for encapsulation. As mentioned in Section II-A a physical trench separation was used to isolate the bottom elements of the array. The separation etching process used was developed at DTU Nanolab and is a modified 3-step Bosch process called deposit, remove, etch, multistep (DREM) [68]. The multiple steps have been fine-tuned to eliminate mask-erosion during etching (achieving so-called "infinite" selectivity [68]) and preserve scallop and hole uniformity even for high aspect ratios.

The fabrication process illustrated in Fig. 4 started with a highly doped $525\,\mu\mathrm{m}$ thick silicon wafer having a resistivity of $\rho < 0.025\,\Omega\,\mathrm{cm}$ corresponding to a donor doping level, N_d, of $10^{19}\,\mathrm{cm}^{-3}$. First a silicon dioxide layer of $375\,\mathrm{nm}$, used for insulation, was grown in a dry thermal oxidation process at $1100\,^{\circ}\mathrm{C}$, then a low pressure chemical vapour deposition (LPCVD) silicon nitride of $55.6\,\mathrm{nm}$ and an LPCVD

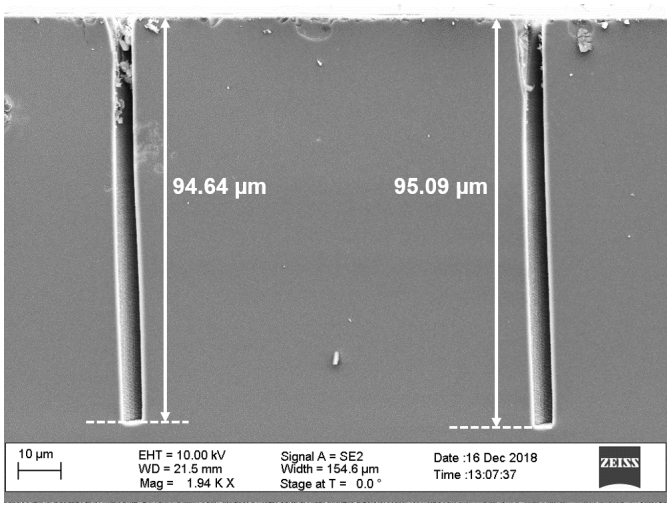

Figure 5. Scanning electron microscope image illustrating the DREM trench etched in step 5) of the fabrication process.

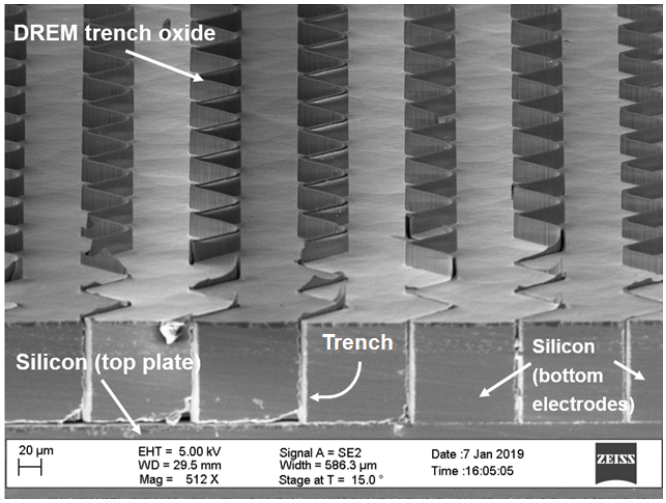

Figure 6. Scanning electron microscope image of a test structure illustrating the cross-section of the backside of the wafer after step 9), before polishing. The exposed DREM trench oxide walls separating the bottom electrodes are clearly visible. This was also previously presented in [54].

polycrystalline silicon (poly-Si) layer was deposited on top (using Tempress horizontal furnaces), see step 1). The poly-Si layer was then patterned with circles representing cells in a photolithography step with the diameter stated in Table I and etched using a poly-Si etching solution (HNO_3:BHF:H_2O (20:1:20)), step 2). The pattern was transferred into the nitride using hot phosphoric acid (H_3PO_4 at $160\,^{\circ}\mathrm{C}$) and the poly-Si masking layer was stripped using RIE (SPTS Pegasus). This will leave the nitride masking pads on top of the oxide in place of the cavities, step 3).

At this point the oxide surface was patterned with resist and trenches were etched using RIE (advanced oxide etcher (AOE) STS MESC Multiplex ICP) into the oxide in the kerf between the elements to expose the underlying silicon substrate, step 4). Then, the DREM process was performed at a temperature of $-19\,^{\circ}\mathrm{C}$ using the SPTS Pegasus for a trench etch depth of around $100\,\mu\mathrm{m}$, step 5). These can be seen in Fig. 5, where deep straight trenches have been etched in silicon.

The wafer was then cleaned in RCA cleaning solution, and a second thermal oxidation process was performed in a wet oxidizing environment at $1100\,^{\circ}\mathrm{C}$ to grow the post oxide to a total thickness of $825\,\mathrm{nm}$, step 6). This formed the cavities through the LOCOS process with a gap height of $196\,\mathrm{nm}$, excluding the nitride pad thickness. The device wafer was RCA cleaned again together with a poly-silicon-on-insulator (PSOI) wafer [69], which has been custom made to match the desired plate thickness. The structured device wafer and the PSOI wafer were then fusion bonded together, illustrated in step 7), at $400\,^{\circ}\mathrm{C}$ with a tool pressure of $4\,\mathrm{bar}$ (performed on a Süss SB6 wafer bonder) and then subsequently annealed at $1100\,^{\circ}\mathrm{C}$ for $70\,\mathrm{min}$ to form permanent silane bonds.

The oxide layer on the backside of the bonded wafer stack was removed with a BHF solution, step 8). Most of the silicon substrate was removed using lapping (Logitech PM5 Lapping & Polishing System), leaving approximately $150\,\mu\mathrm{m}$ to $180\,\mu\mathrm{m}$. To completely separate the bottom electrodes from the backside the remaining $50\,\mu\mathrm{m}$ to $80\,\mu\mathrm{m}$ was etched using RIE (advanced silicon etcher (ASE) STS MESC Multiplex ICP)), step 9), exposing the trenches and oxide from step 6), seen in Fig. 6.

The backside surface was then polished to remove the free-standing oxide and to reduce the roughness necessary for anodic bonding, step 10). This was performed using a Logitech CM62 Orbis CMP (Chemical Mechanical Polishing) machine. A $500\,\mu\mathrm{m}$ thick borosilicate glass wafer was anodically bonded to the $100\,\mu\mathrm{m}$ thick electrodes on the backside using a four step voltage ramp ($200\,\mathrm{V}/400\,\mathrm{V}/600\,\mathrm{V}/800\,\mathrm{V}$) at an elevated temperature of $375\,^{\circ}\mathrm{C}$, step 11). The top poly-Si layer, two buried oxide (BOX) layers and the bulk of the PSOI handle wafer were then removed in a combination of dry and wet etching using RIE, BHF, KOH at $80\,^{\circ}\mathrm{C}$, and BHF, which left only the poly-Si top plate, step 12). The dashed line illustrates a shift in the perspective between the cross-section of the bottom electrode to the left of the line and the top electrode to the right, respectively.

Holes for contacting the bottom electrode pads were made by etching through the poly-Si plate and post oxide using a resist mask with a RIE ASE process tool, step 13). During this process it was discovered that not all post oxide was etched for some of the contact pads due to the formation of a sulphur compound, see Fig. 7. Multiple cleaning steps with RCA, HCl, HNO_3, and Piranha were tried without success. As a result, this prevented a complete access to the incomplete pads making wire bonds unreliable and lowering the electrode yield. The wafer surface was then coated in $400\,\mathrm{nm}$ aluminium (utilizing a Temescal FC-2000 e-beam evaporator), which was patterned using a PES Al etching solution [70] to form the top metal electrodes. Finally, the plate was etched through on the ASE to separate the top electrodes completely, step 14).

The last step was dicing the wafer using a (DISCO DAD-321) dicing saw.

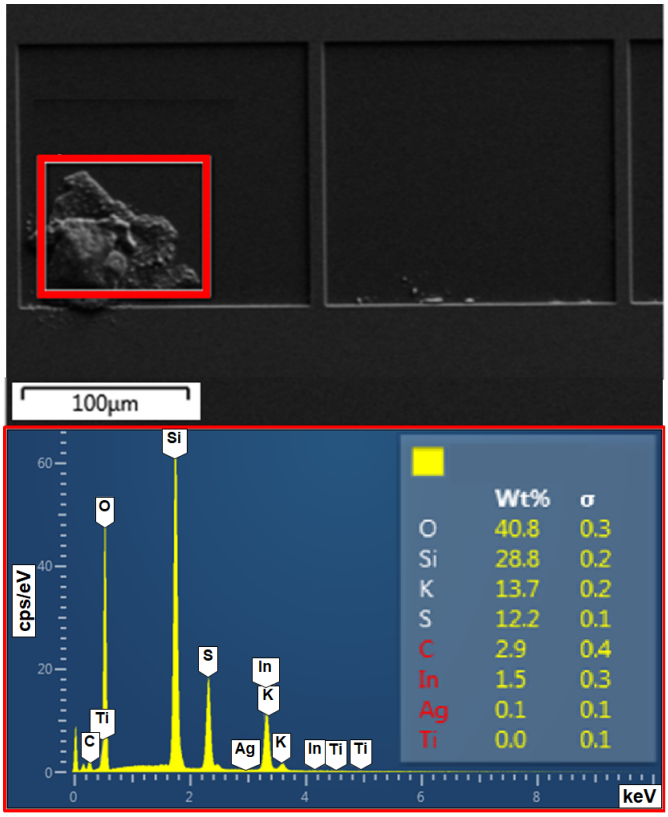

Figure 7. Scanning electron microscope image showing an example of a particle consisting of a sulphur compound. This partially blocks the SiO_2 etching process in step 13) in Fig. 4 which prevents the opening to some of the bottom electrodes, and leads to problems in the definition of top electrodes in step 14), thus reducing the yield. The inset represents an EDX spectrum of the area marked in red, showing a high concentration of sulphur and potassium which is not observed in particle-free areas.

III. Assembly

The diced array chip was mounted and glued to a rigid-flexible four-armed printed circuit board (PCB), and wire bonding was performed to connect the individual element contact pads on the chip to the PCB. The top and bottom electrodes were designated as rows and columns, respectively, and each of the four sides of the chip, of either odd or even elements, were wire bonded to each PCB arm for a total of 384 channel connections, depicted in Fig. 8. The assembly of the transducer probe was done at the facilities of BK Medical (State College, PA, USA). A tall glob-top dam was glued to the edges of the rigid PCB to ensure that neither the wire bonds or the chip were damaged by external mechanical stresses during scanning or assembly. The array was then encapsulated by filling the dam with room temperature vulcanizing (RTV) silicone, RTV664, described in more detail in [16], [71]. The thickness of the RTV directly on top of the chip was 0.485 mm on average. On top of the shield, the final layer of RTV was 0.595 mm

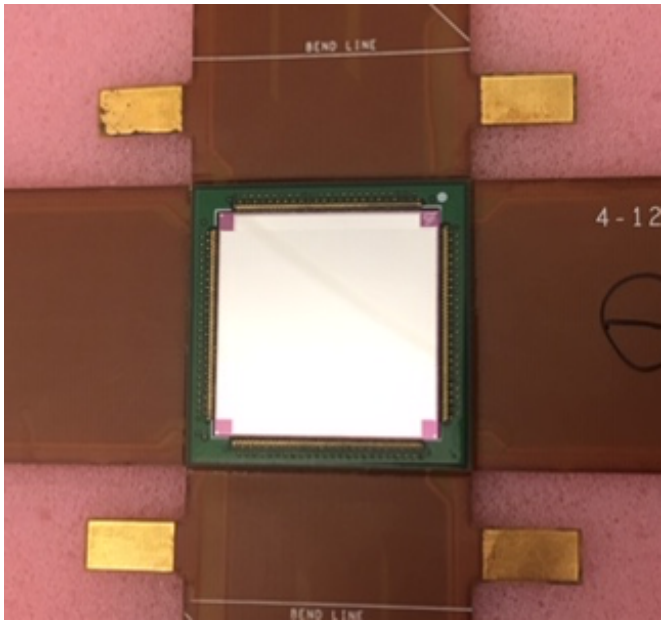

Figure 8. Flex rigid PCB with the mounted and wire bonded chip. Each arm of the PCB is connected to a section of the array; north and south, east and west, corresponding to even and odd rows or columns, respectively.

on average. The attenuation of the RTV was 2.3 dB/mm at 4.5 MHz, so the total one-way attenuation is 2.5 dB for this array. An aluminised polymer film (12.5 µm polypropylene with a sub-micron thick aluminium layer), used as electromagnetic interference (EMI) ground shielding, was applied before the silicone cures and the PCB was mounted in a 3D milled PPSU probe nose-piece. Another layer of silicone was applied to the array surface and levelled to the probe edge, thus completely sealing and insulating the array.

The four sections of the rigid-flexible PCB were folded and connected to four preamplifier boards. The boards are each equipped with six MAX14822 16-channel high voltage (HV)-protected transimpedance low noise active amplifier ICs with a bandwidth of 45 MHz. These amplifiers are capable of supplying high voltage AC in transmit (TX) and receive (RX) individually on each channel of the probe superimposed on a DC bias. Each board has support for 96 channels, and two boards, pairing either the odd or even element, are connected with board-to-board connectors. Each pair of amplifier boards were connected to a 192 odd or even channel coaxial scanner cable (BK Medical, Herlev, Denmark). The board pairs were then shielded in Kapton and copper tape. Two cooling hoses for inlet and outlet were then encapsulated along with the boards within the probe shell by two 3D milled shell pieces, effectively sealing the transducer probe handle. The assembled probe is seen in Fig. 9.

Figure 9. Assembled three-part custom 3D milled PPSU probe handle. The RCA CMUT array is buried underneath the stack of RTV silicone, aluminium polymer foil and silicone covering the nose piece. The two cooling hoses can be seen protruding beside the scanner cables.

IV. Characterization

A. Thermal

The probe handle is fitted with an inlet and outlet tube for air cooling of the amplifier boards during scanning. An experiment was performed to evaluate the cooling capability during idle mode and when emitting a suitable imaging sequence. Temperature measurements were performed in air, see Fig. 10, on the side of the assembled probe body and on the front sole of the nose piece using two FLIR C2 thermal imaging system cameras mounted on a frame. These measurements showed that the idling temperature of the probe when supplied with a DC voltage of 190 V, corresponding to 160 V at the chip level, gives an average temperature at $\approx$ 31 °C on the sole (blue) and $\approx$ 36.5 °C on the side (red) after 25 min. An imaging sequence with a synthetic aperture (SA) using 18 elements, 192 emissions, a pulse repetition frequency of 12 kHz, and 75 V peak-to-peak was then used as excitation signal. The surface temperature of the sole rose $\approx$ 2 °C during the measurement, reaching a maximum average of 32.8 °C (yellow) after 5 min. The probe side had a stable surface temperature of $\approx$ 36.5 °C (purple) throughout the measurement which is caused by the underlying voltage regulator on the amplifier boards. The temperature rise and surface temperature of the transducer body and sole when idling and imaging were both found acceptable for experimental external use below the FDA and DS/EN limits for scanning [72]. The airflow inside the current probe design is, however, likely restricted by the preamplifier boards and their shielding and the internal temperature is probably higher than what is measured on the surface.

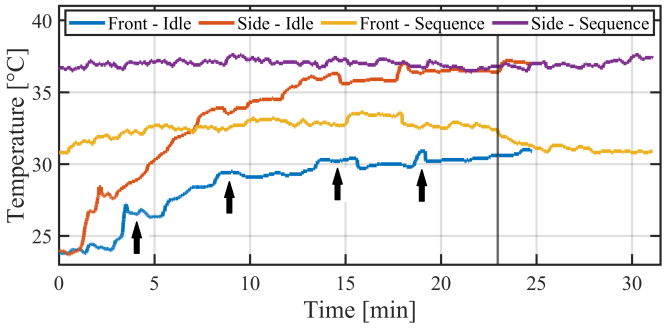

Figure 10. Thermal measurements performed on the assembled probe body using a setup with two FLIR C2 thermal imaging system cameras. These were mounted on a frame to measure the temperature on the probe from the side and the front. Measurements were performed in idle mode with an applied bias voltage and when using an imaging sequence. The vertical line at 23 min indicates when the sequence used for excitation is stopped. The slight variations in the dataset, illustrated by the black arrows for the blue curve, are caused by the thermal cameras performing automatic re-calibration during the measurements.

B. Electrical

The electrical response of the CMUT array has been characterized before it was mounted in the probe handle using impedance measurements. These were performed using an Agilent 4294A Precision Impedance Analyzer. During the measurements the bias voltage was supplied through a bias tee by a Keithley 2410 sourcemeter.

Measurements were performed on separate linear test arrays and single test elements located in the corners of the 192+192 arrays to provide an accurate pull-in voltage for the array. The DC voltage supplied by the sourcemeter was varied between 0 V to 200 V while a 50 mV AC voltage from the impedance analyser was superimposed on top. The voltage sweep could then be used to find the pull-in voltage. With a constant supplied DC bias the array showed a stable performance and exhibited no charging. This showcases the effectiveness of the LOCOS fabrication process.

Fig. 11 shows measurements, performed on a test element, of the impedance magnitude and phase from 1 MHz to 25 MHz for an applied voltage of 150 V. A pull-in voltage of 186 V was measured which compares well with the designed pull-in voltage of 190 V.
The measured center frequency was 9.25 MHz at a bias of $\approx$ 80 % of the pull-in voltage which is in good agreement with the COMSOL simulated value of 9.15 MHz in air. Using the same bias voltage the electromechanical coupling factor is calculated to be $k^2 = 4.5\,\%$.

C. Acoustical

Acoustical characterization of the assembled probe was performed on the experimental research scanner SARUS [73] using the approach in [74] and the transducer impulse responses were determined as described in [75].

1) Impulse response

The one-way impulse and two-way pulse-echo responses were

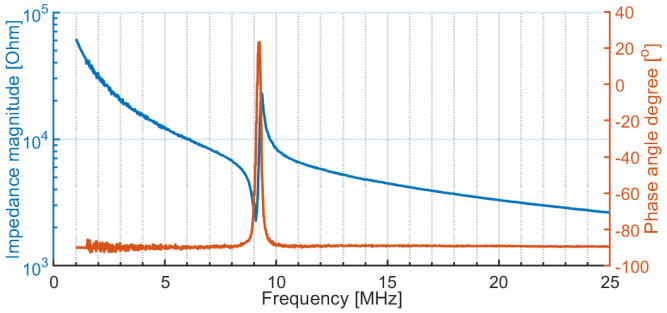

Figure 11. Impedance measurement of a CMUT test element at 150 V DC bias and 50 mV AC. The resonance and anti-resonance peaks are seen at 9.1 MHz and 9.3 MHz, respectively.

measured by submerging the probe in deionized (DI) water with either a hydrophone or a planar steel reflector placed 35 mm from the transducer surface, respectively. Emitting and receiving was done with one element at a time for all rows and columns, respectively. The DC bias was set to 160 V and the AC excitation voltage up to 150 V peak-to-peak (±75 V) . The voltage levels were set to reflect the measured pull-in voltage mentioned in Section IV-B. The hydrophone used to measure the pressure in immersion was an Onda HGL-0400 hydrophone connected to an Onda AH-2010 amplifier.

The elements have been grouped into three categories depending on their maximum impulse response values from the acoustic measurements in transmit and in receive, see Fig. 12. The overall element yield of the finished array in transmit has been measured to 109 (57.4 %) for the rows and 123 (64.7 %) for the columns. This was based on elements with an impulse response maximum value over $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$, designated as functional elements. The semi-functional elements have a lower response between $2.9 \times 10^{14}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (52 rows and 32 columns) and the defect or not connected (NC) elements have less than $2.9 \times 10^{14}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (29 rows and 35 columns). Only the functional elements have been used for further acoustic characterization. The element yield measured in receive (pulse-echo) was 65.8 % and 43.7 % for functional rows and columns, respectively, with a cut-off at $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$. For semi-functional elements it was 1.1 % and 12.6 % for rows and columns, respectively, with a cut-off at $6.5 \times 10^{-5}\,\mathrm{V\,V^{-1}}$, and for NC elements the yield was 33.2 % for rows and 43.7 % for columns. The yield problems seem to be related to the formation of the sulphur compound mentioned in Section II-B.

The average transmit impulse response of the functional rows and columns can be seen in Fig. 13. The solid blue and red lines represent the response measured in $\mathrm{Pa\,V^{-1}\,s^{-2}}$ of the rows and columns, respectively, and the dashed lines in the same colour represent the envelope of the signal. The maximum impulse response values are between $1.3 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ to $2.5 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$. It can be seen from the data that the signal transmitted from the rows is ≈ 55 % of the response of the columns. The received pulse-echo signal

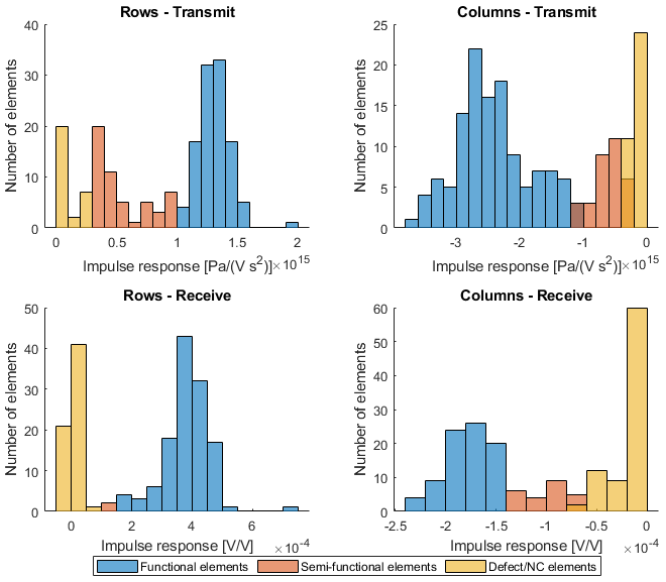

Figure 12. Histogram of impulse response of all row and column elements. The elements are grouped into three categories depending on their maximum impulse response values.

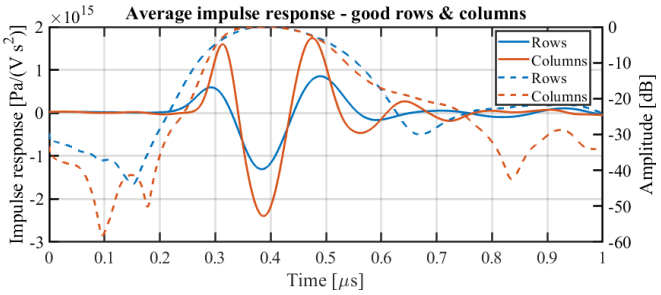

Figure 13. Average impulse response (TX) and the normalized envelope of the functional row and column elements with amplitudes above $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$.

in Fig. 14 shows a longer pulse with a more pronounced ringing for the rows compared to the transmit measurements. The ratio between the row and column main peaks is around 2.4 with the rows now having a higher amplitude than the columns. The average transmit sensitivity of the rows and columns was found to be $1.3 \pm 0.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (rows) and $2.4 \pm 0.6 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (columns), with a total average of $1.9 \pm 0.7 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$. The sensitivity for the pulse-echo measurements was $3.8 \pm 0.7 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ (rows) and $1.8 \pm 0.2 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ (columns), with a total average of $3.0 \pm 0.2 \times 10^{-4}\,\mathrm{V\,V^{-1}}$.

2) Center frequency and uniformity

The center frequencies of the rows and columns were found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses of the transmit and pulse-echo signals plotted in Fig. 15 and Fig. 16 using the expression:

$$f_c = \frac{\sum_{i=0}^{N/2} S(i\,f_s/N) \cdot i\,f_s/N}{\sum_{i=0}^{N/2} S(i\,f_s/(N))} \tag{5}$$

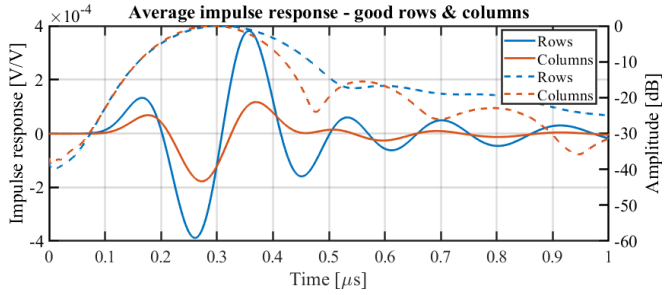

Figure 14. Average impulse response (PE) and the normalized envelope of the functional row and column elements with amplitudes above $1.4\times10^{-4}\,\mathrm{V\,V^{-1}}$.

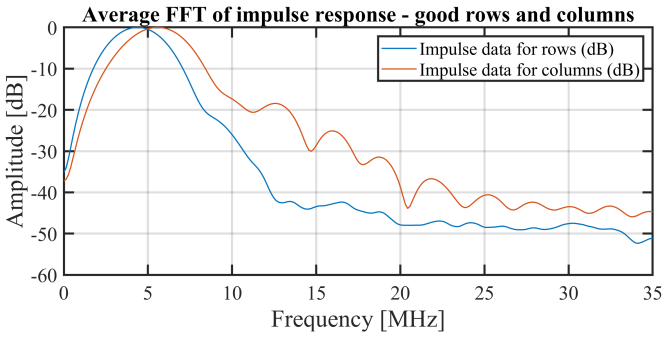

Figure 15. Average spectra of the impulse response in transmit (TX) of the functional row and column elements with amplitudes above $1.1\times10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$.

with f_s being the sample frequency of 70 MHz and N the number of frequency bins in the spectrum, S. In Fig. 17 the extracted center frequency f_c is plotted for each element showing the uniformity across the array in transmit (Fig. 17(a)) and pulse-echo (Fig. 17(b)). The average center frequencies of the functional row- and column elements were 5.0 ± 0.1 MHz (rows) and 6.85 ± 0.30 MHz (columns) with the total average being 6.0 ± 0.9 MHz in transmit, and 5.3 ± 0.2 MHz (rows) and 5.5 ± 0.5 MHz (columns) with the total average of 5.3 ± 0.4 MHz in pulse-echo. The peak frequency was also extracted from the spectral data and gave an average of 5.0 ± 0.6 MHz and 4.5 ± 0.5 MHz in transmit and pulse-echo, respectively, also seen in Table II.

These values correspond reasonably well with the predicted resonance frequency in immersion of 4.5 MHz in both transmit and pulse-echo. However, the center frequency of the columns in transmit and the rows in pulse-echo both lie between 1 MHz to 1.5 MHz higher when biased at 86 % of $V_{\text{pull-in}}$.

3) Bandwidth

The frequency bandwidth (BW) of each element was found at the -3 dB and -6 dB points of the Fourier transformed impulse responses of the transmit and pulse-echo measurements, respectively. The mean BW for the functional rows and columns in transmit was 3.3 ± 0.2 MHz and 4.2 ± 0.4 MHz, respectively, with a total mean of 3.7 ± 0.5 MHz. In pulse-echo the mean BW was 4.2 ± 0.1 MHz and 5.3 ± 0.8 MHz for rows and columns, respectively, with a total average of 4.6 ± 0.7 MHz.

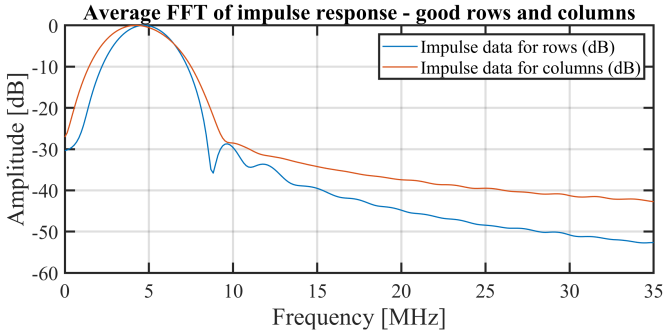

Figure 16. Average spectra of the impulse response in pulse-echo (PE) of the functional row and column elements with amplitudes above $1.4\times10^{-4}\,\mathrm{V\,V^{-1}}$.

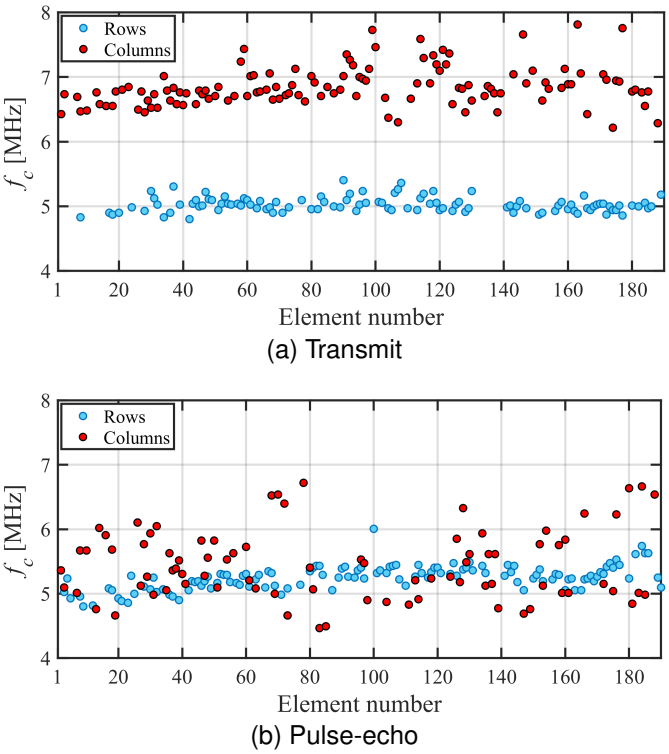

Figure 17. Extracted center frequencies across the array for each element in transmit (a) and pulse-echo (b). The frequencies were found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses. The average center frequency of functional row and column elements in the probe is 6.0 ± 0.9 MHz in transmit and 5.3 ± 0.4 MHz in pulse-echo.

The relative fractional bandwidth for the rows and columns in transmit was 65.2 ± 3.7 % and 60.7 ± 4.0 % with a total mean of 62.8 ± 4.5 %. In pulse-echo this was 79.5 ± 3.7 % and 96.4 ± 87.7 % for the rows and columns, respectively, with a total mean of 86.2 ± 10.4 %.

4) ωRC - Pressure uniformity

The effect of the electrode resistance on the transmit uniformity has been estimated by measuring the pressure field along the top and bottom electrodes. The pressure field was mapped in immersion by moving the Onda HGL-0400 hydrophone in the x-y plane in steps of 0.5 mm with a distance of 5 mm

Table II
RESULTS OBTAINED FROM ACOUSTICAL MEASUREMENTS OF THE PROBE IN TRANSMIT AND PULSE-ECHO

	Transmit			Pulse-echo		
Parameter	Row	Column	Total	Row	Column	Total
Center frequency [MHz]	5.03 ± 0.11	6.85 ± 0.30	5.99 ± 0.94	5.25 ± 0.19	5.45 ± 0.54	5.33 ± 0.38
Peak frequency [MHz]	4.38 ± 0.16	5.59 ± 0.25	5.02 ± 0.64	4.70 ± 0.09	4.21 ± 0.39	4.50 ± 0.35
Center frequency bandwidth [MHz]	3.28 ± 0.19	4.16 ± 0.37	3.74 ± 0.53	4.17 ± 0.13	5.27 ± 0.80	4.61 ± 0.74
Relative fractional bandwidth [%]	65.23 ± 3.69	60.68 ± 3.98	62.82 ± 4.47	79.47 ± 3.66	96.40 ± 8.77	86.23 ± 10.37
Sensitivity [$\mathrm{PaV^{-1}s^{-2}}$]/10^{15}	1.3 ± 0.1	2.4 ± 0.6	1.9 ± 0.7	—	—	—
Sensitivity [$\mu\mathrm{VV^{-1}}$]	—	—	—	380 ± 70	180 ± 20	300 ± 20

from the transducer surface. This creates a grid of 49×49 measurements with an area of $24.5\,\mathrm{mm} \times 24.5\,\mathrm{mm}$ which completely captures the array. A 4-cycle sinusoidal $6.5\,\mathrm{MHz}$ pulse with an amplitude of $V_{\mathrm{AC}} = \pm 75\,\mathrm{V}$ has been used to excite three evenly spaced row elements and three column elements. The pressure maps shown in Fig. 18 are each an average of three elements and the plots have been normalized to their maximum value and log compressed. In Fig. 18(a) for the top electrodes (rows), it is seen that the pressure distribution is even along the elements. The mean value of the first and last 1/4 part of the element has been calculated as an estimate of the uniformity as $-2.4\,\mathrm{dB}$ and $-2.9\,\mathrm{dB}$. Fig. 18(b) depicts the bottom electrodes (columns) for which similar values have been calculated as $-1.9\,\mathrm{dB}$ near the contact pads and $-3.0\,\mathrm{dB}$ near the end of the elements. This corresponds to a drop to $88 \pm 16\,\%$ of the initial amplitude, or $12\,\%$ attenuation. The ωRC value for the measurement frequency is 0.55, which corresponds to a drop to $97.6\,\%$ of the initial value or $2.4\,\%$ attenuation. The measured attenuation is larger than the predicted value which could be caused by the low yield of the orthogonal elements providing the grounding during the measurement.

This value can be compared to an attenuation of $74\,\%$ measured on a previously fabricated 92+92 RCA array with a center frequency of $4.5\,\mathrm{MHz}$ and a bottom electrode resistivity of $\lessapprox 0.1\,\Omega\,\mathrm{cm}$ [49].

The data depicted in Fig. 18, which is an average of three emitting row and column elements, exhibited large variations in the recorded pressure and this likely causes the large standard deviations of the attenuation.

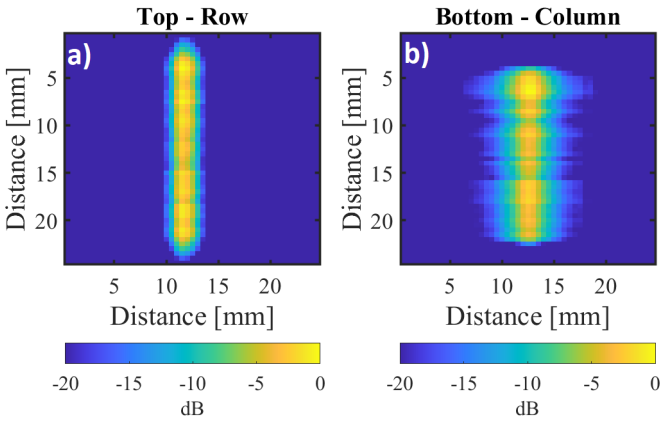

Figure 18. Average peak pressure field of elements excited at $6.5\,\mathrm{MHz}$. The pressure is mapped for three different top and bottom electrodes using a hydrophone and an average is shown in (a) for top electrodes (rows) and in (b) the bottom electrodes (columns). The pressure is uniform along the top electrodes. The pressure measured along the bottom electrodes shows a clear maximum value in the top of the contact but remains mostly uniform along the element. The measured pressures have been normalized to $489.8\,\mathrm{kPa}$ and $554.7\,\mathrm{kPa}$ for the rows and columns, respectively.

V. IMAGING

The imaging capabilities of the probe was evaluated using the SARUS system by scanning a wire phantom, a cyst phantom, and a stereolithography 3D printed hydrogel phantom with isolated $205 \times 205 \times 80\,\mu\mathrm{m}^3$ embedded cavities, which function as point scatter targets [76]. The scatterers were placed in a $6 \times 4 \times 4$ grid with a spacing of $2.05\,\mathrm{mm}$. 3D imaging was performed using a SA sequence with 96 row and 96 column emissions and three orthogonal planes are shown in Fig. 19. From this the resolution of the point spread function (PSF) could be determined in the axial direction as $0.82\,\lambda$ ($0.1880\,\mathrm{mm}$) and in the lateral direction as $1.72\,\lambda$ ($0.3936\,\mathrm{mm}$). The side-to-main lobe level was fairly high at $-11.90\,\mathrm{dB}$ due to scattering from the phantom surrounding the point cavities. The resolution is visualized in Fig. 20, which depicts three different planes from the volumetric scan of a wire phantom. The phantom is a matrix of wires immersed in water with little attenuation. The x-z (lateral) plane shows the wires as horizontal lines, the $y-z$ (azimuthal) plane shows two columns of wire cross-sections as dots, and the $x-y$ (transverse) plane depicts a single wire. The resolution in this phantom was in the axial direction $1.16\,\lambda$ ($0.2654\,\mathrm{mm}$) and in the lateral direction $1.56\,\lambda$ ($0.3562\,\mathrm{mm}$). The contrast was $-16.90\,\mathrm{dB}$ due to the many missing elements.

The penetration depth was found at the point when the signal to noise ratio (SNR) attains a value of $0\,\mathrm{dB}$, shown in Fig. 21, and was experimentally obtained by imaging a tissue mimicking cyst phantom with an attenuation of 0.5 dB/[MHz cm] using a SA sequence with 96+96 emissions at $6.5\,\mathrm{MHz}$. This excitation frequency was chosen to use the full bandwidth of the probe to gain the best possible resolution. The transducer reaches a depth of $150\,\lambda$, where the wavelength λ in this phantom is $0.2375\,\mathrm{mm}$. This corresponds to a penetration depth of $3.6\,\mathrm{cm}$ again due to the many missing elements.

VI. DISCUSSION

The amplitude of the impulse response of the row elements during pulse-echo measurements was found to be a factor of

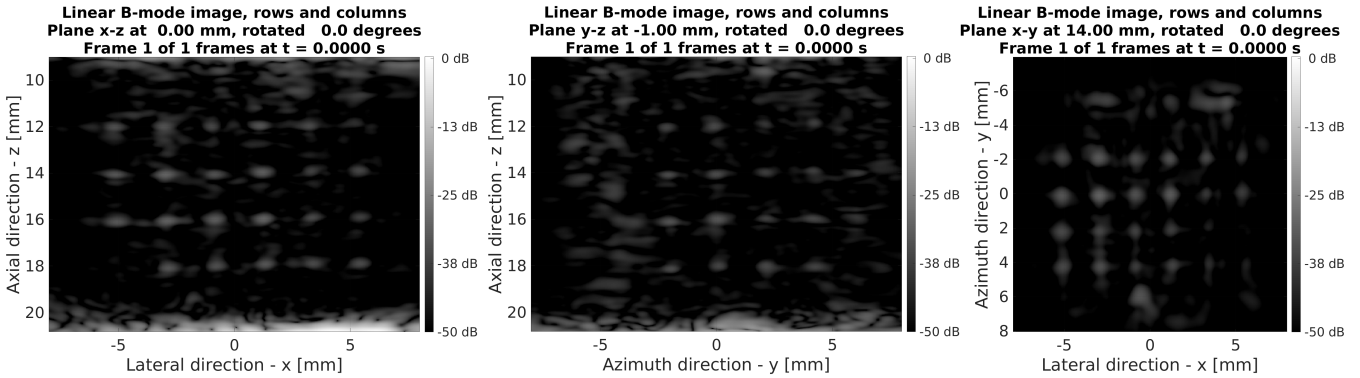

Figure 19. Point spread functions in three orthogonal planes obtained from a stereolithography 3D printed hydrogel phantom using the 190+190 transducer probe. The phantom has a grid of $6 \times 4 \times 4$ isolated $205 \times 205 \times 80\,\mu\text{m}^3$ embedded cavities, which function as scattering point targets.

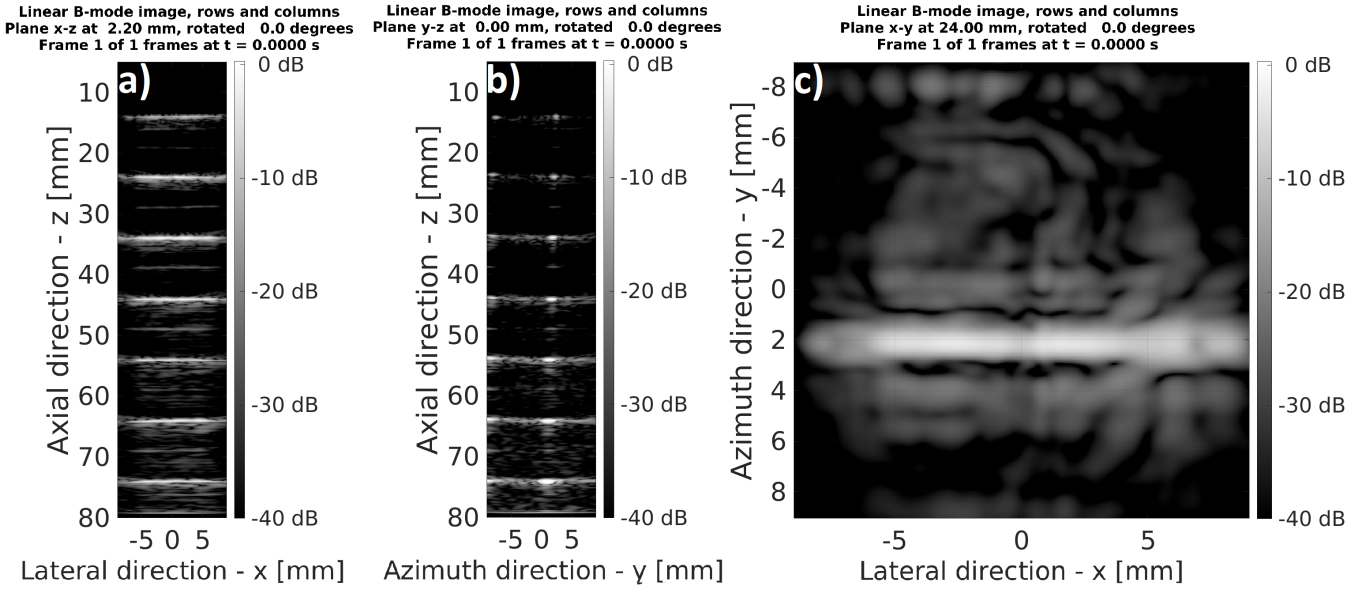

Figure 20. Imaging planes of a wire phantom obtained using the 190+190 transducer probe. The three different planes depict (a) the horizontal wires along in the x-direction (x-z plane), (b) two columns of wire cross-sections (y-z plane) and (c) the top of a single wire (x-y plane).

2.4 times higher than the columns. This reduction in receive sensitivity for columns is likely due to the aforementioned parasitic capacitance in Section I-C. Since a glass wafer is used as the substrate instead of an SOI wafer during fabrication this effect was hypothesised to be lower as the coupling should be significantly reduced. However, the $100\,\mu\text{m}$ thick and $\approx 2.1\,\text{cm}$ long bottom electrodes separated by a $2.5\,\mu\text{m}$ wide trench can potentially contribute to an increased parasitic capacitance, which ultimately will lower the sensitivity. During the transmit measurements, a reduction in the transmit sensitivity for the rows by a factor of 1.92 compared to the columns was observed. It is also observed that in transmit, the columns have a higher center frequency than the rows even though all CMUT cells have the dimensions, and the plate thickness is uniform across the array. These effects are currently not understood and is the subject for future work.

A previously fabricated 92+92 RCA CMUT probe [77], which is based on an SOI wafer substrate with a $20\,\mu\text{m}$ device layer, exhibited a reduction of the bottom electrode receive sensitivity by a factor of around 3.3. The presented 190+190 fusion-anodic bonded probe shows a clear improvement in receive sensitivity over the previous SOI wafer based fusion bonded design. The presented probe has, however, shown problems with element yield and demonstrated only around $55\,\%$ working elements. This is believed to be due the formation of a sulphur compound in the processing chamber when etching an opening to the bottom electrodes. Ultimately, this prevented some wire bonds from making proper contact and lowered the overall yield and performance of the probe. Solving this problem requires further investigation and tuning of the cleaning processes, the chamber conditioning, and the gas composition used when performing the silicon oxide etching process on the samples.

Ultrasound imaging showed that the probe is capable of performing 3D volumetric imaging, but the low SNR limits the penetration depth to $150\,\lambda$ corresponding to $3.6\,\text{cm}$. The

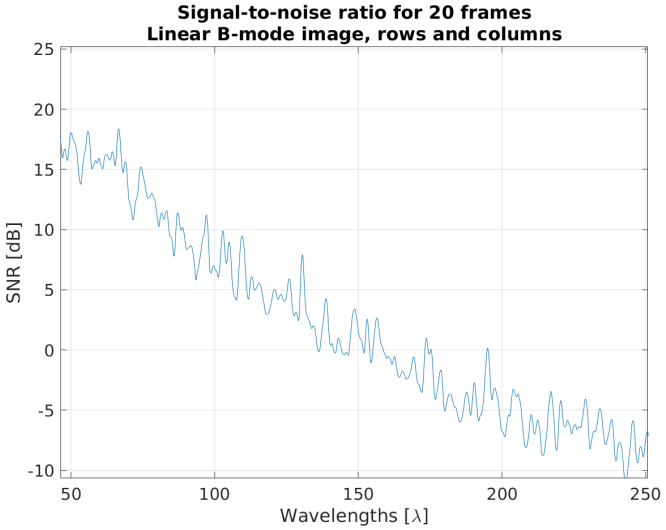

Figure 21. SNR of the 190+190 RCA probe for a tissue mimicking phantom phantom with an acoustical attenuation of 0.5 dB/[MHz cm]. The penetration depth is roughly $150\,\lambda$ when the SNR reaches 0, corresponding to $3.6\,\mathrm{cm}$ as the wavelength in this phantom is $0.2375\,\mathrm{mm}$ when imaging with a frequency of $6.5\,\mathrm{MHz}$.

imaging performance of the probe is naturally also limited by the low number of working elements, which affects the main-to-side lobe levels. It is, however, demonstrated that full volumetric imaging is possible, and the point spread function is isotropic in all three directions with a volume rate comparable to normal 2D imaging with a linear array probe.

The probe has sub-$\lambda/2$ pitch and normally there would be no advantage in linear array imaging, but for second harmonic imaging grating lobes could be avoided at the double center frequency. Such measurements have, however, not yet been conducted.

VII. Conclusion

The developed hand-held 190+190 RCA CMUT ultrasound probe with integrated edge apodization and active cooling was fabricated using a standard fusion bonding process utilizing LOCOS in combination with an anodic bonding process and an etch separating the bottom electrodes. The array was wire bonded and mounted in a 3D milled PPSU probe handle. The element yield of the elements with an impulse response higher than $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$ in transmit and pulse-echo, respectively, was a total of $61.1\,\%$ and $54.7\,\%$. This was in part due to the formation of a sulphur compound in the bottom electrode contact holes during fabrication. To improve the yield the microfabrication process can be further optimised. The formation of the sulphur compound can be avoided by further optimising the process conditions including temperature control, chamber pre-conditioning and gas flow. Characterization of the probe in transmit showed that the maximum value of the averaged impulse responses of the columns was a factor of 1.8 times higher than the rows in transmit. In pulse-echo the maximum value of the averaged impulse responses of the rows was a factor of 2.4 times higher than the columns due to the substrate coupling effect. Compared to a previously fabricated probe, where the averaged maximum impulse response of the rows were a factor of 3.3 times higher than the columns, the substrate coupling effect has been reduced. The weighted center frequencies were $6.0 \pm 0.1\,\mathrm{MHz}$ in transmit and $5.3 \pm 0.5\,\mathrm{MHz}$ in pulse-echo with relative fractional bandwidths of $62.8 \pm 4.5\,\%$ and $86.2 \pm 10.4\,\%$, which is close to the designed center frequency of $4.5\,\mathrm{MHz}$. The attenuation of the transmit pressure along the top electrodes was found to be insignificant. For the bottom electrodes the transmit pressure was attenuated by $12\,\%$, which is a clear improvement when compared to previous results where an attenuation of $74\,\%$ was measured. This demonstrates that using a highly doped ($< 0.025\,\Omega\,\mathrm{cm}$) $100\,\mu\mathrm{m}$ thick substrate in the fabrication process can solve the previously mentioned problems concerning high electrode resistances and the formation of delay lines. The imaging performance of the probe was determined using a 3D printed point scatter phantom, a wire phantom, and a cyst phantom showing for the first two a reasonable contrast of $-11.90\,\mathrm{dB}$ to $-16.90\,\mathrm{dB}$, considering the many missing elements, and the resolution was $0.82\,\lambda$ to $1.72\,\lambda$ (axial) and $1.56\,\lambda$ to $1.72\,\lambda$ (lateral), demonstrating the 3D volumetric capabilities with a near isotropic point spread function. The SNR measured on the tissue mimicking cyst phantom was low, resulting in a penetration depth of around $3.6\,\mathrm{cm}$ due to many missing elements. In conclusion, the fabrication process using thick highly doped silicon bottom electrodes and an insulating glass substrate has improved the pressure uniformity when emitting with the bottom electrodes and reduced the substrate coupling effect.

Acknowledgement

This work is financially supported by Innovation Fund Denmark (7050-00004B).

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