**DTU Library**

# A Design Methodology for High-Voltage, Highly-Integrated Switched-Capacitor Power Converters, and Implementation at 48 V-12 V, 23 W/cm$^3$ and 93.5 % Peak Efficiency

**Henriksen, Markus Mogensen; Larsen, Dennis Øland; Muntal, Pere Llimós**

Link back to DTU Orbit

# A Design Methodology for High-Voltage, Highly-Integrated Switched-Capacitor Power Converters, and Implementation at 48 V-12 V, 23 W/cm³ and 93.5 % Peak Efficiency

Markus Mogensen Henriksen, *Student Member, IEEE,* Dennis Øland Larsen, *Member, IEEE,* Pere Llimós Muntal

*Abstract*—In this work a design methodology and key considerations for high-voltage and highly-integrated switched-capacitor power converters is presented. The design methodology describes the power losses in high-voltage applications, where switching losses and gate-driver losses start becoming dominant compared to fully integrated, low voltage and low power applications. The design methodology is applicable for any highly-integrated switched-capacitor topology. To verify the design methodology a 48 V-12 V ladder switched-capacitor power converter in a 180 nm SOI BCD process, with external capacitors is implemented. The floating gate-drivers and a clock controller responsible for the power switch control are also presented. The peak efficiency of the proposed power converter is measured to be 93.5 %, and 24.5 W maximum output power, resulting in a power density of 23 W/cm³.

*Index Terms*—High-voltage, switched-capacitor converter, integrated power converter, power losses, data center application

## I. Introduction

**H**IGH-VOLTAGE power converters have traditionally been inductor based and implemented using discrete components. This method can achieve high efficiency for a wide range of voltages and currents [1]–[3]. The main drawbacks include bulky and expensive inductors and a high-voltage rating requirement for the power switches, since they need to handle the full input voltage, in most topologies. In the pursuit of increasing the power density of power converters together with recent advancements in high-voltage semiconductor technology, highly-integrated power converters are becoming interesting in applications in which so far the discrete power converters are dominating [4]–[14]. In this work highly-integrated power converters refer to power converters with an integrated power stage and gate-drivers and high-voltage refers to converter input voltages that exceeds the maximum voltage of the digital logic cells used in the given fabrication process. These applications include power converters in LED drivers, servers in data centers or dc-dc converters in automotive. Some of the advantages of highly-integrated power converters are a reduced production cost and

an increased power density. The increase in power density comes partially from the monolithic integration itself and that the switching frequency can be increased leading to smaller discrete passive components. The main disadvantages are complicated integrated circuit (IC) design and robustness challenges from parasitic inductance and resistance due to the interface with the IC [15]. The highly-integrated power converters are traditionally switched-capacitor power converters with discrete capacitors [16]. In the switched-capacitor power converters, low resistance power switches connects capacitors in different configurations in multiple clock phases to realize various voltage ratios dependent on the topology. This means that the maximum voltage across the power switches is usually lower compared to traditional inductor-based power converters, leading to the possibility of using lower voltage
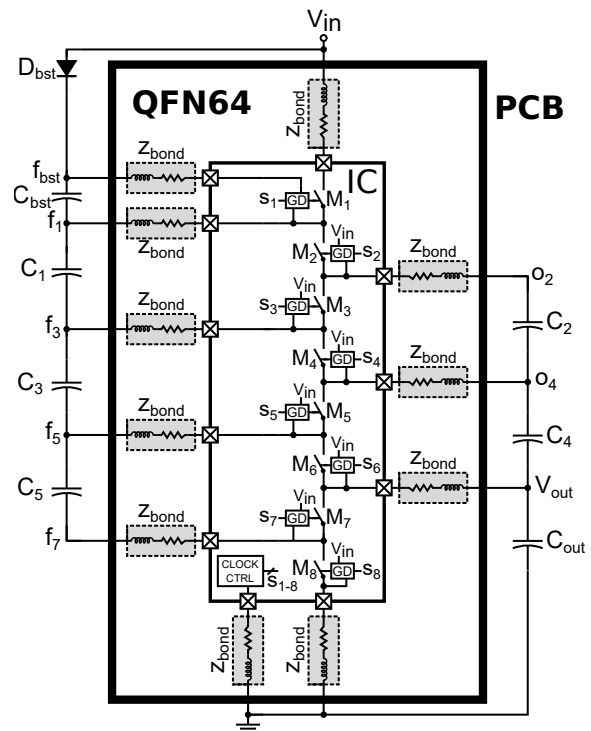
Fig. 1. A switched-capacitor power converter with an integrated power stage, gate-drivers and clock controller and external capacitors showing the bonding wire parasitics in the QFN64 chip package.

This article has been accepted for publication in IEEE Transactions on Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2023.3288592

TRANSACTION ON POWER ELECTRONICS, REGULAR PAPER SPECIAL SECTION ON SWITCHED CAPACITOR CONVERTERS SCCS
2

devices with better on-resistance while also leading to a lower V-A product figure-of-merit [17]. The hard-charging of the capacitors in the switched-capacitor power converter lead to high capacitor peak currents, which increases the RMS current of the external capacitors. To lower these peak currents hybrid switched-capacitor topologies, using one or multiple inductors to achieve soft-charging, has gained interest recently [7], [8], [18], [19]. The compatibility of a switched-capacitor topology to achieve resonant and soft-charging using a single inductor is documented in [20] and [21]. These hybrid converters have mostly been discrete solutions [22]–[24] but also highly-integrated hybrid converters have been published [25]–[27].

In 2021 [6] presented a $48\,\mathrm{V}$ to 3-3.6 V highly-integrated 4:1 hybrid Dickson power converter for automotive applications with a high peak efficiency of $95.3\,\%$ and a single $4.7\,\mu\mathrm{H}$ inductor. The use of a Dickson switched-capacitor power converter ensures the conversion from $48\,\mathrm{V}$-$12\,\mathrm{V}$, while adding an inductor enables regulation down to the desired output voltage. The work in [6] deals with some of the challenges of high-voltage, highly-integrated switched-capacitor converter such as safe start-up and floating gate-driver design. In 2022 [7] presented a $48\,\mathrm{V}$ to $1\,\mathrm{V}$ hybrid converter combining a 3:1 ladder converter and a capacitor assisted dual-inductor filter. It achieves a peak efficiency of $91.1\,\%$ and is able to operate at a switching frequency of $5\,\mathrm{MHz}$, meaning that the inductor size can be decreased to $2 \times 0.82\,\mu\mathrm{H}$. In 2023 [25] presented a single-inductor multi-stage (SIMS) hybrid converter. It achieves a wide input voltage range of $5\,\mathrm{V}$ to $24\,\mathrm{V}$ while providing a regulated output voltage range of $2.8\,\mathrm{V}$-$4.2\,\mathrm{V}$. It achieves this by cascading two highly-integrated switched-capacitor converter stages connected by a single inductor and having 4 operating modes to achieve a high peak efficiency of $94.8\,\%$ and a maximum output power of 21 W. Both [6], [7] and [25] discusses how to introduce inductive elements to improve on the switched-capacitor power converter performance, combining the high conversion ratio capabilities of the switched-capacitor converter with the soft-charging and output voltage regulation benefits of the buck converter. These works do however not discuss in detail the proper design methodology for the switched-capacitor power converter design itself. The work in [17] discusses in great detail some of these considerations but is mostly focused on fully integrated and low voltage applications, where especially gate-driver losses can mostly be neglected. In [28] a sizing methodology for fully integrated switched-capacitor converters maximizing efficiency under area and load power constraints is presented. The work in [28] does however not deal with conditions where the power converter input voltage exceeds the power switch and flying capacitor voltage ratings. It does also not provide any new insight when discrete flying capacitors are used such as in highly-integrated switched-capacitor power converters.

This work presents a design methodology and the key considerations when designing high-voltage, highly-integrated switched-capacitor converters and demonstrates the approach by designing a switched-capacitor power converter. The methodology can be used for any highly-integrated switched-capacitor power converter topology. This includes the optimal sizing of the power switches by defining the power losses in the switched-capacitor power converter also including the gate-driver losses which start becoming dominant in high-voltage applications and the optimal external discrete capacitors scaling. Section II presents the highly-integrated switched-capacitor power converter fundamentals, presenting the various power losses and reformulates them as functions of total switch area, switching frequency and load current to allow for optimization for high efficiency. It also derives and presents a novel expression for the optimal number of external capacitors to use for a given printed circuit board (PCB) capacitor footprint area derived by Lagrange Multipliers, which can be used for any switched-capacitor converter topology using discrete flying capacitors. Section III shows the implementation of a $48\,\mathrm{V}$-$12\,\mathrm{V}$ ladder highly-integrated switched-capacitor power converter with integrated floating gate-drivers, a clock controller and the optimization method for the design of the integrated power stage designed in a $180\,\mathrm{nm}$ Silicon-On-Insulator (SOI) process. Section IV presents the experimental measurement results of the $48\,\mathrm{V}$-$12\,\mathrm{V}$ highly-integrated switched-capacitor power converter showing the efficiency measurements for various output load currents and switching frequencies, transient load response, switching node at maximum output load and thermal performance and compares it to the proposed model and the simulation results. Section V discusses the experimental results and compares it to other designs. Finally, section VI concludes the work.

## II. HIGHLY-INTEGRATED SWITCHED-CAPACITOR POWER CONVERTER METHODOLOGY

In Fig. 1 a switched-capacitor step down converter with a fixed voltage ratio of 4:1 using a ladder topology can be seen. The power converter consists of an integrated power stage, gate-drivers and clock controller. The capacitors are external multi layer ceramic capacitors (MLCC) since they offer higher capacitance density compared to on-chip capacitors. The power switches $M_1$-$M_8$ are driven by floating gate-drivers, which inputs, $s_1$-$s_8$, are the gate signals generated by the clock controller. The gate signals $s_1$, $s_3$, $s_5$ and $s_7$ are switched in phase ($\varphi_1$) and $s_2$, $s_4$, $s_6$ and $s_8$ are switched in phase ($\varphi_2$). The clock controller is responsible for clock generation and dead-time control between the two phases. In Fig. 1 the parasitic resistance and inductance from the wire bonding is also shown. These bonding wires affect the performance and reliability of the power converter [15]. The challenge of optimal design of both the size of the power switches and capacitors in switched-capacitor power converters is well
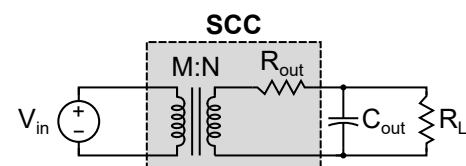


Fig. 2. Model of a switched-capacitor converter (SCC) with an ideal lossless transformer and a series resistance. $R_L$ represents a resistive load.

described in [29]. This work is mostly focused on low voltage, low power designs seeking to minimize the various power losses. These losses includes the charging and discharging of the capacitors and the conduction and switching losses of the power switches. The behavior of a switched-capacitor power converter can be modelled as seen in Fig. 2. Here the switched-capacitor converter is modelled as an ideal lossless transformer with a winding ratio of $M/N$ and an output series resistance $R_{out}$. The winding ratio $M/N$ relates to the fixed conversion ratio of the switched-capacitor converters, which is topology and implementation dependent. The series output resistance, $R_{out}$, is a function of both the power converter switching frequency and total switch conductance and can be approximated as:

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \qquad (1)$$

where $R_{SSL}$ and $R_{FSL}$ are the slow-switching limit resistance and fast-switching limit resistance respectively. The slow-switching limit models the losses when charging and discharging of the capacitors and is a function of both frequency and capacitor size:

$$R_{SSL} = \sum_i \frac{a_{c,i}^2}{C_i \cdot f_{sw}} \qquad (2)$$

where $a_{c,i}$ is the topology dependent capacitor charge multiplier vector describing the normalized charge for the respective capacitor, $C_i$, for each switching period. $f_{sw}$ is the frequency of the power converter. From (2) it can be seen that the losses are decreased by increasing capacitance and frequency.

The fast-switching limit, $R_{FSL}$ models the conduction losses of the power switches and is a function of the effective on-resistance of the power switches ($R_{ds}$).

$$R_{FSL} = 2 \left( \sum_i R_{ds,i} a_{r,i}^2 \right) \qquad (3)$$

where $a_{r,i}$ is the topology dependent switch charge multiplier vector describing the normalized charge for each power switch. $R_{ds,i}$ is the equivalent on-resistance of the power switches and is dependent on the process dependent area specific resistance of the power switch devices used and the total chip area designated for the power switches:

$$R_{ds,i} = \frac{K_{A,i}}{A_{sw} \cdot \frac{a_{r,i}}{\sum_k (a_{r,k})}} \qquad (4)$$

Where $A_{sw}$ is the total switch area, $K_{A,i}$ is the area specific resistance for the power switch device used. In the case of the ladder topology the maximum drain-source voltage of all the switches is the same:

$$V_{ds,max} = \frac{N}{M} V_{in} \qquad (5)$$

This means that the same devices can be used for all power switches and (3) can be written as:

$$R_{FSL} = \frac{2}{G_{tot}} \left( \sum_i \| a_{r,i} \| \right)^2 \qquad (6)$$

Where $G_{tot}$ is the total switch conductance, since all $R_{ds}$ in (4) have the same area specific resistance ($K_A$). The power

loss due to $R_{out}$ is dependent on the output load current and can be described as:

$$P_{rout} = I_{out}^2 \cdot R_{out} \qquad (7)$$

This means, that a target load current is required for choosing proper capacitor sizes and total switch area.

In high-voltage applications there are additional losses that should be taken into account, since their impact scales with the input voltage. These are the losses that are related to the parasitic capacitances of the power switches. The switching losses of the power switches are the losses from charging and discharging the output capacitor, $C_{oss} = C_{ds} + C_{dg}$ of the power switches. The switching loss of a single power switch can be described by:

$$P_{sw} = V_{ds} \cdot Q_{oss} \cdot f_{sw} \qquad (8)$$

Where $Q_{oss}$ is the total charge required for charging/discharging the drain-source capacitance of the power switch. The drain-source charge, $Q_{oss}$ can be rewritten into:

$$Q_{oss} = C_{oss} \cdot V_{ds} \qquad (9)$$

This capacitance is dependent on the type of power switch and the total area and be expressed as:

$$C_{oss} = \beta_{coss} \cdot \frac{A_{sw} \cdot a_{r,i}}{\sum_k a_{r,k}} \qquad (10)$$

Where $\beta_{coss}$ is the specific drain-source capacitance per switch area and $A_{sw}$ is the total power switch area. Using this we can rewrite (8) as dependent on both switching frequency and total power switch area:

$$P_{sw} = f_{sw} \cdot \sum_i \left( V_{ds,i}^2 \cdot \beta_{coss,i} \cdot \frac{A_{sw} \cdot a_{r,i}}{\sum_k a_{r,k}} \right) \qquad (11)$$

### A. Gate-Drivers

In highly-integrated power converters the power switches are controlled by integrated gate-drivers. The gate-drivers are referenced to the source of their respective power switch. The supply voltage of the gate-driver is dependent on the implementation. Various solutions for supplying floating gate-drivers have been investigated in other works, utilizing either charge-pump and bootstrapping techniques [4], [18] or internal supplies of the switched-capacitor converter itself [9]. The power consumption of the gate-drivers is therefore dependent on not only the size of the switch it is driving (gate capacitance of power switch) but also the input voltage, topology and implementation.

The total power consumption of all the gate-drivers can be described as:

$$P_{gd} = \sum_i (V_{DD,i} \cdot Q_{gg,i} \cdot f_{sw}) \qquad (12)$$

Where $V_{DD,i}$ is the supply voltage of the specific gate-driver and $Q_{gg,i}$ is the total gate charge required to charge the power switch gate capacitance. The gate-charge in (12) can be rewritten as:

$$Q_{gg,i} = C_{gg,i} \cdot V_{gs} \qquad (13)$$

Where $V_{gs}$ is the required gate-source voltage to turn on the power switch and $C_{gg,i}$ is the equivalent linear gate capacitance. The gate capacitance is dependent on the area specific gate capacitance ($\beta_{cgg}$), for the power switches used and the total switch area:

$$C_{gg,i} = \beta_{cgg,i} \left( \frac{A_{sw} a_{r,i}}{\sum_k a_{r,k}} \right) \tag{14}$$

The total gate-driver losses can then be described as:

$$P_{gd} = f_{sw} \cdot V_{gs} \sum_i \left( V_{DD,i} \cdot \beta_{cgg,i} \left( \frac{A_{sw} a_{r,i}}{\sum_k a_{r,k}} \right) \right) \tag{15}$$

These are only the losses related to driving the gate capacitance of the power switches. The quiescent current of the gate-driver is implementation dependent and contributes to the total gate-driver power consumption.

### B. External Flying Capacitor Sizing

For highly-integrated power converters with external capacitors it is often required to have multiple capacitors in parallel to fulfill the optimal design criteria described in [29]. This is a trade-off between improving the $R_{SSL}$ and using additional PCB footprint area for the discrete capacitors ($A_{cap}$). The scaling of each of the flying capacitors is topology dependent and can be expressed as:

$$C_i = C_i' \cdot \lfloor K_{c,i} \rfloor \tag{16}$$

Where $C_i$ is the total capacitance of each flying capacitor, $C_i'$ is the dc bias derated capacitance of each unit flying capacitor and $\lfloor K_{c,i} \rfloor$ is the topology dependent optimized capacitor component scaling parameter rounded down to the nearest integer. $K_{c,i}$ expresses the optimum number of unit flying capacitors ($C_i'$) in parallel for each flying capacitor. We find $K_{c,i}$ by using Lagrange Multipliers. The Lagrangian consists of an expression for the impedance at the slow-switching limit to be minimized $f(\mathbf{k})$, the constraint on the total capacitance area $h(\mathbf{k})$ and the Lagrange multiplier $\lambda$:

$$\mathcal{L}(\mathbf{k}, \lambda) = f(\mathbf{k}) + \lambda h(\mathbf{k}) \tag{17}$$

We want to minimize $f(\mathbf{k})$ under the constraint of the total area $h(\mathbf{k})$, these can be expressed as:

$$f(\mathbf{k}) = \sum_{i=1}^{N_{cap}} \frac{a_{c,i}^2}{K_{c,i} \cdot C_i'}$$
$$h(\mathbf{k}) = \sum_{i=1}^{N_{cap}} K_{c,i} A_{c,i} - A_{cap} \tag{18}$$

Where $A_{cap}$ is the total footprint area of all the external discrete capacitors, $A_{c,i}$ is the footprint area of each unit capacitance and $N_{cap}$ are the number of flying capacitors in the topology. Inserting (18) into (17):

$$\mathcal{L}(\mathbf{k}, \lambda) = \sum_{i=1}^{N_{cap}} \frac{a_{c,i}^2}{K_{c,i} \cdot C_i'} + \lambda \left( \sum_{i=1}^{N_{cap}} K_{c,i} A_{c,i} - A_{cap} \right) \tag{19}$$

Taking the partial derivative of $\mathcal{L}(\mathbf{k}, \lambda)$ with respect to $K_{c,i}$, setting it equal to zero and isolating for $K_{c,i}$ yields:

$$\frac{\partial \mathcal{L}}{\partial K_{c,i}} = \frac{-a_{c,i}^2}{K_{c,i}^2 C_i'} + \lambda A_{c,i} = 0$$
$$K_{c,i} = \frac{a_{c,i}}{\sqrt{\lambda A_{c,i} C_i'}} \tag{20}$$

We then take the partial derivative of $\mathcal{L}(\mathbf{k}, \lambda)$ with respect to $\lambda$, set it equal to zero and use the expression for $K_{c,i}$ found in (20):

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum_{i=1}^{N_{cap}} K_{c,i} A_{c,i} - A_{cap} = 0$$
$$= \sum_{i=1}^{N_{cap}} \left( \frac{A_{c,i} a_{c,i}}{\sqrt{\lambda A_{c,i} C_i'}} \right) - A_{cap} = 0 \tag{21}$$

Isolating $\sqrt{\lambda}$ in (21) yields:

$$\sqrt{\lambda} = \frac{1}{A_{cap}} \sum_{i=1}^{N_{cap}} \left( \frac{\sqrt{A_{c,i} a_{c,i}}}{\sqrt{C_i'}} \right) \tag{22}$$

Inserting (22) into (20) then yields the optimized expression for $K_{c,i}$:

$$K_{c,i} = \frac{A_{cap} \cdot a_{c,i}}{\sqrt{A_{c,i} \cdot C_i'} \cdot \sum_{j=1}^{N_{cap}} \left( \frac{\sqrt{A_{c,j} a_{c,j}}}{\sqrt{C_j'}} \right)} \tag{23}$$

Note that since $K_{c,i}$ depends on the capacitor charge multiplier vector $\mathbf{a_c}$ it is topology dependent. $K_{c,i}$ therefore tells for a given total capacitance footprint area, how many capacitors to put in parallel for each flying capacitor. This optimal capacitor scaling can be used for any highly-integrated switched-capacitor power converter topology.

### III. IMPLEMENTATION

To show how the presented power losses can be used to design high-voltage, highly-integrated switched-capacitor power converters a $48\,\text{V}$-$12\,\text{V}$ ladder topology switched-capacitor power converter is implemented in a $180\,\text{nm}$ SOI process. The integrated power stage and the sizing of the external flying capacitors are designed using the proposed sizing methodology presented in Section II. The proposed converter is intended as an intermediate power converter in applications such as automotive or data centers dc power bus. The output voltage of the implemented power converter is therefore unregulated. The schematic of the proposed design can be seen in Fig. 1.

### A. Flying Capacitors and Power Stage Design

For a 4:1 ladder topology, the charge multiplier vector, $\mathbf{a_c}$, describing the output normalized capacitor charge flow vector is:

$$\mathbf{a_c} = \left[ \frac{1}{4}, \frac{1}{4}, \frac{2}{4}, \frac{2}{4}, \frac{3}{4} \right] \tag{24}$$

For the ladder topology the voltage rating of each flying capacitor are all equal to $V_{C,max} = V_{out}$. This means that the same external discrete capacitor can be used for all flying
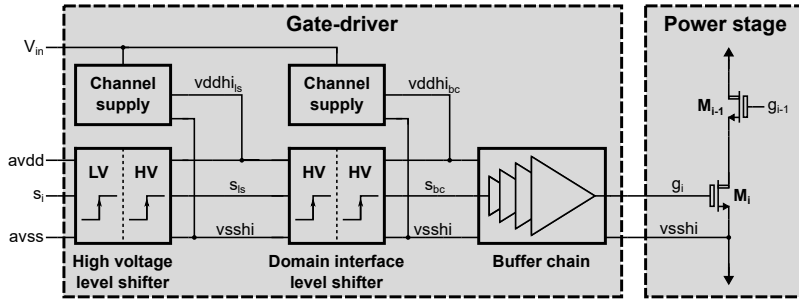
Fig. 3. Diagram of the implemented floating gate-driver for driving switches $M_1$-$M_8$.
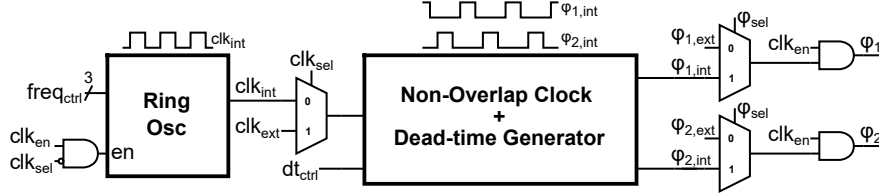


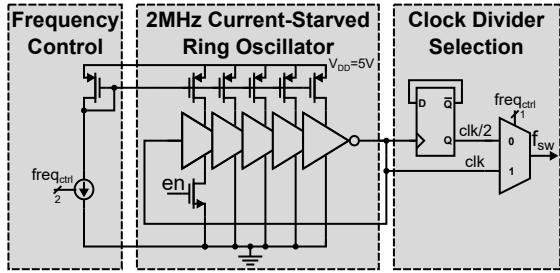Fig. 4. Digital clock controller with integrated ring oscillator, non-overlapping clock and dead-time generator.



Fig. 5. 2 MHz, 9-stage current-starved ring oscillator with 3-bit frequency selection.

capacitors. A total capacitance area of $A_{cap} = 22.5\,\mathrm{mm}^2$ was chosen for the footprint area of the capacitors and the GRM21BC71E106KE11, $10\,\mu\mathrm{F}$ MLC capacitors from Murata [30] are used. From [30] it can be seen that the the maximum frequency is around $2\,\mathrm{MHz}$, before becoming inductive and that it has a dc bias capacitance derating of $-73.1\,\%$ at $12\,\mathrm{V}$. Using (23) then leads to:

$$\lfloor K_c \rfloor = [1,\ 1,\ 2,\ 2,\ 3] \tag{25}$$

The total $12\,\mathrm{V}$ derated capacitance for each flying capacitor is therefore:

$$\mathbf{C_{fly}} = \begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \end{bmatrix} = \begin{bmatrix} 2.69\,\mu\mathrm{F} \\ 2.69\,\mu\mathrm{F} \\ 5.38\,\mu\mathrm{F} \\ 5.38\,\mu\mathrm{F} \\ 8.07\,\mu\mathrm{F} \end{bmatrix} \tag{26}$$

The power switches should be able to handle a maximum $V_{ds}$ voltage of $12\,\mathrm{V}$. Some margin is added and $20\,\mathrm{V}$ devices are used for the integrated power stage. The power switches are scaled by their switch charge multiplier vector for a 4:1 ladder topology:

$$\mathbf{a_r} = \begin{bmatrix} \dfrac{1}{4},\ \dfrac{1}{4},\ \dfrac{1}{4},\ \dfrac{1}{4},\ \dfrac{1}{4},\ \dfrac{1}{4},\ \dfrac{3}{4},\ \dfrac{3}{4} \end{bmatrix} \tag{27}$$

The switch conductance, and thereby the switch areas are then scaled by $a_r \cdot N$, where N is the conversion ratio. In this case meaning that $M_{7,8}$ should have three times the conductance of $M_{1-6}$. To further ensure safe operation during start-up the top switch ($M_1$) is chosen as a $60\,\mathrm{V}$ device instead. This device has a worse area specific resistance and a larger area specific capacitances ($\beta_{cgg}$, $\beta_{coss}$). This device is scaled such that the $R_{ds}$ of $M_1$ corresponds to that of $M_2 - M_6$.

The area specific gate capacitance ($\beta_{cgg}$) can be found from simulation by observing the charge required for turning on the transistor for different total switch areas. This simulation was performed for the used switches with a drain-source voltage of $12\,\mathrm{V}$ and a step voltage on the gate-source of the transistor. Similarly the area specific drain-source capacitance ($\beta_{coss}$) was found from simulation with a gate-source voltage of $0\,\mathrm{V}$ and a step voltage across the drain-source of the transistor. These parameters are used to designate the desired total switching area and which sets the requirements for the gate-driver capabilities.

### B. Gate-Driver Implementation

The structure of the designed gate-drivers can be seen in Fig. 3. These are based on the ones used in [9]. In this work two channel-supply generators consisting of a shunt-regulator generates a $5\,\mathrm{V}$ supply for a level shifter and a buffer chain referenced to the vsshi node, which is connected to the source of the respective power switch. The channel supplies are split in two, since the channel supply for the buffer chain will have a large voltage drop when charging the gate capacitance of
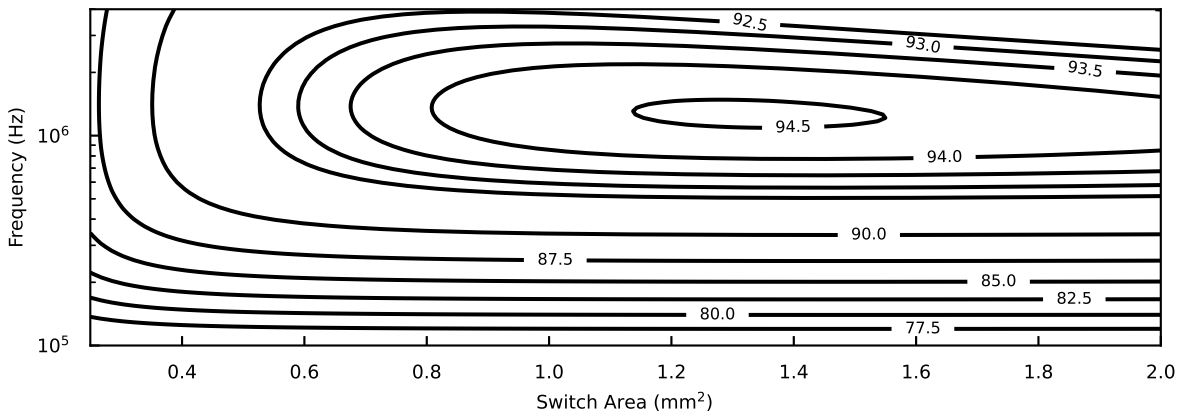
Fig. 6. Efficiency of $48\,\text{V-}12\,\text{V}$ switched-capacitor power for different switching frequencies ($f_{sw}$) and total for power switch area ($A_{sw}$) using the proposed model. Calculated for $2\,\text{A}$ load current.
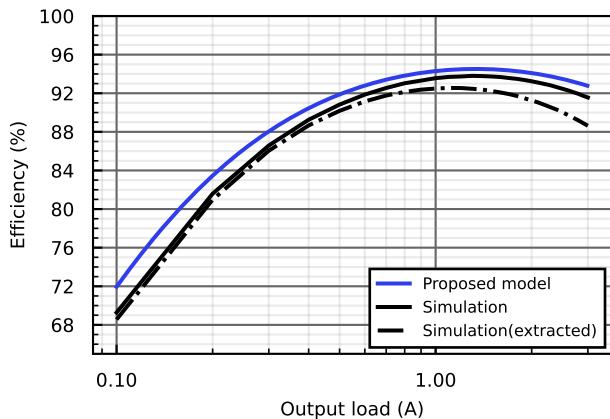


Fig. 7. Efficiency curve for output load current of $100\,\text{mA}$ to $3\,\text{A}$ with a $f_{sw} = 1\,\text{MHz}$ for the proposed model and for the simulated results.
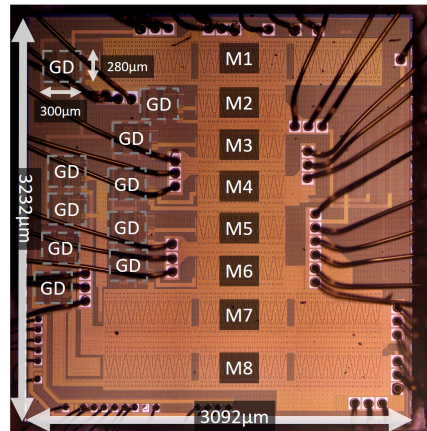


Fig. 8. Microscope photo of the $48\,\text{V-}12\,\text{V}$ switched-capacitor power converter IC with an integrated power stage ($M_1 - M_8$) and gate-drivers (GD).

the power switch. Since the channel supply for the buffer chain is noisy, a level shifter is used to interface between the two channel supplies, $\text{vddhi}_{\text{ls}}$ and $\text{vddhi}_{\text{bc}}$. In this work, we have decided to supply the channel-supplies from the power converter input instead of across the external capacitors as seen in [9]. This enables for a faster and more robust start-up at the cost of a higher power consumption.

In Fig. 1 it can be seen that the gate-driver supply voltages are dependent on which power switch they are driving. For the top gate-driver, driving $M_1$, the supply voltage is only $\frac{1}{4}V_{in}$, whereas for the bottom gate-driver, driving $M_8$, the supply voltage is the full input voltage of $V_{in}$. The gate-driver supply voltages can be described as:

$$\mathbf{V_{DD}} = V_{in} \cdot \left[\frac{1}{4}, \frac{1}{4}, \frac{2}{4}, \frac{2}{4}, \frac{3}{4}, \frac{3}{4}, 1, 1\right] \qquad (28)$$

Since the two bottom power switches are three times larger, than the rest, the driving capabilities of the gate-drivers driving these are increased to ensure equal rise-time for all power switches.

The large gate-drain capacitance of the power switches can lead to self turn-on, whenever the drain node is switched. This will lead to shoot-through current and is undesirable. The pull-down capabilities of the buffer chain is therefore designed to handle this inrush current from the gate-drain capacitor, ensuring that the voltage seen on the gate-source voltage of the power switch, does not exceed the threshold voltage of the device. The simulated quiescent current of the implemented floating gate-driver is $52.34\,\mu\text{A}$ leading to a total quiescent current for all the gate-drivers of $523.4\,\mu\text{A}$.

### C. Clock Controller

The implementation of the clock controller can be seen in Fig. 4. The designed clock controller consists of an integrated $2\,\text{MHz}$ ring oscillator with a 3-bit frequency trimming bit $\text{freq}_{\text{ctrl}}$. For further debugging in the laboratory the option of having an external clock is also enabled by $\text{clk}_{\text{sel}}$. The clock controller also consists of a non-overlapping clock generator, that generates the two switching phases for the power stage. The non-overlapping clock generator has a 1-bit signal for
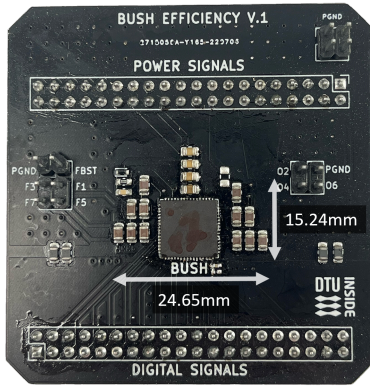
Fig. 9. Close-up of test PCB for experimental measurements.

choosing between two different dead-times. These dead-times are $20\,\mathrm{ns}$ and $35\,\mathrm{ns}$. The selection signal $\varphi_{\mathrm{sel}}$ selects either the internal phases generated by the non-overlapping clock generator or from an external signal generator.

In Fig. 5 the implemented $2\,\mathrm{MHz}$ current-starved ring oscillator can be seen. The most significant bit of the trimming signal, $\mathrm{freq}_{\mathrm{ctrl}}$ chooses either the $2\,\mathrm{MHz}$ clock signal from the ring oscillator or the clock divider output of $1\,\mathrm{MHz}$. The two other bits of $\mathrm{freq}_{\mathrm{ctrl}}$ trims the bias current for the PMOS cascodes responsible for the current-starving of the ring oscillator. The clock controller is supplied by an external $5\,\mathrm{V}$ supply.

### D. Power Losses

The total power loss from the switched-capacitor power converter can be described as:

$$P_{loss} = P_{rout} + P_{sw} + P_{gd} \qquad (29)$$

With the chosen external capacitors, power switch scaling and extracted parasitic switch capacitances the power loss becomes a function of the total switch area, frequency and load current. In this work the power converter is designed for a maximum of $2\,\mathrm{A}$ output current. In Fig. 6 a contour plot of the calculated power converter efficiency for a $48\,\mathrm{V}\text{-}12\,\mathrm{V}$ ladder converter

### TABLE I
COMPONENT LISTING OF IMPLEMENTED CONVERTER.

| Component | Part Number | Parameters |
|---|---|---|
| IC | | ASIC, QFN package, 64pins |
| $C_{bst}$ | GCJ188R71E473KA01D | $25\,\mathrm{V}$, $47\,\mathrm{nF}$ |
| $C_1$-$C_5$ | GRM21BC71E106KE11K | $25\,\mathrm{V}$, $10\,\mu\mathrm{F}$ |
| $D_{bst}$ | 1SS400-G | $90\,\mathrm{V}$, $100\,\mathrm{mA}$ |
| Microcontroller | Raspberry Pi 3 | |

using the proposed model based on power loss expressions in (7), (11) and (15) and the optimum external capacitor scaling based on (23) can be seen as a function of both total switch area ($A_{sw}$) and switching frequency ($f_{sw}$). From Fig. 6 it can be seen that a maximum exists at around $A_{sw} = 1.3\,\mathrm{mm}^2$ and for a switching frequency of around $1.1\,\mathrm{MHz}$. Note that this is not taking into account the added resistance and inductance of the bonding wires for the interface with the QFN package used. These bonding wires lower the peak efficiency and have an impact on the effective output resistance of the power converter. Furthermore, due to the inductance of the bonding wires together with any PCB trace inductance and series inductance in the external capacitors the power loss dependency on the switching frequency is also expected to be higher than what is modelled here. This is not an issue, since the final switching frequency can be adjusted using the trimming bits of the ring oscillator. In Fig. 7 the calculated efficiency for an output load current from $0.1\,\mathrm{A}$ to $3\,\mathrm{A}$ can be seen. The calculations are based on the proposed model with the power losses described in section II. The calculations are based on a total switch area of $1.365\,\mathrm{mm}^2$ and a switching frequency of $1\,\mathrm{MHz}$. In Fig. 7 the simulated efficiency with and without modelling the bonding wire parasitic resistance and the post-layout extracted view of the integrated power stage can also be seen.

It can be seen from Fig. 7 that the slopes of the efficiency curves for higher output currents is similar for the proposed model and the simulation results indicating that the output resistances are similar. The offset between the proposed model
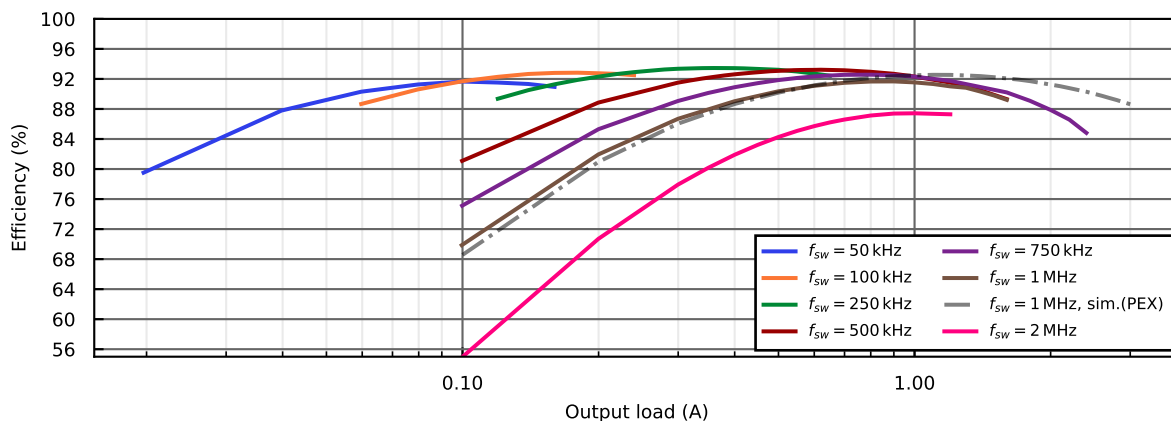


Fig. 10. Measured efficiency of $48\,\mathrm{V}\text{-}12\,\mathrm{V}$ switched-capacitor power for different load currents and switching frequencies.
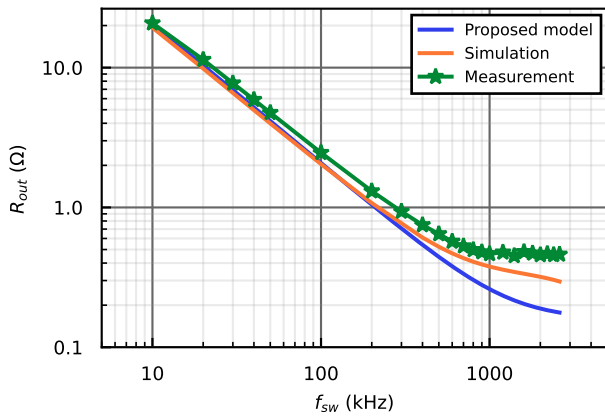
Fig. 11. Comparison of output resistance for the proposed model, simulation and measurement results. With $100\,\mathrm{mA}$ output load current.
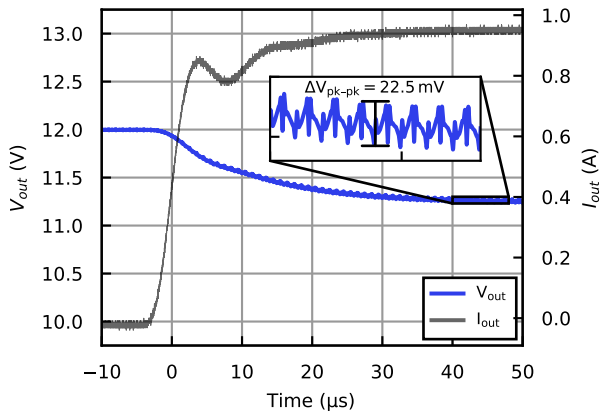


Fig. 13. Measurement of the $f_1$ switching node and the output voltage at maximum load conditions with $f_{sw} = 750\,\mathrm{kHz}$. Measurements are $20\,\mathrm{MHz}$ bandwidth limited.



Fig. 12. Measurement of the output voltage when an output load step of $1\,\mathrm{A}$ is applied. $V_{out}$ is $20\,\mathrm{MHz}$ bandwidth limited.
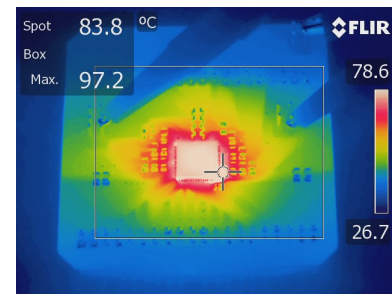


Fig. 14. Thermal measurement of the highly-integrated switched-capacitor power converter with an output load current of (a) $1.6\,\mathrm{A}$ and (b) $2.2\,\mathrm{A}$.

and the simulated efficiency is mainly due to the quiescent current of the gate-drivers and other circuitry, which is not taken into account for the power loss calculation. Furthermore, it can be seen that when modelling the bonding wire series resistance and simulating with post-layout extracted parasitics the output resistance is increased, which changes the overall efficiency and the drop-off slope of the efficiency curve for higher output currents, where the power loss due to the effective output resistance becomes dominant.

The $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor power converter was designed and fabricated in a $180\,\mathrm{nm}$ SOI BCD process. A microscope photo of the IC can be seen in Fig. 8 with annotations for the power switches and the gate-drivers.

## IV. EXPERIMENTAL RESULTS

To verify the implemented switched-capacitor power converter a PCB for testing the efficiency for different output loads and switching frequencies has been designed. The test PCB consists of the designed chip and external capacitors. Thermal vias under and around the IC package have been added to help mitigate thermal heating during high output load currents. The
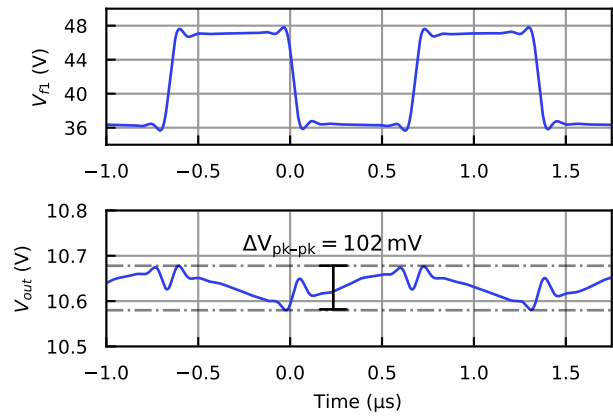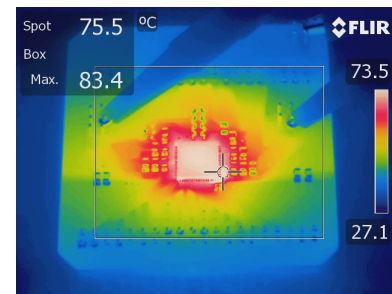
focus of the prototype is to verify the maximum efficiency and maximum output power capabilities of the highly-integrated switched-capacitor converter. The test setup consists of a $5\,\mathrm{V}$ power supply for the digital domain and IOs, a $48\,\mathrm{V}$, $100\,\mathrm{W}$ power supply for supplying the input voltage, a function generator for testing different switching frequencies and a digital current load. The digital control of the chip is controlled from a Python script through a Raspberry Pi. A close view of the PCB of the full power converter can be seen in Fig. 9. Here the QFN64 package containing the chip and the external flying capacitors can be seen. The total volume of the power converter is $1.07\,\mathrm{cm}^3$ including the PCB thickness. In Table I a summary of the used components for the proposed power converter can be seen. The measured efficiency for different

This article has been accepted for publication in IEEE Transactions on Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2023.3288592

TRANSACTION ON POWER ELECTRONICS, REGULAR PAPER SPECIAL SECTION ON SWITCHED CAPACITOR CONVERTERS SCCS 9

TABLE II
PERFORMANCE COMPARISON.

| Design | [19] | [31] | [6] | [18] | [1] | **This work** |
|---|---|---|---|---|---|---|
| **Topology** | Series-Capacitor Buck | QSD | 4:1 Hybrid Dickson | 12-level Series-Capacitor Buck | LLC DCX | **4:1 Ladder SCC** |
| **Process** | N/R | 180 nm BCD | 130 nm SOI-BCD | 180 nm BCD + discrete GaN | Discrete | **180 nm SOI-BCD** |
| $V_{in}$ **(V)** | 12 | 48 | 20-60 | 36-60 | 48 | **48** |
| $V_{out}$ **(V)** | 1.2 | 1.2 | 3-3.6 | 0.5-1 | 12 | **12** |
| $f_{sw,eff}$ **(MHz)** | 2 | 0.5 | 0.32 | 2.5 | 1.6 | **0.25** |
| **Max. Eff. (%)** | 87.7@4.8 W | 88.5@4.2 W | 91.4@4.62 W | 90.2@1.5 W | 97.3@160 W | **93.5@4.18 W** |
| **Dimension W × L × H (mm)** | 13.1 × 10 × 2.8* | N/R | N/R | 17 × 15 × 2.5 | 30 × 20 × 7.84 | **15.24 × 24.65 × 2.85** |
| **Max. $P_{out}$ (W)** | 12 | 12 | 9.9 | 8 | 250 | **24.6** |
| **Power density (W/cm³)** | 32.71* | N/R | N/R | 12.07 | 53.09 | **23.0** |
| **Regulated/Isolated** | Yes/No | Yes/No | Yes/No | Yes/No | No/Yes | **No/No** |

*Estimated from paper, N/R = Not reported.

output load currents and for different switching frequencies can be seen in Fig. 10. Simulation results for a switching frequency of 1 MHz with extracted parasitics can also be seen for comparison. The figure shows a peak efficiency of 93.5 % at a load current of 360 mA and a switching frequency of 250 kHz. From Fig. 10 it can also be seen, that if a simple frequency control scheme is implemented there is potential for above 90 % efficiency from a wide current range of 80 mA to 1.4 A. Comparing the 1 MHz measurement results to the simulation results, it can be seen that for low loads there is a very good correspondence. While for higher loads, the slope of the measurements curve is steeper indicating a higher output resistance. To investigate this difference the output resistance was measured and compared to both the proposed model results and the simulated output resistance. This comparison can be seen in Fig. 11. Here it is clear, that the $R_{SSL}$ matches well for the proposed model, simulation and measurement results. The $R_{FSL}$ is about 150 mΩ higher than expected from simulation. This increase is most likely due to the additional PCB trace inductance and resistance that has not been modelled properly in simulation. In Fig. 10 it can also be seen that there seems to be increased losses when going to switching frequencies around 1 MHz and above. This can be seen since the measurement results for 750 kHz outperforms the 1 MHz results, even for higher load currents. This could be because of the frequency limit of the external capacitors used, which start becoming inductive and have increased ESR from around 2 MHz [30].

To investigate the transient load performance, the output voltage $V_{out}$ with a load step of 1 A and a switching frequency of 1 MHz can be seen in Fig. 12. This load condition is around the maximum efficiency of the power converter for the 1 MHz switching frequency. The output voltage is measured with a bandwidth limit of 20 MHz. The output current waveform is captured using a Hioki 3273-50, dc-50 MHz bandwidth current probe. From Fig. 12 it can seen that the output voltage ripple is 22.5 mV for a 1 A load. Additionally a measurement of one of the switching nodes, $f_1$ and the output voltage at maximum load condition of 2.2 A can be seen in Fig. 13. Here it can be seen that the output voltage drops to an average of around 10.65 V and the output voltage ripple is increased to 102 mV.

In Fig. 14 thermal measurements for a load current of 1.6 A and 2.2 A respectively, can be seen. These measurements are performed with a switching frequency of 750 kHz and no external cooling. The measurement at 1.6 A is made as this is where the conduction losses start being dominant, and therefore the main heat dissipation will shift from the external capacitors to inside of the IC as can be seen from Fig. 10. The 2.2 A measurement is close to the maximum load current of 2.4 A and therefore Fig. 14b gives better insight into the maximum thermal capabilities. Both thermal measurements are made after applying the load and waiting for 1 minute to reach thermal steady-state. It can be seen from Fig. 14 that the maximum temperature of 97.2 °C is close to the output voltage node of the IC, which is expected since the highest current is drawn from this node based on the switch charge multiplier vector of the ladder topology.

The maximum output power is 24.6 W leading to a power density of 23 W/cm³ including the PCB thickness.

## V. DISCUSSION

The proposed general design methodology and considerations presented in this work enables the design of more efficient highly-integrated switched-capacitor power converters under load current and constraints of both the integrated die area and the flying capacitor PCB area. The integrated power switch design optimization presented can also be used for hybrid switched-capacitor converters to achieve optimal design of the integrated power stage. The methodology differs from other previously presented methodologies since it focuses on highly-integrated switched-capacitor converters. This difference includes the losses that scales with the converter input voltage, such as gate-driver losses and switching losses. In traditional sizing methodologies such as in [28] floating gate-drivers and their increased losses due to their voltage supply is not taken into account, since it focuses on fully integrated, low voltage applications. The use of external discrete flying capacitors also means, that the traditional capacitor sizing methodology is not useful since the optimal scaling needs to take the discretized capacitor sizes into account. On the other hand, bottom-plate capacitor charge/discharge losses are not taken into account in this work, since the ratio between

the discrete flying capacitor sizes compared to the parasitic capacitances at the flying nodes is usually so small, that it can be neglected.

The performance of the proposed power converter can be seen in Tab. II together with other selected designs for a performance comparison on peak efficiency, maximum output power and power density. The regulation and isolation capabilities of the power converters are included in Tab. II since these features can effect the peak efficiency, maximum output power and power density, which we want to compare. The designs were selected based on similar application, input voltage range and power levels as is recommended by [32] when doing metrics comparison for power converters. The designs from [6], [19], [31] are all highly-integrated power converters where the power stage is integrated but the passive components are external, as in the proposed power converter in this design. They all utilize one or more inductors. In [19] The input voltage is $12\,\mathrm{V}$ to a point-of-load voltage of $1\,\mathrm{V}$. It is included since it is a highly-integrated solution, that is in a similar output power level as the proposed converter. The work in [31] is a quadruple step-down converter utilizing a 4-phase switching scheme to achieve series capacitor charge-balancing. The topology in [31] is an extension on the double step-down converter (DSD) and achieves great performance since it can utilize higher conductive switches, since the maximum $V_{ds}$ is only $12\,\mathrm{V}$, where LDMOS transistor have a better $P_{fom}(\mathrm{m\Omega \cdot nC})$ compared to GaN technologies [18]. The work in [6] is a 4:1 hybrid Dickson switched-capacitor converter using a single series-inductor at the output. This way the power converter utilizes the good step-down capabilities of switched-capacitor converters [17], while utilizing the inductor to achieve high efficiency outside of the ideal voltage conversion rate of the 4:1 Dickson topology. The design in [6] does not report a power density for the full design. The design in [18] aims to use a high step-down Dickson 12:1 converter with a 2 phase series-buck converter to lower the maximum $V_{ds}$ of the power switches to $5\,\mathrm{V}$, which means that it can use high-conductive $5\,\mathrm{V}$ devices. It uses a discrete GaN device for the top switch, to ensure safe start-up and tolerate the full input voltage. While the design is very compact and highly-integrated it suffers from a high conduction loss due to the large amount of switches, which limits the maximum power. The design in [1] is not monolithic. It is included since it is targeting the same application and shows how by careful optimization of the passive components, in this case a planar matrix transformer in a LLC converter, it can achieve high power density and peak efficiency. The design in [1] uses GaN devices for the power switches. The work does achieve the highest efficiency and maximum power.

The proposed design achieves the highest peak efficiency and maximum power of the highly-integrated designs. The power density in [19] is higher showing the benefits of careful selection of used passive components and PCB layout. The design in [19] also utilizes flip-chip packaging for the IC making the footprint even smaller. The QFN64 package used in this work is $9\,\mathrm{mm} \times 9\,\mathrm{mm}$, which is about 8 times larger than the designed IC leading to wasted PCB footprint area. Utilizing flip-chip packaging together with an interposer

technology would further increase both thermal performance and volume increasing the power density for highly-integrated power converters [33]. It is important to note that the designs in [6], [18], [31] are point-of-load converters and that for the proposed design and the design in [1] there needs to be cascade converter to reach the desired point-of-load voltage. This will further decrease both the total efficiency and power density. The proposed design in this work and its design considerations could be incorporated in designs similar to [6], [18], [31] to further increase both maximum power and power density.

## VI. CONCLUSION

In this study the design methodology for designing high-voltage, highly-integrated switched-capacitor power converters is presented and demonstrated with an implemented $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor power converter with an integrated power stage, floating gate-drivers and clock controller in a $180\,\mathrm{nm}$ SOI process. This work presents an extended insight in the main power losses to consider in high-voltage applications, taking into account the trade-offs between lower conduction losses, but larger switching and gate-driver losses when the total integrated switch area is increased. The $48\,\mathrm{V}$-$12\,\mathrm{V}$ ladder topology switched-capacitor power converter has been implemented using the proposed design methodology to size the integrated power stage and external capacitors. The implemented gate-drivers and clock controller has also been shown and discussed. The performance of the highly-integrated switched-capacitor power converter has been verified with experimental results. The designed power converter achieves a peak efficiency of $93.5\,\%$ at $4.18\,\mathrm{W}$ and a maximum output power of $24.6\,\mathrm{W}$ leading to a power density of $23\,\mathrm{W/cm^3}$. Finally a discussion of the proposed power converter is presented, comparing the proposed power converter to recently published works in the same application, input voltage range and power level. Here the proposed design showed similar performance to highly-integrated inductor based topologies, while being apple to handle a larger maximum output power. To the best of the authors' knowledge, the proposed converter using a fully integrated power stage and gate-drivers and hard-charging of the capacitors is the only published power converter to achieve competitive efficiency, maximum output power and power density with an $48\,\mathrm{V}$ input voltage. This performance can help advancements in both traditional and hybrid switched-capacitor power converters.

## REFERENCES

[1] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48-V Voltage Regulator Module with PCB Winding Matrix Transformer for Future Data Centers," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9302–9310, 2017.

[2] L. Yu, S. Xu, L. Li, Y. Wu, C. Yang, L. Shi, and W. Sun, "Modeling and Control of Quasi-Parallel Sigma DC-DC Converter for Single-Stage 48-V Voltage Regulator," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7333–7345, 2022.

[3] J. Hu, S. Member, B. Wen, R. Burgos, R. Fernandez, and A. Mclean, "Design of a Flying-Capacitor-Based Voltage Divider LLC Resonant Converter for USB-C PD Charger in Aircraft Applications," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1–17, 2023.

[4] C. Rindfleisch and B. Wicht, "A 110/230 V AC and 15-400 V DC 0.3 W Power-Supply IC With Integrated Active Zero-Crossing Buffer," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3816–3824, 2022.

[5] C. Rindfleisch, J. Otten, and B. Wicht, "A Highly-Integrated 20-300V 0.5W Active-Clamp Flyback DCDC Converter with 76.7% Peak Efficiency," in *Proceedings of the Custom Integrated Circuits Conference*, vol. 2022-April. IEEE, 2022, pp. 2022–2023.

[6] M. Ashourloo, V. R. Namburi, G. V. Pique, J. Pigott, H. J. Bergveld, A. E. Sherif, and O. Trescases, "An Automotive-Grade Monolithic Masterless Fault-Tolerant Hybrid Dickson DC-DC Converter for 48-V Multi-Phase Applications," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3608–3618, 2021.

[7] C. Chen, J. Liu, and H. Lee, "A 2.5-5MHz 87% Peak Efficiency 48V-to-1V Integrated Hybrid DC-DC Converter Adopting Ladder SC Network with Capacitor-Assisted Dual-Inductor Filtering," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 2022-February. IEEE, 2022, pp. 234–236.

[8] P. Assem, W. C. Liu, Y. Lei, P. K. Hanumolu, and R. C. Pilawa-Podgurski, "Hybrid Dickson Switched-Capacitor Converter with Wide Conversion Ratio in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 9, pp. 2513–2528, 2020.

[9] C. Le, D. L. Gerber, M. Kline, S. R. Sanders, and P. R. Kinget, "Reconfigurable hybrid-switched-capacitor-resonant LED driver for multiple mains voltages," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 1871–1883, 2018.

[10] A. Barner, J. Wittmann, T. Rosahl, and B. Wicht, "A 10 MHz, 48-to-5V synchronous converter with dead time enabled 125 ps resolution zero-voltage switching," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2016-May, no. Ccm. IEEE, 2016, pp. 106–110.

[11] K. Wei, Y. Ramadass, and D. B. Ma, "A Direct 12V/24V-to-1V 3W 91.2and In-Situ Precharge Rate Regulation," in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*. San Francisco, CA, USA: IEEE, 2020, pp. 2019–2021.

[12] G. Villar-Piqué, H. J. Bergveld, and E. Alarcón, "Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4156–4167, 2013.

[13] C. Wang, Y. Lu, N. Sun, and R. P. Martins, "A 3-Phase Resonant Switched-Capacitor Converter for Data Center 48-V Rack Power Distribution," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2714–2724, 2021.

[14] Y. Wang, J. Zhang, Y. Guan, and D. Xu, "Analysis and Design of a Two-Phase Series Capacitor Dual-Path Hybrid DC-DC Converter," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9492–9502, 2022.

[15] M. M. Henriksen, D. O. Larsen, and P. L. Muntal, "Analysis and Design of Start-up Circuits for a 48V-12V Switched-Capacitor Converter in a 180 nm SOI Process," in *2021 IEEE Nordic Circuits and Systems Conference, NORCAS 2021 - Proceedings*, 2021, pp. 3–9.

[16] V. W. Ng, M. D. Seeman, and S. R. Sanders, "Minimum PCB footprint point-of-load DC-DC converter realized with Switched-Capacitor architecture," in *2009 IEEE Energy Conversion Congress and Exposition, ECCE 2009*. IEEE, 2009, pp. 1575–1581.

[17] M. D. Seeman, V. W. Ng, H. P. Le, M. John, E. Alon, and S. R. Sanders, "A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies," *2010 IEEE 12th Workshop on Control and Modeling for Power Electronics, COMPEL 2010*, pp. 1–7, 2010.

[18] H. Cao, X. Yang, C. Xue, L. He, Z. Tan, M. Zhao, Y. Ding, W. Li, and W. Qu, "A 12-Level Series-Capacitor 48-1V DC-DC Converter with On-Chip Switch and GaN Hybrid Power Conversion," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3628–3638, 2021.

[19] P. S. Shenoy, O. Lazaro, R. Ramani, M. Amaro, W. Wiktor, J. Khayat, and B. Lynch, "A 5 MHz, 12 V, 10 A, monolithically integrated two-phase series capacitor buck converter," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2016-May, pp. 66–72, 2016.

[20] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, 2015.

[21] Y. Lei, W. C. Liu, and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate and Design Hybrid Switched-Capacitor and Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2227–2240, 2018.

[22] W. C. Liu, Z. Ye, and R. C. Pilawa-Podgurski, "A 97A/in3 Current Density 48-to-4 v Two-Stage Resonant Switched-Capacitor Converter for Data Center Applications," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2020-March, pp. 468–474, 2020.

[23] Z. Ye, Y. Lei, and R. C. Pilawa-Podgurski, "The Cascaded Resonant Converter: A Hybrid Switched-Capacitor Topology with High Power Density and Efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946–4958, 2020.

[24] N. M. Ellis, R. A. Abramson, R. Mahony, and R. C. Pilawa-Podgurski, "The Symmetric Dual Inductor Hybrid (SDIH) Converter for Direct 48V-to-PoL Conversion," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1–13, 2023.

[25] C. Hardy and H. P. Le, "11.5 A 21W 94.8Single-Inductor Multi-Stage Hybrid DC-DC Converter," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 2023-February, pp. 190–192, 2023.

[26] G. Cai, Y. Lu, and R. P. Martins, "11.9 A Compact 12V-to-1V 91.8Efficiency Hybrid Resonant Switched-Capacitor Parallel Inductor (ReSC-PL) Buck Converter," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 2023-February, pp. 198–200, 2023.

[27] W. L. Zeng, G. Cai, C. F. Lee, C. S. Lam, Y. Lu, S. W. Sin, and R. P. Martins, "11.10 A 12V-lnput 1V-1.8V-Output 93.7Quad-Path Hybrid DC-DC Converter," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 2023-February, pp. 200–202, 2023.

[28] J. De Vos, D. Flandre, and D. Bol, "A sizing methodology for on-chip switched-capacitor DC/DC converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 5, pp. 1597–1606, 2014.

[29] M. D. Seeman, S. R. Sanders, and C. Hall, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[30] Murata, "GRM21BC71E106KE11 Datasheet," pp. 1–4, 2022. [Online]. Available: https://www.murata.com/en-global/api/pdfdownloadapi?cate=luCeramicCapacitorsSMD&partno=GRM21BC71E106KE11%23

[31] H. Han, M. W. Ko, J. H. Cho, G. G. Kang, S. T. Koh, H. H. Bae, and H. S. Kim, "A Monolithic 48V-to-1V 10A Quadruple Step-Down DC-DC Converter with Hysteretic Copied On-Time 4-Phase Control and 2× Slew Rate All-Hysteretic Mode," *Digest of Technical Papers - Symposium on VLSI Technology*, vol. 2022-June, pp. 182–183, 2022.

[32] H. Tarzamni, H. S. Gohari, M. Sabahi, and J. Kyyra, "Non-Isolated High Step-Up DC-DC Converters: Comparative Review and Metrics Applicability," *IEEE Transactions on Power Electronics*, 2023.

[33] Y. A. Nour, H. L. Thanh, A. M. Ammar, D. Ø. Larsen, and P. L. Muntal, "Patent: Power converter assembly," p. 20, 2021. [Online]. Available: https://patents.google.com/patent/WO2021234158A1/