

# Highly--Integrated Switched--Capacitor DC--DC Converters

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*Publication date:*
2023

*Document Version*
Publisher's PDF, also known as Version of record

**Highly-Integrated Switched-Capacitor DC-DC Converters**

Ph.D. Thesis
August, 2023

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Published by: DTU, Department of Electrical and Photonics Engineering, Richard Petersens Plads, Building 325, 2nd floor, 2800 Kgs. Lyngby Denmark
https://electro.dtu.dk/
Comments: This thesis is submitted in partial fulfillment of the requirements for obtaining the Ph.D. in Electrical Engineering at the Technical University of Denmark.

## Abstract

The increasing demand for power converters with high energy efficiency and power density has sparked interest in highly-integrated switched-capacitor converters to replace traditional inductor-based switch-mode power supplies. The switched-capacitor converter leverages the benefits of capacitors offering increased energy density compared to inductors and superior power switch utilization to that of inductor-based switch-mode power supplies. By integrating power switches, gate-drivers, and digital control circuits, and utilizing high energy density MLC capacitors, larger output power can be achieved while maintaining a high power density through monolithic integration.

This research focuses on fixed-ratio DC-DC converters, particularly in the context of a DC bus for 48 V-12 V, common in various applications. The developed design methodology optimizes power switch sizing considering intrinsic and parasitic capacitance losses. Additionally, the optimization of external flying capacitors is presented.

Experimental results of a fabricated IC implementing a 4:1 Ladder topology with integrated switches, gate-drivers and digital clock control demonstrate the effectiveness of the design methodology. The measured peak efficiency for the 48 V-12 V highly-integrated switched-capacitor converter is 93.5 %, achieving a maximum output power of 24.6 W, leading to a maximum power density of 23 $\mathrm{W/cm^3}$.

Addressing startup challenges, three proposed solutions, consisting of a passive startup strategy, a switch-conductance control strategy, and an active pre-charge circuit strategy, have been simulated and the active pre-charge circuit has been validated experimentally, with the active pre-charge circuit ensuring that the peak inrush current of the 48 V-12 V highly-integrated switched-capacitor converter is only 534 mA.

Furthermore, this research explores hybrid switched-capacitor converters, eliminating charge redistribution losses of the flying capacitors to enhance energy efficiency and power density. A visual multi-step approach and an equivalent output resistance analysis for non-idealities have been developed to examine the soft-charging capabilities of hybrid switched-capacitor converters.

In conclusion, this study demonstrates the potential of highly-integrated switched-capacitor converters to meet the increasing demands of high energy efficiency and power density in consumer electronics, offering promising solutions for future power conversion technologies.

## Resumé

Den stigende efterspørgsel efter strømforsyninger med høj energieffektivitet og effektdensitet har vakt interesse for højtintegrerede switched-kondensatorstrømforsyninger, der erstatter traditionelle spole-baserede switch-mode strømforsyninger. switched-kondensatorstrømforsyninger udnytter fordelene ved kondensatorer, der tilbyder øget energitæthed i forhold til spoler og overlegen udnyttelse af effekttransistorer i forhold til spolebaserede switch-mode strømforsyninger. Ved at integrere effekttransistorerne, gate-drivere og digitale kontrolkredsløb og udnytte højenergitætte MLC-kondensatorer kan der opnås større udgangseffekt, samtidig med at der opretholdes en høj effekttæthed gennem monolitisk integration.

Dette forskningsprojekt fokuserer på fast-ratio DC-DC strømforsyninger, især i sammenhængen af en DC-bus for 48 V-12 V, almindelig i forskellige applikationer. Den udviklede designmetode optimerer effekttransistorerne under hensyntagen til intrinsiske og parasitiske kondensator energitab. Derudover præsenteres optimeringen af eksterne flyvekondensatorer.

Eksperimentelle resultater af et produceret integreret kredsløb, der implementerer en 4:1 Ladder-topologi med integrerede effekttransistorer, gate-drivere og digitalt kontrolkredsløb, viser effektiviteten af designmetoden. Den målte maksimale energieffektivitet for den 48 V-12 V højtintegrerede skifte-kondensator-strømforsyning er 93.5 %, der opnår en maksimal udgangseffekt på 24.6 W, hvilket fører til en maksimal effekttæthed på $23\,\mathrm{W/cm^3}$.

Vedrørende opstartudfordringer er der foreslået tre strategier, bestående af en passiv opstartsstrategi, en transistor-ledningsevne kontrolstrategi og en aktiv foropladningskredsløbsstrategi, der er blevet simuleret, og det aktive foropladningskredsløb er blevet valideret eksperimentelt, hvilket sikrer, at maksimalstrømmen under opstarten af den 48 V-12 V højtintegrerede switched-kondensator-strømforsyning kun er 534 mA.

Desuden undersøger dette forskningsprojekt hybrid switched-kondensatorstrømforsyninger, der eliminerer ladningsomfordelings tab af flyvekondensatorer for at forbedre energieffektivitet og effekttæthed. Der er udviklet en visuel flertrins tilgang og en analyse af den ækvivalente udgangsmodstand for ikke-ideelle forhold til at undersøge de bløde opladningsevner af hybrid switched-kondensator-strømforsyninger.

Afslutningsvis demonstrerer dette forskningsstudie potentialet for højtintegrerede switched-kondensator-strømforsyninger til at imødekomme de stigende krav til høj energieffektivitet og effekttæthed inden for forbrugerelektronik og tilbyder lovende løsninger for fremtidige strømforsyningsteknologier.

## Acknowledgements

This Ph.D. thesis was prepared at the Department of Electrical and Photonics Engineering at the Technical University of Denmark in fulfillment of the requirements for acquiring a Doctor of Philosophy degree. The research was conducted between December 2019 and August 2023, including two 4-month project leaves during which the student was employed at Skycore Semiconductors. The Ph.D. project lasted a total of three years.

The last almost four years have been some of the most challenging and mind-changing journeys of my life. From dealing with isolation due to Covid-19 to pushing my own understanding of integrated circuit design and electrical engineering, this project has been a significant endeavor. It would not have been possible without the unlimited support I received both at work and in my personal life. I am grateful for those who believed in me, pushed me to excel, and kept me grounded whenever ambition threatened to challenge reality. I feel fortunate to be surrounded by so many wonderful and supportive people. Therefore, I would like to express my heartfelt thanks to some of those who made the last four years as a Ph.D. student truly special. A special thank you:

- to my supervisors Dennis Øland Larsen and Pere Llimós Muntal. The technical knowledge, personal support and encouragement that you have provided me throughout my M.Sc. and Ph.D. studies is far beyond what can be expected.
- to the rest of the team at Skycore Semiconductors, Thomas Souvignet and Guifré Vendrell Pausas. The technical knowledge and the fun I've had from working together with you has been amazing.
- to my main supervisor and group leader Michael A. E. Andersen, for standing in, when I needed it and for helping out with all practical matters and giving me the opportunity to pursue this Ph.D. project.
- to my former supervisor, Ivan H. H. Jørgensen, for introducing me to the world of analog integrated circuit design and sharing your technical knowledge throughout my M.Sc. studies. The occasional backhanded compliments (one of which has given a name to my IC: ”Bush”) never cease to astonish, impress and amuse. Thanks for believing in a lazy ”daller-røv.”.
- to my great colleagues at the Electronics Group (ELE) at DTU Electro both former and current. I've been a part of this group since 2017 in the forms of student, teaching assistant and finally Ph.D. student and colleague. Here I've formed great friendships and I've enjoyed all the technical discussions throughout the years. A special thank you to Allan Jørgensen for handling our servers and EDA tools, which is what enables all the research in analog integrated circuit design. To Maria del Carmen Sandoval for ensuring that our lab equipment is always running perfectly and for always being helpful in solving any practical matters related to the lab.
- to Professor Bernhard Wicht from the Mixed-Signal Schaltungen group at the Institute für Mikroelektronische Systeme (IMS), Leibniz Universität Hannover for welcoming me truly and fully into your amazing research group for my 2.5 months external research stay. Being surrounded by the very skilled and like-minded researchers at IMS truly increased my understanding of electrical circuits and integrated circuit design. A special thank you to my office mate at IMS, Jens Otten for all our technical (and non-technical) discussions and for introducing me to Vönertag.
- to all my friends from my time at DTU. So many good memories both in and out of

university. A special thank you to Peter Karstensen, Nick Thanthrige and Johnny Seehusen for the years of fun and friendship.

- to my childhood friend Frederik Steen Jensen for the 24 years of friendship and support. I'm grateful for all our memories throughout school, high-school and as adults.
- to my loving partner Ea Buchholtz (and Vilma), for the love and support throughout this Ph.D. project. You've kept me sane and made these last three years so very enjoyable.
- Finally, a very special thank you and my deepest gratitude to my loving family for believing in me and for your support.

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# 1 Introduction

## 1.1 Project motivation

In recent years, the rapid growth of electronic devices and the increasing demand for portable and energy efficient solutions have presented significant challenges in the field of power electronics. As electronic systems become more compact and power-hungry due to increase in performance and features, the need for highly energy efficient and space-saving power conversion technologies becomes paramount [1]–[7]. The power conversion is required to transform the produced electricity into a voltage range and form that our electronics can utilize. Power conversion happens multiple times from energy production to energy consumer, which leads to energy loss in the form of heat dissipation. An example illustration of the conversion steps required for some typical applications can be seen in Fig. 1.1.

From the electrical grid power conversion is handled by high energy efficient power converters, which transform the voltage from 230 V/110 V alternating-current (AC) to a rectified direct-current (DC) voltage.

The energy efficiency of the power converters is often the limiting factor in regards of electronics performance. The efficiency requirements for external power supplies below 250 W was recently updated in 2019 in the European Commision Regulation[1]. Figure 1.2

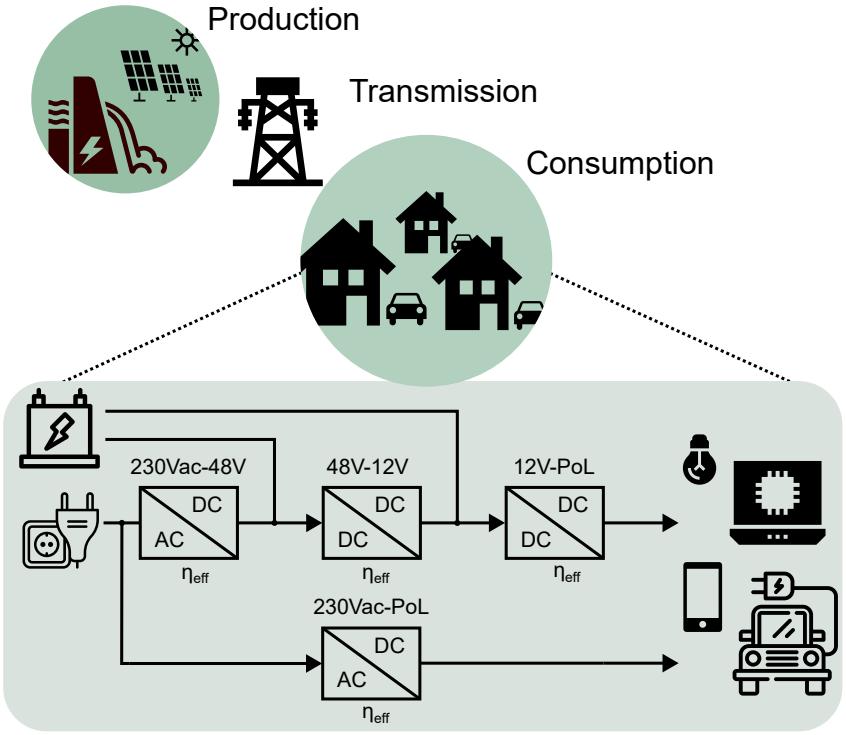



Figure 1.1: Illustration of the electricity path from energy production to consumption and an example of conversion steps from the electrical grid to various applications.

[1] COMMISSION REGULATION (EU) 2019/1782 of 1 October 2019 laying down ecodesign requirements for external power supplies pursuant to Directive 2009/125/EC of the European Parliament and of the Council

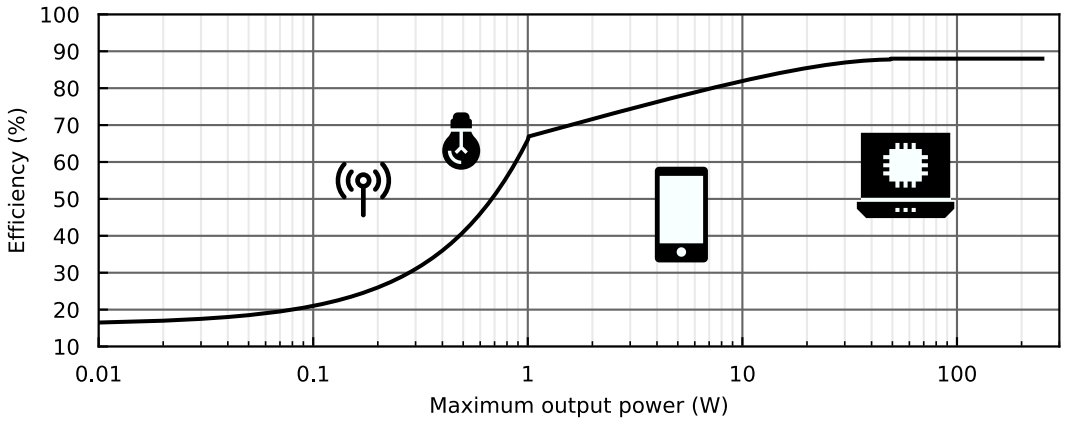



Figure 1.2: Required energy efficiency for external power supplies per EU Commission regulation from April 1st 2020 and some typical applications such as IoT, LED, smartphones and laptops for the different power levels.

shows the new required energy efficiency for external power supplies up to 250 W maximum output power. According to the commission report the EU regulation have an estimated potential to deliver annual final energy savings in excess of 260 TW h by 2030, which is equivalent to reducing greenhouse gas emissions by approximately 100 million tonnes. The EU regulation commission report shows the demand for the development and design of highly energy efficient power converters to ensure further technology advancements in computation and electrification.

To minimize conversion losses, power converter systems are moving towards fewer conversion steps [1]. Thereby, designing power converters that can interface directly with the electrical grid and the end energy consumer. Furthermore, the size of power converters become increasingly critical with emerging small wearable electronics. In this context, switched-capacitor converters have emerged as a promising alternative to traditional inductor-based power converters due to their reduction in physical size and ability to achieve high voltage conversion ratios while maintaining a high efficiency [4], [8], [9].

The aim of this Ph.D. project is to investigate the feasibility of highly-integrated switched-capacitor converters using monolithic integrated power switches, gate-drivers and digital control and external discrete passive components in applications ranging from 1 W-300 W and below 400 V input voltage. This includes the understanding of operation, modeling and design of highly-integrated switched-capacitor-based converters.

and repealing Commission Regulation (EC) [2019] OJ L272/95

## 1.2 Thesis objectives and scope

The main objective of this thesis is to investigate if power converters based on highly-integrated switched-capacitor techniques can outperform inductor-based power converters in terms of energy efficiency and power density. To investigate this, the following research questions were proposed:

- **Design and optimization:** How can highly-integrated switched-capacitor DC-DC converters be designed in regards of increasing energy efficiency for a physical size constraint?
- **Safe start-up:** Which challenges related to safe start-up of highly-integrated switched-capacitor converters are there and how can these challenges be solved?
- **Topology investigation:** Does converter topologies exist that are better suited for high-voltage and high-power switched-capacitor converters than those currently used including hybrid converters using a small inductor?

The research questions are investigated by a combination of theoretical and experimental work. The theoretical work includes analysis, modeling and simulation of switched-capacitor converters to minimize their operational and intrinsic power losses. The experimental work includes a prototype custom designed integrated circuit for implementing a 48 V-12 V highly-integrated switched-capacitor converter with a safe start-up circuit and measurements to prove the feasibility of using highly-integrated switched-capacitor converters in general consumer electronic applications.

### 1.2.1 Scope

The scope of the project are DC-DC power converters in the 1-300 W output power range and below 400 V input voltage utilizing external passive components and integrated gate-drivers, power switches and digital control. The main performance metrics of interest in this thesis are energy efficiency and power density. Voltage regulation is not considered in this research project.

### 1.2.2 Research contributions

The main research contributions (RC) from the Ph.D. project is listed below. The items list the overall contribution, while the nested items (RC 1.*) specify the sub-contributions in more detail.

**RC 1) Improvement in the design of highly-integrated switched-capacitor converters**

*RC 1.1)* An optimization methodology of integrated power stage based on reformulated switched-capacitor power losses minimizing power losses in the integrated power stage

*RC 1.2)* An optimization methodology of discrete flying capacitance sizing based on Lagrange multipliers minimizing the power losses in the passive components

*RC 1.3)* A highly-integrated switched-capacitor converter implementation at 48 V-12 V achieving 23 $\mathrm{W/cm^3}$ and a peak output efficiency of 93.5 %

**RC 2) Analysis and design of safe start-up operation for switched-capacitor converters**

*RC 2.1)* Investigation on main challenges regarding safe start-up of switched-capacitor converters.

*RC 2.2)* Presentation of three different strategies to handle the main challenges regarding safe start-up of switched-capacitor converters

*RC 2.3)* Implementation of an active pre-charge start-up circuit ensuring safe start-up for a 48 V-12 V switched-capacitor converter

**RC 3) Analysis and understanding of hybrid switched-capacitor converters**

*RC 3.1)* Determination of the slow-switching limit equivalent resistance of hybrid converters by calculation

*RC 3.2)* A visual multi-step inspection method for determining the soft-charging capabilities of switched-capacitor topologies, providing improved understanding of the trade-offs for different topologies in regards to hybrid converters

*RC 3.3)* Analysis of the effects of capacitor scaling mismatch variation on soft-charging capabilities of hybrid converters

## 1.3 Thesis outline

In Fig. 1.3, an overview of the thesis outline, along with the related publications in the appendices, is presented. Here, the three main research questions are also annotated. This thesis combines the work from the listed publications with additional content. To help guide the reader, the chapter sections, which mostly summarize the related publications, have been annotated in Fig. 1.3. Some sections present additional content beyond what has been described in the publications, and some sections are entirely new additional content that has not been published. The chapters are structured as follows:

Chapter 2 provides a short overview of inductive and capacitive approaches to DC-DC power converters, highlighting some of the advantages of switched-capacitor converters. It also includes a comparison of capacitance density for external MLC capacitors and monolithic integrated capacitor options. Additionally, an extensive state-of-the-art survey is presented, comparing discrete, highly-integrated, and fully-integrated power converters across various applications ranging from 1 mW to 1 kW, with a maximum input voltage of 400 V. The goal of this survey is to provide insights into the best implementations for various applications and requirements.

Chapter 3 covers the fundamental analysis of the operation and modeling of highly-integrated switched-capacitor converters. It describes the main power losses of highly-integrated switched-capacitor converters and their dependencies.

Chapter 4 introduces a design and optimization methodology for highly-integrated switched-capacitor converters. It includes a presentation of different gate-driver strategies and a comparison of these. Moreover, a Lagrange Multiplier optimization of the external flying-capacitors used for highly-integrated switched-capacitor converters is presented, along with two design examples. An optimization of the sizing of the integrated switches used for the highly-integrated switched-capacitor converters is then discussed, based on a reformulation of the power losses described in chapter 3. This reformulation of the power losses allows for designing the optimal sizes of the integrated switches and for choosing the optimal switching frequency of the power converter. An example of the optimization of the integrated switches is also provided. Finally, a 48 V-12 V highly-integrated switched-capacitor converter using a 4:1 Ladder topology is presented, where the main design considerations of the integrated circuits are shown, and experimental verification of a prototype power converter using the designed and fabricated IC is performed.

Chapter 5 addresses the challenges of ensuring safe start-up for switched-capacitor converters. This includes a description of the origin of these challenges and a presentation of

three different possible strategies to mitigate the improper flying capacitor voltages during the input voltage ramp-up and the large peak inrush currents as the power converter is enabled. An experimental verification of a fully-integrated active pre-charge start-up circuit is performed, and the relevant waveforms and measurements are presented and discussed.

Chapter 6 covers the operation and analysis of hybrid switched-capacitor converters. This includes a method of determining the slow-switching limit resistance of hybrid converters and a visual multi-step approach to determine the soft-charging capabilities of a hybrid converter topology. Additionally, some of the non-ideality challenges of achieving soft-charging in hybrid converters are discussed, including a stochastic analysis of the impact of capacitor mismatch variation on the soft-charging of a hybrid converter and some challenges when the constant current source is implemented using an inductor.

Chapter 7 concludes the findings of this Ph.D. project and provides suggestions for future research possibilities related to this work.

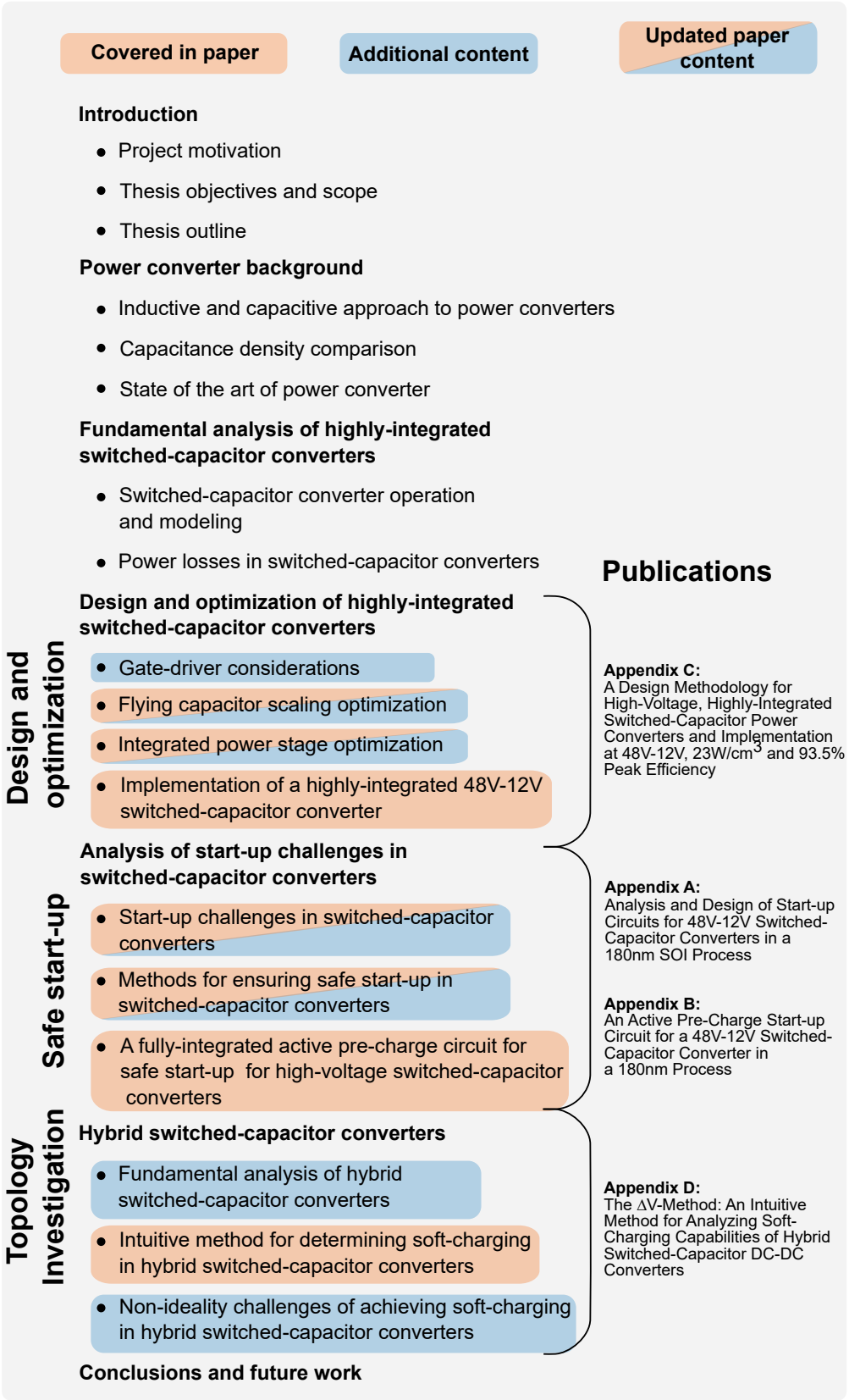



Figure 1.3: Thesis outline for the Ph.D. dissertation and how to relates to research questions and publications.

# 2 Power converter background

In this chapter, an overview of the current DC-DC power converters is given. A comparison of capacitance density for both integrated and discrete capacitors is shown, which motivates the decision for highly-integrated switched-capacitor converters. A state of the art survey for various state of the art power converter implementations is presented to demonstrate the trends in power converters for different power levels, input voltages, and power densities.

## 2.1 Inductive and capacitive approach to power converters

Many electronic applications such as laptop chargers, USB-C, data center and electrical vehicles demand power conversion solutions that can efficiently handle medium power levels while maintaining high energy efficiency and compact form factors. Traditional inductor-based converters have served well in many applications, but they often struggle to meet the stringent requirements of modern electronic systems in terms of size, weight, efficiency, and cost-effectiveness [10], [11]. This is especially due to the inductive elements, which ensure high efficiency and voltage regulation. Ongoing research is being carried into integrating these inductors into the printed circuit board (PCB) of the power converter, reducing the height [12]–[15]. The PCB integration of the inductive elements does however increase design complexity, power losses and production costs.

A benefit of inductor-based power converters is the galvanic isolation from using a magnetic transformer as a part of the energy conversion. While capacitive galvanic isolation can be achieved [16], [17] it comes at a cost of much lower efficiency compared to magnetic galvanic isolation. This makes inductor-based power converters preferable in applications, where isolation is required.

As high-voltage Complementary Metal Oxide Semiconductor (CMOS) processes have advanced, the possibility of designing integrated circuits (ICs) that can directly handle the voltage levels of the electrical grid has emerged. This advancement could reduce the

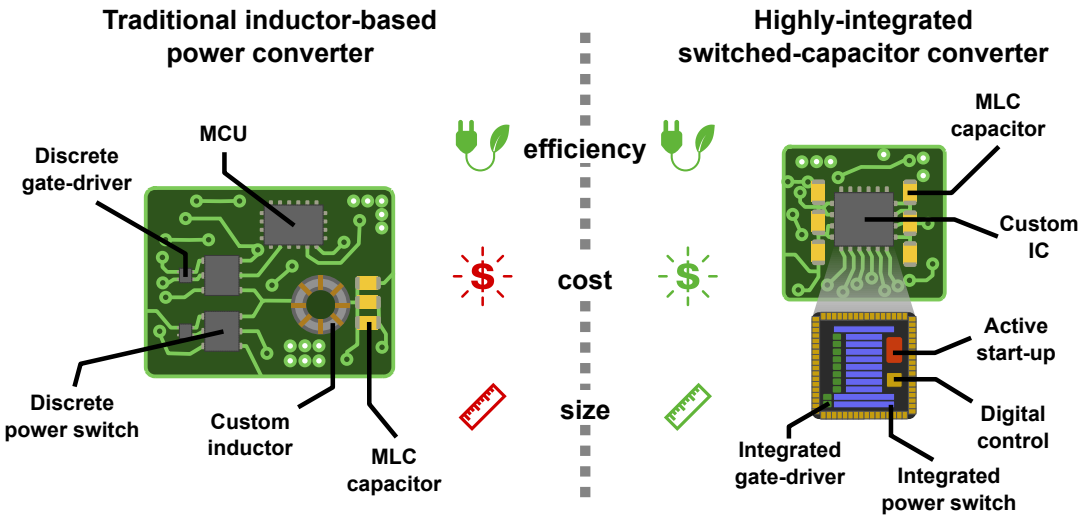



Figure 2.1: Simplified illustration comparing inductor-based converters and highly-integrated switched-capacitor converters.

required number of cascaded energy conversions from electrical production to electrical consumption, which increases the overall energy efficiency as we are moving towards point-of-load (PoL) converters.

An illustrated comparison between discrete inductor-based DC-DC converters and highly-integrated switched-capacitor DC-DC converters can be seen in Fig. 2.1. The use of discrete components for all required gate-drivers and power switches in the inductor-based converter leads to a larger PCB footprint increasing the overall volume and size. To achieve high efficiency, custom inductors are often used, which operate at high frequencies to reduce the inductance requirement and ultimately size. The increased switching frequency does however lead to higher losses in the power switches due to parasitic capacitances.

When moving towards higher voltages, the inductor-based converters suffer from the power switches having to tolerate the full input voltage. The increase in maximum voltage rating of power switches increases the on-state resistance of the power switches leading to an increase in conduction losses. Most state of the art inductor-based converters use Gallium-Nitride Field Effect Transistors (GaNFETs), which have a lower on-state resistance compared to silicon-based MOSFETs.

In the case of the highly-integrated switched-capacitor converters, the gate-drivers, power switches and digital control are all be monolithic integrated. This reduces the size and allows for customization on the requirements and operation of these circuits. Another benefit of switched-capacitor topologies is that the power switches only needs to block a fraction of the input voltage dependent on topology and conversion ratio of the implementation. This means that lower voltage devices with lower on-state resistance can be used, thereby achieving high efficiency even for larger input voltages.

Fully-integrated switched-capacitor converters have generally been designed for low voltage, and low power applications [18]–[25]. While a fully-integrated switched-capacitor IC from 400 V-12 V has recently been published in [26], they are still constrained to power levels below 1 W, which is mainly due to the low energy density of on-chip capacitors. Fully-integrated power converters using on-chip inductors have also been reported in [27]–[32]. Common for these are low peak efficiencies, input voltages and maximum output power. This is due to the low Q-factor of integrated inductors, which limits the possible performance since very high switching frequencies must be used [33]–[35].

The utilization of the power switch voltage blocking benefit of switched-capacitor converters, the integration and application specific design of integrated gate-drivers, power stage and digital control together with energy dense discrete capacitors is the main motivation for using highly-integrated switched-capacitor converters in medium power level applications compared to inductor-based converters.

## 2.2 Capacitance density comparison

The capacitance density for different DC bias voltages and types of capacitors can be seen in Fig. 2.2. In this example Murata Multi Layer Ceramic (MLC) capacitors are used with different standard package sizes[1]. All the considered MLC capacitors are of the general purpose series (GRM) with a temperature range of $-55\,°C$-$125\,°C$ and a capacitance tolerance of $\pm 10\,\%$. A 10 V, 25 V and 50 V maximum voltage rating is included for all considered package sizes. The capacitance of MLC capacitors depends heavily on the

[1] capacitor values extracted using Murata's SimSurfing tool: https://ds.murata.co.jp/simsurfing/

DC bias voltage, therefore it is important to take this into account when choosing the discrete components.

In Fig. 2.2 an integrated MOSFET capacitor (MOSCAP) and an integrated triple metal-insulator-metal (TMIM) capacitor are also shown. While the capacitance of these does not depend much on DC bias voltages, their capacitance densities are more than a magnitude lower compared to discrete MLC capacitors. For the height of the integrated MOSCAP and TMIM a standard chip height of 750 µm is assumed. Additionally, the 3D structure silicon capacitor presented in [36] is also included. While, this silicon capacitor is still not available on the market and has a maximum breakdown voltage of 10 V and a lifetime operating DC bias voltage of 2 V it shows very promising results. The 3D silicon capacitor has a reported thickness below 50 µm enabling placement in between bumps in wafer-level chip scale packaging(WLCSP) allowing for small form factor highly-integrated power converters. The 3D silicon capacitor is included for this comparison mainly to give a glimpse of the future prospect of highly-integrated power converters using external capacitors.

From Fig. 2.2 it can be seen that in regards of power density, when DC bias voltages of 10 V is required a 0402 package MLC capacitor should be used. While when moving towards 25 V the 0805 and 1206 package size have a very similar capacitance density and should be used instead to maximize capacitance density.

Due to the large difference in capacitance density between discrete MLC capacitors and integrated TMIM or MOSCAP capacitors, discrete capacitors should be used for applications which aims to supply above 1 W of output power. Integrating the gate-drivers,

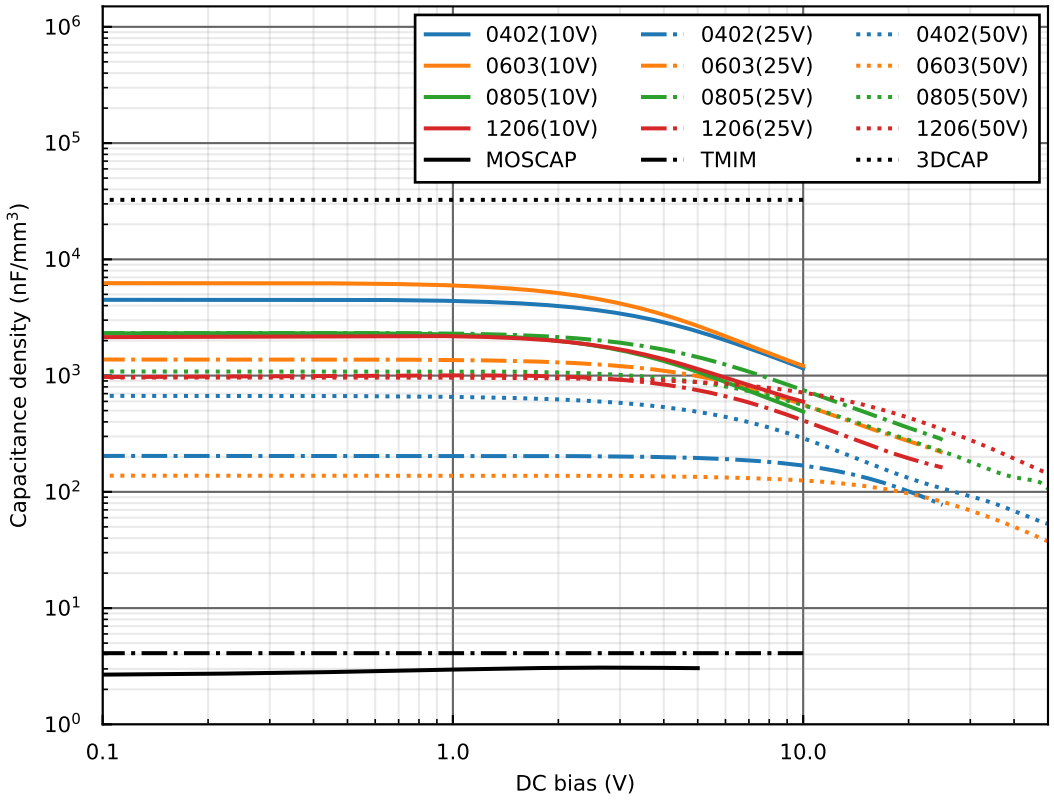



Figure 2.2: Capacitor density for different DC bias voltages and capacitor types.

power switches and digital control on-chip ensure low volume and the possibility of more complex and application specific implementations. These are the main benefits of highly-integrated power converters.

Highly-integrated switched-capacitor converters utilizes the advancements in high-voltage CMOS processes together with the superior power density of MLC capacitors to increase the maximum power and power density of switched-capacitor converters. For switched-capacitor converters considering the DC bias derating of the flying capacitors is essential, since all flying capacitors usually block a fraction of the input voltage. Thereby, making it vital when moving towards higher input voltages as the capacitor values directly effect the energy efficiency of the switched-capacitor converters.

## 2.3 State of the art of power converters

To investigate the performance of state of the art power converters a broad survey has been conducted. The point of the survey is not to do direct comparisons but to attempt to see trends and patterns for different implementation types and their power levels. In this survey power converters are split into 9 different types. These types and the used annotation to distinguish them are described in Table 2.1. In the case of discrete and highly-integrated implementations the PCB thickness is taken into account. Where the PCB thickness is not reported in the published work, a 1.6 mm thickness, which is the most common for a 2 layer PCB is assumed. For the fully-integrated solutions, unless otherwise stated, a 750 µm die thickness is used to convert from the typical area-form power density to volumetric-form. Fully-integrated solutions that are not intended for interfacing with an external source or load are not considered in this survey. The implementations are all reported from 2007-2023 to ensure recent advancements. Only DC-DC converters are considered. AC-DC implementations are considered, when the performance of only the DC-DC step is reported as well and the volume not taking into account the rectification can be estimated. The maximum input voltage is below 400 V and maximum output power is between 1 mW-1 kW. The implementations used in the survey can be seen in Table 2.2.

The data from Table 2.2 have been illustrated in Fig. 2.3 for four different metrics. In

Table 2.1: Power converter groups for state of the art survey and their used prefix and suffix to distinguish them.

| Implementation | Type | prefix | suffix |
|---|---|---|---|
| Discrete | inductive switch-mode power supply | di- | -smps |
| | switched-capacitor converter | di- | -scc |
| | hybrid converter | di- | -hscc |
| Highly-integrated | inductive switch-mode power supply | hi- | -smps |
| | switched-capacitor converter | hi- | -scc |
| | hybrid converter | hi- | -hscc |
| Fully-integrated | inductive switch-mode power supply | fi- | -smps |
| | switched-capacitor converter | fi- | -scc |
| | hybrid converter | fi- | -hscc |

Fig. 2.3a the peak efficiency versus the maximum output power of the implementations can be seen. Here it can be seen that for higher power the discrete implementations dominate, which is related to thermal limitations of integrated solutions due to heating from intrinsic power losses. For power levels between 1-100 W highly-integrated implementations show a promising and in some cases such as [37] and [38] even outperforming discrete implementations in terms of peak efficiency at similar power levels. The fully-integrated solutions are all limited to below 1 W and the highest achieved efficiency of 84.7 % is reported in [39].

In Fig. 2.3b the maximum power density versus the maximum output power can be seen for all implementations. Here it can clearly be seen, that while the fully-integrated solutions are limited in maximum output power their power density is high due to the monolithic integration. The highest overall power density is achieved by [37] and is a highly-integrated switched-capacitor converter. Note, that for higher power levels the discrete solutions cannot compete on power density with the highly-integrated solutions. The discrete solutions with the highest power density are are switched-capacitor and hybrid switched-capacitor converters, indicating that these implementations can achieve higher power density than traditional inductor-based converters.

Since input voltage greatly effects the design challenges of power converters, a figure showing power density versus input voltage can be seen in Fig. 2.3c. Here it can clearly be seen that the fully-integrated solutions have in general been limited to lower input voltages, which is due to technology limitations of semiconductor fabrication. The recent 400 V-12 V switched-capacitor converter implementation in [26] is pushing that boundary using a 180 nm high-voltage SOI-BCD process with devices that can tolerate up to 375 V. In the popular 48 V input voltage application space, the hybrid and switched-capacitor converters are achieving the greatest power density.

To take into account the conversion ratio the Efficiency Enhancement Factor (EEF) [40] is used and shown versus maximum power in Fig. 2.3d. The EEF compares the achieved efficiency to that of an ideal linear regulator:

$$EEF = 1 - \frac{\eta_{lin}}{\eta_i} \tag{2.1}$$

where $\eta_i$ is the efficiency of the implementation and $\eta_{lin}$ is the efficiency of an ideal linear regulator, which can be described as just:

$$\eta_{lin} = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \frac{V_{out}}{V_{in}} \tag{2.2}$$

since $I_{out} = I_{in}$ for a linear regulator. The EEF thereby indicates how much better the implementation is in terms of efficiency compared to an ideal linear regulator.

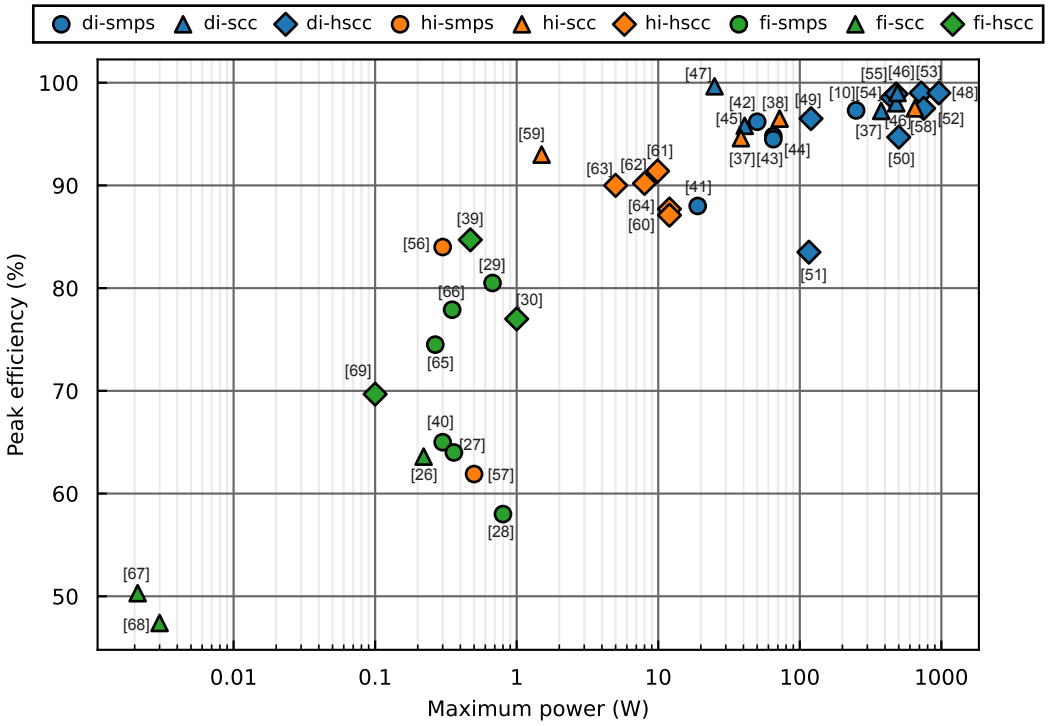
From Fig. 2.3d it can be seen solutions including an inductor such as the traditional inductor-based converters and the hybrid switched-capacitor converters achieve the highest EEF. The highly-integrated solutions achieve very high EEF in their power levels, showing the benefits of partial monolithic integration in achieving high performance.

Additional figures comparing various performance metrics can be found in Appendix E.

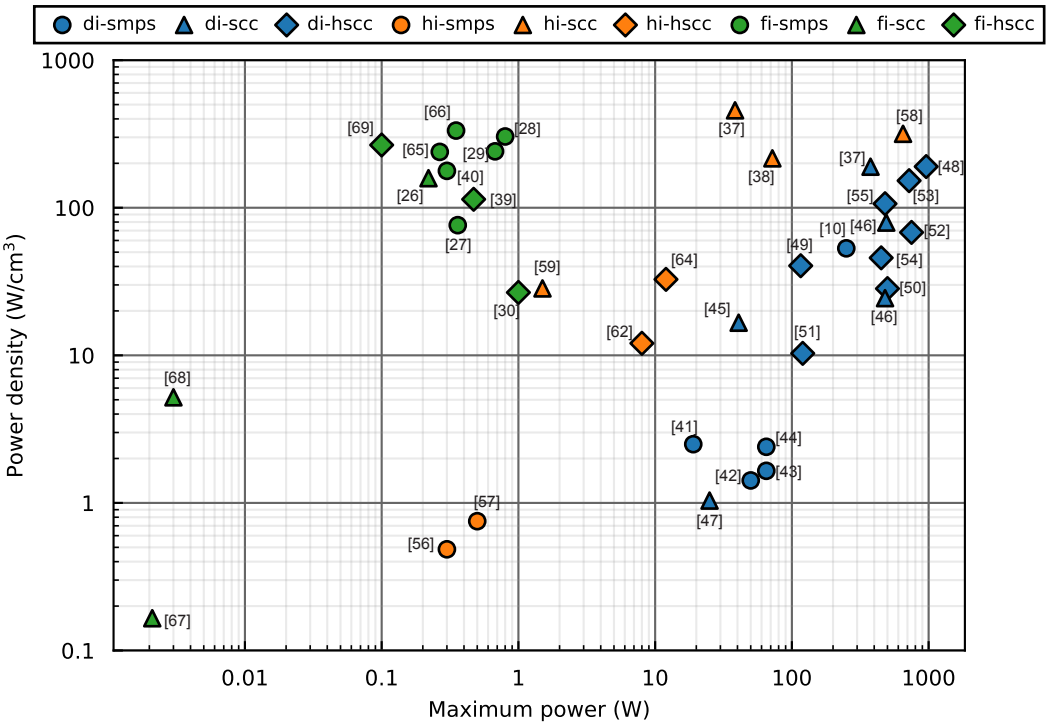
Table 2.2: State of the art survey implementations.

| Implementation | | Author | Year | $V_{in}$ (V) | $V_{out}$ (V) | Max. power (W) | Volume ($cm^3$) | Power density ($W/cm^3$) | Peak efficiency (%) | EEF (%) | fsw (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Discrete | di-smps | [41] | 2020 | 48 | 30 | 19 | 7.6 | 2.5 | 88 | +28.98 | 14 |
| | | [42] | 2019 | 380 | 9 | 50 | 35.211 | 1.42 | 96.2 | +97.54 | 1.3M |
| | | [43] | 2018 | 190 | 20 | 65 | 39.394 | 1.65 | 94.8 | +88.9 | 0.22 |
| | | [44] | 2018 | 230 | 20 | 65 | 27.083 | 2.4 | 94.5 | +90.8 | 0.49 |
| | | [10] | 2017 | 48 | 12 | 250 | 4.7089 | 53.09 | 97.3 | +74.31 | 1.6 |
| | di-scc | [37] | 2023 | 48 | 12 | 376 | 1.982 | 189.7 | 97.25 | +74.29 | 0.5 |
| | | [45] | 2021 | 16 | 4 | 40.8 | 2.4527* | 16.63 | 95.8 | +73.9 | 0.6 |
| | | [46] | 2018 | 48 | 12 | 480 | 19.664† | 24.41 | 98 | +74.49 | 0.2 |
| | | [46] | 2018 | 48 | 24 | 490 | 6.1767† | 79.33 | 99 | +49.5 | 0.2 |
| | | [47] | 2016 | 18 | 4.5 | 25 | 24.096*† | 1.038 | 99.65 | +74.91 | 0.1 |
| | di-hscc | [48] | 2023 | 48 | 12 | 960 | 5.0503* | 190.1 | 99 | +74.75 | 0.1 |
| | | [49] | 2023 | 48 | 1 | 116 | 2.8671 | 40.46 | 83.5 | +97.5 | 0.75 |
| | | [50] | 2023 | 48 | 1 | 500 | 17.658 | 28.32 | 94.7 | +97.8 | 0.15 |
| | | [51] | 2022 | 48 | 6 | 120 | 11.636 | 10.313 | 96.5 | +87.05 | 0.1 |
| | | [52] | 2022 | 48 | 5.1 | 750 | 11.02 | 68.058 | 97.5 | +89.10 | 0.45 |
| | | [53] | 2019 | 48 | 12 | 720 | 4.7195 | 152.6 | 99 | +74.75 | 0.1 |
| | | [54] | 2018 | 54 | 8.82 | 450 | 9.8322 | 45.77 | 98.6 | +83.43 | 0.387 |
| | | [55] | 2018 | 48 | 12 | 480 | 4.5 | 106.5 | 98.9 | +74.72 | 0.1 |
| Highly-integrated | hi-smps | [56] | 2022 | 12.5 | 10 | 0.3 | 0.655 | 0.485 | 84 | +4.762 | 2 |
| | | [57] | 2021 | 325 | 10 | 0.5 | 0.6649 | 0.752 | 61.9 | +95.03 | 1 |
| | hi-scc | [37] | 2022 | 48 | 12 | 38.4 | 0.084 | 457.1 | 94.6 | +73.57 | 0.5 |
| | | [58] | 2021 | 40 | 10 | 650 | 2.0511 | 316.9 | 97.5 | +74.36 | n.r. |
| | | [38] | 2021 | 48 | 12 | 72 | 0.3332 | 216.1 | 96.5 | +74.09 | n.r. |
| | | [59] | 2009 | 12 | 1.5 | 1.5 | 0.0528 | 28.41 | 93 | +86.56 | n.r. |
| | hi-hscc | [60] | 2022 | 48 | 1.2 | 12 | n.r. | n.r. | 87.1 | +97.13 | 0.5 |
| | | [61] | 2021 | 48 | 3.3 | 9.9 | n.r. | n.r. | 91.4 | +92.48 | 0.32 |
| | | [62] | 2021 | 48 | 1 | 8 | 0.663 | 12.07 | 90.2 | +97.69 | 2.5 |
| | | [63] | 2016 | 48 | 10 | 5 | n.r. | n.r. | 90 | +76.85 | 2 |
| | | [64] | 2016 | 12 | 1.2 | 12 | 0.3668 | 32.71 | 87.7 | +88.6 | 2 |
| Fully-integrated | fi-smps | [65] | 2011 | 1.2 | 0.88 | 0.266 | 0.0011 | 239 | 74.5 | +1.566 | 300 |
| | | [28] | 2009 | 2.6 | 1.2 | 0.8 | 0.0026 | 304 | 58 | +20.42 | 225 |
| | | [29] | 2009 | 3.3 | 2.5 | 0.675 | 0.0028 | 241.1 | 80.5 | +5.891 | 180 |
| | | [40] | 2008 | 3.6 | 1.8 | 0.3 | 0.0017 | 177.8 | 65 | +23.08 | 140 |
| | | [66] | 2008 | 1.2 | 0.9 | 0.35 | 0.0011 | 333.3 | 77.9 | +3.723 | 170 |
| | | [27] | 2007 | 2.8 | 1.8 | 0.36 | 0.0047 | 76.19 | 64 | -0.446 | 45 |
| | fi-scc | [26] | 2022 | 400 | 12 | 0.22 | 0.0014 | 158.6 | 63.6 | +95.28 | n.r. |
| | | [67] | 2020 | 42 | 3 | 0.002 | 0.0127 | 0.165 | 50.3 | +85.8 | n.r. |
| | | [68] | 2018 | 17 | 3.3 | 0.003 | 0.0006 | 5.195 | 47.4 | +59.05 | n.r. |
| | fi-hscc | [39] | 2023 | 2.5 | 1.25 | 0.471 | 0.0041 | 114.1 | 84.7 | +40.97 | 44 |
| | | [30] | 2012 | 2.4 | 1 | 1 | 0.0375 | 26.67 | 77 | +45.89 | 200 |
| | | [69] | 2008 | 3.6 | 1 | 0.1 | 0.0004 | 266.1 | 69.68 | +60.14 | 37.3 |

*Estimated from paper, †gate-driver area not included, n.r. = Not reported.

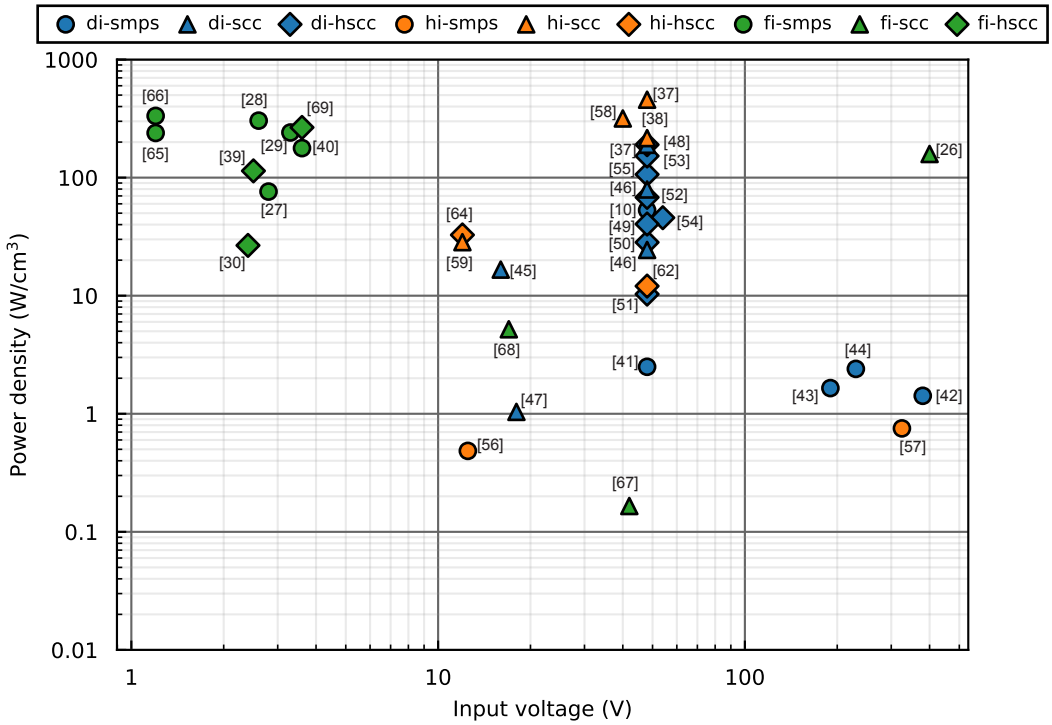



(a) Peak efficiency versus maximum output power for state of the art power converters.

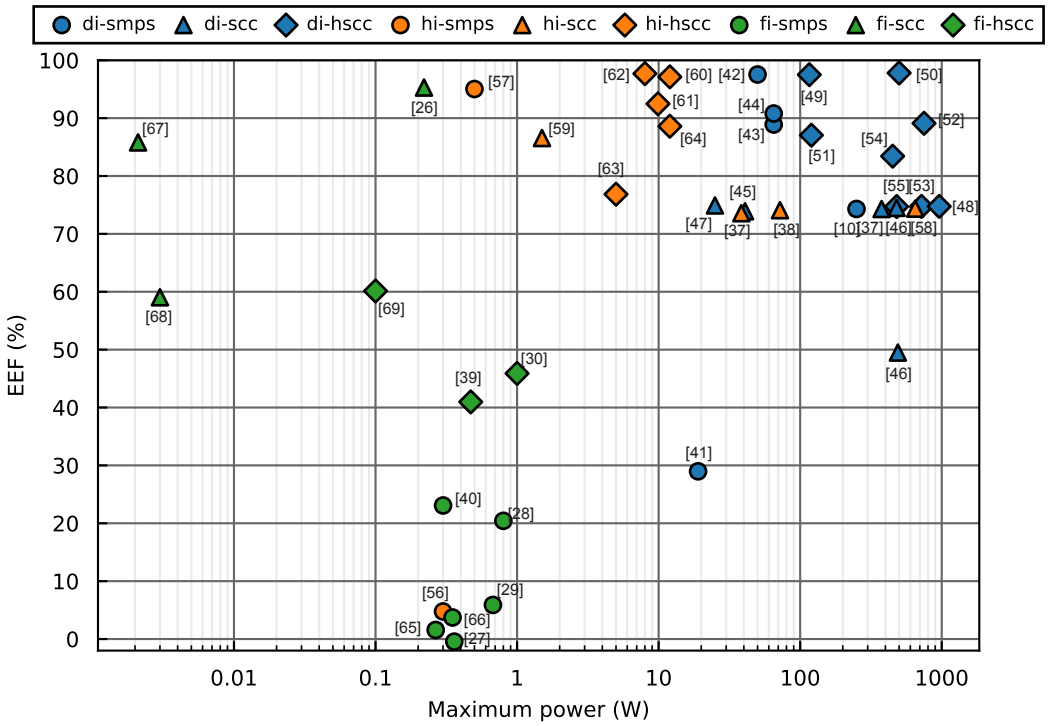



(b) Power density versus maximum output power for state of the art power converters.

Figure 2.3: State of the art survey for power converters up to 1 kW and maximum input voltage of 400 V.




(c) Power density versus input voltage for state of the art power converters




(d) Efficiency Enhancement Factor (EEF) versus maximum output power for state of the art power converters

Figure 2.3: State of the art survey for power converters up to 1 kW and maximum input voltage of 400 V.

## 2.4 Summary

In this chapter, a brief overview of the different advantages and disadvantages of traditional inductor-based power converters and switched-capacitor converters is provided. The better switch utilization in switched-capacitor converters, due to the lowered voltage stress, leads to the motivation for designing switched-capacitor converters for high-conversion ratio applications. A comparison of capacitance densities between integrated and discrete capacitors was also shown. This comparison demonstrated that due to the much higher capacitance density and maximum voltage ratings of the MLC capacitors, external flying capacitors are necessary for applications where higher output power is required. Finally, a state of the art survey was presented, comparing 41 various implementations divided into 9 categories. Here, the potential advantages of using highly-integrated switched-capacitor-based power converters in medium power levels of 1-100 W were shown. The power converter implementations were compared across 4 different performance metrics. The state of the art survey motivates the design of highly-integrated switched-capacitor converters for medium power levels.

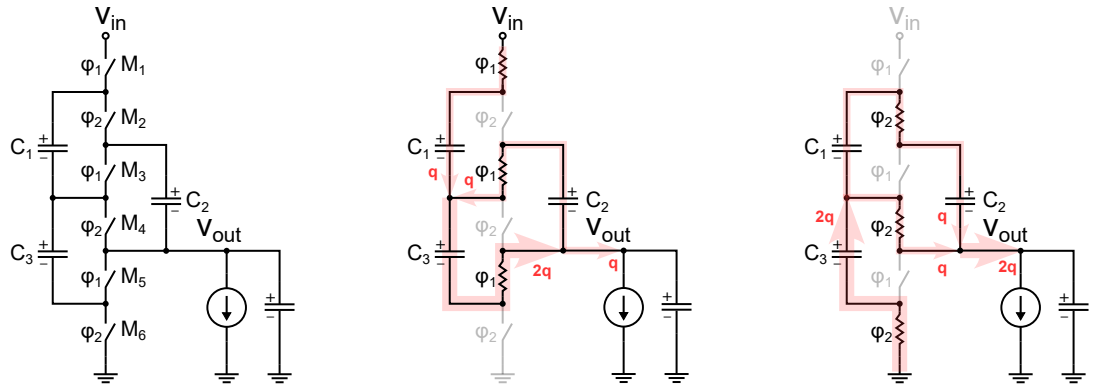
# 3 Fundamental analysis of highly-integrated switched-capacitor converters

In this chapter, the fundamental analysis and background of switched-capacitor converters are described. This involves the switching operation, their equivalent phase networks and how they relate to the simplified ideal transformer model. The main power losses of switched-capacitor converters are also described.

## 3.1 Switched-capacitor operation and modeling

Switched-capacitor converters operate by transferring charge from the input voltage source to an output load through capacitor phase networks, that are controlled and connected by switches. A switched-capacitor topology is a unique connection of flying capacitors and switches, that result is a specific charge transfer from the input to the output. Many popular topologies like the Dickson, Ladder, Series-parallel and Fibonacci topology can be extended in a repeating manner to achieve different voltage conversion ratios. The analysis and understanding of the operation and modeling of switched-capacitor converters has been covered in [70]–[74]. Any topology and its conversion ratio can be analyzed by looking at the topology in each of the switching phases [73], [75]. These equivalent circuits are referred to as the phase network equivalent circuits.

In Fig. 3.1 a two-phase 3:1 Ladder topology can be seen with its equivalent phase networks in Fig. 3.1b and Fig. 3.1c for phase 1 and phase 2, respectively. When the switches are turned on, they are simplified to resistors corresponding to the on-state resistance of the switches. The charge flow has been visualized in both phases. The charge flow can be determined by visual inspection as described in [75], by realizing that the charge of each capacitor across all phases (a full switching period) must sum to zero in periodic steady-state operation. A starting point, such as $C_1$ in phase 1 ($\varphi_1$) is often a good choice, but any starting point can be used. Solving the charge flow analysis is then a matter of




(a) 3:1 Ladder topology.

(b) Phase network during $\varphi_1$ of 3:1 Ladder topology.

(c) Phase network during $\varphi_2$ of 3:1 Ladder topology.

Figure 3.1: The phase networks of a 3:1 Ladder topology.

determining the capacitor charges going back and forth between the phase networks and using Kirchoff's' current law (KCL).

The charge flow for the flying capacitors is referred to as the capacitor charge flow multiplier and is often normalized by the total charge flowing to the output load:

$$\mathbf{a_c^j} = [q_{c,1}^j \quad q_{c,2}^j \quad \cdots \quad q_{c,N}^j]^T / q_{out} \tag{3.1}$$

Where $N$ is the number of flying capacitors and $j$ refers to the switching phase. Note, that for a two-phase switched-capacitor converter that $a_{c,i}^1 = -a_{c,i}^2$ due to energy conservation.

For the 3:1 Ladder in Fig. 3.1a the capacitor charge flow multiplier in each phase is:

$$\begin{aligned} \mathbf{a_c^1} &= [1/3 \quad -1/3 \quad 2/3]^T \\ \mathbf{a_c^2} &= [-1/3 \quad 1/3 \quad -2/3]^T \end{aligned} \tag{3.2}$$

Similarly, the charge flowing in the switches can be determined from the charge flow analysis. Note, that for the switches, the charge does not sum to zero. Charge only flows when the switch is turned on. The switch charge flow multiplier is defined as:

$$\mathbf{a_r^j} = [q_{sw,1}^j \quad q_{sw,2}^j \quad \cdots \quad q_{sw,N}^j]^T / q_{out} \tag{3.3}$$

where $N$ refers to the number of switches and $j$ refers to the phase. Note, that for a two-phase switched-capacitor converter the charge flow multiplier will be zero in one phase.

The switch charge flow multiplier for the 3:1 Ladder topology is:

$$\begin{aligned} \mathbf{a_r^1} &= [1/3 \quad 0 \quad 1/3 \quad 0 \quad -2/3 \quad 0]^T \\ \mathbf{a_r^2} &= [0 \quad 1/3 \quad 0 \quad 1/3 \quad 0 \quad -2/3]^T \end{aligned} \tag{3.4}$$

The ideal conversion ratio of a switched-capacitor topology can be determined by assuming no power loss in the converter:

$$P_{in} = P_{out} \tag{3.5}$$

Rewriting in terms of average input and output voltage and currents:

$$V_{in} \cdot I_{in} = V_{out} \cdot I_{out} \tag{3.6}$$

The average input and output current depends on the input and output charge and the switching period:

$$V_{in} \cdot q_{in} / T_{sw} = V_{out} \cdot q_{out} / T_{sw} \tag{3.7}$$

Isolating the ideal conversion ratio $M/N = V_{in}/V_{out}$:

$$\frac{V_{in}}{V_{out}} = \frac{q_{out}}{q_{in}} \tag{3.8}$$

In the case of the 3:1 Ladder converter the ideal voltage conversion ratio can be determined by:

$$M/N = q_{out}/q_{in} = 3/1 \tag{3.9}$$

This will be the voltage conversion ratio in the case of a lossless converter. In reality, there are losses associated with the conduction of the switches and the charge redistribution of the flying capacitors, which effects the voltage conversion ratio.

### 3.1.1 The slow-switching limit

In this section the slow-switching limit is presented and discussed to assess the frequency dependent intrinsic losses of switched-capacitor converters due to capacitor voltage mismatch leading to charge redistribution losses.

Consider the 2:1 series-parallel topology in Fig. 3.2 with the equivalent phase networks. In this example, the output capacitance is considered infinitely large, equaling a voltage source $V_{out}$. During phase two ($\varphi_2$), the capacitor $C_1$ is being discharged from the output load through the $RC$-network. This charge transfer from $C_1$ to the output leads to a voltage change on the $C_1$ flying capacitor. The voltage across the capacitor can be expressed as:

$$v_{c,1}(t) = (V_{out} - v_{c1,t=0}) \left(1 - e^{-\frac{t}{RC_1}}\right) \tag{3.10}$$

Where $R$ is the total series resistance of both switches, and in reality also of the equivalent series resistance (ESR) of the flying capacitor. The $v_{c1,t=0}$ is the initial voltage across the capacitor at the start of phase 2. $V_{out} - v_{c1,t=0}$ is the initial voltage difference between the capacitor and the output voltage. This is denoted as:

$$\Delta V_{c,1} = V_{out} - v_{c1,t=0} \tag{3.11}$$

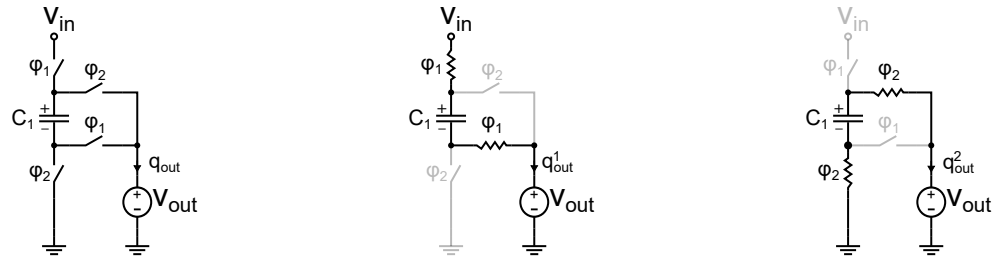
The energy is dissipated in the series resistor. The current in the series resistor is:

$$i_R(t) = \frac{V_{out} - v_{c,1}(t)}{R} \tag{3.12}$$

The energy dissipated in the resistor can be expressed as:

$$E_R = \int_{t=0}^{T} R \cdot i_R(t)^2 dt \tag{3.13}$$

Where $T$ is the charging time. We assess the energy dissipated in the resistor during a single phase, since the total dissipated energy is simply twice that for a two-phase converter, when we operate in periodic steady-state. Meaning ,that the total switching period $T_{sw} = 2 \cdot T$, assuming that the phases have equal duration, i.e. 50 % duty cycle.




(a) 2:1 series-parallel. (b) Phase network during $\varphi_1$. (c) Phase network during $\varphi_2$.

Figure 3.2: The phase networks of a 2:1 series-parallel topology.

The energy dissipated in the resistor during a single phase is:

$$\begin{aligned} E_R &= \int_{t=0}^{T} R \cdot i_R(t)^2 dt \\ &= \int_{t=0}^{T} R \cdot \left( \frac{V_{out} - v_{c,1}(t)}{R} \right)^2 dt \\ &= \int_{t=0}^{T} \frac{\Delta V_{c,1}^2}{R} e^{-\frac{2t}{RC_1}} dt \\ &= \frac{\Delta V_{c,1}^2}{R} \left[ -\frac{RC_1}{2} e^{\frac{-2 \cdot 0}{RC_1}} + \frac{RC_1}{2} e^{\frac{-2 \cdot T}{RC_1}} \right] \end{aligned} \tag{3.14}$$

Assuming that the charging time, $T$, is much longer than the time constant of the $RC_1$-network. This assumption of $T \gg RC_1$ is the slow-switching limit region. Evaluating the energy dissipated in the resistor then simplifies to:

$$E_R = \frac{1}{2} C_1 \Delta V_{c,1}^2 \tag{3.15}$$

Which is the well known energy dissipation of a resistor in an RC network, when a capacitor is being charged/discharged. Note, that while the energy is dissipated in the resistor, it is not dependent on its size.

For a switched-capacitor converter the capacitor is charged and discharged various times across a switching period. The average power dissipation is therefore:

$$\begin{aligned} P_R &= E_R \cdot f_{sw} \\ &= \frac{1}{2} C_1 \Delta V_{c,1}^2 f_{sw} \end{aligned} \tag{3.16}$$

The voltage change $\Delta V_{c,1}$ can be rewritten as:

$$\Delta V_{c,1} = \frac{|q_{c,1}^1|}{C_1} = \frac{|q_{c,1}^2|}{C_1} \tag{3.17}$$

where $q_{c,1}^1$ and $q_{c,2}^2$ is the charge in $C_1$ during phase 1 and phase 2 respectively.

The average output load current can be described as:

$$I_{load,avg} = q_{out} \cdot f_{sw} \tag{3.18}$$

Here $q_{out}$ is the total charge in both switching cycles. Note, that for the series-parallel topology all the charge delivered to the output load comes from the flying capacitor. This means that:

$$|q_{c,1}^1| + |q_{c,1}^2| = q_{out} \tag{3.19}$$

and due to conservation of energy:

$$q_{c,1}^1 = -q_{c,1}^2 \tag{3.20}$$

Which yields that:

$$|q_{c,1}^1| = |q_{c,1}^2| = \frac{1}{2} q_{out} \tag{3.21}$$

Now using (3.17), (3.18) and (3.21) the capacitor voltage mismatch $\Delta V_{c,1}$ can be rewritten as:

$$\Delta V_{c,1} = \frac{I_{load,avg}}{2C_1 f_{sw}} \tag{3.22}$$

Inserting (3.22) into (3.16) yields:

$$P_R = \frac{1}{8C_1 f_{sw}} (I_{load,avg})^2 \tag{3.23}$$

This is the power loss due to the charge redistribution per switching phase. For the series-parallel with two phases, the total power loss due to the charge redistribution is therefore:

$$\begin{aligned} P_{loss} &= 2 \cdot \frac{1}{8C_1 f_{sw}} (I_{load,avg})^2 \\ &= \frac{1}{4C_1 f_{sw}} (I_{load,avg})^2 \end{aligned} \tag{3.24}$$

Note, that these losses only occur, whenever charge is being delivered to the output load. This makes it different from other frequency dependent losses such as parasitic capacitor switching losses in the switches and bottom-plate losses from capacitors, which do not depend on the output load. From (3.24) it can be seen, that the power loss due to the charge redistribution is lowered when increasing switching frequency of the capacitance. The equivalent resistance of the two-phase series-parallel topology due to charge redistribution losses can easily be seen from (3.24):

$$R_{SSL} = \frac{1}{4C_1 f_{sw}} \tag{3.25}$$

In [75] it was shown, that for more complicated topologies than the 2:1 series-parallel the equivalent resistance $R_{SSL}$ due to charge redistribution losses, can be written as.

$$R_{SSL} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} \frac{\left(a_{c,i}^{j}\right)^2}{2C_i f_{sw}} \tag{3.26}$$

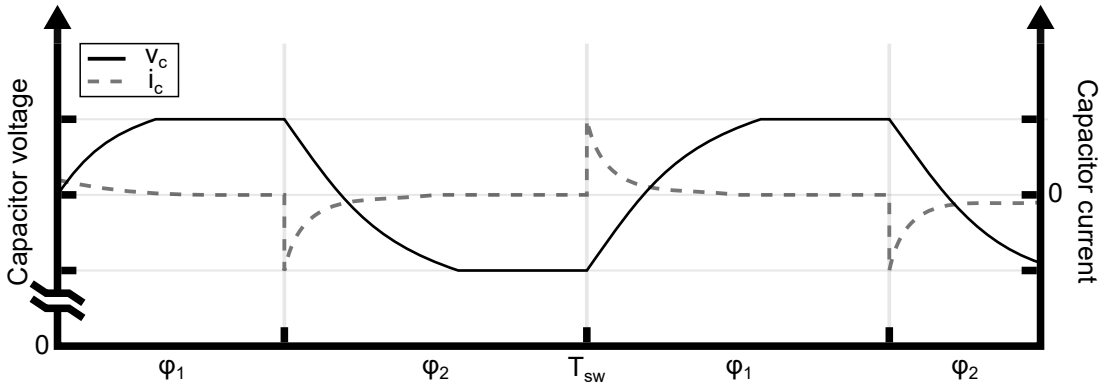



Figure 3.3: Illustration of flying capacitor voltage and current waveforms when operating in the slow-switching limit region.

Here the expression takes into account any number of flying capacitors and switching phases with the individual losses from each capacitor being a linear combination dependent on how much of the charge delivered to the output that comes from each flying capacitor. Note, that the series resistance from the capacitor ESR and switch on-state resistance does not contribute to the charge redistribution losses.

The flying capacitor voltage and current waveforms when operating in the slow-switching limit can be seen in Fig. 3.3 and with an voltage source output load. The charging and discharging happens at the start of each phase, leading to large peak currents.

### 3.1.2 The fast-switching limit

In this section the fast-switching limit is presented and discussed to assess the intrinsic conduction losses of switched-capacitor converters from the on-state resistance of the switches.

The total conduction losses of the on-state resistance of the switches due to charge being delivered to the load can be examined by considering the linear combination of the charge flowing in each power switch during a whole switching period. The average current flowing in each switch during any phase can be described as:

$$i_r^j = \frac{q_r^j}{D_j} f_{sw} \tag{3.27}$$

Where $D_j$ is the duty cycle of the phase. For equal phase times, the simplifies to $D_j = 1/n$, where $n$ is the number of phases. The average current in the switch is always a fraction of the average load current. Using that the average load current can be expressed as:

$$I_{load,avg} = q_{out} \cdot f_{sw} \tag{3.28}$$

We can rewrite (3.27) as:

$$i_r^j = \frac{q_r^j}{q_{out} D_j} \cdot I_{load,avg} \tag{3.29}$$

The average power dissipated in each switch during each phase can then be expressed as:

$$\begin{aligned} P_r^j &= D_j \cdot R \cdot (i_r^j)^2 \\ &= \frac{R}{D_j} \left( \frac{q_r^j}{q_{out}} \cdot I_{load,avg} \right)^2 \end{aligned} \tag{3.30}$$

The total power dissipated in all switches is then simply the sum of all switch losses and across all phases:

$$P_{FSL} = \sum_{i}^{N_{switches}} \sum_{j=1}^{n} \frac{R_i}{D_j} \left( \frac{q_{r,i}^j}{q_{out}} \cdot I_{load,avg} \right)^2 \tag{3.31}$$

While the slow-switching limit losses decreased with frequency, the conduction losses of the switches do not. This means, that for a high switching frequency, these conduction losses will dominate leading to the fast-switching limit region naming. The equivalent resistance due to the fast-switching losses is then:

$$R_{FSL} = \sum_{i}^{N_{switches}} \sum_{j=1}^{n} \frac{R_i}{D_j} (a_{r,i}^j)^2 \tag{3.32}$$

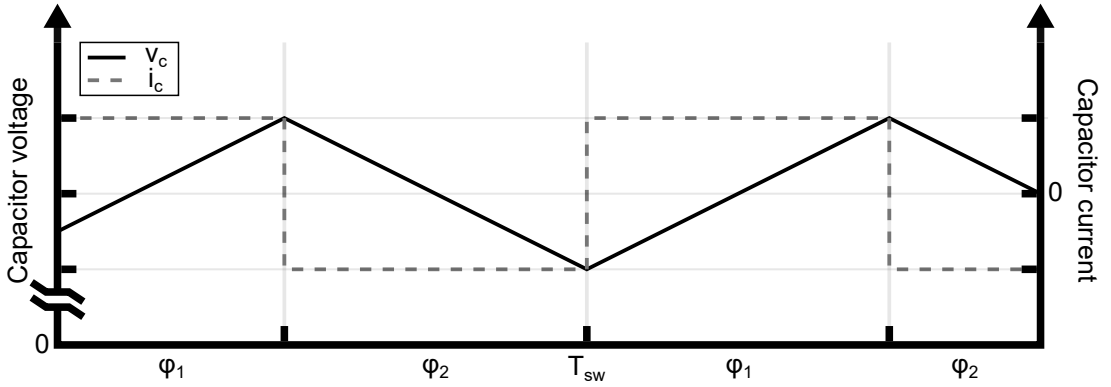



Figure 3.4: Illustration of flying capacitor voltage and current waveforms when operating in the fast-switching limit region.

where $a_{r,i}$ is simply:

$$a_{r,i}^{j} = \frac{q_{r,i}^{j}}{q_{out}} \tag{3.33}$$

In Fig. 3.4 the flying capacitor waveforms can be seen when operating in the extreme fast-switching limit region. Since the switching period is very short, very little charge is being delivered to and from the flying capacitor each phase. Thereby, almost no voltage mismatch occurs leading to no charge redistribution losses. While, the waveform in Fig. 3.4 looks identical to the charging/discharging of a capacitor using a constant current source, it is simply equivalent to that of the slow-switching limit capacitor waveforms in Fig. 3.3, when considering only the first fractions of each phase.

## 3.2 Power losses in switched-capacitor converters

Any switched-capacitor topology can be modelled as a lossless transformer with a M:N turns ratio and a series resistance $R_{out}$ as seen in Fig. 3.5.

The series output resistance models all load dependent losses of the switched-capacitor converter. These include both the FSL losses due to the conduction of the switches and the SSL losses from the charge redistribution of the flying capacitors.

The equivalent series resistance and inductance of the flying capacitors also contribute to conduction losses of the topology. This can easily be incorporated into the approximated output resistance. The ESR loss contribution can be derived similarly as for the $R_{FSL}$, but considering that the charge flow vector is the same of the respective flying capacitor instead [75]:

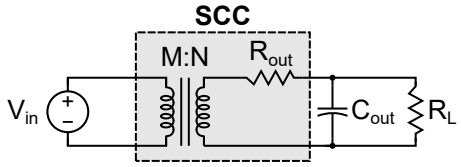



Figure 3.5: Simplified switched-capacitor converter (SCC) model consisting of a lossless transformer with a turn ratio of M:N and a series output resistance $R_{out}$.

$$P_{ESR} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} ESR_i \cdot (a_{c,i}^{j})^2 \cdot (I_{load,avg})^2 \tag{3.34}$$

The equivalent resistance due to ESR losses $R_{ESR}$ is then:

$$R_{ESR} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} ESR_i \cdot (a_{c,i}^{j})^2 \tag{3.35}$$

Furthermore, the equivalent series inductance (ESL) loss contribution can be derived. The magnitude of the impedance of the inductor at a given frequency is:

$$ESL = 2\pi f_{sw} L \tag{3.36}$$

The ESL experience identical charge flows as in the case of the ESR leading to [75]:

$$P_{ESL} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} 2\pi f_{sw} \cdot ESL_i \cdot (a_{c,i}^{j})^2 \cdot (I_{load,avg})^2 \tag{3.37}$$

The equivalent resistance due to ESL losses $R_{ESL}$ is then:

$$R_{ESL} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} 2\pi f_{sw} \cdot ESL_i \cdot (a_{c,i}^{j})^2 \tag{3.38}$$

Incorporating these losses the equivalent series output resistance ($R_{out}$) of a switched-capacitor converter can then be approximated by [75]:

$$R_{out} = \sqrt{(R_{FSL} + R_{ESR} + R_{ESL})^2 + R_{SSL}^2} \tag{3.39}$$

The total losses due to the output resistance is then:

$$P_{rout} = R_{out} \cdot i_{out}^2 \tag{3.40}$$

In Fig. 3.6 an example of the fast-switching limit resistance ($R_{FSL}$), slow-switching limit resistance ($R_{SSL}$), the equivalent series resistance ($R_{ESR}$), the equivalent series inductance ($R_{ESL}$) and the approximated output resistance for a switched-capacitor converter can be seen as a function of switching frequency $f_{sw}$. As expected the $R_{SSL}$ decreases with an increase in frequency, with the slope being dependent on flying capacitor sizes and the capacitor charge multiplier vector ($\mathbf{a_c}$) of the topology. The $R_{FSL}$ is constant with frequency and only dependent on on-state resistance of the switches and the switch charge multiplier vector of the topology. The $R_{ESR}$ is also constant with frequency and usually much lower than the $R_{FSL}$. The parasitic inductance of the capacitor (ESL) leads to the output impedance increasing at higher frequencies. Usually, switched-capacitor converters are operated at a switching frequency close to the knee-region between the SSL and FSL regions [73].

While the load dependent losses from $R_{out}$ depend directly on the topology, there are losses which depends primarily on semiconductor fabrication technology and switching

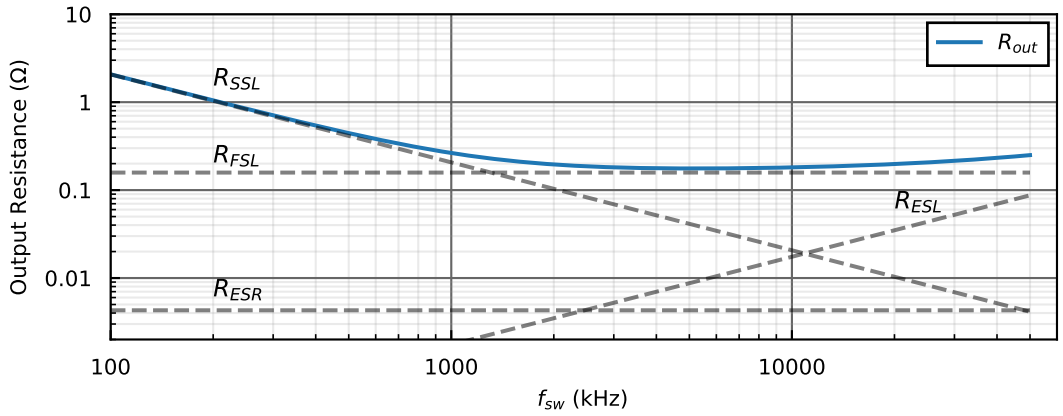



Figure 3.6: Output resistance for a switched-capacitor converter as a function of switching frequency.

frequency of the converter. One of the main losses is the switching losses from charging and discharging the parasitic drain capacitance of the switches. The energy required to charge/discharge this capacitor is:

$$E_{oss} = \frac{1}{2} Q_{oss} V_{ds} \tag{3.41}$$

where $Q_{oss}$ is the total required charge to charge the parasitic capacitance of the switch and $V_{ds}$ is the maximum blocking voltage of the switch. The total average switching power loss across a full period for each switch is then:

$$P_{sw} = \frac{n}{2} Q_{oss} V_{ds} f_{sw} \tag{3.42}$$

where $n$ is the number of phases in which the switch is charged/discharged. The required charge $Q_{oss}$ can be described as:

$$Q_{oss} = C_{oss} V_{ds} \tag{3.43}$$

Where $C_{oss}$ is the equivalent linearized capacitor of the switch. The total switching losses for any switched-capacitor converter is then simply the linear combination of these switching losses:

$$P_{sw} = \frac{n}{2} \sum_{i}^{N_{switches}} C_{oss} V_{ds,i}^2 f_{sw} \tag{3.44}$$

A benefit of switched-capacitor converters compared to traditional inductor-based converters is, that the switches only have to block a fraction of the total input voltage. The switch blocking voltages depend on conversion ratio and topology. This is one of the benefits for using switched-capacitor converters in implementations where a high conversion ratio is required. Naturally, more switches are also used compared to traditional inductor-based converters, such as a buck converter but since the switching loss scales with the blocking voltage squared, there is usually a benefit from using switched-capacitor converters.

For controlling the gate-signals of the switches, gate-drivers are required to drive the gate capacitance. The gate capacitance scales with the area of the switch and can become

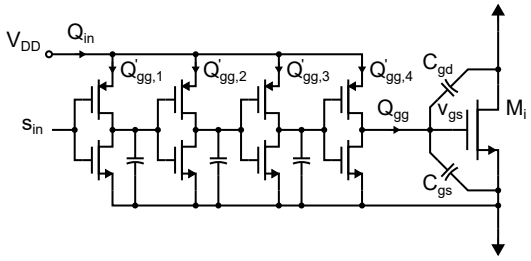



Figure 3.7: Buffer chain for illustrating charge efficiency, when driving a power switch.

significant in applications, where low on-state resistance, and thereby large area switches are required. Furthermore, the gate-drivers consisting of a buffer chain does not have a 100 % charge efficiency. This means, that some charge is required for driving the inverter chain. The charge efficiency of a buffer chain is defined as:

$$\alpha = Q_{gg}/Q_{in} \tag{3.45}$$

Where $Q_{gg}$ is the required charge for charging/discharging the total gate capacitance of the switch, and $Q_{in}$ is the charge drawn from the input source of the buffer chain. This is illustrated in Fig. 3.7, where $Q'_{gg,i}$ are all the charges required for driving the parasitic capacitances of the inverter stages. Usually, a charge efficiency above 95 % can easily be achieved by choosing a proper amount of inverter stages and inverter stage drive strength scalings.

The gate-driver losses of a single switch can then be approximated similarly as in the case of the switching losses, by first estimating the energy required to charge/discharge the parasitic capacitor and then evaluating it across a full switching period:

$$P_{gd} = \frac{n}{2\alpha} V_{DD} Q_{gg} f_{sw} \tag{3.46}$$

Where $n$ is the number of phases, in which the parasitic gate capacitance is charged. The total gate-driver losses is a linear combination of all the gate-driver losses:

$$P_{gd} = \frac{n}{2\alpha} \sum_{i}^{N_{switches}} V_{DD,i} Q_{gg,i} f_{sw} \tag{3.47}$$

Where it is assumed, that $\alpha$ is the same for all gate-drivers. Additionally, any idle losses due to the quiescent current of the implementation of the gate-driver itself will further add to these losses.

Other losses such as bottom-plate parasitic capacitance losses can be dominant in fully-integrated implementations, where the flying capacitors are integrated and of a similar magnitude in capacitance to the parasitic capacitance from the bottom-plate to the substrate. In general, for highly-integrated and discrete solutions, these parasitic capacitance losses are much less dominating, since the flying capacitors have a much larger capacitance.

## 3.3 Summary

This chapter presented a description of the fundamental operation of switched-capacitor converters. Furthermore, it presented the dominating power losses in highly-integrated switched-capacitor converters. These losses are summarized below:

**Intrinsic load dependent losses**
These are losses that are dependent on topology and load current. Here presented as equivalent resistances.

**Slow-switching limit loss resistance:**

$$R_{SSL} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} \frac{\left(a_{c,i}^{j}\right)^2}{2C_i f_{sw}} \tag{3.48}$$

**Fast-switching limit loss resistance:**

$$R_{FSL} = \sum_{i}^{N_{switches}} \sum_{j=1}^{n} \frac{R_i}{D_j} (a_{r,i}^{j})^2 \tag{3.49}$$

**Flying capacitor ESR loss resistance:**

$$R_{ESR} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} ESR_i \cdot (a_{c,i}^{j})^2 \tag{3.50}$$

**Flying capacitor ESL loss resistance:**

$$R_{ESL} = \sum_{i}^{N_{caps}} \sum_{j=1}^{n} 2\pi f_{sw} \cdot ESL_i \cdot (a_{c,i}^{j})^2 \tag{3.51}$$

The losses can be used to approximate the output resistance of the converter:

$$R_{out} = \sqrt{(R_{FSL} + R_{ESR} + R_{ESL})^2 + R_{SSL}^2} \tag{3.52}$$

**Parasitic frequency dependent losses**
These are losses that are dependent on topology, switch and capacitor technology and switching frequency of the converter.

**Switching losses:**

$$P_{sw} = \frac{n}{2} \sum_{i}^{N_{switches}} C_{oss} V_{ds,i}^2 f_{sw} \tag{3.53}$$

**Gate-driver losses:**

$$P_{gd} = \frac{n}{2\alpha} \sum_{i}^{N_{switches}} V_{DD,i} Q_{gg,i} f_{sw} \tag{3.54}$$

With these fundamental losses of switched-capacitor converters defined and understood an approach to minimize these to ensure a high energy-efficient design can be done.

# 4 Design and optimization of highly-integrated switched-capacitor converters

In this chapter the design and optimization of highly-integrated switched-capacitor converters is presented. Three different gate-driving methods of controlling the integrated switches of the converter are presented and compared in regards of power losses and complexity of implementation. The capacitance sizing of the discrete flying capacitors are then optimized using Lagrange Multiplier to minimize the slow-switching resistance under a PCB area constraint. The power losses of the integrated switches described in section 3.2 are then reformulated as function of total designated integrated switch area and switching frequency, to allow for an optimization of the integrated power stage. To verify the theoretical work a 48 V-12 V highly-integrated switched-capacitor converter has been designed and fabricated and the experimental results are presented and discussed.

This chapter is in general a more detailed description of the work presented in the publication shown in Appendix C, which was authored as a part of the Ph.D. project.

## 4.1 Gate-driver considerations

This section describes different methods of driving the power switches in switched-capacitor converters and compares their respective benefits and downsides. A discussion on the impact of drive strength on power converter efficiency is also presented. In this work a gate-driver refers to both the level shifter and buffer chain and any other circuitry between the low voltage switch signal and the high voltage level shifted signal at the gate of the power switch.

### 4.1.1 Gate-driver strategies for switched-capacitor converters

High-side gate-drivers are often required for most of the power switches in switched-capacitor converters. This is needed for the power switches, that are not directly connected to ground. This requires level shifting of the gate signal, since the buffer chain, which drives the power switches are connected to the source of the power switch. Different strategies can be used to supply these high-side gate-drivers. Some general used strategies for supplying high-side gate-drivers are presented here.

**Bootstrap supply**

In Fig. 4.1 a high-side gate-driver consisting of a level shifter and a buffer chain can be seen. This gate-driver is supplied from a bootstrap circuit, consisting of a diode $D_{bst}$ connected to a low voltage supply avdd and a bootstrap capacitor $C_{bst}$ connected between the source of the switch $M_i$ and the supply of the buffer chain. The bootstrap supply strategy in Fig. 4.1 requires that the source of $M_i$ is connected to ground during one of the switching phases, through switch $M_{i+1}$. The supply of the buffer chain, which is the voltage between vddhi and vsshi using a bootstrap supply is then:

$$\text{vddhi} - \text{vsshi} = \text{avdd} - V_{f,Dbst} \tag{4.1}$$

where $V_f$ is the forward voltage of the bootstrap diode. The voltage drop on vddhi due to charge being delivered to the parasitic gate-capacitance of the switch $M_i$ is dependent

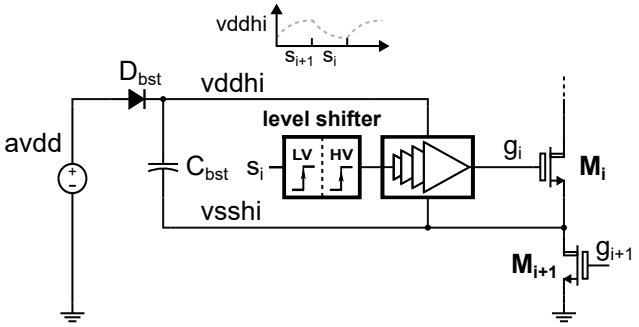



Figure 4.1: Gate-driver being supplied from a bootstrap supply.

on the size of the bootstrap capacitor $C_{bst}$ and the charge required to turn on the power switch:

$$\Delta\text{vddhi} = \frac{Q_{gg}}{C_{bst}} \tag{4.2}$$

where $Q_{gg}$ is the required charge to charge the gate capacitance of the switch and $C_{bst}$ is the bootstrap capacitor. The bootstrap supply circuit is simple to implement, but the requirement of the switch $M_i$ having to be connected to ground during a switching phase limits its usability. The average current requirement of the diode depends on the gate charge and the switching frequency:

$$I_{Dbst,avg} = \frac{n}{2} Q_{gg} f_{sw} \tag{4.3}$$

where $n$ is the number of phases, that the switch $M_i$ in Fig. 4.1 is connected to ground in a switching period. This sets the sizing requirements of the bootstrap diode to ensure that its current density is not exceeded. Naturally, the bootstrap maximum current should also be considered.

The voltage drop across the diode as it is conducting (while $M_i$ is connected to ground) is dependent on both the forward voltage of the diode and the voltage drop due to $C_{bst}$ being disharged:

$$\begin{aligned} V_{Dbst} &= \text{avdd} - (\text{vddhi} - \Delta\text{vddhi}) \\ &= \text{avdd} - \text{avdd} + V_{f,Dbst} + \frac{Q_{gg}}{C_{bst}} \\ &= V_{f,Dbst} + \frac{Q_{gg}}{C_{bst}} \end{aligned} \tag{4.4}$$

The average power loss of the bootstrap supply, which is dissipated in the bootstrap diode can then be expressed as:

$$\begin{aligned} P_{loss,bst} &= V_{Dbst} I_{Dbst,avg} \\ &= \frac{n}{2C_{bst}} (V_{f,Dbst} C_{bst} + Q_{gg}) Q_{gg} f_{sw} \end{aligned} \tag{4.5}$$

Note, that for $V_{f,Dbst} = 0\,\text{V}$, then (4.5) resembles the loss in a resistor when charging/discharging an RC circuit with a voltage source.

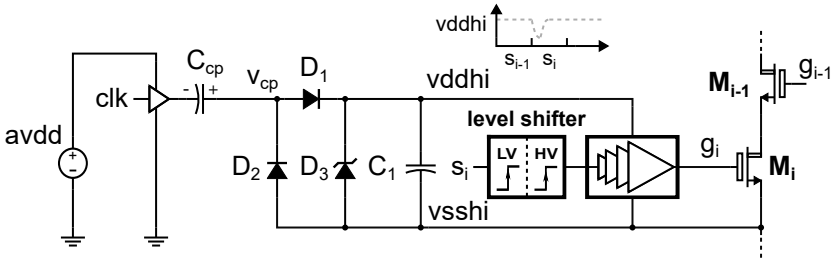



Figure 4.2: Gate-driver being supplied from a charge-pump supply.

**Charge pump supply**

For gate-drivers not connected to ground in any switching phase, a charge pump similar to Fig. 4.2 can be used as a supply. In this case, the charge pump capacitor $C_{cp}$ is driven from a buffer, which is driven by a clock signal and supplied from the ground-referred low voltage supply avdd. When the negative plate of $C_{cp}$ is connected to ground, $D_2$ is turned on, making the voltage at $v_{cp}$ equal to:

$$v_{cp}^0 = \text{vsshi} - V_{f,D2} \tag{4.6}$$

Where $v_{cp}^0$ indicates, when the clock signal driving the buffer is low. Whenever the clock signal goes high, the voltage at $v_{cp}$ is changed to:

$$v_{cp}^1 = \text{vsshi} + \text{avdd} - V_{f,D2} \tag{4.7}$$

Where $v_{cp}^1$ indicates the clock signal driving the buffer being high. When the vddhi voltage drops due to $C_1$ being discharged from supplying the buffer chain, $D_1$ turns on and charges vddhi to:

$$\text{vddhi} = v_{cp}^1 - V_{f,D1} \tag{4.8}$$

Inserting (4.7) into (4.8) and assuming identical diodes of $D_1$ and $D_2$ the gate-driver supply voltage becomes:

$$\text{vddhi} - \text{vsshi} = \text{avdd} - 2V_f \tag{4.9}$$

The zener diode $D_3$ is inserted to ensure, that the voltage across $C_1$ does not exceed the maximum voltage ratings of the buffer chain. This can happen in the case of a large swing on vsshi.

The expression in (4.7) is without considering the output resistance of the charge pump. In reality, the vddhi voltage depends on the switching frequency of the charge pump, the size of $C_{cp}$ and $C_1$, the buffer strength driving the negative plate of $C_{cp}$ and the required gate charged for driving the power switch. The clock frequency can be much lower than the switching frequency of the power converter as seen in the gate-drivers in [56], where a clock frequency 16 times lower than the power converter switching frequency was used to supply the gate-drivers. The voltage drop depends on the ratio between the switching frequency of the converter and the clock frequency of the charge-pump and the size of the decoupling capacitor $C_1$:

$$\Delta\text{vddhi} = \frac{f_{sw}}{f_{sw,cp}} \cdot \frac{Q_{gg}}{C_1} \tag{4.10}$$

where $f_{sw}$ is the power converter switching frequency and $f_{sw,cp}$ is the clock frequency of the charge pump. The equivalent output resistance of the charge pump in Fig. 4.2 is

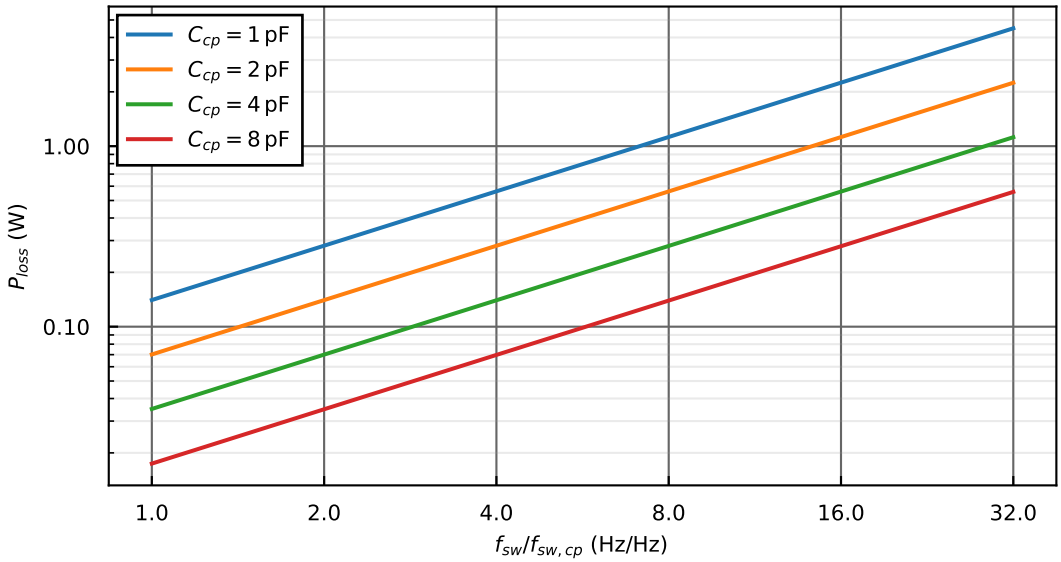



Figure 4.3: Calculated charge pump supply losses for various ratios between power converter and charge pump switching frequencies and $C_{cp}$ sizes.

assumed dominant by its slow-switching limit resistance and can be described as:

$$R_{out} \approx \frac{C_1}{C_1 + C_{cp}} \cdot \frac{1}{4 C_{cp} f_{sw,cp}} \tag{4.11}$$

The average power dissipated in the chargepump due to charge redistribution is therefore:

$$\begin{aligned} P_{loss,cp} &= R_{out} \cdot (I_{avg,gg})^2 \\ &= \frac{C_1}{4 C_{cp}(C_1 + C_{cp})} \frac{f_{sw}^2}{f_{sw,cp}} Q_{gg}^2 \end{aligned} \tag{4.12}$$

The calculated charge pump losses for a charge pump supplying a gate-driver with a gate charge of $Q_{gg} = 750\,\text{pC}$, and $C_1 = 10\,\text{nF}$ is shown in Fig. 4.3 for various ratios of $f_{sw}/f_{sw,cp}$ and for different sizes of $C_{cp}$. Notice, that the large value of $C_1$ is required, to ensure that $C_1$ is not completely discharged for higher $f_{sw}/f_{sw,cp}$ ratios. In Fig. 4.3 the penalty of choosing a lower clock frequency of the charge pump compared to the power converter frequency can clearly be seen. This is a trade-off between on-chip area and power consumption.

**Regulator supply**

Another approach is to generate the vddhi supply from a regulator connected to the input of the switched-capacitor converter as illustrated in Fig. 4.4. The complexity of the regulator depends on the application but often a simple shunt regulator can be used as seen in [17]. The benefit of using a shunt regulator is that it does not have negative feedback and therefore stability does not have to be considered. The downside is that the shunt regulator is not able to regulate to its reference voltage, whenever current is drawn from it. Instead the voltage at vddhi will drop in the beginning of the switching phase and then return to the desired regulator voltage as the required charge has been delivered to the

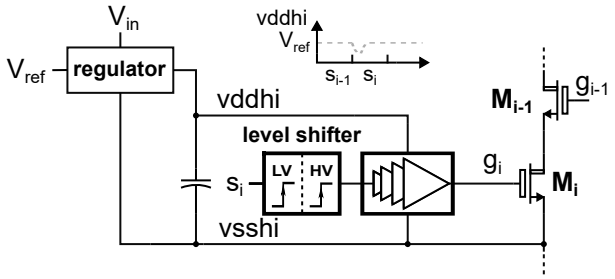



Figure 4.4: Gate-driver being supplied from a regulator supply.

gate of the power switch. Using a regulator the vddhi voltage is then able to be charged to the desired gate-source voltage of the power switch.

Connecting the regulator to the input of the power converter ensures, that the gate-drivers can be controlled as soon as $V_{in}$ exceeds the required voltage to drive the power switches. This can be useful during start-up. Connecting the regulator to the input voltage of the power converter does however also increase the power consumption of the gate-drivers since the ideal efficiency of the regulator is:

$$\eta_{eff} = \frac{P_{in}}{P_{in} + P_{loss}} = \frac{\text{vddhi} - \text{vsshi}}{V_{in} - \text{vsshi}} \tag{4.13}$$

Where the average input power $P_{in}$ is:

$$\begin{aligned} P_{in} &= (V_{in} - \text{vsshi}) \cdot I_{gg,avg} \\ &= (V_{in} - \text{vsshi}) Q_{gg} f_{sw} \end{aligned} \tag{4.14}$$

Rearranging (4.13) to isolate $P_{loss}$ we obtain:

$$P_{loss} = \eta_{eff} \cdot Q_{gg} f_{sw} (V_{in} - \text{vddhi}) \tag{4.15}$$

The increase in power consumption compared to the bootstrap or charge-pump method therefore depends on the placement of the power switch in the switched-capacitor topology and the input voltage of the power converter. The vsshi voltage is often connected to a flying capacitor and thereby an output voltage multiple fraction of the power converter input voltage, with the power switches closer to the input voltage having lower losses than switches closer to the ground of the power converter.

Using a regulator to supply the gate-driver also effects the minimum input voltage of the power converter, since $V_{in}$ − vsshi must be larger than the gate-source voltage for all gate-drivers. Depending on the conversion ratio of the switched-capacitor converter, this means that $V_{in}$ has to be a multiple of the required gate-source voltage:

$$V_{in,min} = N \cdot V_{gs} \tag{4.16}$$

### 4.1.2 Comparison on gate-driver methods

A summary of the key points of the three gate-driver supply strategies presented can be seen in Table 4.1. The main take-away is that each strategy has various advantages depending on the application and implementation. The bootstrap supply is limited in the sense, that it can only be used for switches that are connected to ground in at least one phase. It does however have the lowest complexity of implementation and power loss.

Table 4.1: Comparison between different gate-driver supplying strategies.

| | Supply voltage | $P_{loss}$ | Usability |
|---|---|---|---|
| Bootstrap | avdd $- V_f$ | $\frac{n}{2C_{bst}}(V_{f,Dbst}C_{bst} + Q_{gg})Q_{gg}f_{sw}$ | Limited |
| Charge pump | avdd $- 2V_f$ | $\frac{C_1}{4C_{cp}(C_1+C_{cp})}\frac{f_{sw}^2}{f_{sw,cp}}Q_{gg}^2$ | Anywhere |
| Regulator | avdd | $\eta_{eff} \cdot Q_{gg}f_{sw}(V_{in} -$ vddhi$)$ | Anywhere |

The charge pump is also simple in implementation and can be used for supplying any gate-driver. The regulator supply of the gate-driver has the highest design complexity but can also be used to supply any gate-driver in a switched-capacitor converter. The power loss depends on both the input voltage of the power converter and where the vsshi node is in the switched-capacitor converter. For switches located closer to the ground of the power converter, the conversion ratio from the input to the gate-driver supply is larger, which lowers the efficiency of the regulator.

Both the bootstrap and the charge pump supply relies on an external low voltage supply as an input voltage to generate the gate-driver supply. While, this low voltage supply is most definitely present in a switched-capacitor converter, the power loss associated with generating the low voltage supply should be incorporated for a more fair comparison between the gate-driver supply power loss strategies.

## 4.2 Discrete flying capacitor scaling optimization

This section describes the strategy of PCB area assignment for the discrete flying capacitors in highly-integrated switched-capacitor converters. The challenge is that for highly-integrated switched-capacitor converters, multiple parallel flying capacitors are often required to achieve the required performance both in regards of efficiency and maximum power. For a given PCB area, it is desired to know which flying capacitors size to increase first as to maximize its impact on efficiency. This problem differs from what was described in [73], where integrated capacitors were mostly assumed and the sizing of these is close to continuous. In [73] the optimum capacitor values for any topology is found by doing Lagrange multiplier optimization based on the assumption that the voltage rating of the capacitors is what dictates the capacitor area as well. For discrete capacitors, the capacitor area is dependent on the package type and size. The package types, and thereby area, come in discrete steps and while the voltage rating does influence the capacitance and area the designer would typically choose the package type with the highest capacitance density with the desired voltage rating. The question is then rather how many of these unit capacitors are to be put in parallel for best area utilization.

This section is a more detailed description of the work presented in the publications shown in Appendix C and expands on that work with more thorough explanations and design examples.

### 4.2.1 Deriving the optimal unit flying capacitor scaling

To optimize the energy-efficiency it is desired to minimize the slow-switching limit resistance ($R_{SSL}$) described in (3.26) for any given total flying capacitor PCB area for any switched-capacitor topology. For this Lagrange multiplier optimization [76] is used but with a different constraint function than what was used in [73]. The function to be min-

imized $f(\mathbf{k})$ and the constraint function $h(\mathbf{k})$, which describes the total flying capacitor PCB area. Here **k** refers to a vector of flying capacitor scalings indicating how many unit capacitors are placed in parallel for the external flying capacitors:

$$\mathbf{k} = [K_{c,1}, K_{c,2}, \cdots, K_{c,N_{cap}}]^T \tag{4.17}$$

The Lagrange multiplier optimization can be expressed as:

$$\mathcal{L}(\mathbf{k}, \lambda) = f(\mathbf{k}) + \lambda \cdot h(\mathbf{k}) \tag{4.18}$$

Where $f(\mathbf{k})$ and $h(\mathbf{k})$ can be described as:

$$\begin{aligned} f(\mathbf{k}) &= \sum_{i=1}^{N_{cap}} \frac{a_{c,i}^2}{K_{c,i} C_i'} \\ h(\mathbf{k}) &= \sum_{i=1}^{N_{cap}} K_{c,i} A_{c,i} - A_{cap} \end{aligned} \tag{4.19}$$

Where $a_{c,i}$ is the capacitor charge multiplier vector, $C_i'$ is the unit discrete flying capacitor vector, $K_{c,i}$ is the scaling parameter vector of the respective unit capacitor, $A_{c,i}$ is the unit capacitor PCB area and $A_{cap}$ is the designated total PCB area for flying capacitors. In reality, $K_{c,i}$ is a discrete number denoting how many unit capacitors, for each flying capacitor, are put in parallel. For the optimization $K_{c,i}$ is however considered continuous. Note, that the switching frequency is not included in (4.19). This is because it does not affect the minimization and is therefore emitted for simplicity. Inserting (4.19) into (4.18) we obtain:

$$\mathcal{L}(\mathbf{k}, \lambda) = \sum_{i=1}^{N_{cap}} \frac{a_{c,i}^2}{K_{c,i} C_i'} + \lambda \left( \sum_{i=1}^{N_{cap}} K_{c,i} A_{c,i} - A_{cap} \right) \tag{4.20}$$

Taking the partial derivative of $\mathcal{L}(\mathbf{k}, \lambda)$ with respect to $K_{c,i}$ leads to:

$$\frac{\partial \mathcal{L}}{\partial K_{c,i}} = -\frac{a_{c,i}^2}{K_{c,i}^2 C_i'} + \lambda A_{c,i} \tag{4.21}$$

Setting (4.21) equal to zero and isolating for $K_{c,i}$ then yields:

$$\begin{aligned} 0 &= -\frac{a_{c,i}^2}{K_{c,i}^2 C_i'} + \lambda A_{c,i} \\ K_{c,i} &= \frac{a_{c,i}}{\sqrt{\lambda A_{c,i} C_i'}} \end{aligned} \tag{4.22}$$

The derivative of $\mathcal{L}(\mathbf{k}, \lambda)$ with respect to $\lambda$ leads to:

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum_{i=1}^{N_{cap}} K_{c,i} A_{c,i} - A_{cap} \tag{4.23}$$

Setting (4.23) equal to zero and inserting the expression for $K_{c,i}$ obtained in (4.22) yields:

$$\sum_{i=1}^{N_{cap}} \frac{A_{c,i} a_{c,i}}{\sqrt{\lambda A_{c,i} C_i'}} - A_{cap} = 0 \tag{4.24}$$

Isolating for $\sqrt{\lambda}$:

$$\sqrt{\lambda} = \frac{1}{A_{cap}} \sum_{i=1}^{N_{cap}} \left( \frac{\sqrt{A_{c,i} a_{c,i}}}{\sqrt{C_i'}} \right) \tag{4.25}$$

Inserting (4.25) into (4.22) then yields the optimized unit capacitor scaling vector $K_{c,i}$:

$$K_{c,i} = \frac{A_{cap} \cdot a_{c,i}}{\sqrt{A_{c,i} \cdot C_i'} \cdot \sum_{j=1}^{N_{cap}} \left( \frac{\sqrt{A_{c,j}} a_{c,j}}{\sqrt{C_j'}} \right)} \tag{4.26}$$

The expression in (4.26) is the floating point optimized unit capacitor scaling vector. In reality the scaling vector consists of integers. The used scaling vector is therefore the expression in (4.26) rounded down to the nearest integer, which is denoted by $\lfloor K_{c,i} \rfloor$. The optimized flying capacitor values can then be expressed as:

$$C_i = C_i^{'} \cdot \lfloor K_{c,i} \rfloor \tag{4.27}$$

where $C_i$ denote the total capacitor value for each flying capacitor in the topology. Note, that the expression in (4.26) is topology independent and can be applied for any switched-capacitor converter topology making it very useful when assigning the adequate PCB area for the highly-integrated power converter.

The derived capacitor scaling does not take into account the additional benefit of lowering the effective series resistance (ESR) of the flying capacitors.

### 4.2.2 Example of optimal design of discrete flying capacitors in highly-integrated switched-capacitor converters

Table 4.2: Specifications for capacitor scaling example

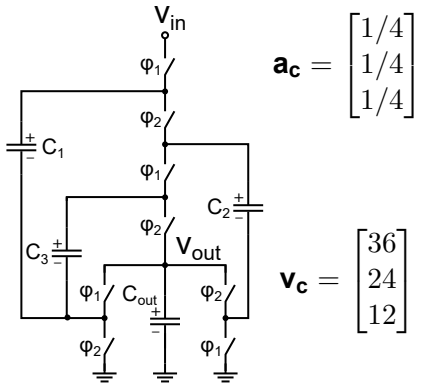
| Input voltage | Conversion ratio | MLCC package size |
|---|---|---|
| 48 V | 4 to 1 | 0805 (2012M) |

To clarify how the discrete flying capacitor design can depend on the topology an example of two 4:1 switched-capacitor topologies with discrete flying capacitors and their respective capacitor scaling is presented. The specifications for both design can be seen in Table 4.2. The two chosen topologies are the 4:1 Ladder topology and the 4:1 Dickson topology.

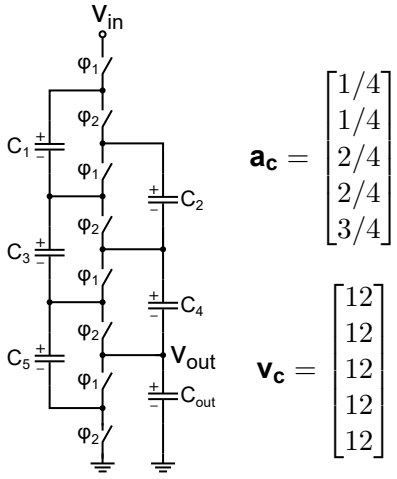
The 4:1 ladder topology requires 5 flying capacitors, which all have a maximum blocking voltage of 12 V for a 48 V input voltage. The 4:1 Dickson topology requires only 3 flying capacitors, but their blocking voltages are 36 V, 24 V and 12 V for $C_1$, $C_2$ and $C_3$ respectively. The two topologies, their capacitor charge flow multiplier vectors and the maximum blocking voltages can be seen in Fig. 4.5.

Table 4.3: Discrete capacitors used for 4:1 Dickson and 4:1 Ladder topology in optimal flying capacitor scaling example.

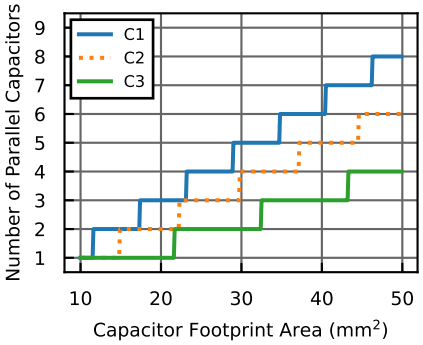
| Flying Capacitor | Capacitance (DC bias derated) [$\mu$F] | Rated voltage [V] | Size [mm$^2$] | Vendor | Part# |
|---|---|---|---|---|---|
| | | **4:1 Dickson** | | | |
| $\mathbf{C_1}$ | 10 (0.77) | 50 | 2.5 | Murata | GRM21BR61H106ME43K |
| $\mathbf{C_2}$ | 10 (1.27) | 36 | 2.5 | Murata | GRM21BR6YA106KE43K |
| $\mathbf{C_3}$ | 10 (2.69) | 25 | 2.5 | Murata | GRM21BC71E106KE11 |
| | | **4:1 Ladder** | | | |
| $\mathbf{C_1 - C_5}$ | 10 (2.69) | 25 | 2.5 | Murata | GRM21BC71E106KE11 |



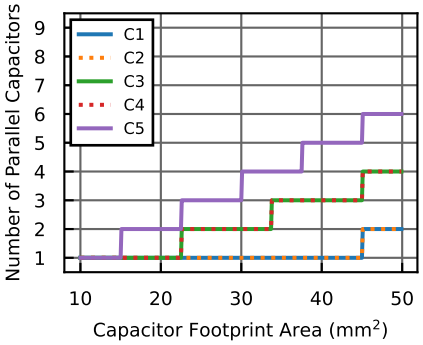

(a) 4:1 Dickson topology.




(b) 4:1 Ladder topology.



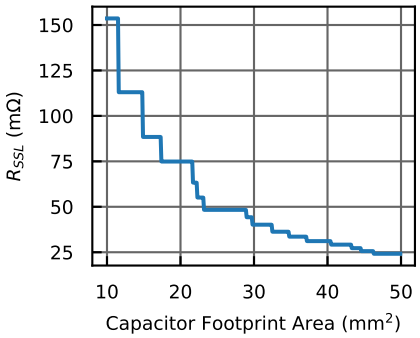

(c) Optimal flying capacitor scaling for a specific capacitor footprint area, in a 4:1 Dickson converter



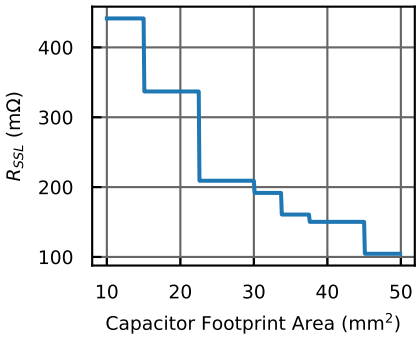

(d) Optimal flying capacitor scaling for a specific capacitor footprint area, in a 4:1 Ladder converter

Figure 4.5: The 4:1 Ladder and Dickson topologies with their capacitor charge multiplier vectors ($\mathbf{a_c}$), maximum blocking voltages ($\mathbf{v_c}$) and their respective optimal flying capacitor scalings for different capacitor footprint areas.

The chosen discrete capacitors for each topology together with their rated voltages and DC biased capacitance can be seen in Table 4.3. Here it can be seen, that since the 4:1 Dickson topology has different voltage ratings for the three flying capacitors, three




(a) $R_{SSL}$ of the 4:1 Dickson converter when increasing capacitor footprint PCB area, with optimal capacitor scaling.




(b) $R_{SSL}$ of the 4:1 Ladder converter when increasing capacitor footprint PCB area, with optimal capacitor scaling.

Figure 4.6: Comparison between $R_{SSL}$ for the 4:1 Dickson and 4:1 Ladder converter with optimized discrete capacitor scalings for a switching frequency of $f_{sw} = 1$ MHz.

different MLC capacitors are used. While they are all 10 µF capacitors, their DC bias derated voltages can be seen to be significantly lower. For the 4:1 Ladder topology the same MLC capacitor can be used for all five flying capacitors. For the calculation of the optimal unit flying capacitor scaling, the DC bias derated capacitance is used.

In Fig. 4.5 the calculated optimal unit flying capacitor scalings can be seen for both the 4:1 Dickson and 4:1 Ladder topology for a capacitor PCB footprint area from 10 mm$^2$-50 mm$^2$. When comparing Fig. 4.5c and Fig. 4.5d it can be seen how the capacitor scaling is different for the two topologies.

In the 4:1 Dickson topology the $C_1$ flying capacitor, which sees the highest voltage, should be prioritized when scaling the flying capacitors. In the case of the 4:1 Ladder topology, the capacitors all have the same voltage stress, but $C_5$ should be prioritized, since it is being charged and discharged the most during each switching period. The figures in Fig. 4.5c and Fig. 4.5d are very useful, when a deciding on how large a PCB area to assign for the power converter.

In Fig. 4.6 the calculated $R_{SSL}$ for the 4:1 Dickson and 4:1 Ladder converter can be seen as a function of the capacitor footprint PCB area for a switching frequency of $f_{sw} = 1$ MHz. Here the optimal scalings have been used and it is now possible to compare the optimized $R_{SSL}$ between the two topologies. It can be seen from Fig. 4.6 that the $R_{SSL}$ of the 4:1 Dickson is always more than half that of the 4:1 Ladder converter for the same PCB area. That fits well with the general understanding of the $K_{SSL}$ metrics comparison presented in [73]. Note that for both cases the benefit of increasing the capacitor footprint area on the $R_{SSL}$ starts to diminish after 22.5 mm$^2$. For a full comparison on topology selection the $R_{FSL}$ also needs to be taken into account together with other implementation specific advantages and disadvantages.

The presented example shows that the applicability of the presented capacitor scaling factor in both the design phase and in topology selection. The example is simplified for clarity by locking the used MLC capacitor package sizes, but the capacitor scaling expression in (4.26) does enable the designer of having different package sizes ($A_{c,i}$) for each flying capacitor. The optimal capacitor scaling presented is important for ensuring a high power density for the highly-integrated power converters, since the discrete ca-

pacitors often limits the maximum output power and sets the overall volume of the power converter.

## 4.3 Integrated power stage optimization

This section describes the optimal sizing of the integrated power stage for an assigned integrated chip area and switching frequency for highly-integrated switched-capacitor converters. This optimal sizing has been tackled earlier by both [73] and [77], but both works focus on fully-integrated, low voltage solutions. In the case of [73] the gate-driving losses are neglected, since usually in fully-integrated and low voltage applications they are not relevant compared to the total losses. In [77] the switching losses from charging and discharging the drain-source capacitance is neglected, because these losses are also usually not dominant in low voltage fully-integrated switched-capacitor converters. Both works describe the bottom-plate losses of the flying capacitors, since they assume integrated capacitances.

Even though [77] does describe the gate-driver losses, it is assuming that buffer-chains in the gate-drivers can be driven directly from the power converter input voltage. While this is often the case for low voltage switched-capacitor converters, it underestimates the gate-driver losses in cases where the power converter input voltage far exceeds the voltage ratings of the power switches used. Therefore, to enable optimal design of the integrated power stage in the case of high-voltage switched-capacitor converters, the power losses described in Section 3.2 are reformulated as a function of the total integrated power switch area and switching frequency. Since the focus of this research project is highly-integrated switched-capacitor converters, the bottom plate capacitor losses and other parasitic capacitances due to PCB routing are not included, since the use of discrete flying capacitors make these losses negligible.

This section provides a more detailed description of the work presented in the publications shown in Appendix C and expands on that work with a more generalized optimization of the integrated power stage that works for any topology and provides a more in-depth design example using the proposed optimization method.

### 4.3.1 Reformulating switched-capacitor converter power losses

The fast-switching limit resistance, $R_{FSL}$ described in section 3.1.2 models the conduction losses of the power switches and is a function of the effective on-state resistance of the power switches ($R_{ds}$). The $R_{FSL}$ for a two-phase switched-capacitor converter with a duty cycle of 50 % is expressed as:

$$R_{FSL} = 2\left(\sum_i R_{ds,i} a_{r,i}^2\right) \tag{4.28}$$

The on-state resistance $R_{ds}$ has a inverse linear dependency on the area of the power switch. Assigning the power switch resistance $R_{ds}$ dependent on the switch charge flow multiplier $a_r$, we can describe the individual switch as resistance as function of the total assigned integrated power switch area $A_{sw}$:

$$R_{ds,i} = \frac{K_{A,i}}{A_{sw} \cdot \frac{a_{r,i}}{\sum_k (a_{r,k})}} \tag{4.29}$$

Where $K_A$ is the area specific on-state resistance for the power switch used, which is often obtained from process documentation or can easily be achieved by characterization of the power switch used by simulation. This parameter is fabrication process dependent

and highly dependent on the maximum voltage rating as well. The issue with (4.29) is that for topologies with power switches with various voltage requirements the area specific on-state resistance $K_A$ can lead to inefficient sizing of the switches. To take this into account, assigning the power switch area such that this difference in $K_A$ is taken into account can be expressed as:

$$A_{sw,i}^{'} = \frac{K_{A,i} \cdot A_{sw} \cdot a_{r,i}}{\sum_k (a_{r,k} \cdot K_{A,k})} \tag{4.30}$$

Where $A_{sw,i}^{'}$ is the area of each power switch. The re-scaled $R_{ds,i}$ can then be expressed as:

$$\begin{aligned} R_{ds,i} &= \frac{K_{A,i}}{A_{sw,i}^{'}} \\ &= \frac{\sum_k (a_{r,k} \cdot K_{A,k})}{A_{sw} \cdot a_{r,i}} \end{aligned} \tag{4.31}$$

Inserting (4.31) into (4.28) we obtain:

$$\begin{aligned} R_{FSL} &= 2 \sum_i \left( \frac{a_{r,i}^2 \sum_k (a_{r,k} \cdot K_{A,k})}{A_{sw} \cdot a_{r,i}} \right) \\ &= 2 \sum_i \left( \frac{a_{r,i} \sum_k (a_{r,k} \cdot K_{A,k})}{A_{sw}} \right) \end{aligned} \tag{4.32}$$

The power loss due to the equivalent output resistance is therefore dependent on both switching frequency, from the $R_{SSL}$, and the total integrated power switch area due to the $R_{FSL}$:

$$\begin{aligned} P_{rout} &= I_{out}^2 \cdot R_{out} \\ &= I_{out}^2 \cdot \sqrt{R_{SSL}^2(f_{sw}) + R_{FSL}^2(A_{sw})} \end{aligned} \tag{4.33}$$

The switching losses of the integrated power switches occur since the total capacitance seen from the drain of the power switch is charged and recharged during each switching period. The switching losses for a single power switch was expressed in (3.42) and is rewritten here for a two-phase converter for convenience:

$$P_{sw} = V_{ds} Q_{oss} f_{sw} \tag{4.34}$$

Where $V_{ds}$ is the drain-source voltage of the power switch and $Q_{oss}$ is the required charge to charge and discharge the total output capacitance of the power switch. The drain-source charge $Q_{oss}$ can be rewritten as:

$$Q_{oss} = C_{oss} \cdot V_{ds} \tag{4.35}$$

Where $C_{oss}$ is the equivalent linear capacitance seen between drain and source of the power switch. This capacitance is dependent on the area and type of power switch used. We therefore rewrite $C_{oss}$ as:

$$\begin{aligned} C_{oss,i} &= \beta_{coss,i} \cdot A_{sw,i}^{'} \\ &= \beta_{coss,i} \cdot \frac{K_{A,i} \cdot A_{sw} \cdot a_{r,i}}{\sum_k (a_{r,k} \cdot K_{A,k})} \end{aligned} \tag{4.36}$$

where $\beta_{coss}$ is the area specific drain-source capacitance for the used power switch. This parameter is dependent on the maximum voltage rating of the device. Combining (4.34), (4.35) and (4.36) the total switching loss from all power switches can then be expressed as:

$$P_{sw} = f_{sw} \cdot \sum_i \left( V_{ds,i}^2 \cdot \beta_{coss,i} \cdot \frac{K_{A,i} \cdot A_{sw} \cdot a_{r,i}}{\sum_k (a_{r,k} \cdot K_{A,k})} \right) \tag{4.37}$$

Similarly the power losses from charging and discharging the gate capacitance of a power switch described in (3.46) can be reformulated as an expression of the total power switch area $A_{sw}$. Equation (3.46) for a two-phase converter is rewritten here for convenience:

$$P_{gd} = \frac{1}{\alpha} V_{DD} Q_{gg} f_{sw} \tag{4.38}$$

where $Q_{gg}$ is the required charge to charge/discharge the power switch total gate capacitance to the required gate-source voltage, $V_{gs}$. $V_{DD}$ is the supply of the gate-driver and is implementation dependent and $\alpha$ is the gate-driver charge efficiency. $Q_{gg}$ can be expressed as:

$$Q_{gg} = C_{gg} \cdot V_{gs} \tag{4.39}$$

The power switch gate-capacitance is dependent on the area of the power switch. Using the same sizing factor $A_{sw}^{'}$ as earlier the gate-capacitance of any power switch in a topology can be expressed as:

$$\begin{aligned} C_{gg,i} &= \beta_{cgg,i} \cdot A_{sw,i}^{'} \\ &= \beta_{cgg,i} \cdot \frac{K_{A,i} \cdot A_{sw} \cdot a_{r,i}}{\sum_k (a_{r,k} \cdot K_{A,k})} \end{aligned} \tag{4.40}$$

Using this we can express the total power loss due to charging/discharging the gate-capacitance of all power switches as:

$$P_{gd} = \frac{f_{sw} V_{gs}}{\alpha} \sum_i^{N_{switches}} \left( V_{DD,i} \cdot \beta_{cgg,i} \cdot \frac{K_{A,i} \cdot A_{sw} \cdot a_{r,i}}{\sum_k (a_{r,k} \cdot K_{A,k})} \right) \tag{4.41}$$

Note, that the gate-driver supply here is noted as a vector. This is to generalize the expression in (4.41), since for some implementations of the gate-drivers the supply voltage can vary depending on the power switch. The equivalent series resistance (ESR) and inductance (ESL) of the discrete capacitors also contribute to additional power losses. These losses are usually included in the effective output impedance, $R_{out}$, as a part of the $R_{FSL}$ losses [75]. The losses from both the ESR and ESL of the capacitors depend on the optimal capacitor scalings described in section 4.2. The total equivalent output resistance due to the ESR of the flying capacitors can be expressed as:

$$R_{ESR} = 2 \cdot \sum_i^{N_{caps}} \left( a_{c,i}^2 \cdot \frac{ESR_i}{\lfloor K_{c,i} \rfloor} \right) \tag{4.42}$$

The capacitor scaling factor $K_C$ is included here, since adding multiple capacitors in parallel reduces the ESR and ESL. Similarly, the total equivalent output resistance due to the ESL can be expressed as:

$$R_{ESL} = 4 \cdot \sum_i^{N_{caps}} \left( a_{c,i}^2 \cdot 2\pi f_{sw} \cdot \frac{ESL_i}{\lfloor K_{c,i} \rfloor} \right) \tag{4.43}$$

Table 4.4: The impact of increasing input voltage, power switch area, switching frequency and output load on the power loss components in highly-integrated switched-capacitor converters.

| | $\uparrow V_{in}$ | $\uparrow A_{sw}$ | $\uparrow f_{sw}$ | $\uparrow i_{out}$ |
|---|---|---|---|---|
| $P_{rout}$ | $\uparrow$ | $\downarrow\downarrow$ | $\downarrow\downarrow$ | $\uparrow\uparrow$ |
| $P_{sw}$ | $\uparrow\uparrow$ | $\uparrow\uparrow$ | $\uparrow\uparrow$ | -- |
| $P_{gd}$ | $\uparrow$ | $\uparrow\uparrow$ | $\uparrow\uparrow$ | -- |

Note, that while neither (4.42) nor (4.43) are dependent on the integrated switch area, they are easy to incorporate to help give a more accurate estimate on the expected power loss in the switched-capacitor converter. Furthermore, the $R_{ESL}$ is dependent on switching frequency and thereby gives information regarding the choice of power converter switching frequency. The total series output resistance, $R_{out}$ of a switched-capacitor converter including $R_{ESR}$ and $R_{ESL}$ can be approximated as:

$$R_{out} = \sqrt{R_{SSL}^2 + (R_{FSL} + R_{ESR} + R_{ESL})^2} \tag{4.44}$$

The total power loss in a highly-integrated switched-capacitor converter can then be expressed as:

$$P_{loss} = P_{rout} + P_{sw} + P_{gd} \tag{4.45}$$

The impact of increasing $V_{in}$, $A_{sw}$ and $f_{sw}$ on the power losses is summarized in Table 4.4. An increase in power losses is indicated by an $\uparrow$-symbol. In Table 4.4 two arrows means a direct impact, while a single arrow indicates that the power loss is impacted by second order effects. For the $P_{gd}$ the impact from increasing the converter input voltage depends on the implementation as described in section 4.1. While the $P_{rout}$ does not directly depend on the input voltage, the area specific on-state resistance of the power switches does. Additionally, the DC bias derated capacitance values of the discrete flying capacitors also depend on the input voltage.

From Table 4.4 it can be seen, that an optimum switching frequency and total power switch area for a given output load current must exist, that achieves the lowest total power losses.

### 4.3.2 Example of optimal design of integrated power stage for a 4:1 Ladder topology

Table 4.5: Specifications for integrated power stage design example

| Input voltage | Conversion ratio | Topology | Load current |
|---|---|---|---|
| 48 V | 4 to 1 | Ladder | 1 A |

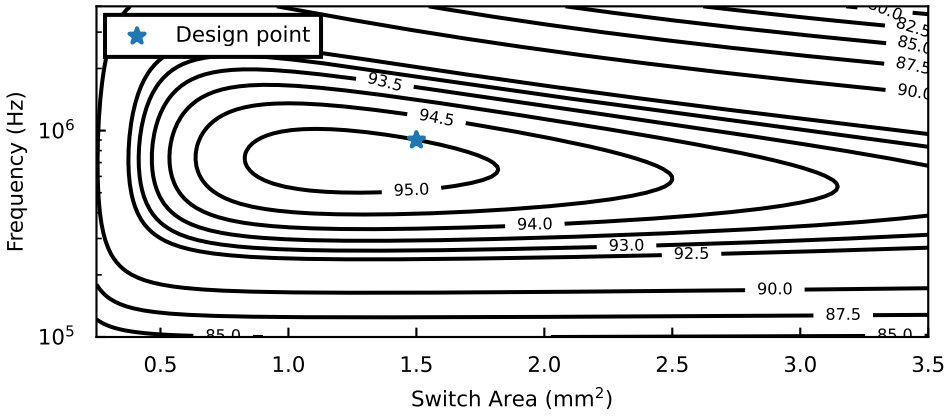
To clarify how the reformulated power losses in section 4.3.1 can be used to design an integrated power stage, an example of the design of a 4:1 Ladder converter is shown. The discrete flying capacitors are sized based on the example from section 4.2.2 with a total PCB area of $A_{cap} = 22.5\,\text{mm}^2$ and using the same discrete MLC capacitors. This leads to an optimal capacitor scaling vector:

$$\lfloor \mathbf{K_c} \rfloor = [1, 1, 2, 2, 3]^T \tag{4.46}$$

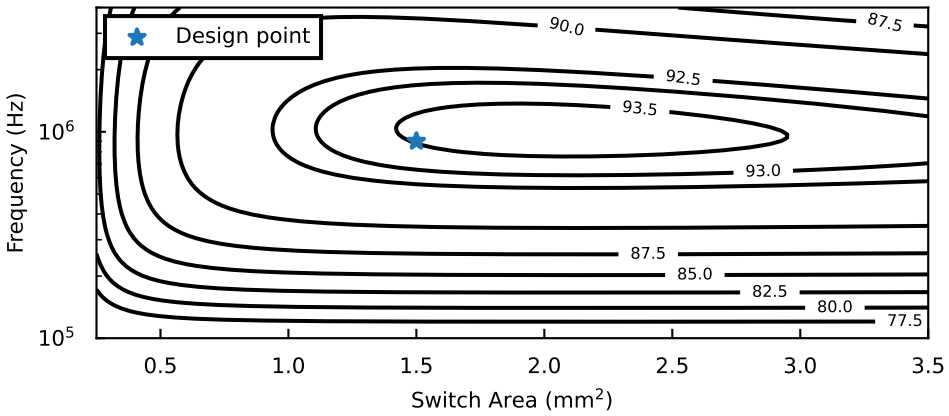
The specifications for the designed switched-capacitor converter can be seen in Table 4.5. The output load current indicates the load condition where we want to minimize the power stage losses. The gate-drivers implementation assumed is the floating gate-driver with a shunt regulator supplied from the input voltage for all gate-drivers discussed in section

Table 4.6: Power switches used for the 4:1 Ladder integrated power stage example and their extracted characterized values.

| **Power switch** | **Rated voltage** [V] | $\mathbf{K_A}$ [mΩmm$^2$] | $\beta_{\mathbf{cgg}}$ [nF/mm$^2$] | $\beta_{\mathbf{coss}}$ [nF/mm$^2$] |
|---|---|---|---|---|
| $\mathbf{M_1}$ | 60 | 75 | 8.8 | 2.6 |
| $\mathbf{M_2 - M_8}$ | 20 | 12 | 7 | 1.35 |




(a) Contour plot of the estimated efficiency of the 4:1 Ladder switched-capacitor converter for 1 A load current for different switching frequencies and total power switch area.




(b) Contour plot of the estimated efficiency of the 4:1 Ladder switched-capacitor converter for 2 A load current for different switching frequencies and total power switch area.

Figure 4.7: Efficiency curves for different switch areas and switching frequencies for the 4:1 Ladder integrated power stage design example.

Table 4.7: Areas and resulting power switch resistances and parasitic capacitances per switch for the 4:1 Ladder integrated power stage design example.

| **Power switch** | **Rated voltage** [V] | **Area** [mm$^2$] | $\mathbf{R_{on}}$ [m$\Omega$] | $\mathbf{C_{gg}}$ [pF] | $\mathbf{C_{oss}}$ [pF] |
|---|---|---|---|---|---|
| $\mathbf{M_1}$ | 60 | 0.543 | 138 | 416 | 123 |
| $\mathbf{M_2 - M_6}$ | 20 | 0.087 | 138 | 115 | 22.3 |
| $\mathbf{M_7 - M_8}$ | 20 | 0.261 | 46 | 344 | 66.8 |

4.1. This results in a gate-driver supply vector ($\mathbf{V_{DD}}$) equal to:

$$\mathbf{V_{DD}} = [12, 12, 24, 24, 36, 36, 48, 48]^T \tag{4.47}$$

Even though the Ladder topology has equal voltage ratings for all power switches ($V_r = V_{in}/N$) it is decided in this example to use a 60 V device for the top switch. This is to ensure that the power converter can tolerate the full input voltage and does not get damaged during start-up. The area specific on-state resistance, area specific gate-source capacitance and area specific drain-source capacitance for the chosen power switches can be seen in Table 4.6. The values in Table 4.6 are derived based on extracted values from simulation results for the power switches. Using the specifications in Table 4.5 and the extracted values from Table 4.6 together with the reformulated power loss equations from section 4.3.1 the power loss as a function of both switching frequency and total power switch area can be calculated.

The calculated efficiency for both a 1 A and 2 A load current can be seen as a contour plot in Fig. 4.7. For the 1 A output load condition in Fig. 4.7a it can be seen that the maximum efficiency can be achieved around a total switch area of 1.25 mm$^2$ and a switching frequency of 700 kHz. To illustrate how the load current affects the optimal design point, the efficiency for a load current of 2 A can be seen in Fig. 4.7b. To achieve the highest efficiency in this design point, the total switch area should be 2 mm$^2$ and the switching frequency should be increased to around 1 MHz. In general, as we increase the output

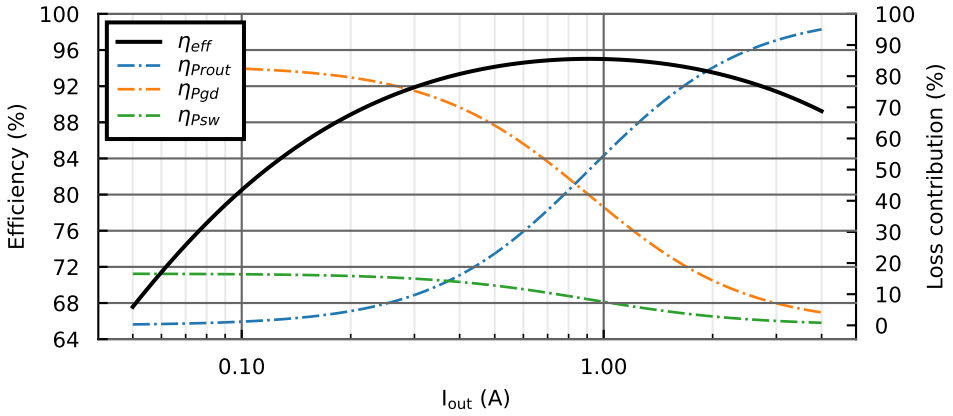



Figure 4.8: Estimated efficiency ($\eta_{eff}$) and the power loss contribution in percent for $P_{rout}$, $P_{gd}$ and $P_{sw}$ for different load currents for the 4:1 Ladder integrated power stage design example with $A_{sw} = 1.5$ mm$^2$ and $f_{sw} = 1$ MHz.

load, the $P_{rout}$ losses start to dominate, which means that the benefit of increasing both switch area and switching frequency on reducing the $P_{rout}$ losses outweighs the increase in switching losses and gate-driver losses. This is shown by the optimum moving towards to upper right of the contour plot, when increasing the load current. For this example a design point between the two load conditions is chosen.

In this example a switch area of 1.5 mm$^2$ and a switching frequency of 900 kHz is chosen based on the results of the contour plot in Fig. 4.7. The resulting switch resistances, switch areas and switch capacitances can be seen in Table 4.7. Note, that the size of $M_1$ is 6.25 times bigger than $M_2 - M_6$, since $K_{A,M1}/K_{A,M2-6} = 6.25$, similarly $M_7 - M_8$ are 3 times larger than $M_2 - M_6$, since the charge multiplier for $M_7$ and $M_8$ is 3 times larger. The calculated estimated power converter efficiency as a function of the output load for the design example can be seen in Fig. 4.8 together with the different power loss contributions in percentage of the total power loss. Here it can be seen that the maximum efficiency is achieved at 1 A and that the efficiency drops below 90 % at around an output load current of 4 A. Furthermore, it can be seen that for lower loads, especially the gate-driver losses are dominant in the low load condition and that the transition from the $P_{rout}$ losses becoming dominant happens around the peak efficiency point.

The presented example shows how the reformulated power losses as a function of the total integrated power switch area and the switching frequency can lead to initial sizing of the integrated power stage. While the example was shown for a 4:1 Ladder topology, the methodology is general and can be used for any switched-capacitor converter topology. After the initial sizing further high accuracy simulations should be used to verify the expected calculated performance.

## 4.4 Implementation of a highly-integrated, 48 V-12 V switched-capacitor converter

To verify the design methodology a 48 V-12 V highly-integrated switched-capacitor converter has been implemented in a 180 nm SOI-BCD process. The switched-capacitor converter has been designed for a 2 A output current using the proposed methodology. The integrated chip consists of an integrated power stage using high-voltage devices, integrated gate-drivers using shunt regulators to generate the local level shifter and buffer chain supplies, a digital clock controller with a 1-2 MHz ring-oscillator and a two-phase non-overlapping clock generator with a 1-bit adjustable dead-time. The power converter has been designed with focus on maximizing power density and peak efficiency by using the design methodologies for the integrated power-stage and flying capacitors described in this chapter. A schematic of the proposed power converter can be seen in Fig. 4.9.

This section describes the design considerations of the integrated circuits and verification measurements of the highly-integrated switched-capacitor converter. It is a more detailed description of the work presented in the publications shown in Appendix C and expands on that work with a more detailed description of some of auxiliary integrated circuits implemented and their performance.

### 4.4.1 Gate-driver

An overview of the gate-driver used for driving the integrated power stage can be seen in Fig. 4.10. The gate-driver consists for a high-voltage level shifter from the digital 5 V supply to the floating high-voltage level shifter supply ($\text{vddhi}_{\text{ls}}$), two channel supplies, which are generated by two identical shunt regulators, a domain interface level shifter to ensure no latch-up glitches between the two high-voltage floating supplies and a buffer chain, which drives the power switch. The shunt regulator used to generate $\text{vddhi}_{\text{ls}}$ and

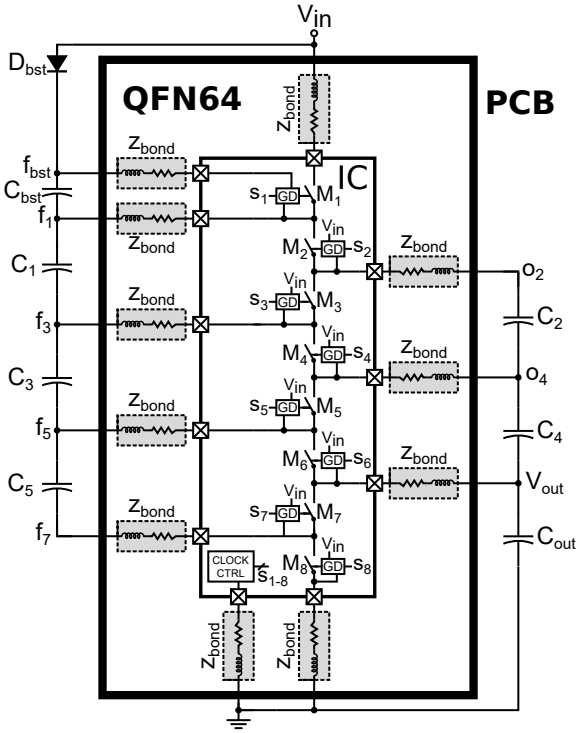



Figure 4.9: Schematic of implemented highly-integrated 4:1 ladder switched-capacitor converter with an integrated power stage, gate-drivers and clock controller and external flying capacitors.

$\text{vddhi}_{bc}$ can be seen in Fig. 4.11. The shunt regulator pass device $M_{pass}$ is sized such, that the voltage drop on $\text{vddhi}_{ls}$ does not cause glitches in the level shifter. The reference of the shunt regulator is generated by a zener diode ($D_1$) and a bipolar device ($Q_1$), which is diode-connected to generate a 6 V reference voltage. $M_1$ is a depleted 60 V device, which generates a current source together with $R_1$. The output voltage of the shunt regulator under no-load condition is:

$$vddhi_{ls} = V_{ref} - V_{th,Mpass} \tag{4.48}$$

Decoupling capacitors are placed at both the reference voltage node and the output of the shunt regulator to deal with transient load currents and switching noise as vsshi is a

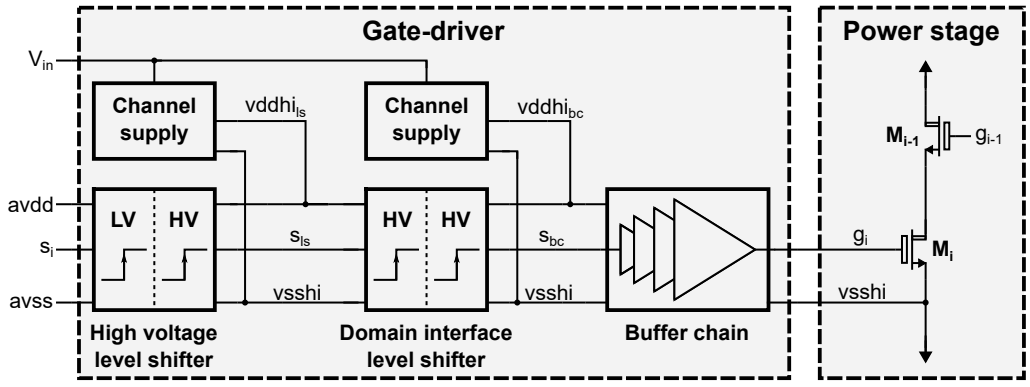



Figure 4.10: Block level view of the floating gate-drivers used to drive the power switches.

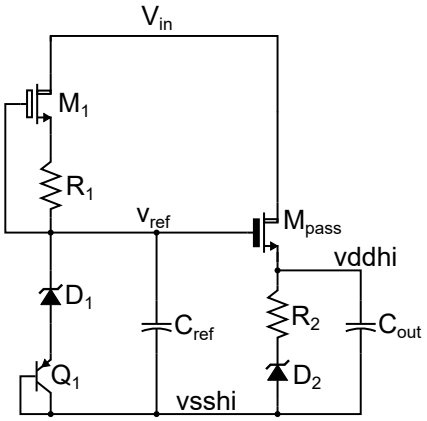



Figure 4.11: Shunt regulator used to generate the $vddhi_{ls}$ and $vddhi_{bc}$ supplies in the floating gate-driver.

switching node for the switched-capacitor converter for all gate-drivers driving odd numbered power switches ($M_1$, $M_3$, $M_5$ and $M_7$). A zener diode is connected at the output of the shunt regulator (vddhi) as over-voltage protection for the 5 V supply, such that it does not damage the 5 V devices used for the level shifter and buffer chain.

The level shifter can be seen in Fig. 4.12. It consists of a logic block, where either pulse-trigger mode or level-trigger mode can be chosen, which is controlled by the lvl_trig bit. In level-trigger mode, the input clock $s_i$ is simply passed through a non-overlapping clock generator as the set and reset signal for the level shifter. In pulse-trigger mode a short pulse at the rising clock edge is used as the set signal and a pulse at the falling edge is used as the reset signal. When operating in level-trigger mode the 60 V $M_1$ and $M_2$ transistors are constantly drawing a quiescent current, which leads to a large static power consumption of the level shifter. The pulse-trigger mode only draws current for a short duration, until the level shifter has made a decision. The Schottkey diodes are used to ensure that the gate-source voltages of the 5 V PMOS transistors $M_3$, $M_4$, $M_5$, $M_6$, $M_9$ and $M_{10}$ do node exceed their maximum voltage rating. Resistors $R_1$, $R_2$, $R_3$ and $R_4$ are inserted to ensure no floating voltage nets, since neither $vddhi_{ls}$ or vsshi are well defined

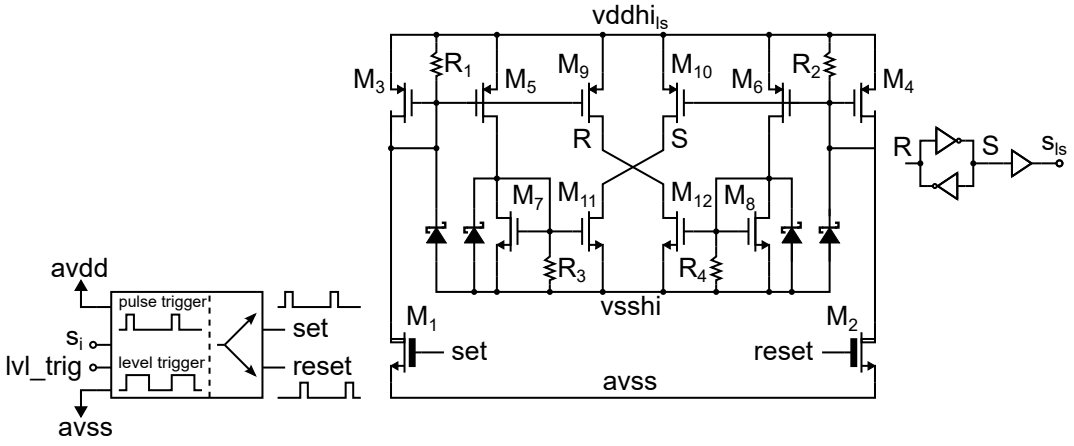



Figure 4.12: Schematic of the level shifter used to interface between the digital 5 V domain (avdd) to the channel supply domain $vddhi_{ls}$ for the floating gate-drivers.

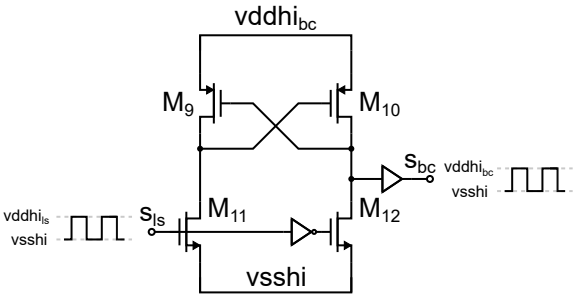



Figure 4.13: Domain interface level shifter to interface between the two channel supply domains in the gate-driver.

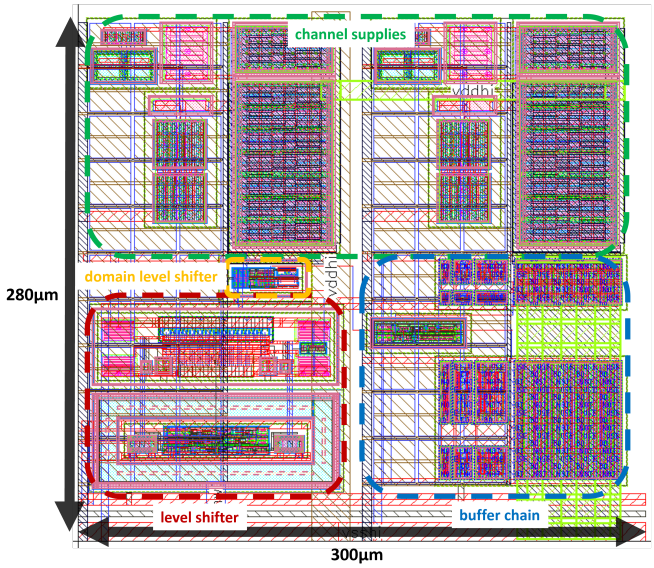



Figure 4.14: Layout of the integrated gate-driver used for driving the power switches.

during start-up, which can cause unwanted glitches at the output of the level shifter.

The domain interface level shifter can be seen in Fig. 4.13. As mentioned the domain interface level shifter is required, since we cannot ensure that the two floating supplies from the shunt regulators have the exact same voltage, which can cause glitches.

The gate-driver layout can be seen in Fig. 4.14. The total area of the gate-driver is 0.084 mm$^2$. The same gate-driver is used for driving all power switches, but two in parallel are used to drive $M_7$ and $M_8$. This corresponds to a total of 10 gate-drivers, which then consume 0.84 mm$^2$ of the total 10 mm$^2$ chip area.

### 4.4.2 Clock controller

The an overview of the implemented clock controller can be seen in Fig. 4.15. The clock controller consists of a 2 MHz current-starved ring oscillator and a non-overlapping clock generator with dead-time control. A multiplexer is used to choose between an external clock and the internal and multiplexers are also used to enable the supply of the clock phases ($\varphi_1$, $\varphi_2$) directly from an external source.

The 2 MHz current-starved ring oscillator can be seen in Fig. 4.16. The 3-bit $\text{freq}_{\text{ctrl}}$ signal adjusts the frequency of the ring oscillator. The most significant bit controls a clock divider,

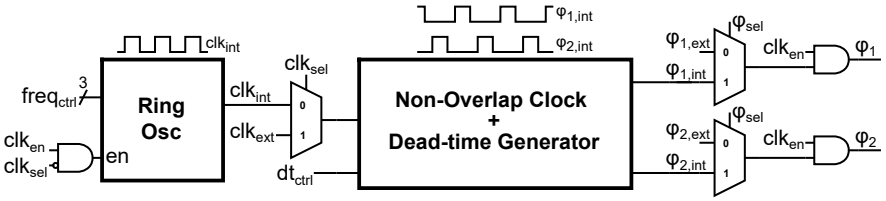



Figure 4.15: Overview of the implemented clock controller consisting of a 2 MHz ring oscillator and a non-overlapping clock generator with dead-time control.

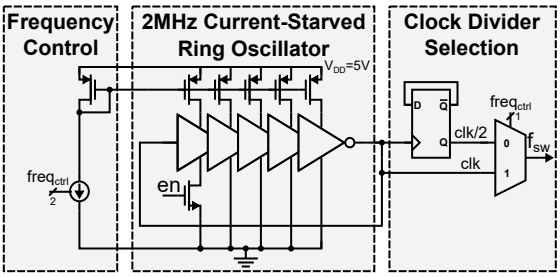



Figure 4.16: Schematic of the implemented 2 MHz current-starved ring oscillator, with frequency control and a clock divider.

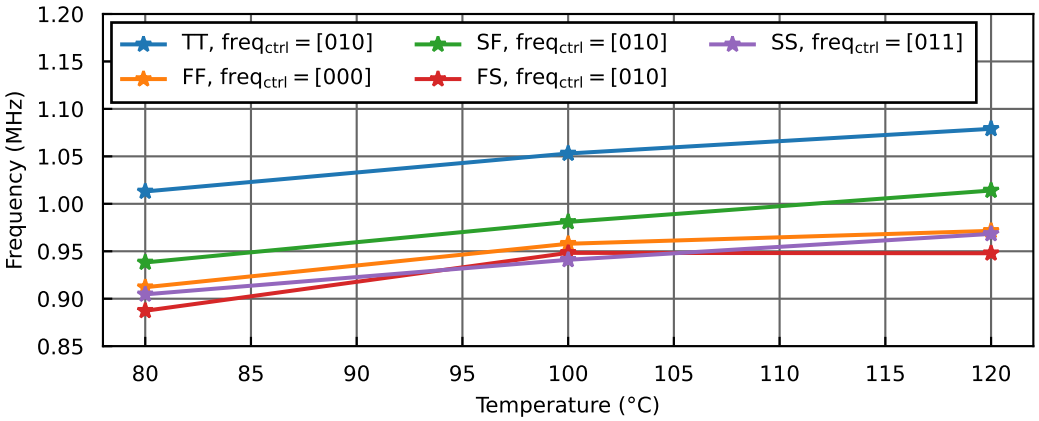



Figure 4.17: Simulated frequency of the ring oscillator across process corners and temperature. Simulated with extracted parasitics.

adjusting the frequency down to 1 MHz, while the other two bits control the biasing current of the PMOS cascodes of the inverter chain. The bias currents have been trimmed such, that lowest standard deviation was achieved across process corners around a 2 MHz frequency. In Fig. 4.17 the simulated frequency of $\text{clk}_{\text{int}}$ of the clock controller can be seen across process corners with their trimmed values. The simulation is made with extracted parasitics of the clock controller. The ring oscillator has been designed for 2 MHz around 100 °C, since the IC is expected to operate around this temperature. It can be seen, that there is still a large range of frequency spread for the ring oscillator, which is expected since only 2-bits are used to trim the biasing current.

The schematic of the implemented non-overlapping clock generator with a 1-bit dead-time control can be seen in Fig. 4.18. The circuit is responsible for generating $\varphi_1$ and $\varphi_2$

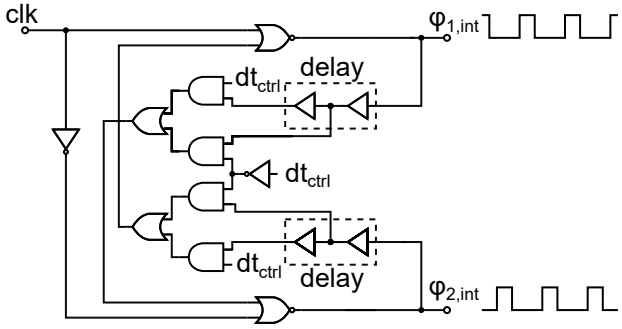



Figure 4.18: Schematic of the non-overlapping clock generator with a 1-bit dead-time control.

from the input clock signal and implements two different dead-times using delay buffers. The dead-times implemented are 26 ns and 42 ns. A lower dead-time is desirable since the dead-time effects the effective frequency of the switched-capacitor converter. If the dead-time is too low a shoot-through condition can occur in the power switches, which can damage the switches and lower efficiency.

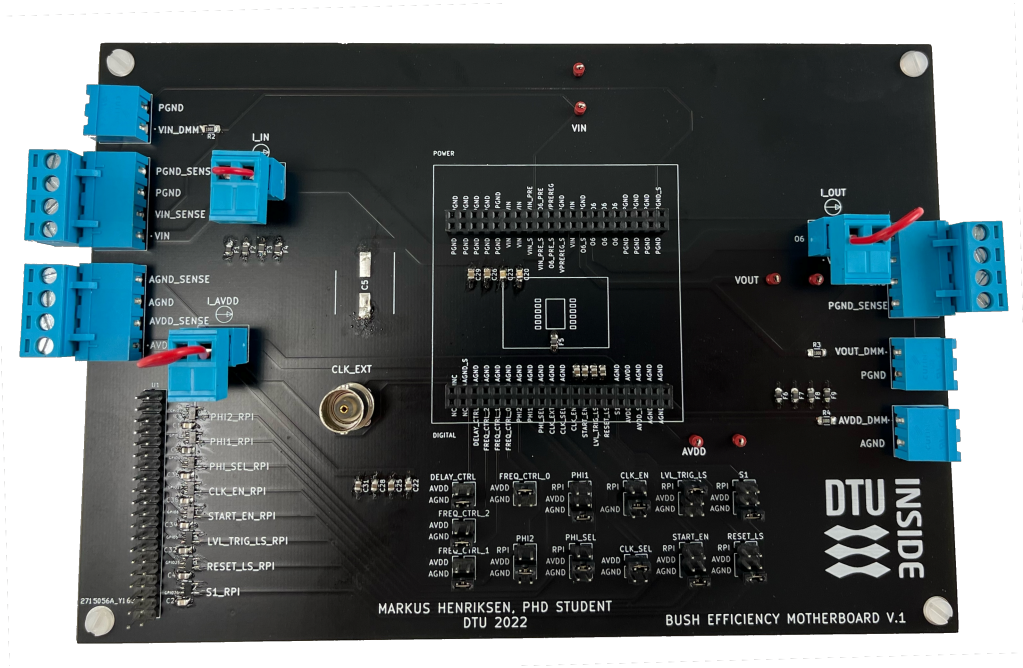
### 4.4.3 Verification setup

For the experimental results a prototype test PCB was made for implementing the designed highly-integrated switched-capacitor converter. The fabricated IC was packaged in a QFN 64-pin package, since multiple parallel bonding wires were used for the connections from the IC die to the external flying capacitors. The efficiency verification PCB consists of a motherboard and a daughterboard setup. The motherboard and daughterboards can be seen in Fig. 4.19. This setup is chosen, since it makes it easier to debug and test the power converter itself.

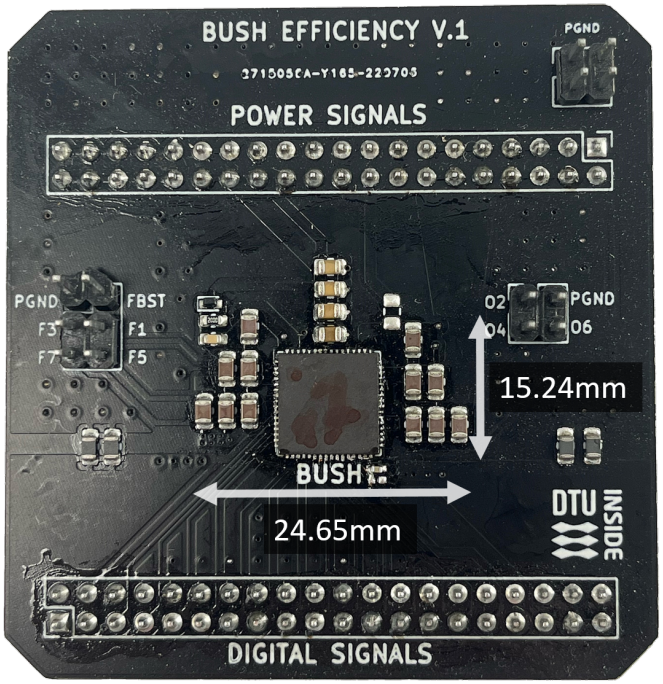
The PCB footprint area of the highly-integrated switched-capacitor converter is 24.65 mm$\times$ 15.24 mm and is annotated in Fig. 4.19b. This area includes all the flying capacitors, the $3 \times 10$ µF output capacitance for filtering the output ripple and the bootstrap capacitor and diode for supplying the integrated gate-driver of the top power switch $M_1$. The area is estimated as the smallest possible square that encases the components. The height of the power converter including the PCB is 2.6 mm, which leads to a total volume of 0.98 cm$^3$.

The verification setup used for measuring the efficiency and performance of the prototype converter can be seen in Fig. 4.20. The measurement station is controlled via a Python script running from a laptop. The script initialises and sets up all the instruments used. For the supply of the input of the power converter a 100 W source measure unit (SMU) is used. A 20 W SMU is used for the 5 V digital supply. The programming bits of the clock controller are supplied by an Raspberry Pi, which are controlled from the Python script. The input and output voltage was measured using a digital multi-meter (DMM). An 8-channel oscilloscope was used to measure any transient waveforms of the switching nodes in the switched-capacitor converter. A digital load was used as load current. The verification of the start-up circuit in the implementation is discussed in section 5.3.

The use of a scripted measurement setup ensures reliable, consistent and fast measurements and verification of the prototype.




(a) Prototype motherboard PCB for easy debugging of the highly-integrated switched-capacitor converter and connection to instruments.




(b) Prototype daughterboard PCB for testing the efficiency of the 48 V-12 V switched-capacitor converter.

Figure 4.19: Prototype testing PCBs for verifying the performance of the highly-integrated switched-capacitor converter.

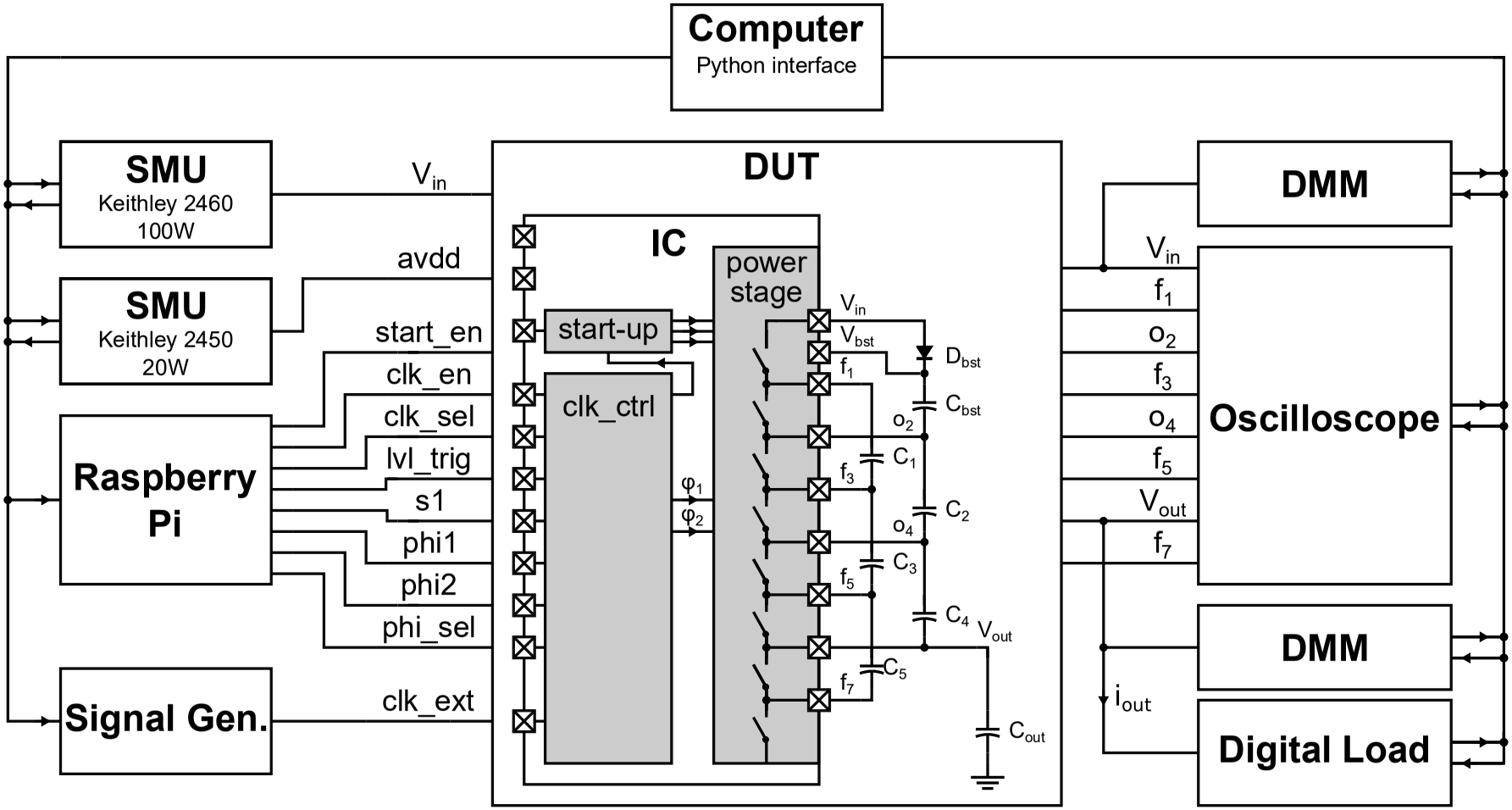



Figure 4.20: Overview of the experimental measurement setup used for testing the prototype switched-capacitor converter.

### 4.4.4 Experimental results

A die photo of the taped-out IC can be seen in Fig. 4.21. The area of the die is 10 mm$^2$. A 60 V power switch have been used for $M_1$ to ensure, that it could withstand the full input voltage. The 10 identical gate-drivers have been annotated as well in Fig. 4.21.

In Fig. 4.22 the efficiency of the prototype highly-integrated switched-capacitor converter can be seen for different load currents and switching frequencies. For these measurements an external clock was used, so that the impact of the switching frequency on the power converter efficiency could be investigated. From Fig. 4.22 it can be seen, that the power converter achieves a maximum efficiency of 93.5 % at a load current of 360 mA with a 250 kHz switching frequency. The measured output power at this current load is 4.18 W. The maximum output power of 24.6 W is achieved with a switching frequency of 750 kHz. Additionally, it can be seen that should a simple frequency controller be implemented for the highly-integrated switched-capacitor converter, then an >90 % efficiency can be achieved for a wide load range of 55 mA-1.65 A.

In Fig. 4.22 a simulation of the efficiency at a switching frequency of 1 MHz with extracted parasitics and an estimate of the bonding wire resistances can also be seen together with the measured results at 1 MHz. Comparing the simulated and measured efficiency it can be seen, that at low loads, there is a good correspondence, but when moving towards higher loads, where $P_{rout}$ losses become dominant the measured results shows significantly worse performance. At maximum measured load of 1.6 A the difference in efficiency is 2.12 % corresponding to a power loss difference of 410 mW between measurement and simulation. The difference in efficiency at higher loads indicates that the output resistance of the designed switched-capacitor converter is larger than initially expected. To investigate this the output resistance of the switched-capacitor converter was measured. The output resistance, together with the simulated output resistance with ex-

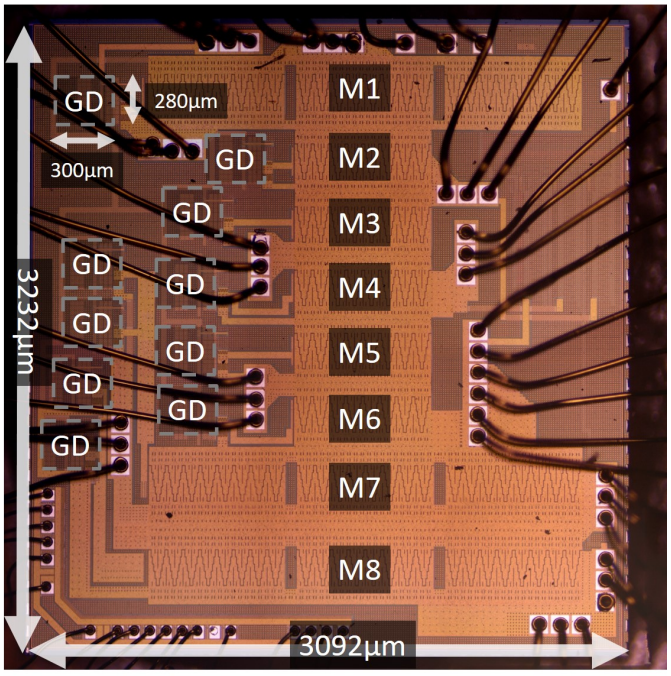



Figure 4.21: Die photo of the implemented IC with the gate-drivers and power switches annotated.

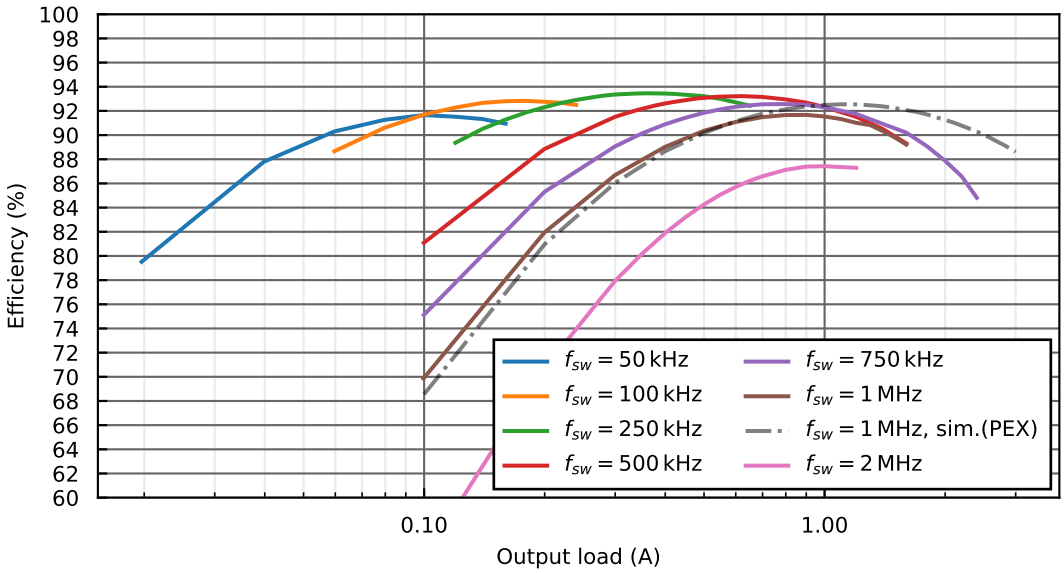



Figure 4.22: Measured efficiency of implemented prototype for various switching frequencies and load currents.

tracted parasitics and modeling the expected resistance in the bonding wires can be seen in Fig. 4.23. Here the calculated expected output resistance is also shown. From Fig. 4.23 it can be seen, that especially the estimation on the losses due to conduction losses are not properly modeled neither in calculations or simulation. This can be seen, since the measured output resistance at high frequencies, where conduction losses are dominant, is 150 m$\Omega$ higher than the simulated resistance. This is most likely due to the PCB trace resistance, which has not been modeled. Additionally, the extracted resistive parasitics of the power switches include only parts of the top level routing, meaning that the total metal routing resistance inside the IC is higher in the measured implementation than anticipated in the parasitic extraction simulation results.

To evaluate the transient performance of the designed prototype a load step of 1 A is applied to the power converter. The output voltage of the switched-capacitor converter

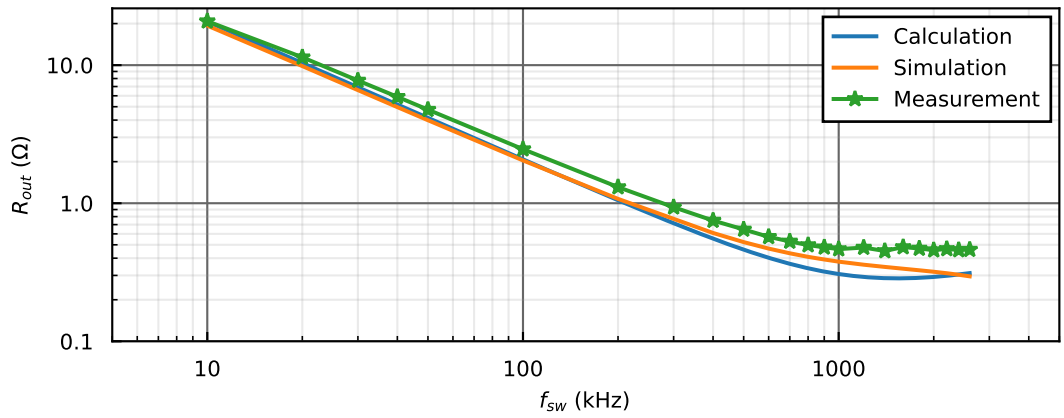



Figure 4.23: Comparison between the measured, simulated and calculated output resistance of the highly-integrated switched-capacitor converter.

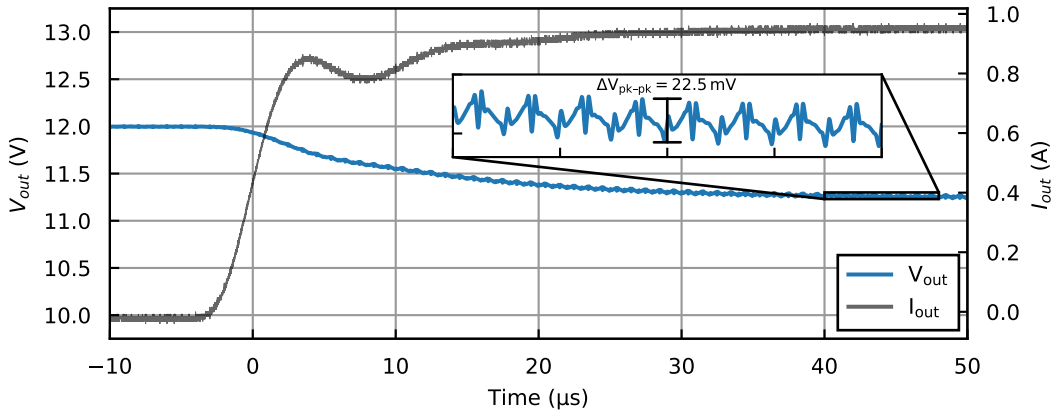



Figure 4.24: Transient response at the output of the switched-capacitor converter with a 1 A output load step. Voltage waveform is 20 MHz bandwidth limited.

together with the current load can be seen in Fig. 4.24. The current waveform is captured using a Hioki 3273-50 DC-50 MHz bandwidth current probe. The output voltage waveform is 20 MHz bandwidth limited. The unregulated output voltage settles at 11.25 V with a voltage ripple of 22.5 mV.

To investigate the output voltage ripple at maximum load conditions, the top switching node $f_1$ and the output voltage was measured as shown in Fig. 4.25 with an output load of 2.2 A. Here the output voltage ripple is increased to 102 mV and the average voltage is decreased to 10.63 V. It can be seen, that some ringing occur on both $V_{f1}$ and the output. These are during the dead time of 42 ns from the integrated clock controller.

In Fig. 4.26 two thermal pictures of the prototype highly-integrated switched-capacitor converter can be seen for a 1.6 A and a 2.2 A load condition. These are both measured with a switching frequency of 750 kHz. The thermal pictures are taken after the power converter has reached thermal steady-state and without any external cooling. For the 1.6 A load condition shown in Fig. 4.26a the maximum temperature is 83.4 °C. For the 2.2 A load condition in Fig. 4.26b, which is close to the maximum output power of 2.4 A, the

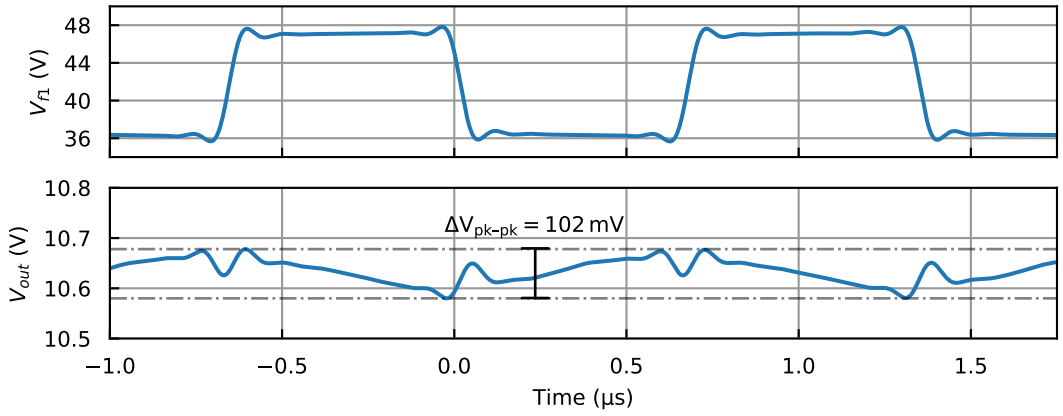
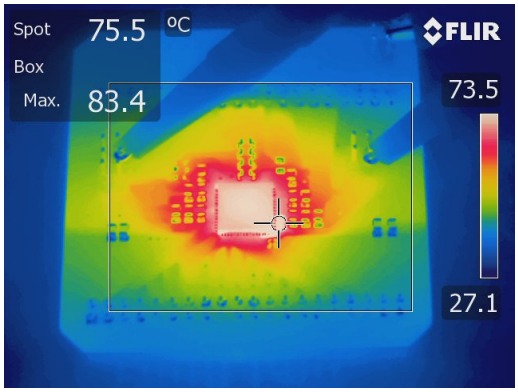
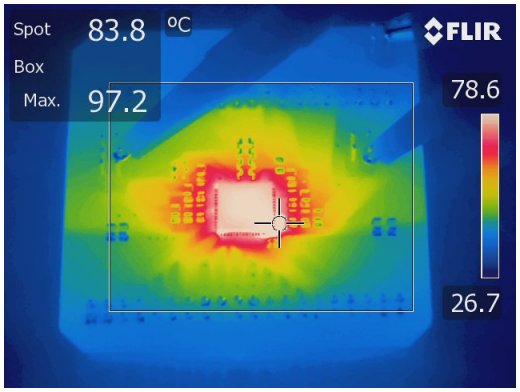



Figure 4.25: Measurement of the switching node voltage at $f_1$ and the output voltage ripple with a load current of 2.2 A. Waveforms are 20 MHz bandwidth limited.




(a) Thermal picture of the implemented switched-capacitor converter at 1.6 A output load.




(b) Thermal picture of the implemented switched-capacitor converter at 2.2 A output load.

Figure 4.26: Thermal pictures of the prototype switched-capacitor converter for two different load conditions.

maximum temperature has increased to 97.2 °C. In both cases the maximum temperature occur close to the $f_7$ and output node of the converter, where the highest currents are also expected from the charge multiplier vector for the Ladder topology.

### 4.4.5 Discussion on experimental results

From the thermal measurements at maximum load conditions it was shown that the maximum temperature of the power converter prototype reached 97.2 °C. This measurement was done without an external cooling fan, since the performance of the prototype and not that of an external fan was desired to be evaluated. Still in hindsight higher output power could probably have been tested to see the thermal limitation of the prototype before failure. This would increase the measured maximum output power and thereby the power density of the implementation.

The PCB layout of the prototype test board used for evaluating the performance could also be optimized for smaller area. Due to non-optimal bonding wire pad placements on the IC, the routing of some of the nodes lead to larger spacings between the chip package and the flying capacitors. This could be solved by better top-level layout floor-planning of the IC.

As can be seen from the daughterboard PCB in Fig. 4.19b the probe pads for measuring the transient waveforms of the switching nodes $f_1 - f_7$ and $o_2 - o_4$ have unnecessary long ground loops, which leads to ringing due to the wire inductance of the probes used. This ringing is filtered from the 20 MHz bandwidth of the measurement, but a measurement with a bandwidth of 100 MHz would have been interesting to better evaluate the ringing on the switching nodes due to the parasitic inductance of the bonding wires during the dead-time.

## 4.5 Summary

In this chapter a design and optimization methodology of highly-integrated switched-capacitors was presented. Three different strategies for supplying the floating gate-drivers required for driving the integrated switches were presented and their advantages and disadvantages in terms of utility and energy efficiency were summarized.

The discrete flying capacitors were optimized under a PCB area constraint, to determine

Table 4.8: Summary of experimental results for the 48 V-12 V highly-integrated switched-capacitor converter prototype.

| Topology | Process | $V_{in}$ (V) | $V_{out}$ (V) | $f_{sw}$ (kHz) | Max. Eff. (%) | Dimensions W × L × H (mm) | Max. $P_{out}$ (W) | Power density ($W/cm^3$) |
|---|---|---|---|---|---|---|---|---|
| 4:1 Ladder | 180 nm SOI-BCD | 48 | 12 | 0.25 | 93.5@4.18 W | 15.24 × 24.65 × 2.85 | 24.6 | 23.0 |

the optimal amount of parallel unit capacitors for each flying capacitor for a given PCB area in any highly-integrated switched-capacitor topology. The integrated switches were optimized based on a reformulation of the power losses described in section 3.2, where the losses were described as a function of the total integrated switch area and the switching frequency of the converter. This allows for an optimization of the switch area and switching frequency of the converter for a given load condition and for any highly-integrated switched-capacitor topology.

To verify the design and optimization methodology a 48 V-12 V highly-integrated switched-capacitor converter prototype was designed and fabricated in a 180 nm SOI-BCD process. A description of the gate-drivers and the clock generator was presented. A prototype test PCB was designed to evaluate the performance of the power converter. The measurement results are summarized in Table 4.8. Finally, a brief discussion on the experimental results and suggestions for improvements were presented.

# 5 Analysis of start-up challenges in switched-capacitor converters

This chapter describes the design challenges regarding safe start-up of highly-integrated switched-capacitor converters. It presents the various challenges when dealing with safe start-up related to maximum inrush currents and ensuring, that the maximum voltage ratings of the switches are not exceeded. Different methods to ensure safe start-up are presented, evaluated with simulation results and compared. A prototype of a fully integrated active pre-charge circuit for safe start-up for a 48 V-12 V highly-integrated switched-capacitor converter has been designed, fabricated and measured to verify the concept.

This chapter is a more detailed description of the work presented in the publications shown in Appendix A and Appendix B, which were authored as a part of the Ph.D. project.

## 5.1 Start-up challenges in switched-capacitor converters

While start-up has been widely researched for inductor-based power converters leading to various inrush current limitation circuits and strategies [78]–[86], the start-up challenges for switched-capacitor-based converters have only recently started to become a research focus [17], [87]–[89]. Compared to traditional inductor-based power converters, where the start-up challenge is mostly concerning limiting the inrush current from the input voltage source, the switched-capacitor converter suffers from both inrush currents and that the switches and passive components are usually not designed to handle the full input voltage. Without a start-up strategy, there is no way to ensure that the maximum voltage and current ratings of the active and passive components are not exceeded.

The inrush current in switched-capacitor converters originates from the flying capacitors voltages having a large mismatch as the input voltage is ramping up. The flying capacitors are charged through parasitic capacitor paths either from the switches or other circuits interfacing with the input of the converter. Predicting the flying capacitor voltages before enabling the power converter is not practical without a dedicated start-up strategy.

Depending on the topology, rise-time of the input voltage and the switched-capacitor implementation the inrush currents can easily become destructive to the converter. For switched-capacitor converters, the large inrush currents during start-up is experienced at all nodes of the converter, since it occurs due to the voltage mismatch of the flying capacitors being connected in parallel through low on-state resistance switches. A single input inrush current limiting circuit such as used for inductor-based power converters is therefore not enough to ensure safe start-up.

Ensuring that the maximum voltage ratings of the switches and flying capacitors are not exceeded is another challenge of ensuring safe start-up of switched-capacitor converters. One of the main benefits of switched-capacitor converters is that both the flying capacitors and the switches only see a fraction of the input voltage in steady-state operation, thereby making use of switches with lower area specific on-state resistance and higher capacitance density capacitors. This does however mean, that during start-up these maximum voltage ratings can be exceeded and be destructive to the power converter unless a safe start-up strategy is implemented.

### 5.1.1 Start-up voltage challenges in switched-capacitor converters

As the input voltage ramps up the flying capacitors are charged through parasitic charging paths from the switches or other circuitry. This can lead to individual maximum voltage ratings of the switches and flying capacitors being exceeded and thereby destructive to the converter.

The voltages of the flying capacitors as the input ramps up depends on the topology and the rise-time of the input voltage ramp. In general, this is difficult to assess for a given topology, since all the parasitic charging paths can be hard to determine accurately. Therefore, it is necessary to implement a strategy that controls the flying capacitor voltages.

A highly-integrated 4:1 Ladder topology with external flying capacitors and integrated power stage and gate-drivers can be seen in Fig. 5.1. Here the parasitic capacitances of the switches are shown as well to emphasize the complex parasitic charging paths during the start-up. The size of these parasitic capacitances depend on the size of the switches. The highly-integrated switched-capacitor converter in Fig. 5.1 is implemented with gate-drivers with a regulator supply connected to the input voltage. This will lead to additional charging paths from the input to the flying capacitor nodes. Additionally, there will be capacitive coupling between the voltage nodes due to the PCB traces.

A transient simulation of the highly-integrated 4:1 Ladder converter illustrated in Fig. 5.1 has been performed with an input voltage of 48 V, a 1 ms rise-time ramp and no start-up strategy can as seen in Fig. 5.2. From Fig. 5.2 it is clear, that the voltage nodes of the switched-capacitor converter are charged even with the converter being disabled and the switches open. Furthermore, it can be seen that the voltages do not end up at the desired

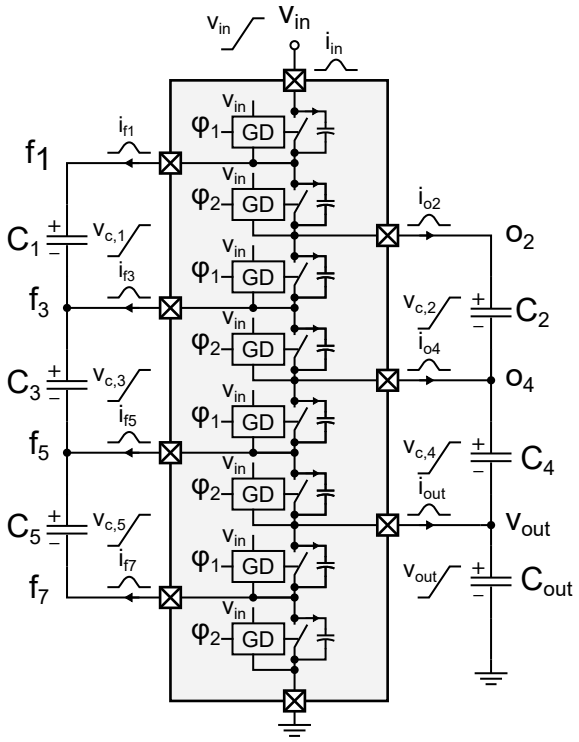



Figure 5.1: A highly-integrated 4:1 Ladder switched-capacitor converter with annotated voltage ramps and currents due to parasitic charging paths during input voltage ramp-up.

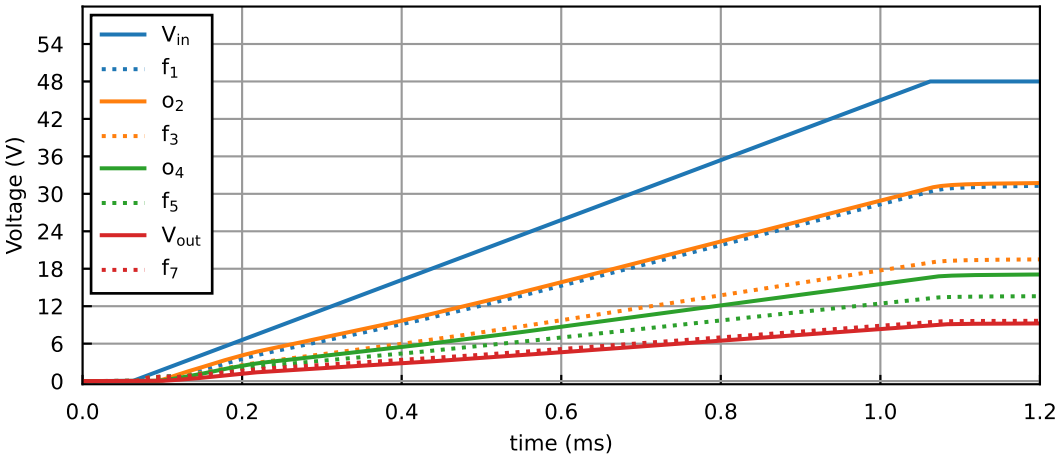



Figure 5.2: Simulated voltage nodes of 4:1 Ladder highly-integrated converter with no safe start-up strategy.

steady-state voltages for a 4:1 Ladder converter. This simulation is not including PCB trace capacitance and can not be used to predict the actual voltage nodes in an physical implementation, since that would also depend on starting conditions, leftover charge from a previous booting cycle, sizes of the passive and integrated components and therefore practically non-predictable. Instead the simulation can be used to verify that the voltage nodes will be charged to some values and that it has the possibility to exceed the individual steady-state maximum voltages of the switches, indicating that a dedicated start-up strategy is necessary for ensuring safe start-up of the switched-capacitor converter.

### 5.1.2 Start-up inrush currents in highly-integrated switched-capacitor converters

When the switched-capacitor converter is enabled, the flying capacitors are connected in parallel through low on-state resistance switches. The voltage mismatch between these capacitors therefore leads to high peak currents for the first couple of switching cycles until the steady-state voltages of all nodes have been reached. In highly-integrated switched-capacitor converters these peak currents can be destructive to both the integrated circuit but also the bonding wires (or any other die connection) acting as interconnection between the PCB and IC.

The parallel connection of the external flying capacitors can be described as a series RLC circuit connecting the flying capacitors with a mismatch voltage $V_s$. An illustration of the connection of two flying capacitors for a highly-integrated switched-capacitor converter can be seen in Fig. 5.3 together with the equivalent RLC circuit. Here both the parasitic resistance and inductance of the bonding wires and the equivalent series resistance and inductance of the external flying capacitors are illustrated, since these all contribute to the inrush peak current waveform. Note, that four bonding wires and two switches are used when connecting the external capacitors. The integrated switches are modelled by an ideal switch with a series resistance $R_{ds}$ equivalent to the on-state resistance of the switches. The $R_{ds}$ is usually the dominant resistance in the RLC circuit while the $4L_{bond}$ contribute the most to the series inductance. The equivalent circuit resistance can be described as:

$$R' = 2R_{ds} + 2 \cdot ESR + 4R_{bond} \tag{5.1}$$

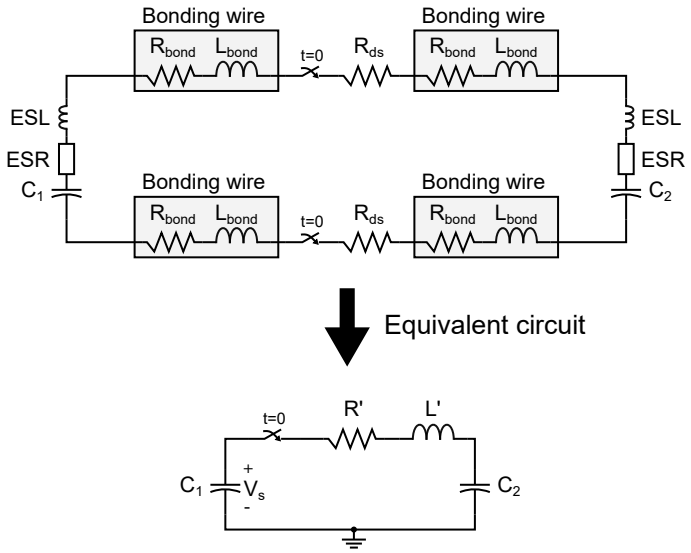



Figure 5.3: Equivalent series RLC circuit when two external flying capacitors are connected in parallel by integrated switches.

and the equivalent circuit inductance is:

$$L' = 4L_{bond} + 2 \cdot ESL \tag{5.2}$$

The peak inrush current as the two capacitors are connected can be approximated by [90]:

$$i_{peak} = \frac{V_s}{L' \cdot \omega_d} \mathrm{e}^{\frac{-\alpha\pi}{2\omega_d}} \tag{5.3}$$

where $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$, $\omega_0 = \sqrt{\frac{C_1+C_2}{L'C_1C_2}}$ and $\alpha = \frac{R'}{2L'}$. The series RLC system is typically under-damped since a low on-state resistance is desired to achieve a high converter efficiency. This under-damping is what can lead to large peak currents during start-up until $V_s$ has been decreased enough in steady-state operation. The inductance comes primarily from the bonding wire inductance and the PCB trace inductance and is also minimized to ensure high efficiency. The damping factor for a series RLC circuit can be expressed as:

$$\zeta = \frac{\alpha}{\omega_0} \tag{5.4}$$

The system is described as under-damped for $\zeta < 1$, critically damped for $\zeta = 1$ and over-damped for $\zeta > 1$. Rearranging (5.4) to isolate the equivalent flying capacitor value $C_1C_2/(C_1 + C_2)$ the requirement if over-damping is desired, and thereby lower peak currents, can be expressed as:

$$\frac{C_1C_2}{C_1 + C_2} > \frac{4L'}{R'^2} \tag{5.5}$$

Depending on the implementation and application this sizing requirement of the flying capacitor is not always feasible. Especially for implementations targeting higher output power and thereby requiring really low on-state resistances and design for really low parasitic series inductance to achieve good efficiency.

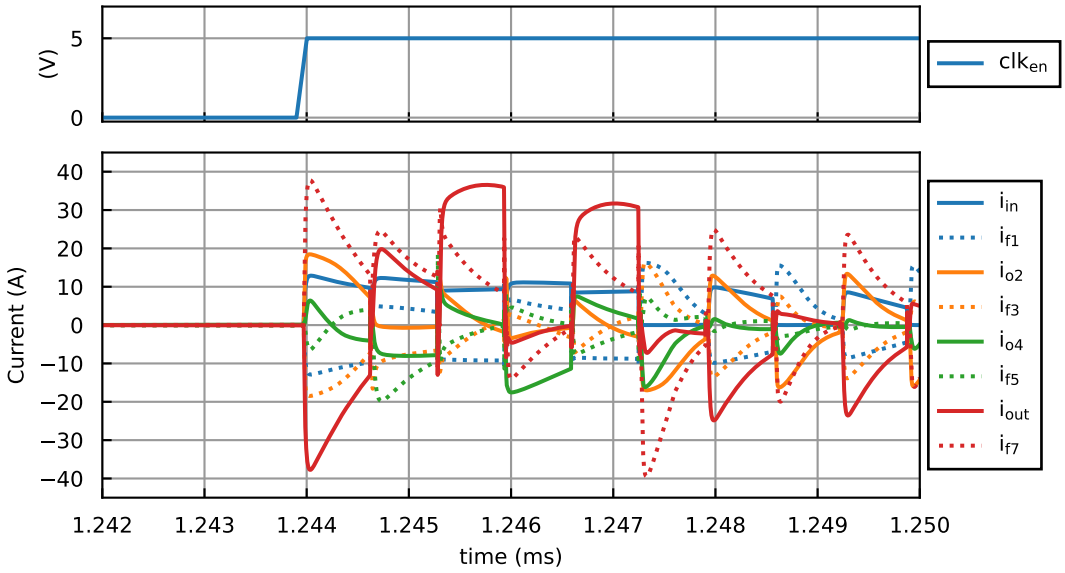



Figure 5.4: Simulated currents in 4:1 Ladder highly-integrated converter with no safe start-up strategy.

A simulation of the inrush currents for the highly-integrated 4:1 Ladder switched-capacitor converter in Fig. 5.1 can be seen in Fig. 5.4. Here the $clk_{en}$ signal refers to the enable signal of power converter, where the flying capacitors, which have been charged to the voltages simulated in Fig. 5.2 are first connected in parallel. The simulation shows, that the maximum peak currents can reach almost 40 A, which would to damaging of the IC and bonding wires. This illustrates the requirement that a start-up strategy is implemented to handle the peak currents as expressed in (5.3) to ensure safe start-up of highly-integrated switched-capacitor converters.

### 5.1.3 Summary of start-up challenges in switched-capacitor converters

The challenges of achieving safe start-up of switched-capacitor converters consists in general of two challenges. (1) the maximum voltage ratings of the switches and capacitors should not be exceeded as the input voltage ramps up. (2) the peak inrush currents due to the flying capacitor voltage mismatch should be handles such, that it does not damage the IC.

Depending on the application and implementation of the switched-capacitor converter these two challenges can have different priorities. For low-power applications where the on-state resistance of the switches are in the range of 0.5-2 $\Omega$, the equivalent series RLC circuit between the parallel connection of the flying capacitors are usually over-damped and the peak inrush currents are not necessarily of a great concern.

For high-power applications the necessity of low on-state resistance of the switches to ensure high energy-efficiency leads to an under-damped series RLC circuit for the parallel connections of the flying capacitors. This means that the peak inrush currents can become very large and damage the packaging interface such as bonding wires and the IC itself.

Ensuring that the maximum voltage ratings are not exceeded is critical for any application and implementation and a safe start-up strategy to solve this challenge is necessary for all switched-capacitor converters, where the input voltage exceeds that of the individual voltage ratings of the used devices.

## 5.2 Methods for ensuring safe start-up in switched-capacitor converters

This section will address both start-up challenges, since the scope of this Ph.D. project is for applications requiring low on-state resistances and input voltages that exceed the individual maximum ratings of both the external flying capacitors and the integrated switches.

This section provides three approaches to solving the safe start-up challenges of switched-capacitor converters. The three methods are; a passive start-up method, a switch conductance modulation and an active pre-charging circuit method. These methods have different benefits and downsides and the best option depends on the implementation and application of the switched-capacitor converter.

### 5.2.1 Passive start-up method

A way of ensuring that the voltages do not exceed the maximum voltage ratings of the switches and flying capacitors is to make a designated charge path that ensures that the flying capacitors of the converters are charged to voltages close to the steady-state operation values as the input voltage ramps up.

An example of this can be seen for a highly-integrated 4:1 Ladder topology switched-capacitor converter in Fig. 5.5. Here a capacitor $C_{start}$ is connected between the input voltage and the $O_2$ node. This creates a charging path from the input to the capacitors $C_{start}$, $C_2$, $C_4$ and $C_{out}$. To properly charge $C_1$, $C_3$ and $C_5$ the gate signal $s_1$ for the top switch $M_1$ is enabled as soon as the gate-driver is able to, so that a charging path from $V_{in}$ is created through flying capacitors $C_1$, $C_3$ and $C_5$. This makes the voltage at $f_7$ increase and turns on the body diode of $M_7$ connected the capacitor string to $C_{out}$. The equivalent capacitor network circuit during the start-up ramp can also be seen in Fig. 5.5.

Here it is assumed that the on-state resistance of $M_1$ is low enough, that the $f_1$ node is so close to $V_{in}$ that the bootstrap diode $D_{bst}$ is not enabled and therefore $C_{bst}$ does not alter the charging network. From Fig. 5.5 it is clear that the passive start-up methods inflicts

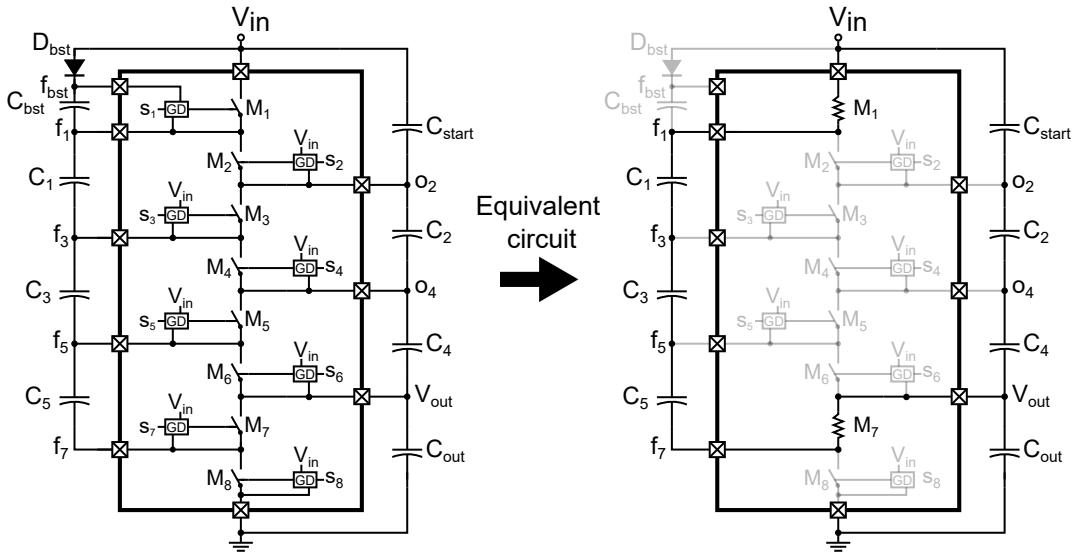



Figure 5.5: A highly-integrated 4:1 Ladder switched-capacitor converter with a passive safe start-up strategy using $C_{start}$ to create a charging path from $V_{in}$ to all flying capacitors and the equivalent charging path circuit.

sizing requirements to the flying capacitor in order to ensure, that the final voltages reach the desired steady-state voltages.

For the 4:1 Ladder topology all capacitors must be charged to same steady-state voltage of $\frac{1}{4}V_{in}$. This is achieved by sizing the capacitors as:

$$C_{start} = C_1 = C_2 = C_3 = C_4 = C_5 = \frac{1}{2}C_{out} \tag{5.6}$$

For other topologies, the sizing requirement will differ, since the steady-state voltages differ. This can however always be solved by either manipulating the charging paths and turning on more switches in the power stage, by a different sizing scheme of the flying capacitors or a combination of both.

A transient simulation of the highly-integrated 4:1 Ladder topology switched-capacitor converter flying node voltages for an input voltage ramp-up from 0 V to 48 V in 1 ms is shown in Fig. 5.6. Here parasitic inductance and resistance is added to the bonding wires and with flying capacitors $C_{start}$, $C_1$, $C_2$, $C_3$, $C_4$ and $C_6$ being 5.4 µF and $C_{out} = 10.8$ µF. From Fig. 5.6 it can be seen, that all flying node voltages are settled very close to the desired steady-state voltages. Note, that this is before the power converter clock is enabled and with only $M_1$ enabled.

After the input ramp, a transient simulation of the currents flowing into the IC as the power converter clock is enabled can be seen in Fig. 5.7. Here an initial peak current of just above 6 A is simulated for $i_{in}$, due to the remaining mismatch voltage of the flying capacitors. The currents are settled within a single switching period. While the simulation still shows, that the inrush peak current of is in the order of 7-8 times larger than the steady-state currents, this is still an improvement to the 40 A simulation results shown in Fig. 5.4 where no start-up strategy is used.

A key benefit of the passive start-up method is that it only requires a single capacitor to be achieved and no additional circuitry is required. The complexity and power loss associated with the passive start-up method is therefore low and can be implemented post-fabrication. Some downsides are that the sizing requirements conflicts with the optimal sizing scalings presented in chapter 4, thereby leading to a sub-optimal power converter

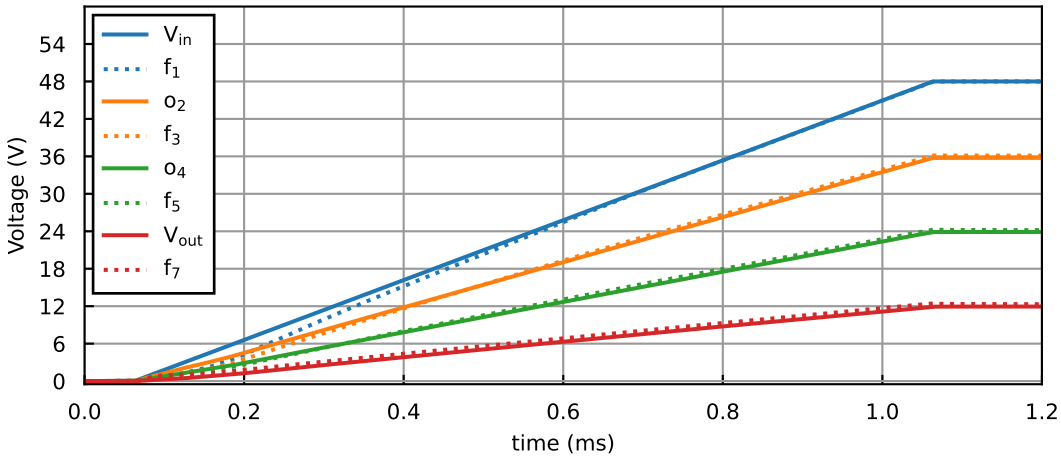



Figure 5.6: Simulated voltage nodes of highly-integrated 4:1 Ladder switched-capacitor converter using a passive safe start-up strategy.

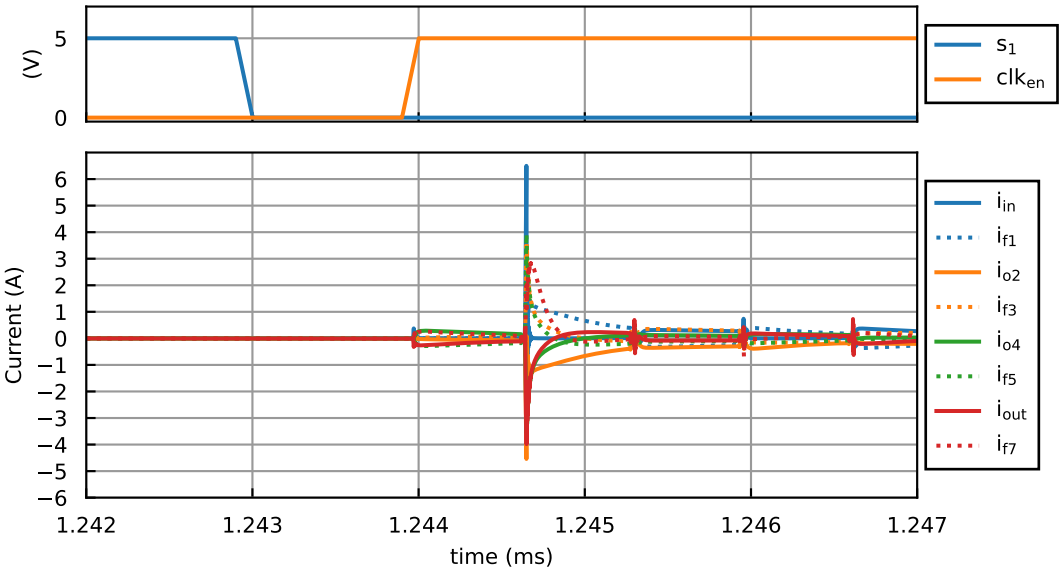



Figure 5.7: Simulated currents in highly-integrated 4:1 Ladder switched-capacitor converter using a passive safe start-up strategy.

design in regards of power density. Furthermore, capacitor variance will lead to variation in the final capacitor voltages. This can lead to an increase in the inrush currents.

The passive start-up method is most suitable for low power or fully integrated solutions, where the on-state resistances of the switches are higher and not exceeding the maximum voltage ratings of the switches and flying capacitors are the main concerns.

### 5.2.2 Switch conductance control method

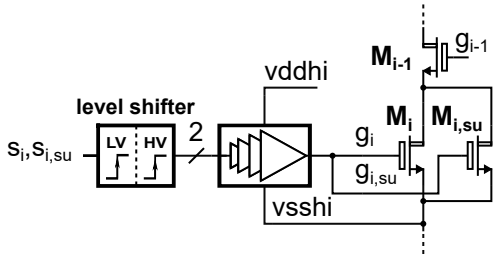



Figure 5.8: Illustration of switch conductance control to ensure safe start-up for switched-capacitor converters, by only enabling a small part of the switch during start-up to limit the inrush currents.

Since the large peak inrush start-up currents happens due to the flying capacitors being connected by low on-state resistance switches while having a voltage mismatch, another approach is to change the on-state resistance during start-up. This start-up strategy is referred to as switch conductance control. The basic idea is to only enable a small part of the switch until the power converter reaches its steady-state voltages. This has previously been presented in [90] as a start-up strategy for a buck converter, but can be used for any type of power converter.

An example of an implementation of the switch conductance control can be seen in Fig. 5.8. Here the floating gate-drivers require another control signal in order to control only a frac-

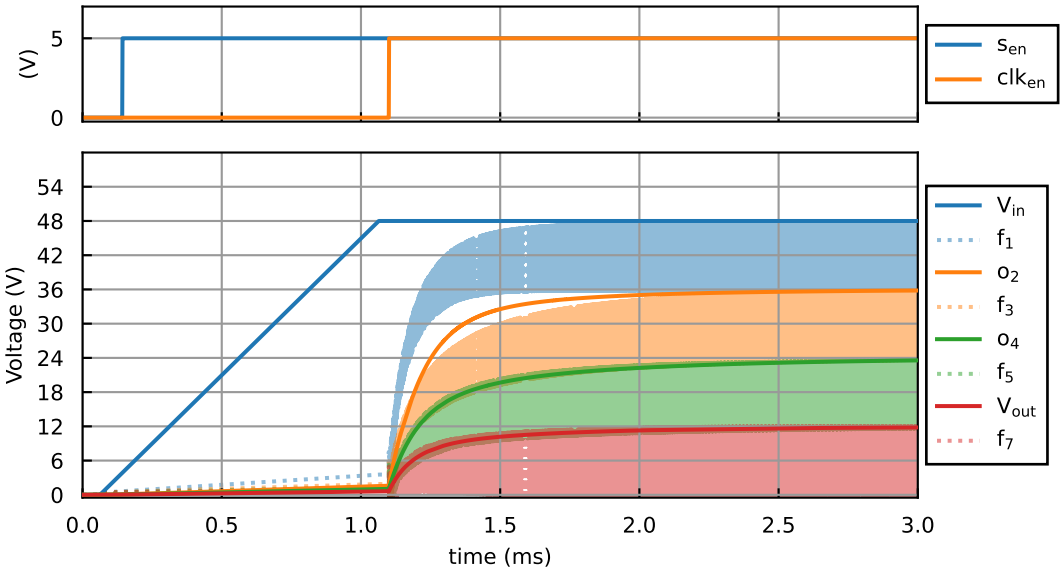



Figure 5.9: Simulated voltage nodes of highly-integrated 4:1 Ladder switched-capacitor converter using switch conductance control to ensure safe start-up.

tion ($M_{i,su}$) of the total power switch $M_i$. This increases complexity of the gate-driver and control.

The switch conductance control is primarily focusing on limiting the inrush currents. To ensure that the maximum voltage ratings for the switches and capacitors are not exceeded different strategies depending on the application and implementation can be considered. The switch conductance control can be combined with the passive start-up method to lower the peak currents simulated and shown in Fig. 5.7 or if possible in the application the clock for the low conductance switches can be enabled early as the input voltage

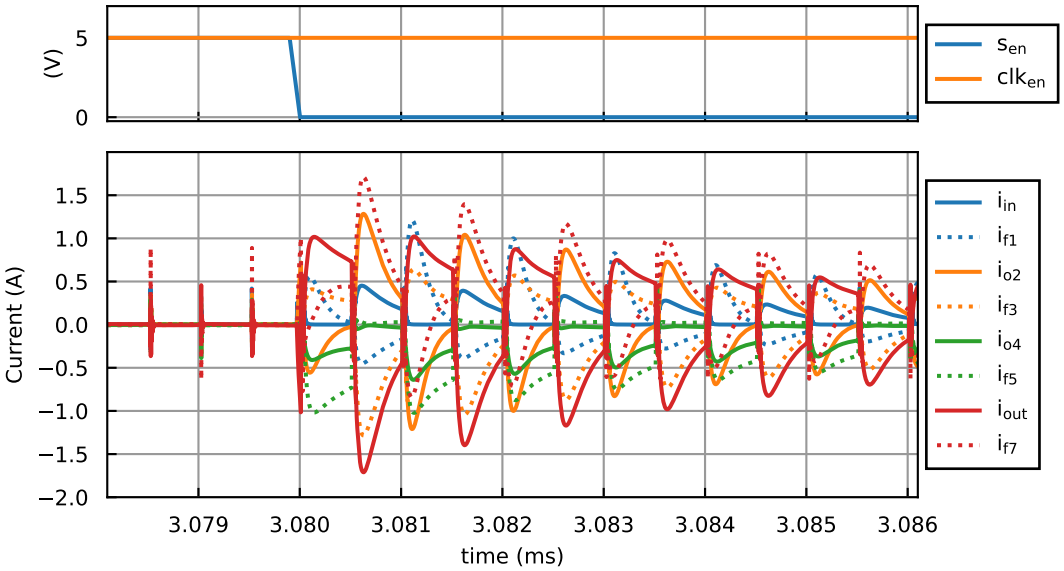



Figure 5.10: Simulated inrush currents in highly-integrated 4:1 Ladder switched-capacitor converter using switch conductance control to ensure safe start-up.

ramps up before any voltage ratings are exceeded. If switch devices that can tolerate the full input voltage are available, the top switch can also be designed to handle the full input voltage, while the input ramps up by enabling all other switches in the power stage.

The on-state resistance of a N-MOSFET switch operating in the linear region can be expressed as:

$$R_{ds} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_t)} \tag{5.7}$$

where $\mu_n$ is the electron mobility, $C_{ox}$ is the gate oxide capacitance per unit area, W and L is the width and length of the MOSFET, $V_{GS}$ is the gate-source voltage and $V_t$ is the threshold voltage of the device.

The on-state resistance of the $M_{i,su}$ needs to be high enough to ensure that the equivalent series RLC system is over-damped. A larger on-state resistance does however also mean a slower settling time of the flying nodes.

A transient simulation of the voltage nodes of a highly-integrated 4:1 Ladder topology switched-capacitor converter using switch conductance control for start-up can be seen in Fig. 5.9. Here the start-up procedure consists of the input voltage being ramped up and then enabling the low conductance switches only until the voltage have reached the desired steady-state. When the desired steady-state voltages have been reached the full conductance of the switches are enabled by disabling the start-up control bit $s_{en}$.

This simulation is using on-state resistances of 25 $\Omega$ for the low conductance mode and 105 m$\Omega$ for the normal operation. The inrush peak currents as the high conductance mode is enabled can be seen in Fig. 5.10. Here it can be seen that the maximum peak current is around 1.7 A and that the current waveform settles within 6 switching periods to the steady-state peak currents.

The switch conductance control method limits the inrush peak currents by using only a small part of the switches until the switched-capacitor nodes have reached the desired steady-state. The method can be used for any topology to ensure safe start-up. The switch conductance control does not inherently ensure that the maximum voltages of the switches and flying capacitors are not exceeded. The method can be combined with other start-up methods such as the passive start-up methods. Another possibility is enabling the low conductance switches while the input voltage is still ramping up, thereby ensuring that the maximum voltages of both switches and flying capacitors are not exceeded.

### 5.2.3 Active pre-charge circuit method

Another method to ensure that the flying capacitor voltages are at their desired steady-state values before enabling the power converter clock, is to have a circuit responsible for charging the flying capacitors to a set reference voltage. This is referred to as an active pre-charge circuit.

The concept is an integrated circuit, that charges all flying capacitors from the input voltage to a reference voltage as the input ramps up. This means that the mismatch voltage of the flying capacitors as the power converter clock is enabled is so small, that the inrush start-up currents do not damage the IC. Furthermore, it ensures that the maximum voltage ratings of both switches and flying capacitors are not exceeded.

There are various methods of designing an active pre-charge circuit, but most consists of simple linear regulators. An example using a shunt regulator can be seen in Fig. 5.11. It consists of a large pass transistor $M_{pass}$ with a sink resistor $R_{sink}$, which is enabled by

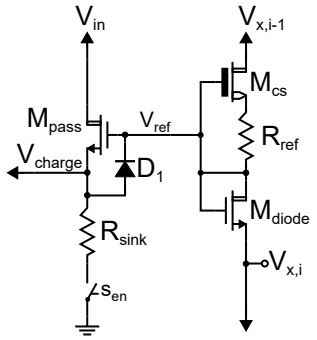



Figure 5.11: Shunt regulator used as active pre-charge circuit block for charging flying capacitors.

the start-up control bit $s_{en}$. The diode $D_1$ is there to ensure, that the $V_{gs}$ of $M_{pass}$ does not exceed its minimum value. The shunt regulator generates a voltage equal to:

$$V_{charge} = V_{ref} - V_{t,Mpass} \tag{5.8}$$

Since the $V_{gs}$ needs to be larger than $V_{t,Mpass}$ in order for the $M_{pass}$ device to charge.

The $V_x$ node of the active pre-charge circuit in Fig. 5.11 is generated by a resistor string from the input voltage to ground. These resistor string voltages are the steady-state reference voltages desired for the different flying capacitors. To ensure that $V_{charge} = V_x$, a diode coupled replica of the pass transistor $M_{diode}$ is biased by a currents source consisting of a depletion device $M_{cs}$ and $R_{ref}$. This ensures that the generated $V_{ref}$ is:

$$V_{ref} = V_x + V_{t,Mdiode} \tag{5.9}$$

Matching $M_{pass}$ and $M_{diode}$ carefully then means that $V_{t,Mpass} \approx V_{t,Mdiode}$ across local and global variations and for various temperatures. Utilizing this means the generated voltage of the active pre-charge circuit described in (5.8) can be rewritten as:

$$V_{charge} = V_x + V_{t,Mdiode} - V_{t,Mpass} \approx V_x \tag{5.10}$$

In Fig. 5.12 a highly-integrated 4:1 Ladder topology switched-capacitor converter with the entire active pre-charge circuit (APC) can be seen. Three identical active pre-charge circuit blocks are required for generating each of the reference voltages of the switched-capacitor converter. The active pre-charge circuits are directly connected to flying capacitors $C_2$, $C_4$ and $C_{out}$. To ensure, that $C_1$, $C_3$ and $C_5$ gets charged as well, the bottom switch $M_8$ is enabled by the start-up control bit $s_{en}$. This forces the voltage at $f_7$ to ground, which turns on the body diode of $M_2$, $M_4$ and $M_6$ such that $C_1$, $C_3$ and $C_5$ are also charged by the active pre-charge circuit and connected in parallel with $C_2$, $C_4$ and $C_{out}$ respectively.

When the active pre-charge circuit has charged the flying capacitors to the desired steady-state voltages the start-up control bit is disabled, which disconnects the $R_{sink}$ resistance of the individual ACP blocks and changes the bottom resistor in the resistor string generating the $V_x$ reference voltages. All the $V_x$ values are shifted down, such that the reference voltages are below the steady-state voltages of the capacitors. This disables the $M_{pass}$ transistor, such that it does not charge the flying nodes. No overlap of $s_{en}$ and the clock enable of the power converter system clock is allowed, since that would short the output

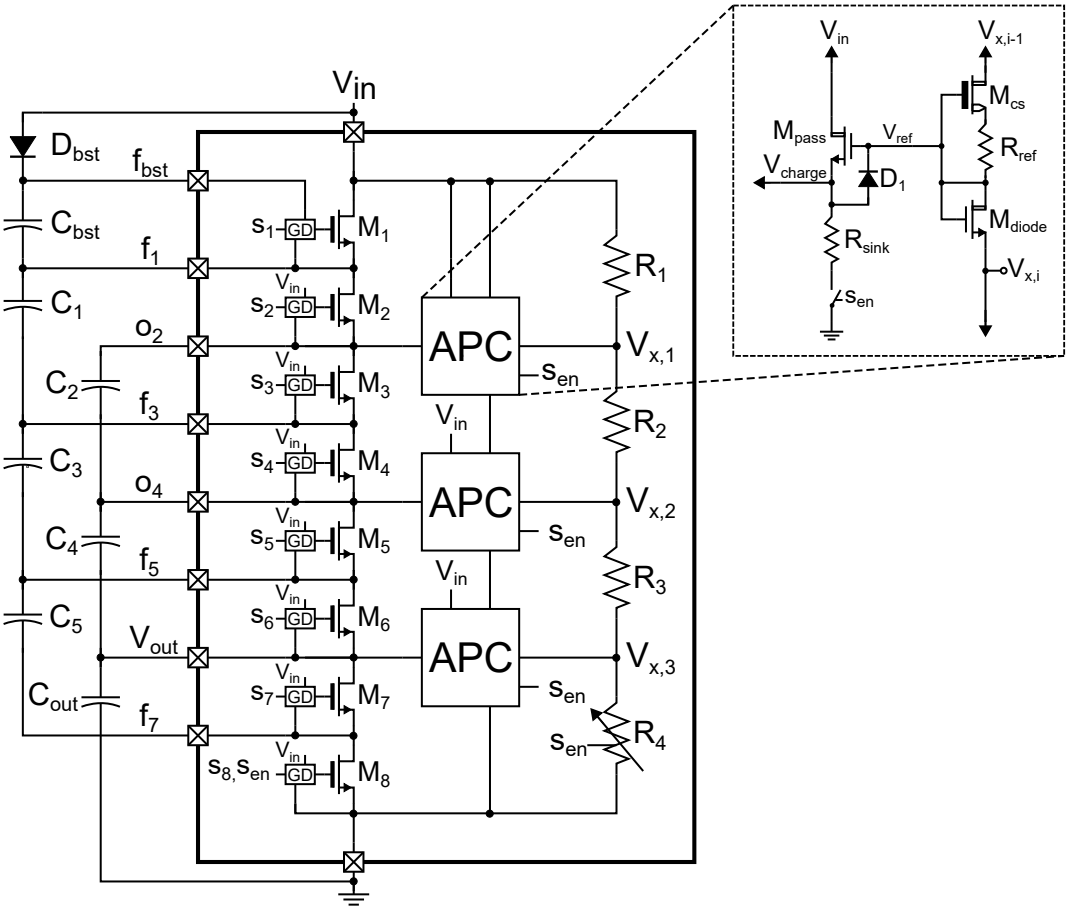



Figure 5.12: A highly-integrated 4:1 Ladder switched-capacitor converter with an active pre-charge circuit (APC) to ensure safe start-up.

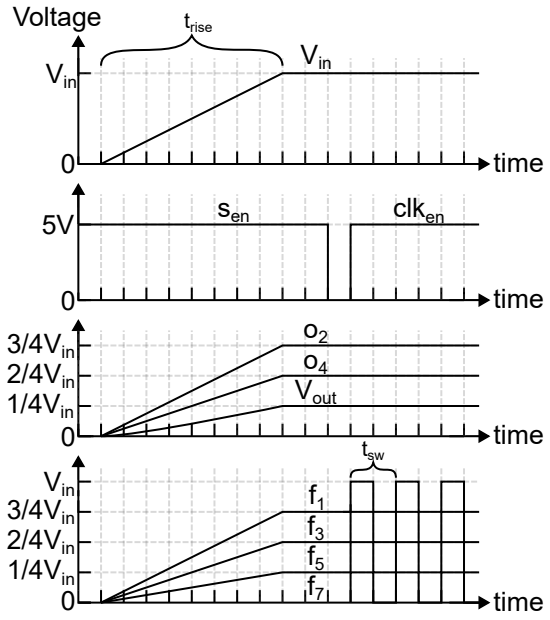



Figure 5.13: Start-up procedure for the active pre-charge circuit.

voltage of the power converter through $M_7$ and $M_8$. The start-up procedure is illustrated in Fig. 5.13.

A transient simulation of the voltage nodes of the highly-integrated 4:1 Ladder switched-capacitor converter using an active pre-charge circuit to ensure safe start-up similar to Fig. 5.12 can be seen in Fig. 5.14.

Here it can be seen, that the voltage nodes are charged to the desired steady-state voltages. A closer look into the transient simulated inrush currents as the clock is enabled can be seen in Fig. 5.15. This shows that the maximum peak currents are below 1.5 A and that it is close to the expected steady state inrush peak currents. The maximum currents occur in $f_7$ and $V_{out}$, which aligns well with the charge vector multiplier for the 4:1 Ladder topology, which indicates the largest steady-state currents through $C_5$ and $C_{out}$.

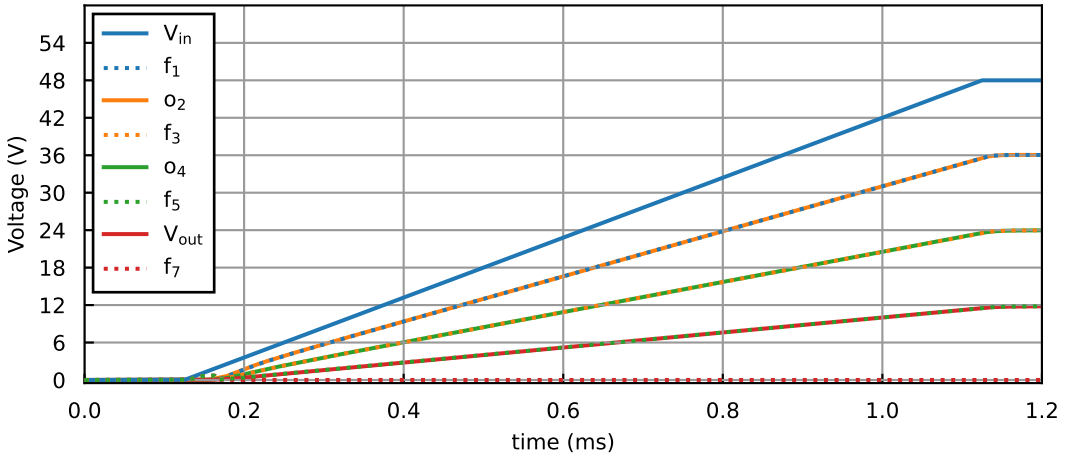



Figure 5.14: Simulated voltage nodes of a highly-integrated 4:1 Ladder switched-capacitor converter with using an active pre-charge circuit to ensure safe start-up.

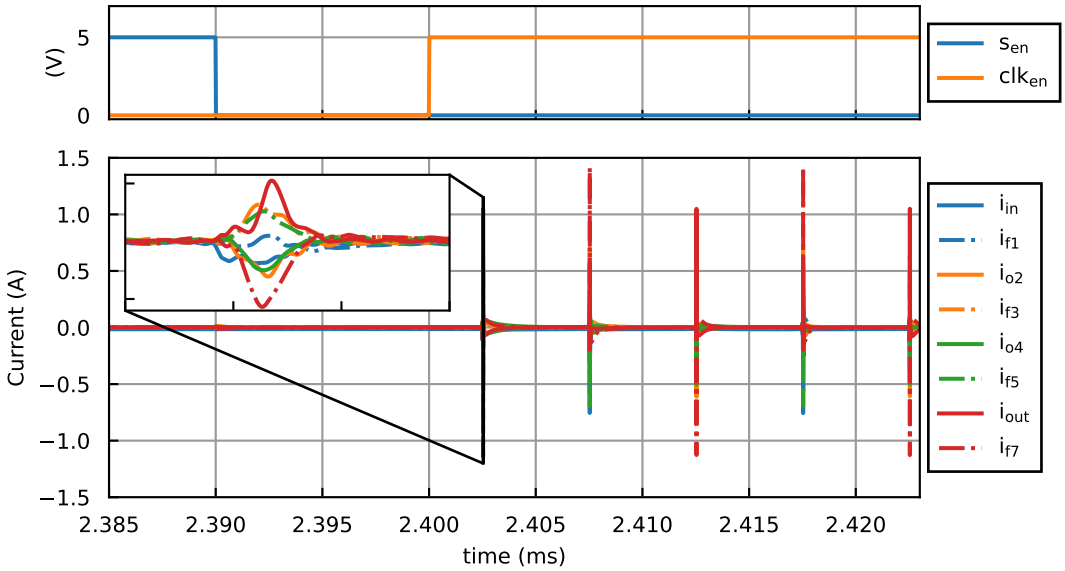



Figure 5.15: Simulated currents for a highly-integrated 4:1 Ladder switched-capacitor converter with using an active pre-charge circuit to ensure safe start-up.

The active pre-charge methods can ensure that both the maximum voltage ratings of the switches are not exceeded and that the inrush currents are limited to what can be expected in steady-state. The downside of the active pre-charge circuit is that it consumes a quiescent current from the resistor string. This can make it less appealing in low power applications, where the quiescent current can impact overall the overall power converter efficiency. The active pre-charge method does however not require any additional external components compared to the passive start-up method.

## 5.3 A fully-integrated active pre-charge circuit for safe start-up for high-voltage switched-capacitor converters

To verify that a safe start-up strategy can be implemented for highly-integrated switched-capacitor converters an active pre-charge circuit similar to that of Fig. 5.12 was fabricated in a 180 nm SOI-BCD process. The whole active pre-charge circuit, including a resistor string consisting of 4 resistors with a total series resistance of 460 k$\Omega$, was implemented based on three identical active pre-charge circuit blocks using a shunt regulator to pre-charge the external flying capacitors.

An experimental baseline of no start-up strategy is not measured, since it would be damaging to the IC. Therefore, as a baseline, the simulated 40 A peak inrush currents presented in section 5.1.2 is used as comparison for the experimental measurement results.

This section is a more detailed description of the experimental results presented in the publication shown in Appendix B, which was authored as a part of the Ph.D. project.

### 5.3.1 Verification setup

For the experimental verification of the active pre-charge circuit a protoptype test PCB was made implementing a 48 V-12 V highly-integrated switched-capacitor converter with an integrated power-stage and active pre-charge circuit and external flying capacitors.

The prototype test PCB can be seen in Fig. 5.16. The test PCB includes measurement loops between the flying capacitors and the IC to investigate the peak inrush currents as

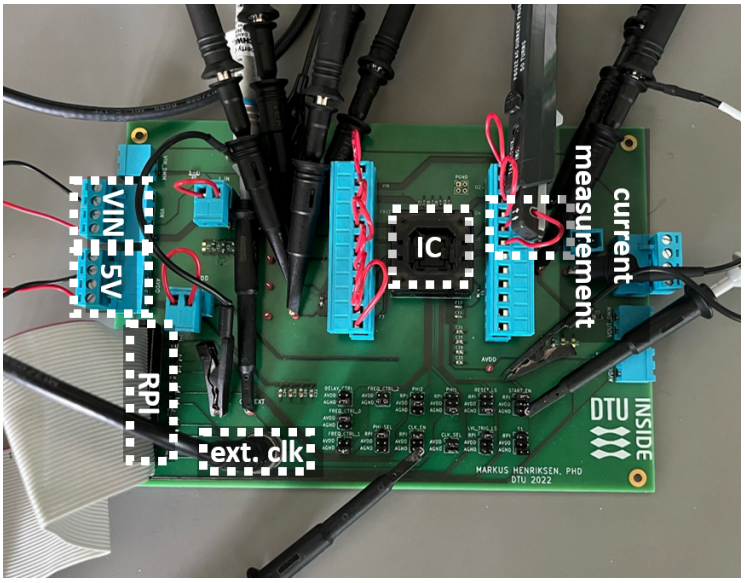



Figure 5.16: Photo of measurement setup used for experimental verification of the active pre-charge circuit safe start-up method.

the power converter clock is enabled after safe start-up operation. A Tektronix P6022 120 MHz current probe clamp is used for the current waveform measurements. The current loops does add additional series inductance and resistance to the power converter, which effects the peak inrush currents. Therefore, it is important to also measure all the switching node voltages during the input voltage ramp-up as well, to ensure that the active pre-charge circuit charges the flying capacitors to the desired steady-state voltages. All the voltage nodes of the switched-capacitor converter is measured together with the clock enable bit ($clk_{en}$) and the start-up enable bit ($s_{en}$). An external clock generator is used for generating the power converter system clock. A 64-pin IC socket is used as interconnection between the fabricated IC and the prototype test PCB. This socket introduces additional series resistance and inductance.

An overview of the experimental verification measurement setup can be seen in Fig. 5.17. The verification is controlled by a Python script interfacing with two source measurement units (SMUs) supplying the input voltage and the digital 5 V supply. A Raspberry Pi is used to generate the chip control signals and disable the start-up control bit $s_{en}$ just before the clock signal is enabled.

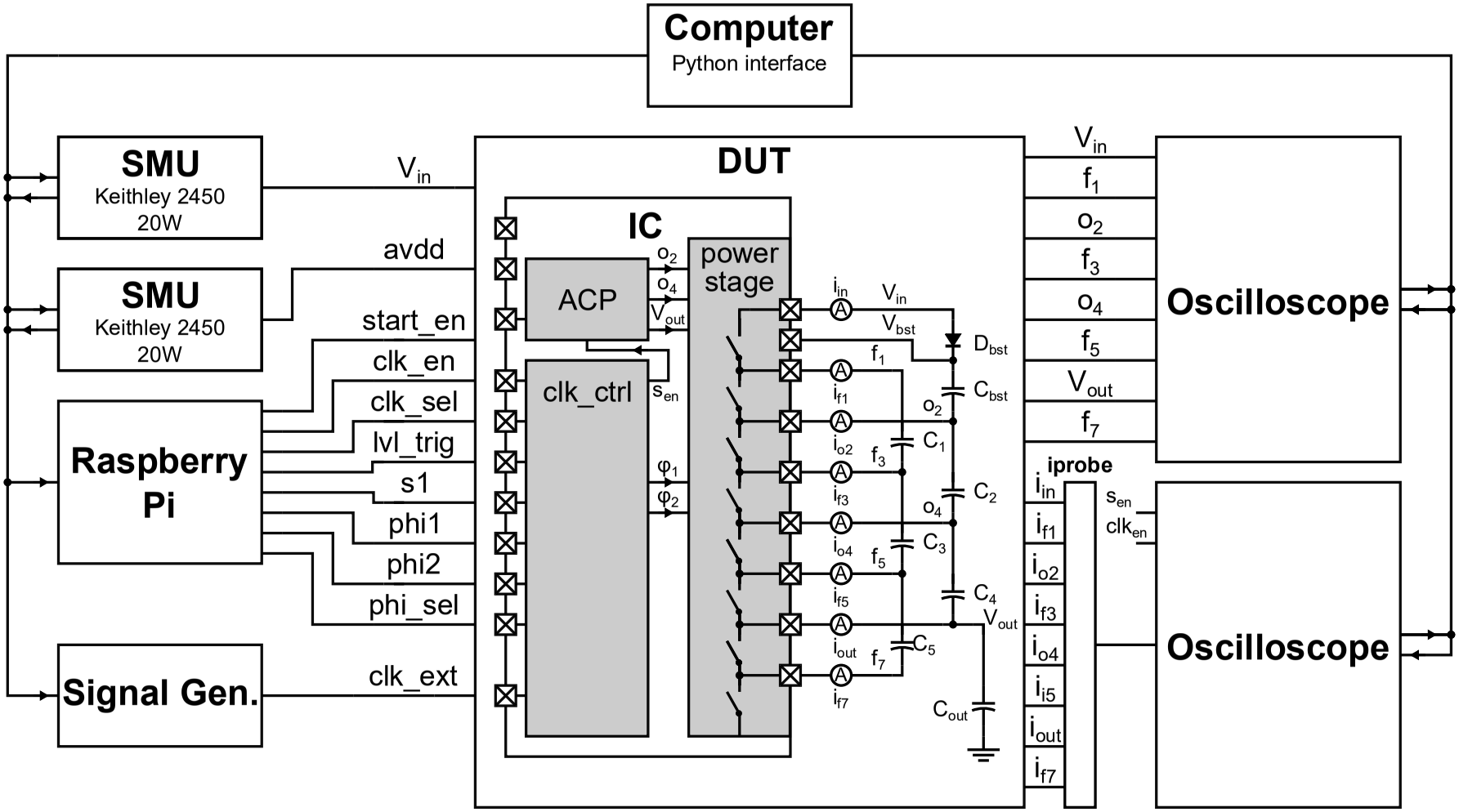



Figure 5.17: Illustration of the whole automated measurement setup controlled by a Python script from a laptop.

### 5.3.2 Experimental results

The experimental measurements shown here focuses on capturing both the voltage nodes of the highly-integrated switched-capacitor converter and capture the peak inrush current as the converter was enabled, hereby verifying the concept of the active pre-charge circuit start-up strategy to ensure safe start-up for switched-capacitor converters.

A die photo showing the fabricated IC prototype consisting of the integrated gate-drivers, switches and active pre-charge circuit can be seen in Fig. 5.18. An exploded view showing the layout of the full active pre-charge circuit can also be seen. The dimensions of the integrated active pre-charge circuit is 911 µm $\times$ 743 µm. The pass transistor of the three identical active pre-charge circuit blocks are sized such, that it is able to charge the external flying capacitors as the input voltage ramps up, without experiencing any slew rate limitations. A 60 V device has been used for the pass device, such that it is able to tolerate the full input voltage.

Careful matching for the layout of the resistor string has been made to ensure, that the local mismatch does not alter the reference voltages for the active pre-charge significantly.

In Fig. 5.19 the measured voltage nodes of the 48 V-12 V highly-integrated switched-capacitor converter prototype using an active pre-charge circuit method to ensure safe start-up can be seen for an input voltage ramp with a 8.5 ms rise-time.

From Fig. 5.19 it can be seen that all the flying nodes are being charged to the desired steady-state voltages and that for a 8.5 ms rise-time, the active pre-charge circuit is able to charge the external flying capacitors without slewing. This verifies the functionality of the designed active pre-charge circuit blocks to ensure that the maximum voltage ratings of the integrated switches and the flying capacitors are not exceeded during start-up.

In order to investigate the peak inrush current the current flowing into the $f_7$ node of the IC is measured using the Tektronix P6022 current probe clamp is used to capture the inrush current waveform as the power converter clock is enabled. The $f_7$ node is chosen,

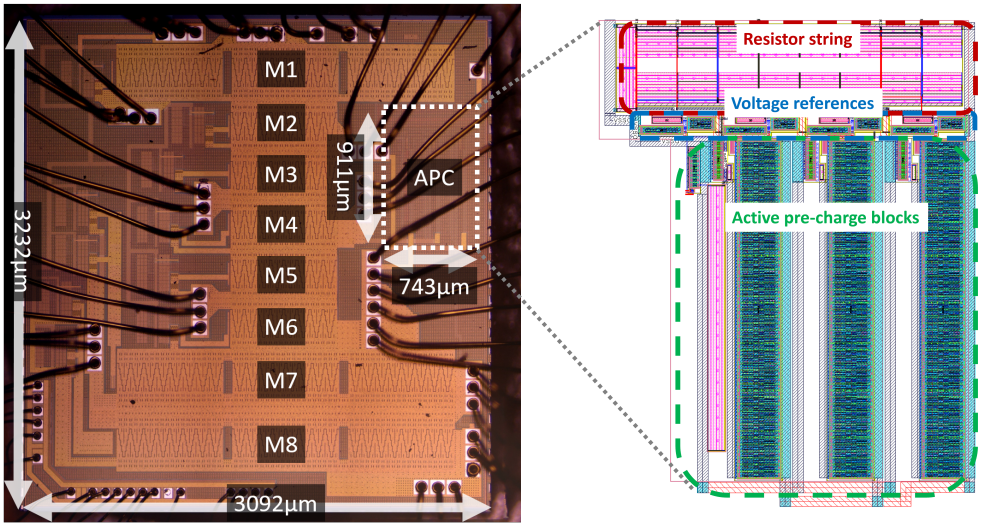



Figure 5.18: Die photo of the fabricated 48 V-12 V showing the active pre-charge circuit to ensure safe start-up together with an exploded view showing the layout of the active pre-charge circuit.

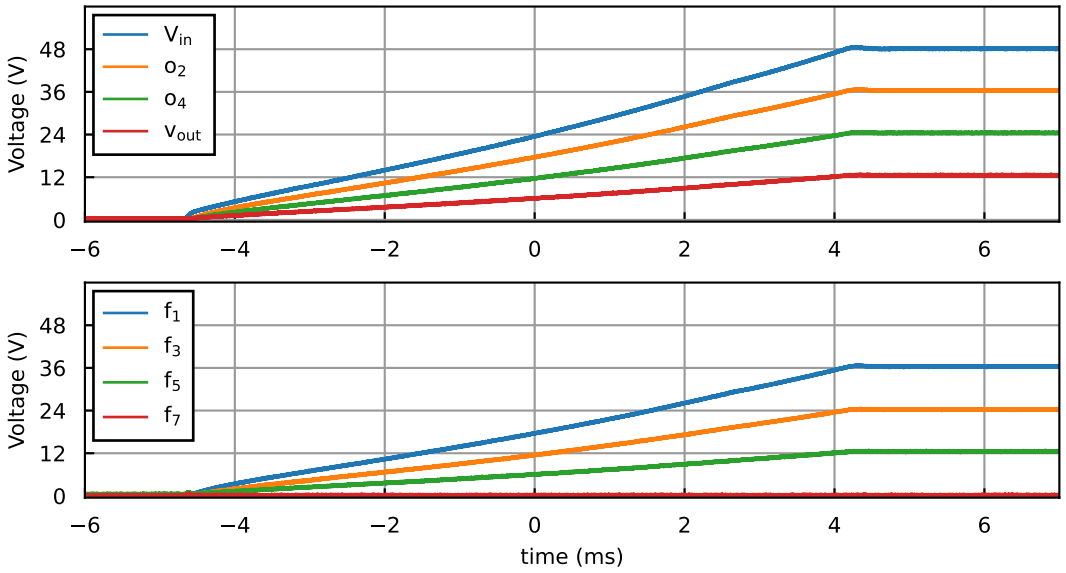



Figure 5.19: Measured switched-capacitor voltage nodes during start-up with active pre-charge circuit enabled.

since this is where simulation and analysis shows that the maximum peak current should occur according to the charge multiplier vector for a 4:1 Ladder topology. The current waveform can be seen together with the start-up control bit $s_{en}$ and the power converter clock enable signal $clk_{en}$ in Fig. 5.20. The measurement shows, that a peak current of only 534 mA flows into $f_7$. The current waveform settles to its steady-state peak current of below 100 mA within seven switching periods.

The prototype verifies that an active pre-charge circuit can be used to ensure safe start-up of highly-integrated switched-capacitor converters. The quiescent current of the active

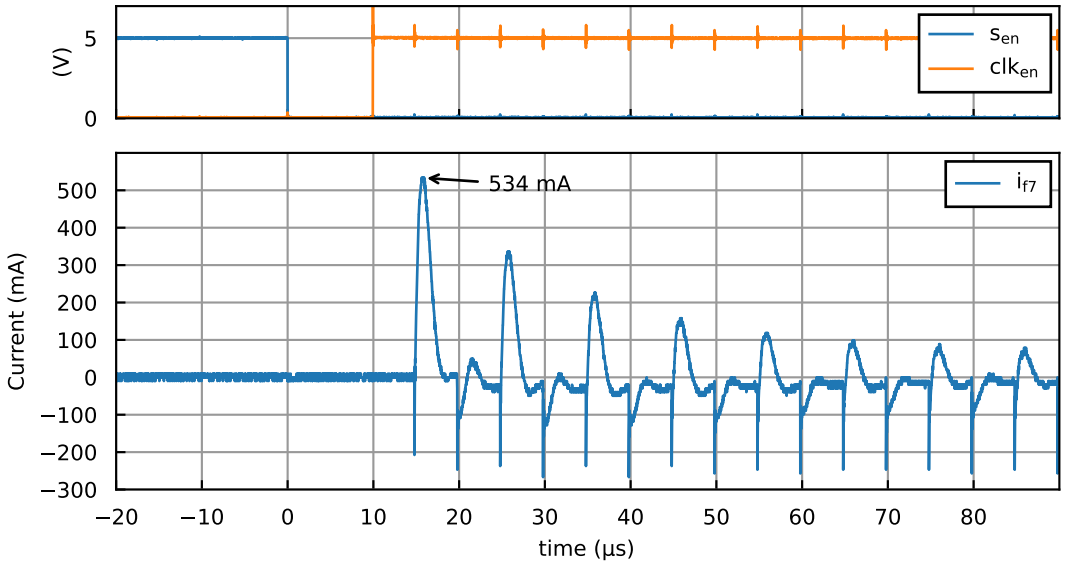



Figure 5.20: Measured current flowing into $f_7$ during first switching cycles after safe start-up.

pre-charge circuit is 105 µA, which has very little impact on the overall energy efficiency of the designed power converter. The active pre-charge circuit is also able to ensure that the maximum voltage ratings of the flying capacitors and integrated switches are not exceeded. Comparing the measurement results of the current waveform to the simulated currents in Fig. 5.15 it can be seen, that the settling time for the peak current is much longer. This indicates that the inductance and resistance is significantly higher for the prototype PCB board, than what was estimated in the initial simulations. This increase in inductance and resistance also assists in lowering the overall peak current.

### 5.3.3 Discussion of experimental results and additional findings

Table 5.1: Summary of active pre-charge circuit experimental results.

| Quies. current (sim.) | Rated voltage | Area | Peak inrush current |
|---|---|---|---|
| 105 µA | 60 V | 911 µm × 734 µm = 0.67 mm$^2$ | 534 mA |

The proposed active pre-charge circuit has been verified through experimental results to achieve safe start-up of the highly-integrated 48 V-12 V switched-capacitor converter. No baseline without the active pre-charge circuit method has been measured, since this is damaging to the IC. The simulation results indicate that peak currents of above 40 A can be expected without a safe start-up strategy. These peak currents would be damaging to the IC and bonding wires used for the interconnection between the die and the QFN64 package. The prototype test PCB board does however introduce additional series resistance and inductance due to the current measurement loops, which would lower these peak currents compared to the simulation results. A summary of the performance of the active pre-charge circuit can be seen in Table 5.1.

During the experimental verification it was discovered, that the active pre-charge circuit would sometimes fail in charging the flying capacitors during start-up after repeated use. After various testing the strongest current hypothesis is that during the shut-down sequence, the designed active pre-charge circuit will sometimes be damaged. The shut-down was not properly taken into account during the design phase of the active pre-charge circuit and simulation results show, that some of the voltage ratings of the pre-charge circuit blocks are exceeded during shut-down, which is the cause of reason to speculate, why the shut-down might be the issue.

The shut-down needs to be handled in the design phase of the active pre-charge circuit blocks, such that robust repeated start-up sequences can be verified and achieved.

## 5.4 Summary

In this chapter, the two main general challenges of ensuring safe start-up for switched-capacitor converters was presented. These two challenges are ensuring that the maximum voltage ratings of the discrete flying capacitors and integrated switches are not exceeded as the input voltage ramps up, and that the peak inrush currents that occur during the first switching periods do not exceed the maximum ratings of the chip packaging and the IC itself.

These two challenges were assessed based on simulation results of a 48 V-12 V highly-integrated Ladder switched-capacitor converter, were no start-up strategy was used. This verified the requirement for a dedicated start-up strategy to ensure safe start-up.

Three safe start-up strategies were presented and simulation results of these were shown

in order to evaluate their performance. The three strategies presented are; a passive start-up strategy using a discrete capacitor connected to the input voltage, a switch-conductance control strategy limiting the inrush currents of the converter by using high on-state resistance switches during start-up and an active pre-charge circuit strategy were a fully-integrated regulator network charges the flying capacitors to their desired steady-state voltages before the power converter is enabled.

To verify the possibility of achieving safe start-up of a highly-integrated switched-capacitor converter an active pre-charge circuit was implemented in a 180 nm SOI-BCD process together with the 48 V-12 V highly-integrated switched-capacitor converter presented in section 4.4.4. Experimental results of the active pre-charge circuit start-up strategy showed that the flying capacitors were all charged to their desired steady-state voltages and the resulting peak inrush current were measured to be only 534 mA.

# 6 Hybrid switched-capacitor converters

In this chapter, the operation and analysis of the hybrid switched-capacitor converter is described. This includes a description of soft-charging of the flying capacitors and determining the output resistance of these converters. A visual multi-step approach of determining the soft-charging capabilities of hybrid switched-capacitor converters is explained and presented by examples. This description of the visual multi-step approach for determining soft-charging is an expanded description based on the publication shown in Appendix D, which was authored as a part of the Ph.D. project.

A brief discussion on the impact of non-idealities on hybrid switched-capacitor converters is also shown and demonstrated with a combination of modeling and simulation results.

## 6.1 Fundamental analysis of hybrid switched-capacitor converters

Hybrid switched-capacitor converters consists of a switched-capacitor converter topology with one or multiple inductors inserted to combine the lower voltage requirement benefits for the switches and flying capacitors with the output voltage regulation and efficiency benefits of traditional inductor-based converters. Note, that this significantly increases the topology space of switched-capacitor converters, since every topology can have different placements of local or distributed inductors, which have various benefits and downsides depending on the application and implementation.

The hybrid converters discussed in this chapter are all step-down converters, but step-up conversion can also be achieved using hybrid switched-capacitor converters.

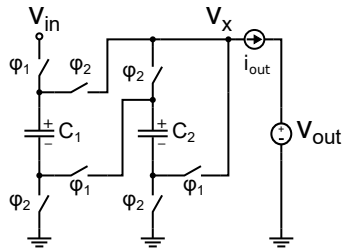
### 6.1.1 Soft-charging in hybrid switched-capacitor converters

The switched-capacitor converter can achieve great efficiency and power density for large voltage conversion ratios due to the effective use of both switches and flying capacitors with lower voltage ratings. However, the switched-capacitor converter does require high switching frequencies or large external flying capacitors to achieve low output resistance $R_{out}$ [73]. This is due to the charge redistribution losses between the flying capacitors, which happens because of their voltage mismatch. This operation of the switched-capacitor converter is referred to as hard-charging of the flying capacitors [91].

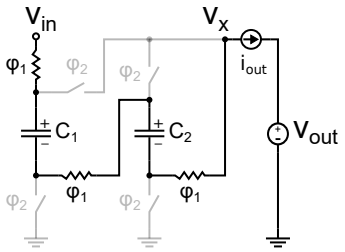
Consider the 3:1 series-parallel switched-capacitor converter in Fig. 6.1 with an added constant current source in series with the output. The two phases $\varphi_1$ and $\varphi_2$ and their equivalent phase networks is also shown in Fig. 6.1b and Fig. 6.1c respectively. The flying capacitors are charged/discharged through a constant current source instead of a voltage source, such as for the case with the idealized switched-capacitor converter case explained in chapter 3. This means, that the capacitor voltages are charged/discharged by:

$$\begin{aligned} \Delta V_{c,i}^{1} &= \frac{1}{C_i} \int_{t=0}^{T_1} i_{out}\, dt \\ \Delta V_{c,i}^{2} &= -\frac{1}{C_i} \int_{t=0}^{T_2} i_{out}\, dt \end{aligned} \tag{6.1}$$

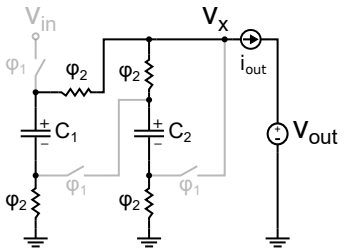
where $\Delta V_{c,i}^{1}$ and $\Delta V_{c,i}^{2}$ is the voltage change of capacitor $i$ during phase 1 and phase 2 respectively. $T_1$ and $T_2$ are the phase time durations, where $T_{sw} = T_1 + T_2$. For steady-state operation of the hybrid converter it also holds that $\Delta V_{c,i}^{1} + \Delta V_{c,i}^{2} = 0$.




(a) 3:1 hybrid Series-Parallel converter topology.

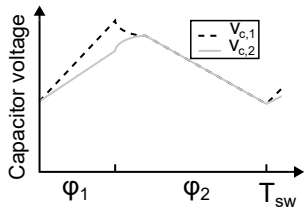



(b) 3:1 hybrid Series-Parallel converter topology during phase 1.

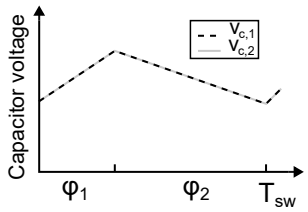



(c) 3:1 hybrid Series-Parallel converter topology during phase 2.

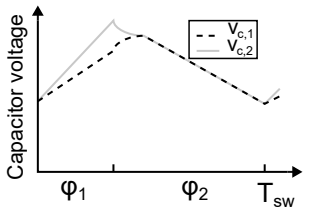
Figure 6.1: 3:1 hybrid Series-Parallel converter topology with a constant current source in series with the output and its equivalent phase networks.



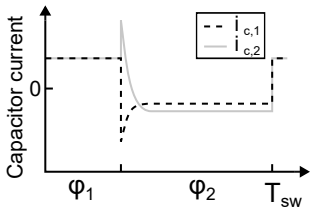

(a) 3:1 Series-Parallel capacitor voltages with $C_1 < C_2$.



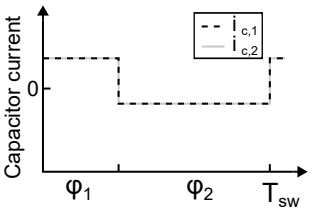

(b) 3:1 Series-Parallel capacitor voltages with $C_1 = C_2$.



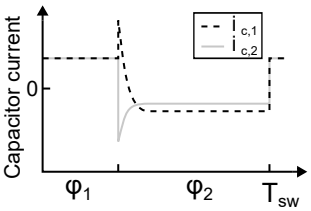

(c) 3:1 Series-Parallel capacitor voltages with $C_1 < C_2$.




(d) 3:1 Series-Parallel capacitor currents with $C_1 < C_2$.




(e) 3:1 Series-Parallel capacitor currents with $C_1 = C_2$.




(f) 3:1 Series-Parallel capacitor currents with $C_1 > C_2$.

Figure 6.2: Capacitor voltage and current waveforms for the 3:1 hybrid Series-Parallel converter for different capacitor size conditions.

The benefit of charging the capacitors through a constant current source, is that the voltage at $V_x$ can change instantaneously, compared to the pure switched-capacitor converter case, where it is tied to the output voltage source (or large DC decoupling capacitor). Therefore, if we can charge the flying capacitors to exactly the same voltage before connecting them in parallel, there will be no voltage mismatch and therefore no charge redistribution losses.

Looking at the 3:1 hybrid Series-Parallel converter in Fig. 6.1 it can be seen, that since both $C_1$ and $C_2$ are charged by the same current during phase 1, in order to ensure that the voltage changes at the end of phase 1 ($\Delta V_{c,1}^1$, $\Delta V_{c,2}^1$) are equal, they need to have the same capacitance. Note, that the ideal constant current source allows for instantaneous voltage change at the switching node $V_x$, which is what decouples the two flying capacitors $C_1$ and $C_2$ from the output voltage source during phase 2.

The capacitor voltage and current waveforms for the 3:1 hybrid Series-Parallel converter is illustrated in Fig. 6.2 with three different capacitor sizing conditions. Here it can be seen, that when $C_1 \neq C_2$, voltage mismatch happens during the end of phase 1, which means that a current spike on both capacitors are seen due to charge redistribution.

In the case of $C_1 = C_2$, the charge redistribution losses are completely removed. In this case the $R_{SSL}$ of the hybrid switched-capacitor converter is $0\,\Omega$, meaning that the output resistance of the converter is only dependent on the conduction losses in the switches and has no frequency dependency. This is referred to as soft-charging and can greatly improve the power converter efficiency.

The phase timings are important in hybrid converters to ensure, that the capacitors are charged and discharged to the desired amount. The timings can be determined by the output charge in each phase:

$$\begin{aligned} D_1 &= T_1/T_{sw} = q_{out}^1/q_{out} \\ D_2 &= T_2/T_{sw} = q_{out}^2/q_{out} \end{aligned} \tag{6.2}$$

The soft-charging means that the voltage ripple on the capacitors is increased compared to the pure switched-capacitor converter. This also increases the voltage rating requirements for both the flying capacitors and the switches, since the switching node $V_x$, doesn't bound the voltages. The voltage ripple sets the sizing requirements on the flying capacitors, since it should be sized such that for maximum output current of the converter, the voltage ripple doesn't exceed the maximum voltage ratings of the flying capacitors and switches. This sizing requirement is still often much smaller, than the sizing requirements to ensure low $R_{SSL}$ at a reasonable switching frequency in a traditional switched-capacitor converter.

### 6.1.2 Determining slow-switching limit resistance of hybrid switched-capacitor converters

In other published works such as in [92] the output resistance of hybrid converters have been examined assuming that no charge redistribution losses occur leading to the $R_{SSL}$ of the converter being zero. This corresponds to the required capacitors being perfectly matched to their required scalings to achieve soft-charging. In this section the $R_{SSL}$ is examined and a method for determining it for hybrid converters with a constant current source in series with the output is presented. The motivation for this is to examine what happens, when the flying capacitors are not properly sized.

The $R_{SSL}$ of a hybrid converter can be determined by considering all energy lost as capacitor networks are connected in parallel for each phase. The approach is to determine parallel branches, the equivalent capacitance in these branches and the settling voltages as they are connected in all phases. The energy lost in the series resistances due to voltage mismatch can then be calculated for each branch by determining the energy available before the parallel connection:

$$E_{1,k}^j = \frac{1}{2} \sum_i^{N_{caps}} C_i \Delta V_{c,i}^2 \tag{6.3}$$

where $j$ is referring to the respective phase and $k$ is referring to the parallel branch. The energy available after the parallel connection is:

$$E_{2,k}^j = \frac{1}{2} C_{eq,k}^j (\Delta V_{ceq,k}^j)^2 \tag{6.4}$$

Both the equivalent capacitance $C_{eq}$ and the equivalent settling voltage $\Delta V_{c,eq}$ can be determine by circuit analysis. The energy loss $E_{loss,k}$ for each number of parallel connections of capacitors $k$ in a topology is then:

$$E^j_{loss,k} = E^j_{1,k} - E^j_{2,k} \tag{6.5}$$

And the total energy loss for the topology is:

$$E_{loss,tot} = \sum_{j}^{N_{phases}} \sum_{k} E^j_{loss,k} \tag{6.6}$$

The average power loss across a switching period is determined by:

$$P_{loss} = E_{loss,tot} f_{sw} \tag{6.7}$$

and the equivalent resistance can be determined by:

$$R_{ssl,sp31} = \frac{P_{loss}}{i^2_{out}} = \frac{P_{loss}}{(q_{out} f_{sw})^2} \tag{6.8}$$

**Slow-switching limit equivalent resistance of 3:1 hybrid Series-Parallel converter**

Consider again the 3:1 hybrid Series-Parallel converter in Fig. 6.1. To determine the equivalent output resistance due to charge redistribution losses ($R_{SSL}$) we consider the end of phase 1, just before the the two flying capacitors are connected in parallel in phase 2. Here only a single parallel branch exists and only in a single phase (phase 2). The energy loss in this case can be determined as:

$$E_{loss} = \frac{1}{2} \frac{C_1 C_2}{C_1 + C_2} (\Delta V^1_{c,1} - \Delta V^1_{c,2})^2 \tag{6.9}$$

where the capacitor voltage changes at the end of phase 1, which are charged by the constant current source can be expressed as:

$$\begin{aligned} \Delta V^1_{c,1} &= \frac{q^1_{c,1}}{C_1} = \frac{a^1_{c,1}}{C_1} q_{out} \\ \Delta V^1_{c,2} &= \frac{q^1_{c,2}}{C_2} = \frac{a^1_{c,2}}{C_2} q_{out} \end{aligned} \tag{6.10}$$

since the capacitor charge multiplier is defined as $a^1_{c,i} = \frac{q^1_{c,i}}{q_{out}}$. Note, that $q_{out} = q^1_{out} + q^2_{out}$. Meaning the total charge delivered to the load during the full switching period.

Note, that since the charge redistribution only happens during the transition from phase 1 to phase 2, the power loss is not multiplied by two.

The equivalent output resistance due to the charge redistribution losses can then be determined for the 3:1 Series-Parallel:

$$\begin{aligned} R_{SSL,sp31} &= \frac{P_{loss}}{i^2_{out}} = \frac{P_{loss}}{(q_{out} f_{sw})^2} \\ &= \frac{(a^1_{c,2} C_1 - a^1_{c,1} C_2)^2}{2 C_1 C_2 (C_1 + C_2) f_{sw}} \end{aligned} \tag{6.11}$$

From (6.11) it can be seen that in order, to achieve an $R_{SSL,sp31} = 0\,\Omega$, the following condition must be true:

$$a^1_{c,1} C_2 = a^1_{c,2} C_1 \tag{6.12}$$

since $a^1_{c,1} = a^1_{c,2} = \frac{1}{3}$ for the 3:1 Series-Parallel converter, this means that to ensure soft-charging $C_1 = C_2$ as expected.

## 6.2 Intuitive method for determining soft-charging capabilities in hybrid switched-capacitor converters

This section describes an intuitive, visual multi-step approach to determining the soft-charging capabilities of hybrid switched-capacitor converters. This section is in general a more detailed description of the work presented in the publication shown in Appendix D, which was authored as a part of the Ph.D. project.

In the case of the 3:1 Series-Parallel converter it was possible to find a sizing scheme of $C_1$ and $C_2$, which could ensure soft-charging. This is not always the case for all topologies with a single output inductor at the output. Some topologies such as the 4:1 Dickson and the 4:1 Ladder topology do not have a practical capacitor sizing to ensure no charge redistribution losses of the flying capacitors.

A method to determine whether a topology can achieve soft-charging was presented in [91]. It determines the soft-charging capabilities by describing the system equations of the phase networks of the topology and utilizing two additional constraints to solve the required capacitor scalings.

The two constraints, which ensures soft-charging in a hybrid converter are:

**Constraint (1) - flying capacitor voltage change**
The flying capacitor voltage change due to charge being delivered to the output load must sum to zero across a full switching cycle in steady-state operation:

$$\Delta V^1_{c,i} + \Delta V^2_{c,i} + \cdots + \Delta V^j_{c,i} = 0 \tag{6.13}$$

This constraint applies for all flying capacitors in the switched-capacitor converter.

Note, that this constraint is not fulfilled in the case of traditional switched-capacitor converters, since the flying capacitor network will always have a phase connected in parallel with the output voltage source (or a large DC decoupling capacitor). Since an ideal DC voltage source has no voltage change, the parallel flying capacitor network would have to also have no voltage change during the parallel phase, while delivering charge to the output. Therefore, the only solution for traditional switched-capacitor converters to (6.13) is the rather impractical solution of infinitely large capacitors since:

$$\Delta V_c = \frac{q_c}{C} \tag{6.14}$$

Constraint (1) is reformulation of the cause of the charge redistribution losses described in section 3.1.1.

**Constraint (2) - Kirchoff's voltage law**
The second constraint states that for each equivalent phase network, Kirchoff's voltage law (KVL) must hold in each loop of the topology:

$$\sum_{k} \Delta V_{c,i}^{k} = 0 \tag{6.15}$$

where $k$ is the different loops in the equivalent phase network. Note, that only the small-signal voltage changes are considered in this constraint. In reality the large signal behaviour of the hybrid converter does effect the soft-charging behaviour such as shown in [93], but for determining the soft-charging capabilities of a topology the large signals behaviour can be neglected.

Combining constraint (1) and (2) ensures that no voltage mismatch occurs for all flying capacitors in any topology [91]. While the work in [91] used linear algebra to solve the system equations of the equivalent phase networks using the presented constraints and then finding the resulting capacitor scalings, that ensures soft-charging this method is not approachable and does not provide a good intuition with the topology under analysis.

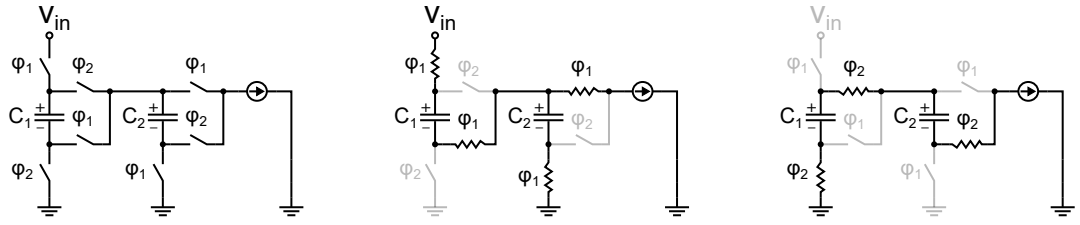
A more approachable method to determine if a hybrid converter can achieve soft-charging can instead be found by a visual multi-step approach inspired by what [75] presented for determining the charge multiplier vectors for any topology using an iterative approach. The method requires that the charge multiplier vector has been found previously and is based on analyzing the equivalent phase networks of the topology.

This visual multi-step approach to determine the soft-charging capabilities of a switched-capacitor topology is explained with the following examples.

### 6.2.1 Example 1: Determining the soft-charging capabilities of a 3:1 hybrid Fibonacci topology

The 3:1 hybrid Fibonacci switched-capacitor converter can be seen in Fig. 6.3 together with its equivalent phase networks in Fig. 6.3b and Fig. 6.3c for phase 1 and phase 2, respectively. The charge flow vectors for the 3:1 Fibonacci topology can be determined from a visual inspection of the phase networks as described in [75].

The soft-charging capability is now found by first choosing a starting point for the method similarly to charge flow analysis. A good starting point is usually a capacitor connected to the input voltage source in a phase. For this example $C_1$ is chosen during phase 1 as a suitable starting point. The method finds the normalized capacitor voltage changes as the flying capacitors are delivering charge to the constant output current source. The

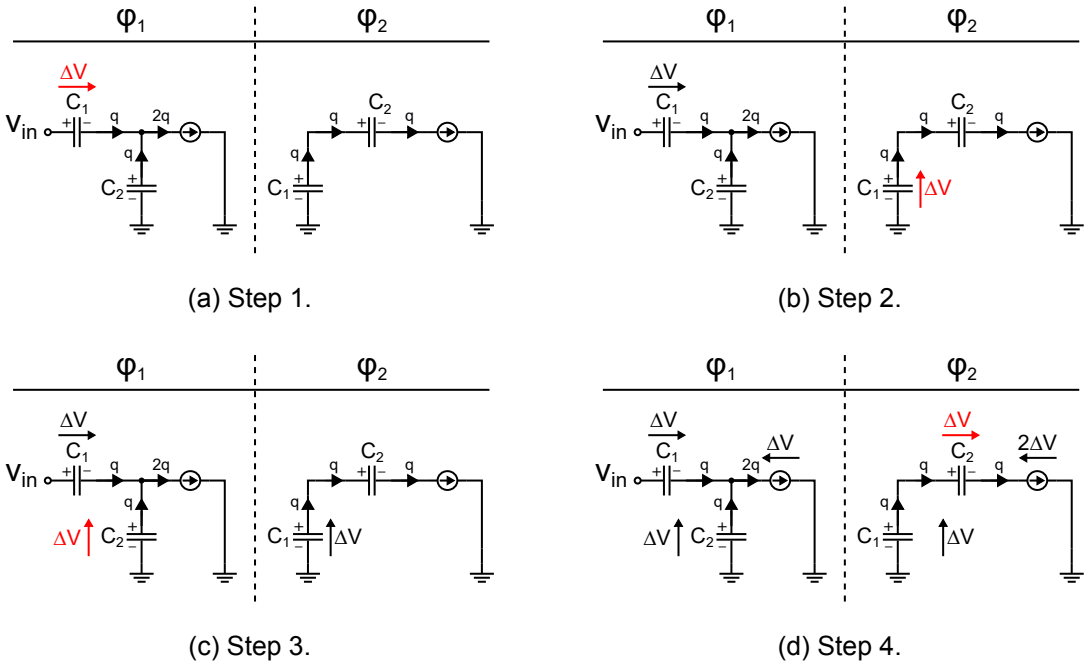



(a) 3:1 hybrid Fibonacci converter topology.

(b) 3:1 hybrid Fibonacci converter topology during phase 1.

(c) 3:1 hybrid Fibonacci converter topology during phase 2.

Figure 6.3: 3:1 hybrid Fibonacci topology and equivalent phase networks.




(a) Step 1.

(b) Step 2.

(c) Step 3.

(d) Step 4.

Figure 6.4: Determining the soft-charging capabilities of the 3:1 hybrid Fibonacci converter by visual inspection example.

normalized voltages are denoted $\Delta V$. Note, that as an ideal voltage source is assumed for the input voltage, there is no voltage change at $V_{in}$ leading to $\Delta V_{in} = 0$ for all phases. The visual multi-step approach for determining the soft-charging capabilities for the 3:1 hybrid Fibonacci converter is illustrated in Fig. 6.4 and can be done as follows:

**Step 1)** Phase 1: Charge flowing into the positive terminal of $C_1$ yields: $\Delta V_{c,1}^1 = +1\Delta V$ indicated across $C_1$ in Fig. 6.4a.

**Step 2)** Phase 2: Because of constraint (1): $\Delta V_{c,1}^2 = -1\Delta V$, i.e., the polarity of the voltage across $C_1$ changes (but not its absolute value). This is indicated across $C_1$ in phase 2 in Fig. 6.4b.

**Step 3)** Phase 1: KVL yields: $\Delta V_{c,2}^1 = \Delta V_{in}^1 - \Delta V_{c,1}^1 = -1\Delta V$. This is indicated across $C_2$ in Fig. 6.4c.

**Step 4)** Phase 2: Because of constraint (1) the polarity of $\Delta V_{c,2}$ changes with respect to phase 1 leading to: $\Delta V_{c,2}^2 = +1\Delta V$. This is indicated in Fig. 6.4d.

The resulting voltage changes for the 3:1 hybrid Fibonacci converter is therefore:

$$\mathbf{\Delta V^1} = \begin{bmatrix} \Delta V_{in}^1 \\ \Delta V_{c,1}^1 \\ \Delta V_{c,2}^1 \\ \Delta V_{out}^1 \end{bmatrix} = \begin{bmatrix} +0 \\ +1 \\ -1 \\ -1 \end{bmatrix}, \quad \mathbf{\Delta V^2} = \begin{bmatrix} \Delta V_{in}^2 \\ \Delta V_{c,1}^2 \\ \Delta V_{c,2}^2 \\ \Delta V_{out}^2 \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \\ -2 \end{bmatrix} \tag{6.16}$$

The charge vectors for the 3:1 hybrid Fibonacci converter is:

$$\mathbf{q_c^1} = \begin{bmatrix} q_{in}^1 \\ q_{c,1}^1 \\ q_{c,2}^1 \\ q_{out}^1 \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \\ -1 \\ +2 \end{bmatrix}, \ \mathbf{q_c^2} = \begin{bmatrix} q_{in}^2 \\ q_{c,1}^2 \\ q_{c,2}^2 \\ q_{out}^2 \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \\ +1 \end{bmatrix} \tag{6.17}$$

We can now determine the required normalized capacitor scalings $K_{c,i}$ for each capacitor to achieve soft-charging for the 3:1 hybrid Fibonacci converter:

$$K_{c,i} = \frac{q_{c,i}}{\Delta V_{c,i}} \tag{6.18}$$

The resulting required capacitor scalings to achieve soft-charging for the 3:1 Fibonacci converter are then:

$$\mathbf{K_c} = \begin{bmatrix} K_{c,1} \\ K_{c,2} \end{bmatrix} = \begin{bmatrix} +1 \\ +1 \end{bmatrix} \tag{6.19}$$

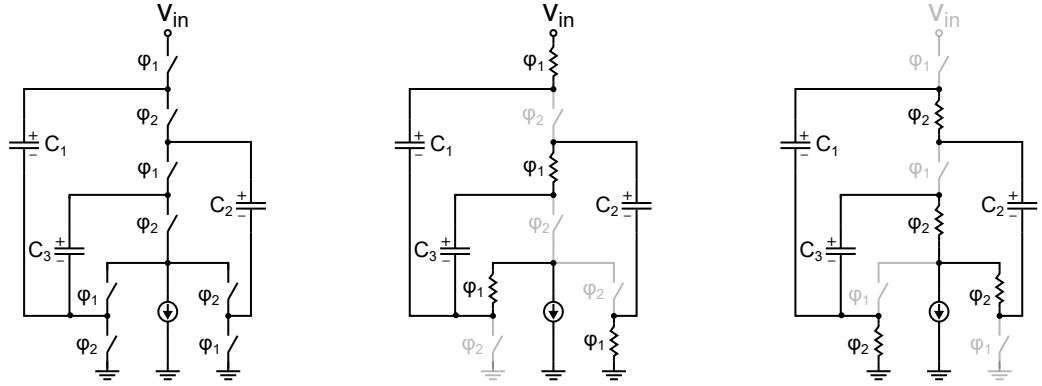
Meaning that in order to achieve soft-charging for the 3:1 Fibonacci converter $C_1 = C_2$ is required. Note, that signed capacitor scalings are used, since for some topologies negative scaling factors are required to achieve soft-charging. This is the case for the 4:1 Ladder and the 4:1 Cockcroft-Walton topology.

The method can be used for more complex topologies and for converters using more than just two phases. So far no topology has been encountered in which the soft-charging can not be determined by a visual multi-step approach. However, should a topology be encountered where this is the case, the method in [91] can be used instead.

### 6.2.2 Example 2: Determining the soft-charging capabilities of a 4:1 hybrid Dickson topology

Consider the 4:1 hybrid Dickson converter in Fig. 6.5 with its equivalent phase networks shown in Fig. 6.5b and Fig. 6.5c for phase 1 and phase 2, respectively.

From initially inspecting the equivalent phase networks in Fig. 6.5 it is unclear whether or not this topology can achieve soft-charging of the flying capacitors and what the required




(a) The 4:1 hybrid Dickson converter topology.

(b) The 4:1 hybrid Dickson converter topology during phase 1.

(c) The 4:1 hybrid Dickson converter topology during phase 2.

Figure 6.5: 4:1 hybrid Dickson topology and equivalent phase networks

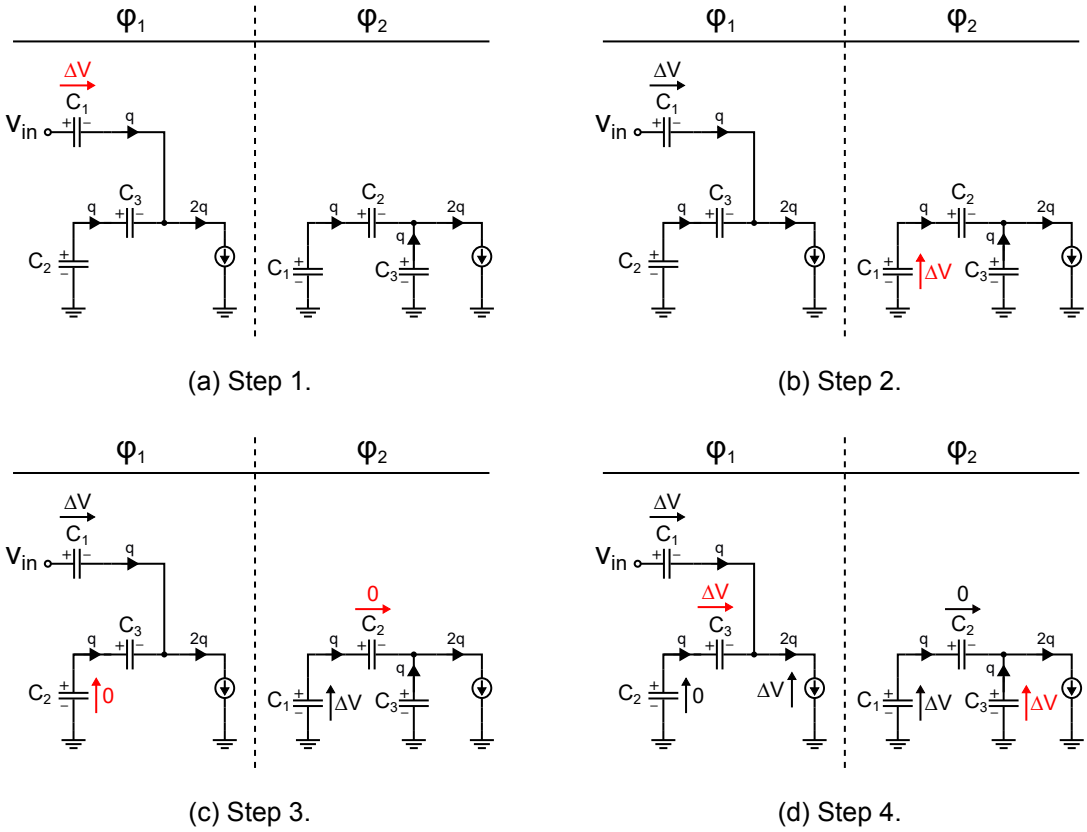



Figure 6.6: Determining the soft-charging capabilities of the 4:1 hybrid Dickson converter by visual inspection example.

capacitor scalings would be. Using the two constraints for determining soft-charging the capacitor voltage mismatches can be found in a few steps. The steps are illustrated in Fig. 6.6 and are performed as follows:

**Step 1)** Phase 1: Charge flowing into positive terminal of $C_1$ yields: $\Delta V_{c,1}^1 = +1\Delta V$. This is indicated in Fig. 6.6a.

**Step 2)** Phase 2: Constraint (1) yields: $\Delta V_{c,1}^2 = -1\Delta V$. This is indicated in Fig. 6.6b .

**Step 3)** Using constraint (2):

- KVL phase 1: $\Delta V_{c,1}^1 = \Delta V_{c,3}^1 - \Delta V_{c,2}^1$.
- KVL phase 2: $\Delta V_{c,1}^2 = \Delta V_{c,3}^2 + \Delta V_{c,2}^2$.
- Using this with constraint (1) yields: $\Delta V_{c,2}^1 = -0$ and $\Delta V_{c,2}^2 = +0$. This is indicated in Fig. 6.6c.

**Step 4)** Using constraint (2):

- Phase 2: Utilizing that $\Delta V_{c,2}^2 = +0$ yields for $\Delta V_{c,3}^2$: $\Delta V_{c,3}^2 = \Delta V_{c,1}^2 = -1\Delta V$.
- Phase 1: Constraint (1) yields: $\Delta V_{c,3}^1$ = $+1\Delta V$. This is indicated in Fig. 6.6d.

The resulting voltage changes for the 4:1 hybrid Dickson are then:

$$\mathbf{\Delta V^1} = \begin{bmatrix} \Delta V_{in}^1 \\ \Delta V_{c,1}^1 \\ \Delta V_{c,2}^1 \\ \Delta V_{c,3}^1 \\ \Delta V_{out}^1 \end{bmatrix} = \begin{bmatrix} +0 \\ +1 \\ -0 \\ +1 \\ -1 \end{bmatrix}, \ \mathbf{\Delta V^2} = \begin{bmatrix} \Delta V_{in}^2 \\ \Delta V_{c,1}^2 \\ \Delta V_{c,2}^2 \\ \Delta V_{c,3}^2 \\ \Delta V_{out}^2 \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +0 \\ -1 \\ -1 \end{bmatrix} \tag{6.20}$$

Note, that signed zeros are used for the voltage mismatch of $C_2$. This is important, since it otherwise can lead to wrong calculations of the capacitor scalings, which can be negative.

The capacitor charge flow vectors for the 4:1 hybrid Dickson topology is:

$$\mathbf{q_c^1} = \begin{bmatrix} q_{in}^1 \\ q_{c,1}^1 \\ q_{c,2}^1 \\ q_{c,3}^1 \\ q_{out}^1 \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \\ -1 \\ +1 \\ +2 \end{bmatrix}, \ \mathbf{q_c^2} = \begin{bmatrix} q_{in}^2 \\ q_{c,1}^2 \\ q_{c,2}^2 \\ q_{c,3}^2 \\ q_{out}^2 \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \\ -1 \\ +2 \end{bmatrix} \tag{6.21}$$

The resulting capacitor scalings for the 4:1 hybrid Dickson can then be determined:

$$\mathbf{K_c^1} = \begin{bmatrix} K_{c,1} \\ K_{c,2} \\ K_{c,3} \end{bmatrix} = \begin{bmatrix} +1 \\ +\infty \\ +1 \end{bmatrix} \tag{6.22}$$

Meaning that $C_1 = C_3$ and that $C_2 = +\infty \cdot C_1$. This shows that the 4:1 Dickson can only achieve soft-charging if $C_2$ is acting like an ideal voltage source (or infinite capacitance) leading to no voltage change as it is being charged or discharged. Therefore, soft-charging of the flying capacitors is not possible and charge redistribution losses will occur in the 4:1 hybrid Dickson converter. Nevertheless, the $R_{SSL}$ is lowered compared to that of a traditional switched-capacitor converter [91], since the voltage mismatch will be lower for the same capacitor sizes and switching frequency compared to the traditional switched-capacitor converter case.

Using the presented method in section 6.1.2 to determine the equivalent output resistance due to charge redistribution losses for hybrid converters, the $R_{SSL}$ of the 4:1 hybrid

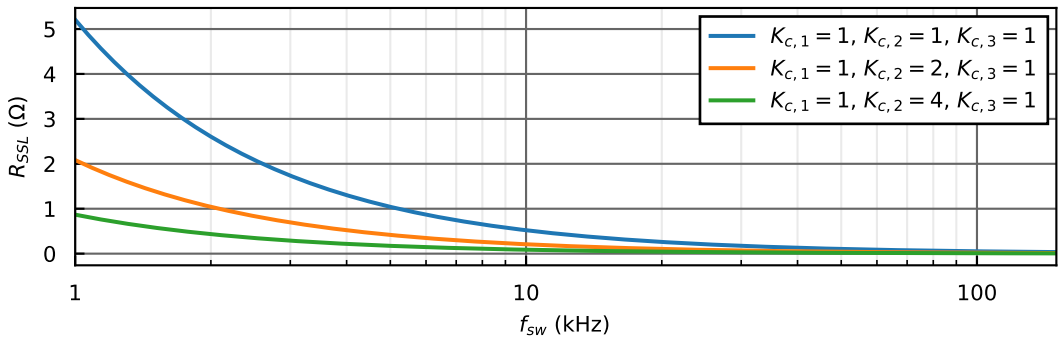



Figure 6.7: Calculated $R_{SSL}$ of 4:1 hybrid Dickson converter for different scaling factors $K_{c,i}$.

Dickson for increasing values of $K_{c,2}$ can be determined. The $R_{SSL}$ across switching frequency $f_{sw}$ can be seen in Fig. 6.7. The total capacitance is kept the same of $C_{tot} = 3\,\mu$F for all three calculations.

From Fig. 6.7 it can be seen, that the $R_{SSL}$ does decrease as $K_{c,2}$ increases as expected from the result of the visual inspection method.

### 6.2.3 Soft-charging capabilities of hybrid Dickson converter for different conversion ratios

In this section it is shown that for the hybrid Dickson topology, its soft-charging capabilities depend on the conversion ratio.

For all odd conversion ratio implementations of the Dickson topology, it is possible to find a capacitor scaling vector to achieve soft-charging, while for all even conversion ratios it requires one or more capacitors to be infinitely large, as for the 4:1 hybrid Dickson. This conversion ratio dependency of soft-charging for the hybrid Dickson converter has also recently been mentioned in [93].

The resulting voltage mismatch vectors and capacitor scalings vectors for the 5:1 Dickson, 6:1 Dickson and the 7:1 Dickson can be seen in Fig. 6.8. Here the calculated $R_{SSL}$ values for each conversion ratio across switching frequency can also be seen. The $R_{SSL}$ has been calculated using the presented method in section 6.1.2. The total capacitance is kept the same of $C_{tot} = 3\,\mu$F for all conversion ratios. For the even ratio conversion ratio, the capacitors that are required to be infinite, has a scaling factor of 4 times larger than the other flying capacitors instead.

The $R_{SSL}$ plot in Fig. 6.8d confirms, that the soft-charging capabilities are dependent on the conversion ratio for the hybrid Dickson topology. Furthermore, it can be seen that the flying capacitor scalings start becoming more complex to implement as the conversion ratio is increased, since the required flying capacitor scalings to achieve soft-charging become non-integers.

If identical discrete external capacitors are used for the flying capacitors for the hybrid converter the capacitor scaling to achieve soft-charging must be expanded to nearest all integer values. For the 7:1 hybrid Dickson converter this leads to the following required capacitor scaling to achieve soft-charging:

$$\mathbf{K_c} = \begin{bmatrix} 2 \\ 6 \\ 3 \\ 3 \\ 6 \\ 2 \end{bmatrix} \tag{6.23}$$

Meaning that a total of 22 unit capacitors are required to ensure soft-charging for the 7:1 hybrid converter, when identical unit capacitors are used to realize the flying capacitors.

If non identical flying capacitors are used, then matching the capacitor values to exactly the required capacitor scalings is difficult to achieve, which leads to voltage mismatch in the converter and therefore an increase in $R_{SSL}$.

$$\mathbf{\Delta V^1} = \begin{bmatrix} +1 \\ -0.5 \\ +0.5 \\ -1 \end{bmatrix}, \; \mathbf{\Delta V^2} = \begin{bmatrix} -1 \\ +0.5 \\ -0.5 \\ +1 \end{bmatrix},$$

$$\mathbf{K_c} = \begin{bmatrix} 1 \\ 2 \\ 2 \\ 1 \end{bmatrix}$$

(a) Voltage changes for each phase and required capacitor values for the 5:1 hybrid Dickson.

$$\mathbf{\Delta V^1} = \begin{bmatrix} +1 \\ -0 \\ +1 \\ -0 \\ +1 \end{bmatrix}, \; \mathbf{\Delta V^2} = \begin{bmatrix} -1 \\ +0 \\ -1 \\ +0 \\ -1 \end{bmatrix},$$

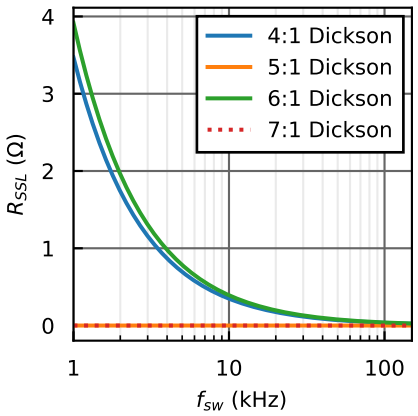
$$\mathbf{K_c} = \begin{bmatrix} 1 \\ \infty \\ 1 \\ \infty \\ 1 \end{bmatrix}$$

(b) Voltage changes for each phase and required capacitor values for the 6:1 hybrid Dickson.

$$\mathbf{\Delta V^1} = \begin{bmatrix} +1 \\ -1/3 \\ +2/3 \\ -2/3 \\ +1/3 \\ -1 \end{bmatrix}, \; \mathbf{\Delta V^2} = \begin{bmatrix} -1 \\ +1/3 \\ -2/3 \\ +2/3 \\ -1/3 \\ +1 \end{bmatrix},$$

$$\mathbf{K_c} = \begin{bmatrix} 1 \\ 3 \\ 3/2 \\ 3/2 \\ 3 \\ 1 \end{bmatrix}$$

(c) Voltage changes for each phase and required capacitor values for the 7:1 hybrid Dickson converter.




(d) Calculated $R_{SSL}$ for 4 different conversion ratios of the hybrid Dickson converter.

Figure 6.8: The voltage changes and capacitor scalings required for soft-charging for the 5:1, 6:1 and 7:1 hybrid Dickson topology using only two phases together with the calculated $R_{SSL}$ for each conversion ratio.

## 6.3 Non-ideality challenges of achieving soft-charging in hybrid switched-capacitor converters

So far perfect matching of the capacitors and an ideal current source at the output has been assumed for the sake of simplicity in the analysis of hybrid switched-capacitor converters. This section describes how capacitor mismatch can effect the soft-charging capabilities of a hybrid converter. This is shown by a statistical analysis for a 5:1 hybrid Dickson converter, where the flying capacitors are given a stochastic variation to examine the impact of capacitor mismatch on the soft-charging capabilities of a hybrid converter.

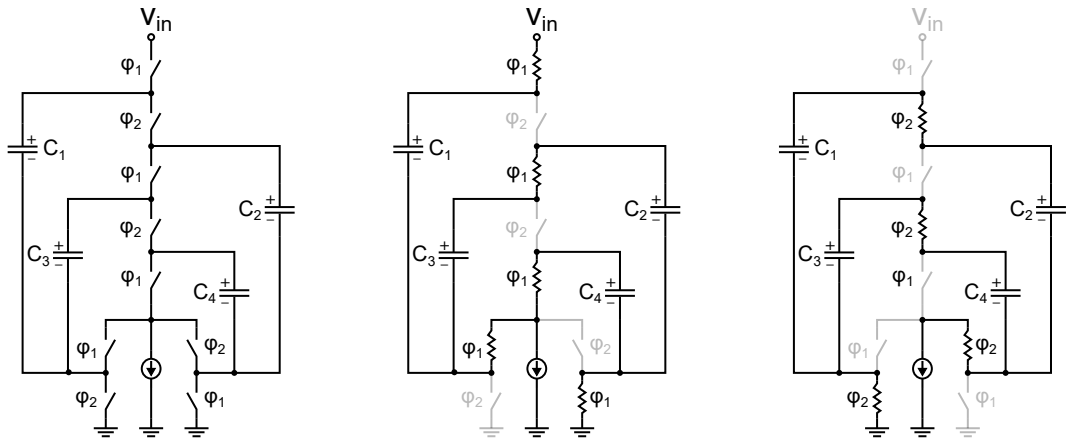
Furthermore, split-phase control, which was first presented in [91] is presented and described. The split-phase method can enable soft-charging for hybrid Dickson converters with an even conversion ratio by adding two additional switching phases. The required split-phase timings for all switching phases to achieve soft-charging are determined for a 4:1 hybrid Dickson converter using the visual multi-step approach presented in section 6.2. The description for determining the split-phase timings using the visual multi-step approach for the 4:1 hybrid Dickson converter is an expanded explanation based on the publication shown in Appendix D, which was authored as a part of the Ph.D. project.

Furthermore, the effect of realizing the constant current source by using an inductor is described and simulation results of the output resistance and transient waveforms of a 2:1 hybrid Series-Parallel converter is presented.

### 6.3.1 Impact of capacitor variations on soft-charging capabilities for hybrid converters

While the addition of a constant current source in series with the output of some switched-capacitor topologies enables soft-charging of the flying capacitors, for most topologies this requires exact matching of the capacitors. To investigate, how capacitor voltage mismatch can impact the soft-charging capabilities of a hybrid switched-capacitor converter, consider the 5:1 hybrid Dickson converter in Fig. 6.9 and its equivalent phase networks in Fig. 6.9b and Fig. 6.9c for phase 1 and 2 respectively.

The required capacitor scalings for the 5:1 hybrid converter to achieve soft-charging of the flying capacitors is shown in Fig. 6.8a but is repeated here for convenience:




(a) 5:1 hybrid Dickson converter topology.

(b) 5:1 hybrid Dickson converter topology during phase 1.

(c) 5:1 hybrid Dickson converter topology during phase 2.

Figure 6.9: The 5:1 hybrid Dickson converter and its equivalent phase networks.

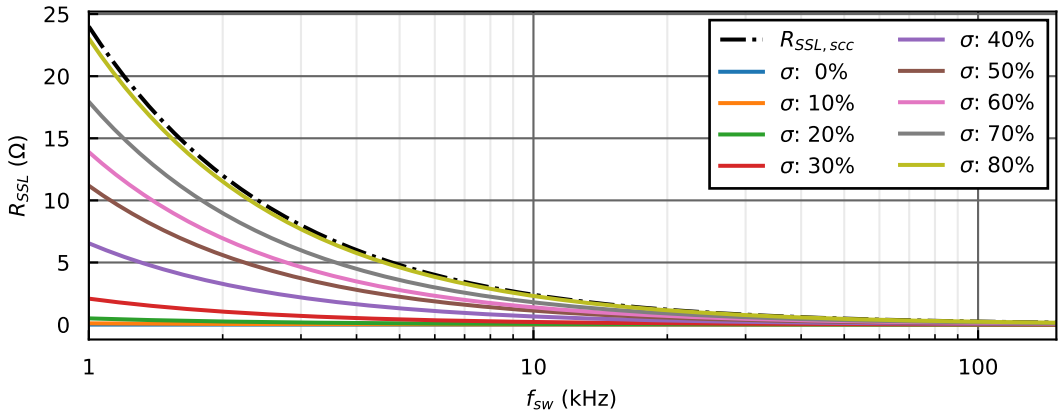



Figure 6.10: $R_{SSL}$ as a function of switching frequency for a 5:1 hybrid Dickson converter with different capacitor mismatches.

$$\mathbf{K_c} = \begin{bmatrix} K_{c,1} \\ K_{c,2} \\ K_{c,3} \\ K_{c,4} \end{bmatrix} = \begin{bmatrix} 1 \\ 2 \\ 2 \\ 1 \end{bmatrix} \tag{6.24}$$

Now consider a capacitor mismatch with a normal distribution with an mean value of 0 and a standard deviation of $\sigma$. These variations will lead to a violation of the required capacitor scalings and charge redistribution losses will occur. To analyze how these variations could impact the $R_{SSL}$ a statistical analysis has been made where all capacitors are scaled by:

$$C_i = C_{unit} \cdot K_{c,i} \cdot (1 + \mathcal{N}(0, \sigma^2)) \tag{6.25}$$

The $R_{SSL}$ of the 5:1 hybrid converter is then calculated for different values of $\sigma$ to investigate hos this impact the $R_{SSL}$. Since the capacitor values are now stochastic, 1000 simulations are run for each standard deviation value so as to lower the standard error. For the calculation a truncated normal distribution is used with values between -1 and 1.

The result of these calculations can be seen in Fig. 6.10 with standard deviation from 0 %-80 % and across switching frequency. The $R_{SSL}$ of a typical 5:1 Dickson switched-capacitor converter is also included for comparison. The unit capacitance $C_{unit}$ used for the calculations is 5 µF leading to an average total capacitance used of 30 µF.

For the 5:1 Dickson it can be seen, that the losses start increasing for standard deviations larger than 30 %. Tolerances for MLC capacitors are at most 20 % from production variation, but when considering that since the flying capacitors have to block different DC voltages, and therefore will have different capacitances due to DC bias voltage variations the mismatch can be much higher.

The results in Fig. 6.10 can not be used to predict the expected $R_{SSL}$ of the 5:1 hybrid Dickson converter, since that would need to include the implementation of the flying capacitors taking into account their exact values after DC bias derating. Still the results in Fig. 6.10 does show, that capacitor mismatch can become an issue and lead to the charge redistribution losses being on par with the normal switched-capacitor converter.

### 6.3.2 Split-phase control to ensure soft-charging of Dickson converters

A method for enabling soft-charging for the hybrid Dickson converter for any conversion ratio was first presented in [94]. Here soft-charging is achieved for the 4:1 hybrid Dickson converter by adding two additional switching phases. These two additional phases are referred to as split-phases. The 4:1 hybrid Dickson with split-phase control can be seen in Fig. 6.11. The two normal phases for the 4:1 Dickson converter is phase $\varphi_{1a}$ and $\varphi_{2a}$, where $\varphi_{1b}$ and $\varphi_{2b}$ are the split-phases. With the additional two phases there now exists infinite solutions to the capacitor charge vector analysis and thereby the voltage changes and capacitor scalings to ensure soft-charging.

Another way of expressing these infinite solution is, that for each capacitor scaling there exists a charge flow and voltage mismatch vector solution that ensures soft-charging. Remember that the charge flow is related to the phase time duration in terms of duty cycle as mentioned in section 6.1:

$$D^{\varphi,j} = \frac{q_{out}^{\varphi,j}}{q_{out}} \tag{6.26}$$

where $j$ is the respective switching phase and $q_{out} = \sum_j q_{out}^j$. The challenge is therefore, for a given desired capacitor scaling, to find the required phase timings to ensure soft-charging. For this the method presented in section 6.2 can be used again. The resulting capacitor charges and voltage changes for the case where $K_{c,1} = K_{c,2} = K_{c,3} = 1$ are also shown in Fig. 6.11. They are found with the following steps:

**Step 1)** Phase $\varphi_{1a}$: charge flowing into $C_1$ leads to a voltage change. Which is used as a suitable starting point and given the value of $2q$. With $K_{c,1} = 1$, this leads to a voltage change of $\Delta V_{c,1}^{1a} = 2\Delta V$.

**Step 2)** Phase $\varphi_{1a}$: Since $-q_{c,2}^{1a} = q_{c,3}^{1a}$, $K_{c,2} = K_{c,3}$ and $-\Delta V_{c,2} + \Delta V_{c,3} = \Delta V_{c,1} = 2\Delta V$, the voltage changes across $C_2$ and $C_3$ during phase $\varphi_{1a}$ must be: $\Delta V_{c,2}^{1a} = -\Delta V$, $\Delta V_{c,3}^{1a} = \Delta V$. Meaning that the charge in $C_2$ and $C_3$ during phase $\varphi_{1a}$ is then: $q_{c,2}^{1a} = -1q$, $q_{c,3}^{1a} = 1q$.

**Step 3)**

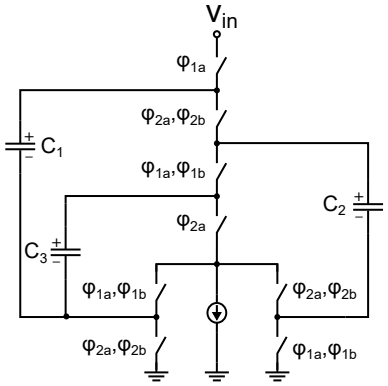
- Due to constraint (1): $\Delta V_{c,1}^{1a} = -(\Delta V_{c,1}^{2a} + \Delta V_{c,1}^{2b}) = 2\Delta V$.
- Since $-q_{c,1}^{2a} = q_{c,2}^{2a}$ and $-q_{c,1}^{2b} = q_{c,2}^{2b}$ and $K_{c,1} = K_{c,2}$ the voltage changes of $C_2$ in phase $\varphi_{2a}$ and $\varphi_{2b}$ must be: $\Delta V_{c,2}^{2a} + \Delta V_{c,2}^{2b} = 2\Delta V$.
- Using constraint (1) we can then find the voltage change for $C_2$ in phase $\varphi_{1b}$: $\Delta V_{c,2}^{1a} + \Delta V_{c,2}^{2a} + \Delta V_{c,2}^{2b} + \Delta V_{c,2}^{1b} = 0$. This means that: $\Delta V_{c,2}^{1b} = -\Delta V$. Using that $K_{c,2} = 1$, the charge in $C_2$ during phase $\varphi_{1b}$ is: $q_{c,2}^{1b} = -1q$.

**Step 4)** Phase $\varphi_{1b}$: Since $q_{c,2}^{1b} = -1q$ the voltage change across $C_3$ is: $\Delta V_{c,3}^{1b} = \Delta V$. Leading to a charge in $C_3$: $q_{c,3}^{1b} = 1q$.

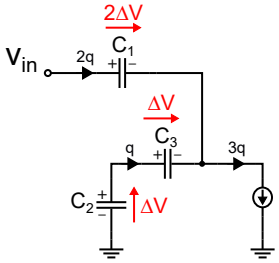
**Step 5** Constraint (1): Since $\Delta V_{c,3}^{1a} + \Delta V_{c,3}^{1b} + \Delta V_{c,3}^{2a} = 0$, the voltage change across $C_3$ in phase $\varphi_{2a}$ is: $\Delta V_{c,3}^{2a} = -2\Delta V$. Leading to a charge in $C_3$ of: $q_{c,3}^{2a} = -2q$.

**Step 6)** Phase $\varphi_{2a}$: Using constraint (2) together with $\Delta V_{c,1}^{2a} = \Delta V_{c,2}^{2a}$ the KVL loop of $C_1$, $C_2$ and $C_3$ can now be solved: $\Delta V_{c,1}^{2a} + \Delta V_{c,2}^{2a} + \Delta V_{c,3}^{2a} = -\Delta V + \Delta V_{c,2}^{2a} - 2\Delta V = 0$. Leading to $\Delta V_{c,1} = -\Delta V$ and $\Delta V_{c,2}^{2a} = \Delta V$. The charge in $C_1$ and $C_2$ is then: $q_{c,2}^{2a} = -q_{c,1}^{2a} = 1q$.

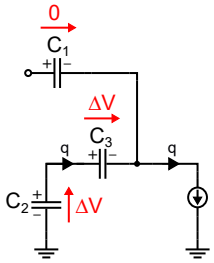
**Step 7)** Phase $\varphi_{2b}$: Constraint (1) can now be used to find the remaining voltage changes and charges in $C_1$ and $C_2$: $\Delta V_{c,1}^{1a} + \Delta V_{c,1}^{2a} + \Delta V_{c,1}^{2b} = 2\Delta - \Delta V + \Delta V_{c,1}^{2b} = 0$. Leading to $\Delta V_{c,1}^{2b} = -\Delta V$. The voltage change for $C_2$ is then $\Delta V_{c,2}^{2b} = \Delta V$. Leading to a charge in $C_1$ and $C_2$ of $q_{c,2}^{2b} = -q_{c,1}^{2b} = 1q$.



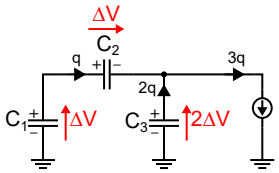

(a) 4:1 hybrid Dickson converter topology with split-phase control.



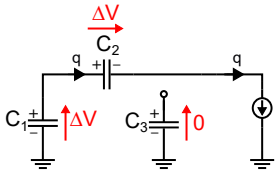

(b) 4:1 hybrid Dickson converter topology during phase $\varphi_{1a}$.




(c) 4:1 hybrid Dickson converter topology during phase $\varphi_{1b}$.




(d) 4:1 hybrid Dickson converter topology during phase $\varphi_{2a}$.




(e) 4:1 hybrid Dickson converter topology during phase $\varphi_{2b}$.

Figure 6.11: Equivalent phase networks for a 4:1 hybrid Dickson converter using split-phase control and the annotated voltage changes and charges assuming $C_1 = C_2 = C_3$.

All charges and corresponding voltage changes have now been found. The corresponding voltage changes are:

$$\begin{aligned}
\mathbf{\Delta V_c^{1a}} &= \begin{bmatrix} \Delta V_{c,1}^{1a} \\ \Delta V_{c,2}^{1a} \\ \Delta V_{c,3}^{1a} \end{bmatrix} = \begin{bmatrix} +2 \\ -1 \\ +1 \end{bmatrix}, \; \mathbf{\Delta V_c^{1b}} = \begin{bmatrix} \Delta V_{c,1}^{1b} \\ \Delta V_{c,2}^{1b} \\ \Delta V_{c,3}^{1b} \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \end{bmatrix}, \\
\mathbf{\Delta V_c^{2a}} &= \begin{bmatrix} \Delta V_{c,1}^{2a} \\ \Delta V_{c,2}^{2a} \\ \Delta V_{c,3}^{2a} \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \\ -2 \end{bmatrix}, \; \mathbf{\Delta V_c^{2b}} = \begin{bmatrix} \Delta V_{c,1}^{2b} \\ \Delta V_{c,2}^{2b} \\ \Delta V_{c,3}^{2b} \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \\ 0 \end{bmatrix}
\end{aligned} \tag{6.27}$$

and the resulting charge vectors for each phase are:

$$\begin{aligned}
\mathbf{q^{1a}} &= \begin{bmatrix} q_{in}^{1a} \\ q_{c,1}^{1a} \\ q_{c,2}^{1a} \\ q_{c,3}^{1a} \\ q_{out}^{1a} \end{bmatrix} = \begin{bmatrix} -2 \\ +2 \\ -1 \\ +1 \\ +3 \end{bmatrix}, \; \mathbf{q^{1b}} = \begin{bmatrix} q_{in}^{1b} \\ q_{c,1}^{1b} \\ q_{c,2}^{1b} \\ q_{c,3}^{1b} \\ q_{out}^{1b} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -1 \\ +1 \\ +1 \end{bmatrix}, \\
\mathbf{q^{2a}} &= \begin{bmatrix} q_{in}^{2a} \\ q_{c,1}^{2a} \\ q_{c,2}^{2a} \\ q_{c,3}^{2a} \\ q_{out}^{2a} \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \\ -2 \\ +3 \end{bmatrix}, \; \mathbf{q^{2b}} = \begin{bmatrix} q_{in}^{2b} \\ q_{c,1}^{2b} \\ q_{c,2}^{2b} \\ q_{c,3}^{2b} \\ q_{out}^{2b} \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \\ 0 \\ +1 \end{bmatrix}
\end{aligned} \tag{6.28}$$

We can check that the implementation ensures a 4:1 conversion ratio by calculating the ideal voltage conversion ratio:

$$iVCR = \left| \frac{q_{out}}{q_{in}} \right| = \frac{8}{2} = \frac{4}{1} \tag{6.29}$$

The resulting duty cycles to ensure soft-charging using split-phase control is then:

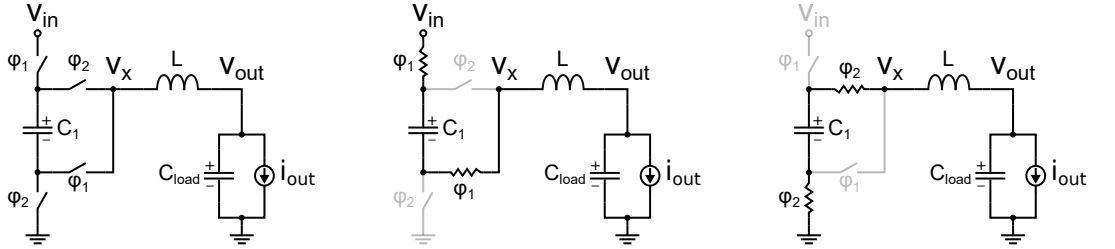
$$\begin{aligned}
D_{1a} &= t_{1a}/T_{sw} = q_{out}^{1a}/q_{out,tot} = 3/8 \\
D_{1b} &= t_{1b}/T_{sw} = q_{out}^{1b}/q_{out,tot} = 1/8 \\
D_{2a} &= t_{2a}/T_{sw} = q_{out}^{2a}/q_{out,tot} = 3/8 \\
D_{2b} &= t_{2b}/T_{sw} = q_{out}^{2b}/q_{out,tot} = 1/8
\end{aligned} \tag{6.30}$$

Note, that we could have assumed any other scaling of the flying capacitors and achieved a new solution with different phase timings. This means, that no matter the conversion ratio or the mismatch of the flying capacitors it can be compensated by changing the duty cycles of the phases. Two closed-loop controllers utilizing this have recently been presented in [95], [96] for hybrid converters using split-phase control. Here periodic sampling of the voltage mismatch is being used to change the duty cycles of the split-phases compensating for capacitor mismatch and non-idealities due to large signal behaviour in the implementation.

### 6.3.3 Using an inductor as a constant current source

So far an ideal constant current source has been considered to achieve soft-charging in the hybrid converters presented. In a practical implementation an inductor is most often used to realize the constant current source. This introduces some additional challenges since the voltage change across the inductor leads to ripple currents. Consider the 2:1 hybrid Series-Parallel converter using an inductor in series with the output in Fig. 6.12 with the phase equivalent networks shown in Fig. 6.12b and Fig. 6.12c for phase 1 and phase 2, respectively.

In Fig. 6.13 the simulated voltage and current waveforms of flying capacitor $C_1$ and the

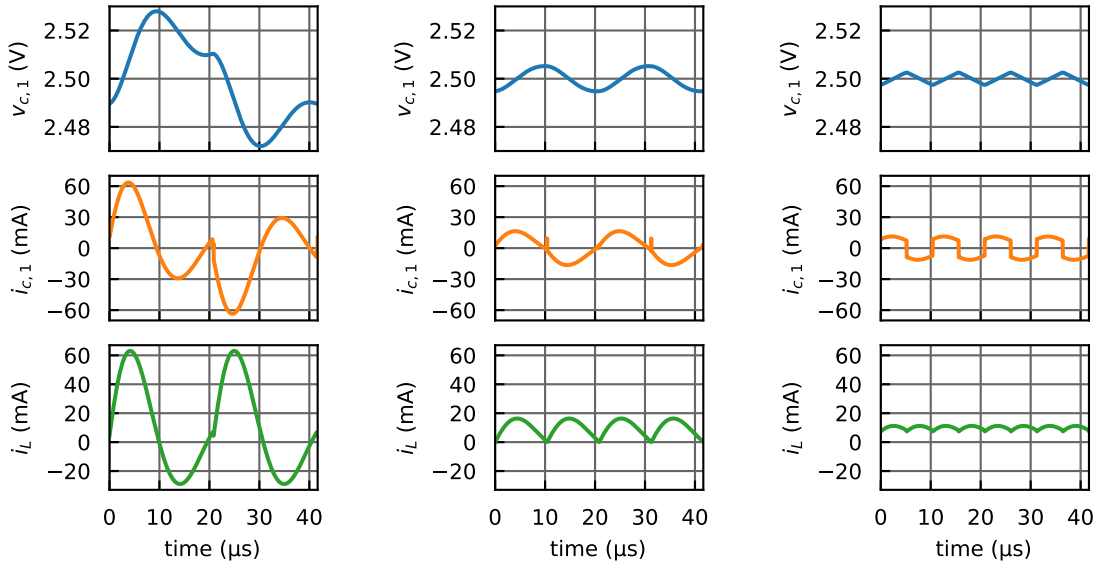



(a) The 2:1 hybrid Series-Parallel converter topology with a series output inductor.

(b) The 2:1 hybrid Series-Parallel converter topology with a series output inductor during phase 1.

(c) The 2:1 hybrid Series-Parallel converter topology with a series output inductor during phase 2.

Figure 6.12: 2:1 hybrid Series-Parallel topology with an output series inductor acting as a constant current source.




(a) Flying capacitor voltage and current and inductor current waveform at $f_{sw} = \frac{1}{2} f_{res}$.

(b) Flying capacitor voltage and current and inductor current waveform at $f_{sw} = f_{res}$.

(c) Flying capacitor voltage and current and inductor current waveform at $f_{sw} = 2 \cdot f_{res}$.

Figure 6.13: Simulated voltage and current waveforms for 2:1 hybrid Series-Parallel converter with an inductor in series with the output.

inductor in the 2:1 hybrid Series-Parallel converter can be seen for three different switching frequencies. At a frequency half of the resonant frequency, the current in the inductor drops below zero. This means, that the inductor stops acting like a constant current source and soft-charging of the flying capacitor is not achieved. This can be seen in Fig. 6.13a.

Operating at resonant frequency, the current and voltages of the flying capacitor are sinusoidal. The simulated waveforms are shown in Fig. 6.13b. Here it can be seen that the current in the inductor just reaches zero at the end of each phase. Notice a small spike current for the flying capacitor occurs in the transition from phase 1 to phase 2 in Fig. 6.13b indicating, that some voltage mismatch still occurs. At the resonant frequency zero-voltage switching (ZVS) of the switches can also be achieved [91], leading to the switching-losses due to the parasitic drain-source capacitances of the switches, described in section 3.2, to be removed. Operating the hybrid switched-capacitor converter at the resonant frequency thereby maximizes the energy-efficiency of the converter. Ensuring this does however require active control of the switching frequency and the dead-time of the power switches [91].

As the switching frequency is increased to twice the resonant frequency, the voltage change of the flying capacitor, and thereby the voltage ripple on the inductor is decreased, leading to the RMS current in the inductor being equal to the average current. This can be seen in Fig. 6.13c, where the voltage ripple on the capacitor is decreased and soft-charging occurs as can be seen from the flying capacitor current.

For higher values of on-state resistance of the switches, the system becomes over-damped and the benefit of adding the output series inductor is negligible. The damping factor for a hybrid converter with a single inductor at the output is equal to:

$$\zeta = \frac{1}{2} R_{FSL} \sqrt{\frac{C_{eq}}{L}} \tag{6.31}$$

where $C_{eq}$ is the average equivalent capacitance seen from the inductance across a switching period. Rearranging this the requirement of the $R_{FSL}$ to ensure under-damping ($\zeta < 1$) is then:

$$R_{FSL} < 2\sqrt{\frac{L}{C_{eq}}} \tag{6.32}$$

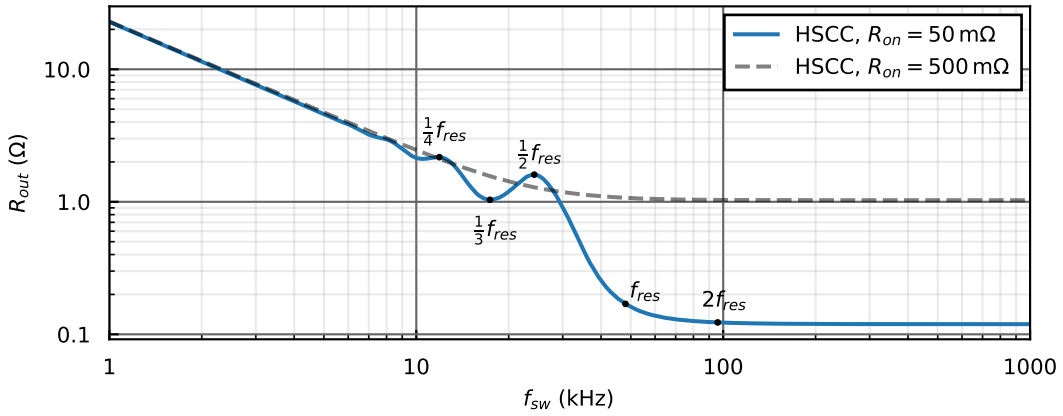



Figure 6.14: Simulated output resistance of a 2:1 Series-Parallel converter with $L = 1\,\mu\text{H}$, $C_1 = 10\,\mu\text{F}$ and $C_{out} = 100\,\mu\text{F}$.

In Fig. 6.14 a simulation with two different values of $R_{on}$ of the switches can be seen for the 2:1 hybrid Series-Parallel converter. Here it can be seen that for a $R_{on} = 500\,\mathrm{m}\Omega$, which leads to a $R_{FSL} \approx 1\,\Omega$, the system is over-damped and there is little benefit of adding an inductor to the switched-capacitor converter. Furthermore, resonant operation can not be achieved in an over-damped system, since the inductor current waveform is not half-sinusoidal, such as for the under-damped system waveforms shown in Fig. 6.13.

For highly-integrated switched-capacitor converters, where the switches are integrated it can be difficult to achieve $R_{FSL}$ low enough to ensure that the system is under-damped. Therefore, topologies with good switch utilization are preferred for hybrid converters such as the Dickson converter [75] or newer variations like the dual-inductor hybrid converter (DIHC) presented in [97], symmetrical dual-inductor hybrid converter (SDIHC) presented in [49] and the flying capacitor multi-level (FCML) hybrid converter such as in [98]–[101].

The output resistance of a traditional 2:1 Series-Parallel switched-capacitor converter is shown in Fig. 6.15 together with the 2:1 hybrid Series-Parallel converter. Here the frequency gain by adding the inductor can be seen. If the same output resistance is accepted, the switching frequency by adding the inductor, can be lowered by approximately the Q-factor of the system for the hybrid converter compared to the traditional switched-capacitor converter:

$$\frac{f_{RC,scc}}{f_{res,hscc}} = \frac{\sqrt{LC}}{R_{FSL}C} = \frac{1}{R_{FSL}}\sqrt{\frac{L}{C}} = Q \tag{6.33}$$

Furthermore, if a reduction of the passive components is desired this corresponds to lowering either the inductor or the equivalent capacitance by a factor of $Q^2$ which can lead to a significant reduction in the overall power converter volume.

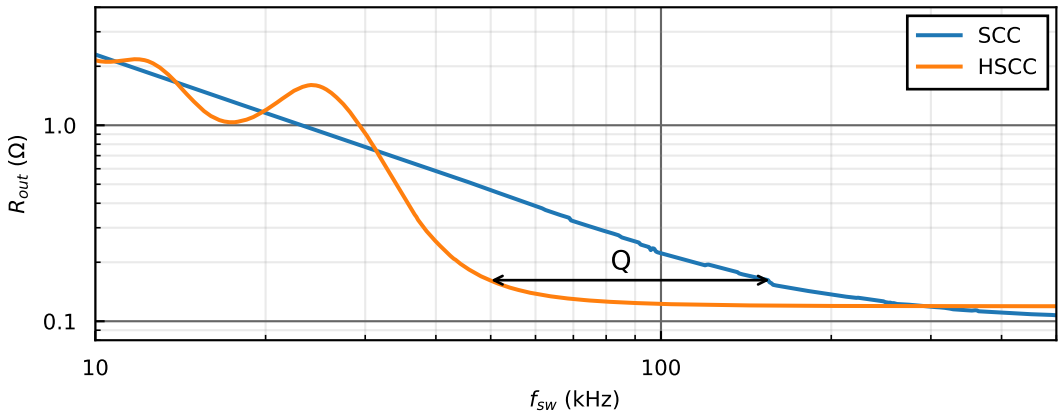



Figure 6.15: Simulated output resistance of a 2:1 switched-capacitor converter with and without an inductor in series with the output.

## 6.4 Summary

In this chapter, the fundamental analysis of switched-capacitor converters with a constant current source in series with the output was presented. The hybrid switched-capacitor converter can achieve high energy-efficiency since the charge redistribution losses from the flying capacitors being connected in parallel in various switching phases is removed. The soft-charging of the capacitors was described and a method for determining the slow-switching limit resistance was presented and shown for a 2:1 hybrid Series-Parallel converter. An intuitive, visual multi-step method for determining the soft-charging capabilities of a switched-capacitor converter topology was explained and various examples determining the soft-charging capabilities for different switched-capacitor topologies was shown.

A description of how capacitor mismatch variations effects the soft-charging capabilities of hybrid converters was also presented. This showed, that since accurate matching of the flying capacitors is required to ensure soft-charging, any capacitor variations due to production variations or from large signal impact on the capacitance of the flying capacitors, will lead to an increase in the voltage mismatch of the flying capacitors and reintroduce charge redistribution losses. This description was supported by statistical analysis of the capacitor variations impact on the $R_{SSL}$ for a 5:1 hybrid Dickson converter.

The capacitor mismatch can be handled with the split-phase control of hybrid converters, which adds to additional switching phases to ensure soft-charging for any capacitor scaling. The split-phase control was examined for a 4:1 hybrid Dickson converter. The necessary phase timings were determined using the visual multi-step approach for determining soft-charging in the split-phase control of the 4:1 hybrid Dickson converter for a desired capacitor scaling.

Finally, the impact of realizing the constant current source at the output of the hybrid converter with an inductor was examined. Simulation results showed the impact on the $R_{SSL}$ versus frequency for the 2:1 hybrid Series-Parallel converter. Here some of the requirements to enable soft-charging was presented, including the required $R_{FSL}$ of the hybrid switched-capacitor converter to ensure proper operation when using an inductor as a constant current source.

# 7 Conclusion and future work

To accommodate the increasing demand for power converters which achieve a high energy efficiency and power density, highly-integrated switched-capacitor converters have gained interest in replacing traditional inductor-based switch-mode power supplies. The general benefits come from the increased energy density of capacitors compared to inductors and the better power switch utilization of switched-capacitor converters. The highly-integrated switched-capacitor converter consists of fully integrated power switches, gate-drivers and digital control circuits, while utilizing the high energy density of MLC capacitors. This means, that it is possible to handle a larger output power compared to the fully integrated switched-capacitor converters, while maintaining a high power density due to the monolithic integration.

The switched-capacitor converter is a fixed-ratio DC-DC converter, where the conversion ratio is dependent on the topology and implementation. These functions well as inter-stage DC-DC converters in a stage of a larger system, where regulation is not required. Therefore, a dc bus for 48 V-12 V was chosen as a focus for this project, since these are common desired rails in various applications.

The monolithic integration of the power stage enables optimization of the sizing of the power switches. Therefore, a design methodology for highly-integrated switched-capacitor converters has been developed formulating the intrinsic power losses and power losses due to the parasitic capacitances of the switches as a function of the size and area specific on-state resistance of the power switches. This leads to a general optimization method for any highly-integrated switched-capacitor converter. Furthermore, a design optimization of the external flying capacitors has been presented optimizing the number of flying capacitors for a desired PCB area using Lagrange Multiplier optimization.

The design methodology was verified with experimental results for a fabricated IC consisting of a 4:1 Ladder topology with an integrated power stage, gate-drivers and clock controller. The measured peak efficiency for the 48 V-12 V highly-integrated switched-capacitor converter is 93.5 %, the maximum measured output power is 24.6 W leading to a maximum power density of $23\,\mathrm{W/cm^3}$.

One of the main challenges in the design of switched-capacitor converters is ensuring safe start-up of the converter. Two challenges were identified in this projects, that can be damaging to a highly-integrated switched-capacitor converter. The maximum voltage ratings of the switches and flying capacitors and the peak inrush currents as the power converter system clock is enabled. These two challenges have been analyzed and three potential solutions have been presented and simulated. The first solution is a passive start-up approach where the addition of a capacitor creates a charging path from the input source to all flying capacitors. The second method is a switch conductance control, where the on-state resistance of the switches are increased during the start-up until the flying capacitor voltages have reached the desired steady-state. The third method is an active pre-charge circuit that consists of a regulator that charges the flying capacitors from the input source.

To verify that safe start-up can be achieved the active pre-charge circuit has taped out and experimental results of the measured flying capacitor voltages and the peak inrush current during start-up have been measured. The peak measured inrush current being only 534 mA. The active pre-charge circuit area is: 911 µm $\times$ 734 µm.

To further increase the energy efficiency and power density of switched-capacitor converters, hybrid switched-capacitor converters were also investigated in this project. The hybrid converter is able to remove the charge redistribution losses of the flying capacitors, by enabling soft-charging of the flying capacitors from a constant current source. In this project a visual multi-step approach of analyzing the soft-charging capabilities hybrid converters and their required flying capacitor scalings was developed and a derivation of the equivalent output resistance ($R_{SSL}$) for hybrid converters due to these charge redistribution losses has been presented. This has been used to analyze various non-idealities such as flying capacitor mismatch on the charge redistribution losses, which is important to consider for highly-integrated switched-capacitor solutions. Furthermore, simulation results of a hybrid converter with an inductor in series with the output acting as a constant current source has been shown and the effect of the inductor to the output resistance has been discussed.

Based on the work presented in this project, highly-integrated switched-capacitor converters have the potential of accommodating the increasing requirements of high energy efficiency and power density for consumer electronics.

## 7.1 Future work

As is clear from this thesis, highly-integrated switched-capacitor converters have a great potential in applications targeting output power levels from 1-300 W. With the increasing research interest in both hybrid and traditional switched-capacitor converters and advancements in high-voltage semiconductor technology the following list are interesting research topics to be explored in the future.

- **400 V-12 V highly-integrated switched-capacitor converter**
  High voltage, high-conversion ratio highly-integrated switched-capacitor converters have recently been enabled by the advancements of high-voltage semiconductor technology. Enabling a direct conversion step from rectified electrical mains to a 12 V intermediate bus could increase overall energy efficiency of the dc bus in various applications.

- **Capacitive galvanic isolation for highly-integrated switched-capacitor converter**
  Galvanic isolation is required for online power converters interfacing directly with the electrical mains. Traditional inductor-based power converters usually achieve galvanic isolation by a transformer. Investigating other methods of achieving galvanic isolation, such as with high-voltage rated capacitors, could lead to small volume AC-DC switched-capacitor converters. The design of a highly-integrated switched-capacitor converter driving a capacitive galvanic isolation with a LC compensation filter is an interesting potential research topic.

- **Safe start-up and shut-down methods for high-voltage switched-capacitor converters**
  While this project presented three potential solutions to ensure safe start-up, further research is required to ensure a volatile and safe operation of the highly-integrated switched-capacitor converter. Furthermore, safe shut-down should be investigated, since this can also lead to damage of the IC if not handled properly.

- **Highly-integrated hybrid switched-capacitor converters**
  Monolithic integration of the power stage, gate-drivers and control circuits for a hybrid switched-capacitor converter could lead to advancements of the energy efficiency and power density of switched-capacitor converters. This could include inte-

grated active controllers for split-phase control for compensating capacitor voltage mismatch to ensure soft-charging and closed-loop output voltage regulation.

- **Packaging improvement**
  In this project a QFN64 package was used for packaging of the IC. To increase power density and the maximum output power, other packaging options using inter-poser packaging technologies should be investigated. This has the potential of including the external flying capacitors into a single package leading to a much smaller form factor of the highly-integrated switched-capacitor converter.

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# A Analysis and Design of Start-up Circuits for a 48V-12V Switched-Capacitor Converter in a 180nm SOI Process

*2021 IEEE Nordic Circuits and Systems Conference (NorCAS 2021)*

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Status: Published

DOI: 10.1109/NorCAS53631.2021.9599860

# Analysis and Design of Start-up Circuits for a 48 V-12 V Switched-Capacitor Converter in a 180 nm SOI Process

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***Abstract*—In this work an analysis, design and layout of two start-up methods for high-voltage switched-capacitor converters is presented. During the converter start-up phase, the capacitors are charged from their initial voltage to their steady-state voltages. If a start-up approach is not considered, this creates undesired large currents in the power switches and chip I/Os, which can damage the chip. A $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor converter with an integrated power stage and external capacitors is designed and taped out in a $180\,\mathrm{nm}$ SOI CMOS process to demonstrate two different approaches of mitigating the start-up problem. The first approach solves the uneven capacitor charging during input ramp-up by creating a charging path from the input to the capacitors and carefully sizing the capacitors. The second approach charges the capacitors with a dedicated active pre-charging circuit and thereby ensures limited peak currents during start-up of the designed switched-capacitor converter. This first start-up method reduces the start-up peak current from $40\,\mathrm{A}$ to $6.5\,\mathrm{A}$ and the second method lowers the peak current to $3.5\,\mathrm{A}$. The designed pre-charge circuit consumes $105\,\mu\mathrm{A}$ quiescent current and has an area of $743\,\mu\mathrm{m} \times 911\,\mu\mathrm{m}$.**

## I. Introduction

Switched-capacitor power converters are becoming more interesting in high-voltage and high-power applications such as in automotive and in data centers due to the lack of magnetic components [1]–[5]. This allows for a higher power density and lower weight since the inductors are usually bulky in traditional power converters. The recent advances in high-voltage semiconductor technology allows for integrating the switches and gate-drivers of the converter, allowing for a lower production cost and smaller size. One draw-back of switched-capacitor converters that is rarely considered is the issue of starting up the converter safely and consistently. When the voltage input of the converter ramps up the large capacitors are charged through undesired parasitic charging paths. This results in large peak currents going into the chip whenever these unmatched voltages are connected through low resistance integrated switches. These large peak currents can damage the bonding wires in the packaging to the integrated circuit (IC). Another issue is that by integrating the power stage resolves in a lack of measurement points to monitor these voltages, therefore precise control of these voltages during start-up is essential for a robust power converter.

Only a few research papers mention the start-up issue of switched-capacitor power converters. In the work of [6] an integrated LED driver is proposed with an input range of $80\,\mathrm{V}$-$90\,\mathrm{V}$ with a single IC. The LED driver is a hybrid resonant switched-capacitor converter also facing some start-up challenges. The start-up solution proposed in [6] is interesting but specific for the topology presented since it is using the gate-drivers to charge the capacitor nodes. In [7] a soft start-up is achieved in a buck converter. This is achieved with integrated power-switches and gate-drivers with additional control signals for only turning on a small part of the switch. This means that the large switch resistance will decrease the large peak current until the output capacitor is charged to the desired level. This solution is interesting because it utilizes the large switches and otherwise only rely on small digital circuitry. The complexity of the solution presented in [7] does however increase since more switches has to be controlled in different voltage domains. This requires an additional level-shifting for each start-up signal and could, dependent on the implementation, take up significant area on-chip.

This paper investigates the challenges of start-up in high-voltage switched-capacitor power converters with integrated switches. To showcase the analysis and explanation of proposed start-up solutions this work is based around a $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor converter implemented as a ladder topology, which has been designed in a $180\,\mathrm{nm}$ SOI process and sent to fabrication. The power converter is designed for a peak efficiency of $92.5\,\%$ at an output power of $12\,\mathrm{W}$. In this topology the challenges of start-up is eminent since large capacitors are connected in parallel in every switching-phase.

This paper is structured as follows: Section II gives an expanded analysis on the challenges of start-up in a high-voltage switched-capacitor converter and shows two possible start-up solutions: an passive and active implementation. Section III shows simulation results of the two start-up solutions. Section IV discusses these simulation results and compared these to previous research. The implications and applications of the two solutions are also discussed. Section V mentions the future work. The integrated circuit has been taped-out in April 2021 and is expected to return December 2021. Section VI concludes the work presented in the paper.

## II. Analysis of start-up in Ladder switched-capacitor converter

In Fig. 1 the $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor ladder converter can be seen. Here the switches $M_1$, $M_3$, $M_5$ and $M_7$ are turned on during phase 1 and $M_2$, $M_4$, $M_6$ and $M_8$ are turned

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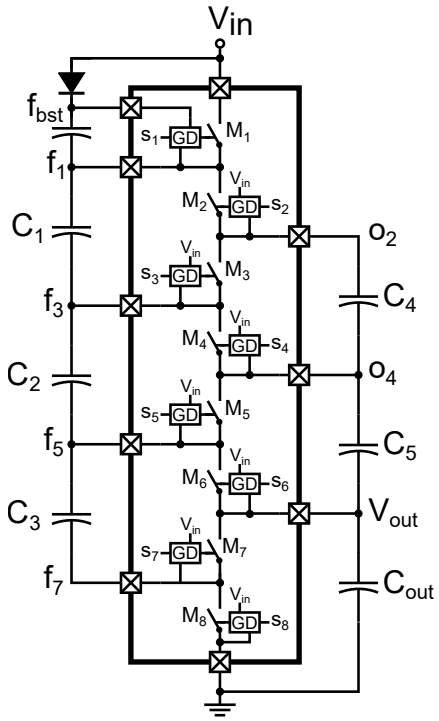


Fig. 1: 4:1 switched-capacitor converter implemented with a ladder topology with the gate-drivers (GD) references to the power converter input.

on during phase 2. The switches are turned on by gate-drivers which are all supplied from the converter input. The connection of the gate-drivers to the power converter input voltage means that the switches can be turned on as the input voltage is ramping up. It does however also mean that there is a leakage current path from the input to all the capacitors through the gate-drivers and the parasitic capacitances of the large switches in the integrated power stage. This together with the parasitic capacitance of the switches themselves means, that during the input voltage ramp-up the capacitors are charged to voltages dependent on the capacitor size and their specific parasitic leakage current.

This results in undesired voltages during the input voltage ramp-up. Since the capacitor voltage differences can easily be several volts and the integrated switches around $100\,\mathrm{m}\Omega$ a large peak current can easily be observed in the first switching periods during start-up. The peak current can be estimated by observing that the connection is an RLC-circuit. [7] The peak current can be expressed as:

$$i_{peak} = \frac{V_s}{L \cdot w_d} \mathrm{e}^{\frac{-R\pi}{4Lw_d}} \tag{1}$$

where $w_d = \sqrt{\frac{1}{LC} - \alpha^2}$ and $\alpha = \frac{R}{2L}$. Here $V_s$ is the capacitor voltage mismatch, R is the total series resistance in the loop dominated by the integrated switches, C is the total capacitance from the output and flying capacitors and L is the total inductance from the bonding wires. This peak current can lead to damage in the bonding wires during start-up. This damaged can be reduced by choosing wider and multiple bonding wires in parallel for each bonding pad but the peak current still resolves in a fragile start-up sequence.

To overcome this challenge the capacitor voltages must be charged such that they match those of the steady-state capacitor voltages. In the case of the 4-1 ladder converter topology that means that all capacitors must have a $1/4V_{in}$ voltages across them before any switching occurs. This should be achieved in a robust fashion without any significant addition to the power loss of the power converter, since that degrades the power efficiency. Note that classical inductor-based power converters also suffers from large inrush currents during start-up. This is usually solved by various inrush limiter circuits such as in [8]. However, this is not a viable solution in the case of a switched-capacitor converter, since the large peak currents originates from the capacitor voltage mismatch and being connecting in parallel through low resistance paths and not from being connected to the power converter input.

### *A. Passive external start-up circuit*

The capacitor voltage mismatch generated by the charge leakage path through the switches can be controlled by connecting a capacitor from $o_2$ to the power converter input. This can be seen in Fig. 2. A start-up control bit ($s_{en}$) controls the $M_1$ switch and a charge path is created through $C_1$, $C_2$ and $C_3$ as they are connected in series with the input. This makes the drain-source voltage of $M_7$ negative turning on the parasitic diode of $M_7$. Thereby an equivalent circuit of series capacitance $C_1 - C_3$ is in parallel with series capacitance $C_{start} - C_5$. To ensure that during the input voltage ramp-up the voltages across all capacitors is the same the capacitors should be sized by

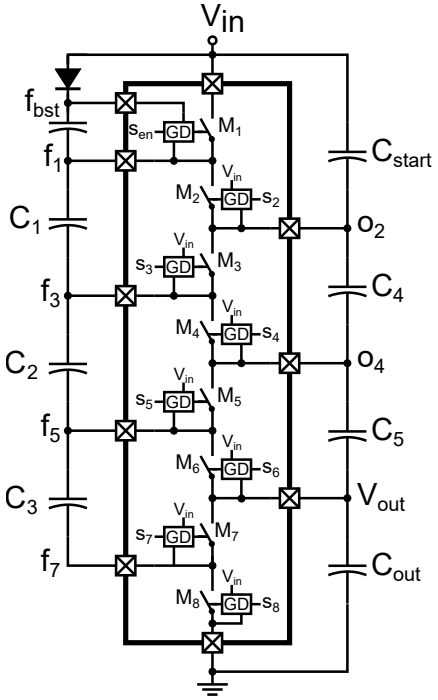


Fig. 2: Switched-capacitor converter implemented with a ladder topology and with the start-up capacitor $C_{start}$ added. The start-up bit $s_{en}$ controls the $M_1$ switch during start-up.

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_{start} = 0.5 \cdot C_{out} \quad (2)$$

This ensures that the voltage across each capacitor $1/4$ of the input voltage. The capacitors' charge times are dependent on the total time constant of the system. This time constant is dependent on bonding wire resistance, capacitor equivalent series resistance and capacitor sizes. The passive start-up circuit is dependent on that $M_1$ can be turned on at an early stage of the start-up procedure. Since the gate signals are controlled on chip by a $5\,\mathrm{V}$ digital supply voltage the input voltage, from which the digital supply voltage is generated, must be above $5\,\mathrm{V}$ before the start-up control bit can be enabled.

This start-up procedure is beneficial since the $C_{start}$ capacitor is an external addition and only specific control of the $M_1$ switch is required. The limitation of the method is the specific capacitor sizing. The optimal sizing of the capacitors follows the charge flow analysis described in [9]. By resizing to ensure a safe start-up this optimal sizing is not fulfilled meaning that the voltage ripple on all capacitors are not equal. This can be neglected by increasing the size of all capacitors, but still resolves in a sub-optimal design, which increases the total area of the power converter. Another limitation of the start-up procedure is that the start-up is dependent on the relative capacitor sizes. Thereby will any variation in the capacitor sizes due to production variation also alter the effectiveness of the start-up method. A benefit of this start-up method is that the addition of $C_{start}$ does not affect the power converter operation or consume any static current. It does however increase the total power converter area since the extra capacitor, $C_{start}$, is added.

### *B. Active internal start-up circuit*

To save area and utilize optimal capacitor sizing an internal circuit responsible for charging the output capacitors ($C_4$, $C_5$ and $C_{out}$) to the desired steady-state voltages can be seen in Fig. 3. The schematic of the active pre-charge circuit (APC) can be seen in Fig. 4. Here the diode-coupled $M_{diode}$ is biased by the depletion-mode transistor $M_{cs}$ and $R_{ref}$ working as a current source. The transistor $M_{diode}$ is biased such that $V_{ref}$ can be expressed as:

$$V_{ref} = V_x + V_{th,Mdiode} \quad (3)$$

where $V_{th,Mdiode}$ is the threshold voltage of $M_{diode}$ and $V_x$ is the reference voltage, which the active pre-charge circuit should charge the $V_{charge}$ node to. The $M_{pass}$ acts as a pass device as long as:

$$V_{eff,Mpass} = V_{ref} - V_{charge} - V_{th,Mdiode} > 0 \quad (4)$$

Where $V_{eff,Mpass}$ is the effective voltage of the pass transistor. This means that the voltage generated at the output of the APC, $V_{charge}$, converges towards:

$$V_{charge} = V_{ref} - V_{th,Mdiode} = V_x + V_{th,Mpass} - V_{th,Mdiode} \quad (5)$$

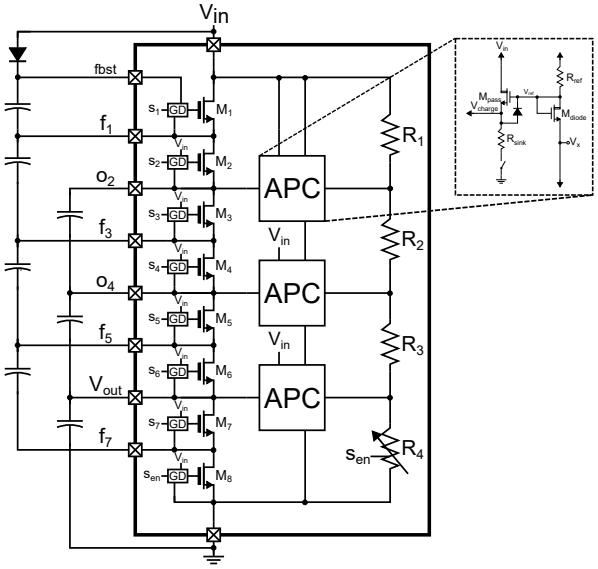


Fig. 3: The 4-to-1 integrated ladder converter with the active pre-charge circuit (APC) blocks.

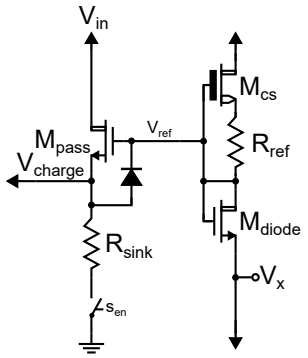


Fig. 4: Active pre-charge circuit block for charging the output capacitors to the desired steady-state voltage.

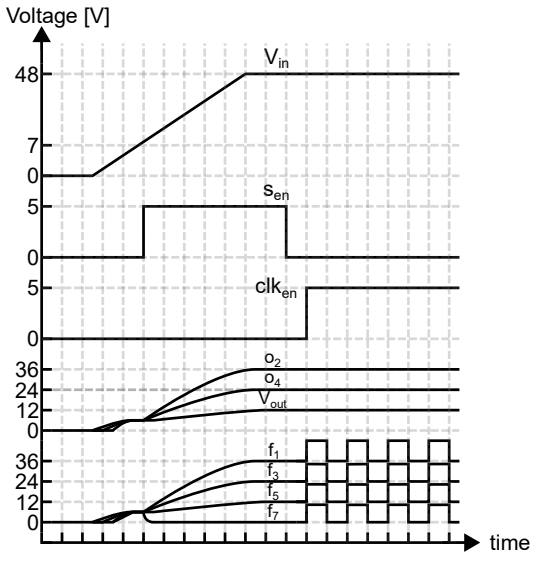


Fig. 5: Start-up procedure and switched-capacitor power converter voltages using the active pre-charge circuit to ensure safe start-up.

by matching $M_{pass}$ and $M_{diode}$ identical threshold voltages can be achieved and the output of the APC becomes:

$$V_{charge} = V_x \tag{6}$$

The resistor $R_{sink}$ is responsible for current sinking, since the $V_{charge}$ can also be above $V_{ref}$ before the start-up circuit is enabled. The reference for the APC blocks are generated by a resistor string ($R_1 - R_4$). Since this is connected directly from the power converter input to ground the total resistance should be designed to be large enough such as the quiescent current does not degenerate the converter efficiency significantly. The resistor ladder generates the voltages $3/4V_{in}$, $1/2V_{in}$ and $1/4V_{in}$. The resistor $R_4$ is a variable resistor controlled by the start-up enable bit $s_{en}$. When $s_{en} = 1$ the resistors are all equal, while when the converter has reached the steady-state voltages and start-up is disabled $R_4$ is reduced thereby decreasing the reference voltages for the APC blocks. This means that $V_{ref}$ for all the APC blocks is decreased and the requirement in (4) is never true, turning off the $M_{pass}$ transistor. The current sinking path through $R_{sink}$ is also turned off by a switch controlled by the $s_{en}$ bit. In Fig. 5 the start-up procedure with the active pre-charge circuit is shown. The input voltage is ramped up and when it reaches above $7\,\mathrm{V}$ the start-up enable signal $s_{en}$ is enabled. This turns on power transistor $M_8$, connecting the flying node $f_7$ to ground. The APC blocks now starts charging the output nodes to the desired steady-state voltages. The flying nodes $f_1$, $f_3$ and $f_5$ are charged through the body diodes of $M_2$, $M_4$ and $M_6$ respectively. This charging current from the APC should be low enough so that the switches are not damaged, since the body diodes have limited charging capabilities. This current is limited by the maximum output current from the pass devices in the APC blocks. This means that when the power converter clock is enabled by $clk_{en}$ the capacitor voltages are all equal to the desired $1/4V_{in}$ and no large peak current is experienced.

## III. Simulation Results

To verify the two proposed start-up methods the high-voltage switched-capacitor power converter has been designed in a $180\,\mathrm{nm}$ SOI process and the performance simulated. The start-up procedure shown in Fig. 5 has been used for both the passive start-up and the active pre-charge start-up method.

### A. Baseline without start-up circuit

A simulation without any of the two start-up methods has also been done to show the bonding wire peak current baseline. In this case the start-up bit $s_{en}$ is kept low and the clock is enabled, when the input voltage has reached the desired $48\,\mathrm{V}$. The switched-capacitor voltages during the input voltage ramp-up with the start-up circuit disabled can be seen in Fig. 6. Here it can be seen that as the input voltage increases so does the capacitor nodes. They do however not reach the desired values for steady-state. In Fig. 7 the bonding wire currents can be seen when the the clock is enabled. Here it is clear that the switched-capacitor nodes have not reached the desired voltages and that this leads to peak currents close to $40\,\mathrm{A}$. It can be seen that the current going into the chip from the $f_7$ node must go through $M_7$ since it can be seen to go out of the $V_{out}$ node. These $40\,\mathrm{A}$ would most likely burn both the bonding wire and damage the $M_7$ switch. Especially after repeated start-up sequences. It can be seen that the peak current decreases with time, since the switched-capacitor nodes settles towards their desired steady-state voltages. In the high-voltage switched-capacitor converter there are 6 bonding wires connected in parallel from the pads from $f_7$ on the chip to the packaging. The same is true for the $V_{out}$-pad. These each have a length of around $3.2\,\mathrm{mm}$ and a diameter of $33\,\mu\mathrm{m}$. With the current being equally distributed this means that the bonding wire's each see about $6.67\,\mathrm{A}$. According to [10] a $3\,\mathrm{mm}$ gold wire with $33\,\mu\mathrm{m}$ diameter have a fusing current of around $0.665\,\mathrm{A}$. This fusing current

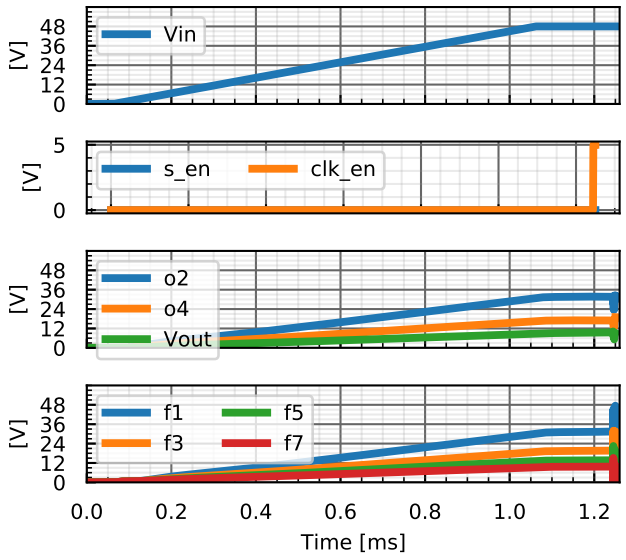


Fig. 6: Switched-capacitor voltages with no start-up method enabled.

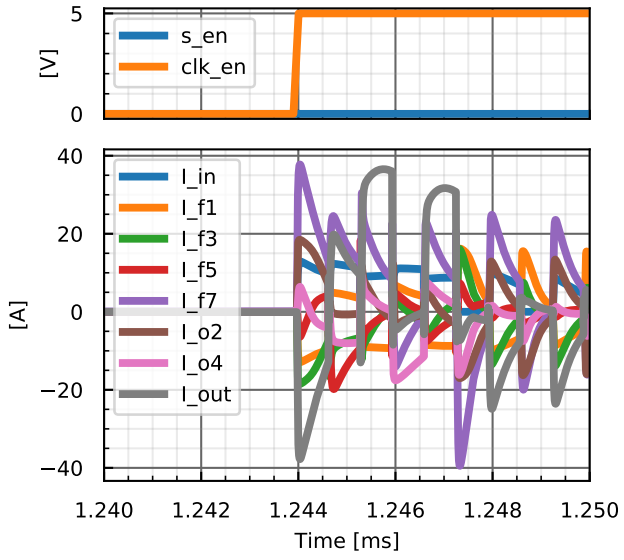


Fig. 7: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with no start-up method enabled.

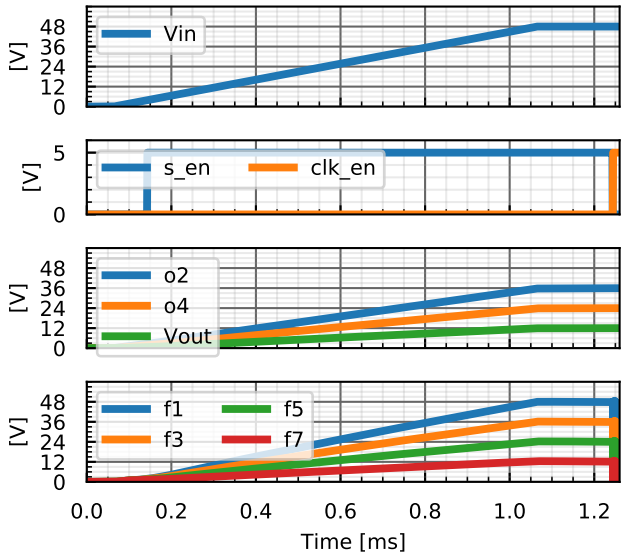


Fig. 8: Switched-capacitor voltages with the passive start-up method.

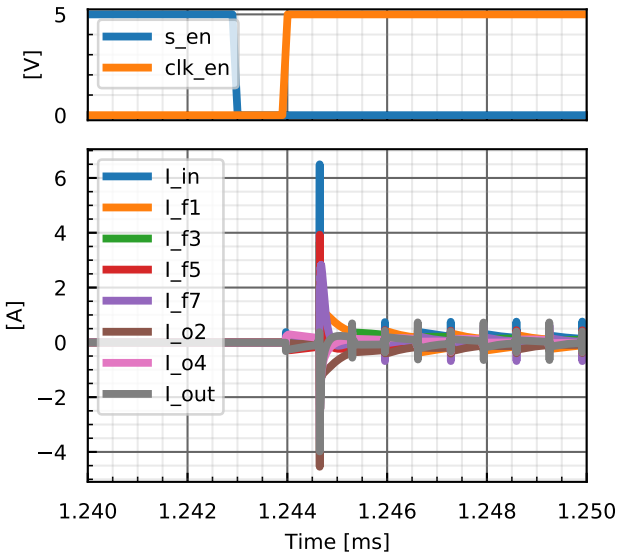


Fig. 9: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with the passive start-up method.

is the bonding wire's RMS fusion current. Estimating the peak current as a triangular wave the approximate peak current fusion current is around:

$$I_{peak} = \sqrt{3} \cdot 0.665\,\text{A} = 1.15\,\text{A} \tag{7}$$

Since the bonding wire peak current is almost six times this limit, the bonding wire would be expected to get damaged during repeated start-up procedures.

### B. Passive start-up method simulation results

In Fig. 8 the switched-capacitor converter voltages nodes can be seen, where a capacitor $C_{start}$ is connected from $o_2$ to $V_{in}$ as is shown in Fig. 2. Here the capacitors $C_{start}$, $C_1$, $C_2$, $C_3$, $C_4$ and $C_5$ are $5.4\,\mu$F and $C_{out}$ is $10.8\,\mu$F. In Fig. 8 $M_1$ is controlled by $s_{en}$ during start-up and $M_1$ therefore connects the $f_1$ node to $V_{in}$. In Fig. 8 it can be seen that all the voltage nodes reach their desired steady-state voltages. In Fig. 9 the switched-capacitor converter bonding wire currents can be seen when the clock is enabled. Now, since the capacitors have approximately the same voltages when connected through the low resistance switches, the maximum peak current is $6.5\,\text{A}$ through the bonding wire connected to the input of the power converter. It can also be seen that after a single switching period the peak current is down to what is expected for steady-state operation. There are 3 bonding wires of length $2.3\,\text{mm}$ connected to the input bonding pad. According to [10] the fusion RMS current for this bonding wire is around $0.95\,\text{A}$. The approximate peak fusion current is then $1.65\,\text{A}$. This is lower than the expected peak current of $\frac{1}{3} \cdot 6.5\,\text{A} = 2.17\,\text{A}$ per bonding wire and could mean that the bonding wire could get damaged after repeated start-up sequences.

### C. Active pre-charge circuit start-up method simulation results

In Fig. 10 the switched-capacitor node voltages can be seen during the input voltage ramp-up. Note that here the $M_8$ switch is turned on by the $s_{en}$ signal, which means that the $f_7$ node is connected to ground. It can be seen from Fig. 10 that all the switched-capacitor voltage nodes reach the desired steady-state. In Fig. 12 the bonding wire currents can be seen when the clock is enabled. In this case, the maximum peak current through a bonding wire is $3.5\,\text{A}$. This is through the output node bonding wire and the $f_7$ node bonding wire. These have 6 bonding wires each, which means that the largest bonding wire current is $0.58\,\text{A}$. With a bonding wire length of $3.2\,\text{mm}$ the peak fusion current is around $1.15\,\text{A}$. This means that the bonding wires should be safe even for repeated starting sequences. The active pre-charge circuit consumes a static $105\,\mu\text{A}$, when the converter has reached steady-state. This means that the active pre-charge circuit does not affect the power converter efficiency in any significant way compared to the power converter output power of $12\,\text{W}$.

## IV. Discussion

A summary of the simulation results of the start-up methods together with the designed switched-capacitor power converter can be seen in Table I. Here it can be seen that the two methods reduces the bonding wire inrush current from $40\,\text{A}$ to $6.5\,\text{A}$ and $3.5\,\text{A}$ for the passive start-up and the active pre-charge method respectively. Since not much prior work has been published on

TABLE I: Summary of the simulation results for the different start-up sequences.

| Start-up method | No start-up | Passive start-up | Active start-up |
|---|---|---|---|
| Maximum peak current [A] | 40 | 6.5 | 3.5 |
| Peak current bonding wire | $V_{out}$ and $f_7$ | $V_{in}$ and $o_2$ | $V_{out}$ and $f_7$ |
| Peak current per bonding wire [A] | 6.67 | 2.17 | 0.58 |
| Peak bonding wire fusion current [A] | 1.15 | 1.65 | 1.15 |
| $I_{quiescent}$ [$\mu$A] | 0 | 0 | 105 |
| Extra capacitor added | No | Yes | No |

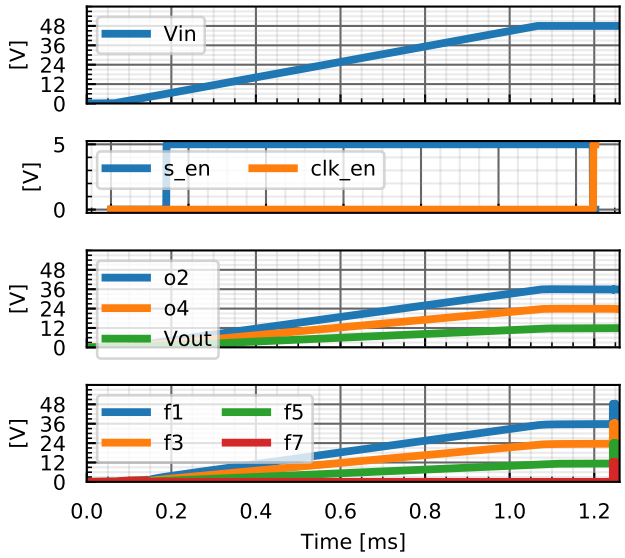


Fig. 10: Switched-capacitor voltages with the active pre-charge start-up method.

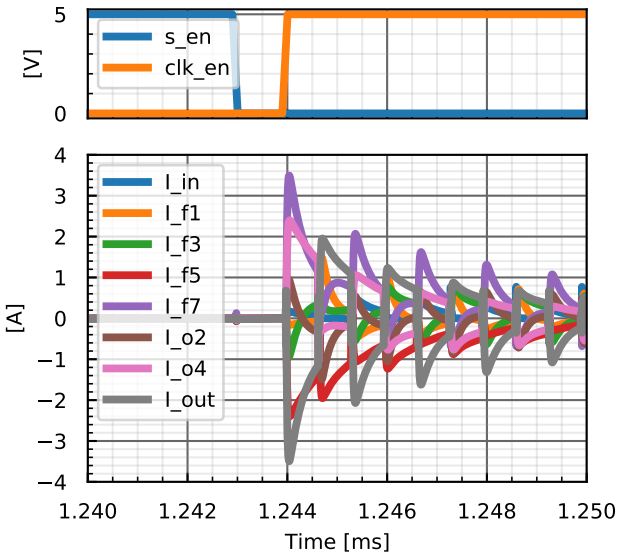


Fig. 12: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with the active pre-charge start-up method.

the challenges of start-up in switched-capacitor converters with an integrated power stage it has not been possible to compare these results with the state-of-the-art. The performance of the active pre-charge start-up method us simulated across global variations and from temperatures at 27 °C, 80 °C and 100 °C. The largest peak current comes from the 27 °C case, which is 3.5 A. The resistor string responsible for the reference voltages for the APCs has been carefully matched, such that local mismatch variations does not alter the APC output voltages.

## V. Future Work

The switched-capacitor converter with the integrated power stage and the active pre-charge start-up circuit has been sent to fabrication and is expected back December 2021. The performance of both the power converter and the start-up sequences described in this paper is to be validated with measurement results. In the future a start-up method based on the work in [7] could also be interesting, since it saves the area of the APC blocks and could lower the quiescent current consumption of the start-up circuit.

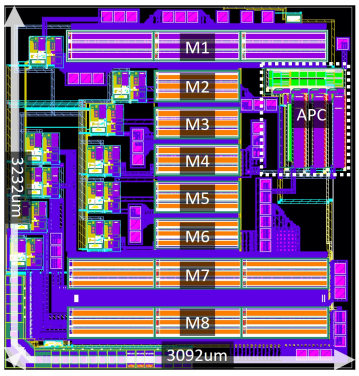


Fig. 11: Layout of the designed and taped out 48 V-12 V switched-capacitor converter with the integrated power stage and active pre-charge circuit (APC).

## VI. Conclusion

Two start-up methods have been designed and presented for a 12 W, 48 V-12 V switched-capacitor power converter with an integrated power stage implemented in a 180 nm SOI process. First an analysis of the challenges in start-up for a switched-capacitor power converter has been presented. Next the two proposed solutions have been shown and the trade-offs of each method presented. The first method controls the top switch of the integrated power stage to charge all capacitors during input ramp-up together with an extra external capacitor and careful sizing of the capacitors to ensure that all capacitors are charged to the same voltages. The second method uses a fully integrated active pre-charge circuit to charge the external capacitors to the desired steady-state voltages before enabling the power converter. Both implementations have been verified in simulation and compared to a baseline of 40 A inrush current from not using a dedicated start-up circuit. The passive method does not consume any additional static current, but does increase the converter size with an added capacitor, additionally it uses sub-optimal capacitor sizing for the converter, this limits the peak inrush current to 6.5 A. The active pre-charge circuit consumes a static 105 µA and has an area of 743 µm×911 µm, this limits the peak inrush current to 3.5 A. Finally, a discussion of the results is presented and future work of the start-up methods is presented.

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# B An Active Pre-Charge Start-up Circuit for a 48V-12V Switched-Capacitor Converter in a 180nm SOI Process

*Springer Analog Integrated Circuits and Signal Processing*

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Status: Submitted

# An Active Pre-Charge Start-up Circuit for a 48V-12V Switched-Capacitor Converter in a 180nm SOI Process

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**Abstract**

In this work an active pre-charge start-up circuit and procedure for high-voltage switched-capacitor converters is presented and verified with measurements. Without a start-up procedure, undesired large currents can occur in the power switches and chip I/Os during start-up, which can damage the chip. To prevent this, the startup circuit charges the capacitors from their initial voltage to their steady-state voltages during the converter start-up phase. A 48 V-12 V switched-capacitor converter with an integrated power stage and discrete capacitors is designed and taped out in a 180 nm SOI CMOS process to demonstrate two different approaches of mitigating the start-up problem. The first approach solves the uneven capacitor charging during input ramp-up by creating a charging path from the input to the capacitors and carefully sizing the capacitors. The second approach charges the capacitors with a dedicated active pre-charging circuit and thereby ensures limited peak currents during start-up of the designed switched-capacitor converter. Measurements show that the active pre-charging circuit reduces the peak inrush current from 40 A to 534 mA. The designed pre-charge circuit consumes 105 µA quiescent current and has an area of 743 µm × 911 µm.

**Keywords:** High-voltage, switched-capacitor, start-up, inrush current, integrated power converter

## 1 Introduction

Switched-capacitor converters are becoming more interesting in high-voltage and high-power applications such as in automotive and in data centers due to the absence of magnetic components [1–5]. This allows for a higher power density and lower weight since the inductors are usually bulky in traditional power converters. The recent advances in high-voltage semiconductor technology allows for integrating the switches and gate-drivers of the power converter, allowing for a lower production cost and smaller size. One draw-back of switched-capacitor converters, which is rarely considered in the literature, is the issue of starting up the converter safely and consistently. When the input voltage of the converter ramps up, the capacitors, which are typically large, are charged through undesired charging paths. When two capacitors with unmatched voltages are connected through a low resistance integrated switch, large currents can flow into the chip. These large peak currents can damage the bonding wires in the packaging to

the integrated circuit (IC) and damage the IC.

Only a few research papers mention the start-up issue of switched-capacitor converters. In the work of [6] an integrated LED driver is proposed with an input range of 80 V-90 V with a single IC. The LED driver is a hybrid resonant switched-capacitor converter also facing some start-up challenges. The start-up approach proposed in [6] is using the gate-drivers to charge the capacitors. This is interesting but the approach is specific for the topology presented, therefore it can not be widely used for different applications. Other approaches have been used for inductor-based converters, such as the soft start-up of the buck converter in [7]. This is achieved with integrated power-switches and gate-drivers with additional control signals for only turning on a small part of the switch. This means that the large switch resistance will decrease the large peak current until the output capacitor is charged to the desired level. This approach is interesting because it utilizes the large switches and otherwise only rely on small digital circuitry. The complexity of the approach presented in [7] does however increase, since more switches have to be controlled in different voltage domains. This requires an additional level-shifting for each start-up signal and could, depending on the implementation, take up significant area on-chip.

This paper investigates the challenges of start-up in high-voltage switched-capacitor converters with integrated switches and proposes two approaches by designing two start-up methods. To showcase the analysis and proposed start-up approaches this work presents an implementation based around a 48 V-12 V switched-capacitor converter implemented as a ladder topology, which has been designed in a 180 nm SOI process and taped out. The power converter has an expected peak efficiency of 94 % at an output power of 15 W. In this topology the challenges of start-up is eminent since large capacitors are connected in parallel in every switching-phase as explained in Section 2.

This paper is structured as follows: Section 2 gives an expanded analysis on the challenges of start-up in a high-voltage switched-capacitor converter and shows two possible start-up approaches: a passive and an active implementation. Section 3 shows simulation results of the passive and active start-up approaches and also

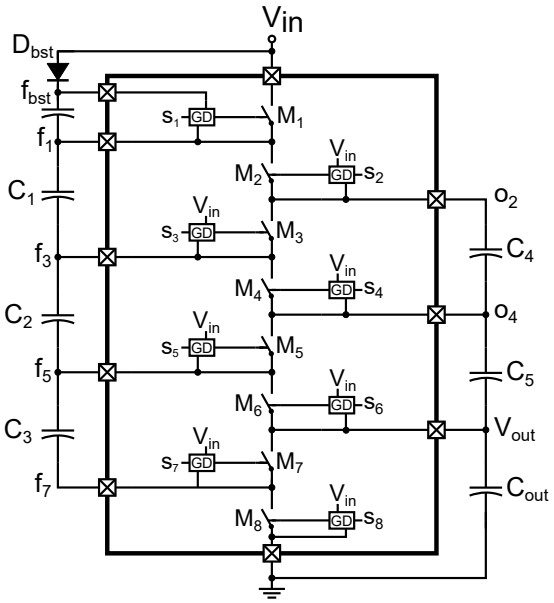


**Fig. 1**: 4:1 switched-capacitor converter implemented with a ladder topology with the gate-drivers (GD) supply connected to the power converter input.

summaries the simulation result findings. Section 4 shows experimental results of the active start-up implementation. Section 5 discusses these experimental results. The implications and applications of the active start-up implementation approach is also discussed. Section 6 concludes the work presented in the paper.

This paper is an extended version of the work in [8] published in IEEE International Nordic Circuits and Systems (NORCAS) in 2021.

## 2 Analysis of start-up in ladder switched-capacitor converter

In Fig. 1 the 4:1 switched-capacitor ladder converter can be seen. Here the switches $M_1$, $M_3$, $M_5$ and $M_7$ are turned on during phase 1 and $M_2$, $M_4$, $M_6$ and $M_8$ are turned on during phase 2. The switches are turned on by gate-drivers which are all supplied from the converter input. The connection of the gate-drivers to the power converter input voltage means that the switches can be turned on as the input voltage is ramping up. It does however also mean that there is a leakage current path from the input to all the

capacitors through the gate-drivers and the parasitic capacitances of the large switches in the integrated power stage. This together with the parasitic capacitance of the switches themselves means, that during the input voltage ramp-up the capacitors are charged to voltages dependent on the capacitor size and their specific parasitic leakage current.

This results in undesired voltages during the input voltage ramp-up. Since the capacitor voltage differences can easily be several volts and the on-resistance of the integrated switches around 100 mΩ a large peak current can easily be observed in the first switching periods during start-up. The peak current can be estimated by observing that the connection is an RLC-circuit.[7] The peak current can be expressed as:

$$i_{peak} = \frac{V_s}{L \cdot w_d} \mathrm{e}^{\frac{-R\pi}{4Lw_d}} \tag{1}$$

where $w_d = \sqrt{\frac{1}{LC} - (\frac{R}{2L})^2}$. Here $V_s$ is the capacitor voltage mismatch, $R$ is the total series resistance in the loop dominated by the integrated switches, C is the total capacitance from the output and flying capacitors and L is the total inductance from the bonding wires. This peak current can lead to damage in the bonding wires during start-up. This damage can be mitigated by choosing wider and multiple bonding wires in parallel for each bonding pad but the peak current still results in a fragile start-up sequence.

To overcome this challenge the capacitor voltages must be charged such that they match those of the steady-state capacitor voltages. In the case of the 4:1 ladder converter topology that means that all capacitors must have a $1/4V_{in}$ voltages across them before any switching occurs. This should be achieved in a robust fashion without any significant addition to the power loss of the power converter, since that degrades the power efficiency. Note that classical inductor-based power converters also suffers from large inrush currents during start-up. This is usually solved by various inrush limiter circuits such as in [9]. However, this is not a viable approach in the case of a switched-capacitor converter, since the large peak currents originates from the capacitor voltage mismatch and being connecting in parallel through low resistance paths and not from being connected to the power converter input.

## 2.1 Passive discrete start-up circuit

The capacitor voltage mismatch generated by the charge leakage path through the switches can be controlled by connecting a capacitor from $o_2$ to the power converter input. This can be seen in Fig. 2. A start-up control bit ($s_{en}$) controls the $M_1$ switch and a charge path is created through $C_1$, $C_2$ and $C_3$ as they are connected in series with the input. Another bit ($clk_{en}$) enables the system clock of the IC. The start-up bit, $s_{en}$, makes the drain-source voltage of $M_7$ negative turning on the parasitic diode of $M_7$. Thereby an equivalent circuit of series capacitance $C_1 - C_3$ is in parallel with series capacitance $C_{start} - C_5$. To ensure that during the input voltage ramp-up the voltages across all capacitors is the same the capacitors should be sized by

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_{start} = 0.5 \cdot C_{out} \tag{2}$$

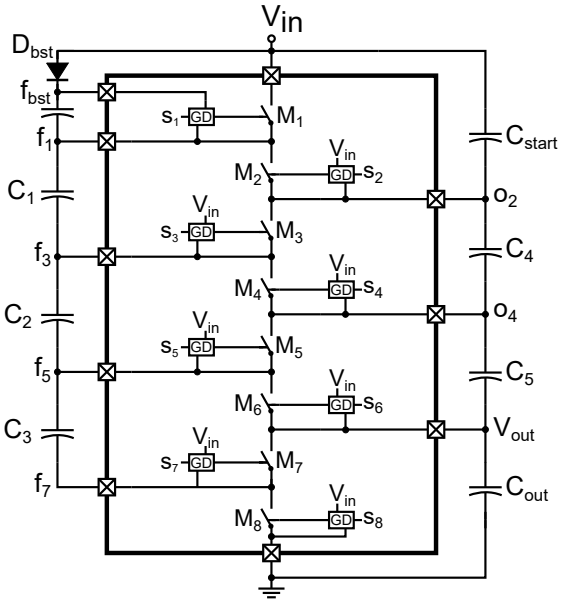


**Fig. 2**: Switched-capacitor converter implemented with a ladder topology and with the start-up capacitor $C_{start}$ added for the passive discrete start-up approach. $M_1$ is turned on during start-up.

This ensures that the voltage across each capacitor 1/4 of the input voltage. The capacitor charging times are dependent on the total time constant of the system. This time constant is dependent on bonding wire resistance, capacitor equivalent series resistance and capacitor sizes. The passive start-up circuit is dependent on that $M_1$ can be turned on at an early stage of the start-up procedure. Since the gate signals are controlled on chip by a 5 V digital supply voltage the input voltage, from which the digital supply voltage is generated, must be above 5 V before the start-up control bit can be enabled reliably. In reality the gate signal can start turning on the $M_1$ switch as soon as the input voltage goes above the transistor threshold voltages, which are dependent on the specific fabrication process.

This start-up procedure is beneficial since the $C_{start}$ capacitor is an external addition and only specific control of the $M_1$ switch is required. The limitation of the method is the specific capacitor sizing. The optimal sizing of the capacitors, in regards to area and efficiency, follows the charge flow analysis described in [10]. By resizing to ensure a safe start-up this optimal sizing is not fulfilled meaning that the voltage ripple on all capacitors are not equal. This can be neglected by increasing the size of all capacitors, but still results in a sub-optimal design, which increases the total area of the power converter. Another limitation of the start-up procedure is that the start-up is dependent on the relative capacitor sizes. Any variation in the capacitor sizes due to production variation will therefore alter the effectiveness of the start-up method. A benefit of this start-up method is that the addition of $C_{start}$ does not affect the power converter operation or consume any static current. It does however increase the total power converter area since the extra capacitor, $C_{start}$, is added.

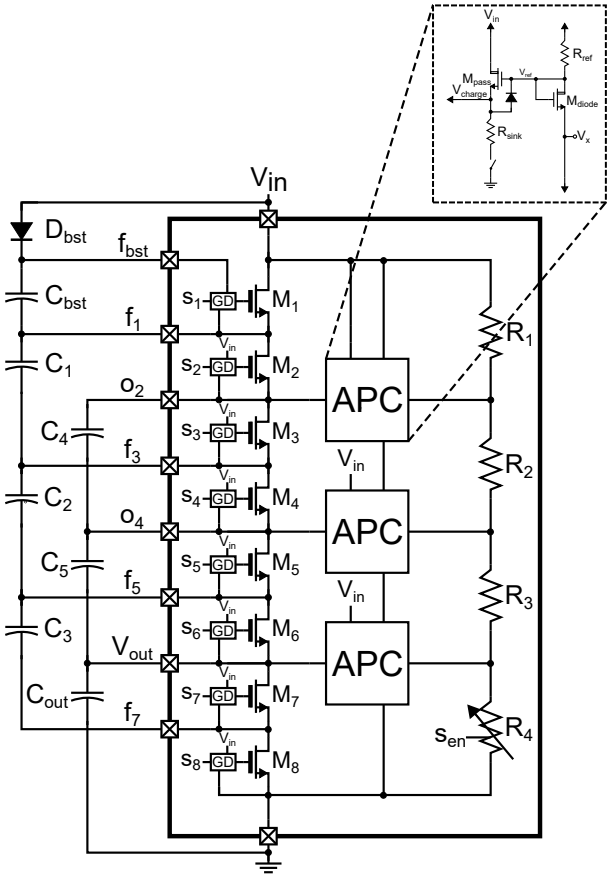


**Fig. 3**: The 4:1 integrated ladder converter with the active pre-charge circuit blocks.

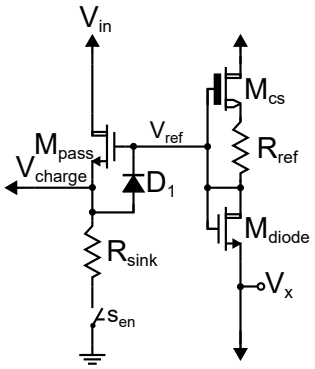


**Fig. 4**: Active pre-charge circuit block for charging the output capacitors to the desired steady-state voltage.

## 2.2 Active integrated start-up circuit

To save area and utilize optimal capacitor sizing an integrated circuit responsible for charging the output capacitors ($C_4$, $C_5$ and $C_{out}$) to the desired steady-state voltages is introduced (Fig. 3). The schematic of the active pre-charge circuit (APC) can be seen in Fig. 4. Here the diode-coupled $M_{diode}$ is biased by the depletion-mode transistor $M_{cs}$ and $R_{ref}$ working as a current source. The transistor $M_{diode}$ is biased such that $V_{ref}$ can be expressed as:

$$V_{ref} = V_x + V_{th,Mdiode} \tag{3}$$

where $V_{th,Mdiode}$ is the threshold voltage of $M_{diode}$ and $V_x$ is the reference voltage, which the active pre-charge circuit should charge the $V_{charge}$ node to. The $M_{pass}$ acts as a pass device as long as:

$$V_{eff,Mpass} = V_{ref} - V_{charge} - V_{th,Mdiode} > 0 \quad (4)$$

Where $V_{eff,Mpass}$ is the effective voltage of the pass transistor. This means that the voltage generated at the output of the APC, $V_{charge}$, converges towards:

$$\begin{aligned} V_{charge} = V_{ref} - V_{th,Mdiode} = V_x \\ +V_{th,Mpass} - V_{th,Mdiode} \end{aligned} \quad (5)$$

by matching $M_{pass}$ and $M_{diode}$ identical threshold voltages can be achieved and the output of the APC becomes:

$$V_{charge} = V_x \quad (6)$$

The resistor $R_{sink}$ is responsible for current sinking, since the $V_{charge}$ can also be above $V_{ref}$ before the start-up circuit is enabled. The reference for the APC blocks are generated by a resistor string

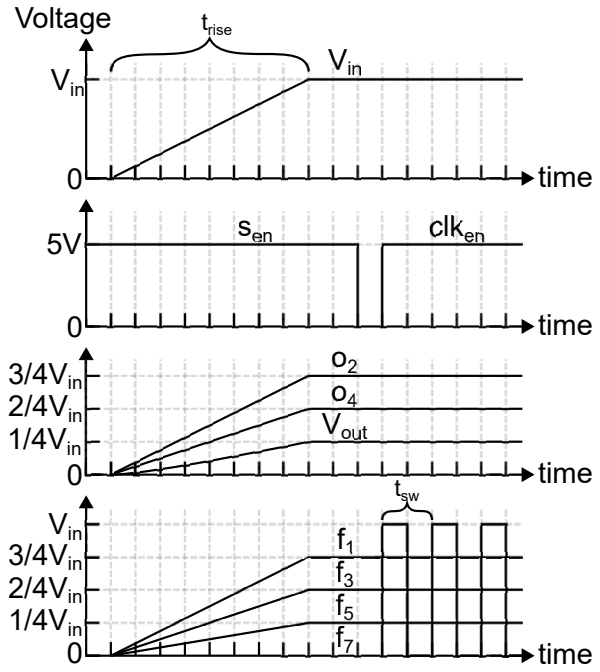


**Fig. 5**: Start-up procedure and switched-capacitor converter voltages using the active pre-charge circuit to ensure safe start-up. $t_{rise}$ is the rise time of the input voltage and $t_{sw}$ is the switching period of the switched-capacitor converter.

$(R_1 - R_4)$. Since this is connected directly from the power converter input to ground the total resistance should be designed to be large enough such as the quiescent current does not degenerate the converter efficiency significantly. The resistor ladder generates the voltages $3/4V_{in}$, $1/2V_{in}$ and $1/4V_{in}$. The resistor $R_4$ is a variable resistor controlled by the start-up enable bit $s_{en}$. When $s_{en} = 1$ the resistors are all equal, while when the converter has reached the steady-state voltages and start-up is disabled $R_4$ is reduced thereby decreasing the reference voltages for the APC blocks. This means that $V_{ref}$ for all the APC blocks is decreased and the requirement in (4) is never true, turning off the $M_{pass}$ transistor. The current sinking path through $R_{sink}$ is also turned off by a switch controlled by the $s_{en}$ bit.

In Fig. 5 the start-up procedure for the active start-up method is shown. First the $s_{en}$ is enabled and $s_2, s_4, s_6$ and $s_8$ is enabled. Afterwards the input voltage is ramped up and as it is increasing the gate-drivers start turning on power transistors $M_2, M_4, M_6$ and $M_8$. This connects $f_1$ to $o_2$, $f_3$ to $o_4$, $f_5$ to $V_{out}$ and $f_7$ to ground. The APC blocks now starts charging the output nodes to the desired steady-state voltages. The flying nodes $f_1$, $f_3$ and $f_5$ are charged through $M_2$, $M_4$ and $M_6$ respectively. The current is limited by the maximum output current from the pass devices in the APC blocks. This current together with the size of the capacitors limits how fast the circuit can start up the power converter. When the power converter has reached its desired steady-state voltages the clock is enabled. At this point the capacitor voltages are all equal to the desired $1/4V_{in}$ and no large peak currents are experienced. Note that this start-up sequence differs from that presented previously in [8]. There the start-up sequence required synchronization between the $s_{en}$ bit and the input voltage ramp. Furthermore, it did not enable $M_2$, $M_4$ and $M_6$ but simply relied on the body-diodes of these power transistors to charge the flying nodes. This means that the active pre-charge circuit would only have sourcing capabilities for $f_1$, $f_3$ and $f_5$ and would not be able to sink current should the capacitor voltages go above the desired steady-state voltages. By using this improved and simpler start-up sequence both sourcing and sinking is made possible and the desired steady-state voltages are achieved during start-up.

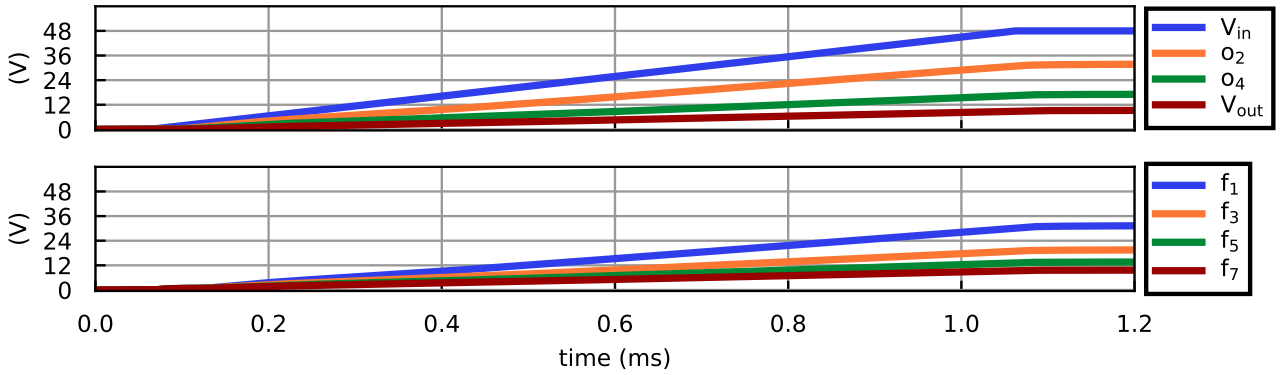


**Fig. 6**: Switched-capacitor voltages with no start-up procedure implemented.

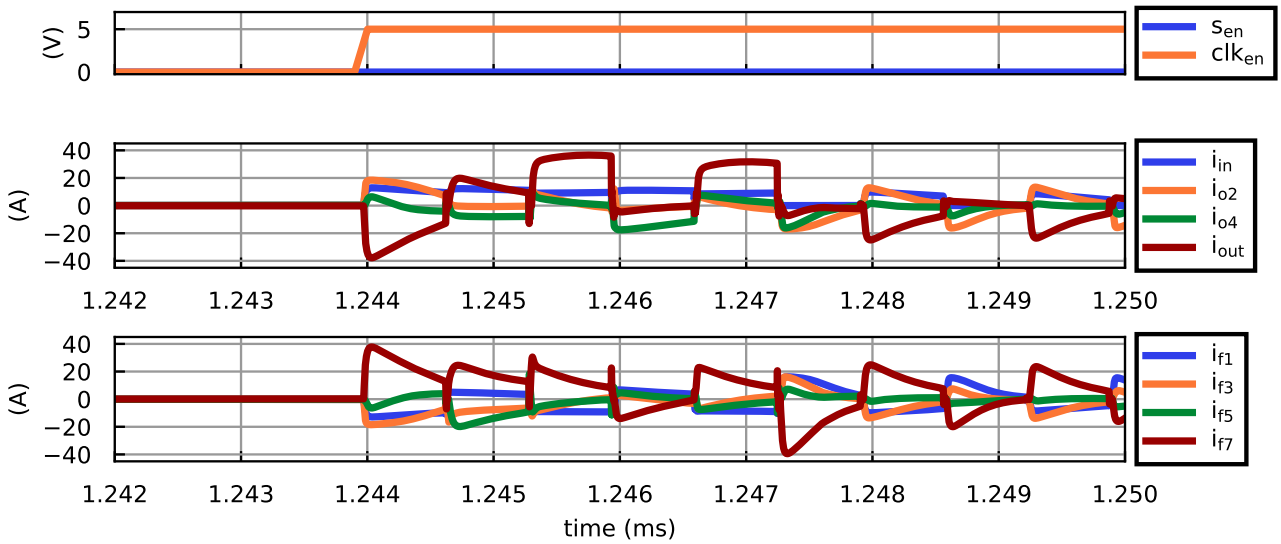


**Fig. 7**: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with no start-up method enabled.

## 3 Simulation results

To verify the two proposed start-up methods a 48 V-12 V switched-capacitor converter has been designed in a 180 nm SOI process and its performance simulated. The start-up procedure shown in Fig. 5 has been used for both the passive start-up and the active pre-charge start-up method.

### 3.1 Baseline without start-up circuit

A simulation without any of the two start-up methods has also been done to show the bonding wire peak current baseline. In this case the start-up bit $s_{en}$ is kept low and the clock is enabled, when the input voltage has reached the desired 48 V. The switched-capacitor voltages during the input voltage ramp-up with the start-up circuit disabled can be seen in Fig. 6. Here it can be seen that as the input voltage increases so does the capacitor nodes. They do however not reach the desired values for steady-state. In Fig. 7 the bonding wire currents can be seen when the the clock is enabled. Here it is clear that the switched-capacitor nodes have not reached the desired voltages and that this leads to peak currents close to 40 A. It can be seen that the current going into the chip from the $f_7$ node must go through $M_7$ since it can be seen to go out of the $V_{out}$ node. These 40 A would most likely burn both the bonding wire and damage the $M_7$ switch. Especially

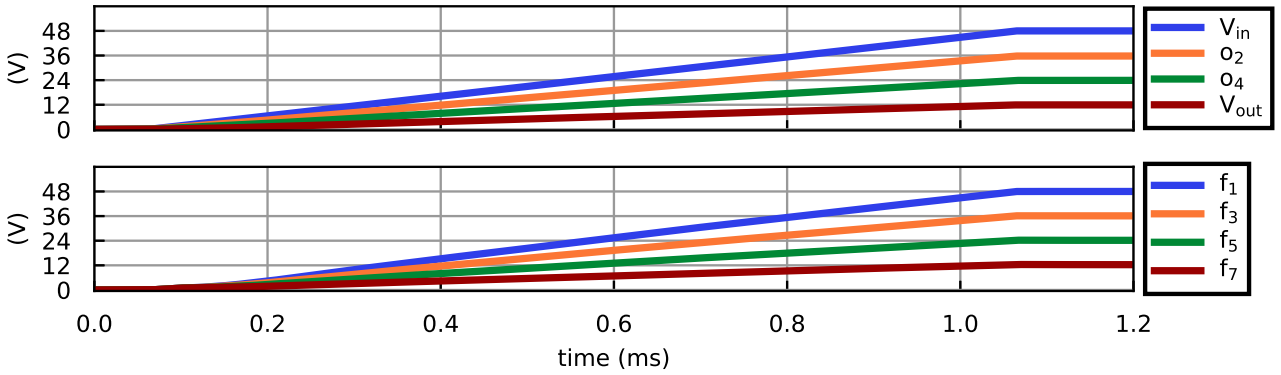


**Fig. 8**: Switched-capacitor voltages with the passive start-up method implemented.

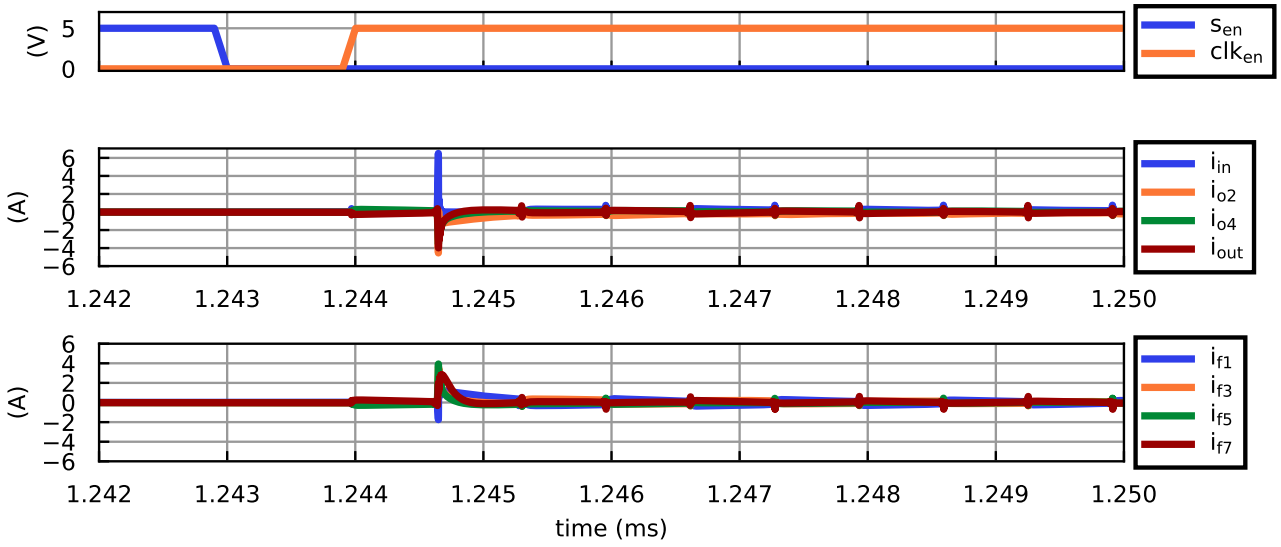


**Fig. 9**: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with the passive start-up method.

after repeated start-up sequences. It can be seen that the peak current decreases with time, since the switched-capacitor nodes settles towards their desired steady-state voltages. In the high-voltage switched-capacitor converter there are 6 bonding wires connected in parallel from the pads from $f_7$ on the chip to the packaging. The same is true for the $V_{out}$-pad. These each have a length of around 3.2 mm and a diameter of 33 $\mu$m. With the current being equally distributed this means that the bonding wire's each see about 6.67 A. According to [11] a 3 mm gold wire with 33 $\mu$m diameter have a DC or RMS fusing current of around 0.665 A. For ensuring safe operation the inrush current going into the IC should be ensured to not pass this threshold. Estimating the peak current as a triangular wave the approximate peak current fusing current is around:

$$I_{peak} = \sqrt{3} \cdot 0.665\,\text{A} = 1.15\,\text{A} \tag{7}$$

Note that the current in (7) is the value for a periodic triangular current wave and that inrush peak currents are not. Therefore, this estimate is conservative. Since the bonding wire peak current for the no start-up procedure is almost six times this limit, the bonding wire would be expected to get damaged during repeated start-up procedures.

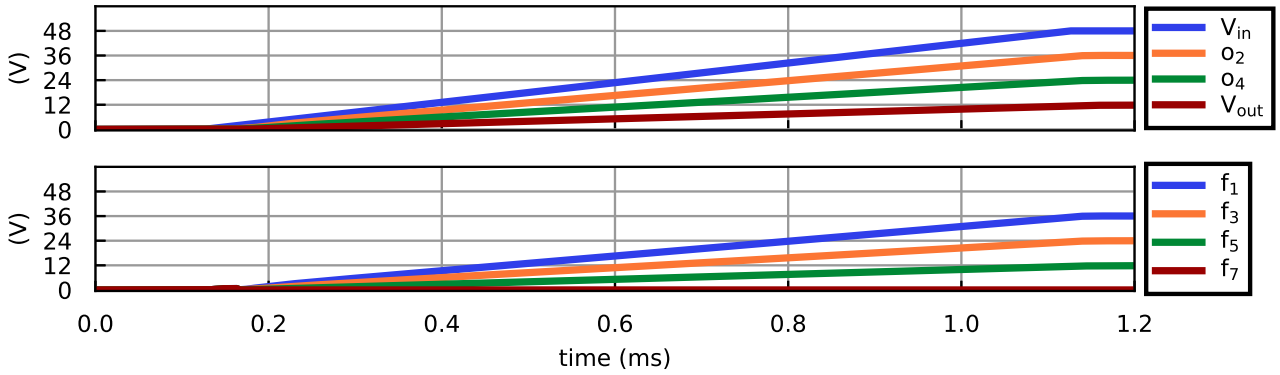


**Fig. 10**: Switched-capacitor converter voltages with the active pre-charge start-up method.

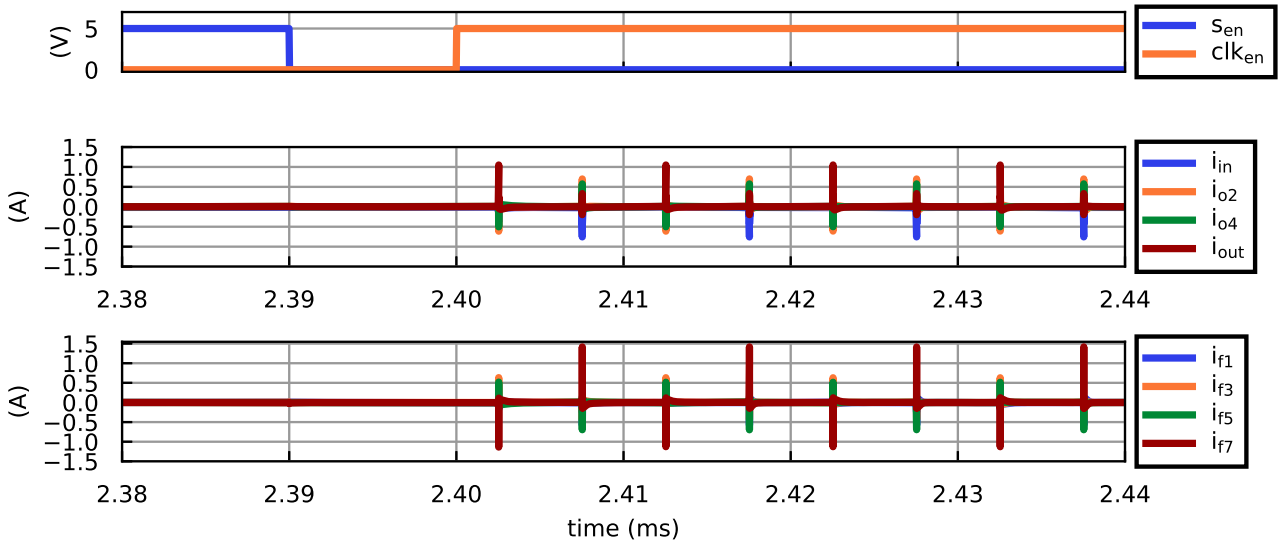


**Fig. 11**: Switched-capacitor converter bonding wire currents when the power converter clock is enabled with the active pre-charge start-up method.

## 3.2 Passive start-up method simulation results

In Fig. 8 the switched-capacitor converter voltage nodes can be seen, where a capacitor $C_{start}$ is connected from $o_2$ to $V_{in}$ as is shown in Fig. 2. Here the capacitors $C_{start}$, $C_1$, $C_2$, $C_3$, $C_4$ and $C_5$ are $5.4\,\mu$F and $C_{out}$ is $10.8\,\mu$F. In Fig. 8 $M_1$ is controlled by $s_{en}$ during start-up and $M_1$ therefore connects the $f_1$ node to $V_{in}$. In Fig. 8 it can be seen that all the voltage nodes reach their desired steady-state voltages. In Fig. 9 the switched-capacitor converter bonding wire currents can be seen when the clock is enabled. Now, since the capacitors have approximately the same voltages when connected through the low resistance switches, the maximum peak current is 6.5 A through the bonding wire connected to the input of the power converter. It can also be seen that after a single switching period the peak current is down to what is expected for steady-state operation. There are 3 bonding wires of length 2.3 mm connected to the input bonding pad. The simulated peak current of each bonding wire is: $\frac{1}{3} \cdot 6.5\,\text{A} = 2.17\,\text{A}$. According to [11] the fusing RMS current for this bonding wire is around 0.95 A. The approximate peak fusing current is then 1.65 A. The simulated peak current per bonding wire current therefore exceeds the allowed peak fusing current, which could mean that the

**Table 1**: Summary of the simulation results for the different start-up sequences.

| Start-up method | No start-up | Passive start-up | Active start-up |
|---|---|---|---|
| Maximum peak current [A] | 40 | 6.5 | 1.5 |
| Peak current bonding wire | $V_{out}$ and $f_7$ | $V_{in}$ and $o_2$ | $V_{out}$ and $f_7$ |
| Peak current per bonding wire [A] | 6.67 | 2.17 | 0.25 |
| Peak bonding wire fusing current [A] | 1.15 | 1.65 | 1.15 |
| $I_{quiescent}$ [$\mu$A] | 0 | 0 | 105 |
| Extra capacitor added | No | Yes | No |

bonding wire could get damaged after repeated start-up sequences.

### 3.3 Active pre-charge circuit start-up method simulation results

In Fig. 10 the switched-capacitor node voltages can be seen during the input voltage ramp-up using the active integrated start-up sequence. Note that the $M_2$, $M_4$, $M_6$ and $M_8$ power switches are enabled during the start-up procedure. It can be seen from Fig. 10 that all the switched-capacitor voltage nodes reach the desired steady-state. The flying nodes of $f_1$, $f_3$, $f_5$ and $f_7$ are seen switching when the clock is enabled at the end of simulation. In Fig. 11 the bonding wire currents can be seen when the clock is enabled. In this case, the maximum peak current through a bonding wire is 1.5 A, which is mostly from the ringing due to the estimate of the parasitic inductance in the bonding wires, which was added to the simulation test bench. It can be seen that the current spikes do not attenuate, since this is the expected steady state current waveform. The maximum current is seen at the output node bonding wire and the $f_7$ node bonding wire. These have 6 bonding wires each, which means that the largest bonding wire current is 0.25 A. With a bonding wire length of 3.2 mm the peak fusing current is around 1.15 A. This means that the bonding wires should be safe even for repeated starting sequences. The active pre-charge circuit consumes a static 105 µA, when the converter has reached steady-state and the $s_{en}$ is disabled. This current consumption comes from the resistor string used as reference in the active pre-charge circuit. The resistor string cannot be disabled, since that would leave the reference voltage for the pass devices in the APC's floating and could cause damage to these. This quiescent current consumption means that the active pre-charge circuit does not affect the power converter efficiency in any significant way compared to the expected power converter output power of 15 W.

### 3.4 Simulation results summary

A summary of the simulation results of the start-up methods together with the designed switched-capacitor converter can be seen in Table 1. Here it can be seen that the two methods reduces the bonding wire inrush current from 40 A to 6.5 A and 1.5 A for the passive start-up and the active pre-charge method respectively. Since to the knowledge of the author prior work has been published on the challenges of start-up in switched-capacitor converters with an integrated power stage it has not been possible to compare these results with the state-of-the-art. The performance of the active pre-charge start-up method is simulated across global variations and from temperatures at 27 °C, 80 °C and 100 °C. The largest peak current comes from the 27 °C case, which is 1.5 A. The resistor string responsible for the reference voltages for the APCs has been carefully matched, such that local mismatch variations does not alter the APC output voltages.

## 4 Experimental results

A microscope photo of the taped out chip can be seen in Fig. 13. The die is 3232 µm × 3092 µm and includes the integrated power stage ($M_1 - M_8$), corresponding gate-drivers, digital clock controller and the active pre-charge start-up circuit. To verify the simulation results the IC have been packaged and tested. The measurements have been made at an input voltage of 48 V. To verify that the chip can safely start up the experimental results are focused on measuring the start-up

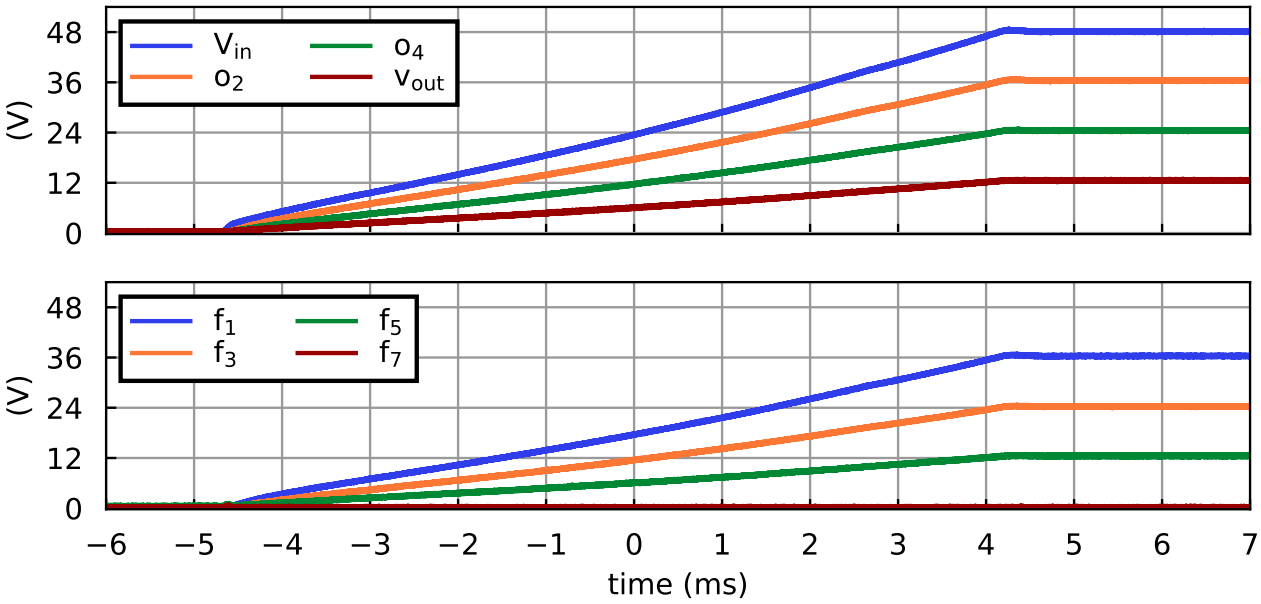


**Fig. 12**: Measurement of switched-capacitor converter voltages during the active integrated start-up sequence.

voltages of the switched-capacitor converter voltage nodes and the largest inrush current, which is the current flowing from the $f_7$ node into the IC. The IC is verified using the test setup seen in Fig. 15. The test setup consists of an 5 V power supply for the digital domain, 48 V power supply for supplying the input voltage and a function generator for the external clock. The digital control bits of the chip are controlled by a Raspberry Pi. The IC is tested in a chip socket for the QFN64 chip package. Only the active integrated start-up method will be tested since it is the only method that ensures safe start-up according to simulation results. The start-up for the measurements corresponds to the one presented in Fig. 5. No load is connected to the power converter during the measurements, since it is assumed that a load will be enabled after the start-up sequence is complete. The input is ramped up at a 8 ms rise time.

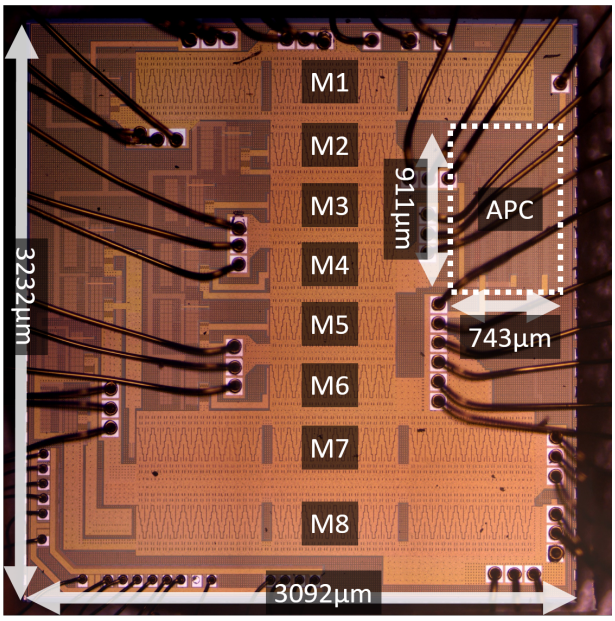


**Fig. 13**: Microscope photo of 48 V-12 V switched-capacitor converter with the integrated power stage and active pre-charge circuit.

The switched-capacitor voltages can be seen in Fig. 12. Here it can be seen that the voltages reach the desired steady-state voltages and that the current sourcing capabilities are able to match the slew rate of the input voltage ramp. This ensures that the power switches in the integrated power stage never see more than the 25 V that they are rated for during start-up. Note that the measurement in Fig. 12 is done before enabling the external clock.

In Fig. 14 the current waveform going from the $f_7$ node into the chip can be seen when the clock

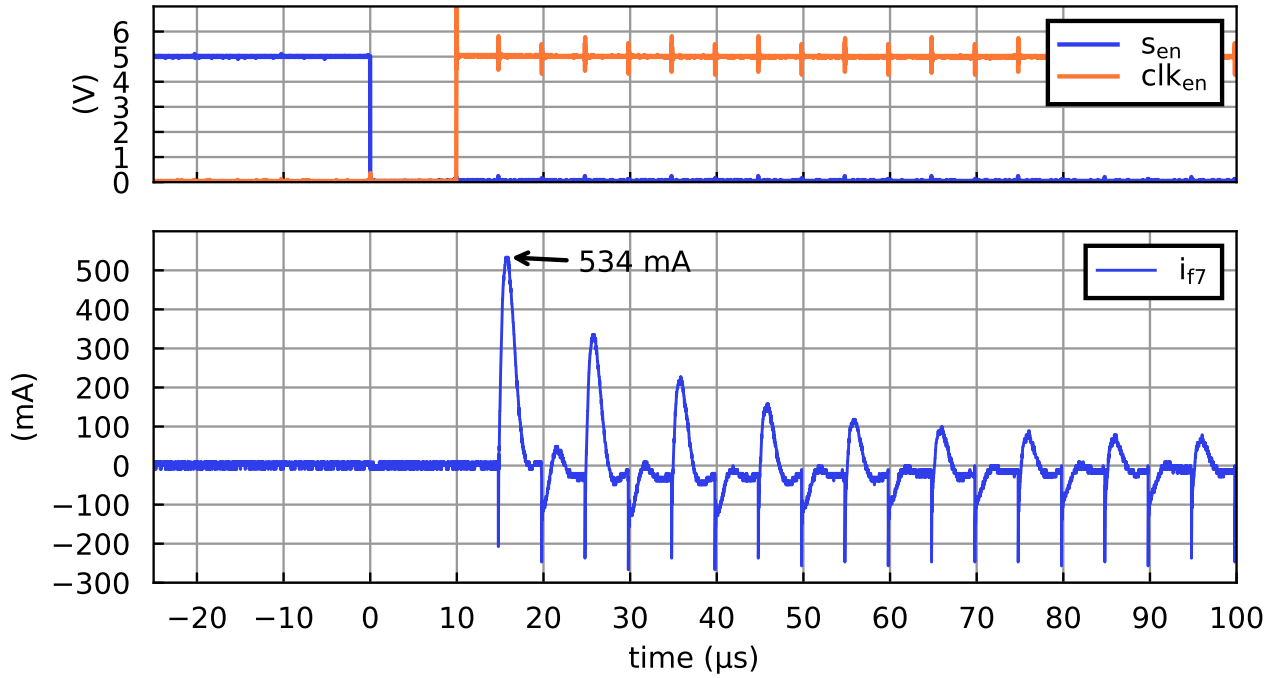


**Fig. 14**: Current from external capacitor going from $f_7$ into the IC, $i_{f7}$, when the clock is first enabled.

is enabled for the first time. The current is measured with a Tektronix P6022 120 MHz current probe clamp used in a current loop. This method does add extra parasitic inductance and resistance from the wires in the current loop. This affects the peak current compared to the simulation results. The bandwidth of the current probe is 120 MHz. The maximum peak current is 534 mA. It can be seen that the peak current settles to the expected steady state current after 6 switching periods.

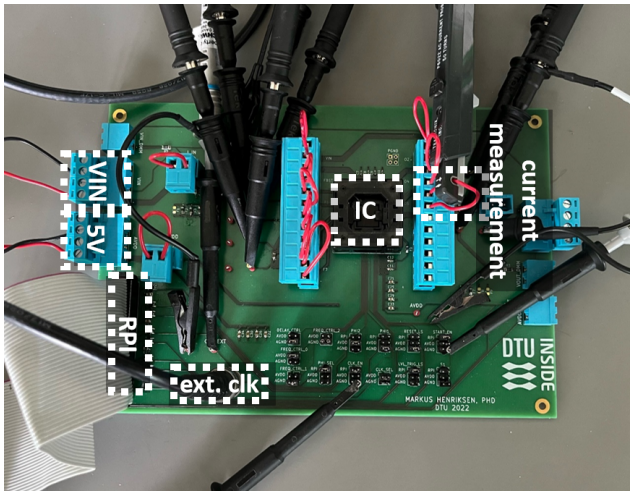


**Fig. 15**: Test setup used for verifying measurements of the active integrated start-up sequence. Showing the 48 V and 5 V supply voltages, external clock (ext. clk), Raspberry Pi interface for digital control (RPI), the socket for the IC and the current loop used for the current measurement.

It was not possible to make a measurement of the quiescent current of the active pre-charge circuit, since it is connected to the input of the switched-capacitor converter. Therefore, the 105 µA quiescent current from simulation cannot be verified. This current draw is from the resistor string in the active pre-charge circuit and is therefore expected to vary with the variation of the large resistor string.

## 5 Performance discussion

The presented measurements of the active integrated start-up method shows that it safely charges the capacitors of the power converter. The start-up procedure limits the inrush current going into the chip whenever the clock is enabled as expected from simulation. The maximum current measured is 534 mA going into $f_7$, $i_{f7}$, which is below the simulation result of 1.5 A. This is

likely due to the added parasitic inductance and resistance from the printed circuit board and current loop used for the current measurement. From Fig. 14 it can also be seen that the peak current settles to its steady-state value within only a few clock cycles. Naturally, no baseline without the start-up procedure can be included for measurement comparison, since that would be destructive for the chip. Instead, the simulation results for start-up without a dedicated start-up procedure can be used as baseline comparison. This shows that the presented method improves by reducing the peak current from an expected 40 A to 534 mA and that it ensures that the 25 V power switches used for the integrated power stage ($M_1 - M_8$) are protected from exceeding these voltages.

# 6 Conclusion

Two start-up methods have been designed and presented for a 48 V-12 V switched-capacitor converter with an integrated power stage implemented in a 180 nm SOI process. First an analysis of the challenges in start-up for a switched-capacitor converter has been presented. Next, the two proposed approaches have been shown and the trade-offs of each method presented. The first method controls the top switch of the integrated power stage to charge all capacitors during input ramp-up together with an extra discrete capacitor and careful sizing of the capacitors to ensure that all capacitors are charged to the same voltages. The second method uses a fully integrated active pre-charge circuit to charge the discrete capacitors to the desired steady-state voltages before enabling the power converter. Both implementations have been verified in simulation and compared to a baseline of 40 A inrush current from not using a dedicated start-up circuit. The passive method does not consume any additional static current, but does increase the converter size with an added capacitor, additionally it uses sub-optimal capacitor sizing for the converter, this limits the peak inrush current to 6.5 A. The active start-up method has been verified with experimental measurements, where the IC have been powered up with the presented start-up sequence. This showed a maximum peak inrush current of 534 mA, which is within the operating thresholds of the bonding wires used in the packaging. Finally, a discussion of the experimental results is presented.

# Declarations

- Funding
  Not applicable
- Competing interests
  I declare that the authors have no competing interests as defined by Springer, or other interests that might be perceived to influence the results and/or discussion reported in this paper.
- Ethics approval
  Not applicable
- Consent to participate
  Not applicable
- Consent for publication
  Not applicable
- Availability of data and materials
  The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.
- Code availability
  Not applicable
- Authors' contributions
  Markus Mogensen Henriksen contributed to the conception of work, wrote the main manuscript, prepared all figures and tables and performed the presented measurements. Dennis Øland Larsen and Pere Llimós Muntal contributed to the conception of the work, supervised the design and the measurements. All authors reviewed the manuscript.

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# C A Design Methodology for High-Voltage, Highly-Integrated Switched-Capacitor Power Converters, and Implementation at 48V-12V, 23 $W/cm^3$ and 93.5% Peak Efficiency

*IEEE Transactions on Power Electronics*

***Markus Mogensen Henriksen**, Dennis Øland Larsen, Pere Llimós Muntal*

Status: Published (Early access)
DOI: 10.1109/TPEL.2023.3288592



# A Design Methodology for High-Voltage, Highly-Integrated Switched-Capacitor Power Converters, and Implementation at 48 V-12 V, 23 W/cm3 and 93.5 % Peak Efficiency

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*Published in:*
IEEE Transactions on Power Electronics

*Link to article, DOI:*
10.1109/TPEL.2023.3288592

*Publication date:*
2023

*Document Version*
Peer reviewed version

# A Design Methodology for High-Voltage, Highly-Integrated Switched-Capacitor Power Converters, and Implementation at 48 V-12 V, 23 W/cm$^3$ and 93.5 % Peak Efficiency

Markus Mogensen Henriksen, *Student Member, IEEE,* Dennis Øland Larsen, *Member, IEEE,* Pere Llimós Muntal

***Abstract*—In this work a design methodology and key considerations for high-voltage and highly-integrated switched-capacitor power converters is presented. The design methodology describes the power losses in high-voltage applications, where switching losses and gate-driver losses start becoming dominant compared to fully integrated, low voltage and low power applications. The design methodology is applicable for any highly-integrated switched-capacitor topology. To verify the design methodology a $48\,\mathrm{V}$-$12\,\mathrm{V}$ ladder switched-capacitor power converter in a $180\,\mathrm{nm}$ SOI BCD process, with external capacitors is implemented. The floating gate-drivers and a clock controller responsible for the power switch control are also presented. The peak efficiency of the proposed power converter is measured to be $93.5\,\%$, and $24.5\,\mathrm{W}$ maximum output power, resulting in a power density of $23\,\mathrm{W/cm^3}$.**

***Index Terms*—High-voltage, switched-capacitor converter, integrated power converter, power losses, data center application**

## I. Introduction

HIGH-VOLTAGE power converters have traditionally been inductor based and implemented using discrete components. This method can achieve high efficiency for a wide range of voltages and currents [1]–[3]. The main drawbacks include bulky and expensive inductors and a high-voltage rating requirement for the power switches, since they need to handle the full input voltage, in most topologies. In the pursuit of increasing the power density of power converters together with recent advancements in high-voltage semiconductor technology, highly-integrated power converters are becoming interesting in applications in which so far the discrete power converters are dominating [4]–[14]. In this work highly-integrated power converters refer to power converters with an integrated power stage and gate-drivers and high-voltage refers to converter input voltages that exceeds the maximum voltage of the digital logic cells used in the given fabrication process. These applications include power converters in LED drivers, servers in data centers or dc-dc converters in automotive. Some of the advantages of highly-integrated power converters are a reduced production cost and an increased power density. The increase in power density comes partially from the monolithic integration itself and that the switching frequency can be increased leading to smaller discrete passive components. The main disadvantages are complicated integrated circuit (IC) design and robustness challenges from parasitic inductance and resistance due to the interface with the IC [15]. The highly-integrated power converters are traditionally switched-capacitor power converters with discrete capacitors [16]. In the switched-capacitor power converters, low resistance power switches connects capacitors in different configurations in multiple clock phases to realize various voltage ratios dependent on the topology. This means that the maximum voltage across the power switches is usually lower compared to traditional inductor-based power converters, leading to the possibility of using lower voltage

Manuscript submitted March 31, 2023

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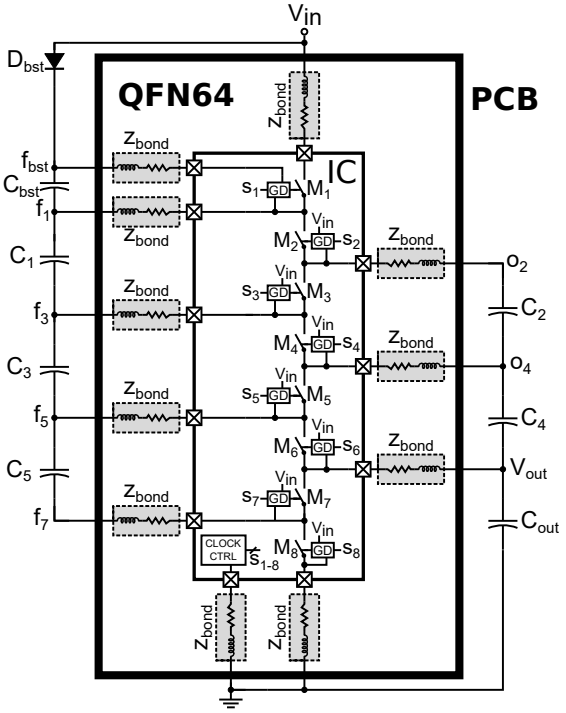


Fig. 1. A switched-capacitor power converter with an integrated power stage, gate-drivers and clock controller and external capacitors showing the bonding wire parasitics in the QFN64 chip package.

devices with better on-resistance while also leading to a lower V-A product figure-of-merit [17]. The hard-charging of the capacitors in the switched-capacitor power converter lead to high capacitor peak currents, which increases the RMS current of the external capacitors. To lower these peak currents hybrid switched-capacitor topologies, using one or multiple inductors to achieve soft-charging, has gained interest recently [7], [8], [18], [19]. The compatibility of a switched-capacitor topology to achieve resonant and soft-charging using a single inductor is documented in [20] and [21]. These hybrid converters have mostly been discrete solutions [22]–[24] but also highly-integrated hybrid converters have been published [25]–[27].

In 2021 [6] presented a $48\,\mathrm{V}$ to 3-$3.6\,\mathrm{V}$ highly-integrated 4:1 hybrid Dickson power converter for automotive applications with a high peak efficiency of $95.3\,\%$ and a single $4.7\,\mu\mathrm{H}$ inductor. The use of a Dickson switched-capacitor power converter ensures the conversion from $48\,\mathrm{V}$-$12\,\mathrm{V}$, while adding an inductor enables regulation down to the desired output voltage. The work in [6] deals with some of the challenges of high-voltage, highly-integrated switched-capacitor converter such as safe start-up and floating gate-driver design. In 2022 [7] presented a $48\,\mathrm{V}$ to $1\,\mathrm{V}$ hybrid converter combining a 3:1 ladder converter and a capacitor assisted dual-inductor filter. It achieves a peak efficiency of $91.1\,\%$ and is able to operate at a switching frequency of $5\,\mathrm{MHz}$, meaning that the inductor size can be decreased to $2 \times 0.82\,\mu\mathrm{H}$. In 2023 [25] presented a single-inductor multi-stage (SIMS) hybrid converter. It achieves a wide input voltage range of $5\,\mathrm{V}$ to $24\,\mathrm{V}$ while providing a regulated output voltage range of $2.8\,\mathrm{V}$-$4.2\,\mathrm{V}$. It achieves this by cascading two highly-integrated switched-capacitor converter stages connected by a single inductor and having 4 operating modes to achieve a high peak efficiency of $94.8\,\%$ and a maximum output power of $21\,\mathrm{W}$. Both [6], [7] and [25] discusses how to introduce inductive elements to improve on the switched-capacitor power converter performance, combining the high conversion ratio capabilities of the switched-capacitor converter with the soft-charging and output voltage regulation benefits of the buck converter. These works do however not discuss in detail the proper design methodology for the switched-capacitor power converter design itself. The work in [17] discusses in great detail some of these considerations but is mostly focused on fully integrated and low voltage applications, where especially gate-driver losses can mostly be neglected. In [28] a sizing methodology for fully integrated switched-capacitor converters maximizing efficiency under area and load power constraints is presented. The work in [28] does however not deal with conditions where the power converter input voltage exceeds the power switch and flying capacitor voltage ratings. It does also not provide any new insight when discrete flying capacitors are used such as in highly-integrated switched-capacitor power converters.

This work presents a design methodology and the key considerations when designing high-voltage, highly-integrated switched-capacitor converters and demonstrates the approach by designing a switched-capacitor power converter. The methodology can be used for any highly-integrated switched-capacitor power converter topology. This includes the optimal sizing of the power switches by defining the power losses in the switched-capacitor power converter also including the gate-driver losses which start becoming dominant in high-voltage applications and the optimal external discrete capacitors scaling. Section II presents the highly-integrated switched-capacitor power converter fundamentals, presenting the various power losses and reformulates them as functions of total switch area, switching frequency and load current to allow for optimization for high efficiency. It also derives and presents a novel expression for the optimal number of external capacitors to use for a given printed circuit board (PCB) capacitor footprint area derived by Lagrange Multipliers, which can be used for any switched-capacitor converter topology using discrete flying capacitors. Section III shows the implementation of a $48\,\mathrm{V}$-$12\,\mathrm{V}$ ladder highly-integrated switched-capacitor power converter with integrated floating gate-drivers, a clock controller and the optimization method for the design of the integrated power stage designed in a $180\,\mathrm{nm}$ Silicon-On-Insulator (SOI) process. Section IV presents the experimental measurement results of the $48\,\mathrm{V}$-$12\,\mathrm{V}$ highly-integrated switched-capacitor power converter showing the efficiency measurements for various output load currents and switching frequencies, transient load response, switching node at maximum output load and thermal performance and compares it to the proposed model and the simulation results. Section V discusses the experimental results and compares it to other designs. Finally, section VI concludes the work.

## II. HIGHLY-INTEGRATED SWITCHED-CAPACITOR POWER CONVERTER METHODOLOGY

In Fig. 1 a switched-capacitor step down converter with a fixed voltage ratio of 4:1 using a ladder topology can be seen. The power converter consists of an integrated power stage, gate-drivers and clock controller. The capacitors are external multi layer ceramic capacitors (MLCC) since they offer higher capacitance density compared to on-chip capacitors. The power switches $M_1$-$M_8$ are driven by floating gate-drivers, which inputs, $s_1$-$s_8$, are the gate signals generated by the clock controller. The gate signals $s_1$, $s_3$, $s_5$ and $s_7$ are switched in phase ($\varphi_1$) and $s_2$, $s_4$, $s_6$ and $s_8$ are switched in phase ($\varphi_2$). The clock controller is responsible for clock generation and dead-time control between the two phases. In Fig. 1 the parasitic resistance and inductance from the wire bonding is also shown. These bonding wires affect the performance and reliability of the power converter [15]. The challenge of optimal design of both the size of the power switches and capacitors in switched-capacitor power converters is well

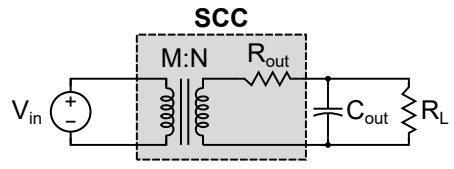


Fig. 2. Model of a switched-capacitor converter (SCC) with an ideal lossless transformer and a series resistance. $R_L$ represents a resistive load.

described in [29]. This work is mostly focused on low voltage, low power designs seeking to minimize the various power losses. These losses includes the charging and discharging of the capacitors and the conduction and switching losses of the power switches. The behavior of a switched-capacitor power converter can be modelled as seen in Fig. 2. Here the switched-capacitor converter is modelled as an ideal lossless transformer with a winding ratio of $M/N$ and an output series resistance $R_{out}$. The winding ratio $M/N$ relates to the fixed conversion ratio of the switched-capacitor converters, which is topology and implementation dependent. The series output resistance, $R_{out}$, is a function of both the power converter switching frequency and total switch conductance and can be approximated as:

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{1}$$

where $R_{SSL}$ and $R_{FSL}$ are the slow-switching limit resistance and fast-switching limit resistance respectively. The slow-switching limit models the losses when charging and discharging of the capacitors and is a function of both frequency and capacitor size:

$$R_{SSL} = \sum_i \frac{a_{c,i}^2}{C_i \cdot f_{sw}} \tag{2}$$

where $a_{c,i}$ is the topology dependent capacitor charge multiplier vector describing the normalized charge for the respective capacitor, $C_i$, for each switching period. $f_{sw}$ is the frequency of the power converter. From (2) it can be seen that the losses are decreased by increasing capacitance and frequency.

The fast-switching limit, $R_{FSL}$ models the conduction losses of the power switches and is a function of the effective on-resistance of the power switches ($R_{ds}$).

$$R_{FSL} = 2\left(\sum_i R_{ds,i} a_{r,i}^2\right) \tag{3}$$

where $a_{r,i}$ is the topology dependent switch charge multiplier vector describing the normalized charge for each power switch. $R_{ds,i}$ is the equivalent on-resistance of the power switches and is dependent on the process dependent area specific resistance of the power switch devices used and the total chip area designated for the power switches:

$$R_{ds,i} = \frac{K_{A,i}}{A_{sw} \cdot \frac{a_{r,i}}{\sum_k (a_{r,k})}} \tag{4}$$

Where $A_{sw}$ is the total switch area, $K_{A,i}$ is the area specific resistance for the power switch device used. In the case of the ladder topology the maximum drain-source voltage of all the switches is the same:

$$V_{ds,max} = \frac{N}{M} V_{in} \tag{5}$$

This means that the same devices can be used for all power switches and (3) can be written as:

$$R_{FSL} = \frac{2}{G_{tot}} \left(\sum_i \|a_{r,i}\|\right)^2 \tag{6}$$

Where $G_{tot}$ is the total switch conductance, since all $R_{ds}$ in (4) have the same area specific resistance ($K_A$). The power loss due to $R_{out}$ is dependent on the output load current and can be described as:

$$P_{rout} = I_{out}^2 \cdot R_{out} \tag{7}$$

This means, that a target load current is required for choosing proper capacitor sizes and total switch area.

In high-voltage applications there are additional losses that should be taken into account, since their impact scales with the input voltage. These are the losses that are related to the parasitic capacitances of the power switches. The switching losses of the power switches are the losses from charging and discharging the output capacitor, $C_{oss} = C_{ds} + C_{dg}$ of the power switches. The switching loss of a single power switch can be described by:

$$P_{sw} = V_{ds} \cdot Q_{oss} \cdot f_{sw} \tag{8}$$

Where $Q_{oss}$ is the total charge required for charging/discharging the drain-source capacitance of the power switch. The drain-source charge, $Q_{oss}$ can be rewritten into:

$$Q_{oss} = C_{oss} \cdot V_{ds} \tag{9}$$

This capacitance is dependent on the type of power switch and the total area and be expressed as:

$$C_{oss} = \beta_{coss} \cdot \frac{A_{sw} \cdot a_{r,i}}{\sum_k a_{r,k}} \tag{10}$$

Where $\beta_{coss}$ is the specific drain-source capacitance per switch area and $A_{sw}$ is the total power switch area. Using this we can rewrite (8) as dependent on both switching frequency and total power switch area:

$$P_{sw} = f_{sw} \cdot \sum_i \left(V_{ds,i}^2 \cdot \beta_{coss,i} \cdot \frac{A_{sw} \cdot a_{r,i}}{\sum_k a_{r,k}}\right) \tag{11}$$

### A. Gate-Drivers

In highly-integrated power converters the power switches are controlled by integrated gate-drivers. The gate-drivers are referenced to the source of their respective power switch. The supply voltage of the gate-driver is dependent on the implementation. Various solutions for supplying floating gate-drivers have been investigated in other works, utilizing either charge-pump and bootstrapping techniques [4], [18] or internal supplies of the switched-capacitor converter itself [9]. The power consumption of the gate-drivers is therefore dependent on not only the size of the switch it is driving (gate capacitance of power switch) but also the input voltage, topology and implementation.

The total power consumption of all the gate-drivers can be described as:

$$P_{gd} = \sum_i \left(V_{DD,i} \cdot Q_{gg,i} \cdot f_{sw}\right) \tag{12}$$

Where $V_{DD,i}$ is the supply voltage of the specific gate-driver and $Q_{gg,i}$ is the total gate charge required to charge the power switch gate capacitance. The gate-charge in (12) can be rewritten as:

$$Q_{gg,i} = C_{gg,i} \cdot V_{gs} \tag{13}$$

Where $V_{gs}$ is the required gate-source voltage to turn on the power switch and $C_{gg,i}$ is the equivalent linear gate capacitance. The gate capacitance is dependent on the area specific gate capacitance ($\beta_{cgg}$), for the power switches used and the total switch area:

$$C_{gg,i} = \beta_{cgg,i}\left(\frac{A_{sw}a_{r,i}}{\sum_k a_{r,k}}\right) \tag{14}$$

The total gate-driver losses can then be described as:

$$P_{gd} = f_{sw}\cdot V_{gs}\sum_i\left(V_{DD,i}\cdot\beta_{cgg,i}\left(\frac{A_{sw}a_{r,i}}{\sum_k a_{r,k}}\right)\right) \tag{15}$$

These are only the losses related to driving the gate capacitance of the power switches. The quiescent current of the gate-driver is implementation dependent and contributes to the total gate-driver power consumption.

### B. External Flying Capacitor Sizing

For highly-integrated power converters with external capacitors it is often required to have multiple capacitors in parallel to fulfill the optimal design criteria described in [29]. This is a trade-off between improving the $R_{SSL}$ and using additional PCB footprint area for the discrete capacitors ($A_{cap}$). The scaling of each of the flying capacitors is topology dependent and can be expressed as:

$$C_i = C_i^{'}\cdot\lfloor K_{c,i}\rfloor \tag{16}$$

Where $C_i$ is the total capacitance of each flying capacitor, $C_i^{'}$ is the dc bias derated capacitance of each unit flying capacitor and $\lfloor K_{c,i}\rfloor$ is the topology dependent optimized capacitor component scaling parameter rounded down to the nearest integer. $K_{c,i}$ expresses the optimum number of unit flying capacitors ($C_i^{'}$) in parallel for each flying capacitor. We find $K_{c,i}$ by using Lagrange Multipliers. The Lagrangian consists of an expression for the impedance at the slow-switching limit to be minimized $f(\mathbf{k})$, the constraint on the total capacitance area $h(\mathbf{k})$ and the Lagrange multiplier $\lambda$:

$$\mathcal{L}(\mathbf{k},\lambda) = f(\mathbf{k}) + \lambda h(\mathbf{k}) \tag{17}$$

We want to minimize $f(\mathbf{k})$ under the constraint of the total area $h(\mathbf{k})$, these can be expressed as:

$$\begin{aligned} f(\mathbf{k}) &= \sum_{i=1}^{N_{cap}}\frac{a_{c,i}^2}{K_{c,i}\cdot C_i^{'}} \\ h(\mathbf{k}) &= \sum_{i=1}^{N_{cap}} K_{c,i}A_{c,i} - A_{cap} \end{aligned} \tag{18}$$

Where $A_{cap}$ is the total footprint area of all the external discrete capacitors, $A_{c,i}$ is the footprint area of each unit capacitance and $N_{cap}$ are the number of flying capacitors in the topology. Inserting (18) into (17):

$$\mathcal{L}(\mathbf{k},\lambda) = \sum_{i=1}^{N_{cap}}\frac{a_{c,i}^2}{K_{c,i}\cdot C_i^{'}} + \lambda\left(\sum_{i=1}^{N_{cap}} K_{c,i}A_{c,i} - A_{cap}\right) \tag{19}$$

Taking the partial derivative of $\mathcal{L}(\mathbf{k},\lambda)$ with respect to $K_{c,i}$, setting it equal to zero and isolating for $K_{c,i}$ yields:

$$\begin{aligned} \frac{\partial\mathcal{L}}{\partial K_{c,i}} &= \frac{-a_{c,i}^2}{K_{c,i}^2 C_i^{'}} + \lambda A_{c,i} = 0 \\ K_{c,i} &= \frac{a_{c,i}}{\sqrt{\lambda A_{c,i}C_i^{'}}} \end{aligned} \tag{20}$$

We then take the partial derivative of $\mathcal{L}(\mathbf{k},\lambda)$ with respect to $\lambda$, set it equal to zero and use the expression for $K_{c,i}$ found in (20):

$$\begin{aligned} \frac{\partial\mathcal{L}}{\partial\lambda} &= \sum_{i=1}^{N_{cap}} K_{c,i}A_{c,i} - A_{cap} = 0 \\ &= \sum_{i=1}^{N_{cap}}\left(\frac{A_{c,i}a_{c,i}}{\sqrt{\lambda A_{c,i}C_i^{'}}}\right) - A_{cap} = 0 \end{aligned} \tag{21}$$

Isolating $\sqrt{\lambda}$ in (21) yields:

$$\sqrt{\lambda} = \frac{1}{A_{cap}}\sum_{i=1}^{N_{cap}}\left(\frac{\sqrt{A_{c,i}a_{c,i}}}{\sqrt{C_i^{'}}}\right) \tag{22}$$

Inserting (22) into (20) then yields the optimized expression for $K_{c,i}$:

$$K_{c,i} = \frac{A_{cap}\cdot a_{c,i}}{\sqrt{A_{c,i}\cdot C_i^{'}}\cdot\sum_{j=1}^{N_{cap}}\left(\frac{\sqrt{A_{c,j}}a_{c,j}}{\sqrt{C_j^{'}}}\right)} \tag{23}$$

Note that since $K_{c,i}$ depends on the capacitor charge multiplier vector $\mathbf{a_c}$ it is topology dependent. $K_{c,i}$ therefore tells for a given total capacitance footprint area, how many capacitors to put in parallel for each flying capacitor. This optimal capacitor scaling can be used for any highly-integrated switched-capacitor power converter topology.

## III. Implementation

To show how the presented power losses can be used to design high-voltage, highly-integrated switched-capacitor power converters a $48\,\mathrm{V}$-$12\,\mathrm{V}$ ladder topology switched-capacitor power converter is implemented in a $180\,\mathrm{nm}$ SOI process. The integrated power stage and the sizing of the external flying capacitors are designed using the proposed sizing methodology presented in Section II. The proposed converter is intended as an intermediate power converter in applications such as automotive or data centers dc power bus. The output voltage of the implemented power converter is therefore unregulated. The schematic of the proposed design can be seen in Fig. 1.

### A. Flying Capacitors and Power Stage Design

For a 4:1 ladder topology, the charge multiplier vector, $\mathbf{a_c}$, describing the output normalized capacitor charge flow vector is:

$$\mathbf{a_c} = \left[\frac{1}{4},\frac{1}{4},\frac{2}{4},\frac{2}{4},\frac{3}{4}\right] \tag{24}$$

For the ladder topology the voltage rating of each flying capacitor are all equal to $V_{C,max} = V_{out}$. This means that the same external discrete capacitor can be used for all flying

This article has been accepted for publication in IEEE Transactions on Power Electronics. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2023.3288592



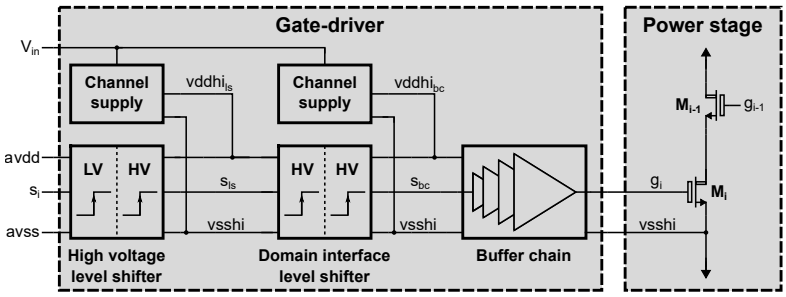


Fig. 3. Diagram of the implemented floating gate-driver for driving switches $M_1$-$M_8$.

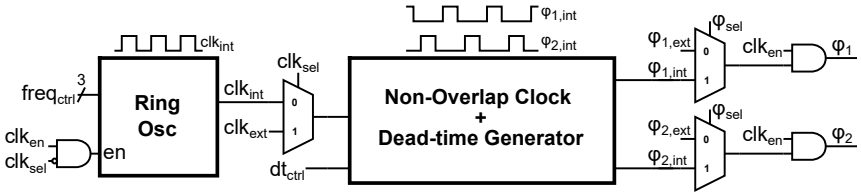


Fig. 4. Digital clock controller with integrated ring oscillator, non-overlapping clock and dead-time generator.

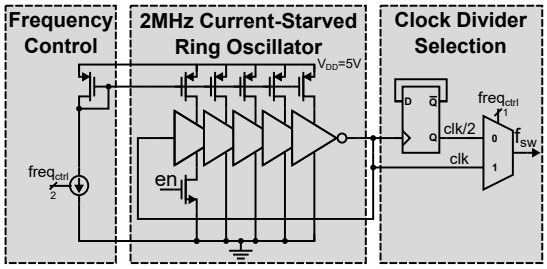


Fig. 5. 2 MHz, 9-stage current-starved ring oscillator with 3-bit frequency selection.

capacitors. A total capacitance area of $A_{cap} = 22.5\,\mathrm{mm}^2$ was chosen for the footprint area of the capacitors and the GRM21BC71E106KE11, 10 µF MLC capacitors from Murata [30] are used. From [30] it can be seen that the the maximum frequency is around 2 MHz, before becoming inductive and that it has a dc bias capacitance derating of $-73.1\,\%$ at 12 V. Using (23) then leads to:

$$\lfloor K_c \rfloor = [1,\ 1,\ 2,\ 2,\ 3] \tag{25}$$

The total 12 V derated capacitance for each flying capacitor is therefore:

$$\mathbf{C_{fly}} = \begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \end{bmatrix} = \begin{bmatrix} 2.69\,\mu\mathrm{F} \\ 2.69\,\mu\mathrm{F} \\ 5.38\,\mu\mathrm{F} \\ 5.38\,\mu\mathrm{F} \\ 8.07\,\mu\mathrm{F} \end{bmatrix} \tag{26}$$

The power switches should be able to handle a maximum $V_{ds}$ voltage of 12 V. Some margin is added and 20 V devices are used for the integrated power stage. The power switches are scaled by their switch charge multiplier vector for a 4:1 ladder topology:

$$\mathbf{a_r} = \left[\frac{1}{4},\ \frac{1}{4},\ \frac{1}{4},\ \frac{1}{4},\ \frac{1}{4},\ \frac{1}{4},\ \frac{3}{4},\ \frac{3}{4}\right] \tag{27}$$

The switch conductance, and thereby the switch areas are then scaled by $a_r \cdot N$, where N is the conversion ratio. In this case meaning that $M_{7,8}$ should have three times the conductance of $M_{1-6}$. To further ensure safe operation during start-up the top switch ($M_1$) is chosen as a 60 V device instead. This device has a worse area specific resistance and a larger area specific capacitances ($\beta_{cgg}$, $\beta_{coss}$). This device is scaled such that the $R_{ds}$ of $M_1$ corresponds to that of $M_2 - M_6$.

The area specific gate capacitance ($\beta_{cgg}$) can be found from simulation by observing the charge required for turning on the transistor for different total switch areas. This simulation was performed for the used switches with a drain-source voltage of 12 V and a step voltage on the gate-source of the transistor. Similarly the area specific drain-source capacitance ($\beta_{coss}$) was found from simulation with a gate-source voltage of 0 V and a step voltage across the drain-source of the transistor. These parameters are used to designate the desired total switching area and which sets the requirements for the gate-driver capabilities.

### *B. Gate-Driver Implementation*

The structure of the designed gate-drivers can be seen in Fig. 3. These are based on the ones used in [9]. In this work two channel-supply generators consisting of a shunt-regulator generates a 5 V supply for a level shifter and a buffer chain referenced to the vsshi node, which is connected to the source of the respective power switch. The channel supplies are split in two, since the channel supply for the buffer chain will have a large voltage drop when charging the gate capacitance of

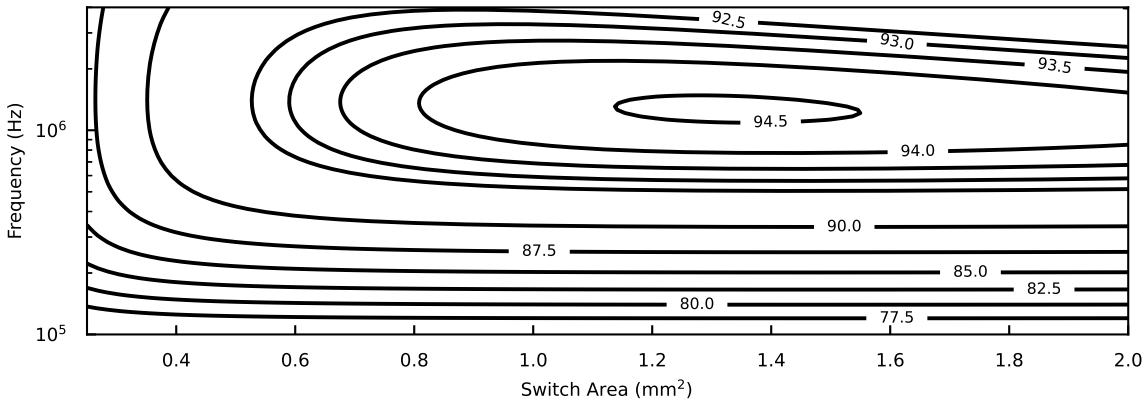


Fig. 6. Efficiency of 48 V-12 V switched-capacitor power for different switching frequencies ($f_{sw}$) and total for power switch area ($A_{sw}$) using the proposed model. Calculated for 2 A load current.

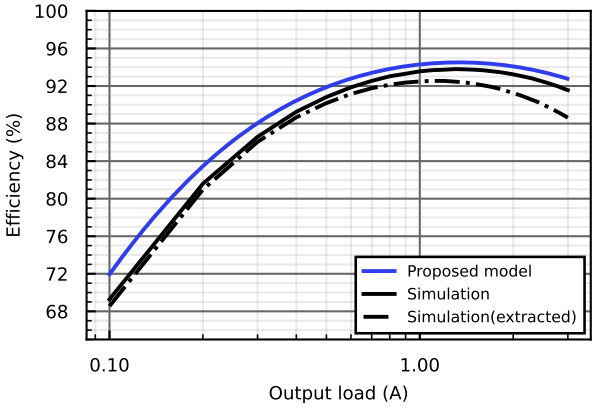


Fig. 7. Efficiency curve for output load current of 100 mA to 3 A with a $f_{sw} = 1$ MHz for the proposed model and for the simulated results.

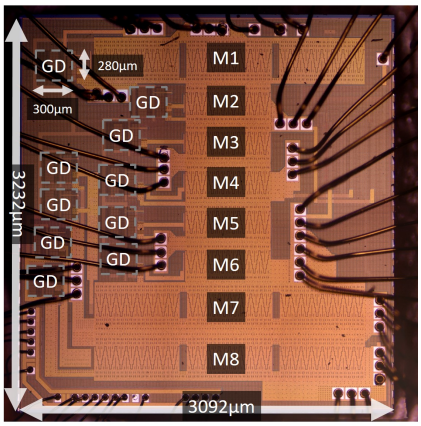


Fig. 8. Microscope photo of the 48 V-12 V switched-capacitor power converter IC with an integrated power stage ($M_1 - M_8$) and gate-drivers (GD).

the power switch. Since the channel supply for the buffer chain is noisy, a level shifter is used to interface between the two channel supplies, $\mathrm{vddhi_{ls}}$ and $\mathrm{vddhi_{bc}}$. In this work, we have decided to supply the channel-supplies from the power converter input instead of across the external capacitors as seen in [9]. This enables for a faster and more robust start-up at the cost of a higher power consumption.

In Fig. 1 it can be seen that the gate-driver supply voltages are dependent on which power switch they are driving. For the top gate-driver, driving $M_1$, the supply voltage is only $\frac{1}{4}V_{in}$, whereas for the bottom gate-driver, driving $M_8$, the supply voltage is the full input voltage of $V_{in}$. The gate-driver supply voltages can be described as:

$$\mathbf{V_{DD}} = V_{in} \cdot \left[\frac{1}{4}, \frac{1}{4}, \frac{2}{4}, \frac{2}{4}, \frac{3}{4}, \frac{3}{4}, 1, 1\right] \tag{28}$$

Since the two bottom power switches are three times larger, than the rest, the driving capabilities of the gate-drivers driving these are increased to ensure equal rise-time for all power switches.

The large gate-drain capacitance of the power switches can lead to self turn-on, whenever the drain node is switched. This will lead to shoot-through current and is undesirable. The pull-down capabilities of the buffer chain is therefore designed to handle this inrush current from the gate-drain capacitor, ensuring that the voltage seen on the gate-source voltage of the power switch, does not exceed the threshold voltage of the device. The simulated quiescent current of the implemented floating gate-driver is 52.34 µA leading to a total quiescent current for all the gate-drivers of 523.4 µA.

### C. Clock Controller

The implementation of the clock controller can be seen in Fig. 4. The designed clock controller consists of an integrated 2 MHz ring oscillator with a 3-bit frequency trimming bit $\mathrm{freq_{ctrl}}$. For further debugging in the laboratory the option of having an external clock is also enabled by $\mathrm{clk_{sel}}$. The clock controller also consists of a non-overlapping clock generator, that generates the two switching phases for the power stage. The non-overlapping clock generator has a 1-bit signal for

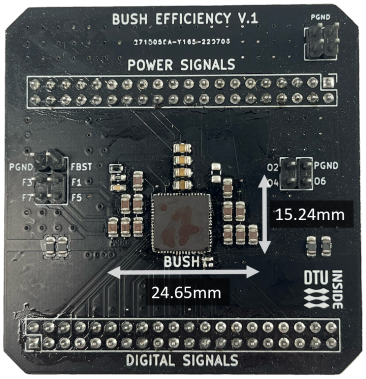


Fig. 9. Close-up of test PCB for experimental measurements.

choosing between two different dead-times. These dead-times are 20 ns and 35 ns. The selection signal $\varphi_{\text{sel}}$ selects either the internal phases generated by the non-overlapping clock generator or from an external signal generator.

In Fig. 5 the implemented 2 MHz current-starved ring oscillator can be seen. The most significant bit of the trimming signal, $\text{freq}_{\text{ctrl}}$ chooses either the 2 MHz clock signal from the ring oscillator or the clock divider output of 1 MHz. The two other bits of $\text{freq}_{\text{ctrl}}$ trims the bias current for the PMOS cascodes responsible for the current-starving of the ring oscillator. The clock controller is supplied by an external 5 V supply.

### D. Power Losses

The total power loss from the switched-capacitor power converter can be described as:

$$P_{loss} = P_{rout} + P_{sw} + P_{gd} \tag{29}$$

With the chosen external capacitors, power switch scaling and extracted parasitic switch capacitances the power loss becomes a function of the total switch area, frequency and load current. In this work the power converter is designed for a maximum of 2 A output current. In Fig. 6 a contour plot of the calculated power converter efficiency for a 48 V-12 V ladder converter

TABLE I
COMPONENT LISTING OF IMPLEMENTED CONVERTER.

| Component | Part Number | Parameters |
|---|---|---|
| IC | | ASIC, QFN package, 64pins |
| $C_{bst}$ | GCJ188R71E473KA01D | 25 V, 47 nF |
| $C_1$-$C_5$ | GRM21BC71E106KE11K | 25 V, 10 µF |
| $D_{bst}$ | 1SS400-G | 90 V, 100 mA |
| Microcontroller | Raspberry Pi 3 | |

using the proposed model based on power loss expressions in (7), (11) and (15) and the optimum external capacitor scaling based on (23) can be seen as a function of both total switch area ($A_{sw}$) and switching frequency ($f_{sw}$). From Fig. 6 it can be seen that a maximum exists at around $A_{sw} = 1.3\,\text{mm}^2$ and for a switching frequency of around 1.1 MHz. Note that this is not taking into account the added resistance and inductance of the bonding wires for the interface with the QFN package used. These bonding wires lower the peak efficiency and have an impact on the effective output resistance of the power converter. Furthermore, due to the inductance of the bonding wires together with any PCB trace inductance and series inductance in the external capacitors the power loss dependency on the switching frequency is also expected to be higher than what is modelled here. This is not an issue, since the final switching frequency can be adjusted using the trimming bits of the ring oscillator. In Fig. 7 the calculated efficiency for an output load current from 0.1 A to 3 A can be seen. The calculations are based on the proposed model with the power losses described in section II. The calculations are based on a total switch area of $1.365\,\text{mm}^2$ and a switching frequency of 1 MHz. In Fig. 7 the simulated efficiency with and without modelling the bonding wire parasitic resistance and the post-layout extracted view of the integrated power stage can also be seen.

It can be seen from Fig. 7 that the slopes of the efficiency curves for higher output currents is similar for the proposed model and the simulation results indicating that the output resistances are similar. The offset between the proposed model

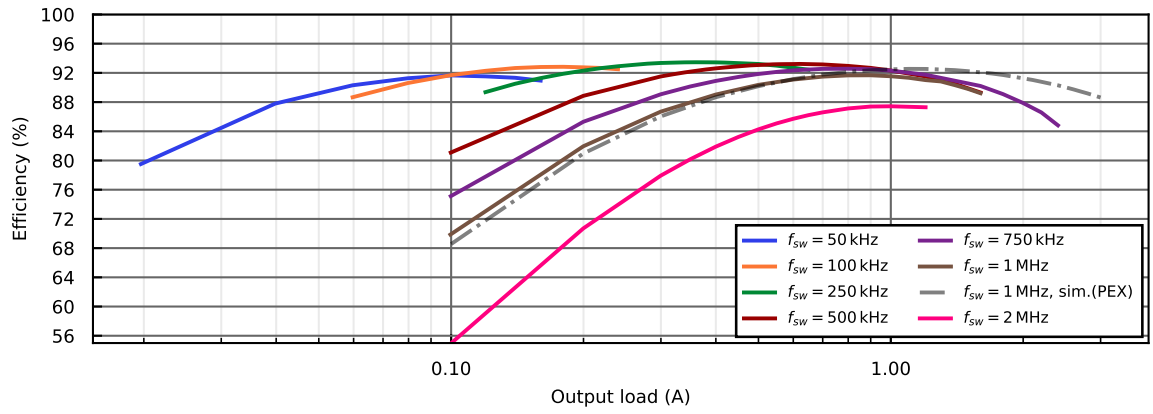


Fig. 10. Measured efficiency of 48 V-12 V switched-capacitor power for different load currents and switching frequencies.

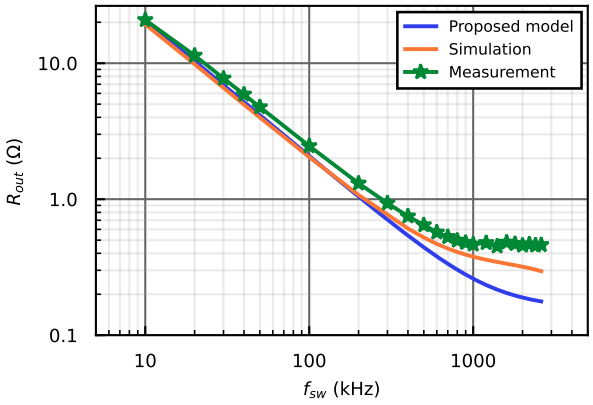


Fig. 11. Comparison of output resistance for the proposed model, simulation and measurement results. With 100 mA output load current.

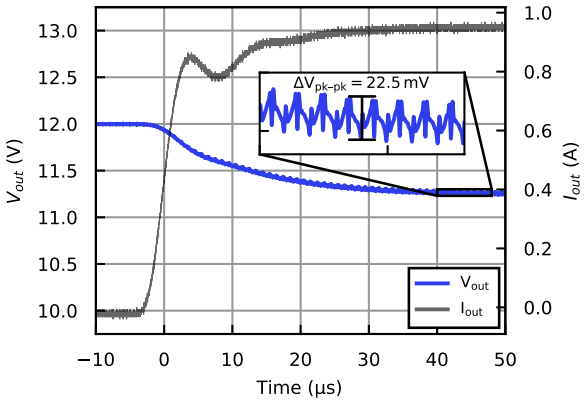


Fig. 12. Measurement of the output voltage when an output load step of 1 A is applied. $V_{out}$ is 20 MHz bandwidth limited.

and the simulated efficiency is mainly due to the quiescent current of the gate-drivers and other circuitry, which is not taken into account for the power loss calculation. Furthermore, it can be seen that when modelling the bonding wire series resistance and simulating with post-layout extracted parasitics the output resistance is increased, which changes the overall efficiency and the drop-off slope of the efficiency curve for higher output currents, where the power loss due to the effective output resistance becomes dominant.

The 48 V-12 V switched-capacitor power converter was designed and fabricated in a 180 nm SOI BCD process. A microscope photo of the IC can be seen in Fig. 8 with annotations for the power switches and the gate-drivers.

## IV. Experimental Results

To verify the implemented switched-capacitor power converter a PCB for testing the efficiency for different output loads and switching frequencies has been designed. The test PCB consists of the designed chip and external capacitors. Thermal vias under and around the IC package have been added to help mitigate thermal heating during high output load currents. The

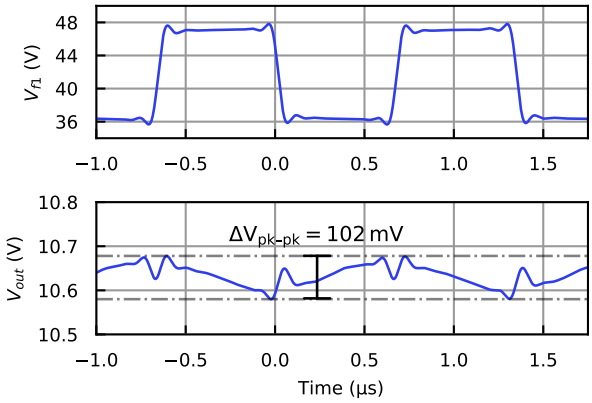


Fig. 13. Measurement of the $f_1$ switching node and the output voltage at maximum load conditions with $f_{sw} = 750$ kHz. Measurements are 20 MHz bandwidth limited.

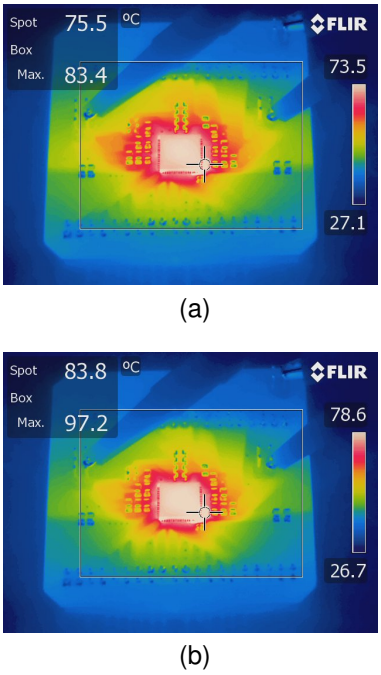


Fig. 14. Thermal measurement of the highly-integrated switched-capacitor power converter with an output load current of (a) 1.6 A and (b) 2.2 A.

focus of the prototype is to verify the maximum efficiency and maximum output power capabilities of the highly-integrated switched-capacitor converter. The test setup consists of a 5 V power supply for the digital domain and IOs, a 48 V, 100 W power supply for supplying the input voltage, a function generator for testing different switching frequencies and a digital current load. The digital control of the chip is controlled from a Python script through a Raspberry Pi. A close view of the PCB of the full power converter can be seen in Fig. 9. Here the QFN64 package containing the chip and the external flying capacitors can be seen. The total volume of the power converter is 1.07 $cm^3$ including the PCB thickness. In Table I a summary of the used components for the proposed power converter can be seen. The measured efficiency for different

TABLE II
PERFORMANCE COMPARISON.

| **Design** | [19] | [31] | [6] | [18] | [1] | **This work** |
|---|---|---|---|---|---|---|
| **Topology** | Series-Capacitor Buck | QSD | 4:1 Hybrid Dickson | 12-level Series-Capacitor Buck | LLC DCX | **4:1 Ladder SCC** |
| **Process** | N/R | 180 nm BCD | 130 nm SOI-BCD | 180 nm BCD + discrete GaN | Discrete | **180 nm SOI-BCD** |
| $\mathbf{V_{in}}$ **(V)** | 12 | 48 | 20-60 | 36-60 | 48 | **48** |
| $\mathbf{V_{out}}$ **(V)** | 1.2 | 1.2 | 3-3.6 | 0.5-1 | 12 | **12** |
| $\mathbf{f_{sw,eff}}$ **(MHz)** | 2 | 0.5 | 0.32 | 2.5 | 1.6 | **0.25** |
| **Max. Eff. (%)** | 87.7@4.8 W | 88.5@4.2 W | 91.4@4.62 W | 90.2@1.5 W | 97.3@160 W | **93.5@4.18 W** |
| **Dimension W × L × H (mm)** | 13.1 × 10 × 2.8* | N/R | N/R | 17 × 15 × 2.5 | 30 × 20 × 7.84 | $\mathbf{15.24 \times 24.65 \times 2.85}$ |
| **Max.** $\mathbf{P_{out}}$ **(W)** | 12 | 12 | 9.9 | 8 | 250 | **24.6** |
| **Power density** $(\mathbf{W/cm^3})$ | 32.71* | N/R | N/R | 12.07 | 53.09 | **23.0** |
| **Regulated/Isolated** | Yes/No | Yes/No | Yes/No | Yes/No | No/Yes | **No/No** |

*Estimated from paper, N/R = Not reported.

output load currents and for different switching frequencies can be seen in Fig. 10. Simulation results for a switching frequency of 1 MHz with extracted parasitics can also be seen for comparison. The figure shows a peak efficiency of 93.5 % at a load current of 360 mA and a switching frequency of 250 kHz. From Fig. 10 it can also be seen, that if a simple frequency control scheme is implemented there is potential for above 90 % efficiency from a wide current range of 80 mA to 1.4 A. Comparing the 1 MHz measurement results to the simulation results, it can be seen that for low loads there is a very good correspondence. While for higher loads, the slope of the measurements curve is steeper indicating a higher output resistance. To investigate this difference the output resistance was measured and compared to both the proposed model results and the simulated output resistance. This comparison can be seen in Fig. 11. Here it is clear, that the $R_{SSL}$ matches well for the proposed model, simulation and measurement results. The $R_{FSL}$ is about 150 mΩ higher than expected from simulation. This increase is most likely due to the additional PCB trace inductance and resistance that has not been modelled properly in simulation. In Fig. 10 it can also be seen that there seems to be increased losses when going to switching frequencies around 1 MHz and above. This can be seen since the measurement results for 750 kHz outperforms the 1 MHz results, even for higher load currents. This could be because of the frequency limit of the external capacitors used, which start becoming inductive and have increased ESR from around 2 MHz [30].

To investigate the transient load performance, the output voltage $V_{out}$ with a load step of 1 A and a switching frequency of 1 MHz can be seen in Fig. 12. This load condition is around the maximum efficiency of the power converter for the 1 MHz switching frequency. The output voltage is measured with a bandwidth limit of 20 MHz. The output current waveform is captured using a Hioki 3273-50, dc-50 MHz bandwidth current probe. From Fig. 12 it can seen that the output voltage ripple is 22.5 mV for a 1 A load. Additionally a measurement of one of the switching nodes, $f_1$ and the output voltage at maximum load condition of 2.2 A can be seen in Fig. 13. Here it can be seen that the output voltage drops to an average of around 10.65 V and the output voltage ripple is increased to 102 mV.

In Fig. 14 thermal measurements for a load current of 1.6 A and 2.2 A respectively, can be seen. These measurements are performed with a switching frequency of 750 kHz and no external cooling. The measurement at 1.6 A is made as this is where the conduction losses start being dominant, and therefore the main heat dissipation will shift from the external capacitors to inside of the IC as can be seen from Fig. 10. The 2.2 A measurement is close to the maximum load current of 2.4 A and therefore Fig. 14b gives better insight into the maximum thermal capabilities. Both thermal measurements are made after applying the load and waiting for 1 minute to reach thermal steady-state. It can be seen from Fig. 14 that the maximum temperature of 97.2 °C is close to the output voltage node of the IC, which is expected since the highest current is drawn from this node based on the switch charge multiplier vector of the ladder topology.

The maximum output power is 24.6 W leading to a power density of 23 $W/cm^3$ including the PCB thickness.

## V. DISCUSSION

The proposed general design methodology and considerations presented in this work enables the design of more efficient highly-integrated switched-capacitor power converters under load current and constraints of both the integrated die area and the flying capacitor PCB area. The integrated power switch design optimization presented can also be used for hybrid switched-capacitor converters to achieve optimal design of the integrated power stage. The methodology differs from other previously presented methodologies since it focuses on highly-integrated switched-capacitor converters. This difference includes the losses that scales with the converter input voltage, such as gate-driver losses and switching losses. In traditional sizing methodologies such as in [28] floating gate-drivers and their increased losses due to their voltage supply is not taken into account, since it focuses on fully integrated, low voltage applications. The use of external discrete flying capacitors also means, that the traditional capacitor sizing methodology is not useful since the optimal scaling needs to take the discretized capacitor sizes into account. On the other hand, bottom-plate capacitor charge/discharge losses are not taken into account in this work, since the ratio between

the discrete flying capacitor sizes compared to the parasitic capacitances at the flying nodes is usually so small, that it can be neglected.

The performance of the proposed power converter can be seen in Tab. II together with other selected designs for a performance comparison on peak efficiency, maximum output power and power density. The regulation and isolation capabilities of the power converters are included in Tab. II since these features can effect the peak efficiency, maximum output power and power density, which we want to compare. The designs were selected based on similar application, input voltage range and power levels as is recommended by [32] when doing metrics comparison for power converters. The designs from [6], [19], [31] are all highly-integrated power converters where the power stage is integrated but the passive components are external, as in the proposed power converter in this design. They all utilize one or more inductors. In [19] The input voltage is $12\,\mathrm{V}$ to a point-of-load voltage of $1\,\mathrm{V}$. It is included since it is a highly-integrated solution, that is in a similar output power level as the proposed converter. The work in [31] is a quadruple step-down converter utilizing a 4-phase switching scheme to achieve series capacitor charge-balancing. The topology in [31] is an extension on the double step-down converter (DSD) and achieves great performance since it can utilize higher conductive switches, since the maximum $V_{ds}$ is only $12\,\mathrm{V}$, where LDMOS transistor have a better $P_{fom}(\mathrm{m\Omega \cdot nC})$ compared to GaN technologies [18]. The work in [6] is a 4:1 hybrid Dickson switched-capacitor converter using a single series-inductor at the output. This way the power converter utilizes the good step-down capabilities of switched-capacitor converters [17], while utilizing the inductor to achieve high efficiency outside of the ideal voltage conversion rate of the 4:1 Dickson topology. The design in [6] does not report a power density for the full design. The design in [18] aims to use a high step-down Dickson 12:1 converter with a 2 phase series-buck converter to lower the maximum $V_{ds}$ of the power switches to $5\,\mathrm{V}$, which means that it can use high-conductive $5\,\mathrm{V}$ devices. It uses a discrete GaN device for the top switch, to ensure safe start-up and tolerate the full input voltage. While the design is very compact and highly-integrated it suffers from a high conduction loss due to the large amount of switches, which limits the maximum power. The design in [1] is not monolithic. It is included since it is targeting the same application and shows how by careful optimization of the passive components, in this case a planar matrix transformer in a LLC converter, it can achieve high power density and peak efficiency. The design in [1] uses GaN devices for the power switches. The work does achieve the highest efficiency and maximum power.

The proposed design achieves the highest peak efficiency and maximum power of the highly-integrated designs. The power density in [19] is higher showing the benefits of careful selection of used passive components and PCB layout. The design in [19] also utilizes flip-chip packaging for the IC making the footprint even smaller. The QFN64 package used in this work is $9\,\mathrm{mm} \times 9\,\mathrm{mm}$, which is about 8 times larger than the designed IC leading to wasted PCB footprint area. Utilizing flip-chip packaging together with an interposer technology would further increase both thermal performance and volume increasing the power density for highly-integrated power converters [33]. It is important to note that the designs in [6], [18], [31] are point-of-load converters and that for the proposed design and the design in [1] there needs to be cascade converter to reach the desired point-of-load voltage. This will further decrease both the total efficiency and power density. The proposed design in this work and its design considerations could be incorporated in designs similar to [6], [18], [31] to further increase both maximum power and power density.

## VI. Conclusion

In this study the design methodology for designing high-voltage, highly-integrated switched-capacitor power converters is presented and demonstrated with an implemented $48\,\mathrm{V}$-$12\,\mathrm{V}$ switched-capacitor power converter with an integrated power stage, floating gate-drivers and clock controller in a $180\,\mathrm{nm}$ SOI process. This work presents an extended insight in the main power losses to consider in high-voltage applications, taking into account the trade-offs between lower conduction losses, but larger switching and gate-driver losses when the total integrated switch area is increased. The $48\,\mathrm{V}$-$12\,\mathrm{V}$ ladder topology switched-capacitor power converter has been implemented using the proposed design methodology to size the integrated power stage and external capacitors. The implemented gate-drivers and clock controller has also been shown and discussed. The performance of the highly-integrated switched-capacitor power converter has been verified with experimental results. The designed power converter achieves a peak efficiency of $93.5\,\%$ at $4.18\,\mathrm{W}$ and a maximum output power of $24.6\,\mathrm{W}$ leading to a power density of $23\,\mathrm{W/cm^3}$. Finally a discussion of the proposed power converter is presented, comparing the proposed power converter to recently published works in the same application, input voltage range and power level. Here the proposed design showed similar performance to highly-integrated inductor based topologies, while being apple to handle a larger maximum output power. To the best of the authors' knowledge, the proposed converter using a fully integrated power stage and gate-drivers and hard-charging of the capacitors is the only published power converter to achieve competitive efficiency, maximum output power and power density with an $48\,\mathrm{V}$ input voltage. This performance can help advancements in both traditional and hybrid switched-capacitor power converters.

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# D The ΔV-Method: An Intuitive Method for Analyzing Soft-Charging Capabilities of Hybrid Switched-Capacitor DC-DC Converters

*IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL23)*

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Status: Accepted



# The ΔV-Method: An Intuitive Method for Analyzing Soft-Charging Capabilities of Hybrid Switched-Capacitor DC-DC Converters

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*Published in:*
Proceedings of IEEE 24<sup>th</sup> Workshop on Control and Modeling for Power Electronics

*Publication date:*
2023

*Document Version*
Peer reviewed version

# The $\Delta$V-Method: An Intuitive Method for Analyzing Soft-Charging Capabilities of Hybrid Switched-Capacitor DC-DC Converters

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***Abstract*—This paper presents an inspection method for analyzing the soft-charging capabilities of switched-capacitor converters (SCC). The method utilizes a multi-step visual approach to derive the voltage changes ($\Delta$V) across each flying capacitor, leading to an intuitive way of understanding the behavior of hybrid-SCC topologies on circuit level. The method is presented by examples and is used to obtain capacitance ratios and split-phase timings for Hybrid Dickson topologies.**

***Index Terms*—hybrid switched-capacitor converter, soft-charging, energy efficient**

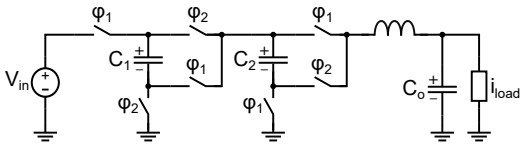
## I. Introduction

The increased requirements for large conversion ratio, high efficient power converters in applications such as data centers, automotive and USB-C power delivery DC-DC systems is leading to the popularity of hybrid switched-capacitor power converters [1]–[7]. They utilize the high voltage step-down ability from switched-capacitor converters (SCC) together with one or more inductors to achieve voltage regulation and sometimes soft-charging of the flying capacitors. The soft-charging capabilities of SCC topologies with a current source in series with the output have been analyzed in [8]. This current source is usually an inductor forming a hybrid DC-DC converter. Nevertheless, hybrid converters are most efficient if all capacitors experience soft-charging. Soft-charging takes place when all capacitors are being charged/discharged without the occurrence of current spikes. This removes part of the equivalent output resistance called the slow switching limit impedance [9]. Most often soft-charging is achieved by constraining the capacitor currents with an inductor. In [8] the soft-charging capability of a topology is determined by deriving the reduced loop matrix in all phases and combining it with the constraint that the voltage changes of each single capacitor have to sum up to zero across all switching phases. Solving these systems of linear equations for the two constraints then results in the required normalized capacitor values to achieve soft-charging for a given topology. However, the presented method in [8] requires linear algebra which lacks the intuition that visual approaches like charge flow analysis provide. Therefore it is difficult to learn and does not give the designer an intuitive understanding on the limiting factors for a given SCC topology. To provide more insight, this work presents a method to determine soft-charging capabilities of SCC topologies by inspection. The method can also be used for multi-phase systems and for multiple inductors placed locally in a topology. Thereby it attributes to better understanding of the limitations and criteria for achieving soft-charging, which can lead to hybrid SCCs with an improved efficiency and power density.

## II. Determination of Soft-Charging Capability by Inspection

The proposed method uses two constraints for evaluating the soft-charging capability of a topology. (1) the capacitor voltage change in all phases due to charge being delivered to the load must sum to zero for each individual flying capacitor ($\Delta V_{c,i}^1 + \Delta V_{c,i}^2 + \ldots + \Delta V_{c,i}^j = 0$). (2) Kirchhoff's voltage law (KVL) must hold for the voltage changes in each loop of the topology in all phases. Utilizing both constraints ensures that there is no voltage mismatch between the capacitors during phase transitions and therefore no charge redistribution losses for the capacitors. The method uses these constraints in a multi-step approach to find the normalized voltage changes across each capacitor for all phases. This is similar in structure to how the charge flow analysis by [9] is performed. Together with the charge flow analysis the capacitance scalings required for soft-charging can then be determined. Since the method analyzes the voltage changes and $\Delta V$ is used to symbolize these changes the method is referred to as voltage change method ($\Delta$V-method).

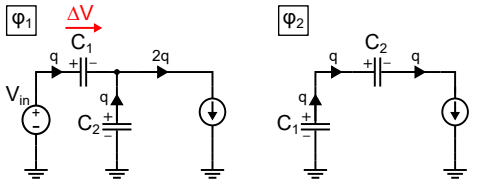
To expand on the method consider the 3:1 Fibonacci SCC in Fig. 1a. Here the charge flow analysis for the SCC was already performed and the result can be seen in Fig. 1b. Large capacitors like the input and output capacitor are approximated as voltage sources and large inductors are approximated as current sources. Similar to the charge flow analysis a good starting point should be chosen for the $\Delta$V-method. In this example, since $C_1$ is connected to a source it is chosen as a starting point. Using that the input voltage source does not have any voltage change when delivering charge we can find



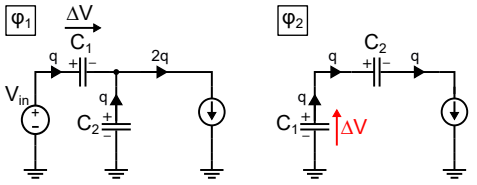

(a) 3:1 Fibonacci SCC with an inductor in series with the output.

$$\begin{bmatrix} q^1_{c,1} \\ q^1_{c,2} \end{bmatrix} = \begin{bmatrix} +1 \\ -1 \end{bmatrix}, \quad \begin{bmatrix} q^2_{c,1} \\ q^2_{c,2} \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \end{bmatrix}$$

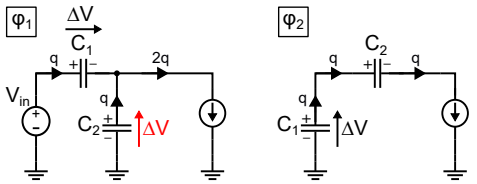
(b) 3:1 Fibonacci SCC capacitor charge flows for each phase.



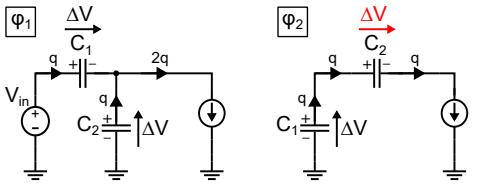

(c) ΔV-method: step 1 phase networks.




(d) ΔV-method: step 2 phase networks.




(e) ΔV-method: step 3 phase networks.




(f) ΔV-method: step 4 phase networks.

Fig. 1: Step-by-step example of using the ΔV-method to determine soft-charging capabilities for a 3:1 Fibonacci SCC with an inductor at the output.

all the capacitor voltage changes by iteration in Fig. 1 as follows:

- Phase 1: Charge flowing into the positive terminal of $C_1$ yields: $\Delta V^1_{c,1} = +1\Delta\text{V}$ indicated across $C_1$ in Fig. 1c.
- Phase 2: Because of constraint (1): $\Delta V^2_{c,1} = -1\Delta\text{V}$, i.e., the polarity of the voltage across $C_1$ changes (but not its absolute value).
- Phase 1: KVL yields: $\Delta V^1_{c,2} = \Delta V^1_{in} - \Delta V^1_{c,1} = -1\Delta\text{V}$.
- Phase 2: Because of constraint (1) the polarity of $\Delta V_{c,2}$ changes with respect to phase 1 leading to: $\Delta V^2_{c,2} = +1\Delta\text{V}$.

All capacitor voltage changes have now been found and can be summarized as:

$$\begin{bmatrix} \Delta V^1_{c,1} \\ \Delta V^1_{c,2} \end{bmatrix} = \begin{bmatrix} +1 \\ -1 \end{bmatrix}, \quad \begin{bmatrix} \Delta V^2_{c,1} \\ \Delta V^2_{c,2} \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \end{bmatrix} \tag{1}$$

Using that $C_i = q_{c,i}/\Delta V_{c,i}$ we also directly find the capacitances using the charge flows from Fig. 1b:

$$\begin{bmatrix} C_1 \\ C_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{2}$$

The 3:1 Fibonacci topology is therefore capable of achieving soft-charging with an inductor in series with the output if both flying capacitors are the same size. This fits with the results of the previously presented method in [8]. Note that the actual value of $\Delta V$ is not required to determine the normalized capacitances and, in turn, to assess if the topology is soft-charging capable.

More complex topologies than the 3:1 Fibonacci converter can be assessed using the same inspection method. In Fig. 2a the 4:1 Dickson topology with an inductor in series with the output can be seen. The solution after using the ΔV-method is shown in Fig. 2b with the voltage changes for each phase summarized in Fig. 2c together with the result of the charge flow analysis.

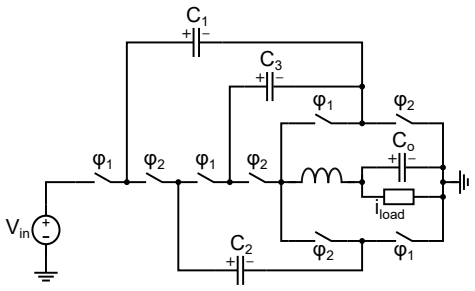
The method is performed in multi-steps as follows:

- Phase 1: Charge flowing into positive terminal of $C_1$ yields: $\Delta V^1_{c,1} = +1\Delta\text{V}$.
- Phase 2: $\Delta V^1_{c,i} + \Delta V^2_{c,i} = 0$ yields: $\Delta V^2_{c,1} = -1\Delta\text{V}$.
- KVL:
  - Phase 1: $\Delta V^1_{c,1} = \Delta V^1_{c,3} - \Delta V^1_{c,2}$.
  - Phase 2: $\Delta V^2_{c,1} = \Delta V^2_{c,3} + \Delta V^2_{c,2}$.
  - Using this with $\Delta V^1_{Cj} + \Delta V^2_{Cj} = 0$ yields: $\Delta V_{c,2} = 0$.
- Phase 2: Utilizing that $\Delta V^2_{c,2} = +0$ yields for $\Delta V^2_{c,3}$: $\Delta V^2_{c,3} = \Delta V^2_{c,1} = -1\Delta\text{V}$.
- Phase 1: $\Delta V^1_{Cj} + \Delta V^2_{Cj} = 0$ yields $\Delta V^1_{c,3}$: $\Delta V^1_{c,3} = +1\Delta\text{V}$.

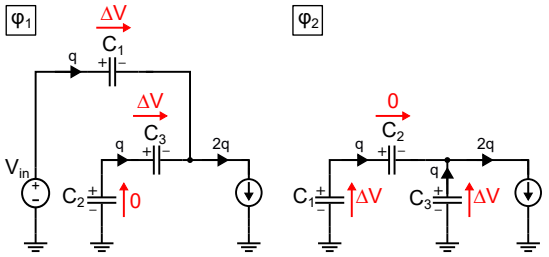
The capacitances can again be found based on the ΔV-method and the results of the charge flow analysis:

$$\begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix} = \begin{bmatrix} 1 \\ \infty \\ 1 \end{bmatrix} \tag{3}$$

For the 4:1 Dickson topology an infinitely large capacitor would be required for $C_2$. Therefore, the topology can not realize soft-charging. Signed zero is used for $\Delta V_{c,2}$ to clarify,




(a) 4:1 Dickson SCC with an inductor in series with the output.

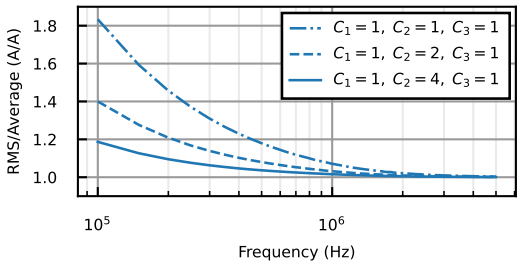



(b) 4:1 Dickson SCC phase networks with notated voltage changes.

$$\begin{bmatrix} q^1_{c,1} \\ q^1_{c,2} \\ q^1_{c,3} \end{bmatrix} = \begin{bmatrix} +1 \\ -1 \\ +1 \end{bmatrix}, \quad \begin{bmatrix} q^2_{c,1} \\ q^2_{c,2} \\ q^2_{c,3} \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \\ -1 \end{bmatrix}$$

$$\begin{bmatrix} \Delta V^1_{c,1} \\ \Delta V^1_{c,2} \\ \Delta V^1_{c,3} \end{bmatrix} = \begin{bmatrix} +1 \\ -0 \\ +1 \end{bmatrix}, \quad \begin{bmatrix} \Delta V^2_{c,1} \\ \Delta V^2_{c,2} \\ \Delta V^2_{c,3} \end{bmatrix} = \begin{bmatrix} -1 \\ +0 \\ -1 \end{bmatrix}$$

(c) 4:1 Dickson SCC capacitor charge flows and voltage changes for each phase.




(d) Simulated 4:1 Dickson SCC current ratio between RMS current and average of the absolute current of $C_1$ for three different designs with same total capacitance.

Fig. 2: Using the $\Delta$V-method to determine soft-charging capabilities for a 4:1 Dickson SCC with an inductor at the output.

that the required $C_2$ capacitance to ensure soft-charging is positive. This is not always the case for other topologies such as the Ladder and Cockcroft-Walton topologies, where a negative voltage change is required for some capacitors, when the capacitors are charged resulting in a negative capacitance requirement to achieve soft-charging. In Fig. 2d the simulated ratio between the RMS current and the average of the absolute current of $C_1$ is shown swept over frequency for three different choices of $C_2$ with the total capacitance kept the same and assuming no inductor current ripple for simplicity. Figure 2d shows that as we increase $C_2$, the capacitors approaches soft-charging. While the capacitors still experience a voltage mismatch, it is lower than for the hard-charging case, which leads to a lower output resistance at the slow-switching limit. Therefore, in practice the total losses due to the charge redistribution are decreased compared to the hard-charging case for the same total capacitance sizes and switching frequency.

The above examples demonstrate that the $\Delta$V-method is a powerful analysis tool that obtains results after a few simple steps. In the case of the 4:1 Dickson topology it was possible to find a KVL constraint for solving the voltage mismatch. This is also the case for Dickson topologies with higher conversion ratios and for any topology encountered by the authors such as the Series-Parallel, Ladder, Doubler and Cockcroft-Walton topologies. The solution obtained by the $\Delta$V-method can always be verified afterwards by checking both KVL and that the voltage change for each capacitor sums to zero for a full switching period. The inspection method only requiring simple KVL equations to analyze the soft-charging capabilities makes it easy to solve the soft-charging requirements even for complicated hybrid converter topologies.

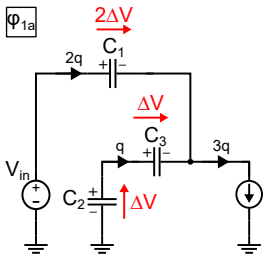
## III. Applying the $\Delta$V-Method

To verify the applicability of the $\Delta$V-method in the analysis of hybrid converters, the inspection method is used to analyze the split-phase control method presented in [10] and the soft-charging capabilities of the Hybrid Dickson topologies for higher conversion ratios.

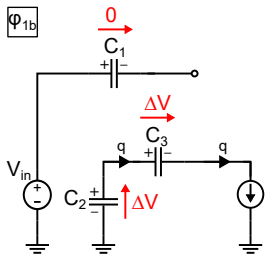
### *A. Analyzing Split-Phase Control of 4:1 Dickson Using The $\Delta$V-Method*

In [10] it is shown that the 4:1 Dickson topology can be made soft-charging by splitting both phases $\varphi_1$ and $\varphi_2$ in two phases each, as shown in Fig. 3. The goal is to find the duty cycles of each phase that permit soft-charging. Applying charge flow vector analysis we find that the system of equations for the 4 phase networks in Fig. 3 is underdetermined. This is because the lengths of the split-phases constitute two degrees of freedom. Each combination of capacitor sizes leads to different timings that achieve soft-charging. For this example we choose $C_1 = C_2 = C_3 = C$ and find the suitable split-phase duty cycles as follows. Denoting $q^{1a}_{c,1} = 2q$ the charge flow analysis yields equation (4).

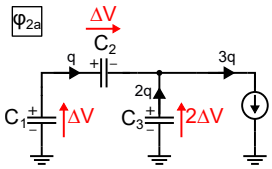
$$\begin{aligned} 2q + q^{2a}_{c,1} + q^{2b}_{c,1} &= 0 \\ 2q + q^{1a}_{c,2} + q^{1b}_{c,2} &= 0 \end{aligned} \tag{4}$$



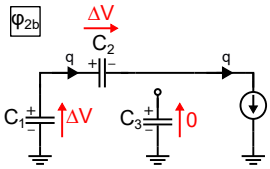

(a) Phase $\varphi_{1a}$ of 4:1 Dickson using split-phase control.




(b) Phase $\varphi_{1b}$ of 4:1 Dickson using split-phase control.




(c) Phase $\varphi_{2a}$ of 4:1 Dickson using split-phase control.




(d) Phase $\varphi_{2b}$ of 4:1 Dickson using split-phase control.

Fig. 3: Phase networks showing charge flow and voltage changes for soft-charging operation using split-phase and assuming equal capacitor sizing.

The two missing constraints in (4) are found with the $\Delta$V-method by using KVL on phases $\varphi_{1a}$ and $\varphi_{2a}$, as shown in equation (5). Phase $\varphi_{1b}$ and $\varphi_{2b}$ do not offer more KVL constraints.

$$\begin{aligned} 2\Delta V &= \Delta V_{c,3}^{1a} + \Delta V_{c,2}^{1a} \\ \Delta V_{c,3}^{2a} &= \Delta V_{c,1}^{2a} + \Delta V_{c,2}^{2a} \end{aligned} \tag{5}$$

Using that $\Delta V = q/C$, (5) can also be formulated in terms of the charge vectors (6).

$$\begin{aligned} q_{c,1}^{1a}/C_1 &= q_{c,3}^{1a}/C_3 + q_{c,2}^{1a}/C_2 \\ q_{c,3}^{2a}/C_3 &= q_{c,1}^{2a}/C_1 + q_{c,2}^{2a}/C_2 \end{aligned} \tag{6}$$

Using that $q_{c,1}^{1a} = 2q$ and $C_1 = C_2 = C_3$ together with (4) and (6) we find that $q_{c,1}^{2a} = q_{c,1}^{2b} = q_{c,2}^{1a} = q_{c,2}^{1b} = -q$. The switching phase networks with their voltage changes and charge flows are depicted in Fig. 3. The voltage change for all capacitors in all phases is:

$$\begin{aligned} \begin{bmatrix} \Delta V_{c,1}^{1a} \\ \Delta V_{c,2}^{1a} \\ \Delta V_{c,3}^{1a} \end{bmatrix} &= \begin{bmatrix} +2 \\ -1 \\ +1 \end{bmatrix}, \quad \begin{bmatrix} \Delta V_{c,1}^{1b} \\ \Delta V_{c,2}^{1b} \\ \Delta V_{c,3}^{1b} \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \end{bmatrix}, \\ \begin{bmatrix} \Delta V_{c,1}^{2a} \\ \Delta V_{c,2}^{2a} \\ \Delta V_{c,3}^{2a} \end{bmatrix} &= \begin{bmatrix} -1 \\ +1 \\ -2 \end{bmatrix}, \quad \begin{bmatrix} \Delta V_{c,1}^{2b} \\ \Delta V_{c,2}^{2b} \\ \Delta V_{c,3}^{2b} \end{bmatrix} = \begin{bmatrix} -1 \\ +1 \\ 0 \end{bmatrix} \end{aligned} \tag{7}$$

Additionally, the charge flow for the input voltage, the flying capacitors and the output in matrix form is:

$$\begin{aligned} \begin{bmatrix} q_{in}^{1a} \\ q_{c,1}^{1a} \\ q_{c,2}^{1a} \\ q_{c,3}^{1a} \\ q_{out}^{1a} \end{bmatrix} &= \begin{bmatrix} +2 \\ +2 \\ -1 \\ +1 \\ +3 \end{bmatrix}, \quad \begin{bmatrix} q_{in}^{1b} \\ q_{c,1}^{1b} \\ q_{c,2}^{1b} \\ q_{c,3}^{1b} \\ q_{out}^{1b} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -1 \\ +1 \\ +1 \end{bmatrix}, \\ \begin{bmatrix} q_{in}^{2a} \\ q_{c,1}^{2a} \\ q_{c,2}^{2a} \\ q_{c,3}^{2a} \\ q_{out}^{2a} \end{bmatrix} &= \begin{bmatrix} 0 \\ -1 \\ +1 \\ -2 \\ +3 \end{bmatrix}, \quad \begin{bmatrix} q_{in}^{2b} \\ q_{c,1}^{2b} \\ q_{c,2}^{2b} \\ q_{c,3}^{2b} \\ q_{out}^{2b} \end{bmatrix} = \begin{bmatrix} 0 \\ -1 \\ +1 \\ 0 \\ +1 \end{bmatrix} \end{aligned} \tag{8}$$

From (7) and (8) it can be seen that it is possible to achieve soft-charging by using split-phase control and having all capacitors the same size. Finally the required duty cycle of any switching phase to ensure soft-charging can be calculated by considering the output charge ($q_{out}$) compared to the output charge summed across all phases:

$$\begin{aligned} D_{1a} &= t_{1a}/T_{sw} = q_{out}^{1a}/q_{out,tot} = 3/8 \\ D_{1b} &= t_{1b}/T_{sw} = q_{out}^{1b}/q_{out,tot} = 1/8 \\ D_{2a} &= t_{2a}/T_{sw} = q_{out}^{2a}/q_{out,tot} = 3/8 \\ D_{2b} &= t_{2b}/T_{sw} = q_{out}^{2b}/q_{out,tot} = 1/8 \end{aligned} \tag{9}$$

It should be noted that this calculation of duty cycle assumes a constant output current and no inductor current ripple. Inferring the duty cycle from the charge flow will become more complex for large current ripple operating modes [11], [12].

$$\mathbf{\Delta V^1} = \begin{bmatrix} +1 \\ -0.5 \\ +0.5 \\ -1 \end{bmatrix}, \ \mathbf{\Delta V^2} = \begin{bmatrix} -1 \\ +0.5 \\ -0.5 \\ +1 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 1 \\ 2 \\ 2 \\ 1 \end{bmatrix}$$

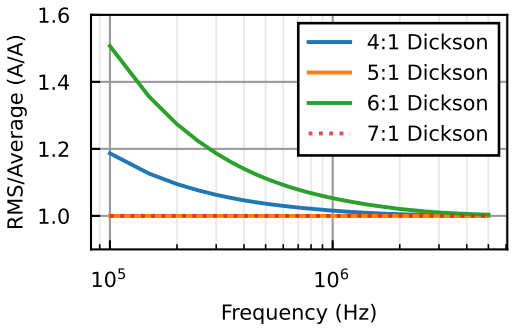
(a) Voltage changes for each phase and required capacitor values for 5:1 Dickson SCC.

$$\mathbf{\Delta V^1} = \begin{bmatrix} +1 \\ -0 \\ +1 \\ -0 \\ +1 \end{bmatrix}, \ \mathbf{\Delta V^2} = \begin{bmatrix} -1 \\ +0 \\ -1 \\ +0 \\ -1 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 1 \\ \infty \\ 1 \\ \infty \\ 1 \end{bmatrix}$$

(b) Voltage changes for each phase and required capacitor values for 6:1 Dickson SCC.

$$\mathbf{\Delta V^1} = \begin{bmatrix} +1 \\ -1/3 \\ +2/3 \\ -2/3 \\ +1/3 \\ -1 \end{bmatrix}, \ \mathbf{\Delta V^2} = \begin{bmatrix} -1 \\ +1/3 \\ -2/3 \\ +2/3 \\ -1/3 \\ +1 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 1 \\ 3 \\ 3/2 \\ 3/2 \\ 3 \\ 1 \end{bmatrix}$$

(c) Voltage changes for each phase and required capacitor values for 7:1 Dickson SCC.




(d) Simulated Dickson SCC current ratio between RMS and average of the absolute current of $C_1$ for 4 different conversion ratios.

Fig. 4: The voltage changes and capacitor scalings required for soft-charging for the 5:1, 6:1 and 7:1 Dickson topology using only two phases together with the simulated current ratio between RMS and average of the absolute currents for $C_1$ for all conversion ratios.

### *B. Soft-Charging Capabilities of Dickson Topology for Different Conversion Ratios*

While the split-phase control can ensure soft-charging of the flying capacitors for the 4:1 Dickson topology we can also use the $\Delta$V-method to analyze the soft charging capabilities of the Dickson topology at other conversion ratios. The analysis approach is the same as presented in Section II and has been done for the 5:1, 6:1 and 7:1 Dickson SCC. The resulting voltage changes and required capacitor sizes are shown in Fig. 4. The simulated current ratio between RMS and average of the absolute current in $C_1$ for the different conversion ratios can be seen in Fig. 4d. For the simulation the total capacitance has been kept constant between the ratios. The plot reveals that all odd conversion ratios can achieve soft-charging without any additional split-phase control and using only a single inductor at the output. Therefore, the designer should consider if an odd conversion ratio Hybrid Dickson could be used instead in the desired application. The 5:1 and 7:1 Dickson converters do require that the two phases have different duty cycles to achieve soft-charging. The duty cycles can again be obtained by observing the output charge in each phase compared to the summed output charge for both phases. For the 5:1 Dickson this means that the duty cycle required for soft-charging is:

$$\begin{aligned} D_1 &= t_1/T = q^1_{out}/q_{out,tot} = 3/5 \\ D_2 &= t_2/T = q^2_{out}/q_{out,tot} = 2/5 \end{aligned} \tag{10}$$

For the 7:1 Dickson the duty cycle required for soft-charging is:

$$\begin{aligned} D_1 &= t_1/T = q^1_{out}/q_{out,tot} = 4/7 \\ D_2 &= t_2/T = q^2_{out}/q_{out,tot} = 3/7 \end{aligned} \tag{11}$$

### *C. Improving Converter Design by Topology Insight from the $\Delta$V-Method*

The fact that the soft-charging capabilities of a specific topology can also be conversion ratio dependent is mentioned in [12]. In 2018 [1] presented a new 7:1 Dual-Inductor Hybrid converter (DIHC) topology, which can achieve soft-charging using two interleaved inductors and achieve output voltage regulation using PWM control. The work in [1] states that the Hybrid Dickson converter can not achieve soft-charging

without split-phase control such as in [10]. While this is true for even order Hybrid Dickson converters, the $\Delta$V-method, presented here, shows that the 7:1 DIHC in [1] could also have been implemented with a 7:1 Hybrid Dickson, thereby using only a single inductor at the output. The output voltage regulation of the 7:1 Hybrid Dickson can then be achieved with similar PWM control.

## IV. Conclusion

An inspection method for determining the soft-charging capabilities of hybrid DC-DC SCCs is introduced. It uses simple steps to visually analyze the voltage changes $\Delta$V across each capacitor. This process leads to an intuitive understanding on how to achieve soft-charging for a given SCC topology, which can then be used to improve efficiency and power density of the converter. The method is applied to determine split-phase timings for a 4:1 Hybrid Dickson converter and to show the inherent soft-charging capability of odd ratio Hybrid Dickson converters. The $\Delta$V-method is easy to use since it does not require the designer to describe the system equations. Instead the phase equivalent circuits are analyzed to help gathering faster and easier insight into specific hybrid converter topologies.

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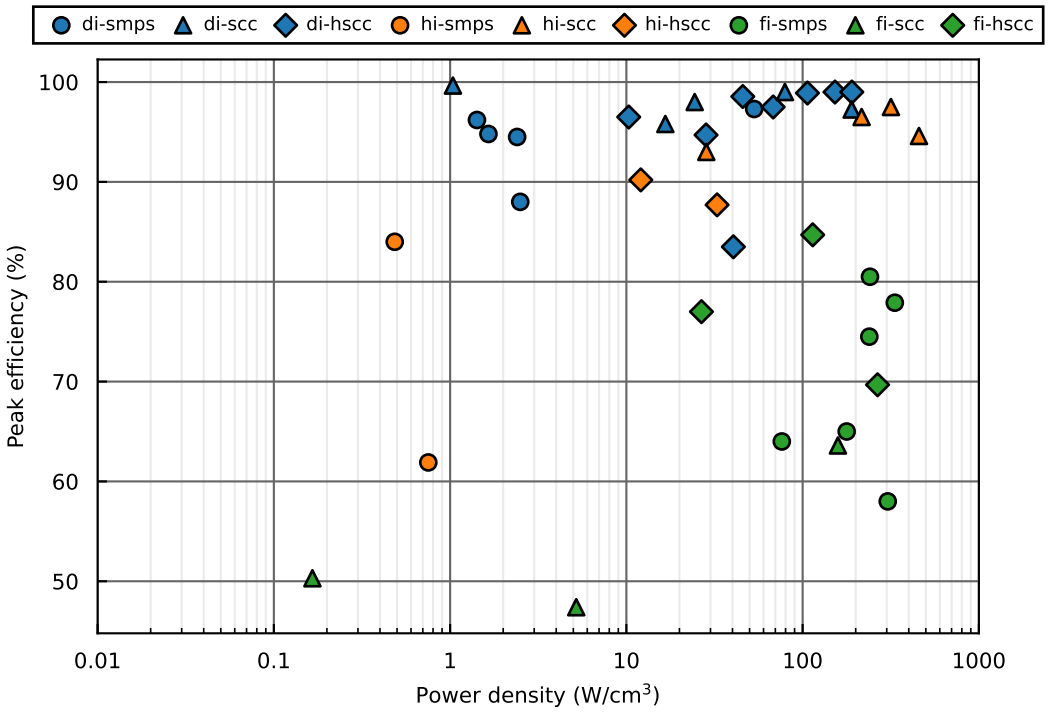
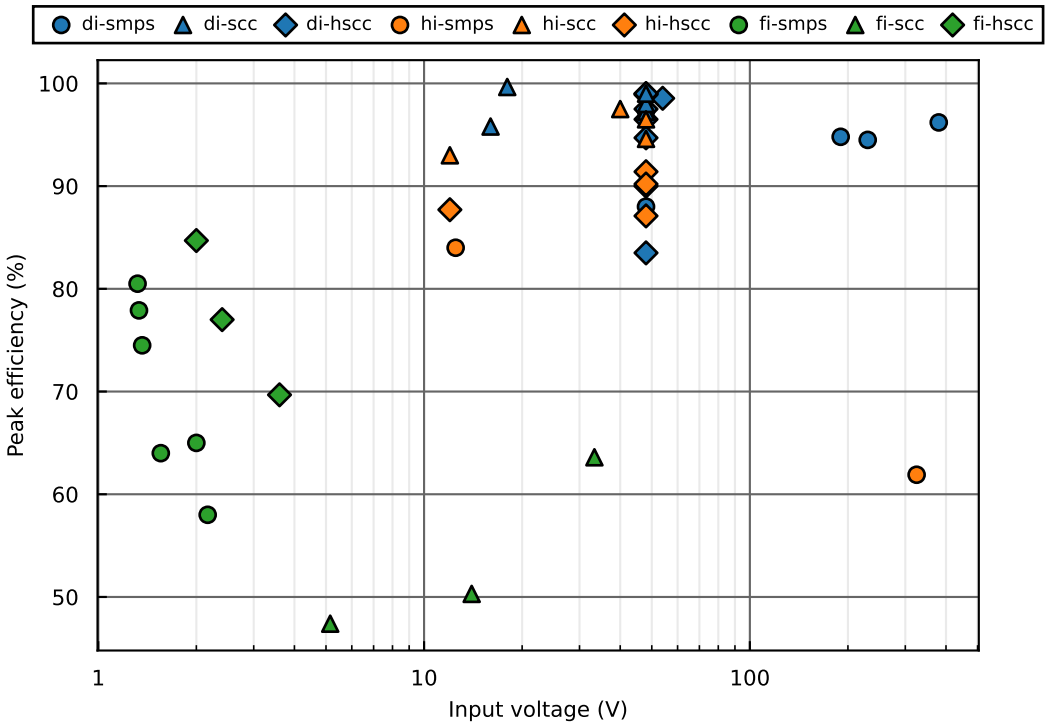
# E Additional figures for state of the art survey

Some additional figures comparing state of the art power converters are shown here. The implementations in the figures are all from the ones presented in Table 2.2.

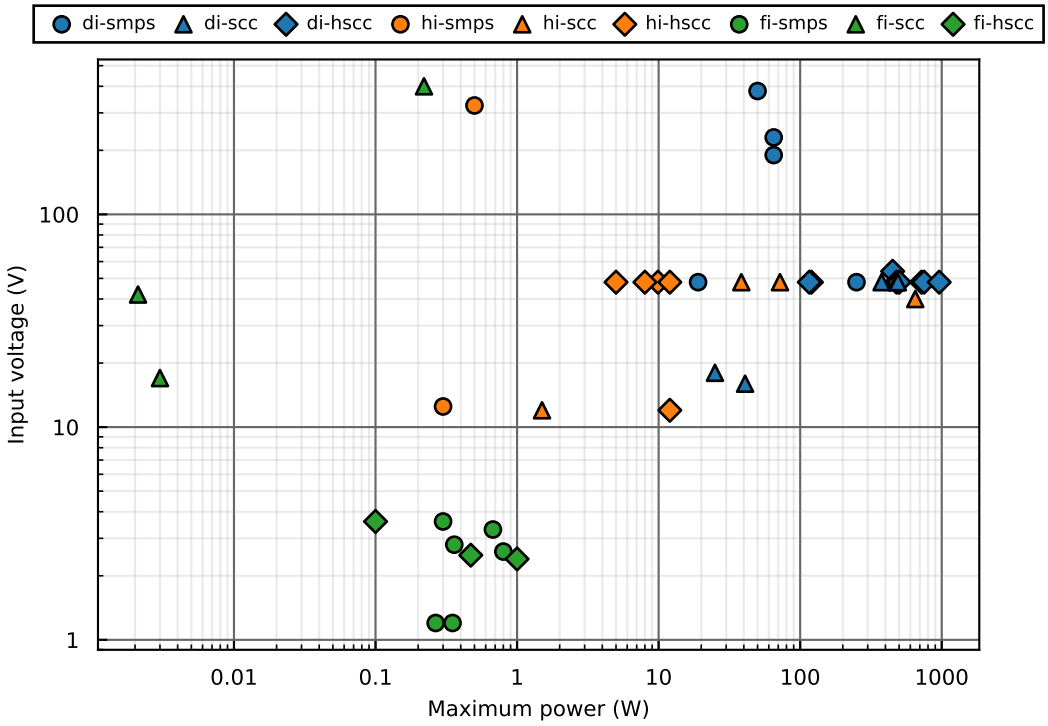



(a) Peak efficiency versus power density for state of the art power converters.

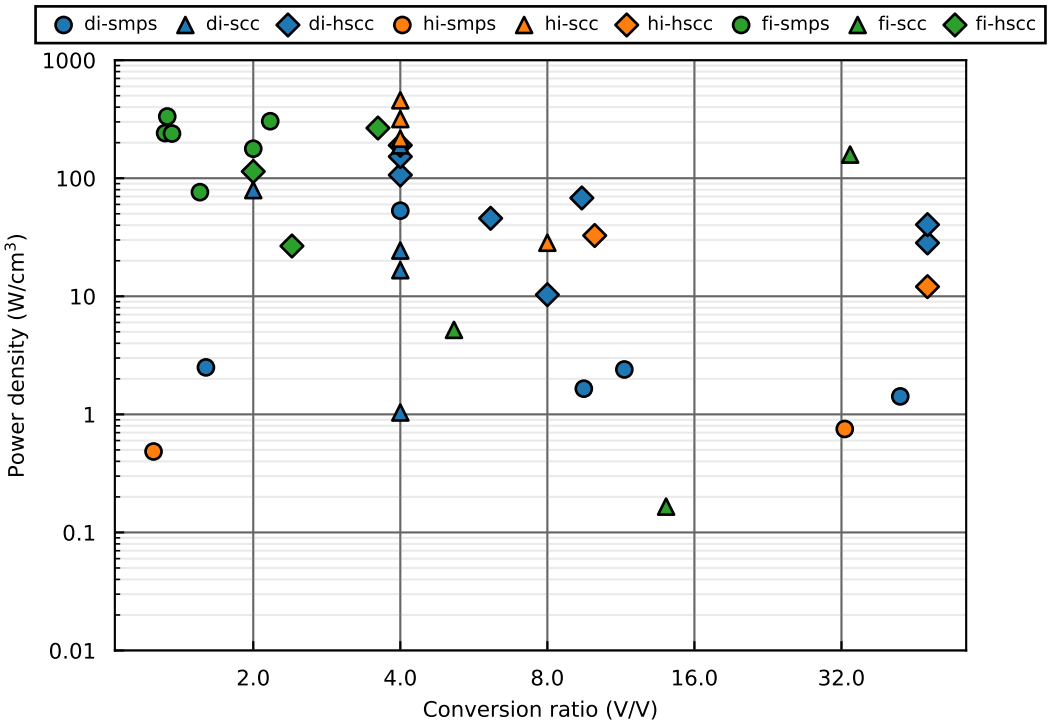



(b) Peak efficiency versus input voltage for state of the art power converters.

Figure E.1: State of the art survey for power converters up to 1 kW and maximum input voltage of 400 V.

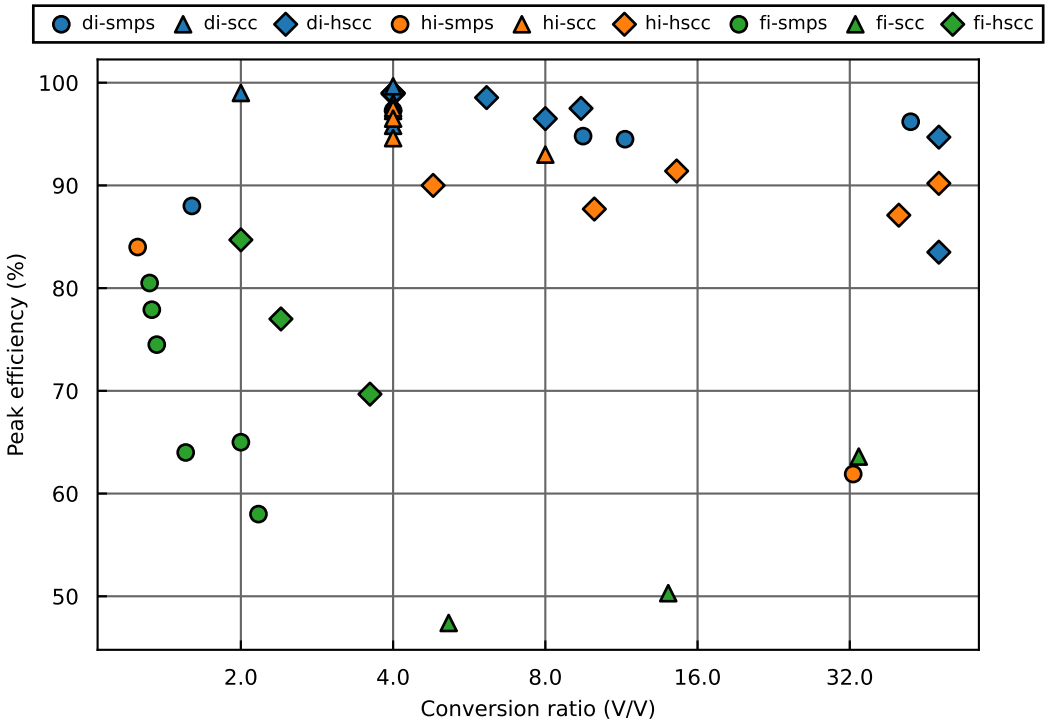



(c) Maximum output power versus input voltage for state of the art power converters.

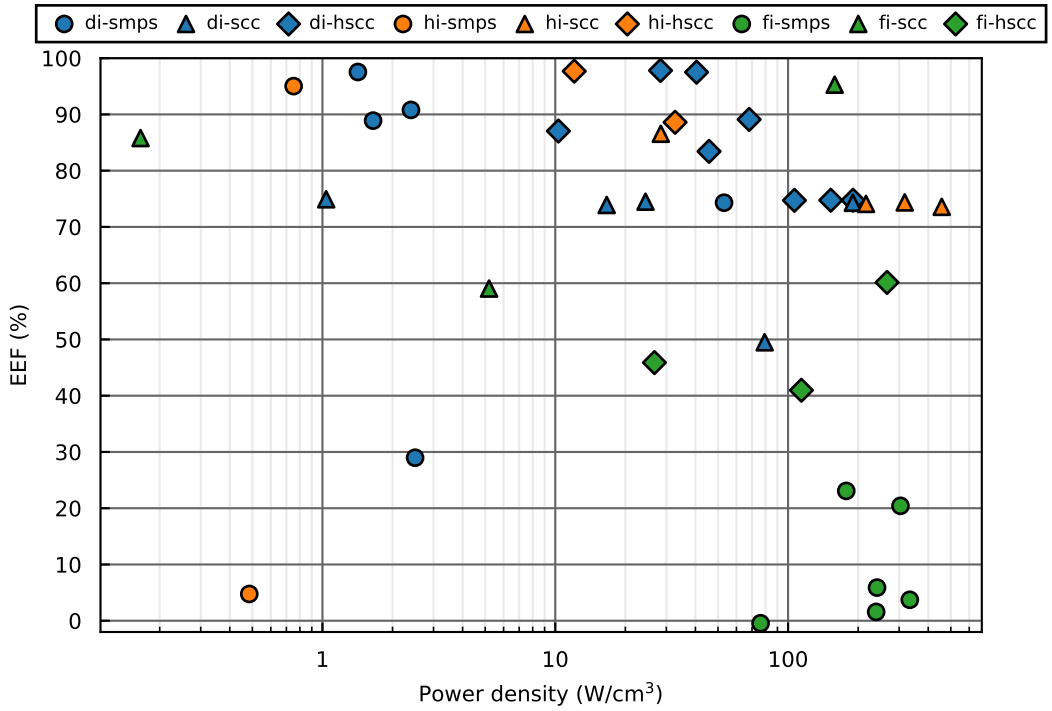



(d) Power density versus conversion ratio for state of the art power converters.

Figure E.1: State of the art survey for power converters up to 1 kW and maximum input voltage of 400 V.




(e) Peak efficiency versus conversion ratio for state of the art power converters.




(f) Efficiency Enhancement Factor (EEF) versus power density for state of the art power converters.

Figure E.1: State of the art survey for power converters up to 1 kW and maximum input voltage of 400 V.