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Influence of semiconductor barrier tunneling on the current-voltage characteristics of tunnel metal-oxide-semiconductor diodes

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Current–voltage characteristics have been examined for Al–SiO_2–pSi diodes with an interfacial oxide thickness of $\delta \approx 20$ Å. The diodes were fabricated on ⟨100⟩ and ⟨111⟩ oriented substrates with an impurity concentration in the range of $N_A = 10^{14}$–10^{16} cm^{-3}. The results show that for low forward voltages, the diode current is increased with increased N_A, but for higher forward voltages, the diode current is decreased as N_A is increased. For the diodes examined in this work, the results presented lead to the conclusion that the diode current should be treated as a superposition of multistep tunneling recombination current and injected minority carrier diffusion current. This can explain the observed values of the diode quality factor n. The results also show that the voltage drop across the oxide V_{ox} is increased with increased N_A, with the result that the lowering of the minority carrier diode current J_{min} is greater than in the usual theory. The conclusion drawn is that the increase in V_{ox} and lowering of J_{min} is due to multistep tunneling of majority carriers through the semiconductor barrier.

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I. INTRODUCTION

In the case of surface barrier devices such as tunnel metal–oxide-semiconductor (MOS) diodes, a large number of carrier transport mechanisms can contribute to the diode current J_D. The relative magnitudes of these components depend upon various parameters, such as metal to semiconductor barrier height ϕ_{ms}, density of interface states N_{SS}, substrate impurity concentration N_A, device voltage V, and device temperature T.

Up until now, the literature has contained several reports on the current mechanism of tunnel MOS diodes and solar cells.[1–12] For silicon MOS solar cells, most of the efforts have been concentrated on the Au–SiO_2–nSi structure[1–3] and the Al–SiO_2–pSi structure.[4–11] For the Au–SiO_2–Si cell, the diode saturation current is treated as a majority carrier tunnel current,[2,3] as the resulting barrier height ϕ_{ms} is relatively low. For the Al–SiO_2–pSi cell an alternate explanation for the experimental observations has been given by Singh, Shewchun, and Green.[6,7] They base their explanation of the Al–SiO_2–pSi solar cell operation on the concept that they are minority carrier tunnel diodes as the resulting barrier height is relatively high. A substantial body of experimental results for this structure has been reported,[8–12] where the conclusions drawn are confirming the minority carrier mode of operation, even if the diode quality factor n of the ln J_D-vs-V characteristics is much larger than unity or the linearity of the characteristic holds over a very limited voltage range. More recently, experimental results have been presented for MOS diodes fabricated on poly-crystalline silicon[13–18] where the effects of grain boundaries have been examined. Among these a very interesting paper is presented by Kar, Ashok, and Fonash,[18] where the results indicate the likelihood of the primary transport mechanisms being multistep tunneling instead of thermionic emission of majority carriers or injection of minority carriers.

The aim of this paper is to present some interesting electrical characteristics, measured on single crystalline silicon MOS diodes, which upon analysis indicate how important multistep tunneling transport of majority carriers may be for these devices. For the first time a discussion is given showing how a combination of multistep tunneling recombination current and injected minority carrier diffusion current will fit to the observed characteristics, taking into account the large n values.

II. THEORETICAL DISCUSSION

Figure 1 shows the electron band diagram of a p-type MOS tunnel diode at a moderate forward bias. As illustrated in Fig. 1, the main transport processes possible are ther-

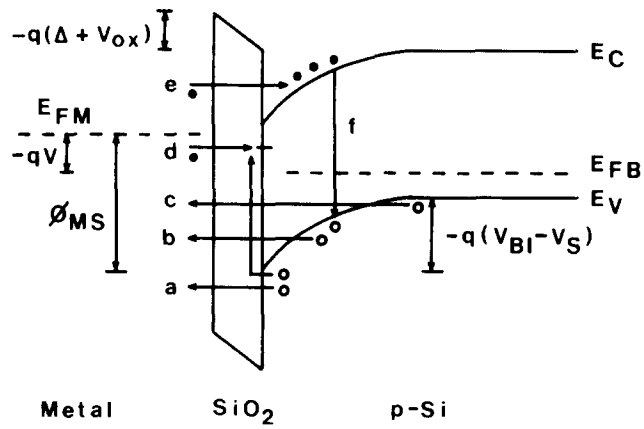

FIG. 1. Electron band diagram of an MOS p–Si diode at a moderate forward voltage V. ϕ_{MS} is the effective metal to semiconductor barrier height, V_{BI} the built-in potential, V_S the semiconductor voltage, Δ is the equilibrium oxide voltage, V_{ox} the additional oxide voltage under forward bias, E_{FB} the bulk fermi level, and E_{FM} the metal fermi level. Various possible mechanisms of carrier transport in dark have been illustrated.

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mionic emission (a), thermionic field emission (b), field emisison (c), recombination tunneling via interface states (d), minority carrier injection (e), and recombination (f).[19–25] The effect of the oxide barrier on processes a–f can be represented by means of an oxide transmission coefficient.[19]

Generally, in these types of diodes, the diode quality factor n is rather high in the low forward voltage region, which usually is explained by recombination processes.[20] With increasing temperature, the influence of the recombination currents become smaller. In the intermediate voltage regime, a number of processes compete for dominance. Among the majority carrier processes (a,b,c, and d), all occurring in parallel, the general belief has been that thermionic emission (a) and recombination tunneling (d) are the important mechanisms at high (room) temperature. The latter requires a high density of gap states suitable located in energy. For intermediate temperatures, it is generally held that thermionic field emission (b) can be important, and at low temperatures field emission (c) can be important, depending on the barrier thickness. For higher doping levels resulting in thinner barriers, the importance of mechanisms (b) and (c) would be further extended in temperature.[25,26] This assessment of processes (b) and (c) is based on the assumption of direct tunneling through the semiconductor barrier region. In parallel with these processes is the minority carrier injection (e). This process can dominate in the intermediate voltage regime if the effective barrier height is sufficiently high to suppress the majority carrier mechanisms.[27]

The mechanisms illustrated in Fig. 1 are usually associated with carrier transport across a surface barrier. From the results presented by Crowell and Rideout,[28] processes (b) and (c) should not be of importance for the doping range and temperature range investigated in this work. However, as pointed out in,[18] the process of multistep tunneling through the silicon barrier should be taken into account.

The multistep tunneling model has been suggested by Riben and Feucht[29,30] from the results of their work in n Ge–p GaAs heterojunctions. Using the results given in Ref. 30 the forward multistep tunneling current through the semiconductor barrier is given by

$$J_D = \beta N_t \exp[-\alpha\theta^{1/2}(V_{BI} - V_S)]. \quad (1)$$

In Eq. (1), β is a constant including the oxide transmission coefficient, N_t the density of traps in the forbidden region, V_{BI} the built-in potential, and V_S the applied voltage. α is a function of substrate doping N_A and is given by

$$\alpha = 4(2m^*)^{1/2}(3q\hbar)^{-1}(2qN_A/\epsilon_s)^{1/2}, \quad (2)$$

where m^* is the electron effective mass and ϵ_s the semiconductor permittivity. From the discussion in Ref. 30, the average energy barrier E_t that the electron will tunnel through is found to be proportional to the square of the electric field; i.e.,

$$E_t = \theta(V_{BI} - V), \quad (3)$$

which defines θ. In Eq. (1), V_{BI} is expected to decrease with increasing temperature in a linear way in accordance with the semiconductor bandgap variation.

From Eqs. (1) and (2) it is seen that the density of traps in the depletion region N_t and the doping level N_A both do have a great influence on the tunneling current. In Eq. (1) V_{BI} follows the logarithmic of N_A while α follows the inverse square root of N_A, so variations will mainly be due to variations in α. The result is that when N_A is increased, α will be decreased, leading to an increased tunneling current J_D, when V_S is kept constant. As the current is due to multistep tunneling of holes through the semiconductor barrier, the surface concentration of holes p_s will be increased when N_A is increased.

The theory of interface state tunneling and surface recombination of the MOS diode structure has been treated in details by Freeman and Dahlke.[23] They use the results obtained by Shockley and Read,[31] but these results do not include the possibility of majority carrier tunneling through the semiconductor barrier from the bulk of the semiconductor to the surface. From these results, the surface concentration of holes p_s is due to thermionic emission and the surface recombination tunneling current [Fig. 1(d)] is a function of the oxide thickness δ, the barrier height ϕ_{ms}, the interface state density N_{SS}, forward voltage V, and temperature T, while the substrate doping level N_A should be of no influence on this current.

From the theory of multistep tunneling it is seen that if the surface concentration of majority carriers p_s is dominated by holes reaching the semiconductor surface by multistep tunneling through the semiconductor barrier from the bulk [path (g) Fig. 2] then the surface recombination current will also be a function of the substrate doping level N_A. In this case, the magnitude of the recombination current increases with increasing N_A.

So, when measuring the recombination current of MOS tunneling diodes as a function of substrate doping, it should be possible to decide whether the recombination current arises from thermionic emission or multistep tunneling. Figure 2 also shows a single-step tunneling recombination process, that is a field emission recombination process [path (h)].

The diodes examined in this work have all been fabricated on single-crystalline Si. For this type of diode, the sur-

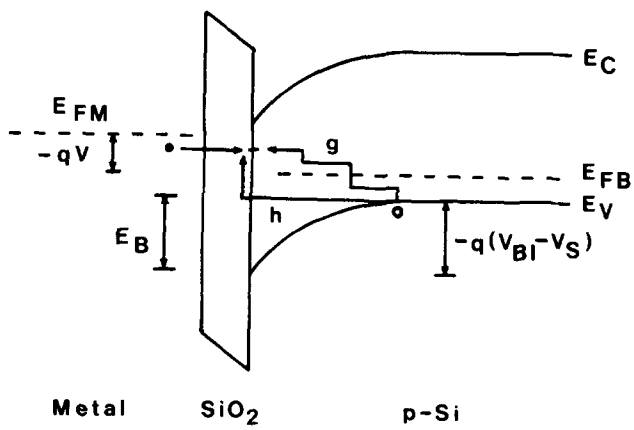


FIG. 2. Semiconductor tunneling recombination currents for an MOS p–Si diode. Process (g) shows multistep tunneling recombination while process (h) shows field emission recombination. E_B is the semiconductor energy barrier equal to $q(V_{BI} - V_S)$.

TABLE I. Orientations and doping concentrations for diodes of Figs. 3 and 4.

Diode No.	2.4	4.2	4.3	6.2	1.1	3.1	5.3
Orientation	100	100	100	100	111	111	111
N_A (cm^{-3})	2×10^{16}	1.8×10^{15}	1.8×10^{15}	4×10^{14}	1.5×10^{16}	3×10^{15}	3×10^{14}

face recombination current is expected to be dominant at low forward voltages only, while for higher forward voltages, the diode current should be dominated by either thermionic emission of majority carriers J_{maj} [path (a) Fig. 1] or diffusion of injected minority carriers J_{min} [path (e) Fig. 1]. As the interfacial oxide thickness is in the range of $\delta = 20$ Å, the tunneling resistance from the oxide layer can be neglected for the injected minority carrier current, where the current limiting factor is given by the diffusion of minority carriers in the bulk.[32]

When comparing the expressions for J_{min} and J_{maj},[33] it is seen that the relative increase with temperature is much larger for the minority carrier current than for the majority carrier current, mainly due to the difference in the activation energies E_G and ϕ_{ms}. So when measuring the diode characteristics as a function of temperature, it should be possible to decide whether the current at high forward voltages is dominated by majority carriers or minority carriers.

When measuring MOS diode characteristics at high forward voltages, the voltage drop across the oxide layer V_{ox} must be taken into account. The voltage across the diode is given by

$$V = V_S + V_{ox}, \tag{4}$$

where V_S is the voltage drop across the semiconductor and V_{ox} is the voltage drop across the oxide layer. The purpose of the work presented in this paper is to point out that when multistep tunneling takes place, the magnitude of V_{ox} will be increased when N_A is increased due to the increased storage of majority carriers at the interface states. The result for the high voltage region is that for a given diode voltage V, the diode current will be lowered due to the increase in V_{ox} when N_A is increased.

As the multistep tunneling recombination current increases with increasing N_A, the result should be that when comparing current–voltage characteristics for diodes with different doping levels, they will cross each other with a cross point voltage increasing with N_A.

For the minority carrier current, the saturation current $J_{0,min}$ is a strong function of N_A, and the decrease in J_{min} will be stronger than expected from the increase in V_{ox}.

Usually in the literature,[19,34] the diode quality factor n is brought into the diode equation. For low forward voltages, high values of n are normally observed due to the recombination currents. If multistep tunneling recombination is dominating in this region, then n would increase with N_{SS} and N_A, and n values larger than two should be possible. In the high forward voltage region, where the diode current dominates, low values of n are normally observed. In this region, the diode quality factor is brought into the diode equation to account for the oxide voltage drop. The semiconductor voltage V_S is given by Eq. (4) and in this case the diode current can be written

$$J = J_0 \exp\left(\frac{q(V - V_{ox})}{kT}\right) = J_0 \exp\left(\frac{qV}{nkT}\right). \tag{5}$$

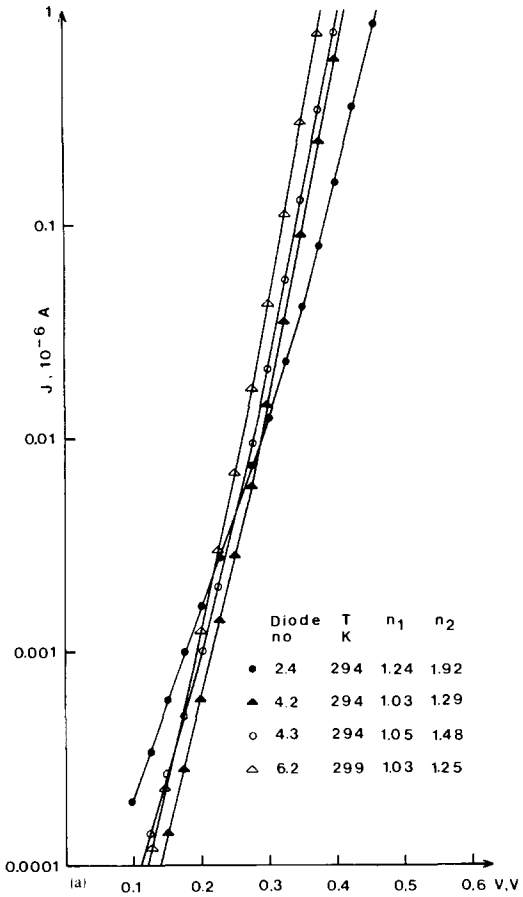
Assuming multistep tunneling, V_{ox} and n are expected to increase with increased values of N_{SS} and N_A.

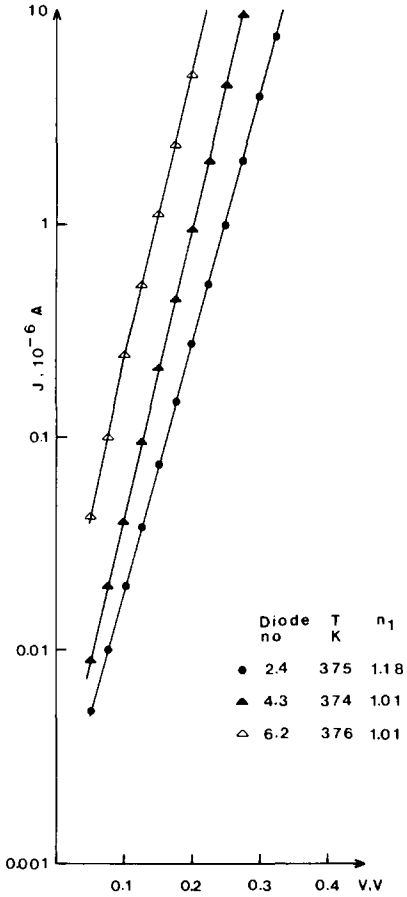
III. FABRICATION

The diodes were fabricated on ⟨100⟩ and ⟨111⟩ 300–400-μm-thick single-crystalline pSi wafers with doping concentrations N_A in the range of 10^{14}–10^{16} cm^{-3}. After a standard cleaning, a thick Al layer of 1 μm was evaporated on the back of the wafers, using electron beam evaporation. Before the growth of the thin oxide layer, the wafers were etched for 10 s in a 1:10 hydrogen–fluorid solution. Then the wafers were sintered in 10% oxygen and 90% nitrogen for 10 min at 500 °C to grow the thin oxide layer of 15–20 Å at the front of the wafers and to obtain a good Ohmic contact at the back. This was followed by the evaporation of a 5000-Å-thick Al layer on the front using filament heating. Then a layer of photoresist was placed on the front and the back of the wafers, the wafers were exposed and in the following etch, the front of the wafers was divided into diodes with a diameter of 0.8 mm resulting in a diode area of 0.504 mm^2.

TABLE II. Measured values of $\frac{q}{kT_1}V(T_1) - \frac{q}{kT_2}V(T_2)$ for $J_D = 1\,\mu$A.

Diode No.	T_1 [K]	T_2 [K]	T_3 [K]	$\frac{q}{kT_1}V_1 - \frac{q}{kT_2}V_2$	$\frac{q}{kT_1}V_1 - \frac{q}{kT_3}V_3$
1.1	295	331	375	5.58	10.37
3.1	295	334	375	5.31	10.18
5.3	295	334	373	5.49	9.80
2.4	294	335	375	6.54	10.58
4.3	299	332	374	4.53	9.43
6.2	294	332	376	6.45	10.54





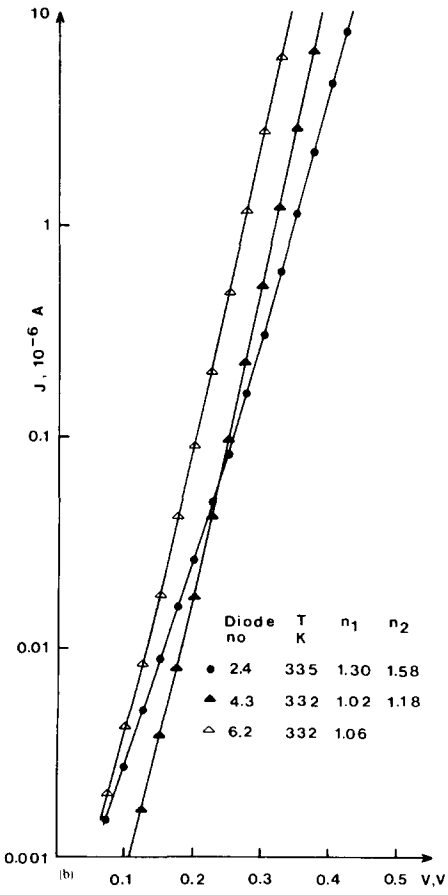


FIG. 3. Current–voltage characteristics for Al–SiO_2–pSi MOS diodes on single crystalline ⟨100⟩ oriented silicon: (a) room temperature $T \approx 295$ K; (b) intermediate temperature $T \approx 333$ K; and (c) high temperature $T \approx 375$ K. The diode area was 5.04×10^{-3} cm^2.

IV. RESULTS AND DISCUSSIONS

Current–voltage characteristics were obtained under dark conditions as a function of temperature with the wafers placed on a resistance-heated brass plate using an iron constantan thermocouple when measuring the temperature.

In Table I, the doping levels and orientations are listed for the diodes whose characteristics are shown in Figs. 3 and 4.

For the ⟨111⟩ oriented diodes of Fig. 4, the characteristics are only shown at room temperature although results similar to those shown in Figs. 3(b) and 3(c) for the ⟨100⟩ oriented diodes were obtained at higher temperatures. In order to examine whether the oxide current for higher voltages is dominated by majority or minority carriers, the diode characteristics are examined as a function of temperature. For a constant diode current J_D, the increase in the saturation current J_0 is given by

$$\ln \frac{J_{02}}{J_{01}} = \left(\frac{q}{kT_1} V_1 - \frac{q}{kT_2} V_2 \right). \tag{6}$$

In Table II the measured values of $\left(\frac{q}{kT_1} V_1 - \frac{q}{kT_2} V_2 \right)$ are listed for a diode current of $J_D = 1\ \mu$A.

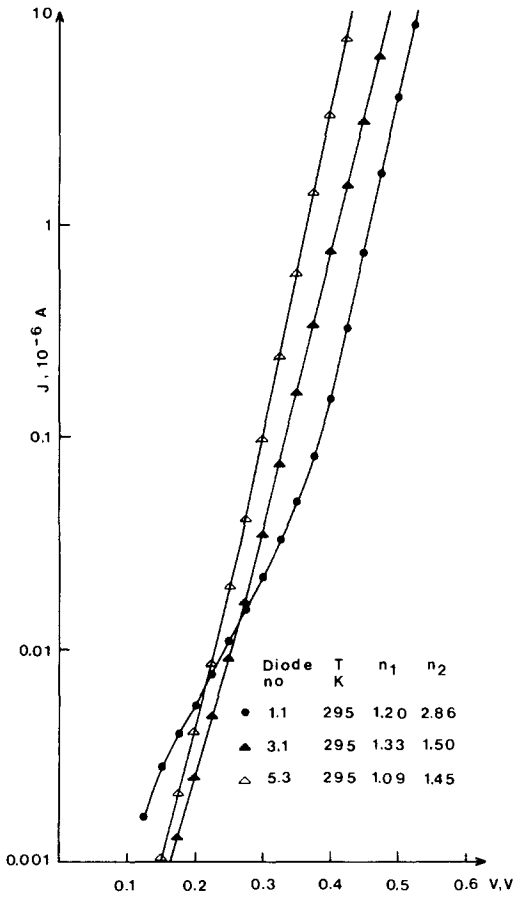


FIG. 4. Current–voltage characteristics for Al–SiO_2–pSi MOS diodes on single crystalline ⟨111⟩ oriented silicon at room temperature, $T = 295$ K. The diode area was 5.04×10^{-3} cm^2.

From the discussion in Ref. 33, it follows that the ratio of the diode saturation current for a minority carrier diffusion current is given by

$$\ln \frac{J_{02}}{J_{01}} = \ln\left[\left(\frac{T_2}{T_1}\right)^{5/2}\right] + \left(\frac{E_G(T_1)}{kT_1} - \frac{E_G(T_2)}{kT_2}\right). \quad (7)$$

Inserting the values of $T_1 = 295$ K, $T_2 = 334$ K, $T_3 = 375$ K, $E_G(T_1) = 1108$ meV, $E_G(T_2) = 1096$ meV, and $E_G(T_3)$ a 1084 meV in Eq. (7), the result is

$$\ln \frac{J_{02}}{J_{01}} = 5.89,$$

and

$$\ln \frac{J_{03}}{J_{01}} = 10.67, \quad (8)$$

which is very close to the measured results presented in Table II. For Eq. (6) to hold, the inserted values of the voltages should be corrected for the voltage drop across the oxide in accordance with Eq. (4). The values of $V_{ox}(T_1)$ and $V_{ox}(T_2)$ to be used in Eq. (6) are assumed to be close to each other so that they nearly cancel. Hence, the values listed in Table II should be good approximations and the results show that the activation energy, E_A for the diode characteristics equals the energy bandgap E_G which is the case for the minority carrier diffusion current, while for a majority carrier current the activation energy $E_A = \phi_{ms}$ which is smaller than E_G.

In order to examine the diode characteristics as a function of doping concentration N_A, characteristics taken at a given temperature have been compared for diodes with different doping. For constant temperature and constant diode current, the ratio of the saturation current is given by

$$\ln \frac{J_{02}}{J_{01}} = \frac{q}{kT}\left[V(N_{A1}) - V(N_{A2})\right] \quad (9)$$

when neglecting the voltage drop across the oxide.

The measured values of J_{02}/J_{01} obtained for $J_D = 1\ \mu$A and different doping levels and temperatures are given in Table III. For an ideal diffusion current, the diffusion length is given by

$$L_n = \sqrt{D_n \tau_n}, \quad (10)$$

where the lifetime τ_n is given by

$$\tau_n = (\sigma_n v_{th} N_t)^{-1}. \quad (11)$$

Assuming that the bulk trap density N_t equals the impurity concentration N_A, L_n is given by $(D_n/\sigma_n v_{th} N_A)^{1/2}$. Using the expression for L_n in the usual theory,[33] the result is

$$\frac{J_{02}}{J_{01}} = \left(\frac{N_{A1}}{N_{A2}}\right)^{1/2}, \quad (12)$$

which is for the ideal case.

From the results in Table III it is seen that the measured values of J_{02}/J_{01} are larger than $(N_{A1}/N_{A2})^{1/2}$. This might be explained by the difference in the oxide voltage drop V_{ox}, as V_{ox} from the previous discussions should increase with increased N_A. If all the differences between the measured values of the saturation current ratios and $(N_{A1}/N_{A2})^{1/2}$ are

TABLE III. Measured values of $q/kT(V_1 - V_2)$ for $J_D = 1\ \mu$A.

Diode No.	T[K]	$\frac{q}{kT}(V_1 - V_2)$	$\frac{J_{02}}{J_{01}}$	$\frac{N_{A1}}{N_{A2}}$	$\left(\frac{N_{A1}}{N_{A2}}\right)^{1/2}$
1.1 – 3.1	295	1.89	6.6	5	2.24
1.1 – 5.3	295	3.60	38.9	50	7.06
3.1 – 5.3	295	1.77	5.88	10	3.16
1.1 – 3.1	375	1.70	5.5	5	2.24
1.1 – 5.3	375	3.1	22.1	50	7.06
3.1 – 5.3	375	1.4	4	10	3.16
2.4 – 4.2	294	1.98	7.2	11.2	3.34
2.4 – 6.2	294	3.24	25.6	50	7.06
4.2 – 6.2	294	1.26	3.52	4.5	2.12

TABLE IV. Differences in oxide voltage drop ΔV_{ox} for diodes with different doping levels.

Diode No.	1.1–3.1	3.1–5.1	1.1–5.3	2.4–4.2	4.2–6.2	2.4–6.2
T[K]	294	295	294	293	293	293
ΔV_{ox}[mV]	27.5	15.7	45.4	19.5	12.8	32.7

explained as differences in V_{ox}, then by the use of Eqs. (9) and (12)

$$\Delta V_{ox} = \frac{kT}{q} \ln\left[\frac{J_{02}}{J_{01}} \cdot \left(\frac{N_{A2}}{N_{A1}} \right)^{1/2} \right], \tag{13}$$

where the values of J_{02}/J_{01} from Table III are to be inserted.

The values for ΔV_{ox} obtained by the use of Eq. (13) are given in Table IV for diodes of ⟨111⟩ and ⟨100⟩ orientations. It is seen that the values of ΔV_{ox} are larger for the ⟨111⟩ oriented diodes than for the ⟨100⟩ oriented diodes, which is in agreement with the previous discussion as the interface state density N_{SS} is expected to be higher for the ⟨100⟩ oriented diodes. When adding the values of ΔV_{ox} for diodes (1.1–3.1) and (3.1–5.3), the results are close to the value obtained for diodes (1.1–5.3) and similar for the ⟨100⟩ oriented diodes. So from the above results, the conclusion is drawn that when the doping level N_A is increased, the minority carrier saturation current $J_{0,min}$ is decreased in accordance with the usual theory as $(N_A)^{-1/2}$, but furthermore it is decreased as an increasing part of the diode voltage V is dropped at the oxide layer V_{ox}.

From Figs. 3 and 4 it is seen that for low forward voltages and temperatures, the diodes current is increased with increased doping levels N_A, while for higher voltages and temperatures the diode current is decreased with increased N_A. From the above discussion, the diode current at high voltages and temperatures is found to be a minority carrier diffusion current, but for low voltages and high values of N_A, the current is dominated by recombination processes. A series of diodes made on substrates with the same doping level as diode No. (1.1), (3.1), (2.4), and (4.2) have been examined at room temperature. When comparing the diode characteristics as for diodes No. (1.1), (3.1), and (2.4), (4.2) [see Figs. 3(a) and 4], they all showed a crossover point between the characteristics for the higher doped diodes and the lower doped diodes. For the ⟨100⟩ oriented cells, the cross point was found in the voltage range of 235–300 mV, while for the ⟨111⟩ oriented substrates the cross point was found in the voltage range of 100–330 mV. So it should be clear, that the diode recombination current for the MOS diode structure is increased with increased values of N_A, resulting in a very high diode quality factor n for low voltages. As n factors larger than 2 has been observed [see Fig. 4] surface recombination is assumed to be the dominating recombination process. The observed increase in the surface recombination current must be due to an increase in the surface concentration of holes p_s, if the values of surface state densities N_{SS} are equal. In accordance with the theoretical discussion, the increase in p_s with increased N_A can be explained by assuming a multistep tunneling process through the semiconductor barrier.

From most of the observed characteristics, the diode quality factor n is increased with N_A, both in the high and low voltage region. This is fully in agreement with the previous discussion, where V_{ox} is increased when p_s is increased with N_A. As the temperature is increased, the relative increase in the minority carrier current is larger than for the recombination current, with the result that the n factor decreases with temperature. For diode No. 3.1, the high n value at high forward voltages is assumed to be due to a poor Ohmic contact.

The device performance of the MOS diodes examined in this work is closely related to the thickness of the interfacial oxide layer δ, as the oxide tunneling resistance and the metal to semiconductor barrier ϕ_{ms} both are strong functions of δ. The results presented in Ref. 35 for Al–pSi MOS diodes show that for small values of δ, that is $\delta \approx 10$ Å, the observed value of ϕ_{ms} is so low that the diode current is dominated by thermionic emission of majority carriers. When δ is increased, the values of the tunneling resistance and ϕ_{ms} are increased, and the majority carrier current decreases to a point where the diode current is dominated by minority carriers.[27]

When comparing the results presented in this work with the results presented in Ref. 18 it is found that the characteristics obtained in this work are a superposition of multistep tunneling recombination currents and minority carrier diffusion currents, whereas those presented in Ref. 18 are dominated by multistep tunneling recombination currents. This is explained as a difference in surface state recombination centers, as the material used in the latter case has been Wacker polycrystalline silicon with a high surface trap density, while the material used in this work has been single crystalline silicon, with a lower surface trap density.

V. CONCLUSIONS

From the experimental results examined in this work, the conclusion is drawn that for the MOS tunnel diode structure, with an interfacial oxide layer of $\delta = 15$–20 Å, the current voltage characteristics are highly dependent on the substrate doping level N_A. The surface recombination current is found to increase with increasing N_A, leading to the conclusion that multistep tunneling of majority carriers [holes] through the semiconductor barrier is the transport mechanism which provides for the surface concentration of holes. For high doping levels, the recombination current is dominating at low forward voltages but for higher voltages and lower doping levels, the results lead to the conclusion that diffusion of minority carriers, electrons, injected from the metal into the semiconductor is the dominating diode current. The diffusion current is decreased with increased N_A, but the decrease is larger than expected from the usual semi-

conductor theory. This is explained as being due to the voltage drop across the oxide layer V_{ox}. As the surface concentration of holes is increased with N_A, V_{ox} will increase with N_A leading to a smaller voltage across the semiconductor V_S and thus a smaller diffusion current for a given diode voltage V.

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