Capacitive Micromachined Ultrasound Transducers for Super resolution Ultrasound Real-time imaging of Erythrocytes

Pedersen, Stine Løvholt Grue

Publication date:
2023

Document Version
Publisher's PDF, also known as Version of record

Citation (APA):
Pedersen, S. L. G. (2023). *Capacitive Micromachined Ultrasound Transducers for Super resolution Ultrasound Real-time imaging of Erythrocytes*. DTU Health Technology.

DTU Health Tech
Department of Health Technology

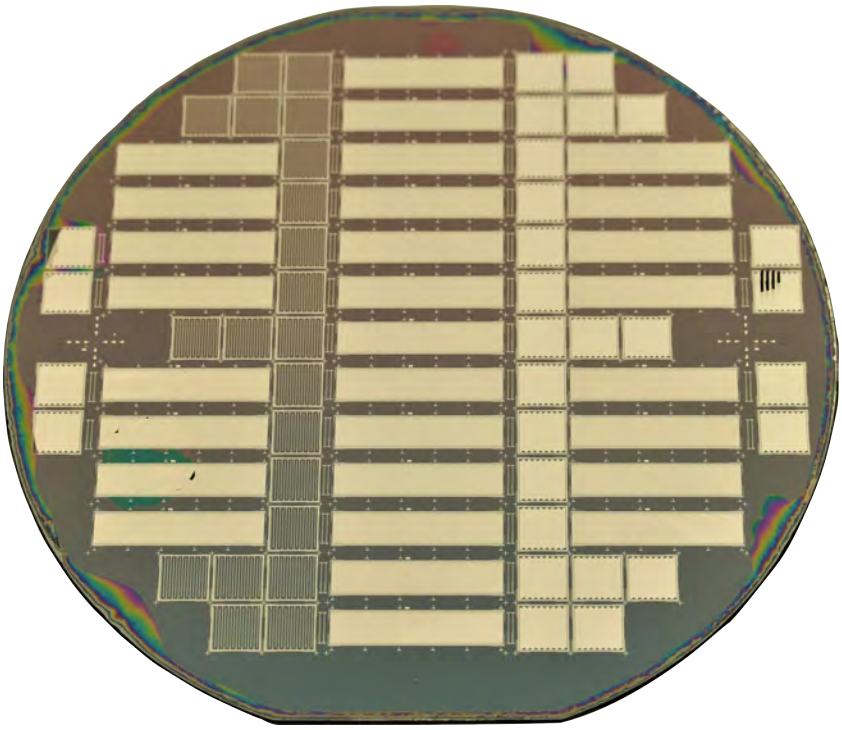
Technical University of Denmark

Ph.D. Thesis

Capacitive Micromachined Ultrasound Transducers for Super resolution Ultrasound Real-time imaging of Erythrocytes

Author:
Stine Løvholt Grue Pedersen

Supervisors:
Prof. Erik Vilain Thomsen
Prof. Jørgen Arendt Jensen



31st July 2023

Kgs. Lyngby, Denmark

Cover image: Wafer with CMUT arrays designed and fabricated during this project for super resolution imaging.

Technical University of Denmark
Department of Health Technology
Ørsteds Plads 345C
2800 Kgs. Lyngby
Denmark
Web: www.healthtech.dtu.dk
E-mail: healthtech-info@dtu.dk
Author e-mail: stlope@dtu.dk

Preface

This Ph.D. thesis has been submitted to The Technical University of Denmark (DTU) as a partial fulfillment of the requirements for the degree of Doctor of Philosophy. The research has been supervised by Professor Erik Vilain Thomsen and Professor Jørgen Arendt Jensen. This thesis comprises a recapitulation of the research conducted from June 2019 to July 2023 at the Institute of Health Technology at DTU.

Prior to this Ph.D. project, the MEMS group at DTU Health Technology had conducted research within the field of Capacitive Micromachined Ultrasonic Transducer (CMUT) for several years. As a result, a profound knowledge of CMUT technology was already established prior to my research.

Stine Løvholt Grue Pedersen
Kgs. Lyngby, July 2023

Summary

Medical ultrasound is a widely used imaging modality, which is considered harmless and cost-effective compared to other imaging modalities like X-rays and CT scans. The ultrasound system relies on a transducer responsible for emitting and receiving ultrasonic waves. Conventional scanner systems utilize a piezo ceramic transducer, typically composed of lead zirconate titanate (PZT) materials.

This thesis investigates an alternative transducer technology, called Capacitive Micromachined Ultrasound Transducers (CMUT), which is fabricated using conventional semiconductor methods. CMUT-based transducers offer various advantages compared to conventional PZT probes, such as temperature stability, greater design flexibility, and broader bandwidth.

The primary objective of this Ph.D. project was to design, develop, and fabricate a linear CMUT-based array for super-resolution ultrasound imaging in real-time of erythrocytes, with the ultimate goal of detecting cancer and diabetes at an earlier stage.

Additionally, the project aimed to design and develop an alternative transducer implementation method utilizing backside contacting, allowing for the integration of a CMUT-based array into a laparoscope. Related process optimization was conducted for processes essential to achieve successful backside contacting and was implemented on a 2D CMUT-based array.

A theoretical framework was provided to enhance the understanding of the CMUT behavior, including the derivation of classical expressions for essential CMUT parameters. Finite element analysis was employed to extend the classical theory to a wider range of plate geometries and clamping conditions.

A 15 MHz transducer with an element pitch of $\lambda/2$ was fabricated and electrically characterized using a novel wafer-level characterization method. The method employed a step-wise selection approach, exclusively focusing on the most promising arrays to save time compared to a comprehensive characterization of all arrays. Four 16-element arrays were assembled and subsequently acoustically characterized, demonstrating successful performance with bandwidths exceeding 100 % during transmission and ranging from

85 % to 120 % based on pulse-echo measurements.

Resumé

Medicinsk ultralyd er en udbredt billedteknik, der betragtes som harmløst og har lavere omkostninger sammenlignet med andre billedmodaliteter såsom røntgen og CT-scanning. En central del af ultralydssystemet er transduceren, som faciliterer udsendelsen og modtagelsen af ultralydsbølger. Konventionelle scanner systemer bruger en piezokeramisk transducer, som typisk er sammensat af materialer såsom blyzirkonattitanat (PZT).

Denne afhandling undersøger en alternativ transducerteknologi kaldet Kapacitive Mikromekaniske Ultralydstransducere (forkortet CMUT), der fremstilles ved hjælp af konventionelle halvledermetoder. CMUT-baserede transducere har flere fordele sammenlignet med konventionelle PZT-prober, såsom temperaturstabilitet, større designfleksibilitet og bredere båndbredde.

Det primære formål med dette Ph.D.-projekt var at designe, udvikle og fabrikere en højfrekvent lineær CMUT-baseret transducer til medicinsk billeddannelse anvendelig til superopløsning i realtid af erytrocytter (røde blodlegemer) med det ultimative formål at detektere kræft og diabetes på et tidligere stadie.

Desuden havde projektet til formål at designe og udvikle en alternativ implementeringsmetode af transduceren ved at anvende bagkontaktering, hvilket muliggøre integration af en CMUT-baseret transducer i et laparoskop. Den nødvendige procesoptimering for at opnå succesfuld bagsidekontaktering blev udført og implementeret på et 2D CMUT array.

Den første del af afhandlingen indeholder en teoretisk gennemgang af essentielle CMUT parametre baseret på klassisk plade teori. For at opnå en bedre forståelse for opførslen af tykke plader, som er påkrævet for at opnå høj frekvens, blev "finite element"-analyse implementeret til at udvide forståelsen fra den klassiske teori til et større parameterrum for pladegeometrier og grænsebetingelser.

En 15 MHz transducer med et element pitch på $\lambda/2$ blev fabrikeret og elektrisk karakteriseret ved hjælp af en nyudviklet "wafer-lever"-karakteriseringsmetode. Metoden er baseret på en trinvis tilgang og udvægelsesmetode til udelukkende at fokusere på de mest lovende arrays for at spare tid i forhold til en omfattende karakterisering af alle arrays. Fire 16-elements ar-

rays blev monteret på "chip carrier boards" og efterfølgende indkasplet før de gennemgik en akustisk karakterisering, hvilket demonstrerede en ydeevne med båndbredder over 100 % under udsendelse og varierende fra 85 % til 120 % baseret på puls-ekko-målinger.

Acknowledgements

First, and foremost, I would like to dedicate a huge thanks to Professor Erik Vilain Thomsen for your exceptional guidance and moral support as my main supervisor throughout this project. I would also like to thank my co-supervisor Professor Jørgen Arendt Jensen for your guidance, dedication, and insightful feedback helping me in the right direction. Thanks for your endless optimism creating a unique and inspiring research environment. I am truly honored for you to let me take part in your cutting-edge research and try to push the limits every day.

Furthermore, I would like to thank the entire team of the MEMS group at DTU Health Technology: Rune Sixten Grass, Kitty Steenberg, Mélanie Audoin, Mathias Engholm, Andreas Havreland, Martin Lind Ommen, and Kasper Fløng Pedersen. I genuinely appreciate the remarkable professional support and collaboration we have shared. I am incredibly proud of the things we have accomplished and for the work environment, you have created. Additionally, I want to thank the students who have worked under my supervision. Your dedication and contributions have played a crucial role in the development and advancement of CMUT technology.

Last, but definitely not least, I would like to extend my deepest gratitude to my family for their support throughout this journey. A special thanks to my daughter, Nora, and you Martin for your unwavering love, support, and encouragement and for always believing in me.

Acronyms

AFM Atomic Force Microscope

AOE Advanced Oxide Etch

ASE Advanced Silicon Etch

BARC Bottom Anti-Reflection Coating

BGA Ball-Grid Array

BHF Buffed HydroFluoric acid

BOX Burried OXide

CCB Chip Carrier Board

Cf Capacitance-frequency

CFU Center for Fast Ultrasound Imaging

CMUT Capacitive Micromachined Ultrasonic Transducer

CPT Classical Plate Theory

CV Capacitance-Voltage

DREM Deposit, Remove, Etch, Multistep

DTU Technical University of Denmark

DUT Device Under Test

EMI Electromagnetic Interference

ERC European Research Council

FEM Finite Element Method

FSDT First order Shear Deformation Theory

H_3PO_4 Phosphoric acid

HCP Hexagonal Closed-Packed

HEPA High Efficiency Particulate Air

HF HydroFluoric acid

HNO_3 Nitric acid

IUS International Ultrasound Symposium

IV current-voltage

KOH Potassium Hydroxide

LNA Low-Noise Amplifier

LOCOS LOCal Oxidation of Silicon

LPCVD Low Pressure Chemical Vapour Deposition

MEMS Micro Electro-Mechanical Systems

NAVMI Non-dimensionalized Added Virtual Mass Incremental

PL Photo Luminescence

PSOI Poly-Silicon-On-Insulator

PZT Lead Zirconate Titanate

RIE Reactive Ion Etching

SEM Scanning Electron Microscope

SNR Signal-to-Noise Ratio

SOI Silicon-On-Insulator

SURE 3-D Super resolution Ultrasound Real time imaging of Erythrocytes

Zf impedance-frequency

Contents

CHAPTER 1

Introduction

The foundation of the field of ultrasound was established from the discovery of the piezoelectric effect first documented by Pierre and Jacques Curie in the early 1880s [1]. In 1946 the French physiotherapist André Denier first proposed the use of ultrasound to create images of the internal structures of the human body [2]. Unluckily, Denier did not manage to build a successful device, resulting in the Austrian neurologist Karl Theo Dussik, in collaboration with his brother Friedreich, to become the first to generate an ultrasonic image for medical purposes [2]. Since the 1950s, the medical ultrasound industry has emerged remarkably, and sonography is now a widely used imaging modality for visualization of soft tissues. The fundamental principle behind modern sonography is still the piezoelectric effect. Examples of one of the most well-known applications are fetus sonographs captured during pregnancy using both 2D and 3D techniques. Compared to other imaging modalities, such as X-rays and CT scans, ultrasound is considered harmless and provides real-time imaging. Furthermore, it is a portable and non-invasive imaging technology that is relatively inexpensive. These factors contribute to its widespread availability in comparison to other imaging modalities. This is further emphasized by the mission of the company Butterfly Network, Inc. (Guilford, CT, USA) whose mission is to produce a hand-held ultrasound device at a price making it achievable worldwide [3]. In 2018 the company released the first handheld, single-probe, whole-body system based on semiconductor technology, more specifically Capacitive Micromachined Ultrasonic Transducer (CMUT) technology.

However, ultrasound does have some limitations. It offers lower resolution and penetration depth compared to X-rays, CT scans, and MRIs. Despite these drawbacks, its numerous advantages have made it a valuable

imaging tool in the medical field.

Ultrasound is defined as acoustic pressure waves with a frequency exceeding 20 kHz, which is beyond the detectable limit for human audibility. Ultrasound images are created by transmitting a pressure wave into a medium. Subsequently, the wave interacts with objects within the medium, resulting in reflection and scattering. The echo signal produced by this interaction is then detected by a transducer, and signal post-processing is employed to generate the well-known grayscale ultrasound B-mode images.

Essential for the ultrasound system is therefore the transducer, which serves the dual purpose of transmitting and receiving the signal. Ultrasonic transducers are found in various shapes and frequencies, each tailored to a specific application. For instance, in cardiovascular ultrasound, the probe must be designed to fit between the ribs to visualize the movement of the heart. This is necessary due to a significant mismatch in acoustic impedance between the bone and tissue. In addition, imaging through bones is infeasible, due to a high signal attenuation, which ranges from 16 dB/MHz cm to 23 dB/MHz cm [4].

Up till this day, the majority of commercially available ultrasound transducers are based on Lead Zirconate Titanate (PZT) materials. When a potential is applied across a PZT crystal it results in material deformation, which generates and emits a sound wave. A piezoelectric crystal can consist of various chemical compositions and extensive investigation and optimization have been conducted over the years [5, 6]. During this thesis, the term PZT will be used as a general reference.

However, these PZT-based transducers have some disadvantages limiting the use for some imaging sequences. In applications involving long bursts of pulsed excitations, the primary limiting factor is the heating that occurs within the transducer itself [7]. Examples of such applications include color Doppler, therapeutics, and B-mode imaging employing coded excitation. Particularly, coded excitation is an interesting technique that can enhance image quality. This imaging technique has shown a significant improvement in penetration depth while preserving both axial resolution and contrast [8, 9]. This means that one of the essential requirements for the transducer is to limit or even eliminate the self-heating problem experienced by the PZT transducer. Furthermore, the transducer should ideally have a frequency bandwidth exceeding 100 %.

In 1994, the first semiconductor-based ultrasound transducer was proposed by Khuri-Yakub as an alternative to the conventional PZT transducer. This innovative concept was presented in the conference proceeding "A surface micromachined electrostatic ultrasonic air transducer" [10]. The paper introduced a 1.9 MHz air transducer with a bandwidth of 20 %, which was four times better than the reference piezo transducer available at the same

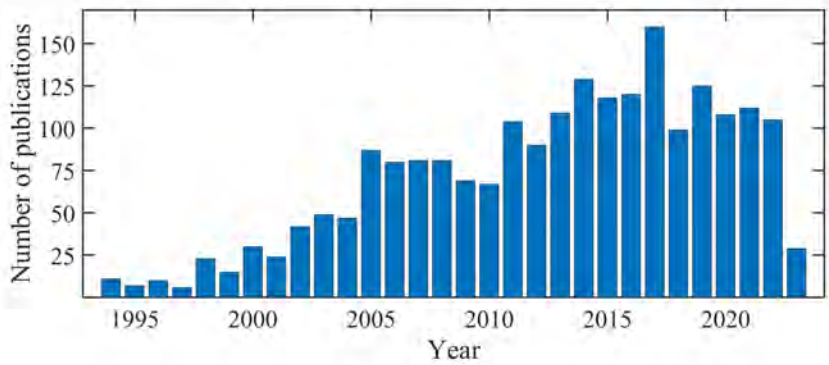


Figure 1.1: Overview of published CMUT papers since 1994. The keywords applied in the search tool Scopus were: "capacitive micromachined ultrasonic transducer*" or "CMUT*" or "Electrostatic ultrasonic air transducer" or "Capacitive Transducer*" or "Surface Micromachined Transducer*"

time. The silicon-based structure was fabricated using a sacrificial release process. An extended version of the paper was published in 1996 as a journal article by the same authors [11]. This publication described the temperature insensitivity of the CMUT in comparison with the very temperature sensitive PZT transducer. The publication became the foundation of the later CMUT research field. Since the mid/late 1990s the CMUT structure has gained widespread interest worldwide, and the number of publications has gradually increased over the years, as presented in Fig. 1.1. Development of CMUT-based arrays is the main focus of this thesis.

1.1 CMUT

A CMUT is a miniature capacitive device that consists of a solid substrate and a flexible top plate, which are separated by an electrically insulating material and a cavity with a defined gap height g. A cross-sectional illustration of the structure is given in Fig. 1.2a. The most commonly used cell layout is either squared or circular [12]. This thesis simply addresses circular cells, with the radius defined as a. The device frequency is determined by the combination of the cell radius and the thickness of the top plate, which is denoted h.

The working principle behind the CMUT is depicted in Fig. 1.2b and 1.2c for transmit and receive, respectively. When a DC potential is applied across the structure, an electrostatic force is generated, causing the flexible top plate to deform towards the substrate. Simultaneously, a mechanical restoring force arises from the stiffness of the plate, counteracting the attraction and establishing an equilibrium state. In this stable position, the plate exhibits a specific center deflection denoted as w_0. If the applied volt-

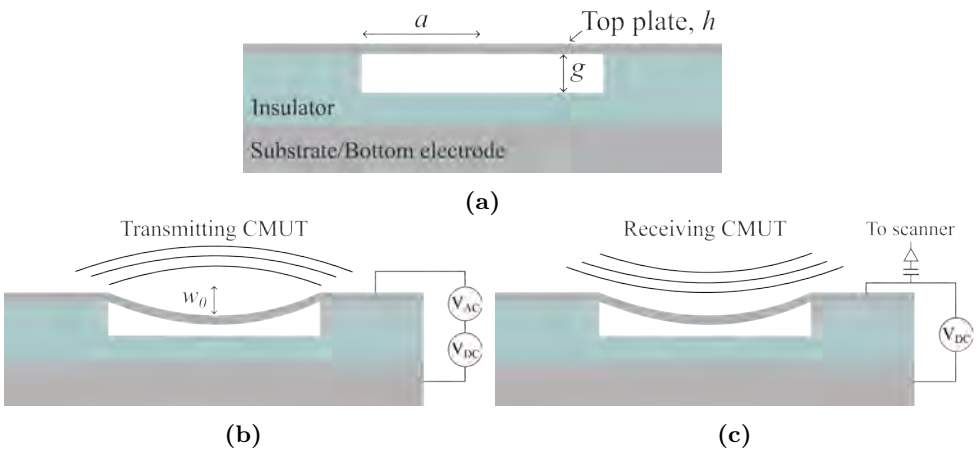


Figure 1.2: Cross-sectional illustration of a CMUT cell. **(a)** Outlines the key definitions for the structure and shows the cell without applied bias. **(b)** Depicts the working principle behind the CMUT in transmit. Sound waves are generated by superimposing an AC potential on top of a DC potential. **(c)** Shows how a pressure wave causes the plate to bend in receive. The signal is transformed into an electrical signal read by the scanner. The figures are not drawn to scale.

age is further increased beyond a certain threshold, known as the pull-in or collapse voltage (V_{pi}), the electrostatic force overcomes the spring force in the plate, resulting in a collapse of the top plate onto the substrate. The insulating material within the cavity is designed to prevent an electrical breakdown of the device when a potential exceeding the pull-in voltage is applied.

Following the preload of the plate, the CMUT is actuated by superimposing an AC signal on top of the DC potential. This induces oscillations of the plate, leading to emission of an acoustical pressure wave. In receive mode, the echoed signal deforms the plate. This mechanical deformation is translated into an electrical signal by measuring a change in capacitance. Through signal processing algorithms, a collection of such signals is transformed into ultrasonic images of the internal structures of the body.

CMUTs offer significant advantages over PZT transducers in terms of design and fabrication flexibility. This is primarily caused by the utilization of semiconductor technology for CMUT fabrication, which provides a larger design space with lithography as the limiting horizontal factor. In contrast, PZT transducers are often fabricated by dicing separate elements in a crystal, making the width of the saw blade a limiting factor for PZT probe fabrication. Furthermore, CMUTs offer more than 100 % bandwidth due to better acoustic matching with the propagation medium. Finally, studies have demonstrated that replacing PZT with CMUTs can effectively minimize the problem of probe self-heating [13–15].

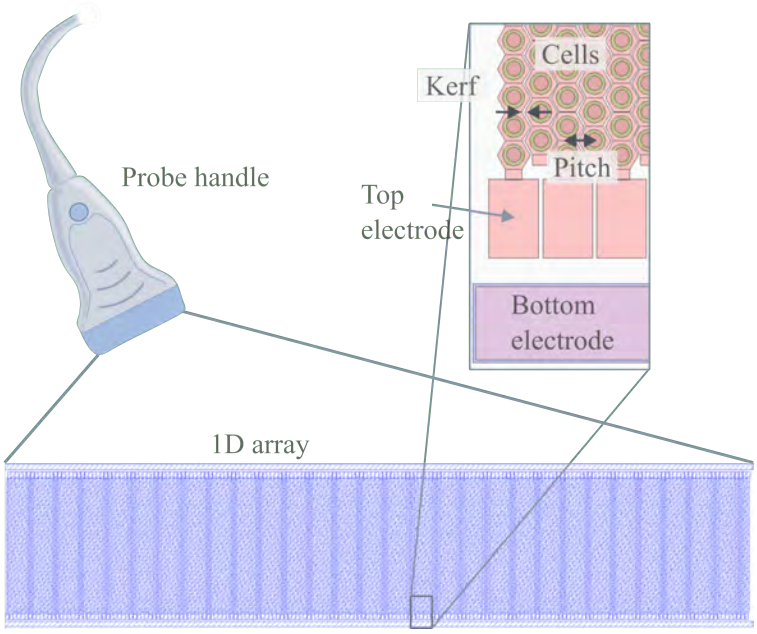


Figure 1.3: Overview of a CMUT-based linear 1D array defining array relevant parameters. Inspired from [16].

The field of ultrasound imaging provides both 2D and 3D image acquisition [17–19]. These two modalities require different probes: 1D arrays are used to acquire 2D images, while 2D arrays are utilized for 3D imaging [20,21]. Various array layouts exist within both categories. This project primarily focuses on 1D arrays, which are also referred to as linear arrays. The outline of a typical linear array, comprising 384 elements, is provided in Fig. 1.3. Each element contains multiple CMUT cells. The distance between the center of two neighboring elements is defined as the pitch, while the width between the elements is referred to as the kerf. According to the findings in [22], the element pitch is a crucial design parameter, that can reduce grating lobes remarkably, thus providing improved image quality. Many linear arrays typically contain a shared bottom electrode, while the top electrode is separated for the individual elements. The elements are then assessed through wire bonds employed for electrical integration [13, 23]. However, alternative structures with a common top electrode and separate bottom electrodes have also been studied in literature [24–27].

Besides the enhanced design flexibility, the utilization of semiconductor techniques facilitates various fabrication methods, each with its individual advantages. Overall two categories exist: the sacrificial release process and the wafer bonding process. The wafer bonding category can be further categorized into various bonding techniques, and an incomplete list includes

fusion bonding, anodic bonding, thermocompression bonding, and adhesive bonding [28]. During this thesis, the investigated fabrication techniques are all based on the fusion bonding technique, which is therefore the bonding technique extensively discussed in the following sections.

1.1.1 Literature Review

The initial suggestion of a CMUT structure was fabricated using a sacrificial release process [11], which has been optimized and refined over the years [29, 30]. The sacrificial release process is based on surface micromachining techniques, where a sacrificial layer is deposited underneath the top plate material. The CMUT structure is subsequently released by wet etching the sacrificial layer through vias in the plate. The etch selectivity between the sacrificial layer and the plate material is crucial for the process. The technique is in general simple and the first proposed process only included one lithography step. Compared to the wafer bonding technique, the sacrificial release process is a high yield process [28]. However, there are certain limitations and drawbacks associated with this approach. These include stiction-related issues, which can impede the release process. Additionally, the stresses experienced by the plate material may pose challenges. Finally, the sacrificial releases process has constraints on the obtainable plate thickness as well as the cavity height [31]. This can impose limitations on the overall design and performance of the system.

In 2002 and 2003, an alternative method was proposed utilizing wafer bonding techniques [32, 33]. This approach employs two wafers: one serving as the substrate where the cavities are defined, and one wafer acting as the top plate. In the early stage of CMUT fabrication using wafer bonding, the cavities were formed by etching into either the substrate or a grown insulating oxide layer. The second wafer consisted of a commercially available Silicon-On-Insulator (SOI) wafer, which was fusion bonded to the substrate wafer. General advantages of wafer bonding processes include greater design flexibility in gap height and top plate thickness. Furthermore, wafer bonding provides a high bonding strength and is highly temperature stable. It facilitates bonding various atmospheric environments, including vacuum. However, compared to the sacrificial release process, the wafer bonding technique generally has a lower yield. The most critical step in this fabrication method is the bonding step itself, which requires a high level of cleanliness, low surface roughness (less than 1.0 nm), and limited wafer bow (less than 5 µm for a 4” wafer) [34].

A reverse sacrificial release process was proposed in 2005 by [26]. This method involved depositing the top plate as the first layer and subsequently building the CMUT structure towards the bottom substrate. It resulted in a common grounded top electrode facing the patient and allowing for electrical integration from the backside, as demonstrated in [20].

Figure 1.4: Four CMUT-based linear probes designed and fabricated by Ph.D. Søren E. Diedrichsen [16].

The first use of a LOCal Oxidation of Silicon (LOCOS) process combined with the fusion bonding approach for CMUT fabrication was published in 2008 [35]. This approach improved the gap height control while reducing the parasitic capacitance. In 2011 the proceeding was supplemented by a more detailed journal paper [36]. The substrate was fabricated by applying two consecutive thermal oxidation steps to form bumps in the silicon. The oxide layer was removed before a conventional LOCOS process was performed using a masking nitride layer. The LOCOS process formed the cavities and prepared the substrate for the subsequent fusion bonding process.

Within the research group of the author, various alternative LOCOS based designs and fabrication methods have been investigated for linear CMUTs [16]. An image of four successfully integrated probes is provided in Fig. 1.4. One of the utilized fabrication methods employed two consecutive LOCOS processes: one to form the silicon bumps and one to create the device cavities. The substrate wafer was then fusion bonded to a SOI wafer. The work resulted in full integration of four probes as part of a collaboration with BK Medical (Herlev, DK).

The fabrication processes applied in this thesis all rely on a combination of LOCOS and fusion bonding. Fusion bonding was chosen due to its advantages over sacrificial release and anodic bonding methods. To accommodate a requirement on high emission frequency, a thick top plate is necessary, which is challenging to achieve with sacrificial release processes [28]. Furthermore, recent findings documented problems with vertical short circuits for the anodic bonding process. These shorts are related to gold pen-

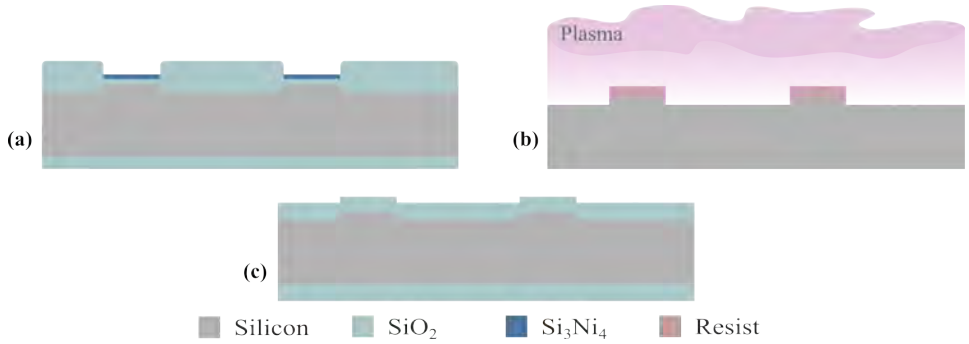


Figure 1.5: Illustrations of the three processing methods tested for silicon bump fabrication during this Ph.D. project. **(a)** Shows fabrication using a LOCOS-based process, **(b)** shows a dry-etching based process, and **(c)** depicts a method applying two consecutive thermal oxidation steps.

etrating a barrier nitride layer connected to the highly doped poly-silicon top electrode and severely decreases the yield [37]. Research conducted by Havreland et. al. [38, 39] highlighted concerns about the ωRC product, where ω represents the angular frequency, and R and C denote the element resistance and capacitance, respectively. The study specifically investigated the impact on the pressure profile along the element for silicon-based devices. However, this does not pose a problem for linear arrays, due to their relatively small elevation height compared to 2D arrays with a high element count. Finally, fusion bonding has been extensively used and optimized within this research group over the last years [16, 39–42]. These processes have demonstrated excellent stability over time and negligible or none dielectric charging effects. This work formed the foundation for the further developments presented in this thesis.

As part of the research conducted during this Ph.D. project, three methods for fabricating the silicon bumps were tested and compared for optimal performance and throughput. Illustrations of the methods are provided in Fig. 1.5. The first method is based on the LOCOS process, using a nitride masking layer shown in (a). It serves as a standard method within this research group. The second method is a time-optimized alternative that utilizes dry etching, depicted in (b). The third method follows the approach proposed by Park et al. [36] and involves two consecutive thermal oxidation processes, as shown in (c).

1.2 Transducer for a Laparoscope

Ultrasound imaging involves a fundamental trade-off between penetration depth and resolution. To obtain high-resolution images, a probe with a high frequency is necessary. However, higher frequencies lead to increased

Figure 1.6: Conceptual overview of a laparoscope with an integrated ultrasound transducer used for guidance during surgery in the abdomen.

attenuation, resulting in a reduction in Signal-to-Noise Ratio (SNR) and limited penetration depth. To overcome this, a smaller transducer size can be employed for in vivo imaging during surgical procedures. By reducing the transducer size, the required penetration depth is decreased, facilitating the acquisition of higher resolution images using a high-frequency transducer. An example of such an integrated transducer is found in a laparoscope, which is a minimally invasive technique [43] with a typical diameter of approximately 5 mm [44]. An illustration of the concept is provided in Fig. 1.6, where the ultrasound transducer is located at the end of the laparoscope.

This Ph.D. project was initially performed in collaboration with the company BK Medical, aiming to integrate a CMUT into a laparoscope, for high resolution visualization of the abdomen. The objective was to fabricate a small-sized transducer array that maintained a high image quality. To meet this goal, certain requirements had to be met for the array. Semiconductor-based technologies used for CMUT fabrication provide significant design flexibility, making them suitable for realization of a high-frequency laparoscopic ultrasound transducer.

Miniaturizing the array was crucial for its implementation in the laparoscope due to space limitations. To maximize the active area of the array in the limited available space, an alternative method, compared to wire bonding approaches, was considered for electrical integration with a Chip Carrier Board (CCB). This involved using the substrate as a via architecture and contact point for Ball-Grid Array (BGA) bonding, as proposed in previous studies [45, 46]. This bonding technique mitigates parasitic contributions from wire bonds and is suitable for large-scale production. It requires separate bottom electrodes and a common top electrode connected to the ground. Furthermore, this approach moves the operational bias voltage away from the patients and eliminates the need for an external electromagnetic interference shield. In the existing literature, successful backside contacting of

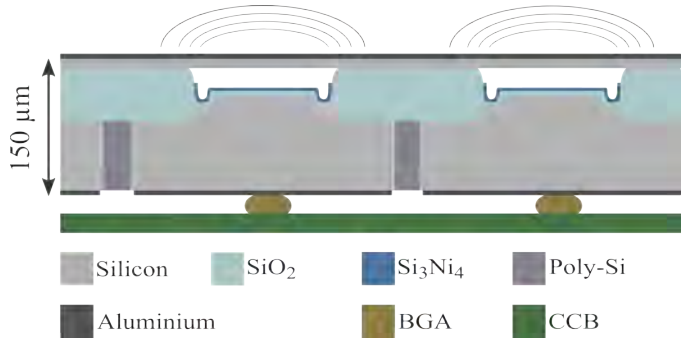


Figure 1.7: Proposed structural cross-section of two CMUT cells integrable with a laparoscope. The bottom electrode is separated by a high aspect ratio silicon etching process. The illustration includes bonding to a CCB and is reprinted from Paper B.

CMUTs has been demonstrated using through-silicon vias filled with poly-silicon or utilizing air-filled trenches as insulation [24, 25].

A conceptual cross-sectional overview of a CMUT structure with separate bottom electrodes is provided in Fig. 1.7. The CMUT cells are fabricated by a LOCOS process, with a bump structure in the center of the cavity. To achieve bottom electrode separation, high aspect ratio silicon trenches are created through a dry etching process described in [47]. These trenches are subsequently electrically insulated from each other using a thermal oxide and mechanically reinforced by poly-silicon plugs. After fusion bonding of the top plate to the substrate, the device can be mounted on a custom-made CCB utilizing BGA bonding methods.

Due to a discontinued collaboration with BK Medical, the scope of the Ph.D. project was changed. Therefore, the fully integrated laparoscopic design was never realized. However, significant efforts were dedicated to optimizing two crucial steps involved in the separation of the bottom electrodes. These optimizations were subsequently implemented in a 2D transducer design, resembling the one described in Paper C.

1.3 Transducer for SURE

This Ph.D. project has partly contributed to the "3-D Super resolution Ultrasound Real-time imaging of Erythrocytes" (SURE) project. The overall objective of the project is to develop an innovative super-resolution ultrasound-based imaging technique capable of resolving capillary flow in the human body. This method involves tracking of individual red blood cells (erythrocytes), which will be a paradigm shift in medical imaging that can innovate and enhance the diagnosis of diseases such as cancer and dia-

betes, as well as various cardiovascular conditions. Early diagnosis is crucial for optimal and effective treatment. The SURE project, funded by the European Research Council (ERC), is a collaborative synergy research initiative involving multiple stakeholders, including the MEMS Applied-Sensors group and the Center for Fast Ultrasound Imaging (CFU), both located at The Technical University of Denmark (DTU) (Kongens Lyngby, DK). Furthermore, Copenhagen University Hospital and The University of Copenhagen are also key participants in the project.

While the ultimate goal of the project is to achieve 3D ultrasound imaging, the foundation for realizing this includes the development of a well-functioning 2D super resolution imaging system. Therefore, a significant part of this thesis focuses on the design, development, and fabrication of a suitable CMUT-based linear transducer. A key parameter of the transducer is the resonance frequency, f_{res}, which affects both the axial and the lateral resolution of the image. The axial resolution is defined as

$$\lambda = \frac{c_{\mathrm{m}}}{f_{\mathrm{res}}} \tag{1.1}$$

where c_{m} denotes the speed of sound in the medium. For body tissue an average value of 1540 m/s is often used [4]. The lateral resolution depends on the imaging depth, Z_{depth} and the aperture width, and is defined as

$$\mathrm{FWHM} = \lambda \frac{Z_{\mathrm{depth}}}{N \times \mathrm{pitch}} = \lambda \mathrm{F}_{\#}. \tag{1.2}$$

Here N is the number of elements and $\mathrm{F}_{\#}$ refers to the F-number, which should be as small as possible to increase the lateral resolution. Based on these relations it can be deduced that high image resolution necessitates a high resonance frequency, as well as a wide aperture, hence a large number of elements. Consequently, the objective was to fabricate a 15 MHz transducer with 384 elements.

Furthermore, the importance of the element periodicity was investigated in the study presented in [22]. The publication compared simulations and measurements for a probe with λ-pitch and $\lambda/2$-pitch. The results demonstrated that, particularly for a low number of emission lines, the $\lambda/2$-pitch transducer exhibited minimal, negligible grating lobes artifacts. Grating lobes can cause a degradation in the point spread function, and thereby reduce the image quality. Based on these findings, an essential requirement for the array designed for the SURE project involved having a pitch equal to $\lambda/2$.

1.4 Publications

This thesis is partly based on the following publications in which the author has contributed as either the main author or as co-author.

Paper A (2022): S. L. Grue Pedersen, A. S. Havreland, O. Hansen and E. V. Thomsen.
"Accurate Radiation Impedance Analysis for CMUT Design,"
Published in *Proceedings of IEEE International Ultrasonics Symposium,* 2022, pp. 1-4.

Paper B (2020): S. L. Grue, M. Engholm and E. V. Thomsen.
"Electrical Insulation of CMUT Elements Using DREM and Lapping,"
Published in *Proceedings of IEEE International Ultrasonics Symposium,* 2020, pp. 1-4.

Paper C (2022): R. S. Grass, M. Engholm, A. S. Havreland, C. Beers, M. L. Ommen, **S. L. G. Pedersen**, L. N. Moesner, M. B. Stuart, M. T. Bhatti, B. G. Tomov, J. A. Jensen, and E. V. Thomsen.
"A Hand-Held 190+190 Row–Column Addressed CMUT Probe for Volumetric Imaging,"
Published in *IEEE Open Journal of Ultrasonics, Ferroelectrics, and Frequency Control,* 2022, vol. 2, pp. 220-236.

In addition to the above publications, the author participated physically at the 2019 IEEE International Ultrasonic Symposium (IUS). In 2020 at the online version of the conference, the author presented a poster about "Electrical Insulation of CMUT Elements Using DREM and Lapping" (Paper B), which is also presented in Chapter 4. In 2021 the author contributed with a poster presentation regarding "Analytical CMUT Modelling using Effective Radius Theory", which is further elaborated in Chapter 2. Finally, the author participated in person at the conference in 2022, presenting a poster about "Accurate Radiation Impedance Analysis for CMUT Design" (Paper A). This work is presented in Chapter 2.

Articles in Preparation

Currently, three articles are in preparation and in partly writing.

The first article is an in-depth description of the work presented at the IUS conference in 2021 about analytical modeling using effective radius theory on CMUTs. This work takes stress distributions in the top plate into account and considers the influence of the clamping conditions on the resonance frequency, the pull-in voltage, and the plate deflection. The conducted work is presented in Chapter 2, Section 2.3.

The second paper investigates the influence of shear effects on key parameters for the CMUT when decreasing the plate aspect ratio due to requirements on high frequency and small pitch arrays. The work is based on Finite Element Method (FEM) simulations of the plate deflection, resonance frequency in vacuum and immersion, as well as the pull-in voltage and distance. The simulations are evaluated against expression without shear effects and new analytical expressions encountering such effects are currently under development. The work is presented in Chapter 2, Section 2.4.

The third planned article includes integration of a 384 linear array with $\lambda/2$-pitch into an in-house made prototype probe described and developed by Ph.D. student Kasper F. Pedersen [48]. The paper is intended to include the entire process from design specifications, to fabrication method, electrical characterization, and probe assembly followed by acoustical characterization, all steps performed within this research group. Currently, a CCB is under development enabling integration of the array into the prototype probe. The CCB is expected to be finalized within the coming months. The work is presented from Chapter 3 to 8.

1.5 Thesis Outline

The remaining of this thesis is divided into nine chapters. Chapter 2 starts by presenting the well-establish classical plate theory widely used for initial analytical array design. Thereafter, a more accurate approximation of the radiation impedance is provided and implemented in the equation of motion used to derive the resonance frequency in immersion. It is followed by a study on the bonding conditions where the stress distribution in the bonding region is included. Finally, the chapter presents a simulation based study, where shear effects in the plate are considered for CMUT key parameters.

Chapter 3 introduces the design methodology used for array design. This work includes both analytical calculations as well as simulation based results. The applied mask layout is subsequently introduced, followed by a simulation based study on the parameter space for a single LOCOS process. The chapter ends with a study analyzing the outline of the cavity comparing the three different fabrication methods, employed for array fabrication.

Chapter 4 presents the process development performed to allow for transducer integration from the backside. This includes the optimization of a deep silicon etching technique in combination with uniform trench filling. The second part of the chapter describes the mechanical substrate thinning technique, called lapping.

Chapter 5 is concerned with the fabrication of a linear array employing a combination of LOCOS and fusion bonding processes. Three different methods are tested for fabrication of the silicon bumps on the substrate

wafer: one based on a conventional LOCOS process, one based on a dry etching RIE process, and one based on a maskless LOCOS process. These methods are explained in detail and compared after the bump fabrication and the cavity definition.

Chapter 6 introduces a novel wafer-level characterization method utilizing visual inspection followed by unbiased impedance measurements. The chapter establishes some selection criteria and highlights potential errors, associated with either measurement technicalities or fabrication errors.

Chapter 7 presents the characterization results obtained from the wafer-level characterization method. Two wafers underwent characterization, one fabricated using two consecutive LOCOS processes and one using the maskless LOCOS process. Based on the criteria defined in Chapter 6, few arrays underwent a full characterization before potential probe integration.

Chapter 8 describes the probe integration process, including the chip mounting, wire bonding, and casting process. The second part of the chapter describes impedance measurements performed subsequent to integration, together with the acoustical measurements performed on the assembled arrays.

Chapter 9 concludes the thesis and discusses future investigations.

CHAPTER 2

Transducer Modeling

The ultrasound transducer is an essential part within an ultrasound system as it is responsible for emitting and receiving the ultrasound waves, which are utilized for image formation. Therefore, understanding and accurately predicting the behavior of the CMUTs is crucial for the advancement of transducer technology. This chapter addresses the transducer modeling from a theoretical and simulation based perspective. The top plate is a central component of the CMUT structure and its geometry significantly affects several key parameters of the ultrasound transducer, including the plate deflection, the resonance frequency, and the pull-in voltage.

Often complicated FEM simulations are employed to predict the transducer behavior, which has the advantage of being reasonable precise. However, such simulations are often both time consuming and do not reveal any scaling relations. For this reason, it is desired to establish a simpler starting point for the design phase by deriving analytic expression for some of the key parameters. Furthermore, the aspect ratio of the plate, denoted a/h, influences the behavior and transducer parameters. Here a denotes the radius and h represents plate thickness, respectively. Based on the plate aspect ratio, plates can be categorized as either thin or thick plates. Since no exact definition exists, this can vary in literature. However, thin plates are often (as well as in this thesis) defined as plates with aspect ratios larger than 10, while thick plates have aspect ratios below 10.

The first section of this chapter describes some of the essential parameters for the CMUT employing classical plate theory. The second section covers analytical modeling of the resonance frequency in immersion, attempting to expand the geometric validity of the expression derived by Lamb in 1920 [49]. The derivation is accomplished through the use of a Padé expansion

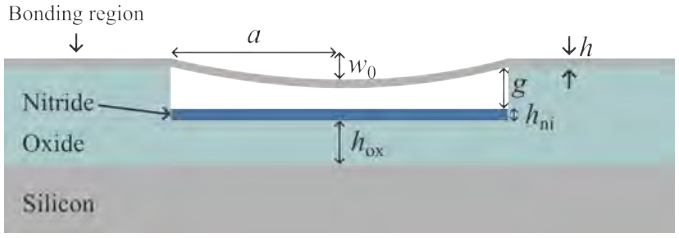


Figure 2.1: Cross-sectional view of a simple CMUT cell. Geometric parameters are defined in the figure. Note, the illustration is not to scale.

of the radiation impedance. FEM simulations were performed to verify the analytical findings.

In the third section, the influence of the clamping conditions is investigated. This is done through FEM simulations, and the findings are subsequently incorporated into the derived classical analytical expressions.

Finally, the last section studies the shear effects on both thick and thin plate geometries, analyzing the impact on transducer key parameters such as the plate deflection, pull-in voltage, capacitance, and resonance frequency in water.

2.1 Classical Plate Theory

Classical plate theory is applicable to plates with large aspect ratios, typically defined as $a/h > 10$. Thin plates have been widely investigated over time and enable many different Micro Electro-Mechanical Systems (MEMS) based devices, such as piezoresistive pressure sensors [50], and capacitive pressure sensors [51], as well as optical pressure sensors [52, 53]. Since the working principle of CMUTs also relates to the top plate behavior, classical plate theory are commonly employed for initial design and analysis of CMUTs. Fig. 2.1 provides an overview of a simplified CMUT structure, including the definition of its geometric parameters.

2.1.1 Plate Deflection

The plate deflection is fundamental for the behavior of the CMUT and influences both the capacitance and the pull-in voltage. The static deflection of an isotropic thin plate is found by solving the isotropic plate equation initially derived by Kirchhoff-Love [54]

$$\frac{\partial^4 w}{\partial x^4} + 2\frac{\partial^4 w}{\partial x^2 \partial y^2} + \frac{\partial^4 w}{\partial y^4} = \frac{p}{D_\mathrm{i}}. \tag{2.1}$$

Here w is the plate deflection, p is the applied pressure and D_i is the plate stiffness, which is also referred to at the isotropic flexural rigidity

$$D_\mathrm{i} = \frac{Y}{12(1-\nu^2)}h^3. \tag{2.2}$$

Y and ν are material parameters known as Young's modulus and Poisson's ratio, respectively. For a thin circular plate clamped at the periphery, the static solution to Eq. (2.1) yields [55]

$$w_\mathrm{thin}(r) = w_{0,\mathrm{thin}}\left(1-\left(\frac{r}{a}\right)^2\right)^2, r \leq a, \tag{2.3}$$

where $w_{0,\mathrm{thin}}$ is the center deflection of the plate and r is the position along the radius. Applying the boundary conditions $\partial w(0)/\partial r = 0$, $\partial w(a)/\partial r = 0$, $w(a) = 0$ and $w(0) < \infty$ the center deflection of the plate results in

$$w_{0,\mathrm{thin}} = \frac{pa^4}{64D_\mathrm{i}}. \tag{2.4}$$

2.1.2 Eigenfrequency

From the field of mechanical engineering the angular resonance frequency of a plate in vacuum can be expressed in terms of the plate dimensions and material properties. The frequency is often calculated using the Raleigh-Ritz approximation method. However, the exact first resonance frequency in vacuum for a clamped circular plate with no applied potential is calculated by Bessel functions [55]. The result is

$$\omega_0 = 10.2158\sqrt{\frac{D_\mathrm{i}}{a^4 h \rho_\mathrm{p}}}, \tag{2.5}$$

where ρ_p is the density of the plate.

Combining Eq. (2.5) and Eq. (2.2) the full expression becomes

$$\omega_0 = 10.2158\sqrt{\frac{Y}{12(1-\nu^2)\rho_\mathrm{p}}}\frac{h}{a^2}, \tag{2.6}$$

which shows that the angular frequency in vacuum scales with h/a^2 and $\sqrt{Y/\rho_\mathrm{p}}$. For silicon the mean value of ν is 0.177, which results in $(1-\nu^2) = 0.97$, illustrating that the influence of Poisson's ratio is very small.

2.1.3 Electrostatic Analysis

Two other important parameters for the CMUT performance are the capacitance and the pull-in voltage. Both depending on the deflection profile of the plate.

Capacitance

First, the capacitance is derived, which is a measure of stored electrical charge, Q, relative to the applied voltage, V. The unit for the capacitance is Farad. The capacitor consists of two conducting plates and, in this case, two intermediate insulating layers, one of oxide and one of nitride (see Fig. 2.1).

The simplest model to describe this system is the parallel plate capacitor model, which has a capacitance of

$$C = \frac{\epsilon_0 \epsilon_\mathrm{r} A}{g_\mathrm{eff}}. \tag{2.7}$$

ϵ_0 and ϵ_r are the vacuum permittivity and relative permittivity of the insulating material, respectively. A is the area of the plate and g_eff is the effective gap between the electrodes. The effective gap can be expressed as a sum over the stack of materials in the active region of the cell

$$g_\mathrm{eff} = g + \sum_{n=1}^{N} \frac{h_n}{\epsilon_{\mathrm{r},n}}, \tag{2.8}$$

where g is the vacuum gap and N is the total number of insulting layers. h_n and $\epsilon_{\mathrm{r},n}$ denote the thickness and the relative permittivity of the nth dielectric layer, respectively. For the material stack present in Fig. 2.1 the effective gap becomes

$$g_\mathrm{eff} = g + \frac{h_\mathrm{ox}}{\epsilon_\mathrm{ox}} + \frac{h_\mathrm{ni}}{\epsilon_\mathrm{ni}}. \tag{2.9}$$

As a result, the total capacitance for zero deflection can be written as

$$C_0 = \left(\frac{1}{C_\mathrm{vac}} + \frac{1}{C_\mathrm{ox}} + \frac{1}{C_\mathrm{ni}} \right)^{-1} = \frac{\epsilon_0 A}{g_\mathrm{eff}}. \tag{2.10}$$

If the plate deflection is taken into account the general expression for the capacitance becomes [56]

$$C = \frac{1}{g_\mathrm{eff}} \int\int \frac{\epsilon_0}{1 - \eta f(x,y)} \mathrm{d}x\mathrm{d}y. \tag{2.11}$$

Here $\eta = w_0/g_\mathrm{eff}$ is the normalized center deflection and $f(x,y)$ is a function describing the shape of the plate deflection. For a parallel capacitor $f(x,y) = 1$, while for a clamped circular plate the function is given by Eq. (2.3). The capacitance of the parallel plate capacitor then yields

$$C_\mathrm{parallel} = C_0 \frac{1}{1-\eta}, \tag{2.12}$$

while for the circular plate the capacitance is calculated in [57] to be

$$C_\mathrm{circular} = C_0 \sqrt{\frac{1}{\eta}} \mathrm{arctanh} \sqrt{\eta}. \tag{2.13}$$

By utilizing the derived capacitance, it is possible to determine the pull-in voltage and distance through energy considerations.

Pull-in Voltage and Distance

To derive the pull-in voltage and distance for the CMUT, the stored energy in transducer is considered. The following derivation will be based on lumped parameters.

Initially, the total energy is defined for the three domains of interest: the mechanical, the electrical and the acoustical domain. The system is assumed to be loss-less, and the energy is composed of four terms [56]. The total stored energy for the mechanical domain is defined as

$$U_{\mathrm{t,m}} = U_{\mathrm{s}} + U_{\mathrm{kin}} - U_{\mathrm{e}} - U_{\mathrm{p}}, \tag{2.14}$$

where U_{s} represents the stored potential energy, U_{kin} is the kinetic energy, U_{e} denotes the electrical energy stored in the capacitor and U_{p} represents the work done on the system by the external pressure. Inserting the lumped parameters K_0 and m_0, denoting the spring constant and the geometrical mass, respectively, leads to a total stored mechanical energy of

$$U_{\mathrm{t,m}} = \frac{1}{2}K_0 w_0^2 + \frac{1}{2}m_0\left(\frac{\partial w_0}{\partial t}\right)^2 - \frac{1}{2}V^2 C(w_0) - p w_0 A. \tag{2.15}$$

V defines the voltage applied to the system. To determine the stored energy in both the electrical and acoustical domains, it is necessary to adjust the signs to accommodate the altered definition of the work and internal energy [56]. The total stored energies yields

$$U_{\mathrm{t,e}} = -\frac{1}{2}K_0 w_0^2 - \frac{1}{2}m_0\left(\frac{\partial w_0}{\partial t}\right)^2 + \frac{1}{2}V^2 C(w_0) - p w_0 A, \tag{2.16}$$

$$U_{\mathrm{t,a}} = -\frac{1}{2}K_0 w_0^2 - \frac{1}{2}m_0\left(\frac{\partial w_0}{\partial t}\right)^2 - \frac{1}{2}V^2 C(w_0) + p w_0 A. \tag{2.17}$$

Differentiating Eq. (2.15), Eq. (2.16) and Eq. (2.17) with respect to equivalent variable, the governing equations can be derived for the three domain. The equivalent variable for the mechanical domain is the plate deflection, w_0 resulting in a force F. For the electrical domain the equivalent variable is the voltage V resulting in an expression for the system charge Q, and finally, for the acoustical domain the equivalent variable is the pressure p, resulting in the volume displacement W. The three derived equations are

$$F = \frac{\partial U_{\mathrm{t,m}}}{\partial w_0} = K_0 w_0 + m_0\frac{\partial^2 w_0}{\partial t^2} - \frac{1}{2}V^2\frac{\partial C(w_0)}{\partial w_0} - pA, \tag{2.18}$$

$$Q = \frac{\partial U_{\mathrm{t,e}}}{\partial V} = VC(w_0), \tag{2.19}$$

$$W = \frac{\partial U_{\mathrm{t,a}}}{\partial p} = w_0 A. \tag{2.20}$$

In combination these three equations provides a nonlinear description of the behavior of the transducer, which will be used in the following to derive the pull-in voltage and the pull-in distance [56]. Notice, that the partial derivative of the capacitance with respect to w_0 will be denoted $C'(w_0)$.

Based on the energy considerations above, the stable position of the capacitor plate can be found, hence the pull-in voltage and distance is derived. The stable position occurs when the spring force of the plate is balanced by the electrostatic force and the pressure applied to the plate. Considering the mechanical force acting on the CMUT the static case becomes

$$F_\mathrm{s} = K_0 w_0 - \frac{1}{2} V^2 C'(w_0) - pA. \tag{2.21}$$

The stable position is found for a given potential when the total force is zero by solving

$$K_0 w_0 = \frac{1}{2} V^2 C'(w_0) + pA. \tag{2.22}$$

By differentiating the total force with respect to the center deflection, w_0, the effective spring constant is found to be

$$K_\mathrm{eff} = \frac{\partial F_\mathrm{s}}{\partial w_0} = K_0 - \frac{1}{2} V^2 C''(w_0). \tag{2.23}$$

This expression shows the "spring softening" effect of the plate, namely the reduction in the spring constant caused by an applied voltage, which is subtracted from the isolated spring constant of the plate, K_0.

The pull-in voltage defines the point where the effective spring constant is zero, hence

$$V_\mathrm{pi} = \sqrt{\frac{2K_0}{C''(w_0)}}. \tag{2.24}$$

Combining Eq. (2.22) and Eq. (2.24), the center deflection when applying the pull-in voltage, known as the pull-in distance, can be calculated by solving

$$K_0 w_{0,\mathrm{pi}} = K_0 \frac{C'(w_{0,\mathrm{pi}})}{C''(w_{0,\mathrm{pi}})} + pA. \tag{2.25}$$

For the circular plate with no applied pressure the relative pull-in distance becomes $\eta_\mathrm{pi,p0,circ} = 0.463$, hence the pull-in potential at this distance is found by combining the value $\eta_\mathrm{pi,p0,circ}$ and Eq. (2.22) leading to

$$V_\mathrm{pi,p0,circ} = \sqrt{\frac{89.4459 D_\mathrm{i} g_\mathrm{eff}^2}{a^2 C_0}}, \tag{2.26}$$

which is equivalent to

$$V_{\text{pi,p0,circ}} = \sqrt{89.4459 \frac{Y g_{\text{eff}}^3}{12\pi(1-\nu^2)\epsilon_0}} \frac{h^{3/2}}{a^2}. \tag{2.27}$$

It the observed that the pull-in voltage depends on the plate geometry and scales with $h^{3/2}/a^2$.

2.2 Resonance Frequency in Immersion

Since the application of the CMUTs developed during this Ph.D. project are intended for providing ultrasound imaging of the body's internal structures, the resonance frequency of the transducer in immersion is of great interest. However, the expression derived by Lamb [49] has limited validity for the plate aspect ratios required for high-resolution imaging demands.

Therefore, the objective of this section is to provide a more accurate analytic expression for the resonance frequency in immersion, covering small plate aspect ratios relevant for medical CMUTs employed for high-resolution imaging. Based on the equation of motion a novel expression for the resonance frequency in immersion is derived. The interaction between the plate and the surrounding medium is modeled using the radiation impedance. Due to the complexity of the complete radiation impedance expression, the resonance frequency can only be solved numerically. To overcome this challenge the radiation impedance is approximated using a Taylor expansion to validate the derivation method against Lamb's expression. Additionally, a Padé approximation is employed to extend the model towards small aspect ratios.

The study presented in this section is based on the research presented at the International Ultrasound Symposium (IUS) 2022 conference, which was subsequently published in a conference proceeding appended in Paper A. This section is extended new FEM data.

The resonance frequency for a single CMUT cell in vacuum without applied potential can simplest be described as a harmonic oscillator by

$$\omega_0 = \sqrt{\frac{K_0}{m_0}}. \tag{2.28}$$

From experiments it is know that the resonance frequency of a device decreases when submerged in water compared to the vacuum frequency. In relation to Eq. (2.28) this decrease can be though of as an added mass from the surrounding medium, which will move together with the vibrating plate. The sum of the geometric mass and the extra mass added by the medium is defined as the effective mass $m_{\text{eff}} = m_0 + \Delta m$.

The resonance frequency in water can then be written as

$$\omega_{\mathrm{r}} = \sqrt{\frac{K_0}{m_0 + \Delta m}}. \tag{2.29}$$

Combining Eq. (2.28) and Eq. (2.29) provides the ratio between the resonance frequency in immersion and in vacuum, which results in

$$\frac{\omega_{\mathrm{r}}}{\omega_0} = \frac{\sqrt{\frac{K_0}{m_0+\Delta m}}}{\sqrt{\frac{K_0}{m_0}}} = \sqrt{\frac{m_0 + \Delta m}{m_0}} = \frac{1}{\sqrt{1 + \frac{\Delta m}{m_0}}}. \tag{2.30}$$

The geometric mass of the plate is defined as $m_0 = \pi a^2 h \rho_{\mathrm{p}}$. The added mass from the medium is simplest though of as a column of water on top of the plate having the same radius as the plate and is thus written as

$$\Delta m = \pi a^2 h_{\mathrm{w}} \rho_{\mathrm{m}}, \tag{2.31}$$

where ρ_{m} is the density of the medium and h_{w} is the unknown height on the water column. Combining this with Eq. (2.30) leads to

$$\frac{\omega_{\mathrm{r}}}{\omega_0} = \frac{1}{\sqrt{1 + \frac{\pi a^2 h_{\mathrm{w}} \rho_{\mathrm{m}}}{\pi a^2 h \rho_{\mathrm{p}}}}} = \frac{1}{\sqrt{1 + \frac{h_{\mathrm{w}}}{h} \frac{\rho_{\mathrm{m}}}{\rho_{\mathrm{p}}}}}. \tag{2.32}$$

A heuristic way to define h_{w} is implemented as $h_{\mathrm{w}} = \Gamma a$, where Γ is a proportionality factor. The argument is that the added mass differs between different plate geometries, thus depends on one of the geometric parameters. However, the molecules of the medium is not expected to experience the thickness of the plate, but rather to be influenced by the radius of the plate. The ratio between the frequency in immersion and vacuum can then be written as

$$\frac{\omega_{\mathrm{r}}}{\omega_0} = \frac{1}{\sqrt{1 + \Gamma \frac{a}{h} \frac{\rho_{\mathrm{m}}}{\rho_{\mathrm{p}}}}}. \tag{2.33}$$

This expression takes on the same form as derived by Lamb for the center frequency of a clamped circular thin plate in immersion [49]. Lamb's expression is established as

$$\frac{\omega_{\mathrm{r}}}{\omega_0} = \frac{1}{\sqrt{1 + \Gamma_{\mathrm{Lamb}} \frac{a}{h} \frac{\rho_{\mathrm{m}}}{\rho_{\mathrm{p}}}}}, \tag{2.34}$$

where Γ_{Lamb} is known as the Non-dimensionalized Added Virtual Mass Incremental (NAVMI) factor [58]. The NAVMI factor is a dimensionless constant, which depends on the boundary conditions of the plate. For a clamped circular plate Lamb states a NAVMI value of $\Gamma_{\mathrm{Lamb}} = 0.6689$. However, the

Table 2.1: Various NAVMI factors found in the literature.

	Lamb	**Powell**	**Kwak**
NAVMI value	0.6689	0.546	0.4667/0.65381
Reference	[49]	[59]	[58]/[60]

resonance frequency of a circular plate has been investigated by several researchers and even though the final expression has the same form, the value of the NAVMI factor varies dependent on the scientist. A few examples are provided with references in Table 2.1.

The model by Lamb assumes that the diameter of the plate is much smaller than the wavelength in the medium, corresponding to $ka \ll 2\pi$, with k being the wavenumber and a the radius of the plate. The expression in Eq. (2.34) is implicitly valid for $ka \leq 0.5$ since the expression is based on some simplification, that will be apparent later in this section. In literature the ka values for CMUTs ranges from 0.3 to 0.6 [16, 33] and with recent interest of $\lambda/2$-pitch designed CMUTs [22], the ka product increases up to 1.35 [61]. This reveals the demand for a more accurate analytical solution valid for larger ka, hence for smaller aspect ratios.

2.2.1 The Harmonic Oscillator Model

To derive an expression for the resonance frequency in immersion valid for devices with large ka, the clamped circular plate is mapped onto a concentrated element harmonic oscillator, which has the equation of motion

$$F_{\text{ext}} = m_0 \frac{d^2x}{dt^2} + K_0 x + F_{\text{w}}. \tag{2.35}$$

F_{ext} is the total external force on the plate, x the deflection and d^2x/dt^2 the acceleration. K_0 is given by Eq. (2.28) and F_{w} is the force from the fluid acting on the CMUT. This force can most simple be described in the frequency domain by introducing the radiation impedance, Z. The force can be expressed as $\hat{F}_{\text{w}} = Z\hat{v}_{\text{a}}$, where $\hat{v}_{\text{a}}$ is the plate velocity. Combining this with Eq. (2.35), the equation of motion becomes

$$\hat{F}_{\text{ext}} = -m_0\omega^2\hat{x}_{\text{m}} + K_0\hat{x}_{\text{m}} + iZ\omega\hat{x}_{\text{a}}. \tag{2.36}$$

$\hat{F}_{\text{ext}}$ and $\hat{x}$ refers to the force and position in the frequency domain, respectively, which are both complex numbers. The subscripts, m and a, refer to the mechanical and acoustical domain, respectively. In order to couple between the two domains a scaling factor $\Lambda = \hat{x}_{\text{a}}/\hat{x}_{\text{m}}$ is required. This is introduced through a lumped model. Rewriting the equation of motion in

Eq. (2.36) leads to an equation of motion in the mechanical domain, which yields

$$\hat{F}_{\text{ext}} = -m_0\omega^2\hat{x}_{\text{m}} + K_0\hat{x}_{\text{m}} + iZ\omega\Lambda\hat{x}_{\text{m}}. \tag{2.37}$$

From this expression the resonance frequency in immersion can be calculated, since resonance occurs when the real part of Eq. (2.37) equals zero, hence

$$0 = m_0(\omega_0^2 - \omega_{\text{r}}^2) - \Im(Z)\Lambda\omega_{\text{r}}. \tag{2.38}$$

This equation reveals the need to determine the radiation impedance of the clamped circular plate, which will be further described in the following subsection.

In order to couple between the mechanical and the acoustical domain a lumped model is now introduced. Recall, the static deflection curve for a circular clamped plate is defined by Eq. (2.3).

Considering the mechanical domain, the kinetic energy for a harmonic vibrating top plate is found by integration. The dynamic velocity at distance r is defined as

$$\hat{v}(r,t) = i\omega w(r)e^{i\omega t}. \tag{2.39}$$

The peak kinetic energy is

$$U_{\text{kin}} = \int_0^a \frac{1}{2}\omega^2 w^2(r)\rho_{\text{p}}h\,2\pi r dr = \frac{1}{2}m_0\left(\frac{\omega w_0}{\sqrt{5}}\right)^2. \tag{2.40}$$

The lumped velocity amplitude can subsequently be identified as $v_{\text{m}} = \omega w_0/\sqrt{5}$, which corresponds to a lumped position amplitude of $x_{\text{m}} = w_0/\sqrt{5}$. At the same lumped position the elastic potential peak energy can be identified as

$$U_{\text{ela}} = \frac{1}{2}K_0 x_{\text{m}}^2 = \frac{1}{2}m_0\omega_0^2 x_{\text{m}}^2 \tag{2.41}$$

such that $K_0 = m_0\omega_0^2$ by definition.

When submerged in a medium the CMUT radiates sound and the radiation impedance is defined as a complex number $Z = R + iX$, where the real part describes the radiated power, while the imaginary part describes the "back action" on the transducer. The radiation impedance is calculated based on the volume velocity, V, of the radiating CMUT plate. The volume velocity is given by

$$V = \int_0^a \omega w(r)\,2\pi r dr = \pi a^2\omega\,\frac{w_0}{3}. \tag{2.42}$$

The harmonic position relevant in the acoustical domain is therefore defined as $\hat{x}_{\text{a}} = (w_0/3)e^{i\omega t}$.

In summary, the lumped position amplitudes are $x_{\text{m}} = w_0/\sqrt{5}$ and $x_{\text{a}} = w_0/3$ for the mechanical and acoustical domains, respectively. The scaling

factor linking the mechanical and acoustical domain becomes

$$\Lambda = \frac{x_{\mathrm{a}}}{x_{\mathrm{m}}} = \frac{\sqrt{5}}{3} = 0.745, \tag{2.43}$$

which can be used for both the position and the velocity based on the harmonic assumption. Using this scaling parameter, the resonance frequency can be calculated from Eq. (2.38), when the radiation impedance is known.

2.2.2 Radiation Impedance

As previously stated, the radiation impedance is a complex number that characterizes both the radiated power and the "back action" on the transducer. For a clamped circular plate the radiation impedance is derived in [62] and expressed in terms of a hypergeometric function, ${}_2F_3$, the expression is

$$\begin{aligned} Z_{\mathrm{plate}} = \Bigg(& \frac{1}{(ka)^5}\big(12(-3+2(ka)^2)J_1(2ka) + ka(36+(ka)^4 - 84J_2(2ka))\big) \\ & + i\frac{512ka}{175\pi}\,{}_2F_3\left(2, \frac{5}{2}; \frac{3}{2}, \frac{7}{2}, \frac{9}{2}; -(ka)^2\right)\Bigg)\rho_{\mathrm{m}}c_{\mathrm{m}}\pi a^2, \end{aligned} \tag{2.44}$$

where J_1 and J_2 are Bessel functions of first and second order. The exact normalized radiation impedance is shown in Fig. 2.2a for the real and the imaginary part. The normalized radiation impedance is plotted as function of ka, which is the wavenumber-radius product. For large ka values the radiation resistance approaches the constant used for normalization; $\rho_{\mathrm{m}}c_{\mathrm{m}}\pi a^2$, while the radiation reactance asymptotic approaches zero.

Combining Eq. (2.38) and Eq. (2.44) the resonance frequency can be solved numerically for any CMUT design. However, to obtain an analytical expression for the resonance frequency in immersion an approximation for the radiation impedance is required. For small ka products the Taylor expansion of Eq. (2.44) can be used. The real part then results in

$$\Re(Z_{\mathrm{Taylor}}) = \frac{1}{2}a^2c_{\mathrm{m}}(ka)^2\pi\rho_{\mathrm{m}} + O(ka)^3, \tag{2.45}$$

while the imaginary part can be approximated by

$$\Im(Z_{\mathrm{Taylor}}) = \frac{512}{175}a^2c_{\mathrm{m}}ka\rho_{\mathrm{m}} + O(ka)^3. \tag{2.46}$$

Notice, that the reactance is linear for small ka values, while the resistance is parabolic. The results are shown in Fig. 2.2b together with the full expression for the radiation impedance. It is seen that the approximation

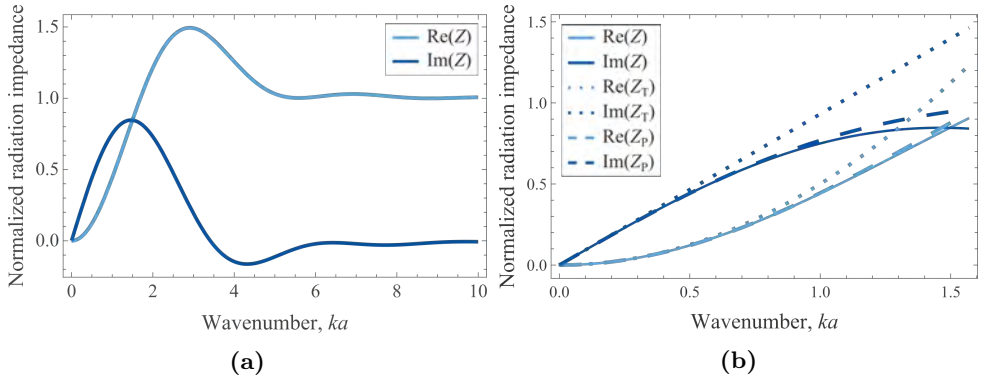


Figure 2.2: (a) The normalized radiation impedance provided in Eq. (2.44) showing the real and imaginary part in a large interval for the wavenumber-radius product, ka. (b) The full expression for the radiation impedance depicted together with the Taylor and Padé approximations in the interval relevant for medical CMUTs.

is only valid for $ka < 0.4$ for the imaginary part and $ka < 0.5$ for the real part.

Due to increasing interest for $\lambda/2$-pitch transducers the ka product increases, which requires an alternative method valid for $ka > 0.5$. For this purpose the Padé approximant [63] is applied to the simplest order, hence (2,2), which is a rational function. Applying the Padé approximation to Eq. (2.44) the real part becomes

$$\Re(Z_{\text{Pade}}) = \frac{a^2 c_{\text{m}} (ka)^2 \pi \rho_{\text{m}}}{2\left(1 + \frac{(ka)^2}{8}\right)} + O(ka)^5, \tag{2.47}$$

and the imaginary part becomes

$$\Im(Z_{\text{Pade}}) = \frac{512 a^2 c_{\text{m}} ka \rho_{\text{m}}}{175\left(1 + \frac{40(ka)^2}{189}\right)} + O(ka)^5. \tag{2.48}$$

Notice, the results obtained using the Padé approximant are identical to the Taylor results multiplied by a correction factor. From Fig. 2.2b, it can be observed that the Padé approximation remains valid for $ka < 1.0$ for the imaginary part, and for $ka < 1.4$ for the real part. The maximum error between the exact solution and the second-order Taylor expansion at $ka = 1.0$ is 24 %, whereas the maximum error for the simplest Padé approximant is 2.5 %. Consequently, the Padé approximation offers a better approximation of the normalized radiation impedance compared to the Taylor expansion when $ka > 0.4$. An additional advantage of the Padé approximant is that it is physically accurate, which implies that when the value of ka becomes large, its real part tends to a constant value, while its imaginary part converges to zero in a similar manner as the full expression of the radiation

impedance. In comparison the Taylor expansion will always, regardless of the approximation order, diverge to either positive or negative infinity for large ka values, which is not physically correct.

By simplifying the radiation impedance using the Padé approximation, it becomes possible to derive a more straightforward analytical formula for the resonance frequency of a CMUT in immersion compared to the full numerical solution. Furthermore, a wider range of ka values are covered compared to the Taylor expansion and the original expression derived by Lamb.

2.2.3 Resulting Resonance Frequency in Immersion

To verify the derivation method applying the harmonic oscillator model together with the radiation impedance, the Taylor expansion of the imaginary part of the radiation impedance provided in Eq. (2.46) is combined with Eq. (2.38), which leads to

$$0 = m_0(\omega_0^2 - \omega_\mathrm{r}^2) - \frac{512}{175} a^2 c_\mathrm{m}\, ka \rho_\mathrm{m} \Lambda\, \omega_\mathrm{r}, \tag{2.49}$$

$$0 = 1 - \frac{\omega_\mathrm{r}^2}{\omega_0^2}\left(1 + \Gamma_\mathrm{Taylor} \frac{a}{h}\frac{\rho_\mathrm{m}}{\rho_\mathrm{p}}\right). \tag{2.50}$$

It is employed that $k = \omega_\mathrm{r}/c_\mathrm{m}$. The ratio between the resonance frequency in immersion and vacuum becomes

$$\frac{\omega_\mathrm{r}}{\omega_0} = \frac{1}{\sqrt{1 + \Gamma_\mathrm{Taylor}\frac{a}{h}\frac{\rho_\mathrm{m}}{\rho_\mathrm{p}}}}. \tag{2.51}$$

Here $\Gamma_\mathrm{Taylor} = \frac{512}{175\pi}\Lambda$ is the NAVMI factor. This equation has the same form as the well-known expression provided in Eq. (2.34). However, the NAVMI factor deviates slightly with $\Gamma_\mathrm{Taylor} = 0.6941$ being a little higher compared to Lamb's value of $\Gamma_\mathrm{Lamb} = 0.6689$. This verifies the derivation method using the lumped equation of motion together with an approximation of the radiation impedance.

In order to cover a wider range of ka values relevant for medical CMUTs, the imaginary Padé approximation in Eq. (2.48) is employed as the radiation impedance. Solving Eq. (2.38) for the resonance frequency in immersion leads to

$$0 = 1 - \frac{\omega_\mathrm{r}^2}{\omega_0^2}\left(1 + \Lambda \frac{\Im(Z_\mathrm{Padé})}{m_0 \omega_\mathrm{r}}\right), \tag{2.52}$$

$$0 = 1 - \frac{\omega_\mathrm{r}^2}{\omega_0^2}\left(1 + \Gamma_\mathrm{Taylor}\frac{a}{h}\frac{\rho_\mathrm{m}}{\rho_\mathrm{p}}\frac{1}{1 + \frac{40(ka)^2}{189}}\right). \tag{2.53}$$

Using that $k_0 = \omega_0/c_\mathrm{m}$ and rearranging, the expression results in

$$0 = 1 - \frac{\omega_\mathrm{r}^2}{\omega_0^2}\left(1 + \Gamma_\mathrm{Taylor}\frac{a}{h}\frac{\rho_\mathrm{m}}{\rho_\mathrm{p}}\frac{1}{1 + \frac{40(k_0a)^2\left(\frac{\omega_\mathrm{r}}{\omega_0}\right)^2}{189}}\right), \tag{2.54}$$

$$0 = 1 - \left(\frac{\omega_\mathrm{r}}{\omega_0}\right)^2\left(1 + \Gamma_\mathrm{Taylor}\frac{a}{h}\frac{\rho_\mathrm{m}}{\rho_\mathrm{p}} - \frac{40(k_0a)^2}{189}\right) - \frac{40(k_0a)^2}{189}\left(\frac{\omega_\mathrm{r}}{\omega_0}\right)^4. \tag{2.55}$$

This is recognized as the form of a second order equation with a known solution, hence the resonance frequency in immersion using the Padé approximation yields

$$\frac{\omega_r^2}{\omega_0^2} = -\frac{c_1 + \sqrt{c_1^2 + 4c_2}}{2c_2}, \tag{2.56}$$

with

$$c_1 = 1 + \Gamma_\mathrm{Taylor}\frac{a\rho_\mathrm{m}}{h\rho_\mathrm{p}} - c_2, \tag{2.57}$$

$$c_2 = \frac{40\,(k_0a)^2}{189} = \frac{40\,(\omega_0 a/c_\mathrm{m})^2}{189}. \tag{2.58}$$

This relatively simple expression can be utilized to determine the resonance frequency in immersion for CMUTs with larger ka values, exceeding the ka range covered by Lamb's expression.

2.2.4 FEM Analysis

To validate the derived expression, FEM simulations were conducted using the COMSOL Multiphysics software. The simulated structure represents a simple single CMUT cell, as depicted in Fig. 2.3. The structure comprises a fixed bottom silicon substrate and a flexible silicon top plate, separated by a vacuum gap. The thickness of the top plate was defined to be $h = 2\,\mu\mathrm{m}$, while the radius were varied to cover a large range of plate aspect ratios. The vacuum gap height was fixed at $80\,\mu\mathrm{m}$ since it has no influence on the unbiased resonance frequency. In the bonding region an intermediate layer of an insulating oxide is located. The structure was vertically clamped in the boundary between the cavity and the bonding region, which is shown with a solid black line in the illustration. The applied material parameters are provided in Table 2.2. Furthermore, the simulations were conducted with an interchangeable surrounding medium of either air or water. The medium had an absorbing boundary defined away from the CMUT structure in order to avoid undesired reflections. This is illustrated by a solid line. The dashed line indicates the axis of rotational symmetry in the structure. The simulations conducted in air were performed without any applied bias determining

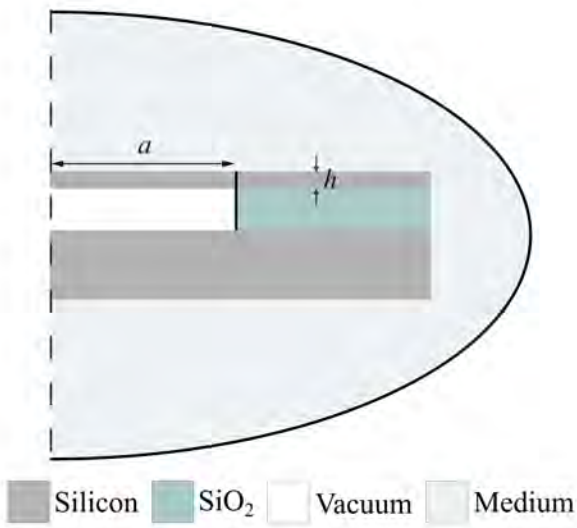


Figure 2.3: Structural outline of a simple 2D CMUT model used in the FEM simulation of the resonance frequency in vacuum and immersion. The structure comprises two silicon plates with a vacuum gap in-between. The fixed boundary is marked as well as the absorbing boundary at the far end of the medium. Additionally, the axis of rotational symmetry is represented by a dashed line.

the eigenfrequency of the structure. However, for the simulations in water, a DC potential of 0.1 V was applied. This value was chosen to prevent any noticeable frequency drift caused by spring softening effects.

The results obtained from the FEM simulations are shown in Fig. 2.4, were they are compared with the well-known Lamb model, the model derived using a Taylor expansion of the radiation impedance and the model derive based on the Padé approximation of the radiation impedance. Additionally, the full numerical solution was included for comparison.

The results are presented as function of the plate aspect ratio a/h. As expected from Eq. (2.51), the Taylor-based solution closely follows the ex-

Table 2.2: Material parameters for silicon and oxide applied in the COMSOL simulations.

Parameter	**Value**	
	Si	SiO_2
Young's modulus, Y [GPa]	148	70
Poisson's ratio, ν	0.177	0.177
Density, ρ [kg/m^3]	2328	2200

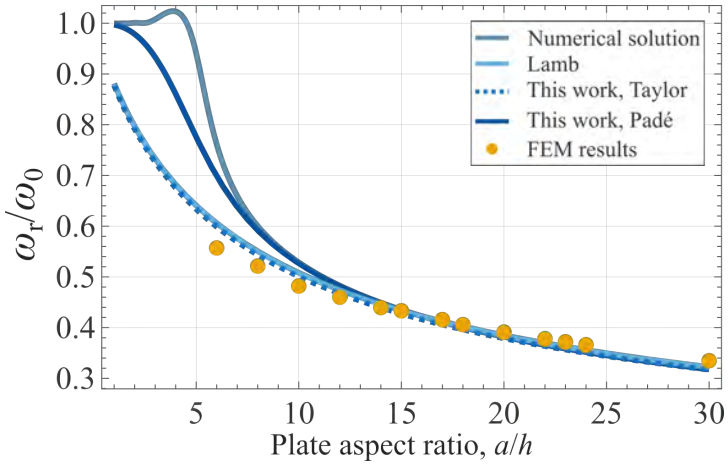


Figure 2.4: The analytical solution by Lamb presented together with the solutions derived using the Taylor and Padé approximations as alternative to the radiation impedance. Furthermore, FEM data are included together with the full numerical solution.

pression provided by Lamb. However, for plate aspect ratios smaller than approximately 13, the models start to deviate from exact numerical solution. For the Padé-based solution, it is evident that it exhibit a greater accuracy over a wider range of plate aspect ratios compared to Lamb's expression. The deviation between the numerical model and the Padé solution starts at approximately $a/h = 8$, which is equivalent with the Padé approximation being more accurate for larger ka values. However, considering the FEM data, a deviation to the models is observed as the aspect ratio is decreased. For $a/h = 20$, the deviation to the Padé model was calculated to $-2.4\,\%$, while the deviation from the Taylor-based solution was $-3.2\,\%$. For a thicker plate with an aspect ratio of $a/h = 10$, the deviation to the Padé model increased to $8.5\,\%$, while the deviation to the Taylor-based solution was $3.8\,\%$.

This discrepancy indicates the need to incorporate additional effects in the model. Notably, thick plates exhibit diverging plate bending behavior compared to thin plates caused by shear effects. Therefore, the observed deviation can be partially attributed to the thin plate assumption, which neglects shear effects in the plate. These effects become increasingly significant for aspect ratios below 10. It should be noted that no definite boundary exist between thick and thin plates, hence an intermediate area of moderately thick plates have also been defined and investigated in literature [64–66]. Consequently, further investigation into shear effects on various plate geometries will be explored in Section 2.4.

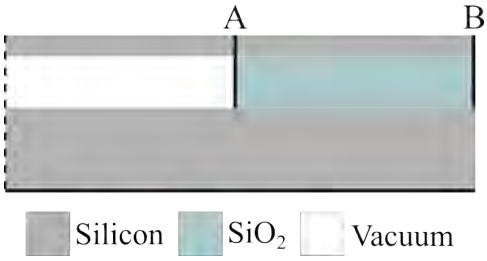


Figure 2.5: Illustration of the simple structure simulated in COMSOL. The structure is based on a flexible silicon top plate and a fixed silicon bottom substrate with an intermediate vacuum gap in the center of the structure and an insulating oxide in the bond region. The fixed boundaries are indicated by black lines and the dashed line shows the axis of symmetry. The material parameters used for silicon is also included.

2.3 Effective Radius Theory

As earlier described, the plate deflection, resonance frequency and the pull-in voltage are some of the key parameters for CMUTs. Considering the analytical solutions for a circular plate derived in Section 2.1, it was assumed that the plate was clamped at the periphery of the cavity, corresponding to the inner edge of the bonding region defined in Fig. 2.1. However, real plates possess elastic boundaries [67,68]. Commonly applied clamping assumptions does not account for the stress distribution in the bonding region, caused by the elastic boundary conditions.

Ryan et.al. demonstrated in [69] that it is possible to incorporate bending, shear deformation, and extensional deformations in the bonding region by application of a modified beam theory. In the work by Hu et.al. [70], a clamped circular plate subjected to a uniform load was modeled. The deflection was corrected by considering three terms: rotational displacement, shear deformation, and lateral pressure.

In 2020 an experimental study performed within this research group [71], demonstrated that the pull-in voltage depended on the clamping conditions of the plate, indicating that stresses in the support region could not be ignored. Therefore, an effective radius theory is proposed. This theory incorporates the stress distribution in the support region into existing analytical expressions and is validated using data generated with the COMSOL Multiphysics software. The optimized analytical theory can be utilized to determine initial design parameters of the CMUTs and serves as a faster alternative to time-consuming FEM simulations.

Since CMUTs are clamped to a supporting structure rather than clamped in a single point, stresses are distributed into the support region which results in a softer plate. The effective radius theory allows the analytical model to include elastic clamping conditions similar to the ones used in

FEM simulation, which is illustrated by point B in Fig. 2.5.

In this heuristic model, the conventional analytic plate radius, denoted a, is replaced by an effective radius defined as

$$a_{\text{eff}} = a + \mathcal{C}h, \tag{2.59}$$

where h is the plate thickness and $\mathcal{C}$ represents a non-dimensional parameter obtained from FEM analysis, dependent on the geometry of the clamped point.

The study presented in this section was partly presented at the IUS 2021 conference, and is a further development of the work presented in [68]. Currently, a publication related to this work is in writing. The analysis will be performed for the plate deflection, the resonance frequency in vacuum and the pull-in voltage.

2.3.1 FEM Model

In order to verify the heuristic proposed model, FEM simulations were performed. These were generated using COMSOL. A simple model was built consisting of a flexible top plate separated from a rigid bottom substrate by an intermediate vacuum gap. A insulating oxide separates the conducting plate from the substrate in the bonding region. A cross-sectional view of the structure is presented in Fig. 2.5. The thickness of the top plate was kept constant at $h = 2\,\mu\text{m}$, while the radius was varied from $20\,\mu\text{m}$ to $200\,\mu\text{m}$, allowing for examination of different plate geometries.

The axis of symmetry is emphasized with a dashed line in the figure and the structure is clamped horizontally at the bottom of the substrate marked with a solid line. According to the vertical clamping of the structure, the simulations were generated by initially clamping the structure at the inner boundary (point A), and subsequently at the outer boundary (point B). This have been accomplished for both the plate deflection, the resonance frequency and the pull-in voltage. All simulations were conducted using vacuum as surrounding medium. The gap height was maintained at constant value of 400 nm. In the deflection simulations, a uniform load of $p = 1 \times 10^3\,\text{Pa}$ was applied to the top plate. Prior to starting the simulations the mesh was optimized in a mesh convergence study.

2.3.2 Plate deflection

In Subsection 2.1.1 the well-known center deflection from classical plate theory was described by Eq. (2.4), which assumed clamping on the cavity periphery. By replacing the radius, a, with the proposed effective radius from Eq. (2.59), the plate deflection utilizing elastic boundary conditions becomes

$$w_{0,\text{elastic}} = w_0(a_{\text{eff}}) = \frac{p(a + \mathcal{C}h)^4}{64D_i}. \tag{2.60}$$

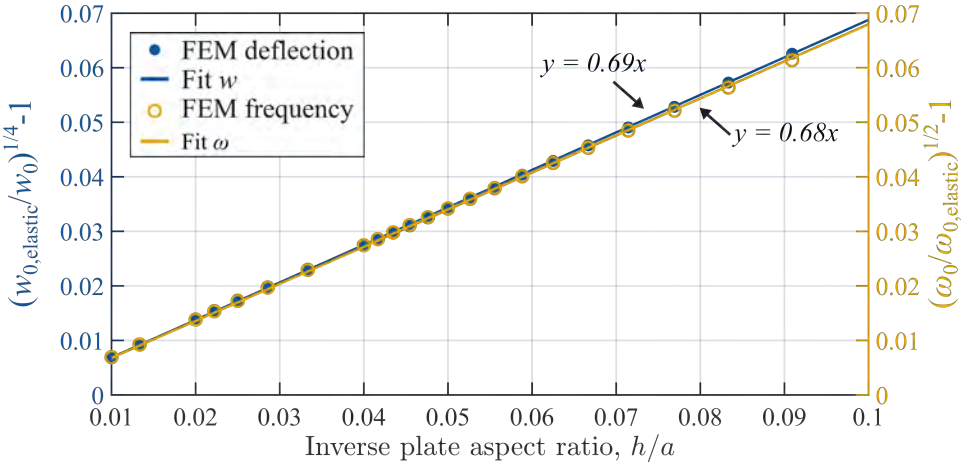


Figure 2.6: FEM data for the plate deflection (left) and the resonance frequency (right) relative to the inverse aspect ratio. The linear tendency expected from Eq. (2.61) is validated by both datasets and $\mathcal{C}$ was found to be 0.69 for the plate deflection and 0.68 for the frequency.

To determine the non-dimensional parameter $\mathcal{C}$, the ratio between the clamped and elastic center deflection was derived

$$\sqrt[4]{\frac{w_{0,\text{elastic}}}{w_0}} = \frac{a + \mathcal{C}h}{a} = 1 + \mathcal{C}\frac{h}{a}. \tag{2.61}$$

This relation is depicted in Fig. 2.6 on the left y-axis together with the obtained simulated data. Employing a linear regression shows a $\mathcal{C}$-value of 0.69, which is slightly higher than the value derived in [68].

2.3.3 Resonance Frequency in Vacuum

Considering the resonance frequency in vacuum, the equation for a clamped plate was provided in Eq. (2.5). Employing the heuristic effective radius to account for elastic clamping of the plate, the expression for angular resonance frequency results in

$$\omega_{0,\text{elastic}} = \omega_0(a_{\text{eff}}) = 10.2158\sqrt{\frac{D_i}{h\rho_p}\frac{1}{(a + \mathcal{C}h)^2}}. \tag{2.62}$$

The ratio between Eq. (2.5) and Eq. (2.62) can then be reduced to

$$\sqrt{\frac{\omega_0}{\omega_{0,\text{elastic}}}} = \frac{a + \mathcal{C}h}{a} = 1 + \mathcal{C} \cdot \frac{h}{a}. \tag{2.63}$$

This shows that the square root of the ratio between the results obtained with clamped and elastic applied boundary condition for a thin plate with

zero applied bias, exhibits a linear relationship with the inverse aspect ratio (h/a).

The right axis in Fig. 2.6 presents the FEM data along with the expression derived in Eq. (2.63). The constant $\mathcal{C}$ was determined to be 0.68.

2.3.4 Pull-in Voltage

The last parameter investigated with respect to the applied boundary conditions was the pull-in voltage. Based on electrostatic analysis the pull-in voltage for a clamped circular plate was derived in Eq. (2.27). Combined with the effective radius theory, the pull-in voltage with elastic clamping conditions results in

$$V_{\text{pi,elastic}} = V_{\text{pi,p0,circ}}(a_{\text{eff}}) = \sqrt{\frac{89.4459 D_{\text{i}} g_{\text{eff}}^2}{C_0} \frac{1}{(a + \mathcal{C}h)^2}}. \tag{2.64}$$

The ratio between the pull-in voltage for a clamped and an elastic plate reduces to

$$\sqrt{\frac{V_{\text{pi,p0,circ}}}{V_{\text{pi,elastic}}}} = \frac{(a + \mathcal{C} \cdot h)}{a} = 1 + \mathcal{C} \cdot \frac{h}{a}, \tag{2.65}$$

which is very similar for the expression derived for the resonance frequency shown in Eq. (2.63). To determine the fitting parameter $\mathcal{C}$, the relation derived in Eq. (2.65) was fitted to FEM-generated data. The vacuum gap height was kept constant for the various geometries. This is possible since the focus is on the ratio between $V_{\text{pi}}(a)$ and $V_{\text{pi}}(a_{\text{eff}})$, rather than the individual pull-in voltages. Furthermore, no pressure was applied to the top plate.

The results of the simulations with varying plate aspect ratio are depicted in Fig. 2.7. The linear regression analysis yielded a value of $\mathcal{C} = 0.67$ for the fitting parameter, which aligns well with the results obtained for the plate deflection and the resonance frequency.

In this section, a new heuristic analytical model has been proposed, introducing an effective radius into well-known expressions for the center deflection of the plate, the resonance frequency in vacuum, and the pull-in voltage. The effective radius depends on the dimensions of the CMUT plate and a fitting parameter $\mathcal{C}$, which was determine to approximately 0.68 based on FEM analysis with two different applied clamping conditions. This concludes that the $\mathcal{C}$ parameter can be determined from different methodologies, yielding the similar results for a specific geometry at the clamping point.

The simulations conducted in this section focused on h/a ratios ranging from 0.01 to 0.1, which corresponds to the regime defined as the thin plate regime by [72]. As the values increase, other effects become more prominent. Considering that the previously fabricated probes in this research group

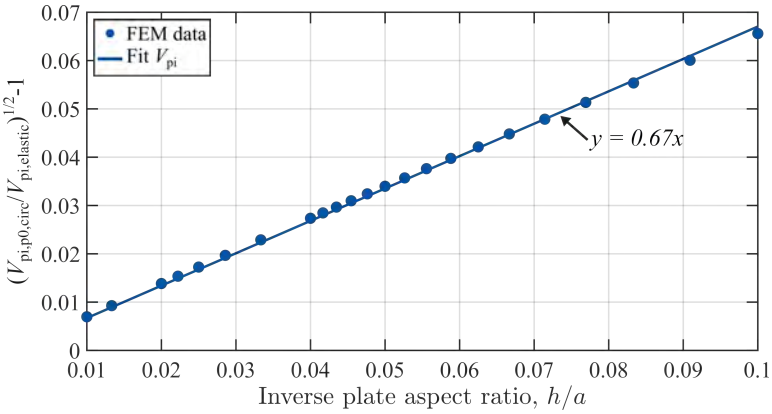


Figure 2.7: Simulation results for the pull-in voltage relative to the inverse aspect ratio, h/a. Eq. (2.65) is fitted to the data resulting in $c = 0.68$.

have inverse plate aspect ratios up to 0.2, it becomes necessary to extend the theory into the thick plate regime, which will be further explored in the following section.

2.4 Shear Effects on Plates

The fundamental properties of CMUTs are often described using Classical Plate Theory (CPT), which is applicable to plates with large aspect ratios typically defined as a/h greater than 10. However, these expressions do not account for transverse shear deformation. With the increasing interest in high-frequency CMUTs and a decreasing pitch size [22], the aspect ratio of the CMUT decreases, resulting in plates with aspect ratios of a/h smaller than 10, also referred to as thick plates.

In [69] the deformation of a bridge structure with a two-sided fixed constraint was modeled incorporating both shear deformation and rotational compliance. It was demonstrated that for $L/h = 10$, where L is the length of the beam, the effect of shear deformation was 12.2 %, while the rotational compliance had an effect of 14.4 %. However, for beams with a smaller aspect ratio of $L/h = 5$, the shear deformation became mode dominant with 51 % correction compared to the the rotational stiffness having an effect of 28 %.

To emphasize the relevance of this study, previously fabricated CMUT-based transducers from various research groups were considered. Examples of publications on what is commonly referred to as thin plate transducers includes [33, 73, 74], which demonstrates plate aspect ratios ranging from 20 to 400. In [36], Park et.al. fabricated two arrays, one with an aspect ratio of 40 and another in the intermediate range between thick and thin plates, with an aspect ratio of 12. CMUTs with even smaller plate aspect ratios

were successfully fabricated and published in [16, 20, 75], presenting designs with plate aspect ratios ranging from 9.9 to 3.04. The central CMUT design, which was developed and fabricated as part of this Ph.D. project, had a plate aspect ratio of 4.96. Therefore, significant interest in studying how the ratio of the plate dimensions affects the key parameters of the transducer exists.

The objective of the work elaborated in this section is to investigate the validity of the existing CPT expressions for key parameters of CMUTs using FEM simulations. The research has been accepted for a poster presentation at the IUS 2023 conference and is intended for a publication during fall.

The study in this section primarily relies on FEM simulations, applying a model similar to the one described in Subsection 2.2.4. The simulations encompassed plate aspect ratios spanning both the thin and thick plate regimes, achieved by varying the radius a from 8 µm to 250 µm, while maintaining a constant plate thickness of $h = 2\,\mu\text{m}$. The results were compared against established CPT expressions for the plate center deflection, the resonance frequency in vacuum and immersion. Furthermore, the pull-in voltage and distance were investigated. In order to compare the simulated results against well-established analytical expressions, the plate was clamped at the periphery of the vacuum cavity.

2.4.1 Plate Deflection and Resonance Frequency

Initially, two plates with different aspect ratios were simulated, and the resulting deflection profiles are visualized together with the expression without shear effects according to CPT (Eq. (2.3)) as presented in Fig. 2.8. Stationary simulations were performed for each plate radius, with a constant uniform boundary load on the top plate of $p = 1 \times 10^3\,\text{Pa}$ and an ambient medium of air. To prevent the top plate collapsing onto the bottom substrate, an adequately large gap height was chosen. Fig. 2.8a shows the result for a very thin plate with a radius of 200 µm and a thickness of 2 µmeter. Contrary, Fig. 2.8b depicts the result for a plate with a radius of 8 µm and a thickness of 2 µm. For the thin plate (Fig. 2.8a) it is observed that the analytical expression closely aligns with the simulated data throughout the entire radial position. However, for the thick plate (Fig. 2.8b), the deflection profile is consistently underestimated across the entire radial position. This clearly demonstrates the inadequacy of Eq. (2.3) as an approximation for thick plates, thus highlighting the necessity for an expanded expression that incorporates additional effects into the well-established CPT expression.

The full deflection profile of a moderately thick plate is known from the field of solid mechanics, where among others Love and Ike have derived similar expressions [72, 76]. The deflection of a plate, including the effect of shear deformation, is the sum of the deflection predicted by CPT (Eq. (2.3))

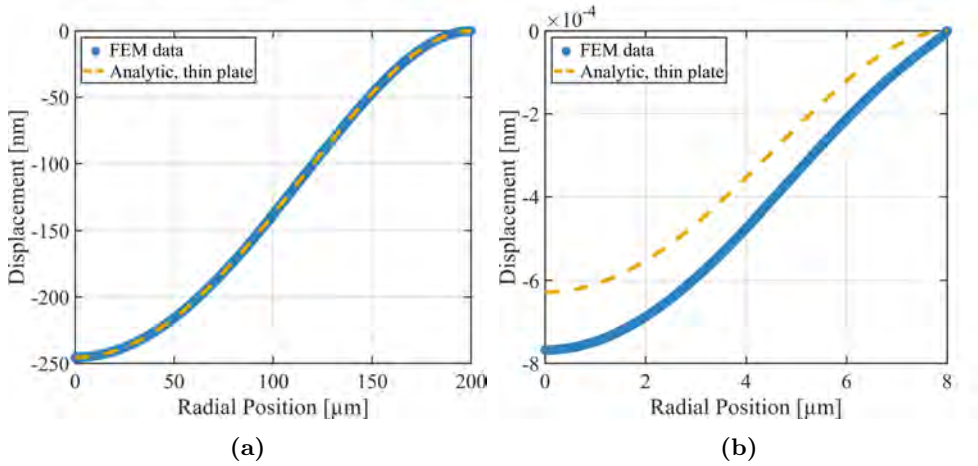


Figure 2.8: Deflection profile of (a) a very thin CMUT plate with $a = 200\,\mu\text{m}$ and (b) a thick CMUT plate with $a = 8\,\mu\text{m}$. The analytic expression without shear effect (Eq. (2.3)) is also included.

and a correction term accounting for shear stress. The precise deflection of an isotropic clamped circular plate is given by [68]

$$w(r) = w_{0,\text{thin}} \left(\left[1 - \left(\frac{r}{a}\right)^2 \right]^2 + \delta \left(\frac{h}{a}\right)^2 \left[1 - \left(\frac{r}{a}\right)^2 \right] \right). \tag{2.66}$$

Here δ represents a prefactor, which has different values in the literature and will be further discussed in the following. $w_{0,\text{thin}}$ represents the center deflection of a thin plate and is defined in Eq. (2.4). By setting $r = 0$, center deflection of a thick plate becomes

$$w_0 = w_{0,\text{thin}} \left(1 + \delta \left(\frac{h}{a}\right)^2 \right). \tag{2.67}$$

For small h/a (corresponding to large aspect ratios a/h), the second term in Eq. (2.67) can be neglected. However, for larger values of h/a (referred to as thick plates) this term becomes significant and increases the deflection beyond what is predicted by the thin plate model Therefore, the influence of shear deformation on the plate deflection cannot be ignored for such plates.

As mentioned, the value of the prefactor δ has been explored by various researchers, including Love, Ike, and Timoschenko [54, 72, 76]. The value depends on the applied boundary conditions, and the values derived by Love and Ike yields

$$\delta_{\text{Love}} = \frac{4}{1-\nu} = 4.86 \tag{2.68}$$

$$\delta_{\text{Ike}} = \frac{8}{3} \frac{1}{(1-\nu)} \frac{1}{\kappa} = 3.89. \tag{2.69}$$

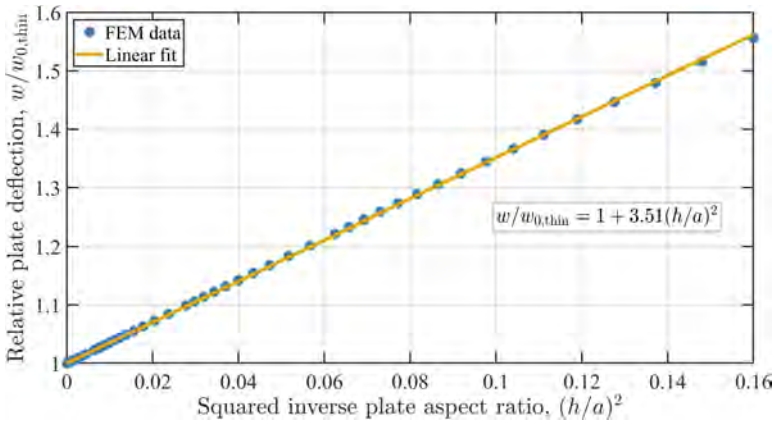


Figure 2.9: Linear relation between the relative plate deflection and the inverse aspect ratio squared as predicted by Eq. (2.67). The fitted δ_{FEM}-value was derived to be 3.51.

It is observed that δ_{Love} exclusively depends on Poisson's ratio, while δ_{Ike} also depends on the shear correction factor κ. The shear correction factor has also been introduced by Mindlin in the context of the flexural behavior of isotropic circular plates, which is known as the First order Shear Deformation Theory (FSDT). The shear correction factor depends on several factors including, the plate material, geometry, loading and boundary conditions, leading to different values reported in the literature [77,78]. The values used in the above calculations were $\nu = 0.177$ and $\kappa = 5/6$. It should be noted that the expression derived by Timoshenko has the same form as δ_{Ike}, but with $\kappa = 2/3$ instead of $\kappa = 5/6$, which then reduces to δ_{Love}.

Considering the variations in literature, it is of interest to determine the value of δ based on FEM simulations and compare the result to Eq. (2.68) and Eq. (2.69). This can be conducted based on Eq. (2.67), the relationship between $w_0/w_{0,\text{thin}}$ and the inverse aspect ratio squared ($(h/a)^2$) reveals a linear relation. Fitting this relationship to the simulated data yields a FEM-based prefactor of $\delta_{\text{FEM}} = 3.51$, as illustrated in Fig. 2.9. The FEM-based value is slightly lower than the one derived by Ike and 1.35 lower than the value derived by Love. These deviations can be partly attributed to the variations in the applied shear correction factor κ.

After determining the prefactor δ, the relative deviations were plotted for both the plate deflection and the resonance frequency in vacuum, as presented in Fig. 2.10. It should be noted that no external pressure was applied to the top plate during the simulations of the resonance frequency, and the vacuum gap height was kept constant at 400 nm. The simulation results were compared to the corresponding expressions from CPT without shear effects. The relative deviation for the center deflection was calculated

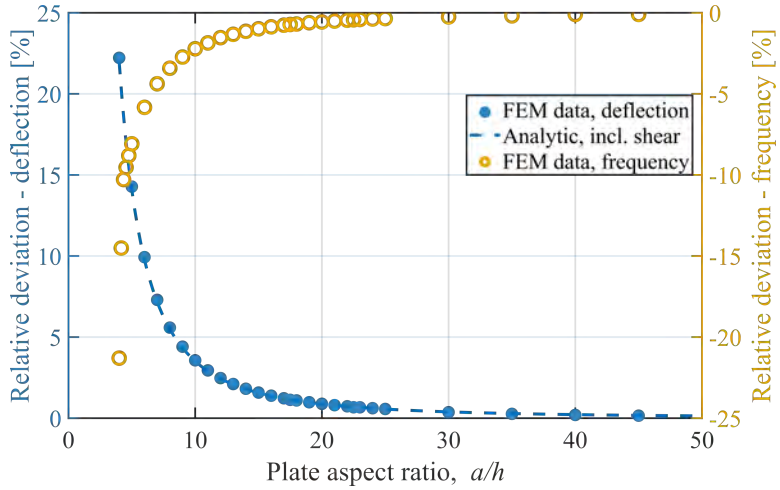


Figure 2.10: Relative deviation for FEM results compared to CPT expression for (left) the center deflection of the plate and (right) for the resonance frequency in air.

by

$$\text{Relative deviation } [\%] = \frac{w_{0,\text{FEM}} - w_{0,\text{thin}}}{w_{0,\text{thin}}} \times 100 \tag{2.70}$$

where $w_{0,\text{FEM}}$ represents the FEM results and $w_{0,\text{thin}}$ is calculated using Eq. (2.4). A similar method was employed for the resonance frequency in vacuum. Here the analytical expression was given by Eq. (2.5). Additionally, the figure also includes the analytical solution for the plate deflection that incorporates shear effects, using the FEM-based prefactor of 3.51.

The obtained results show that as the aspect ratio decreases and enters the thick plate regime, the shear effect has a significant impact on both the plate deflection and the resonance frequency. For an aspect ratio of $a/h = 10$, the plate deflection deviates with 3.6 %, while the resonance frequency deviates by -2.2 %. When the aspect ratio is further reduced to $a/h = 4$, the deviations are 22.2 % and -21.3 % for the plate deflection and the resonance frequency, respectively. However, incorporating shear deformation into the analytic plate deflection formula significantly reduces the error to only 0.21 % for $a/h = 4$. These results clearly indicate that shear effects cannot be neglected for CMUTs with thick plates.

In summary, it is evident that the effect of shear deformation on the plate bending cannot be neglected when the plate aspect ratio is reduced below 10. Furthermore, the shear effect showed a significant impact on the resonance frequency. In the following subsection, the shear effect will be investigated in relation to the pull-in voltage and pull-in distance.

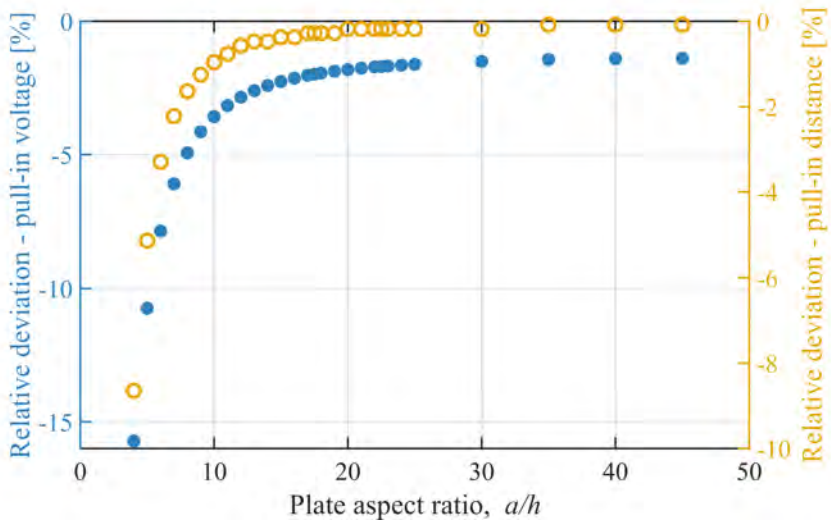


Figure 2.11: Relative deviation for FEM results compared to CPT expression for (left) the pull-in voltage and (right) the pull-in distance.

2.4.2 Pull-in Voltage and Distance

Similarly to the study on plate deflection and resonance frequency in air, investigations were conducted regarding the pull-in voltage and distance. The simulations were performed without external pressure, and the vacuum gap was maintained at a constant value of $g = 400\,\text{nm}$ for all geometries. An electric potential was applied to the bottom of the top plate, and the pull-in voltage and distance were determined by varying the applied voltage. The results, presented in Fig. 2.11, show the deviation in voltage relative to the theoretical expression derived in Eq. (2.27), and the pull-in distance relative to a constant value of $\eta_{\text{pi,p0,circ}} = 0.463$.

For large aspect ratios, a deviation is observed in the pull-in voltage. This deviation is caused by the inexactness of the theoretical expression derived in Eq. (2.27). During derivation of the analytical expression it was assumed that constant force across the cell was applied. However, this assumption becomes invalid as the plate bends under the influence of electrostatic forces. As a consequence, the force is higher at the center compared to the edges. Nevertheless, the deviation remains relatively small, with only 1.4 % for an aspect ratio of 45. In contrast, for small aspect ratios, a noticeable increase in relative deviation is observed. For $a/h = 4$, the deviation for the pull-in voltage is $-15.7\,\%$. On the other hand, the analysis of the pull-in distance indicates a negligible error for thin and moderately thick plates. However, for an aspect ratio of $a/h = 4$, the deviation becomes more significant with 8.6 %. It is worth noting that the CPT predicts a constant pull-in distance at $\eta_{\text{pi,p0,circ}} = 0.463$, regardless of the plate geometry.

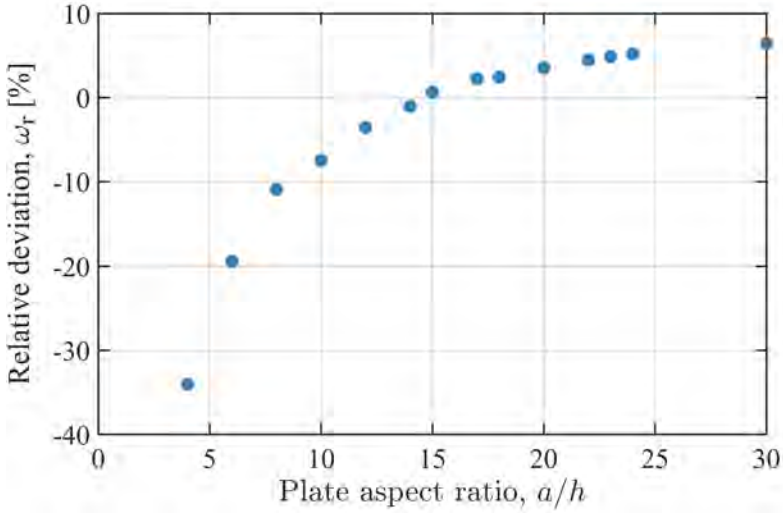


Figure 2.12: Relative deviation between FEM simulated resonance frequency in immersion and the analytical value based on the derived Padé-based solution in Eq. (2.56).

In summary, it is evident that shear effects play a crucial role in both the pull-in voltage and the pull-in distance, and therefore, cannot be disregarded.

2.4.3 Frequency in Immersion

Finally, the resonance frequency in immersion was investigated. The medium surrounding the structure was changed to water with an absorbing boundary far away from the cell to prevent reflections. The simulations were conducted without external load, and a small potential ($Vdc = 0.1\,\mathrm{V}$) was applied to the top plate. The frequency was varied within an interval around the expected resonance frequency, and the frequency was determined from the resulting plot.

The relative deviation of the frequency was calculated by comparing the FEM data to the analytical expression based on the Padé approximation (Eq. (2.56)). The Padé-based solution was selected because it closely matched the exact numerical solution (recall Fig. 2.4). The result for the resonance frequency in immersion presented in Fig. 2.12.

Upon analysis, it was observed that the analytical model underestimated the frequency for large plate aspect ratios, while a negative deviation was found for small aspect ratios. For an aspect ratio of $a/h = 4$, the relative deviation was 34 %, which is higher than the deviation observed for the resonance frequency in vacuum (recall $-21.3\,\%$ deviation for $a/h = 4$).

The findings from this simulation-based study highlight the importance of incorporating shear effects into analytical expressions for addressing CMUTs with high frequency and reduced pitch size. As the transducer design moves towards thicker plates, the impact of shear effects on the transducer behavior becomes more significant. Therefore, there is a growing need to develop analytical models that accurately account for these shear effects. Currently, such models are being further investigated to improve the understanding and analysis of CMUTs in these challenging design regimes.

2.5 Chapter Summary

This chapter provided a comprehensive analysis of crucial parameters for CMUTs. Initially, parameters such as plate deflection, eigenfrequency, capacitance, and pull-in voltage were derived based on the CPT.

The second section focused on deriving the resonance frequency in immersion by considering the equation of motion and radiation impedance. An approximation using a Taylor expansion of the radiation impedance was introduced for validation of the derivation method against Lamb's expression [49]. While this approximation resulted in a 24 % error for $ka = 1.0$, the proposed method applying a more accurate Padé approximant reduced the error to 2.5 %. These approximations were employed to derive an analytical expression for the resonance frequency in immersion. The derived expression exhibited good agreement with FEM data for large plate aspect ratios, but showed a deviation of 8.5 % for plates with aspect ratios below $a/h = 10$, highlighting the need to account for shear effects.

The third section investigated the influence of applied clamping conditions on plate deflection, the resonance frequency in vacuum, and the pull-in voltage. A heuristic model incorporating an effective radius, defined as $a_{\text{eff}} = a + \mathcal{C}h$, was proposed to account for stress distribution in the support bonding region. The fitting parameter $\mathcal{C}$, was found to be approximately 0.68 for thin plates based on simulation results. The effective radius theory provided a good analytical refinement to the well-known expressions, where stresses in the support region were encountered.

Finally, the impact of shear effects was investigated. Due to the latest increasing demand for high-frequency and small-pitch CMUTs, thick plates have gained an increasing interest. Simulations were performed for the plate deflection, the resonance frequency in vacuum and immersion, as well as for the pull-in voltage and distance. For all parameters shear effect was observed to be significant for plate aspect ratios below 10. Employing an exact analytical expression for plate deflection, reduced the deviation from 22.2 % to 0.21 % at $a/h = 4$.

Overall, this chapter highlighted the importance of considering shear effects and correct boundary condition in analytical models. It provided

insights into the behavior of CMUTs, particularly in the context of thick plates and the need for further research in developing accurate expressions for key parameters.

CHAPTER 3

Design and Simulations

This chapter provides a description of the transducer design and related simulations. Three different linear designs are presented. The first design is intended for super resolution imaging as part of the 3-D Super resolution Ultrasound Real time imaging of Erythrocytes (SURE) project. It consists of 384 elements and requires a $\lambda/2-$pitch. The publication "Optimized Plane Wave Imaging for Fast and High-Quality Ultrasound Imaging" [22] demonstrates that grating lobes degrade the image quality by introducing artifacts. The study also shows that grating lobes can be eliminated by using a $\lambda/2-$pitch transducer, resulting in improved image quality. This design is from now on referred to as the Lin384 design for simplicity.

The second and third designs are suitable for integration into a laparoscope, where the transducer footprint is limited. Both designs prioritize a large transducer bandwidth due to the use of coded excitations for image formation [9]. These designs are referred to as LapMUT-A and LapMUT-B, respectively. The main difference between the two designs is the array footprint, with LapMUT-A utilizing the majority of the available area and LapMUT-B aiming for a $\lambda/2-$pitch.

The first section describes the process applied when designing CMUT arrays. The section starts by defining the external design specifications, followed by a step-by-step introduction to the analytical and simulation-based design process. Initial analytical calculations determine the horizontal and lateral parameters of the CMUT, while simulations are used to verify the array's performance and ensure that the design specifications are met. A summary table presents the parameters for the three designs before proceeding to the mask layout in the second section.

The third section presents a simulation-based study on design restrictions related to a single LOCOS process. One limitation of this fabrication method is the elevation of the nitride masking layer. In some designs, this can result in the nitride protruding above the oxide bonding surface, which hinders fusion bonding. The influence of the vacuum cavity height, oxidation temperature, and the thickness of the insulating oxide and nitride layers are investigated. Following the simulation study, a batch is fabricated using parameters that test the limits and the influence of minor aberrations in thicknesses and heights during device processing.

The final section examines the three different fabrication methods used for transducer fabrication of the Lin384 design (see Chapter 5). The simulations focus on the cavity layout, including sidewall obliquity and widening of the cell radius.

3.1 Array Design

When designing CMUT arrays, the external design specifications are determined based on the intended application of the final probe. These specifications are often provided by collaborators and may consist of both non-negotiable requirements and ranges of acceptance.

In many cases, compromises need to be made during the design process. An example highlighting such a compromise is presented in [79], where it is illustrated that increasing the output pressure leads to a reduction in bandwidth. This trade-off between bandwidth and output pressure played a crucial role in the LapMUT design phase. However, due to a shift in research focus during the Ph.D. project, the Lin384 design was chosen for a more detailed investigation.

When analytical calculations have been used to find the initial design parameters, the design is often verified through FEM simulations. These are also acquired to check the performance of the design. Over the years, such simulations have become more complex in order to provide comprehensive performance predictions [79–82].

As an alternative to the time-consuming FEM models, a simple 2D model for a single cell and a 3D model for an infinite array were developed and studied by Postdoc. Mathias Engholm using the software OnScale (PZFlex, Ansys, USA) [83]. The models were employed in this project during the design phase. By comparing the simulation results obtained from the two models with previously fabricated probes within the research group [16], it was observed that the 2D model was in good agreement with the resonance frequency, while the 3D model provided the best prediction of the bandwidth. Therefore, was the 3D model initially employed for preliminary bandwidth simulations, but was later discarded due to ongoing development and inconsistent results regarding the resonance frequency. Further

Table 3.1: External specifications for the 384-element array and the two arrays designed for the laparoscope.

	Lin384	**LapMUT-A**	**LapMUT-B**
Center frequency in immersion	15 MHz	(7–9.5) MHz	(7–9.5) MHz
Element number	384	192	192
Pitch	$\lambda/2$	-	$\lambda/2$
V_{pi}	220 V	220 V	220 V
Bandwidth	-	>100 %	>100 %
Elevation height	0.4 cm	0.8 cm	0.8 cm
Array length	-	<3.8 cm	<3.8 cm

investigation into this behavior was beyond the scope of the current Ph.D. thesis. Consequently, the 2D single-cell OnScale model was utilized for all subsequent design simulations.

A table summarizing the design parameters for the Lin384 design and the two LapMUT designs is provided at the end of this section.

3.1.1 External Design Specifications

The design specifications for the three types of transducers were established based on the end user's requirements and the intended probe application. In the case of the Lin384 design, the primary objective was to test and validate the $\lambda/2$-pitch theory presented in [22]. For the two LapMUT designs, the main goal was to integrate a CMUT-based chip into a laparoscope.

For the Lin384 design, the most crucial specification, as implied by the name, was to have 384 elements with a pitch of $\lambda/2$. The desired center frequency in immersion was 15 MHz, and the pull-in voltage was set at 220 V, with an operating potential at 80 % of the pull-in voltage. The footprint of the array included an elevation height of 0.4 cm, while the width was determined by the pitch and the number of elements. The bandwidth and output pressure were desired to be as large as possible while meeting the other design specifications.

Regarding the two laparoscope designs, the only differing parameter was the array footprint. The first design, referred to as LapMUT-A, aimed to utilize the entire available area for the transducer, resulting in an elevation height of 0.8 cm and a length of 3.8 cm. On the other hand, the second design, referred to as LapMUT-B, maintained the same elevation height while targeting a pitch of $\lambda/2$, which determined the array length. The remaining specifications were identical for both designs. The element count was set to 192, determined by the limitations of the scanner. Another important parameter for the laparoscope designs was to achieve a minimum bandwidth of 100 %. This requirement originated from the intended coding schemes to be

applied. Since bandwidth was a limiting factor, a range of center frequencies in immersion was provided as acceptable, spanning from 7 MHz to 9.5 MHz. The pull-in voltage for both designs was set at 220 V.

A summary table of the specifications for all three designs is presented in Table 3.1.

3.1.2 Design Methodology

Determining the design parameters for a CMUT is an iterative process aimed at fulfilling all criteria and identifying the optimal design. This process relies on a combination of analytic calculations and simulations, where the analytic results serve as a basis for the simulations. In general terms, the design process consists of the following steps for a LOCOS based fabrication process, each of which will be elaborated upon for the Lin834 design. The order of these steps can be adjusted based on the relative importance of different parameters.

The design steps required are

1. Determine the center frequency in immersion and the number of elements.
2. Calculate the element pitch.
3. Select the 2D cell layout, kerf width, and bonding area.
4. Calculate the cell radius.
5. Determine the plate thickness to match the immersion frequency.
6. Choose the operating voltage in percent (relative to the pull-in voltage).
7. Calculate the pull-in voltage.
8. Adjust the gap height and consider fabrication feasibility with the desired processing technique (see Section 3.3).
9. Determine and calculate the vertical parameters (nitride thickness, bump and post oxide height).
10. Verify that the performance meet the specifications.
11. Check for substrate ringing and array effects (Bragg frequency).
12. Perform full FEM simulations for final validation.

1. Frequency and 2. Element Pitch

As shown in Table 3.1, the center frequency for the Lin384 design was specified to be 15 MHz. Utilizing this frequency and the criterion of a $\lambda/2$-pitch,

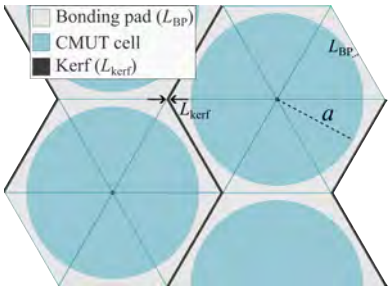


Figure 3.1: Sketch of the hexagonal closed-packed scheme used for the Lin384 design illustrating how to calculate the maximum possible cell radius.

the element pitch was calculated by

$$\frac{\lambda}{2} = \frac{c_{\mathrm{m}}}{2f_{\mathrm{res}}}. \tag{3.1}$$

Employing a speed of sound in the body of 1540 m/s, the pitch results in 51.33 µm.

3. Cell Layout and 4. Radius

Subsequently, the cell layout was determined, encompassing the cell packaging, kerf width, and the size of bonding area. Historically, the majority of applied cell shapes have been either circular or squared [12, 84]. Each with its own distinct advantages. In [56], a comprehensive electrostatic analysis compared circular and square cell layouts. The study investigated various aspects, including capacitance, effective spring constant, pressure-dependent pull-in voltage, and pull-in distance. In all cases, both cell shapes exhibited similar behavior. Based on those results, a circular cell layout was selected, which offers a slightly larger bonding area.

For optimal cell packaging, a Hexagonal Closed-Packed (HCP) grid was chosen. The minimum cell separation distance was determined to be 10 µm plus the width of the kerf, to ensure an adequate bonding area. The kerf width, denoted L_{kerf}, which separates the elements, was set to 4 µm. Additionally, for the Lin384 design, it was decided to only have one cell per element width due to the small pitch. While it is theoretically possible to include more columns of cells, maintaining the same bonding area would decrease the ratio of active area to bonding area, inducing a reduction in emitted pressure. Alternatively, the bonding area can be decreased, however, this poses a risk of bonding failure resulting in a potentially lower yield.

Based on these choices, the maximum achievable cell radius can be calculated by

$$\frac{\lambda}{2} = \sqrt{3}(a + L_{\mathrm{BP}}) + L_{\mathrm{kerf}} \leftrightarrow a = \frac{(\lambda/2 - L_{\mathrm{kerf}})}{\sqrt{3}} - L_{\mathrm{BP}}. \tag{3.2}$$

Here L_{BP} denotes the width of the bonding area. Fig. 3.1 provides an illustration of the HCP structure, defining the different parameters applied in the above equation. Assuming $L_{\mathrm{BP}} = 5\,\mu\mathrm{m}$ and $L_{\mathrm{kerf}} = 4\,\mu\mathrm{m}$, the maximum applicable radius was calculated to 22.3 µm. However, a simulation-based cavity study performed under supervision of the author revealed that during a double LOCOS process, the cell radius increases by 1.3 µm as a result of the oxidation steps. Consequently, adjustments are required in the lithography masks for both the bump and the cavity radii. Hence, the mask layout includes a cell radius of 21 µm.

5. Plate Thickness

The plate thickness calculation was performed using the ratio between the frequency in immersion and the vacuum frequency, as derived in Eq. (2.34). Combined with expression for the resonance frequency in vacuum, given in Eq. (2.6) and the effective radius from Eq. (2.59), the equation to solve becomes

$$\omega_{\mathrm{r}}\sqrt{1+\Gamma_{\mathrm{Taylor}}\frac{a+\mathcal{C}h}{h}\frac{\rho_{\mathrm{m}}}{\rho_{\mathrm{p}}}} = 10.2158\sqrt{\frac{Y}{12(1-\nu^2)\rho_{\mathrm{p}}}}\frac{h}{(a+\mathcal{C}h)^2}. \tag{3.3}$$

The applied cell radius was $a = 22.3\,\mu\mathrm{m}$, a value of 0.68 was used for $\mathcal{C}$ and the NAVMI factor, based on the Taylor approximation, was $\Gamma_{\mathrm{Taylor}} = 0.6941$. The relevant material parameters are summarized in Table 3.2. As specified in Table 3.1, the immersion angular frequency is $\omega_{\mathrm{r}} = 15\,\mathrm{MHz} \times 2\pi$.

Based on these values, the initial plate thickness was calculated to be 4.2 µm. However, the actual CMUT design is more complex than assumed by these analytical models. The models consider a single-layer silicon plate without a top electrode, and are based on an unbiased assumption. However, the desired frequency in immersion is specified under transducer operation at 80 % of the pull-in voltage. Due to spring softening effects, the unbiased resonance frequency should be higher than the design specifications. These factors are challenging to incorporate in a simple analytical model but are taken into account in the FEM simulations, which are further discussed in step 12 of the design process. The results of the FEM study indicated the need for a plate thickness of 4.5 µm having a plate radius of 22.3 µm to achieve an operating frequency in immersion of 15 MHz at the defined potential. For reference the analytical result employing the radius a resulted in $h = 3.4\,\mu\mathrm{m}$. This demonstrates the impact by the effective radius theory, providing a better initial guess for the plate thickness.

6. Operating and 7. Pull-in Voltage

The operating voltage was predetermine to be 80 % of the pull-in, which was specified to be 220 V for all three designs. These parameters were limited by

Table 3.2: Material parameters using for the analytic design calculations.

Paramter	**Value**
Young's modulus silicon, Y	148 GPa
Poisson's ratio, ν	0.177
Density silicon, ρ_{p}	2328 kg/m^3
Density water, ρ_{m}	1000 kg/m^3
Vacuum permittivity, ϵ_0	8.854×10^{-12} F/m
Permittivity oxide, ϵ_{ox}	3.9
Permittivity nitride, ϵ_{ni}	7.5

the scanner properties. The choice of 80 % bias was made to maximize the signal output while ensuring that the CMUT cells do not collapse. During operation the designs were configured to operate with a bias voltage of $V_{\mathrm{DC}} = 176$ V.

8. Gap Height

The gap height was subsequently adjusted to match the pull-in voltage. Initially, the effective gap height was calculated using the analytical expression derived in Eq. (2.27). The applied material parameters for silicon are provided in Table 3.2. The resulting effective gap height was calculated to $g_{\mathrm{eff}} = 147$ nm. However, since the LOCOS structure includes oxide and nitride layers, the effective gap also encompasses these layers. By utilizing Eq. (2.9) with the respective permittivity values for the oxide and nitride layers, and applying an oxide height of $h_{\mathrm{ox}} = 400$ nm and nitride thickness of $h_{\mathrm{ni}} = 55$ nm, the resulting vacuum gap height was calculated to $g = 79.6$ nm.

As a result of the simplifications employed in the analytical expression, the gap height was adjusted to 66 nm based on the simulation results. The details are worked through in step 12, where the FEM simulations are presented.

To determine the feasibility of fabricating the transducers with the obtained dimensions, simulations were conducted using Athena (Silvaco, CA, USA). The simulation code is shown in Appendix I, and the result confirmed that fabrication of a double LOCOS structure was feasible with the identified dimensions, allowing the design process to proceed.

9. Vertical Parameters

The next step involved determining and calculating the vertical parameters based on the chosen fabrication method. This process will be explained for three different approaches: the single LOCOS process, the double LOCOS process, and the maskless LOCOS process.

The single LOCOS process was used to validate the simulation results presented in Section 3.3, while both the double LOCOS process and the maskless LOCOS process were implemented on the device wafers, as described in detail in Chapter 5.

For a LOCOS process, it was crucial to determine the thickness of the nitride and the insulating oxide, as well as the bump height. Combined with the previously established gap height, the post oxide height could be determined.

The nitride layer primarily serves as a diffusion barrier during the LOCOS process. Its thickness was determined based on prior research experience within this research group. Additionally, Fig. 3.15 was consulted to verify the thickness against results found in the literature. The influence of the nitride layer thickness is further investigated in Section 3.3. Similarly, the thickness of the insulating oxide layer was determined based on research experience. This layer acts as an insulation layer during transducer operation and needs to withstand the applied bias without experiencing breakdown. The determined thicknesses for the nitride (h_{ni}) and insulating oxide (h_{ox}) layers were 55 nm and 400 nm, respectively.

Finally, the bump height and bump radius were determined. Based on previous findings elaborated in [16], it was established that the bump radius should be 2/3 of the cavity radius to ensure optimal plate movement. Furthermore, the target height for the bumps (h_{bump}) was set at 500 nm.

Single LOCOS Structure Fig. 3.2a illustrates a single CMUT cell fabricated using the single LOCOS process. The parameters related to the process are defined in the figure. Based on the outlined definitions the post oxide height is defined as

$$h_{\mathrm{post}} = g + h_{\mathrm{ni}} + h_{\mathrm{ox}} + h_{\mathrm{bump}}, \tag{3.4}$$

Employing a volumetric ratio between silicon and oxide of approximately 45 %, the bump height can be expressed

$$h_{\mathrm{bump}} = \frac{1}{2.2}(h_{\mathrm{post}} - h_{\mathrm{ox}}). \tag{3.5}$$

Combining these two equations leads to

$$h_{\mathrm{post}} = \frac{g + h_{\mathrm{ni}}}{1 - \frac{1}{2.2}} + h_{\mathrm{ox}}. \tag{3.6}$$

Once the desired post-oxide height was known, the corresponding oxidation time could be determined.

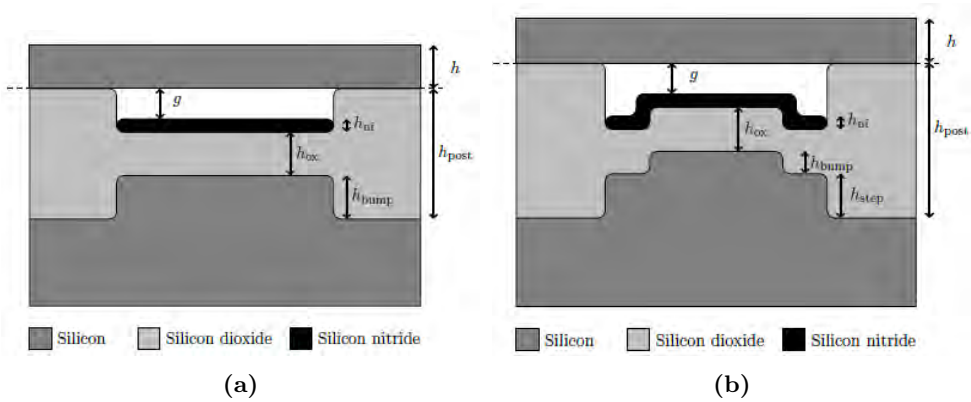


Figure 3.2: Cross-sectional illustration of a CMUT cell fabricated using **(a)** a single LOCOS process and **(b)** a double LOCOS process. The drawings are not to scale and are a reprint from [16].

Double LOCOS Structure Similarly, the post-oxide height for the double LOCOS process can be calculated. Fig. 3.2b depicts a single cell fabricated using the double LOCOS process. The cross-section of the CMUT cell is shown with indications of the relevant parameters. In this process, the bump is formed during the first LOCOS step, while the second step is responsible for defining the post-oxide, which forms the sidewalls of the cell and the bonding surface for subsequent fusion bonding. The post-oxide height is defined as

$$h_{\text{post}} = g + h_{\text{ni}} + h_{\text{ox}} + h_{\text{bump}} + h_{\text{step}}, \tag{3.7}$$

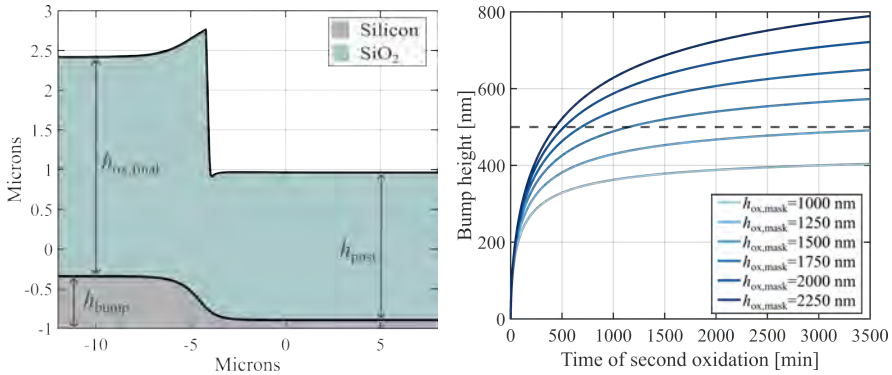
where h_{step} defines the silicon step formed during the second LOCOS process. By introducing $h_{\text{step}} = (1/2.2)(h_{\text{post}} - h_{\text{ox}})$, the expression becomes

$$h_{\text{post}} = \frac{g + h_{\text{ni}} + h_{\text{bump}}}{1 - \frac{1}{2.2}} + h_{\text{ox}}. \tag{3.8}$$

Maskless LOCOS Structure In Fig. 3.3a, the bump fabricated using the maskless LOCOS process is shown after the long oxidation step, creating the bump structure. The thickness of the masking oxide layer is denoted $h_{\text{ox,mask}}$, while $h_{\text{ox,final}}$ represents the oxide thickness on top of the bump after its definition.

To describe the oxide growth during the maskless LOCOS process, the basic equations from the Deal-Grove model are utilized [85]. According to this model, the oxide layer thickness, as a function of time t, can be expressed as

$$x = \frac{1}{2}\left(\sqrt{A^2 + 4B(t+\tau)} - A\right), \tag{3.9}$$



(a) **(b)**

Figure 3.3: **(a)** Cross-sectional illustration of the bump in a CMUT cell fabricated using the maskless LOCOS process. Note, the drawing is not to scale. **(b)** Shows the relationship between the thickness of the oxide mask and the fabrication time required to form a 500 nm silicon bump.

where τ, which represents a time shift, is given by

$$\tau = \frac{x_{\mathrm{i}}^2 + Ax_{\mathrm{i}}}{B}. \tag{3.10}$$

The parameters A and B are process and temperature dependent, and are derived from data acquired from the furnace in the cleanroom at DTU Nanolab. The initial oxide thickness on the substrate, denoted as x_{i}, corresponds to $h_{\mathrm{ox,mask}}$ in this particular case.

The height of the post-oxide layer can be determined using the following equation

$$h_{\mathrm{post}} = 2.2h_{\mathrm{bump}} - h_{\mathrm{ox,mask}} + h_{\mathrm{ox,final}}. \tag{3.11}$$

By incorporating the Deal-Grove model to calculate $h_{\mathrm{ox,final}}$ the equation becomes

$$h_{\mathrm{post}} = 2.2h_{\mathrm{bump}} - h_{\mathrm{ox,mask}} + \frac{1}{2}\left(\sqrt{(A + 2h_{\mathrm{ox,mask}})^2 + 4Bt} - A\right). \tag{3.12}$$

Furthermore, the post-oxide height is replaced by Eq. (3.9), hence the equation to solve becomes

$$h_{\mathrm{bump}} = \frac{1}{2.2}\left[\frac{1}{2}\left(\sqrt{A^2 + 4Bt} - \sqrt{(A + 2h_{\mathrm{ox,mask}})^2 + 4Bt}\right) + h_{\mathrm{ox,mask}}\right]. \tag{3.13}$$

Based on this equation, the impact of the oxide mask thickness was investigated for various thicknesses. The findings are shown in Fig. 3.3b. The results demonstrates that using a mask thickness of 1000 nm or 1250 nm is not feasible for achieving a 500 nm bump. However, the thicker masks are

all feasible, with required oxidation times ranging from approximately 7 h to 19 h. A time optimization study conducted by M.Sc. Søren W. Gjaldbæk under supervision of the author, showed that the time was minimized when using a 2 µm thick oxide mask [86].

It is important to emphasize that the post oxide height in all cases should be adjusted using the specific parameters from the fabrication process to achieve the most accurate result possible.

10. Design Specifications and Performance

For the Lin384 design the key design parameter was the $\lambda/2$-pitch for a 15 MHz probe. These specifications were met in step 3-5. However, to evaluate the design performance, a 2D simulation was carried out using OnScale. This is described in more detail in step 12. The -6 dB bandwidth at 80 % of the pull-in voltage was found to be 77.9 %.

11. Substrate Ringing and Bragg Frequency

Finally, it is crucial to assess the array effects in the design as these can introduce interference with the signals emitted from the CMUTs. Two specific array effects: substrate ringing and the Bragg frequency, were considered.

Substrate ringing occurs when a wave is transmitted into the substrate during sound emission. When reaching the backside of the substrate, the signal is reflected back into the CMUT, interfering with the emitted signal used for imaging. This interference leads to a reduction in image quality. Mathematically, the substrate ringing effect can be described as follows

$$t_{\text{sub}} = \frac{2h_{\text{sub}}}{c_{\text{sub}}}, \tag{3.14}$$

where t_{sub} represents the echo time, h_{sub} is the substrate thickness, and c_{sub} is the speed of sound in the substrate. For the low resistivity silicon wafers utilized in the fabrication of the linear LOCOS-based Lin384 array, the substrate ringing frequency can be calculated as

$$f_{\text{Si}} = \frac{c_{\text{Si}}}{2h_{\text{Si}}} = 8.03\,\text{MHz}. \tag{3.15}$$

This result assumes a longitudinal speed of sound in silicon of $c_{\text{Si}} = 8433\,\text{m/s}$ and a wafer thickness of 525 µm. It is evident that for high-frequency, $\lambda/2$-pitch applications like the Lin384 array, this frequency lies outside the array bandwidth and does not pose a problem. However, for the two LapMUT designs, this frequency falls within the bandwidth and becomes problematic. One potential solution involves the implementation of a backing layer with

a matching acoustical impedance, similar to what is presented in [87]. This layer serves as an absorber, eliminating the reflected sound wave, and should therefore possess high attenuation. Another approach is to shift the substrate ringing signal outside the bandwidth. This can be achieved through substrate thinning, with lapping being a suitable method. By reducing the silicon substrate thickness to 250 µm through lapping, the frequency is shifted to 15.33 MHz. The process development of lapping for silicon wafer thinning, is described in Chapter 4.

The Bragg frequency describes the mutual coupling between the cells and depends on the cell pitch, d_{cell} [42]. It is defined as

$$f_{\text{Bragg}} = \frac{c_{\text{m}}}{d_{\text{cell}}}. \tag{3.16}$$

For an array having $\lambda/2$-pitch, and one cell per element, this equation can be combined with Eq. (3.1), which can then be reduced to

$$f_{\text{Bragg}} = \frac{c_{\text{m}}}{c_{\text{m}}/2f_{\text{res}}} = 2f_{\text{res}}. \tag{3.17}$$

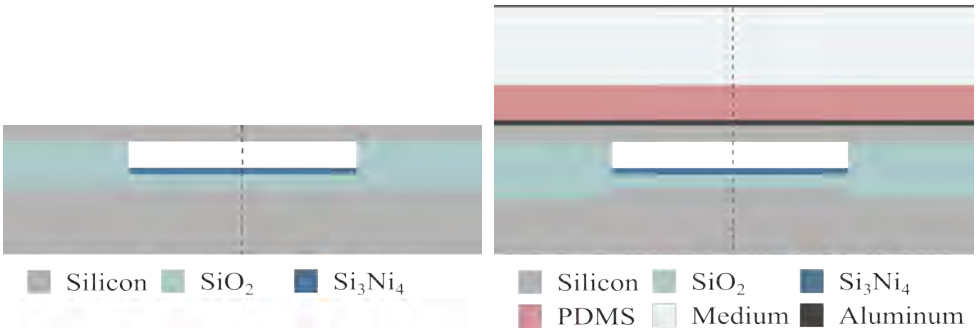
For the Lin384 design having a $\lambda/2$-pitch indicates that the Bragg frequency does not pose a problem, resulting in a value of 30 MHz. In the case of the LapMUT-A and LapMUT-B designs, the cell pitch is 40.7 µm, which corresponds to a Bragg frequency of 37.8 MHz. This Bragg frequency is significantly different from the center frequency in immersion, and does therefore not interfere with the main signal.

12. FEM Simulations

After analytically determining the horizontal and lateral parameters, as well as assessing potential array effects of the CMUT, various simulations were performed using the COMSOL Multiphysics and OnScale (PZFlex, Ansys, USA) software tools. These tools are both FEM-based and are widely used for simulations in the field of ultrasound. While COMSOL allows for electromechanical analysis of the CMUT, used to determine the gap height and pull-in voltage, Onscale provides time-domain responses, enabling simulation of the pressure and the bandwidth. The simulations were carried out using a single CMUT cell with axial symmetry. The parameters obtained from the analytical studies were used as a starting point, and were then adjusted based on the simulation results in an iterative process.

Simulation Models

An overview of the simulated structure applied in the COMSOL simulation is provided in Fig. 3.4a. The CMUT structure comprises a silicon bottom substrate with an insulating oxide and nitride on top. The top plate consists



(a) **(b)**

Figure 3.4: Outline for the two structures simulated in **(a)** COMSOL Multiphysics and **(b)** OnScale, PZFlex. Both structures utilizes a single CMUT cell, with an insulating oxide and nitride in the cavity. Note the illustrations are not to scale.

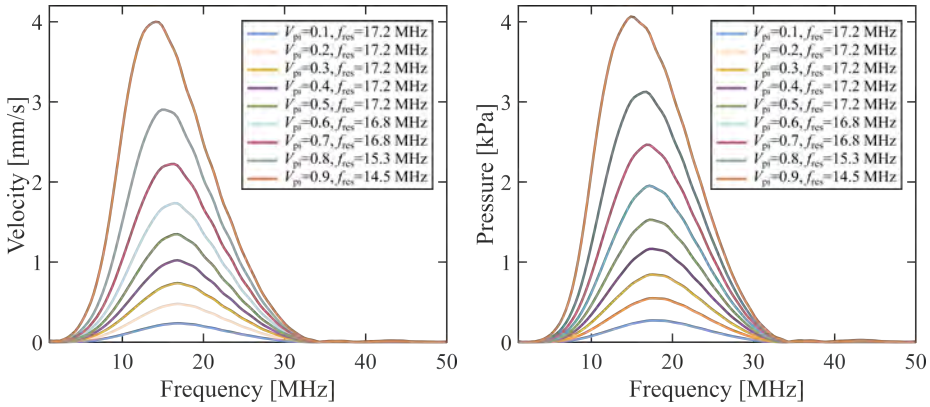
of silicon with an aluminum layer on top. The simulations were performed in air. The COMSOL-based simulation was employed to determine and adjust the gap height to meet the specified voltage requirement. Additionally, it provided an estimate of the biased and unbiased eigenfrequencies of the plate.

Once the gap height was determined, the parameters were applied in the OnScale-based simulation. An illustration of the simulated structure is presented in Fig. 3.4b, which is a further development of the PZFlex model described in [40]. The structure consists of a fixed silicon substrate, with a silicon bump in the cavity region, resembling a LOCOS structure. Furthermore, an insulating oxide and a nitride layer are also included in the same region. The top plate is a silicon plate with an aluminum layer on top. Finally, a 200 µm thick layer of PDMS and a 100 µm water layer were added as medium. Additionally, simulations were performed with air as an interchangeable medium to examine the influence of the PDMS layer. Furthermore, the figure depicts the absorbing boundary at the end of the medium, as well as the axis of symmetry. The dimensions used in the final simulation correspond to the design parameters summarized in Table 3.3.

Simulation Results

The COMSOL simulation results for the Lin384 design yielded a gap height of 66 nm for a 4.5 µm thick top plate and a pull-in voltage of 220 V. The first unbiased eigenfrequency was determined to be 27.0 MHz, while the first biased eigenfrequency (applying $0.8V_{\text{pi}} = 176\,\text{V}$) yielded 23.9 MHz.

In the OnScale simulation, a linear DC voltage ramp was applied with a delayed AC signal of 1 V. The bias voltage was varied between $0.1V_{\text{pi}}$ and $0.9V_{\text{pi}}$. The Fourier transform was then applied to obtained the impulse response, resulting in velocity and pressure data in the frequency domain.



(a) **(b)**

Figure 3.5: Fourier transformed data obtained from OnScale simulations in immersion for various applied bias voltages. The peak frequency was extracted for each bias. **(a)** Shows the simulated velocity, while **(b)** depicts the extracted pressure data.

These frequency responses are shown in Fig. 3.5a and 3.5b, respectively. Notice, that for an applied bias voltage of 80 % of the pull-in voltage, the estimated resonance frequency is 15.3 MHz, which aligns with the external design specifications.

Extracting the maximum values from the frequency responses results in Fig. 3.6a, were the frequencies are presented as function of the applied bias voltage relative to the pull-in voltage. This figure illustrates the spring softening effect, as expected from theory (see Eq. (2.23)). Furthermore, the −6 dB bandwidth was calculated for both the velocity and the pressure. The results are illustrated in Fig. 3.6b, which also includes the maximum pressure. At the operational bias the pressure bandwidth was found to be 77.9 %, while the pressure magnitude was derived to 3124 Pa.

The results of the OnScale simulations conducted in air is presented in Fig. 3.7, where the relationship between the maximum frequencies and the relative applied bias voltages are illustrated. For comparison, Fig. 3.7a displays the results without a PDMS layer, while Fig. 3.7b showcases the results with a PDMS layer on top of the CMUT. It is noteworthy that the presence of PDMS significantly reduces the resonance frequency, making it comparable to the results obtained from the simulations conducted in immersion. Both sets of results demonstrate the spring softening effect, where the resonance frequency decreases as the bias voltage increases. The simulated pressures relative to the frequency are provided in Appendix D.

A summary of the final parameters is provided in Table 3.3.

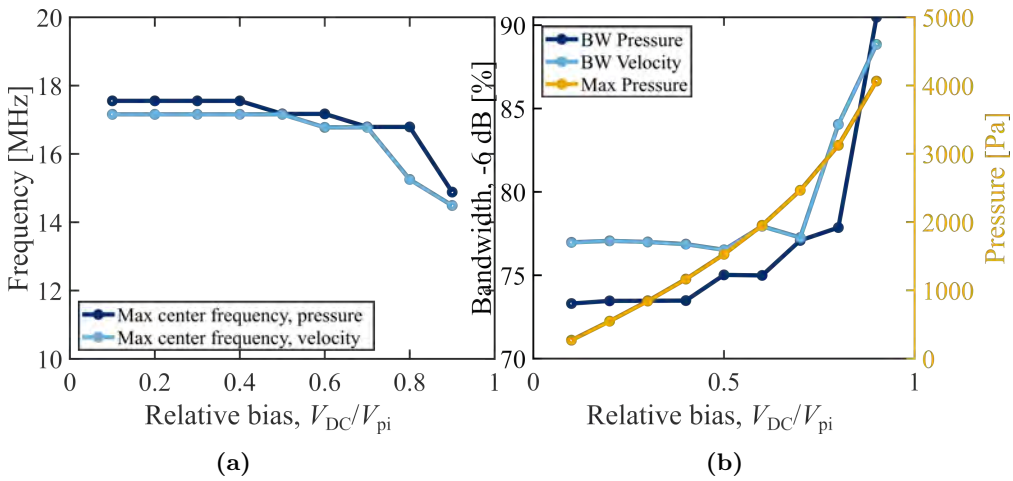


Figure 3.6: OnScale data obtained from simulations in immersion. **(a)** Shows the maximum center frequency plotted against the relative applied voltage. **(b)** Depicts the bandwidth and pressure data plotted against the relative applied bias. Both the peak frequency and the bandwidth are extracted from both the velocity and the pressure data.

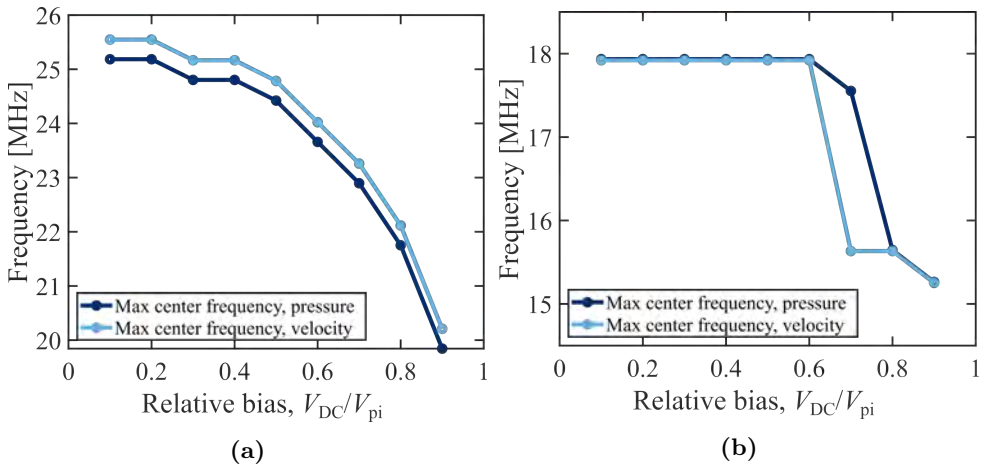


Figure 3.7: Simulation results from the OnScale simulations conducted in air. The graphs depicts the relation between the maximum frequency and the relative applied bias voltage. **(a)** Shows the results without a PDMS layer, while the results in **(b)** is obtained with a PDMS layer. Notice the different y-axis.

Table 3.3: Design specifications for the three developed designs. All three designs were created for a double LOCOS fabrication process.

Parameters	**Lin384**	**LapMUT-A**	**LapMUT-B**	**Unit**
Cell				
Center frequency, immersion[a]	15	9.3	9.3	[MHz]
Center frequency, air[a]	23.9	17.3	17.3	[MHz]
Pull-in voltage, V_{pi}	220	220	220	[V]
DC bias voltage, V_{DC}	$0.8V_{\mathrm{pi}}$	$0.8V_{\mathrm{pi}}$	$0.8V_{\mathrm{pi}}$	[V]
Radius, a	21	20.5	20.5	[µm]
Bump radius, a_{bump}	14	13.53	13.53	[µm]
Bump height, h_{bump}	500	500	500	[nm]
Plate thickness, h	4.5	2.5	2.5	[µm]
Vacuum gap, g	66	136	136	[nm]
Insulating oxide thickness, h_{ox}	400	400	400	[nm]
Post oxide thickness, h_{post}	1539	1669	1669	[nm]
Nitride thickness, h_{ni}	55	55	55	[nm]
Metal thickness	400	400	400	[nm]
Element				
Cell packaging	HCP	HCP	HCP	
Min. bonding area, L_{BP}	5	3	3	[µm]
Cells per element	65	620	310	
Array				
Element pitch	51.33	166.82	85.56	[µm]
Kerf, L_{kerf}	4	4	4	[µm]
Array height	4.0	8.0	8.0	[mm]
Array width	19.8	32.2	16.6	[mm]
Substrate ringing, f_{Si}	8.03	8.03	8.03	[MHz]
Bragg frequency, f_{Bragg}	30	32.8	32.8	[MHz]
Number of elements	384	192	192	
Bandwidth, −6dB[a]	77.9	65.1 (109)[b]	65.1 (109)[b]	[%]

[a] Biased center frequency at V_{DC}.
[b] Result from the discarded 3D OnScale simulation.

3.2 Mask Layout

After finalizing the design process and determining all horizontal and lateral parameters, a wafer map was generated for each of the three designs. In this section the mask layout will be worked through for the 384-element array. However, the wafer maps for the two laparoscope designs follow a similar organization.

Since the double LOCOS process requires most lithography masks, compared to the other employed fabrication methods, this section will focus on elaborating the mask design for this process. The total number of lithography masks for this process is five.

The first two masks defined the bumps and the cavities, respectively. The third mask was used to create openings for the bottom electrodes. Subsequently, another lithography mask was employed to separate the top electrodes and the underlying top plate. To ensure protection of the arrays during dicing and electrical characterization, a final mask was added. This mask left the entire structure covered with photosensitive resist (from now on simply resist), only opening the bonding pads necessary for electrical probing.

The mask layout for the 384-element transducer comprises 29 arrays, each representing the main transducer design. Figure 3.8 provides an illustration of a single array containing 384 elements. The insert shows a close-up view of few CMUT cells, highlighting their structure and packaging, along with three top electrode bond pads. These bond pads are used for probing and subsequently wire bonding. Similar illustrations of the two array designs created for the laparoscope, LapMUT-A and LapMUT-B, can be found in Appendix E.

Additionally, two linear designs with 16 elements were included on the mask layout to accommodate a previously defined CCB for initial acoustic tests. One of these designs, referred to as *Single*, maintains the same cell packaging per element as the actual array elements. The other design, referred to as *Filled*, is fully packed with CMUT cell while keeping the pitch defined from the CCB. These designs are depicted in Fig. 3.9a and 3.9b, respectively. It is important to note that the elevation height is slightly increased in both designs due to the CCB design, resulting in higher capacitance compared to the element capacitance from the 384 element arrays. Appendix E provides similar illustrations for the 16-element arrays for the two LapMUT designs.

An overview of the wafer map, together with the corresponding naming convention, is presented in Fig. 3.10. The large 384-element arrays follow a row-column convention for their naming, while the prefixes S and F denotes *Single* and *Filled* for the 16-element arrays, respectively. The corresponding overview wafer maps for the two LapMUT designs can be found in Appendix E.

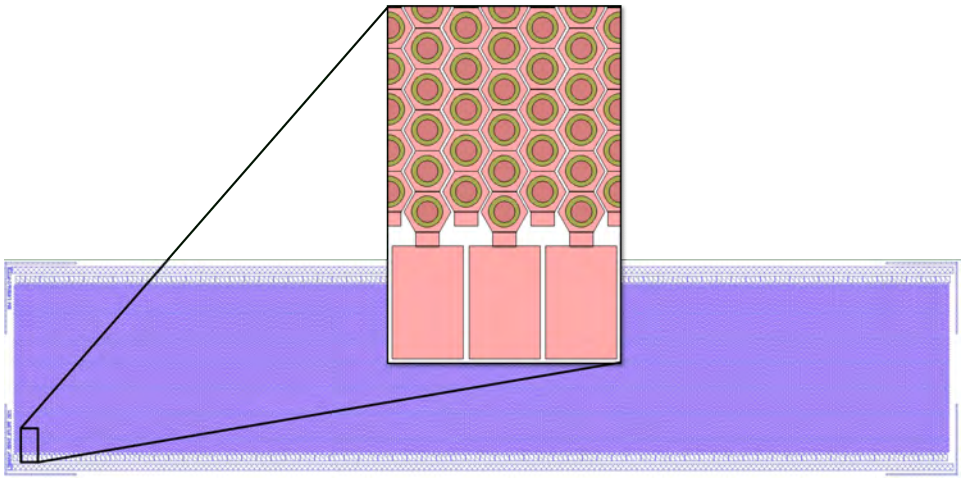
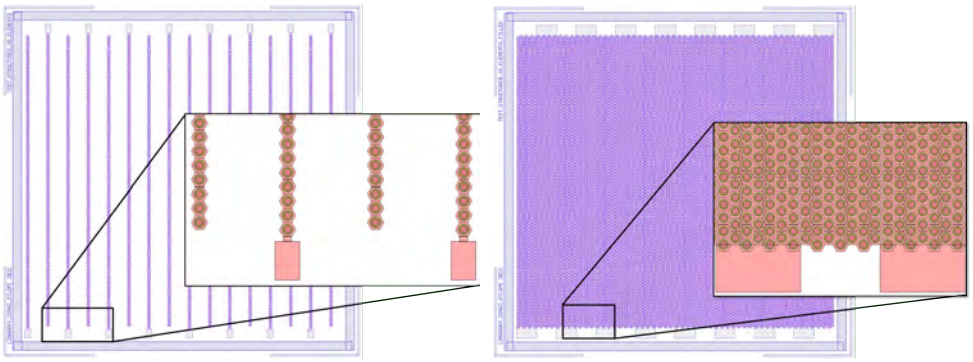


Figure 3.8: Illustration of the linear array comprising 384-elements with a $\lambda/2$-pitch, with a close-up showing the cell packaging.



(a) **(b)**

Figure 3.9: Images depicting the design of **(a)** the *Single* test array and **(b)** the *Filled* test array. Both designs were developed based on the bond pad pitch of a preexisting CCB. The two close-ups shows the cell packaging.

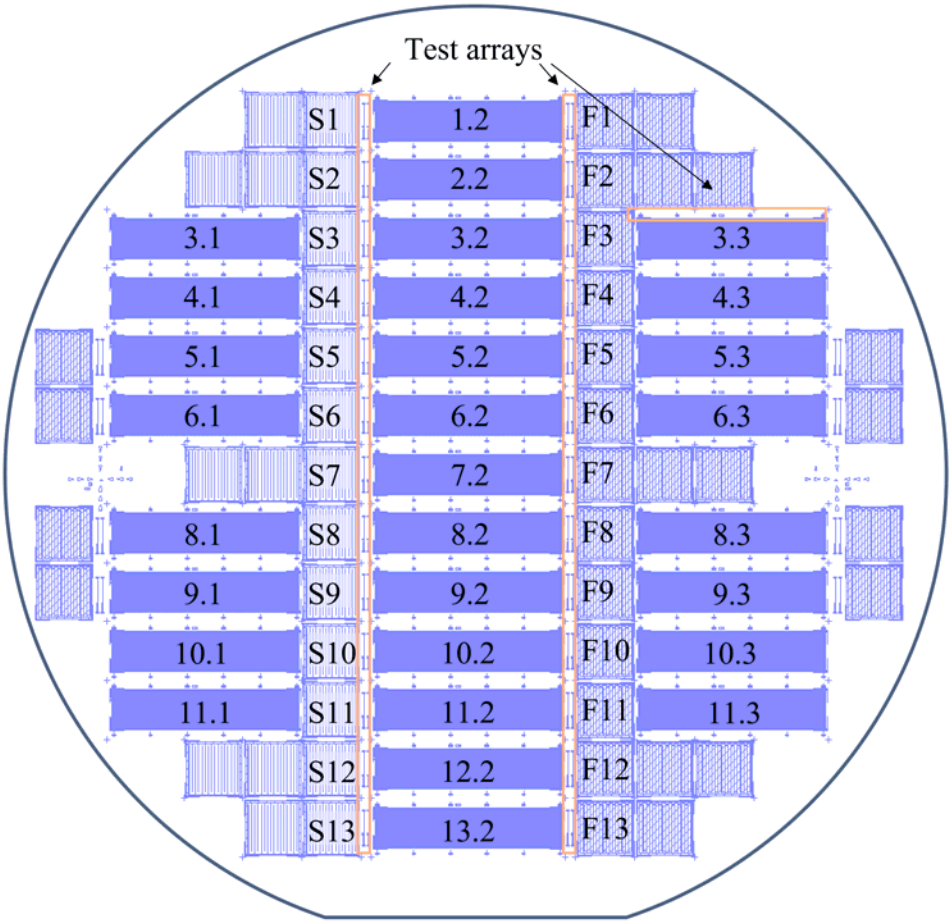


Figure 3.10: Overview of the wafer map and naming convention employed for the Lin384 transducer design.

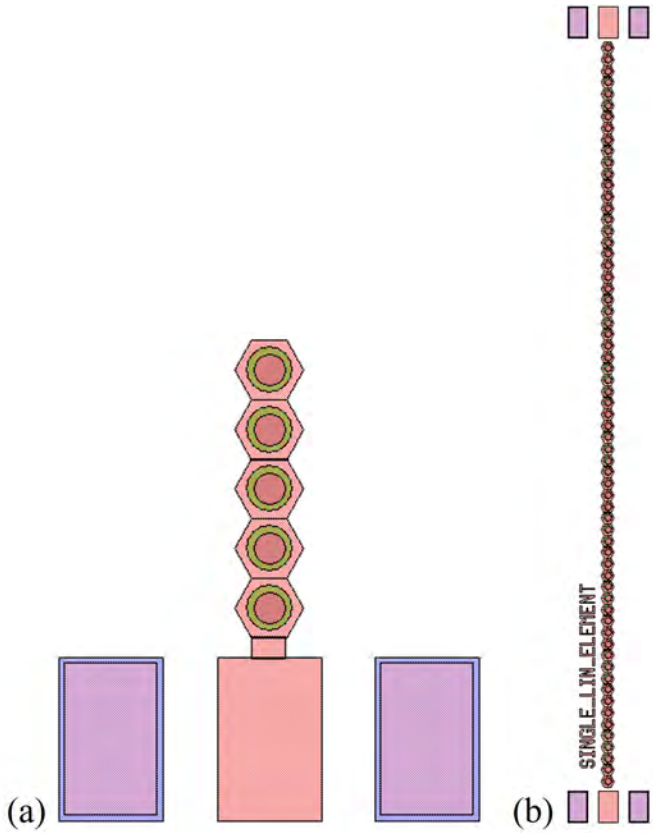


Figure 3.11: Illustration of the two types of test elements added to the mask layout. (a) Shows the five-cell test array located around the large transducer arrays, while (b) shows a test element identical to a single element from the 384-element array. These are located around the center column of large arrays.

In the wafer map, the orange squares indicate the position of the two types of test arrays incorporated into the layout. Between the center column and the 16-element arrays, two columns of test arrays were located. These test arrays resemble the elements in the 384-element arrays. Smaller test arrays consisting of a few CMUT cells were located above and below each large 384-element transducer array, as illustrated above array 3.3 in Fig. 3.10. A detailed view of the two test structures is shown in Fig. 3.11.

To ensure a more uniform load distribution across the wafer, additional 16-element arrays of both the *Single* and *Filled* designs were included in the periphery of the Lin384 wafer. The load distribution is important during fabrication to achieve better uniformity across the wafer. This becomes especially crucial during a Reactive Ion Etching (RIE) process, where uniform etch rates are desired.

3.3 Single LOCOS Cavity Design

The fabrication technique based on LOCOS and fusion bonding offers several advantages over other methods such as sacrificial release or anodic bonding, including reduced parasitic capacitance and robust behavior. However, this technique also has certain drawbacks. One of these drawbacks is elevation of the nitride mask layer, resulting from the 2D diffusion occuring during the oxide growth. If the nitride layer protrudes above the bonding area, which consists of oxide, it can impede the fusion bonding process. This is caused by the highly sensitive nature of the fusion bonding process, which requires a surface roughness below 0.5 nm [88].

The problem with protruding nitride has been addressed for a double LOCOS process in [89]. However, in certain cases, it can be beneficial to conduct an accelerated fabrication process to verify compliance with predetermined design specifications. Therefore, this study aims to investigate the problems associated with nitride protrusions in a single LOCOS process. Furthermore, the parameters having the greatest influence on the problem is identified, and the limits for structures feasible to fabricate is evaluated. Subsequently, a batch was fabricated using the LapMUT-B design to test these limitations.

3.3.1 Simulation Study

This simulation study was conducted using the Athena software (Silvaco, CA, USA), which provides numerical, two-dimensional simulations of semiconductor processing. The simulations were performed utilizing a cell radius of $a = 5\,\mu\text{m}$, as a preliminary study indicated that the cell radius has negligible influence when the other parameters, such as the insulating oxide thickness, gap height, and nitride thickness, are held constant. The applied

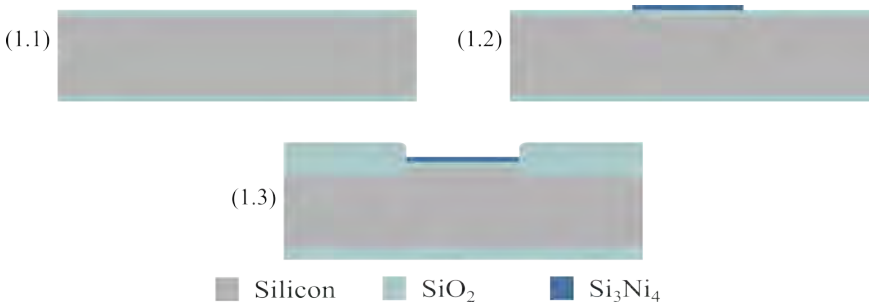


Figure 3.12: Process flow overview utilized in the simulations to explore the parameter space for a single LOCOS process. Note, the dimensions are not to scale.

grid was optimized in a convergence mesh study modified to the applied dimensions. Additionally, the built-in `viscous` oxidation model was compared against the built-in `compressed` oxidation model. No significant difference were observed, thus the `viscous` model was employed in the simulations. Details of this study can be found in Appendix I.1.

An overview of the simulated fabrication process is illustrated in Fig. 3.12. Step (1.1) depicts the growth of the insulating oxide. Step (1.2) shows the deposition and structuring of the masking nitride layer. The final step (1.3) demonstrates the appearance of the cavity formed during the LOCOS process using a wet oxidation process. The chosen layer thicknesses were selected to determine the limits for structures feasible to fabricate.

The initial study focused on examining the impact of temperature during the LOCOS step. The temperature was varied from 950 °C to 1100 °C in increments of 50 °C. In addition, this temperature study was conducted for six different gap heights, g, ranging from 100 nm to 350 nm with 50 nm intervals. During the study, the insulating oxide thickness was kept at a constant value of 400 nm, while the nitride thickness was defined to 50 nm.

The measurement of the nitride peak height was conducted relative to the surface of the bonding area, as depicted in Fig. 3.13. A positive value indicates a protrusion above the bonding surface inhibiting fusion bonding, whereas a negative value indicates that the nitride is positioned below the bonding surface, enabling fusion bonding.

The results of the temperature study are illustrated in Fig. 3.14. It shows that fabricating a gap height of 100 nm is not feasible with the given thicknesses for the insulating oxide and the nitride. This result is consistent across all simulated temperatures. In general, insignificant variations are observed across all gap heights in relation to the applied temperatures. This suggests that temperature does not have a significant impact on the feasibility of fabricating specific designs, although it can be considered for fine process adjustments. Furthermore, the graph shows that gap heights

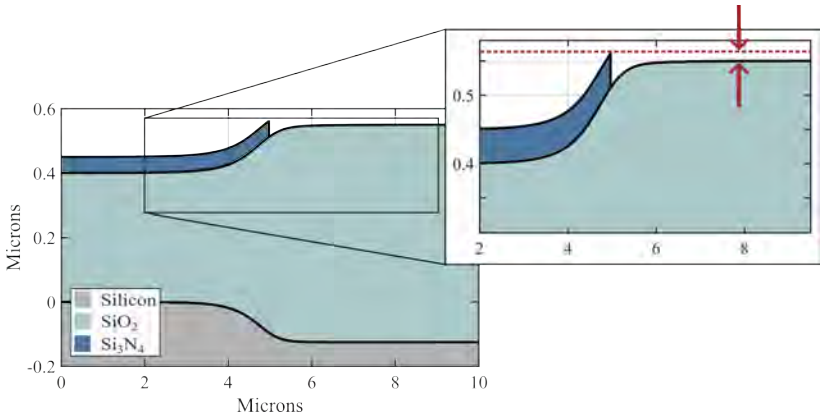


Figure 3.13: The illustration demonstrates the occurrence of a nitride protrusion above the bonding surface. The insert provides a visual representation of the method used to determine the height of the nitride peak.

of 200 nm and above results in a sufficiently negative nitride peak height relative to the oxide surface, indicating that no fabrication related issues are expected to arise. However, for a gap height of 150 nm, a slight negative peak height value is observed. Given the small magnitude of these values, even minor changes in the thickness of either the insulating oxide layer or the nitride layer can potentially cause the fabrication to fail.

The second study aimed to examine the impact of nitride thickness on the fabrication feasibility. To conduct this investigation, the insulation oxide thickness was constant at 400 nm, and a fixed gap height of 150 nm was applied. The LOCOS step was carried out using wet thermal oxidation at 1100 °C for 73 min.

Fig. 3.15 illustrates the minimum required layer thickness of the masking nitride during an oxidation process. The graph encompasses results for both wet and dry oxidation atmospheres, as well as varying processing temperatures. For the wet oxidation conditions of 1100 °C for 73 min, the graph indicates a minimum nitride thickness of 20 nm. Consequently, the simulation study explored nitride thicknesses ranging from 20 nm to 65 nm in steps of 5 nm.

The results are depicted in Fig. 3.16 and demonstrate a significant influence of nitride thickness on the fabrication process. The graph reveals that nitride thicknesses above 60 nm prevent fusion bonding for this structure. Furthermore, is shows that nitride thicknesses of 50 nm and 55 nm are within a gray zone, where fabrication is theoretically possible; however, minor deviations during processing can lead to bonding failures. According to the simulations, thicknesses below 50 nm should be feasible for a gap height of 150 nm. However, it is important to note that the simulation software assumes the nitride to be a perfect barrier, disregarding any diffusion through

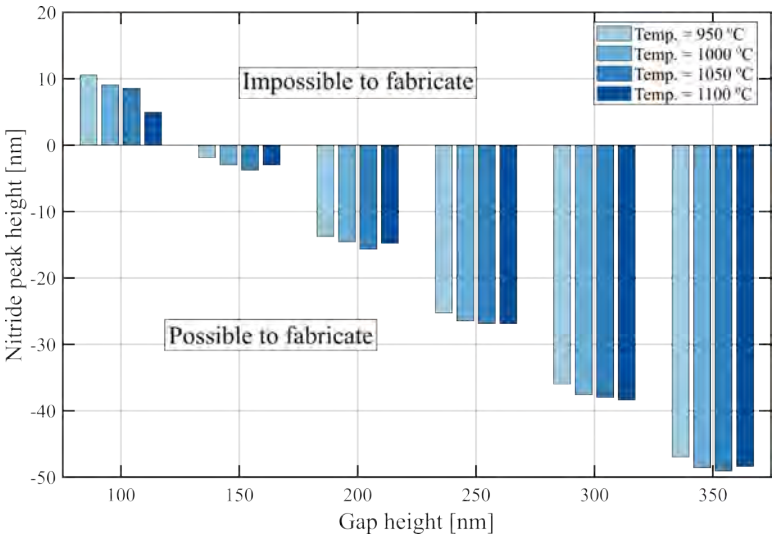


Figure 3.14: Results obtained from a nitride peak study, varying the oxidation temperature and the gap height. The insulating oxide thickness and nitride thickness were maintained at a constant value of 400 nm and 50 nm, respectively.

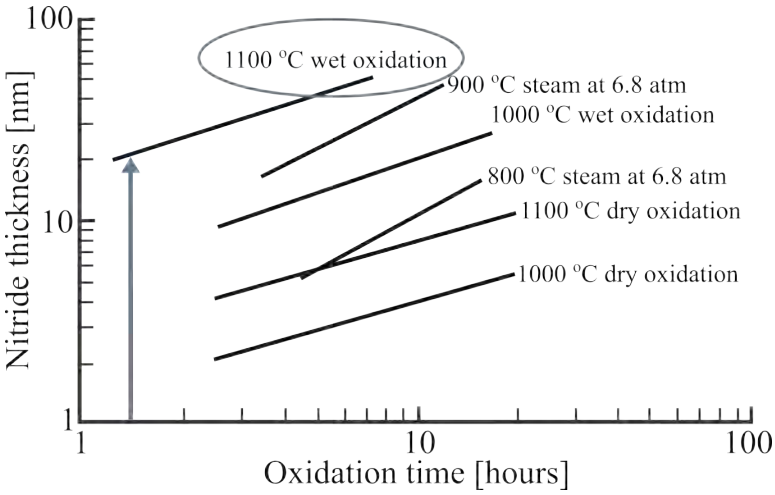


Figure 3.15: Graph showing the minimum required nitride thickness relative to the oxidation time. Relations are shown for different temperatures for both wet and dry processes. The figure is reprinted from [90].

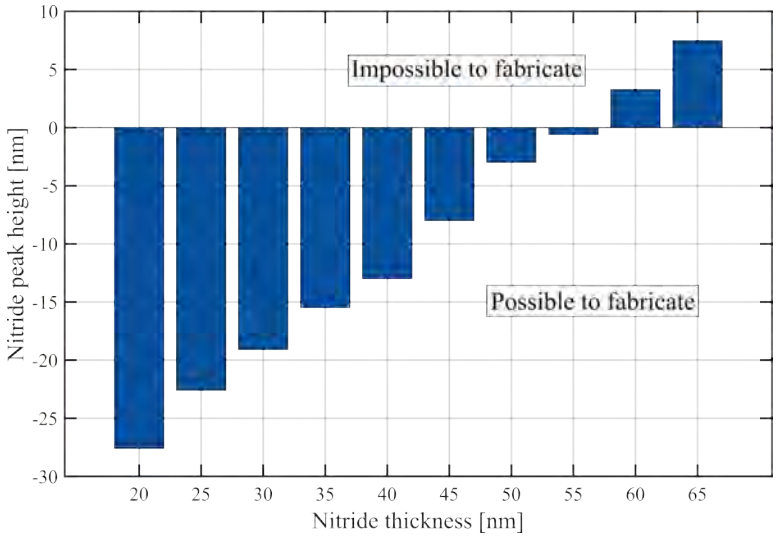


Figure 3.16: Results of the nitride peak simulation, varying the nitride thickness. The temperature and the insulating oxide thickness were kept constant at 1100 °C and 400 nm, respectively.

the nitride layer. As a result, the simulations may predict successful fabrication even with extremely thin nitride layers, which may not be practically achievable.

The final study involved varying the thickness of the insulating oxide layer. While the primary purpose of this layer is to withstand the applied voltages during device operation, this study aimed to establish fabrication limits for device dimensions. Consequently, investigations were also carried out using relatively small oxide heights.

The simulations were conducted with a fixed nitride thickness of 55 nm and wet thermal oxidation at 1100 °C, resulting in a gap height of 150 nm. The results are displayed in Fig. 3.17, indicating that a reduction in the insulating oxide thickness leads to an increase in the final nitride peak height. This can be attributed to the shorter diffusion path for oxygen molecules during the LOCOS step leading to decreased oxidation time. It should be noted that despite significant variations in the insulating oxide thickness, the peak height only exhibits minor fluctuations of a few nanometers. In all cases the magnitude of the nitride peak exceeds −5 nm, which represents an extremely narrow margin during the fabrication process. Consequently, even for the largest simulated insulating oxide layers, none of these cases can guarantee successful fabrication.

In summary, the simulation study indicated that varying the oxidation temperature had a small impact on the nitride peak height. For an insulating oxide thickness of 400 nm and a nitride thickness of 50 nm, a gap height of

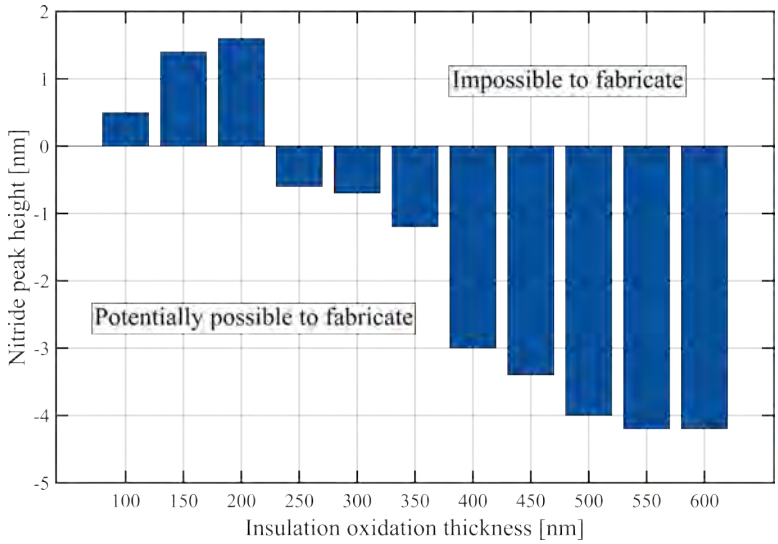


Figure 3.17: Results of the simulation study, where the thickness of the insulating oxide was varied. The temperature was constant at 1100 °C, while the nitride thickness and gap height was 55 nm and 150 nm, respectively.

150 nm showed theoretical potential for successful fabrication. Nevertheless, minor deviations during processing can impede this outcome, necessitating a further increase in the gap height to minimize the risk of nitride protrusion issues.

The second study investigated the influence of the nitride thickness, while maintaining constant values for insulating oxide thickness and gap height. The results showed that the nitride thickness significantly affects the achievable designs. To prevent protrusion-related problems, a nitride thickness below 50 nm is recommended for a gap height of 150 nm, while theoretically a thickness of 50-55 nm should be feasible to fabricate. Thus, achieving successful devices with these dimensions requires meticulous process control.

Contrary, the study on insulating oxide thicknesses revealed minor variations in the nitride protrusion heights, even when varying the oxide thickness by hundreds of nanometers. Consequently, the insulating oxide thickness should be selected so the main priority is the layers ability to withstand the voltage applied to the final device.

In conclusion, the combination of nitride thickness and gap height showed the most significant impact on successful device fabrication using the single LOCOS process. To validate the simulations, a device was subsequently fabricated using a single LOCOS process with a target insulating oxide thickness of 400 nm, and a target nitride thickness of 55 nm. These parameters represent the boundary of what is achievable based on the simulations. The desired gap height was sat to 137 nm, based on the design of the LapMUT array.

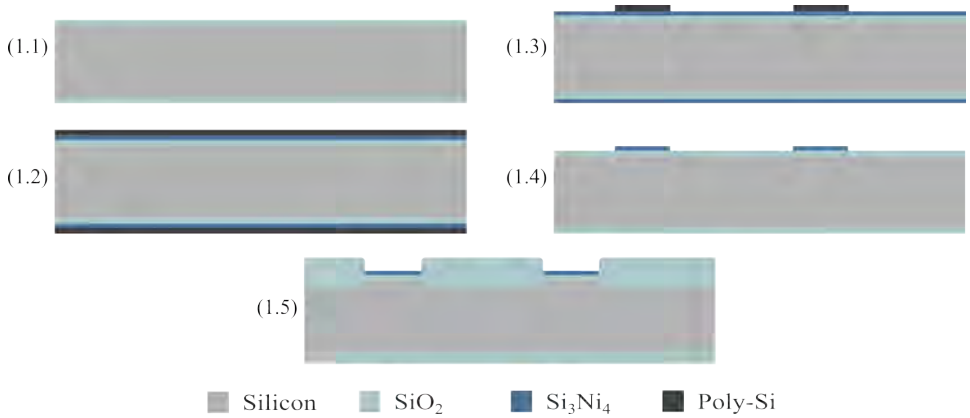


Figure 3.18: Process flow of the single LOCOS process fabricated as a part of the study on nitride protrusions.

3.3.2 Fabrication Study

Based on the simulations a batch was fabricated using the single LOCOS process for the LapMUT-B design.

An overview of the process flow is provided in Fig. 3.18, while a detailed process flow can be found in Appendix J.1. The fabrication process was started by RCA cleaning the wafer, followed by the growth of an oxide layer with a thickness of 394 nm, as shown in step (1.1). Subsequently, a nitride layer and a poly-silicon layer were deposited using Low Pressure Chemical Vapour Deposition (LPCVD) furnaces, resulting in layer thicknesses of 63 nm and 97 nm, respectively. The grown layers are illustrated in step (1.2). As mentioned above exact thickness control can be tedious when fabricating in nano- and micro-scale, leading to deviations from the target thickness of the layers. For this batch, it was intended to grow a 400 nm insulating oxide layer with 55 nm deposited nitride and 100 nm deposited poly-silicon. Despite of these thickness variations, the processing was continued.

Prior to the lithography step, a dose test was conducted on a test wafer to ensure an optimal result. Details regarding the optimized process parameters are provided in Appendix J, Section J.1. Fig. 3.19 displays a microscope image of the structure after lithography, with the insert showcasing a cell radius of 20.5 µm as the design specified. A stylus profilometer was used to check the topography, ensuring a successful lithography process.

Following the lithography process, the next step involved etching the poly-silicon, corresponding to step (1.3) in Fig. 3.18. The wafers were submerged into a wet poly-silicon etch solution composed of HNO_3:BHF:H_2O in a 20:1:20 ratio. This etchant has a prescribed etch rate between 100 nm/min and 200 nm/min, depending on the doping level [91]. Since the etch rate in nitride is zero, the main concern during over etching was to avoid under etching of the defined structures. To address this, an etch time of 2 min

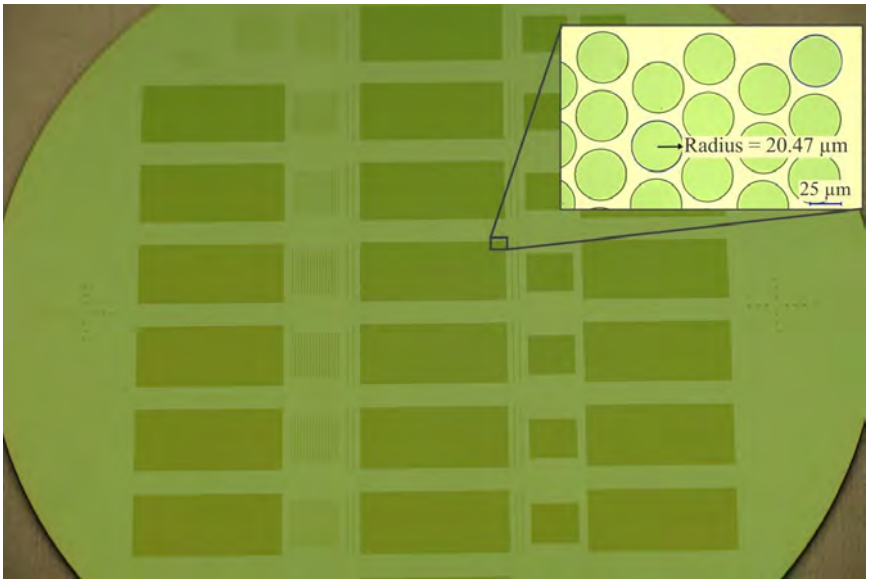


Figure 3.19: The image displays the wafer following the lithography process. The inset showcases a measurement of the cell radius, confirming the use of optimal lithography parameters.

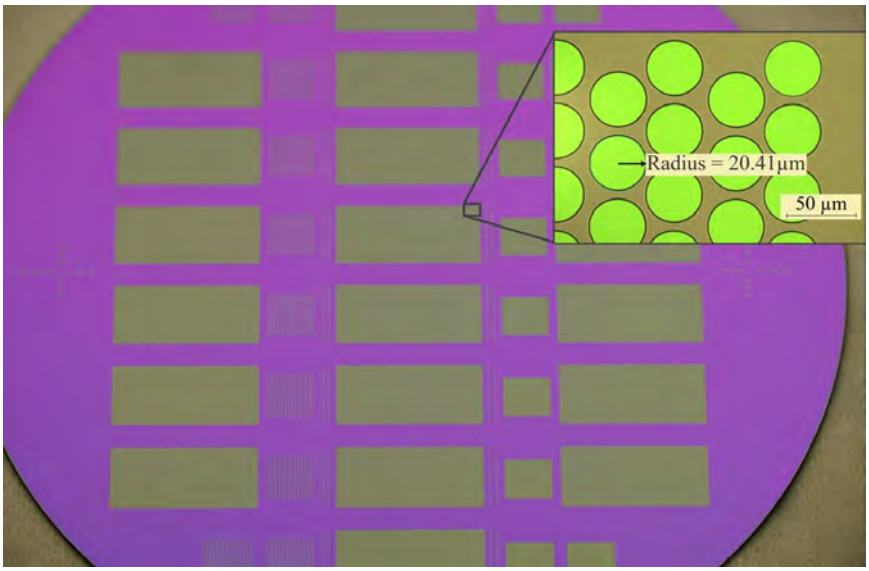


Figure 3.20: Photo and microscope image taken after the poly-silicon etch process, showing the bright purple color of the underlying nitride layer.

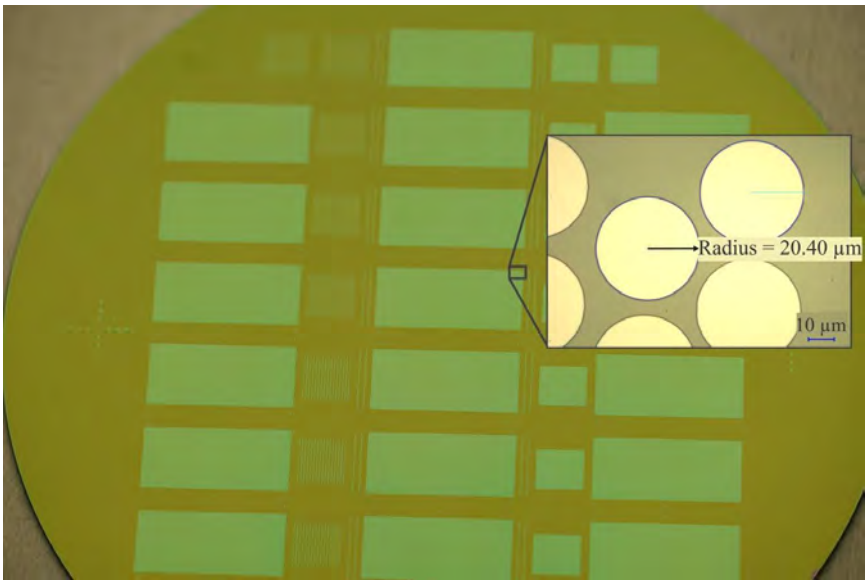


Figure 3.21: Photo of the wafer taken after the nitride etch step. The cell radius was monitored by measurements using the optical microscope, which is shown in the insert.

30 s was employed to ensure removal of any residual poly-silicon between the structures while minimizing the risk of under etching. The wafers were inspected using an optical microscope measuring the cell radius. Additionally, a stylus measurement was performed to examine the height profile of the structures. Fig. 3.20 displays an image of one of the wafers along with the corresponding optical microscope image, showcasing the nitride layer's bright purple color.

The resist was subsequently removed using an oxygen plasma for 50 min. Following this step, both an optical microscope and a stylus profilometer were employed to inspect the wafers, ensuring complete removal of the resist before continuing the processing.

The nitride layer was subsequently etched using a wet solution of 85 wt% H_3PO_4 heated to 160 °C. The etch rate was estimated to be 26 Å/min [91], and considering previous results in the research group, an etch time of 47 min was selected, including a significant over etch to ensure no residual nitride was left between the structures. The result is shown in Fig. 3.21, where a color change is observed around the structures. The insert in the figure confirms that the cell radius was preserved during the etch step.

To complete the structuring of the nitride layer, the poly-silicon mask was removed using the same wet etchant as before. This is illustrated in Fig. 3.18 step (1.4). However, this task was challenging, requiring the wafers to be submerged multiple times, resulting in an extended etch time of 5 min. Due to the presence of the Buffed HydroFluoric acid (BHF) compound in the

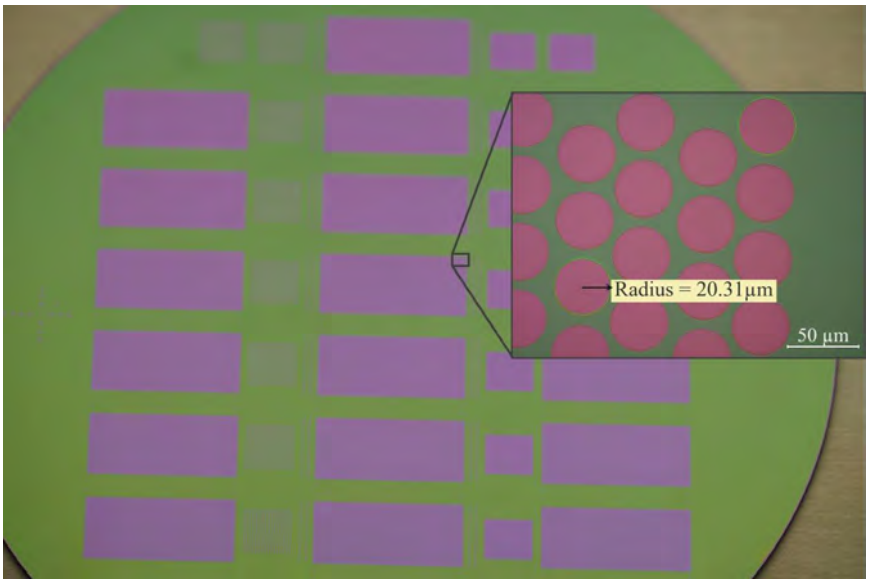


Figure 3.22: Photo of the wafer after removing the poly-silicon mask, illustrating the purple color of the nitride acting as a masking layer on top of the cells. The inserted microscope images was utilized to measure the cell radius.

etchant, part of the insulating oxide layer was unintentionally etched during this step. The stylus profilometer measured a height of 85.5 nm, which corresponds to the 63 nm of deposited nitride and an over etch of 22.5 nm into the oxide layer. This should be accounted for when calculating the processing time for the subsequent LOCOS step. Fig. 3.22 shows the purple color of the nitride in the structured areas, while the insert demonstrates a slight reduction in cell radius after finalizing the nitride mask definition.

The final step in the fabrication process was to perform the LOCOS step, as illustrated in Fig. 3.18 step (1.5). Prior to oxidation, the wafers underwent a piranha cleaning procedure followed by an RCA clean, where the HydroFluoric acid (HF) cleaning steps were omitted to prevent additional removal of the insulating oxide layer. The height of the post-oxide was calculated using Eq. (3.6). However, due to the over etch into the insulating oxide the target height was adjusted resulting in

$$h_{\text{post}} = \frac{(137\,\text{nm} + 63\,\text{nm} + 22.5\,\text{nm})}{0.56} + 394\,\text{nm} - 22.5\,\text{nm} = 769\,\text{nm}. \quad (3.18)$$

The oxidation time required to achieve the desired oxide thickness was determined using an in-house developed script that fits the Deal-Grove model [85] to data extracted from the clean room furnace employed for that specific oxidation step. The process was conducted in a wet environment at 1100 °C. After analysis, the oxidation time was determined to be 73 min, which, based on measurements on a test wafer, corresponds to an oxide

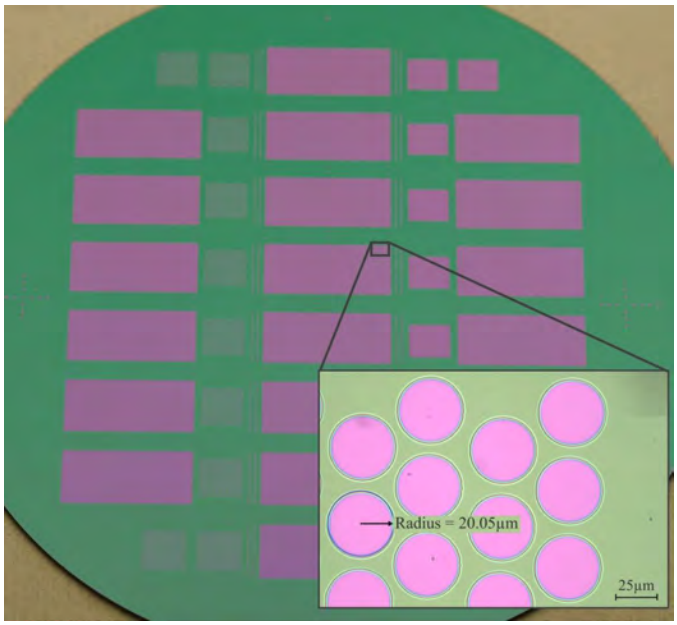


Figure 3.23: Image of the wafer after the LOCOS step defining the cavities. The microscope image shows a reduction in cell radius compared to the design.

thickness of 663 nm. The measured thickness on the test wafer after oxidation was 657 nm. This slight difference may be attributed to day-to-day variations in the furnace performance, highlighting the challenges involved in precise parameter control when performing nano-scale fabrication.

Fig. 3.23 shows an image of the wafer after the LOCOS step, where the inserted microscope image reveal a slight reduction in cell radius when compared to the initial design. According to the simulation study, the parameters investigated in this study push the limits of what can theoretically be fabricated. The stylus profilometer outline shown in Fig. 3.24 highlights the presence of spikes with a height of 32 nm, which are caused by protruding nitride. These relatively large protrusions result from the cumulative effect of minor aberrations and uncertainties encountered during the various fabrication steps. This demonstrates the complexity of fabricating devices with a small tolerance for variations. Furthermore, it is important to consider variations across the wafer, as the central arrays may exhibit no nitride protrusions, but if even a few of the outer arrays have slight protrusions, fusion bonding becomes infeasible.

After the LOCOS step, the wafer underwent characterization using Atomic Force Microscope (AFM) and Scanning Electron Microscope (SEM). The results obtained from the AFM scan are presented in Fig. 3.25, where 3.25a shows an AFM images of the scanned area, while 3.25b depicts the profile across the scanned area. The visible protruding nitride spikes, measuring

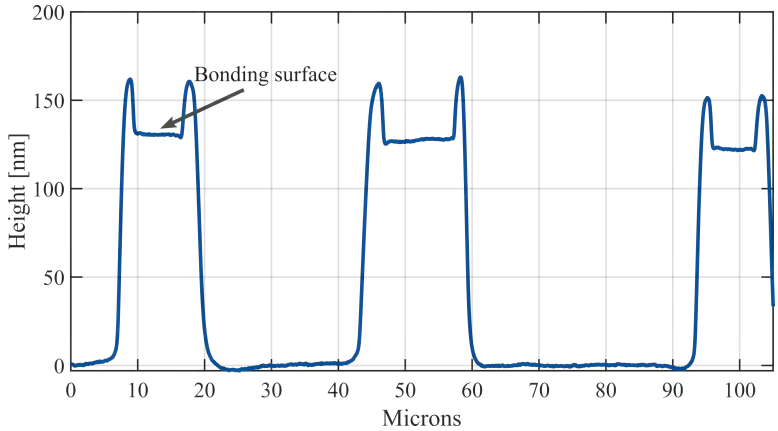


Figure 3.24: Results from a stylus profilometer measurement performed after the LOCOS step. Protrusions with a height of 32 nm are shown above the surface of the bonding area.

25.5 nm in height, are observed alongside the area intended for bonding. This observation serves as a clear illustration of the problem hindering fusion bonding.

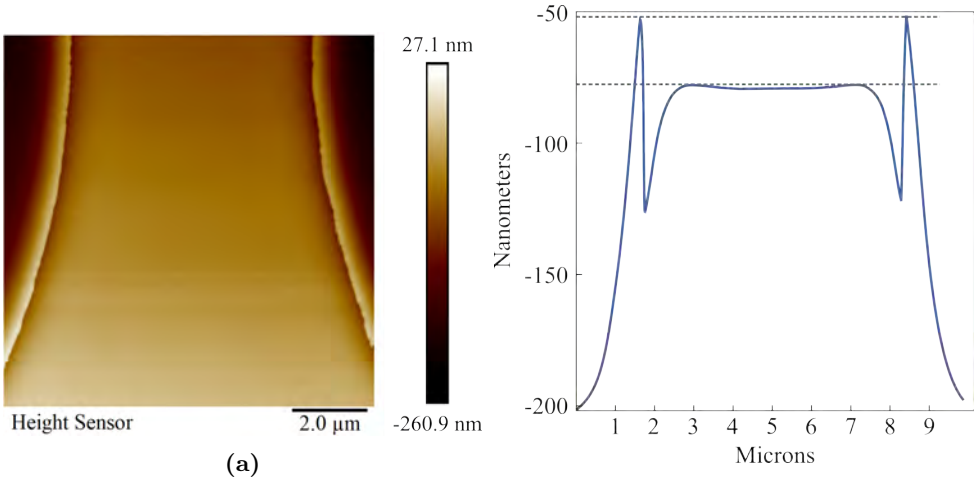
The results of the SEM images are presented in Fig. 3.26. Fig. 3.26a provides an overview images showing a top-down view of multiple cells, revealing a shadow-like feature at the periphery of the cells. This shadow suggests delamination of the nitride in those regions. This observation is further confirmed by the cross-sectional image in Fig. 3.26b, where it is evident that at the edge of the cavity, the nitride rises to such an extent that it starts to delaminate from the underlying oxide layer.

In summary, the simulation study revealed that certain structures, by design, are not feasible to fabricate. The key parameters to be taken into account during the design phase are the thickness of the nitride layer combined with the target gap height. Moreover, the fabrication process demonstrated the challenges associated with structures falling within the theoretical "gray zone" of feasibility, where even minor aberrations can significantly impact the fabrication outcome when working with small error acceptance limits.

3.4 Cavity Study

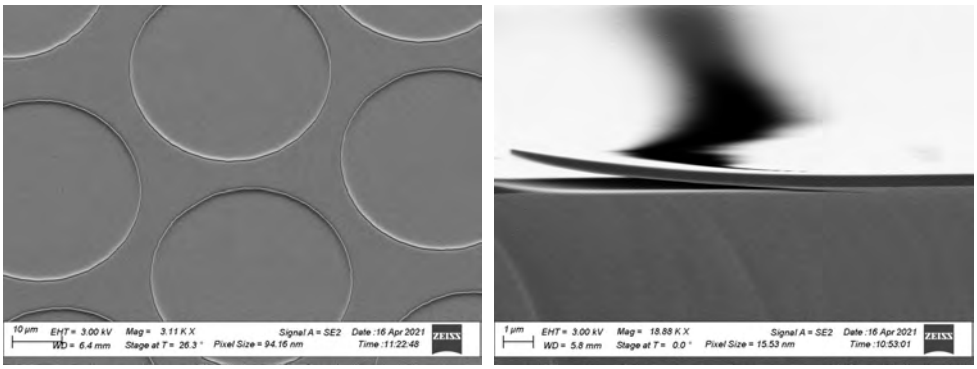
A cavity study was conducted in collaboration with M.Sc. Søren W. Gjaldbæk under supervision of the author. This study aimed to investigate the three different fabrication methods explored as part of this Ph.D. project, namely the double LOCOS, the RIE process and the maskless LOCOS. The simulation software Athena (Silvaco, California) was employed for this purpose.

Based on a preliminary study indicating minimal influence from the cell



(a) **(b)**

Figure 3.25: Results obtained from an AFM scan performed on the wafer after the LOCOS step. **(a)** Shows an image, where the bright color at the edge indicate a height difference. **(b)** Illustrates the cross-sectional measurement, verifying the spikes shown on the stylus profilometer measurement. These spikes hinders fusion bonding.



(a) **(b)**

Figure 3.26: SEM images of the wafer after the LOCOS step defining the cavities. **(a)** Shows a top view of the circular cells, while **(b)** shows a cross-sectional image depicting delamination of the nitride layer, which prevents fusion bonding.

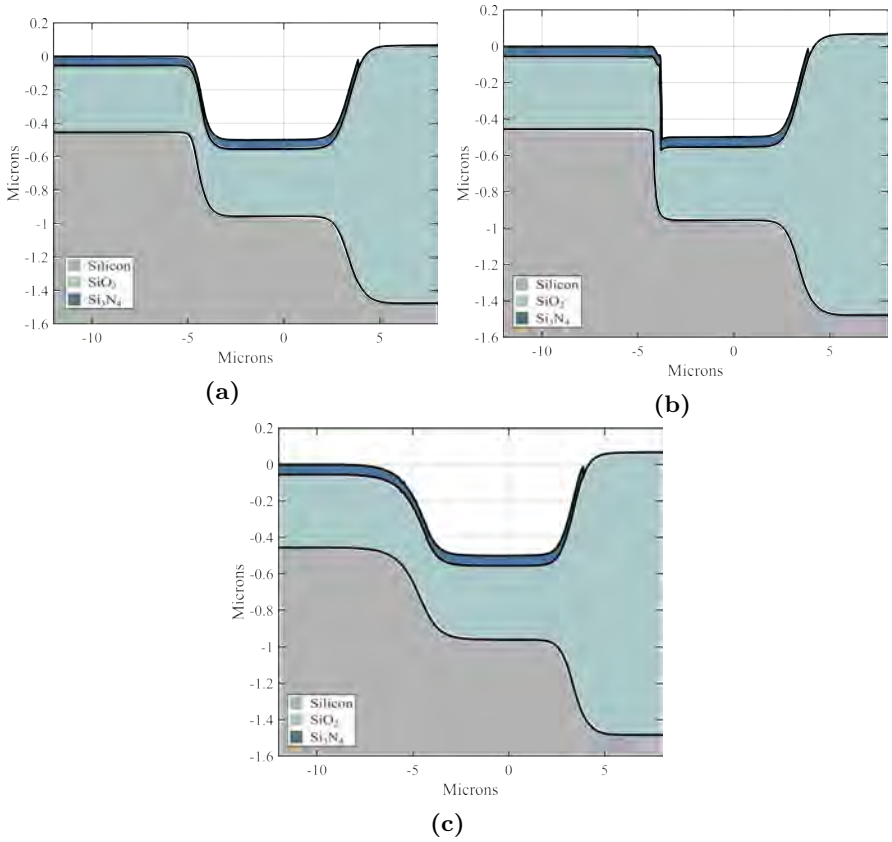


Figure 3.27: Simulation results showing the outline of the finalized bottom substrate for the three different fabrication processes: **(a)** the double LOCOS process, **(b)** the RIE process, and **(c)** the maskless LOCOS process.

radius, a radius of 12 µm was used for all simulations to reduce computation time. The simulations resulted in a consistent gap height of approximately 70 nm for all three fabrication methods. Additional information regarding the simulations can be found in the code provided in Appendix I.

The resulting bottom substrates for the three fabrication processes are presented in Fig. 3.27. A visual inspection of the structures reveals noticeable differences in the cavity outlines among the three cases. The study focused on monitoring three critical parameters: expansion of the cell radius, reduction in the bump radius, and the nitride peak height, which determines the feasibility of the fabrication processes.

To determine the expansion of the cell radius, the point at which the height of the bonding area changed by more than 1 % was identified. This is equivalent to the approach employed in [41, 89]. Areas below this point might not bond to the top plate and thereby contribute to the active cell area instead, affecting the resonance frequency. Therefore, it is important to consider this when designing the mask layout.

Table 3.4: Comparison of simulation results from the cavity study performed in Athena (Silvaco). The three different fabrication processes were compared for the cavity widening, bump reduction and the nitride peak height.

	Δ Radius, a [µm]	**Δ Bump,** a_{bump} [µm]	**Δ Nitride peak** [nm]
Double LOCOS	1.3	-1.1	-136
RIE LOCOS	1.6	-0.3	-110
Maskless LOCOS	2.2	-5.0	-131

The second parameter of interest was the reduction in the bump radius. This parameter was determined by identifying the 1 % height deviation relative to the center of the bump (shown in the left side in the structures in Fig. 3.27). A consistent bump height is of interest, since changes can impact the electric field within the cavity, influencing the forces that pull down the top plate.

The last extracted parameter is the nitride peak height, as explained in Section 3.3. The peak height was determined by measuring the height between the end of the nitride layer and the post oxide region serving as the bonding area.

Table 3.4 summarizes the derived parameters for the three fabrication processes. Common to all three processes were the feasibility of fabrication, as indicated by the nitride peak height, which is sufficiently far from the bonding area, minimizing the risk of protrusion issues due to minor fabrication aberrations. The simulation results also demonstrated a cell radius expansion ranging from 1.3 µm to 2.2 µm, depending on the fabrication process. Additionally, a reduction in the bump radius was observed, ranging from -5.0 µm to -0.3 µm.

Fig. 3.28 provides a comparison of the final oxide structures. Notably, the RIE process exhibits a well-defined bump corner with a steeper sidewall profile compared to the two oxidation-based processes. The maskless LOCOS process, characterized by two consecutive long oxidation steps, produces the most rounded profile, as anticipated.

This study emphasizes that while all three cases involved the use of a LOCOS process to form the cavities, the outline of the bump before the LOCOS step significantly influenced the overall shape of the final cavity structure. Furthermore, it is important to consider the increase in cell radius when designing the mask layout.

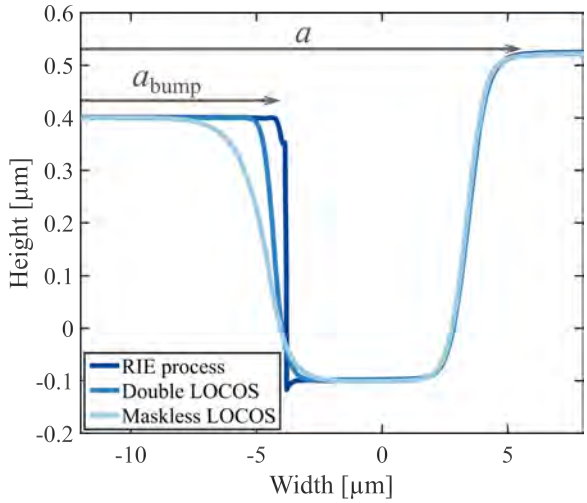


Figure 3.28: Comparison of the extracted final oxide profile for the three fabrication processes.

3.5 Chapter Summary

This chapter presented an overview of the design process and associated simulations for CMUTs. The first section outlined the external design specifications and proceeded with a step-by-step explanation of the design phase. The specific focus was on the Lin384 design, where initial estimates were obtained using analytical expressions. Subsequent simulations using COMSOL and OnScale refined and validated the design parameters, ensuring they met the specified requirements. The resulting parameters for the Lin384 design, as well as the two LapMUT designs, were summarized in Table 3.3.

After determining the parameters, the mask layout was introduced, and the different array designs and their respective locations were specified.

Furthermore, two simulation-based studies were conducted. The first study focused on a single LOCOS process and the nitride layer protruding above the post-oxide surface, which serve as the bonding area. The results revealed that certain structurally design configurations are infeasible to fabricate. The critical parameters to monitor were identified as the thickness of the nitride masking layer and the gap height. To exemplify the sensitivity of the fabrication process to minor deviations, a batch was fabricated, highlighting the challenges faced when operating within a theoretical "gray zone".

Finally, a simulation-based cavity study investigated the structure of the final bottom substrates and compared the outcomes of the three different fabrication processes. It was observed that the cell radius increased in all three cases. Based on the analysis of nitride peak height, it was concluded that fabrication is feasible for all three fabrication techniques. Additionally,

it was emphasized that the increased cell radius should be considered during the mask layout design to achieve the intended radius in the final device.

CHAPTER 4

Process Development

The content of this chapter is partly based on the work presented in Paper B and Paper C, and focuses on bottom electrode separation for silicon based CMUT fabrication processes. The CMUTs in this chapter are utilized using a LOCOS and fusion bonding process as demonstrated in [36]. As part of the process development the author participated in a course at Logitech Ltd (Glasgow, UK), which has provided details for this chapter.

Linear 1D CMUT array have been fabricated using various methods during the last decades. These methods includes sacrifical release, fusion bonding, and anodic bonding. Typically, 1D arrays have been fabricated with a solid bottom substrate and separated top electrodes [16, 31, 36, 40]. However, due to the limited space in a laparoscope, an alternative method for electrically contacting the transducer elements is required.

Previous studies has successfully demonstrated backside contacting of CMUTs obtained by through-silicon vias filled with poly-silicon and by employing air-filled trenches as insulation [24, 25]. Furthermore, a reversed fabrication process using sacrificial release was proposed in 2005 in [26].

The work described in this chapter applies a state-of-the-art high aspect ratio dry etching process called Deposit, Remove, Etch, Multistep (DREM). The process enables bottom electrode separation and utilizes the top electrode as a common ground. Furthermore, this structure allows for integration using the substrate as a via architecture and contact point for BGA bonding. This bonding technique mitigates parasitic contributions from wire bonds, requires less horizontal footprint and is suitable for large scale production. Additionally, the use of an external electromagnetic interference shielding can potentially be omitted, thus further reducing the necessary

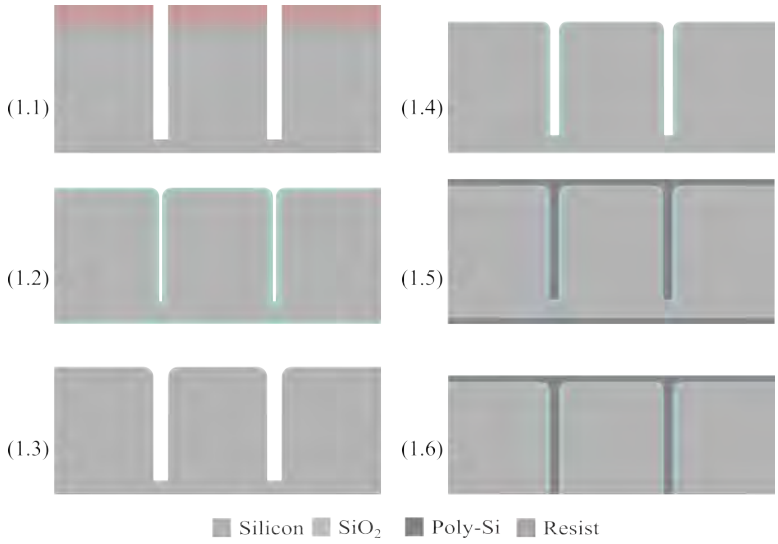


Figure 4.1: Process flow illustrating the fabrication process for bottom electrode separation employing a combination of oxide and poly-silicon plugs. Notice, the figure is not to scale and the DREM trenches were only etched approximately 1/5 into the substrate. The figure is reprinted from Paper B.

space.

The DREM process was initially introduced in [47] and offers a very high aspect ratio silicon etch of more than 1:50. This ratio is feasible due to the high etch selectivity towards conventional photoresist and relies on a RIE process. To insulate the bottom electrodes from each other, a thin oxide layer was thermally grown. Subsequently, the trenches can either left air-filled or plugged by various materials.

The appended Paper C provides an example of a successfully fabricated CMUT based probe utilizing air-filled trenches insulating neighboring bottom electrodes from each other. Mechanical stability was obtained by anodic bonding a glass substrate to the back of the wafer.

However, this method is not directly suitable for fabrication of a laparoscopic probe as it prevents direct electrical backside contacting. Therefore, poly-silicon was used for trench filling as an alternative to ensure mechanical stability of the substrate throughout the subsequent processing steps. After the trenches was defined, lapping was employed as a substrate thinning technique. It is known as a fast and uniform method used to remove thick layers of silicon and other materials.

4.1 Bottom Electrode Separation

An illustration of the process flow that combines the DREM and lapping techniques for separating the bottom electrodes is provided in Fig. 4.1.

The element separation and insulation process consists of six main steps. Initially, a conventional photolithography was used to define the width of the DREM trenches (step 1.1). These were subsequently etched into the substrate applying the procedure described in detail in the following section. After etching the trenches, the resist was removed, and the corners of the trenches were rounded through an oxidation process (step 1.2). Furthermore, this oxidation step decreased the scallop depth caused by the Bosch based DREM process [92]. Step (1.3) depicts the silicon substrate after removal of the oxide, leaving the trenches with more smooth sidewalls. Next, an insulating oxide layer was grown (step 1.4) followed by deposition and trench filling using undoped poly-silicon (step 1.5). Finally, the trenches were separated through a mechanical lapping process, which removed material from the backside of the wafer until the trenches were visible (step 1.6).

To ensure mechanical stability during wafer thinning, it is preferable to perform the thinning process after bonding the top plate to the substrate. The formation of CMUT cells can be carried out either before etching the trenches, as demonstrated in Paper C, or after trench filling, and before substrate thinning, as intended for laparoscopic applications which is described in Paper B. However, due to external factors, fabrication of the laparoscopic transducer was terminated, resulting in the CMUT cells not being implemented on the design with filled trenches.

4.2 DREM and Trench Filling

The high aspect ratio offered by the DREM process facilitates separation of the bottom electrodes used for backside contacting without significantly increasing the width of the kerf. Two different test designs was employed during the optimization process: one with 2.5 µm wide trenches and another with double the width at 5 µm.

The DREM process, illustrated in step (1.1) of Fig. 4.1, relies on a dry etch Bosch process. A more detailed process flow is depicted in Fig. 4.2. Initially, a silicon wafer was patterned using conventional photoresist. Subsequently, the silicon was isotropically etched employing a SF_6 plasma. In the third step, a FC passivation layer was deposited using a C_4F_8 gas. The bottom of the trenches were cleared of the passivation layer by applying a directional argon plasma, as shown in step four. By optimizing the removal step, the passivation layer at the bottom of the trenches could be removed without affecting the masking resist layer. This cycle can then be repeated until the desired depth is achieved, as illustrated in step five and six, corresponding to two and three cycles, respectively.

A more parameter specific process overview is provided in Fig. 4.3, showing the gas flow, platen power and process time for the three main

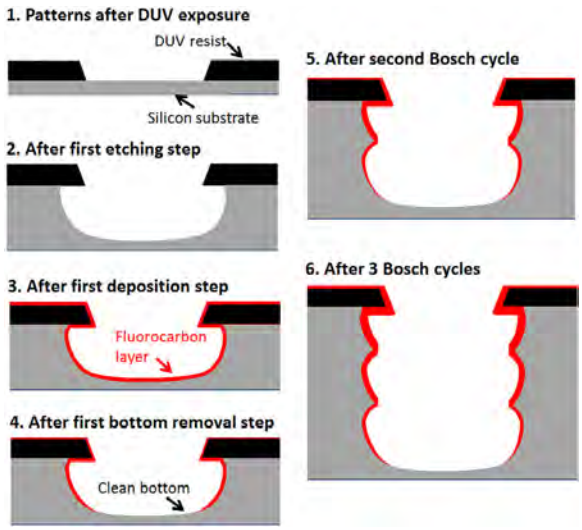


Figure 4.2: Structural overview of the process steps involved in the DREM process. The figure is reprinted from [47].

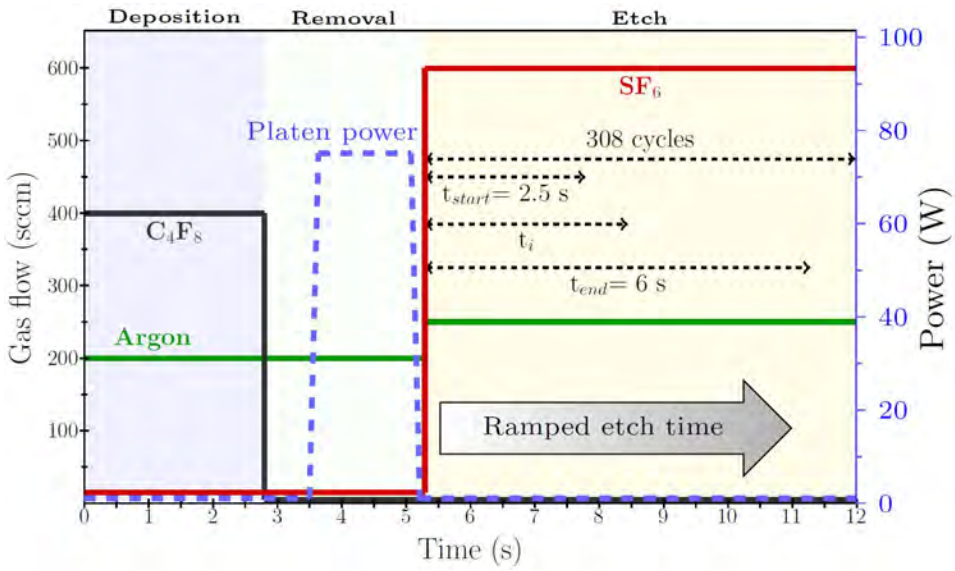


Figure 4.3: Overview of the gas flow, platen power and process time applied in the three individual steps of the DREM process: deposition, removal and etch. The figure is reprinted from Paper B.

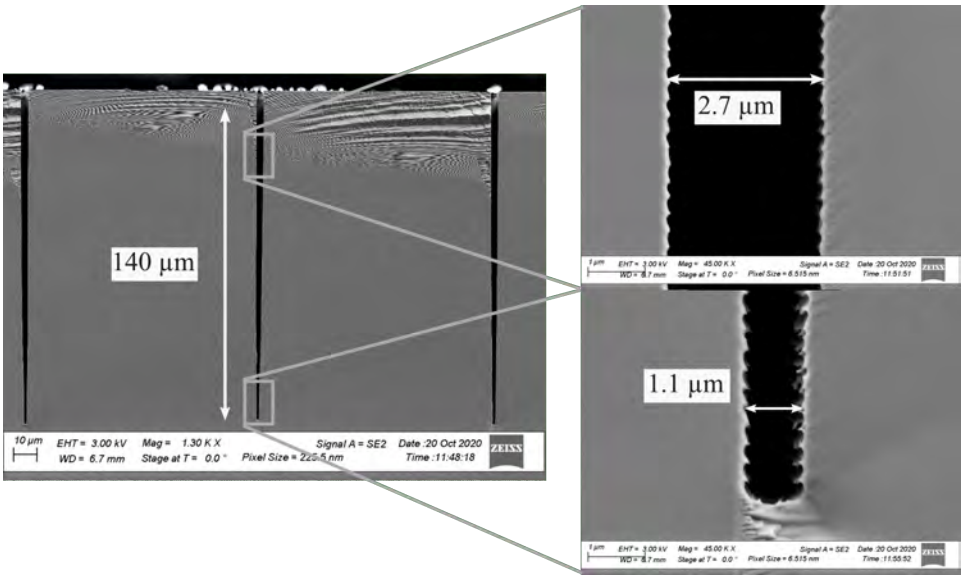


Figure 4.4: Cross-sectional SEM images of the trenches after removal of the resist. The image to the left shows the full trench with a depth measured to 140 µm, while the width varied from 3.2 µm at the top to 1.1 µm at the bottom. Furthermore, the images to the right compares the scallop size at the top and bottom of the trench.

steps: deposition, removal and etch. The chuck temperature was set to the lowest value allowed by the equipment, which, in this case was −19 °C. During the *deposition* step, the platen power was minimized to prevent erosion. A C_4F_8 plasma was used to deposit a FC passivation layer, for a total step time of 2.8 s. After this duration, the C_4F_8 gas was turned off, leaving a low-pressure (5 mTorr) argon plasma in the chamber. The *removal* step required an increased platen power of 75 W with 325 V DC for 1.6 s in order to clear the FC passivation layer at the bottom of the trenches. The total time for the *removal* step was 2.5 s. Finally, the *etch* step utilized a SF_6 based plasma with a gas flow of 600 sccm. A total of 308 cycles were applied. The etch time was gradually increased from 2.5 s to 6 s to ensure consistent scallop sizes along the entire length of the trenches. In the case of air-filled trenches, as demonstrated in the appended Paper C, the trench processing was halted after this step. Further details about the air-filled process are provided in Section 4.3.2.

A SEM image of the resulting trenches after the DREM process is presented in Fig. 4.4. The depth was measured to 139.6 µm, with the width varying from 3.2 µm at the top to 1.1 µm at the bottom, indicating a tapered outline. Furthermore, a trench widening of 0.7 µm was observed compared to the designed width of 2.5 µm. The images to the right compares the scallop size at the top and bottom of the trench.

Following the trench etching process, corner rounding and reduction of

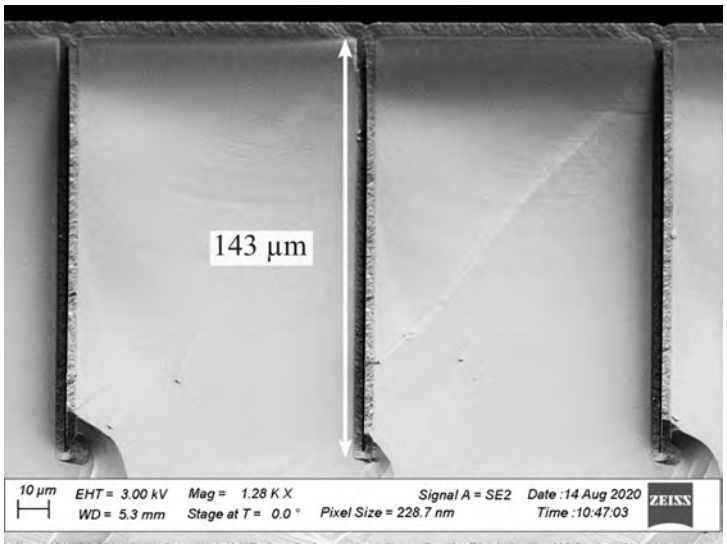
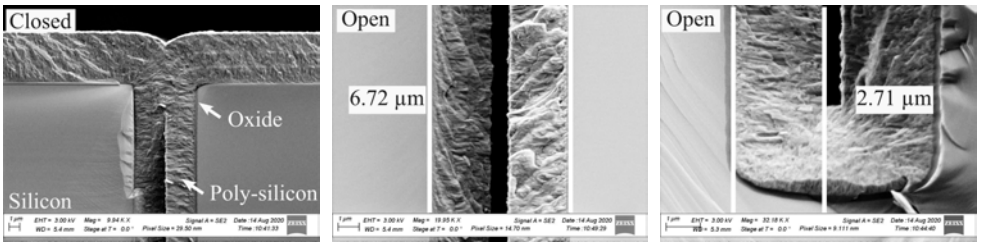


Figure 4.5: SEM image showing a full trench with an insulating grown oxide layer and a deposited poly-silicon. The depth was measure to 143 µm. The figure is reprinted from Paper A.

the scallop size were performed subsequent to removal of the resist. This is illustrated in (step 1.2) in Fig. 4.1. The corner rounding and scallop size reduction was achieved by growing a 500 nm wet thermal oxide at a temperature of 1100 °C. The oxide was subsequently removed using a BHF with wetting agent to enable etching of the high aspect ratio structures. The is shown in step (1.3).

Step (1.4) in Fig. 4.1 demonstrates the growth of the insulating oxide, designed to withstand the applied voltages and prevent transducer breakdown during operation. The target thickness of the oxide was 200 nm, and it was obtained through a dry thermal oxidation process at 1100 °C. Notice, that the two oxidation steps widens the trench, which is a compromise made to achieve rounded corners and smooth sidewalls, facilitating a more uniform trench filling. This filling is illustrated in step (1.5) and was utilized using undoped poly-silicon.

The final trench with an insulating oxide and poly-silicon plug is shown in Fig. 4.5. Magnified images of the top, middle, and bottom of the trench are presented in Fig. 4.6. The applied design for this process aimed for a trench width of 5 µm. However, the SEM images reveals a trench widening compared to the design, which can be partly attributed to the two oxidation steps. Table 4.1 provides the results of measurements of the trench width, oxide thickness, and thickness of the poly-silicon at the three locations along the trench. According to the theory the volumen ratio between silicon and oxide is approximately 45 %, resulting in an expected trench width of 5.66 µm. However, Fig. 4.6 reveals a trench width of 6.7 µm subsequent



(a) **(b)** **(c)**

Figure 4.6: SEM images of the DREM etched trench with an insulating oxide and filled with poly-silicon. The images show **(a)** the top, **(b)** the middle, and **(c)** the bottom of the trench. The figure is reprinted from Paper A.

Table 4.1: Measurements of the trench width, insulating oxide thickness, and thickness of the deposited poly-silicon measured at three different depths.

	Trench width [µm]	**Oxide thickness** [nm]	**Poly-silicon thickness** [µm]
Top	6.70	-	2.82
Middle	6.72	195	2.71
Bottom	6.34	228	2.71

to trench filling, which is 18.4 % wider than expected. This discrepancy is attributed to the isotropic etching process causing the scallops to be wider than the opening defined by the photolithography mask.

The depth of the trench was measured from the overview image provided in Fig. 4.5 and was found to be 143 µm. Furthermore, Fig. 4.6 reveals that the top of the trench was plugged before the middle and the bottom sections. Although corner rounding was initially introduced to mitigate this effect, it was not fully resolved, resulting in a final structure which did not achieve the intended mechanical stability. To overcome this, it is suggested to maintain a constant etch time throughout the 308 cycles, creating a more tapered profile. Subsequent application of additional corner rounding is anticipated to result in a trench that is filled from the bottom upward.

However, due to change of focus during this Ph.D. project, further optimization was not pursued. Implementation of the DREM trenches and the lapping process, was therefore exclusively performed for air-filled trenches, which is further described in Section 4.3.2.

4.3 Lapping

After trench formation a lapping process was employed for substrate thinning. Lapping is a mechanical substrate thinning method employed when flatness, parallelism, thickness and finish are crucial parameters. This process involves the use of a plate, a slurry with abrasive, and a sample.

Unlike chemical or thermal processes, lapping does not cause any chemical or thermal damage to the substrate. Additionally, lapping avoids cooling issues that can occur during long dry etching processes. It offers a higher removal rate and good uniformity control. Finally, due to the completely mechanical nature of lapping the rate will remain constant when reaching the bottom of the filled trenches.

Although lapping is closely related to grinding and polishing methods, each serves different purposes and results in varying removal rates and surface roughness. Fig. 4.7 illustrates the three different categories and highlights the differences. The first and most coarse method is grinding, utilizing a firmly bonded abrasive [93]. This method is employed when rapid material removal or flattening of the sample surface is desired. However, it can cause sub-surface damages and leaves the substrate with a relatively high surface roughness infeasible for applications like fusion bonding. The grain size of the abrasive paper are typically on the order of or larger than 50 µm.

Polishing, on the other hand, is the finest method among the three and is used for mechanical removal of thin layers of material, typically in the order of a few hundred nanometers. It leaves a little or no scratches, and is categorized as a low damage process [93]. Polishing employs a free abrasive slurry, where the grains, typically smaller than 1 µm, are mixed with a liquid. The free abrasive slurry is used in combination with a polishing cloth. This combination achieves highly smooth surfaces with low surface roughness, often less than 0.1 nm. It is suitable for applications requiring a low surface roughness wafer finish, such as fabrication of Poly-Silicon-On-Insulator (PSOI)s [39, 94]. PSOIs are in-house made SOI wafers acting as top plates for the CMUTs fabricated in recent years within this research group.

Lapping, is an intermediate technique, which also uses a free abrasive slurry similar to polishing. However, the grain sizes range from 1 µm to 50 µm. Instead of a cloth, the lapping plate is chosen based on the hardness of the substrate and can be used for brittle materials [93]. Lapping can help minimize sub-surface damage originating from wafer dicing or grinding and produces a smooth, flat, and unpolished surface on the substrate. However, the resulting surface roughness is higher than that achieved by polishing, and direct fusion bonding cannot be performed on lapped surfaces.

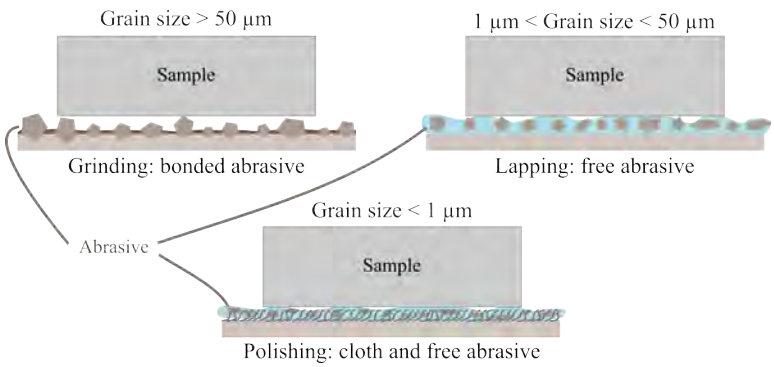


Figure 4.7: Showing the three overall categories of mechanical removal processes similar to lapping. Grinding is the most coarse method, while polishing serves the finish with the lowest surface roughness. The illustration is inspired from [95].

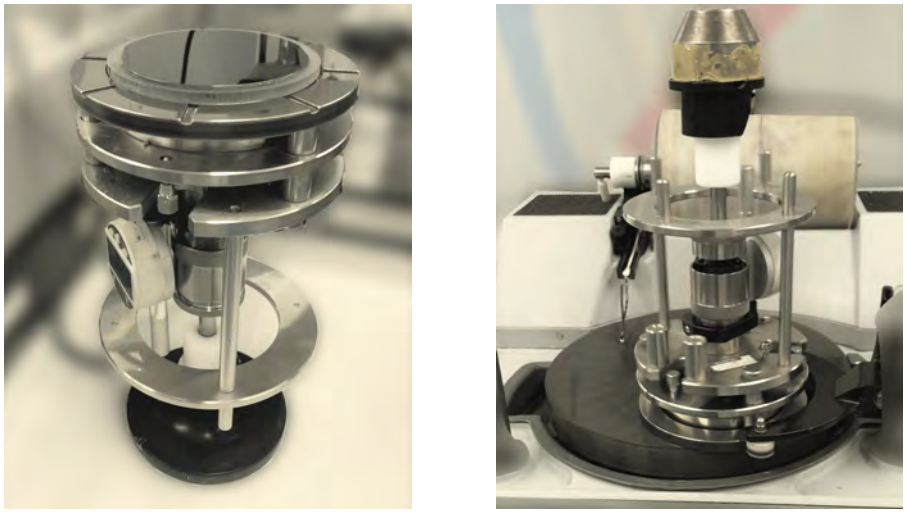
4.3.1 Method

Lapping finds widespread applications in various industries and for various materials, including III-V materials [96], silicon and SOI wafer manufacturing [97], and piezo materials [98].

The lapping equipment consists of several components. The details in this process will be further elaborated later in this section. Starting from the wafer, it is initially mounted on a glass substrate. Subsequent to wafer mounting the glass substrate is placed on a jig and secured using a vacuum. An image of this setup is provided in Fig. 4.8a. To start the lapping process, the jig is placed in the roller arm, keeping it in the correct position on top of the lapping plate, while allowing free rotation during operation. This is depicted in Fig. 4.8b. To increase the lapping rate, a loading weight is placed on top of the jig. The weight of the load also determines the rotation speed of the jig.

Fig. 4.9 provides an overview illustration of the lapping machine utilized in the process. It highlights the lapping plate, along with the slurry cylinder and the slurry feed. Additionally, the mount for the roller arm, which holds the jig, is indicated on the right side of the illustration.

To ensure a planar, optimal lapping process, the wafer mount plays a crucial role. As mentioned, the wafer was mounted on a glass substrate. A bonding jig station was positioned on a heating plate, as shown in Fig. 4.10, and the wafer was mounted onto a glass substrate using wax, which became fluid when heated. An illustration of the bonding stack is provided in Fig. 4.11. Starting from the bottom, the stack includes the bonding jig station with a glass substrate positioned on top of it. A thin layer of wax was applied on top of the heated glass substrate. Subsequently, the wafer was then placed on the wax, and a paper sheet was added to ensure that the second glass substrate exclusively serves to distribute pressure across



(a) **(b)**

Figure 4.8: Images of the jig placed **(a)** upside down, and **(b)** on the lapping plate. The left image shows the wafer mounted on a glass substrate on top, while the right image includes the loading weight, the roller arm and the slurry cylinder.

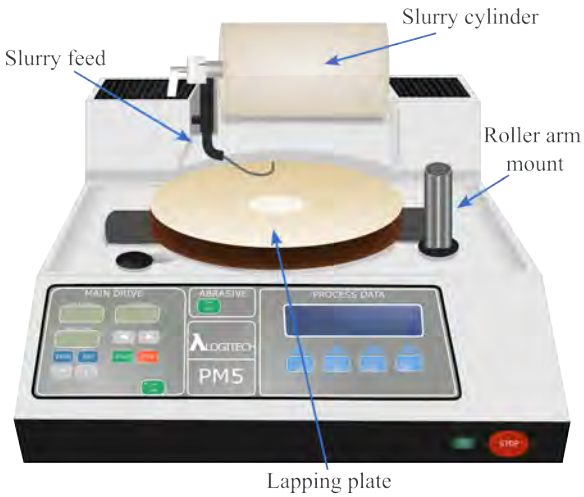


Figure 4.9: Illustration of the machine employed for the lapping process. The lapping plate is marked, as well as the slurry cylinder, the slurry feed and the roller arm mount holding the jig.

Figure 4.10: Image of two bonding jig stations used to mount the wafer onto a glass substrate prior to lapping. The bonding station is placed on to of a hot plate.

the wafer, without bonding to it. The top pin applies pressure to the stack through a pressure divider, ensuring even distribution of the wax underneath the wafer.

It is crucial for the bond quality to ensure planarity of both glass substrates, as well as avoiding air bubbles trapped in the wax. Any irregularities or air bubbles can result in a non-planar wafer, which can significantly affect the quality and uniformity of the lapping process. Visual examples of a good and a poor bond are provided in Fig. 4.12 for comparison. Demounting of the wafer was done by dissolving the wax in a heated solution of Ecoclear (provided by Logitech Ltd), which is a non-solvent cleaning fluid.

Several parameters play crucial roles in the lapping process. These parameters include the sample material hardness, plate flatness, rotational speed of the plate, load on the jig, slurry feed speed, and choice of abrasive material and grain size.

Silicon, which has a hardness of 6.5 on Mohs hardness scale, requires a cast iron plate with grooves for substrate thinning. This is the most common lapping plate materials and provides a high removal rate. The grooves assist in removing material from the interface between the lap plate and the sample. Additionally, the jig must be flat to ensure proper and uniform mounting of the sample substrate. Non-planar surfaces of the jig and lap plate will lead to decreased sample uniformity, which becomes increasingly

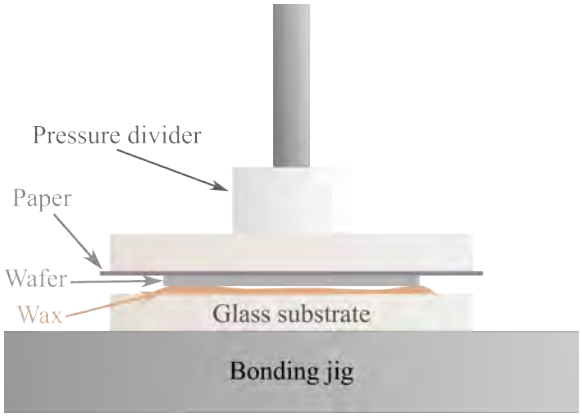
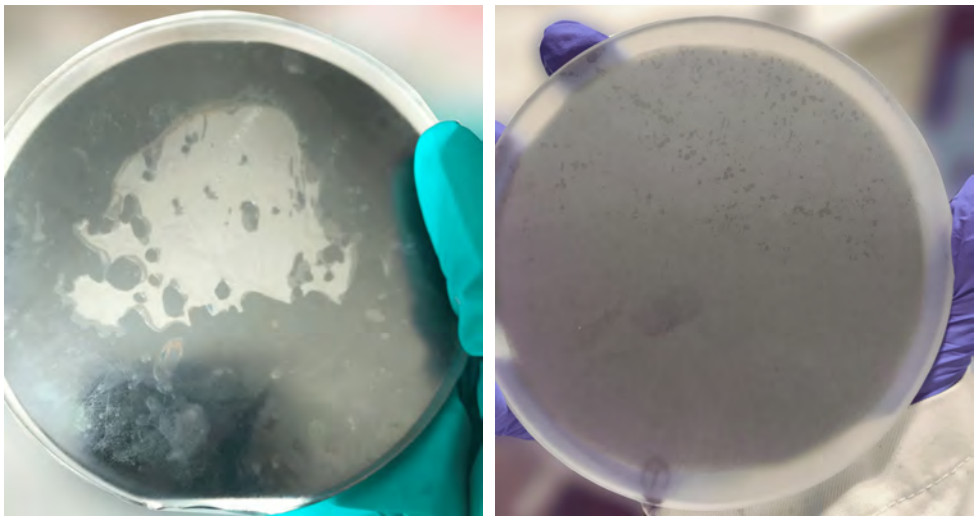


Figure 4.11: Illustrating the stack used wafer mounting onto a glass substrate prior to lapping.



(a) **(b)**

Figure 4.12: **(a)** Depicts poor bonding with trapped air bubbles, while **(b)** shows an ideal uniform bond.

important with larger sample sizes.

The material removal rate is influenced by a combination of the plate speed and the load applied on the jig. Generally, higher plate speed results in higher rate. Similarly, increasing the loading weight increases the rate. However, when lapping harder materials, the load should accordingly adjusted to maintain an adequate removal rate. Furthermore, the combination of plate speed and load can be adjusted to reduce the rate when thin layers of material need to be removed.

Another important parameter is the speed of the slurry application. An optimal feed speed ensures consistent and repeatable surface roughness results. A too high application speed leads to excess slurry on the plate, which does not change the rate and is a waste of material. Conversely, if too little slurry is applied there is a severe risk of the sample touching the plate directly, resulting in wafer damaging.

Finally, the choice of abrasive material depends on the sample material. It is crucial for the abrasive grains to be comparable or harder than the sample. Therefore, alumina oxide is commonly chosen as an inexpensive and widely used abrasive material for silicon lapping. Additionally, the abrasive material should be insoluble in the applied mixing fluid. Alumina oxide provides an excellent finish as the grains break down over time. This type of abrasive material, with a small average grain size (typically 3 µm to 9 µm), is often used as a precursor to a polishing process.

The abrasive grain size affects the material removal rate, as well as the surface finish. The publication "Effects of mixed abrasive grits in slurries on free abrasive machining (FAM) processes" [99] studied different slurries in relation to surface roughness and removal rate. The paper compares a single abrasive slurry containing a silicon carbide abrasive having a mean particle size of 22 µm with a mixed abrasive slurry. The mixed abrasive slurry contained the same concentration of 22 µm abrasives, while also including abrasive with an average grain size of 11 µm. The two slurries were compared for two different loads. Fig. 4.13 presents the results for the removal rate over a time period of 30 min. It was observed that the mixed abrasive slurry achieved a higher removal rate for both loads, with up to 38 % increase compared to employing a single abrasive slurry. Furthermore, the study confirmed that the load applied on top of the jig can be used to adjust the removal rate. It was concluded that both slurries underwent severe grain size reduction during lapping. Part of the reason of increased removal rate for the mixed abrasive slurry was attributed the presence of 11 µm grains. Since this abrasive was added to the same slurry concentration represented in the single abrasive slurry, the mixed abrasive slurry would at any given time have a higher abrasive concentration. This is also true when all larger abrasive grains were reduced in size.

Finally, the paper examined the surface roughness for both types of slurries, as well as the two different loads. Slightly higher average roughness

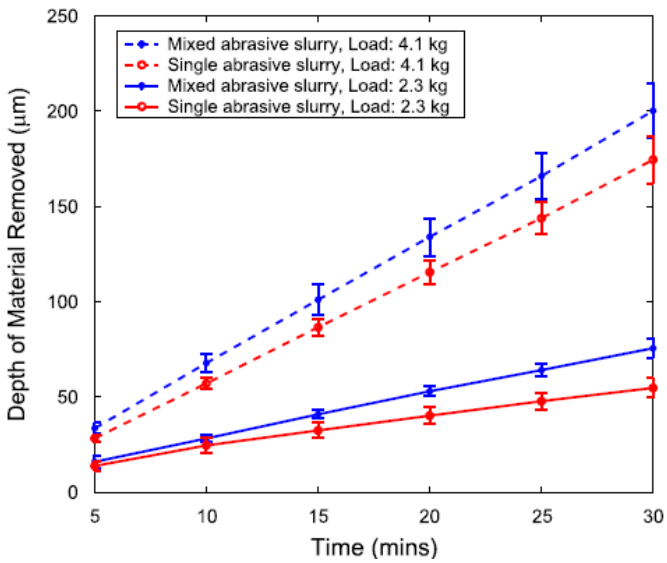
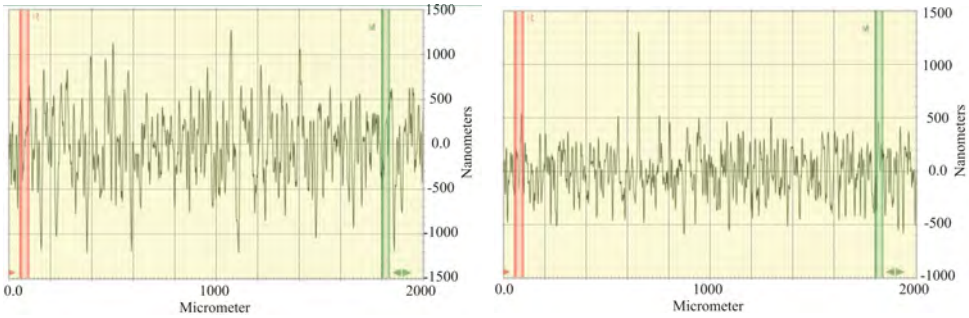


Figure 4.13: Illustrating the load and mix of abrasives effects on the material removal rate during lapping. The figure is reprinted from [99].

values were observed for the larger load (4.1 kg), with a values of 42 µm and 0.43 µm for the mixed and single abrasive slurry, respectively. The smaller load (2.3 kg) resulted in an average roughness of 0.4 µm for both slurries. This revealed that the applied type of slurry showed no significant influence on the surface roughness results due to the grain size transition occurring during the process.

To decrease the surface roughness, the average grain size in the slurry can be reduced. However, it is important to note that reducing the abrasive grain size will lead to additional material removal. Therefore, this adjustment in slurry should be implemented before reaching the desired sample thickness. To verify this a slurry with a 20 µm abrasive grain size was initially used. This resulted in an average surface roughness of 318 nm. Subsequently, the slurry was changed to one containing a 9 µm abrasive grain size, which yielded an average surface roughness of 163 nm. Approximately 60 µm of material was removed through the use of the 9 µm slurry. AFM scans of the surfaces lapped using 20 µm and 9 µm abrasive grains are provided in Fig. 4.14a and 4.14b, respectively. To further enhance the surface smoothness for bonding purposes, an additional polishing step can be introduced.

The lapping technique offers several advantages, making it a widely used and commercially established process known for its precise control and high removal rate. It provides a removal rate of up to 4 µm for silicon when applying a 20 µm aluminum oxide abrasive and a loading weight of 3500 g. Hence, within one hour 240 µm material can be removed. Moreover, lapping is a mechanical process applicable to a wide range of materials, utilizing the



(a) **(b)**

Figure 4.14: AFM data for the average surface roughness of silicon lapped using aluminum oxide abrasive with a grain size of **(a)** 20 µm and **(b)** 9 µm. The average surface roughness's yielded 318 nm and 163 nm, respectively.

same lap plate and abrasive. It is possible to achieve a surface roughness of a few hundred nanometers before a subsequent polishing step. However, there are a few drawbacks associated with this method. Firstly, lapping is considered a dirty process performed outside the cleanroom environment. Consequently, the sample requires subsequent cleaning before re-entering the cleanroom for final processing. Additionally, demounting can be fragile, particularly depending on the thickness of the remaining substrate. The presence of voids on the bonding surface can pose challenges, as the mechanical nature of lapping may result in device damage in such cases. An example of this is illustrated in Fig. 4.15.

Finally, it should be noticed that the process cannot be performed at batch level in the cleanroom at DTU, which depending on the batch size, causes lapping to be a time consuming process.

4.3.2 Application: Row-Column Array

Due to external factors, the fabrication of the transducer array for the laparoscope became less appealing. As an alternative, the optimized lapping process for silicon was utilized on a row-column array developed by Postdoc Mathias Engholm. The design was subsequently mounted in a probe handle, and a comprehensive description of the entire process is provided in Paper C.

The process flow employed to complete a row-column array using a double bonded technique is illustrated in Fig. 4.16. In Step 1), a DREM etch, similar to the one described in Section 4.2, was performed, however the trenches were left air-filled. Removal of the bulk silicon substrate is illustrated in step 4), and was accomplished through lapping.

Initially, the wafer with finalized CMUT cells was mounted on a glass substrate upside down, exposing the backside of the wafer. This was ob-

Figure 4.15: Example of a wafer with void in the bonding interface. During lapping these voids resulted in separation between the substrate and the plate.

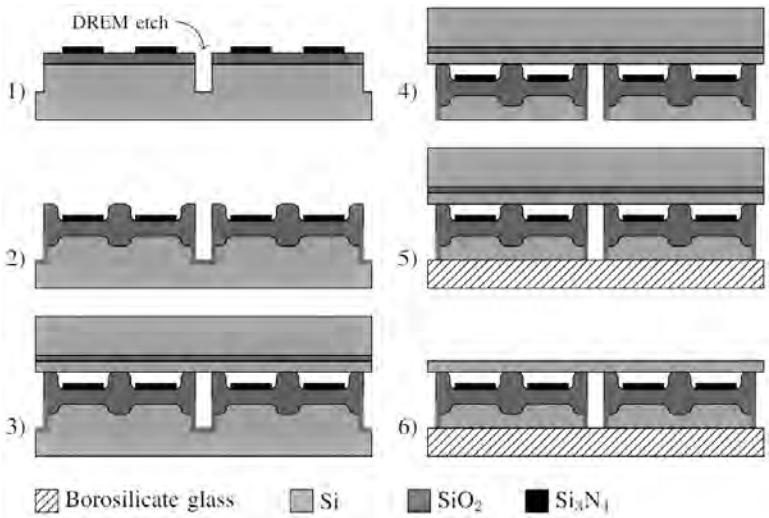


Figure 4.16: Process flow used for fabrication of a row-column array using a double bonded technique. Step 1) depicts the DREM process, while step 3)-4) illustrates removal of the silicon substrate performed using lapping. The figure is reprinted from [39].

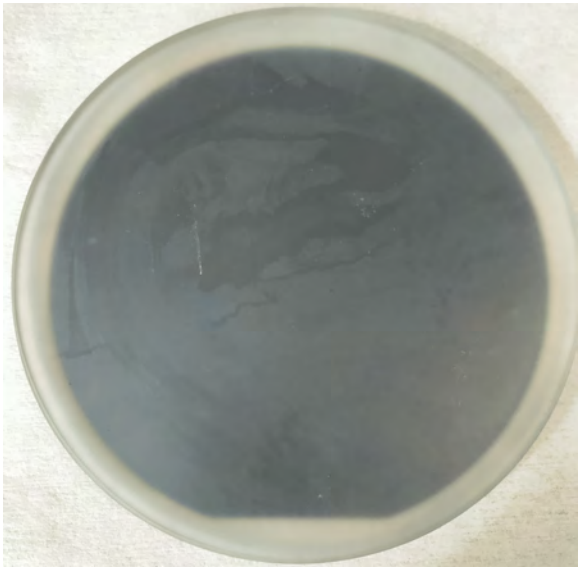


Figure 4.17: Depicting a successful bond for a wafer with row-column arrays.

tained by application of the process described earlier. An image of the bonded wafer is provided in Fig. 4.17, depicting a good bonding uniformity. For the lapping process, a slurry comprising 20 µm aluminum oxide abrasive mixed with water was used. The rotational speed of the plate was set to 70 RPM, and a loading weight of 1045 g was applied, resulting in a removal rate of 2.7 µm/min.

Various tests were conducted on row-column wafer, to stop the lapping process when reaching the DREM structures. An example of a successfully lapped wafer is depicted in Fig. 4.18, where the DREM structures are visible from the backside.

During the process, the rate was continuously monitored using a gauge attached to the jig. Additionally, the lapping was periodically halted to visually inspect the wafer. Height measurements at various positions on the wafer were obtained using a height gauge. However, these measurements were only performed on test wafers to ensure consistency in the lapping rate before proceeding to lap the device wafer. However, to mitigate the risk of lapping excessive material, the lapping process for the device wafer, with potential for probe mounting, was halted approximately 150 µm before reaching the DREM structures. Subsequently, the wafer was polished inside the cleanroom to minimize surface roughness, which was followed by removal of the remaining material using a silicon dry etching process separating the trenches as shown in step 4) in Fig. 4.16. Finally, the wafer was successfully bonded to a glass substrate using the anodic bonding technique (step 5).

A final study included testing the feasibility of removing the wafer handle through lapping after the substrate removal step, and prior to continuing

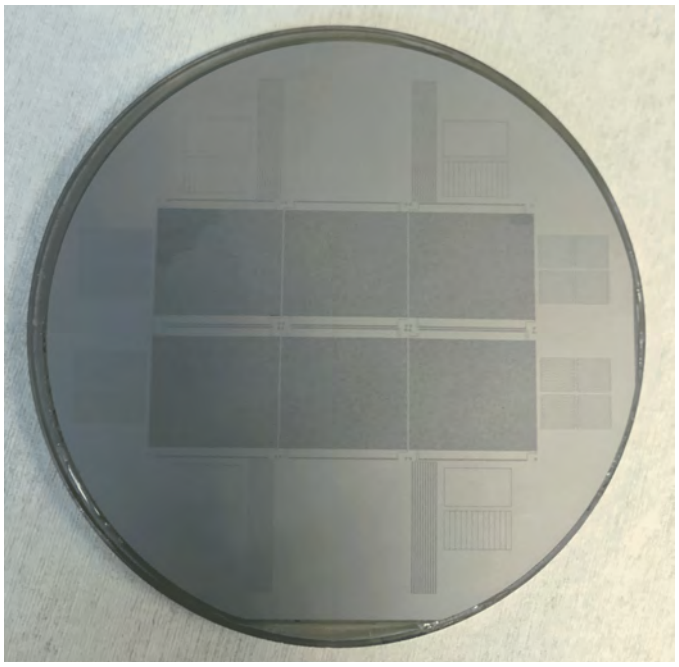


Figure 4.18: Backside of a wafer shown after lapping. The DREM structures are visible, meaning all the silicon substrate was successfully removed.

the processing within the cleanroom. This study was performed on five structured row-column wafers. The handle is commonly removed by dry etching methods and is illustrated in step 6) in Fig. 4.16. After the substrate removal the wafers were demounted by the method described earlier. They were then flipped and remounted with the bottom towards the glass substrate. The handle was removed using the same parameters as for the substrate removal process. However, after finalizing the second lapping process, the wafers were thinned to less than 150 µm, making them extremely fragile and challenging to handle during the subsequent fabrication steps. Based on these difficulties this fabrication method was not further investigated.

4.4 Chapter Summary

This chapter presented an alternative method enabling backside contacting of linear CMUTs by combining the high aspect ratio silicon dry etching method known as DREM with substrate thinning using a lapping technique. Initially, the parameters for the DREM process were optimized resulting in 140 µm deep trenches with a width varying from 3.2 µm at the top to 1.1 µm at the bottom, showing a slightly tapered profile.

Subsequently, a method for filling the trenches by undoped poly-silicon

was proposed. This initially involved a wet thermal oxidation of 500 nm oxide for corner rounding and reducing of the scallops, which is a result of the Bosch based DREM process. The oxide layer was removed and a 200 nm high quality dry thermal oxide was grown to serve as trench insulation for the transducer during operation. Undoped poly-silicon was then deposited. Cross-sectional SEM images of the trench revealed that the top of the trench was plugged before the middle and bottom sections, resulting in lack of mechanical stability of the structure. It was suggested to increase the oxidation step employed for corner rounding and to adjust the DREM recipe to get a more tapered trench outline. However, the process optimization was halted due to external factors.

The second part of the chapter introduced the mechanical process for material removal called lapping. This method is commercially used and provides high removal rates and great uniformity. The key parameters for the lapping process was introduced and evaluated with respect to the removal rate and resulting planarization. This includes the hardness of the sample material, the plate flatness, rotational speed of the lap plate, and the load applied to the jig. Furthermore, it was showed that the applied abrasize type, grain size and slurry concentration all affect the surface finish and the lapping rate. It was demonstrated that by changing the abrasive grain size from 20 µm to 9 µm, the average surface roughness was reduced from 318 nm to 163 nm, respectively.

The optimized lapping process was successfully applied to a row-column array designed and fabricated by Postdoc Mathias Engholm. The fabrication method utilized a double bonded process with air-filled DREM trenches. After successful fabrication of the CMUT structures, the substrate was thinned from the backside by lapping. The wafer was successfully bonded to a glass substrate exhibiting good uniformity. The lapping process used a slurry consisting on 20 µm aluminum oxide abrasive mixed with water. It employed a rotational speed of 70 RPM and a loading weight of 1045 g, resulting in a removal rate of 2.7 µm/min.

The lapping process was carefully monitored using various techniques to ensure consistent results. Additional steps, such as polishing and dry etching, were subsequently employed to achieve the desired surface characteristics required for anodic bonding.

Finally, a study was made investigating the feasibility to remove the wafer handle through lapping following substrate removal. However, the thinned wafers were very fragile with a substrate thickness of 150 µm, which made them challenging to handle during subsequent processing steps. Therefore, it was decided not to further investigate this method.

CHAPTER 5

Transducer Fabrication

This chapter presents the fabrication process of the Lin384 design. Fig. 5.1 provides an overview of the process flow, which is divided into into four main categories: silicon bump definition, gap definition, fusion bonding, and electrode definition.

Three different fabrication batches were conducted simultaneously to test various methods for the bump definition. In all three cases, the gaps were defined using a LOCOS process. The fusion bonding, metalization, and electrode definition steps were performed similarly for all batches.

The first section focuses on the three fabrication methods used for the bump definition. The first applied method has previously been demonstrated by this research group for various designs [16, 40, 41] and is based on a standard LOCOS process. Due to the fact that the final device involves two consecutive LOCOS processes it will be referred to as the double LOCOS process. The second method utilized a RIE process to define the silicon bumps. It is the simplest among the three methods and requires fewer fabrication steps, resulting in shorter fabrication time. This method is referred to as the RIE process. The third method, originally proposed for CMUTs by Park et al. [35], is referred to as the maskless LOCOS process since it employs a thick oxide mask instead of the conventional nitride mask during the long oxidation step. These three methods are subsequently compared with each other and assessed in reference to the simulations presented in Section 3.4.

The second section covers the LOCOS process used to define the CMUT cavities, while the third section presents the fusion bonding of the bottom substrates to in-house made PSOI wafers [39, 94]. Finally, the last section describes the metalization and electrode definition steps, completing the

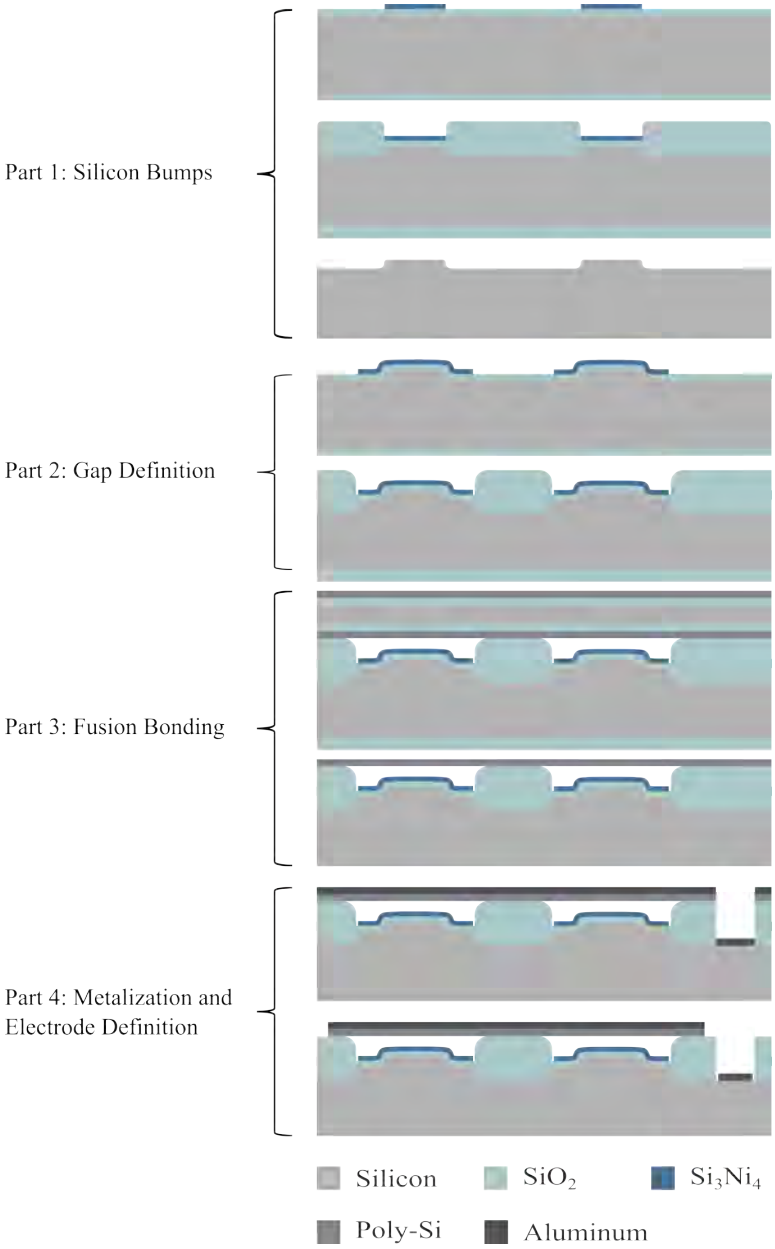


Figure 5.1: An overview of the process flow, highlighting the four main stages: bump definition, gap creation, fusion bonding, and electrode definition. Please note that the dimensions in the figure are not to scale.

fabrication of the devices.

The work described in this chapter was conducted in the clean room at DTU Nanolab in collaboration with M.Sc. Søren W. Gjaldbæk under supervision of the author. Detailed process flows for the three processes can be found in Appendix J, Section J.2-J.4.

5.1 Silicon Bumps

The initial step in the fabrication process involved defining and creating silicon bumps at the center of the CMUT cells. In the research group of the author, the conventional approach has been to employ a double LOCOS process, were two consecutive LOCOS processes are used, as suggested in [36]. Ph.D. Søren Elmin Diederichsen and Postdoc Mathias Engholm have further refined and optimized this process, as described in their respective Ph.D. theses [16, 40]. The following subsection will provide a detailed explanation of this process. Despite being a well-established method, the double LOCOS process is time-consuming, with a turnaround time of several weeks. This is primarily due to the numerous long furnace steps involved and the requirement of a poly-silicon mask to structure the nitride. The extended processing time increases the risk of errors and potential particle contamination resulting from residues in the etch baths and wafer handling. Consequently, alternative methods for fabricating the silicon bumps were explored during this Ph.D. project.

The first alternative method for fabricating the silicon bumps has a short process time and can be completed within a few hours. This method utilizes a RIE process, which simply requires a resist mask.

The second alternative method involves a thermal oxidation process utilizing a thick oxide as the masking material. This method was previously demonstrated by Park et al. [35]. The process offers a reduction in turnaround time compared to the double LOCOS process, however the process is more time-consuming than the RIE process. It is referred to as the maskless LOCOS process. The drawbacks of this method were elaborated in Section 3.4, where simulations revealed that the two extended oxidation steps in this process result in a more rounded bump outline compared to the other two methods. The maskless LOCOS process will be elaborated in more detail compared to the two other fabrication methods, since it provided the best results and is novel within this research group.

During fabrication of the silicon bumps, two critical factors were monitored: the uniformity across the wafer and the surface roughness. Poor uniformity can lead to variations in the gap height across the wafer, which affects the device pull-in and performance. This is undesirable during operation, as the working bias plays a crucial role in the transducer's performance. The surface roughness is important for facilitating the fusion bonding be-

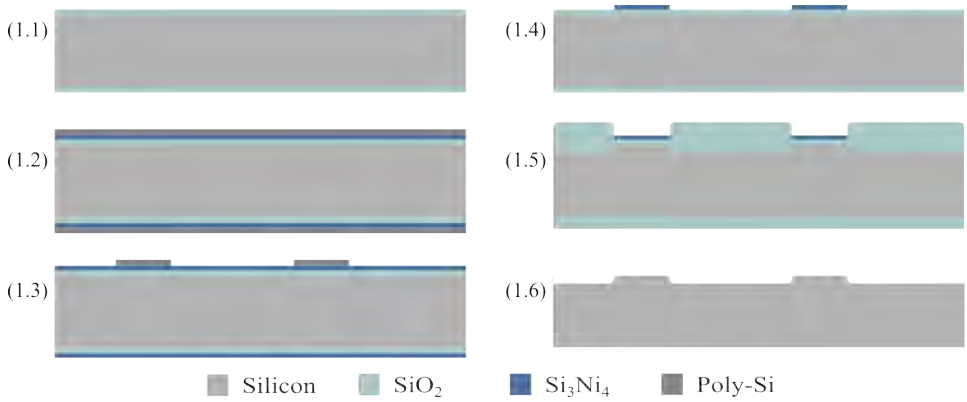


Figure 5.2: Process flow of the double LOCOS process. The dimensions in the figure are not to scale.

tween the top plate and the bottom substrate. The publications [88, 100] establish that successful fusion bonds are more likely to occur when the surface roughness is below approximately 0.5 nm. However, fusion bonding has been demonstrated with a surface roughness up to 1.0 nm [34].

To determine the uniformity of the silicon bump heights across the wafer, measurements were performed on a center element (array 7.2, see 3.2), as well as an element at the top of the wafer (array 1.2). The variation between these measurements were evaluated and used for quantification. The average surface roughness was evaluated using an AFM.

5.1.1 Double LOCOS Process

The first fabrication method employed was the double LOCOS process, and an overview of the process flow is illustrated in Fig. 5.2.

Initially, a dry thermal oxide layer with a thickness of 107 nm was grown on highly n-doped silicon wafers as shown in step (1.1). The exact thickness was not critical, but it influences the subsequent oxidation time, which should be adjusted accordingly. Next, a nitride layer of 46 nm and a poly-silicon layer of 90 nm were deposited on the wafers, see step (1.2).

A conventional UV-lithography step defined the desired bump pattern. Subsequently, the poly-silicon layer was structured using a wet etching solution containing Nitric acid (HNO_3), BHF and water. The etch time was 3 min and the structure after etching is outline in step (1.3). To assess the topography, a Dektak profilometer (from now on referred to as the Dektak) was employed, and the structures were visually inspected using an optical microscope. The height measurement yielded 97.3 nm, indicating a slight overetch into the nitride layer.

The subsequent step involved a wet etch of the nitride layer employing an 85 wt% Phosphoric acid (H_3PO_4) at 160 °C. The etching time for the

nitride layer was set to 45 min, including an overetch to ensure complete removal of residual nitride aroud the bump locations. Following this, the poly-silicon mask was removed (step 1.4).

Inspection of the wafers was conducted using both an optical microscope and the Dektak, resulting in a measured bump height of 79.5 nm. This indicates that 33.5 nm of the oxide layer was etched, leaving behind a 73.5 nm pad oxide layer. These values were utilized in Eq. (3.5) to compute the necessary post-oxide height to achieve the desired bump height of 500 nm. The target oxide thickness for the LOCOS was calculated to 1173.5 nm.

The first LOCOS process was performed using a wet thermal oxide, shown in step (1.5), resulting in a post-oxide height of 1185 nm. Subsequently, the nitride and oxide layers were removed using a sequence of processes involving BHF etching, nitride etching, and an second BHF etching step. This yielded a clean silicon surface, structured with bumps (step 1.6) measuring 498 nm in height, with a variation of less than 0.5 % between the center and the edge of the wafer. The Sensofar instrument was employed to measure the difference in radius at the top and bottom of the bumps, showing a maximum value of 1.1 µm.

5.1.2 RIE Process

The second process investigated for definition of the silicon bumps was the RIE process, which is illustrated in Fig. 5.3. This process involves a dry etching technique that utilizes a resist as the masking material. While this method offers a fast way to fabricate silicon bumps, it also presents several challenges and potential pitfalls. Applying the RIE process for this purpose necessitated a high level of process optimization and a stable etch environment. Additionally, the performance of the applied dry etching equipment exhibited variations on a daily basis, leading to a need for preliminary tests prior to processing, thereby increasing the total processing time. An inherent disadvantage of dry etching is its selectivity towards the underlying material, which can result in increased surface roughness.

The first process step involved patterning a highly n-doped silicon wafer by conventional lithography methods. This is shown in step (1.1). Subsequently, the silicon wafer was etched using a DREM etch process, which is described in more details in Section 4.2. This is illustrated in step (1.2). The process parameters were optimized by M.Sc. Søren W. Gjaldbæk and more details can be found in [86]. The optimization steps involved adjusting the coil temperature, testing the influence of the pre-conditioning of the chamber, incorporating a Bottom Anti-Reflection Coating (BARC) step along with optimizing the associated BARC time, and the number of etch cycles.

The optimized process used in this fabrication process involved four steps

1. Temperature stabilization for 20 min to −10 °C on a dummy wafer.

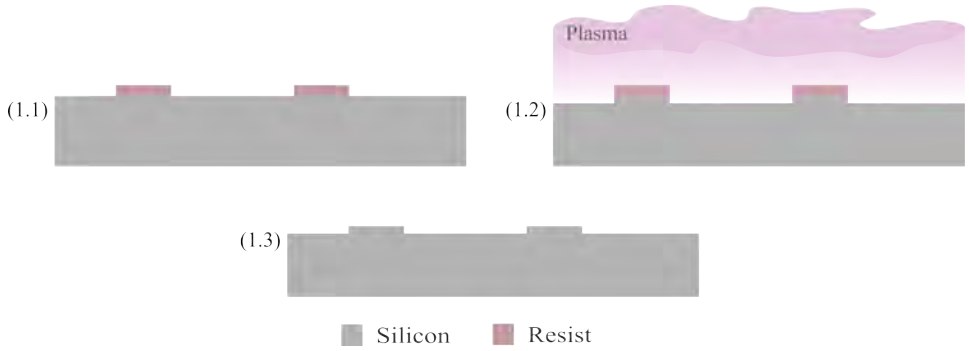


Figure 5.3: Process flow of the RIE based process used to define the silicon bumps. The dimensions in the figure are not to scale.

2. Pre-condition the chamber using a DREM process with a coil power of 0.5 kW and a temperature of −10 °C. Run 45 cycles on a dummy wafer.

3. Test number of cycles using a DREM process with 0.5 kW coil power. The temperature is −10 °C. Apply a 2 min BARC step. Run test wafer with 36 cycles.

4. Bump etch on the device wafers using the same parameters as in step 3. Adjust the number of cycles to 37, based on measurements on the test wafer.

A total number of seven device wafers were processed. The etch rate varied between 11.6 nm/cycle and 12.3 nm/cycle across the wafers. This variability is likely attributed to a chamber preconditioning step that may have been too short. The bump heights, measured on the Dektak, ranged from 428.6 nm to 456.7 nm, and the variation from the center to the edge of the wafers varied from 3.0 % to 5.9 %. The difference between the top and bottom radii measured 0.6 µm. The reduced bump height compared to the design specifications indicated the need for further adjustment of the number of etch cycles.

The surface roughness, determined by the AFM, was observed to be 2.3 nm, which exceeds the maximum limit of 1 nm required to facilitate fusion bonding. However, due to time limitations, the fabrication process proceeded. It was anticipated that the two subsequent thermal oxidations in the LOCOS process, used to define the cavities, would reduce the surface roughness and potentially enable fusion bonding.

5.1.3 Maskless LOCOS Process

The final proposed fabrication method for silicon bumps is referred to as a maskless LOCOS process, and is based on the method described in [36]. This

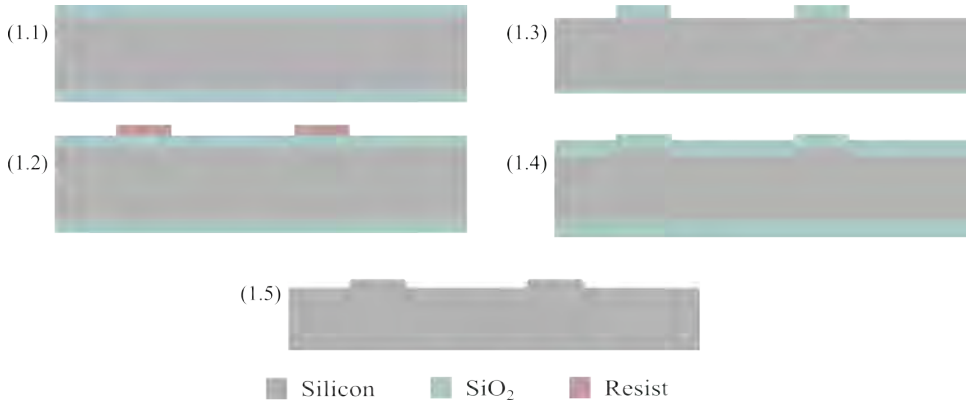
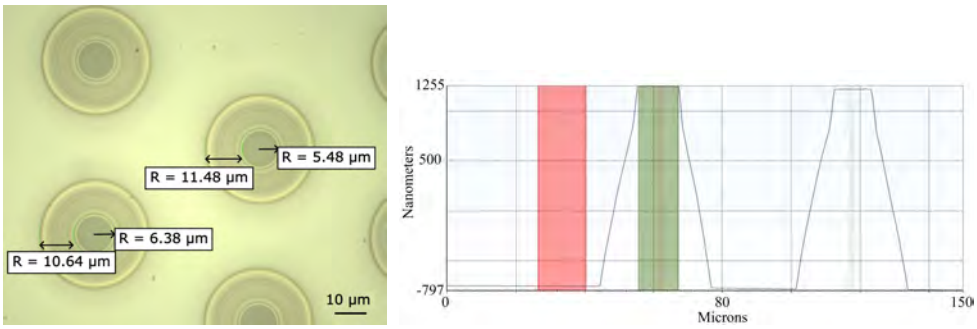


Figure 5.4: Process flow of the maskless LOCOS process used to create silicon bumps. The dimensions in the figure are not to scale.



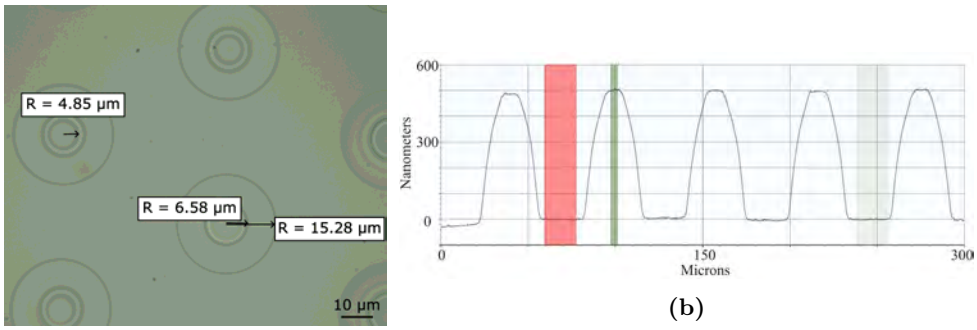
(a) **(b)**

Figure 5.5: Characterization results of the oxide mask after the BHF etch. **(a)** Optical microscope image of the oxide with resist on top. The oblique sidewalls are indicated by the color variation. **(b)** Dektak measurement of the structured oxide after resist removal. The height was measured to 2000 nm.

approach involved creating a thick oxide layer that, after being patterned, served as a diffusion barrier for a subsequent LOCOS step. Once the oxide layer was removed, the silicon surface was left with bumps, similar to those obtained in a conventional LOCOS process. An overview of the process is provided in Fig. 5.4.

In step (1.1), a highly n-doped silicon wafer was subjected to thermal oxidation, resulting in a 1997 nm thick oxide layer. This oxide layer was then patterned using a resist (step 1.2). To etch the oxide, a BHF solution was employed due to its high selectivity towards silicon (step 1.3). This is important since the surface roughness of the area surrounding the bumps plays a critical role for the success of the subsequent fusion bonding process.

Furthermore, due to the nature of chemical wet etches an undercut of 2 µm was expected. However, an optical microscope image, shown in Fig.



(a) (b)

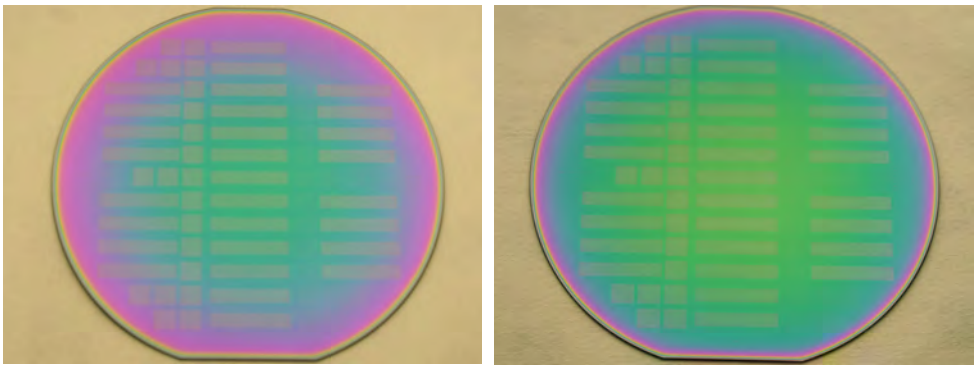
Figure 5.6: Characterization results of the oxide mask after the second oxidation. **(a)** Optical microscope image of the bumps with oxide on top. **(b)** Dektak measurement of the structured silicon surface after the oxide was removed. The bump height was measured to 502 nm.

5.5a, exhibited a significant color variation corresponding to oblique sidewalls. Radius measurements revealed a difference of up to 6 µm, leading to an underetch of up to 11.5 µm caused by capillary forces. The resist was subsequently removed, and the height and topography of the oxide layer were measured using the Dektak. The measurement is presented in Fig. 5.5b, confirming the presence of oblique sidewalls and the height of the oxide layer.

Despite the oblique sidewall issue, the process was continued to test the second oxidation time and the resulting bump height, which is shown in step (1.4). Thus, a RCA clean was performed, followed by a wet thermal oxidation step. Based on Eq. (3.13) and (3.12), the oxidation time was calculated to 8 h 41 min, corresponding to a post oxide height of 1873 nm. The oxidation process resulted in the growth of a 1853 nm thick oxide layer. The entire oxide layer was removed using a 37 min BHF etch (step 1.5), and the bump height was measured to be 502 nm. However, the oblique sidewalls caused by the underetch were transferred into the silicon bumps (see Fig. 5.6), indicating the need to reconsider the structuring method of the oxide.

To mitigate the underetching issues commonly associated with wet chemical etching, the possibility of combining dry and wet etching methods was explored on two test wafers. The Advanced Oxide Etch (AOE) dry etching tool was employed to etch the majority of the oxide layer, with the aim of leaving a residual layer of approximately 200 nm, which would subsequently be removed using a wet BHF etch. This approach benefits on the directional advantages of dry etching and the high selectivity offered by wet etching.

Considering the wafer load, the anticipated etch rate and etch time were 215 nm/min and 8 min, respectively. After the dry etching step, the two test wafers exhibited a color gradient, which is depicted in Fig. 5.7. This color grading arises from variations in the thickness of the oxide layer. To estimate the remaining oxide thickness and determine the required time for the wet



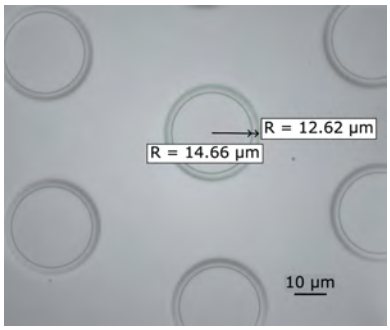
(a) **(b)**

Figure 5.7: Images of two test wafers after a dry etch of the oxide for 8 min leaving approximately **(a)** 450 nm and **(b)** 500 nm in the center of the wafer. The color difference shows the importance of proper preconditioning of the chamber before etching.

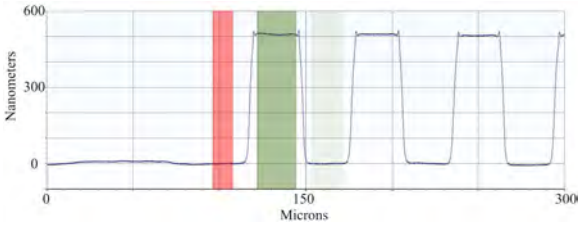
etch, a color chart was utilized. This is found in Appendix G, Fig. G.1. Based on the chart, it was estimated that the remaining oxide thicknesses on the two test wafers were approximately 450 nm and 500 nm, respectively, indicating the need for 6 min and 7.5 min of BHF etching. Notably, the variation observed between the two wafers emphasize the significance of the chamber's condition and stability prior to initiating the etching process.

After the resist was removed and the LOCOS oxidation was performed, a topographic measurement revealed the presence of spikes in the oxide layer at the edges of the bumps. These spikes, likely originating from an underetch of the oxide mask, were also observed in the silicon. Fig. 5.8 displays an optical microscope image and a Dektak measurement illustrating the silicon bumps. The measured bump height was 509 nm, and it was revealed that the oblique shape resulting from the previous wet etching process was significantly reduced.

To reduce the thickness of the residual layer and prevent underetching, the etch time on the AOE for the device batch was extended to 10 min. This adjustment aimed to minimize the required BHF etch time and obtain less oblique sidewalls. The residual layer on the device wafers ranged from 250 nm to 300 nm, resulting in a 4 min BHF etch duration. Following the removal of the resist, the LOCOS oxidation step was conducted, resulting in an oxide thickness of 1902 nm. The oxide layer was subsequently removed, and the wafers were inspected showing no edge spikes. The inspection revealed an average bump height of 510 nm and a difference in top and bottom radii of 3.1 µm. The variation in bump height across the wafer was less than 0.6 %. The maximum surface roughness measurement yielded 0.21 nm, which satisfies the criteria for successful fusion bonding in the subsequent processes.



(a)



(b)

Figure 5.8: Characterization results of the silicon bumps after the oxide was removed. The combination of a dry and a wet etch was used to etch the initial oxide. **(a)** Optical microscope image showing slightly oblique sidewalls. **(b)** Dektak measurement of the silicon bumps with small spikes at the edge of the bumps. The center height was measured to 509 nm.

Table 5.1: Summary of the key results obtained from the three tested processes for silicon bump fabrication. The table includes measurements of the average bump height, variation across the wafer, surface roughness, and sidewall obliquity.

	Bump height [nm]	**Variation** [%]	**Surface roughness** [nm]	**Obliquity** [µm]
Double LOCOS	498	0.5	-	1.1
RIE process	453	5.9	2.3	0.6
Maskless LOCOS	510	0.6	0.2	3.1

5.1.4 Process Comparison

A summary of the most important results from the three different fabrication processes used for the silicon bump formation is presented in Table 5.1. The results demonstrate that the RIE process exhibited larger height variation and surface roughness compared to the other two processes. However, the RIE process produced bumps with less oblique sidewalls, which aligns with the simulations presented in Section 3.4. When comparing the maskless LOCOS process with the conventional double LOCOS process, similar results were observed. The obliquity of the maskless LOCOS process was slightly higher, while both the variation and bump heights were comparable.

These findings facilitates replacing the conventional double LOCOS process with the maskless LOCOS process, which offers the advantage of fewer fabrication steps, reducing the processing time, thus the risk of failure. However, it should be noted that the maskless LOCOS process results in more rounded slopes and corners due to the longer total oxidation time. This

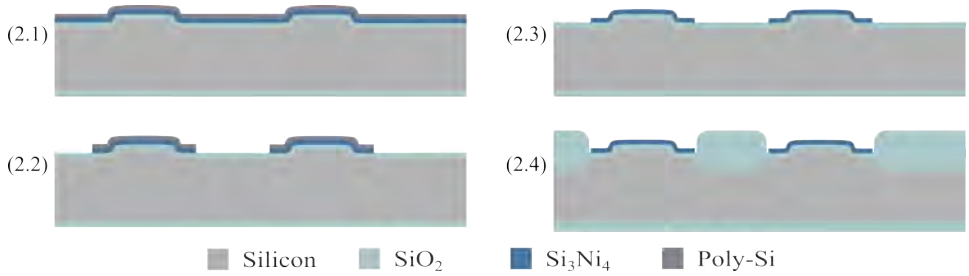


Figure 5.9: Process overview of the second LOCOS step forming the cavities. Notice, the dimensions are not to scale.

will reduce the active area and subsequently affect the capacitance of the CMUT.

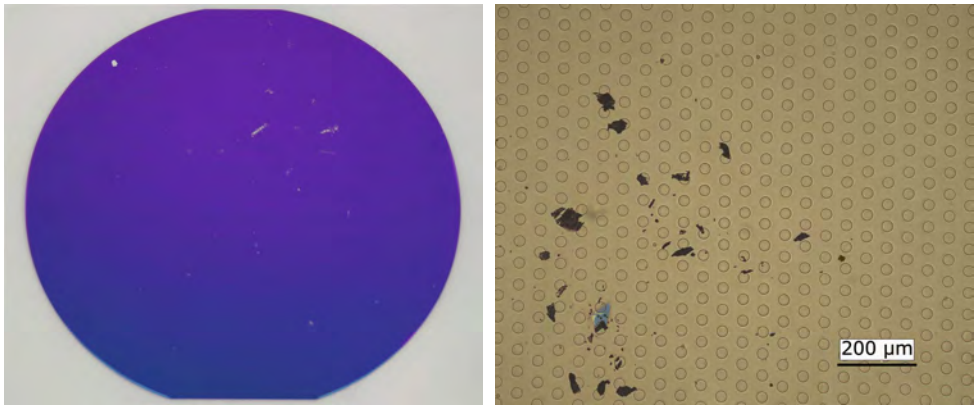
In conclusion, the observed bump profiles support the simulations from Section 3.4, indicating that the RIE process yielded bumps with the straightest sidewalls, while the maskless LOCOS process produced bumps with the most oblique sidewalls. However, it is important to consider that the significant surface roughness in the surrounding area for the RIE process may cause challenges or even prevent subsequent fusion bonding.

5.2 Gap Definition

Following the fabrication of silicon bumps using three different methods, the next step involved creating the gaps and finalize the bottom substrate containing cavities. The desired height for the gaps was set at $g = 66\,\text{nm}$. From this point onwards, the fabrication steps were identical for all three batches, allowing them to be processed together. The final step for fabrication of the bottom substrate involved a LOCOS process, similar to the one described in Subsection 5.1.1. A process flow illustrating these steps is presented in Fig. 5.9.

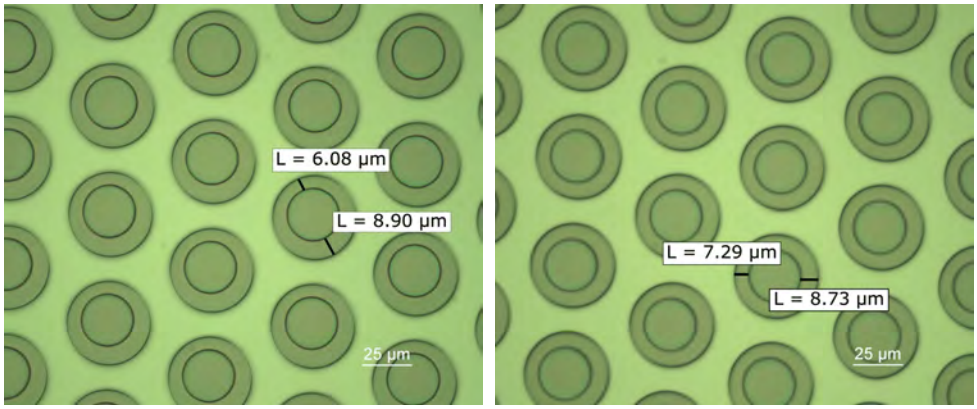
The initial step involved cleaning the wafers through a RCA cleaning process, followed by the growth of a 400 nm dry thermal insulation oxide of high quality. This oxide layer serves as electrical insulation during the operation of the transducer. Next, a nitride layer was deposited on the wafers. However, due to a malfunctioning nitride furnace, large particles were present on the wafers, as depicted in Fig. 5.10. To address this issue, a nitride removal process was performed using a wet H_3PO_4 etch, followed by another RCA clean. As a result, the oxide surface was left clean, however, it was estimated that the two 30 s dips in a HF solution caused an etching of approximately 30 nm of the insulation oxide.

Once the furnace was repaired, a new nitride layer with a thickness of 56.5 nm was deposited, followed by the deposition of a 99.2 nm poly-silicon layer. The deposition steps for these three layers are illustrated in step (2.1).



(a) **(b)**

Figure 5.10: Images of a wafer after nitride deposition using a defect furnace causing contamination with large particles. **(a)** Shows a photo where the particles appear white. **(b)** An optical microscope image with large colored nitride particles.



(a) **(b)**

Figure 5.11: Alignment comparison of one wafer from the **(a)** double LOCOS batch, and **(b)** one from the maskless LOCOS batch.

Subsequently, lithography was performed to define the cavities. However, there was a noticeable misalignment discrepancy observed among the wafers. Fig. 5.11 demonstrates this issue, with Fig. 5.11a displaying a misalignment of approximately 3 µm for wafer 1 from the LOCOS batch, while Fig. 5.11b shows a misalignment of around 1.5 µm for wafer 4 from the maskless LOCOS batch. The use of a manual aligner tool for this process made it more challenging to achieve perfect alignment compared to automated aligners. Despite the slight misalignment, the fabrication process was continued.

The next steps involved structuring of the poly-silicon and nitride layers using HNO_3 and H_3PO_4 solutions, respectively. This process is illustrated in steps (2.2). Between these etching steps, the wafers were inspected using an optical microscope and the Dektak to ensure that no residual poly-silicon remained before the resist was removed. Subsequently, after the nitride etch, another inspection was conducted to confirm the success of the etching process before proceeding to strip the poly-silicon. The poly-silicon mask was removed using wet H_3PO_4, as shown in step (2.3). The remaining height of the nitride layer was measured to be 74.5 nm, indicating that 18 nm of oxide had been etched. This information was taken into account when calculating the oxidation time for the second LOCOS process.

Since the three fabrication methods creating the silicon bumps resulted in varying bump heights, separate calculations were performed to determine the LOCOS oxidation times for each batch. The calculations were based on the average bump heights displayed in Table 5.1. The target heights of the post oxides were determined using Eq. (3.8). For the RIE process, the calculated target height was 1416 nm, while for the double and maskless LOCOS processes, the target heights were 1498 nm and 1520 nm, respectively. The actual grown oxide heights measured 1434 nm for the RIE process and 1528 nm for both the double LOCOS and maskless LOCOS processes. The oxidation process is illustrated in step (2.4) in Fig. 5.9. However, the resulting cavity heights were significantly smaller than expected. This indicates that the ratio between the consumed silicon and the grown oxide is different than expected from theory. The underlying cause of this behavior remains unknown and requires further investigation. Consequently, all three batches underwent an additional thermal oxidation step for 15 min in order to increase the gap height. The final cavity heights for the three batches, along with the thickness of the insulating oxide, nitride, post-oxide, and the surface roughness, are summarized in Table 5.2. Notably, the surface roughness of the RIE process appears to be theoretically too high to achieve a successful fusion bond. However, processing was continued for all three batches despite this concern.

Finally, the outline of the cavities were measured using AFM for the three different fabrication methods. The obtained results for the right side of a cavity are presented in Fig. 5.12. In the figure, the black crosses represents the top of the nitride layer, while the black stars indicate the

Table 5.2: Key results from the three different batches after finalizing the bottom substrates with cavities.

	Ins. oxide [nm]	**Nitride thickness** [nm]	**Cavity height** [nm]	**Post-oxide** [nm]	**Surface roughness** [nm]
Double LOCOS	370	56.5	74	1566	0.24
RIE process	370	56.5	68	1473	1.26
Maskless LOCOS	370	56.5	60	1571	0.19

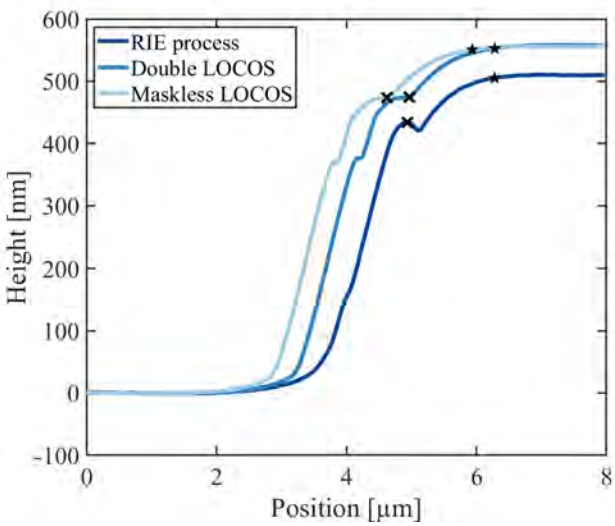
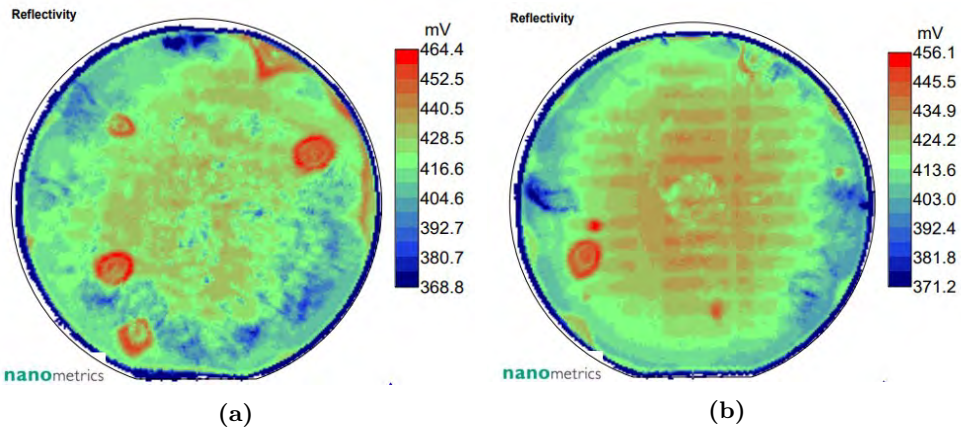


Figure 5.12: Structure outlines from the three different fabrication processes. The results are achieved from AFM measurements and validates the expansion in cell radius of 1.3 µm, predicted by the cavity simulation study elaborated in Section 3.4



(a) **(b)**

Figure 5.13: Photo-luminescence maps of the fusion bonds of **(a)** a double LOCOS wafer and **(b)** a maskless LOCOS wafer. Voids in the bond are shown as dark red areas.

1 % plateau change, as introduced in Section 3.4. The position of the top of the nitride layer was used as reference point to measure the expansion of the cell radius. All three processes exhibited an expansion of 1.3 µm in the cell radius. This is equal to the simulation result obtained for the double LOCOS process and demonstrates that the fabricated cell radius exceeds the dimensions specified in the mask layout with approximately 1.3 µm, yielding a radius of 22.3 µm, which aligns with the intended design.

5.3 Fusion Bonding

After finalizing the bottom substrates, the subsequent crucial step was the fusion bonding process. Fusion bonding is a highly robust bonding technique that forms permanent covalent bonds [101]. This process comprises three main steps: wafer preparation, pre-bonding, and annealing. As mentioned earlier, it is essential for both wafers to have a surface roughness below 1.0 nm and the wafer bow should not exceeding 5 µm to achieve a successful bond [34].

In this process, the top plates were comprised of in-house made PSOI wafers [39, 94], with a device layer thickness of 4.5 µm and a Burried OXide (BOX) thickness of 500 nm. The handle layer consisted of a 350 µm thick silicon wafer. Both the PSOI wafers and the bottom substrates underwent a thorough cleaning process using a RCA clean to remove any surface particles and ensure optimal conditions for the pre-bonding stage. The pre-bonding step was carried out under a High Efficiency Particulate Air (HEPA) filter to maintain a clean environment and minimize the risk of contamination. To achieve a stronger bond, the wafers were subjected to uniform pressure

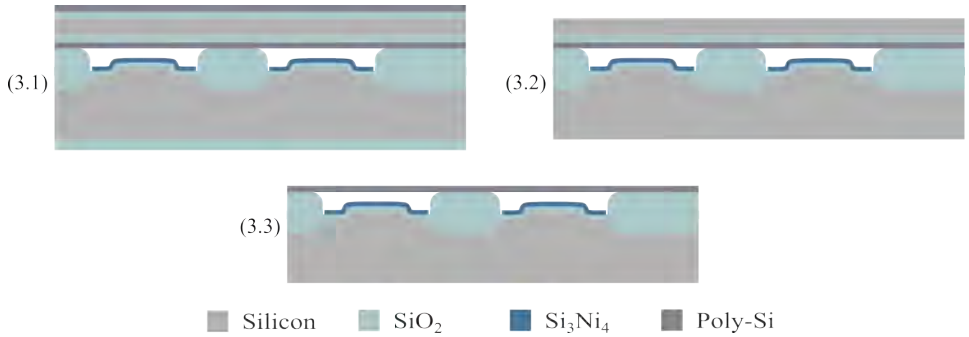


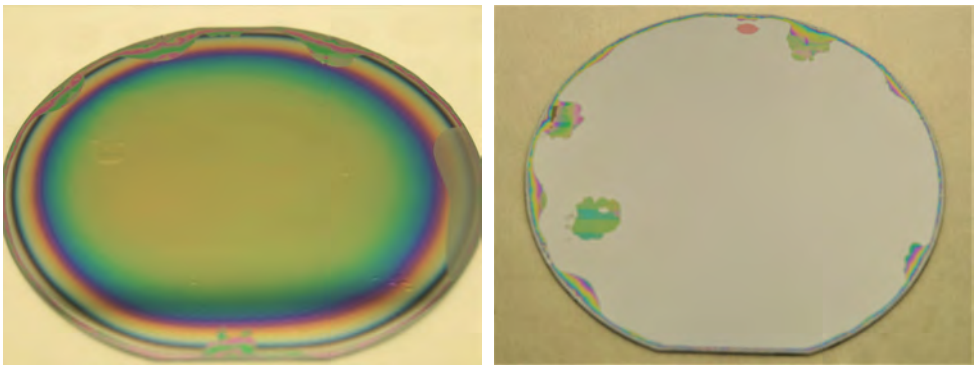
Figure 5.14: Process flow showing the steps after fusion bonding. Note, the dimensions are not to scale.

at 50 °C using a wafer bonder. After a 5 min duration in the wafer bonder, the annealing process took place in a furnace at 1100 °C for 70 min.

As a result, successful bonding was achieved for the wafers from the double LOCOS and the maskless LOCOS batches. However, the RIE processed wafer failed to bond. The surface roughness, measured using AFM, was determined to be 1.26 nm, which did not meet the criterion for fusion bonding. Although there was a 45 % reduction in surface roughness compared to the silicon surface roughness measured before the LOCOS step, it was insufficient for successful fusion bonding. Due to time constraints, the RIE batch was discarded.

After the anneal process, the bonded wafers were subjected to inspection using the Photo Luminescence (PL) mapper, which is a non-contact and non-destructive technique employed to assess bond strength and identify voids within the bonding interface. The resulting wafer maps are presented in Fig. 5.13, revealing the presence of voids in both wafers. Fortunately, the majority of these voids are located along the edges, leaving the possibility of intact arrays in the central region of the wafer.

The subsequent step involved the thinning of the PSOI wafer. The process flow is depicted in Fig. 5.14. Initially, in step (3.1), the two wafers are shown after being fusion bonded. The first layer to be thinned was the poly-silicon layer. This was achieved through a wet 80 °C Potassium Hydroxide (KOH) etch for 10 min, including an overetch. Next, the oxide layer was removed in a BHF etch. These steps are illustrated in step (3.2). In order to enhance future processing, it is advantageous to perform a piranha clean prior to thinning the handle layer. This step eliminates organic compounds that may otherwise act as an etch mask, thereby necessitating a longer etching duration to completely remove the layers. The majority (approximately 250 µm to 280 µm) of the silicon handle was removed using the Advanced Silicon Etch (ASE), while the remaining 70 µm to 100 µm sil-



(a) **(b)**

Figure 5.15: Thinning process of the in-house made PSOI used as a top plate for the CMUTs. **(a)** Shows the BOX layer after the silicon handle was removed in a KOH etch, while **(b)** depicts the poly-silicon top plate after the BOX layer was etched in BHF.

icon was eliminated using KOH for 68 min. This approach benefits from the higher selectivity towards the underlying oxide layer. Finally, the BOX layer was removed using BHF, as shown in step (3.3). Images depicting a wafer during the wet removal of the handle and BOX layers is shown in Fig. 5.15.

5.4 Metallization and Electrode Definition

Once the plate was successfully thinned down, the next step involved defining the bottom electrodes. This process is illustrated in Fig. 5.16. To achieve this, a lithography process was utilized. The top plate and the post-oxide were etched using the ASE for 1 min and 18 s, respectively. Furthermore, the AOE was employed for 9 min and 30 s. This is shown in step (4.1).

Subsequently, the wafers underwent metallization. The e-beam evaporator was utilized to deposit 400 nm aluminum for the electrodes, as shown in step (4.2). Another lithography step was carried out to define the metal electrodes. The aluminum was etched using a wet PES 77-19-4 etch (step 4.3), with an etch rate of 60 nm/min, resulting in an etch time of 9 min and 30 s. Optical microscope inspection was conducted in both bright and dark field modes. Fig. 5.17b demonstrates a successful aluminum etch, exhibiting well-defined top electrodes and kerfs.

The final step in the fabrication process involved separating the top plate. This was achieved using the ASE dry etch tool for a duration of 1 min and 40 s. Subsequently, the resist mask was removed, marking the completion of the fabrication process, shown in step (4.4). However, to protect the wafers during electrical characterization and dicing, a 2 µm resist was spin-coated on top, and openings were created to access the top and bottom electrodes.

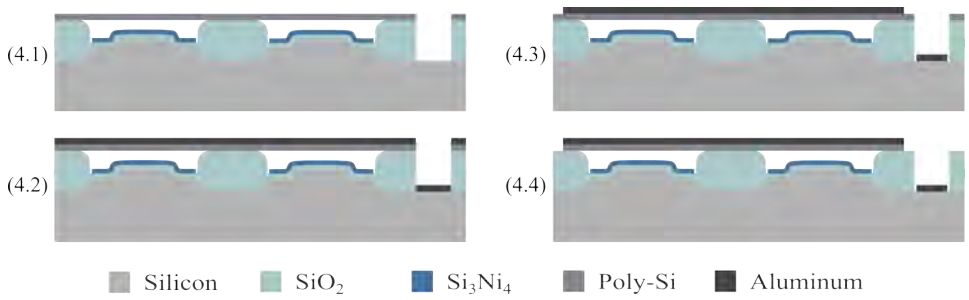
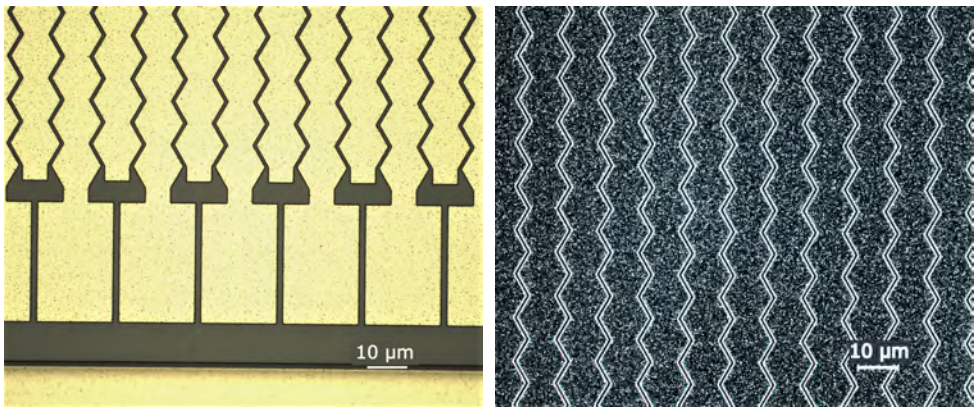
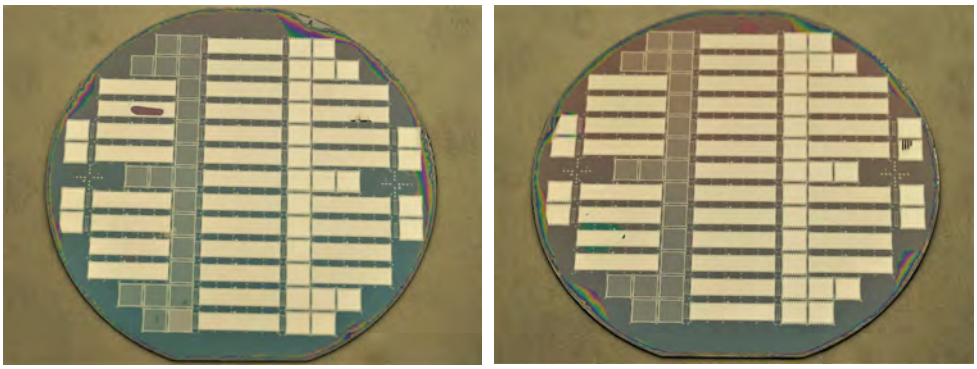


Figure 5.16: Process flow illustration the metallization step, together with the electrode definition. The dimensions are not to scale.



(a) **(b)**

Figure 5.17: Optical microscope images after the aluminum etch. **(a)** Utilizes bright field mode, and **(b)** dark field mode. The pictures illustrates a successful aluminum etch.



(a) **(b)**

Figure 5.18: The two finalized wafers from **(a)** the double LOCOS process and **(b)** the maskless LOCOS process. Both wafers exhibited a significant number of successfully fabricated arrays, although some top plate defects can be observed specifically at the edge arrays.

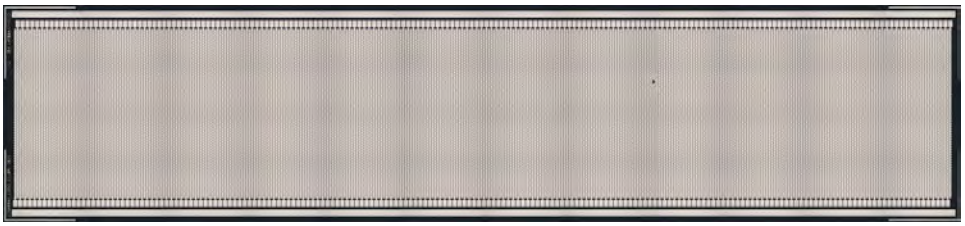
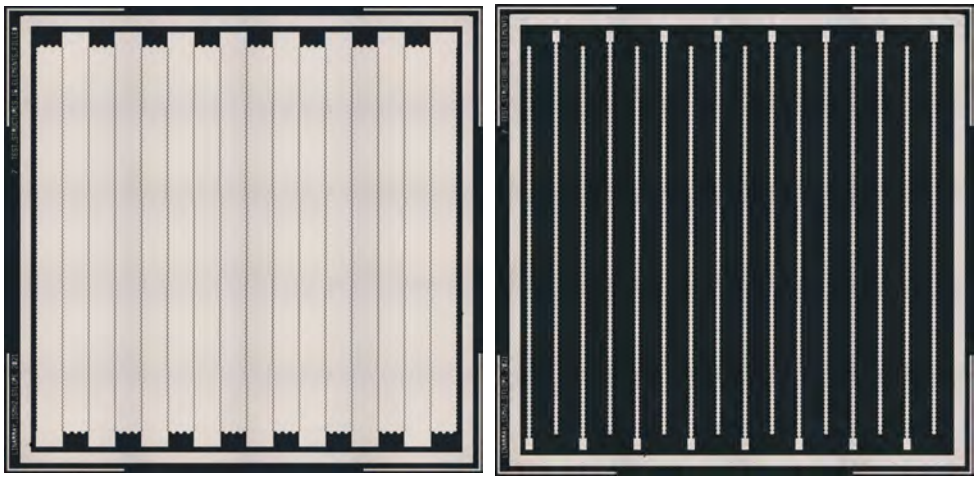


Figure 5.19: A stitched optical microscope image of a Lin384 array (array number 7.2). The image is stitched together from multiple images. A particle is seen in the right side of the array causing short circuit between two adjacent elements.

Fig. 5.18 present one finalized wafer from the double LOCOS batch and one from the maskless LOCOS batch. Visual observation indicates the presence of numerous successful arrays on both wafers. However, some top plate defects can be observed along the edges, as well as small areas with delamination, which were anticipated based on the PL maps in Fig. 5.13. Although these defects are likely to decrease the yield, the large number of arrays on each wafer still allows for comprehensive electrical characterization.

Furthermore, an optical microscope inspection was conducted to identify any particles or contaminants that could potentially cause short circuits between the elements. A stitched overview image of array 7.2 was created and is depicted in Fig. 5.19. Similar images were generated for two 16-element arrays: one of the *Filled* design (array F7) and the other of the *Single* design (array S7). These images are displayed in Fig. 5.20a and 5.20b, respectively, and are all from the maskless LOCOS wafer.



(a) **(b)**

Figure 5.20: Microscope image of two 16-element arrays stitched from multiple images. **(a)** Shows an array of the *Filled* design (F7), while **(b)** shows the *Single* design (S7).

5.5 Chapter Summary

This chapter demonstrated a successful fabrication method for $\lambda/2$-pitch linear arrays with 384 elements based on CMUT technology. The fabrication process involved the use of a LOCOS based and fusion bonding technique. Three different methods for fabricating the silicon bumps were investigated to potentially reduce the fabrication time.

The first method tested was the double LOCOS process, which served as the reference method due to its widespread use and optimization within this research group. The results showed a bump height of 498 nm with a variation across the wafer of 0.5 %. The second method, the RIE process, was explored as a more time-efficient alternative. This approach yielded a slightly smaller bump height of 453 nm with a higher variation of 5.9 % across the wafer. However, the surface roughness was measured to 2.3 nm, which exceeds the limit for successful fusion bonding. The third method, referred to as the maskless LOCOS process, employed a thick oxide mask for subsequent oxidation to form the bumps. This method resulted in a bump height of 510 nm with a variation of 0.6 %.

By comparing these three methods, it was determined that the double LOCOS process and the maskless LOCOS process exhibited the most consistent results, while the RIE process offered a faster fabrication time but required further optimization due to the high surface roughness.

The cavities were, for three batches, created using a conventional LOCOS process. To achieve a desired gap height of 66 nm, the oxidation time was adjusted based on the initial bump heights. However, the anticipated height

of the post oxide resulted in smaller gap heights than expected. The reason for this phenomenon is remains unknown and requires further investigation. As a result, a second oxidation process was carried out on the wafers to increase the gap heights. The resulting heights after oxidation were 74 nm, 68 nm, and 60 nm for the double LOCOS, the RIE, and the maskless LOCOS methods, respectively.

After finalizing the cavity formation, the surface roughness was reevaluated. Unfortunately, the RIE process exceeded the acceptable limit of 1.0 nm for successful fusion bonding, with a roughness measurement of 1.26 nm. Despite this result, all wafers underwent fusion bonding to an in-house made PSOI due to time constraints. As anticipated, the RIE wafers failed to bond, leading to the dismissal of that batch. However, both the double LOCOS and maskless LOCOS wafers successfully bonded. Following the bonding, the PSOI wafer was thinned down, leaving a 4.5 µm poly-silicon layer as the top plate. Metalization of the contacts was carried out using 400 nm aluminum, which was defined through wet etching. These steps completed the fabrication process for two successfully fabricated wafers.

To protect the wafers during electrical characterization and dicing, a 2 µm resist layer was applied on top. Openings were made only for the electrode bonding pads, allowing for electrical measurements to be performed on the wafers.

CHAPTER 6

Electrical Wafer-Level Characterization: Method

With the increasing number of elements and a large number of arrays per wafer, requirements rise to find an optimal wafer-level characterization method. Historically, this research group have used a measuring sequence of impedance-frequency (Zf), followed by a current-voltage (IV) sweep and finalized with a Capacitance-Voltage (CV) sweep. Each of these measurement types will be further explained in the following subsections.

Conducting a comprehensive analysis of an entire wafer is a time-consuming process and conducting a complete characterization using the aforementioned sequence for this specific wafer layout would require 31 consecutive days of automated measurements. Hence, there is a need to discover an alternative approach that provides sufficient information for identifying the most promising arrays for further evaluation, integration and packaging. Even in cases where wafers exhibit high yields, it is crucial to select the most superior arrays for research purposes since only a fraction of the fabricated arrays will end up in a probe. However, this approach differs significantly from production scenarios, where all arrays meeting specific criteria are utilized in ultrasonic probes.

The paper "Performance Assessment of CMUT Arrays Based on Electrical Impedance Test Results" [102] introduces a wafer-level characterization method for CMUTs. In this study, the resonance frequency of the elements is used as the figure of merit, requiring a biased impedance measurement. To accelerate the characterization process, only a subset of elements, accounting for 32 % of the total, is measured on each array. While this approach reduces the characterization time, it does not allow for detection of failures in the untested elements. As an alternative, this thesis investigates the possibility of utilizing an initial fast unbiased Zf screening to provide sufficient

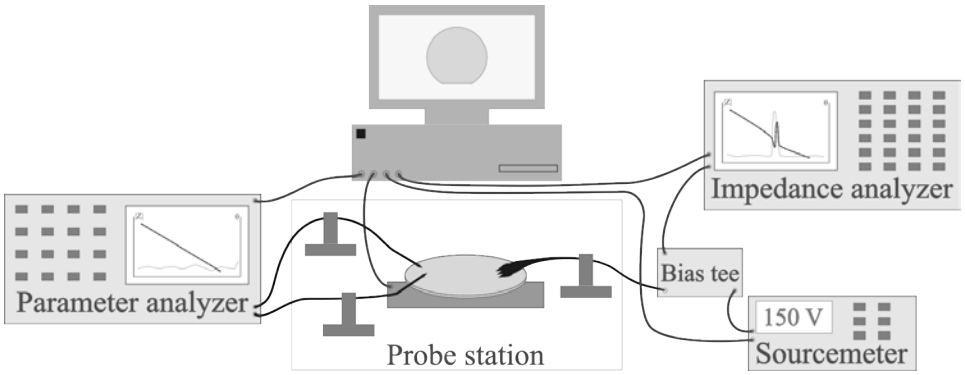


Figure 6.1: Illustration of the two setups employed in the characterization. In the center, the probe station is shown with a wafer placed on the chuck, and the probe positioners holding the probes. On the left side, the two probes connected to the parameter analyzer is depicted. On the right side, the three-pin probe is connected to the impedance analyzer and a source meter via a bias tee. All the components are interconnected and controlled from a computer.

information about the most promising arrays, which can then undergo a full characterization.

This chapter provides an overview of the electrical characterization conducted on the two finalized wafers, specifically one from the maskless LOCOS batch and one from the double LOCOS batch, both of which were successfully fabricated. The measurement setup used for characterization is described in the first section, emphasizing the significance of cable convention and its impact on the measurement results. Additionally, a novel wafer-level characterization method is introduced, starting with visual inspection, which is elaborated upon in the second section. The third section outlines the initial Zf screening performed on all elements, and discusses typical aberrations and their effects on the Zf outputs. Based on the results, a few promising arrays were selected for a comprehensive IV/CV analysis, described in the fourth section. The fifth section focuses on biased, high-frequency Zf measurements utilized to determine the resonance frequency and the pull-in voltage. Due to the time-consuming nature of this analysis, it is performed only on selected elements across an array. Finally, the stability measurement is described and used as a method to evaluate the long-term behavior of the transducer.

6.1 Measurement Setup

The electrical characterization was performed using a Cascade Summit 12K Probe Station, which is a semi-automatic wafer-level tester. Two measurement setups were utilized: the first coupled the probe station with a Keysight

B1500A Semiconductor Parameter Analyzer, while in the second setup the probe station was used with an Agilent E4990A Precision Impedance Analyzer.

An illustration of the setups is provided in Fig. 6.1, depicting the probe station in the center with the chuck, the probe positioners holding the probes, and the connection to a control computer. The wafer was positioned on the chuck and kept in place using vacuum clamping. To ensure accurate measurements, a shield (known as a top-hat) surrounded the chuck, serving the dual purpose of providing Electromagnetic Interference (EMI) shielding and creating a light-tight environment. The probe needles were mounted in the probe positioners to facilitate probe positioning with high accuracy. The microscope was used for both visual inspection and to image the array behavior while increasing the bias voltage to determine the pull-in voltage. This will be described in detail in Section 6.2 and 6.6. Additionally, the illustration demonstrates the two cable connections to the parameter analyzer on the left side of the figure, as well as the connection to the impedance analyzer on the right side of the figure. Notice, the impedance analyzer was connected to a Keithley 2410 Sourcemeter through a bias tee, enabling the application of a large DC bias during probing.

The probe station also facilitated the generation of a wafer map, which contained the precise coordinates of the contact pads of the array elements. This wafer map was then utilized by the parameter analyzer for automated measurements.

Further explanation of the two setups will be provided in the subsequent subsections.

6.1.1 Parameter Analyzer

The first setup involves using the parameter analyzer together with the probe station, illustrated to the left in Fig. 6.1. As briefly mentioned, the connection between the parameter analyzer and the probe station consists of two cables, each connected to a probe needle. One cable carries high current/high potential (H_c/H_p), while the other carries low current/low potential (L_c/L_p). It is crucial to adhere to the cable convention, where H_c/H_p is applied to the bottom electrode and L_c/L_p is applied to the top electrode, particularly when having a conductive substrate. Further details regarding this cable convention will be discussed later in this section.

One significant advantage of the parameter analyzer is its capability for automated probing at wafer level. Using the wafer map generated on the probe station, a measurement sequence and a list specifying the number of elements to be measured can be established.

For the initial wafer screening, an unbiased Zf sweep was performed. The settings applied for this sweep are outlined in Table 6.1. Additionally, the table provides information of the settings used for the subsequent IV and CV

Table 6.1: Sweep parameters for the measurement sequences performed using the parameter analyzer. All measurements were performed using medium integration time.

	Frequency			**Bias**			**Oscillation level**
	start	stop	steps	start	stop	steps	
Zf	1 kHz	1 MHz	76		0 V		50 mV
IV		-		−100 V	100 V	1 V	50 mV
CV		50 kHz		−100 V	100 V	1 V	50 mV

sweeps. The frequency applied during the CV measurement is determined based on the Zf measurement and should be chosen from a stable level in the Capacitance-frequency (Cf) curve, which is described in further detail in Section 6.3.

One limitation of the parameter analyzer is the limited frequency range, spanning from 1 kHz to 5 MHz. This range may not cover the resonance frequency of recent designs within the research group. Consequently, the resonance frequency is determined using the second setup with the impedance analyzer, which will be explained in the next section. Nevertheless, the parameter analyzer can still be used to determine the capacitance of the elements and identifying common errors like short circuits and connected top electrodes.

Cable Convention

The cable convention has been demonstrated to have a significant impact on measurement results, particularly when dealing with a conductive substrate. To obtain representative results, the H_c/H_p terminal should be connected to the chuck or, in this case, the bottom electrode, while the L_c/L_p terminal should be connected to the Device Under Test (DUT), corresponding to the top electrode. This is due to the presence of the chuck-to-ground capacitance, which is shown in Fig. 6.2. When the H_c/H_p terminal is connected to the top electrode, a fraction of the current leaks through the chuck after passing the CMUT, as illustrated in Fig. 6.2(a). However, due to the positioning of the ampere meter, this particular current is not measured, resulting in misleading results. By reversing the terminals and connecting the L_c/L_p terminal to the top electrode, as shown in Fig. 6.2(b), only the current flowing through the CMUT is measured. This change in configuration ensures that the chuck-to-ground capacitance now precedes the device, eliminating the undesired effects.

To illustrate this effect, measurements were conducted with the conventional bias, where H_c/H_p is connected to the bottom electrode and L_c/L_p is connected to the top electrode, as well as with the reversed bias, where

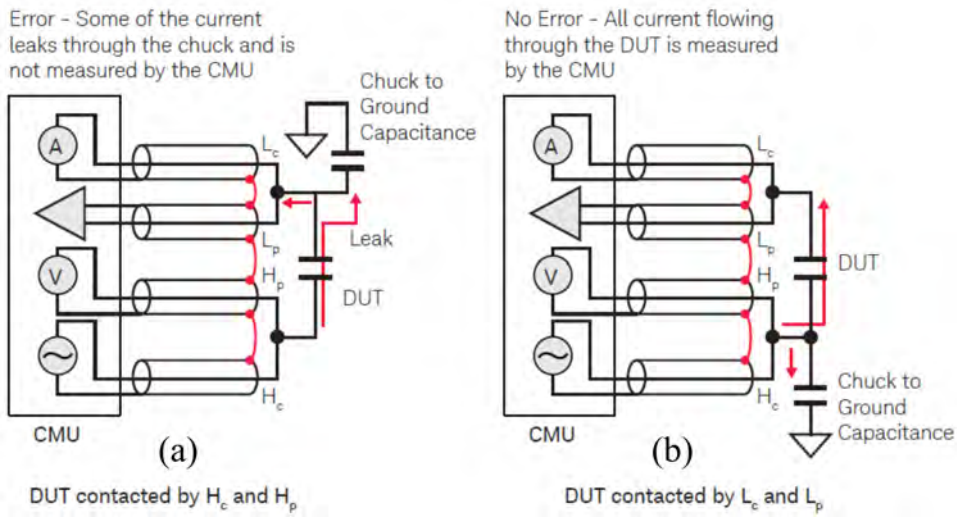


Figure 6.2: Illustration of the importance of probing the Device Under Test (DUT) correctly. (a) Demonstrates the reverse cable convention, resulting in measurement of the leak current. (b) Depicts the correct cable convention, where all current passing through the DUT is measured. The figure is reprinted from [103].

the cable connections are switched. These measurements were performed on Array 1.2 from the wafer processed using the maskless LOCOS method (Chapter 5). Only a subset of the elements was measured to demonstrate the effect. Fig. 6.3 provides two plots summarizing the output of the CV measurements for the conventional cable configuration (Fig. 6.3a) and the reversed cable configuration (Fig. 6.3b). It can be observed that both the series and parallel resistances change over several decades. When the cables are reversed, the parallel resistance decreases by approximately 1 kΩ, while the series resistance increases slightly more than 100 Ω. Additionally, the capacitances exhibit two distinct levels for the reversed cables, whereas for the conventional cable configuration, C_p and C_s have nearly the same value.

These results emphasize the significance of correctly probing the device to obtain representative data when having a conductive substrate.

6.1.2 Impedance Analyzer

The second setup involves the combination of the impedance analyzer and the probe station, which are connected via an in-house made bias tee and a source meter. The setup is illustrated to the right in Fig. 6.1. The probe used is a three-pin probe needle (ACP40-A-GSG-250 from Cascade Microtech) with a pitch of 250 µm, configured with a ground-bias-ground arrangement. However, it is important to note that the last ground pin is disabled and not used in the measurements.

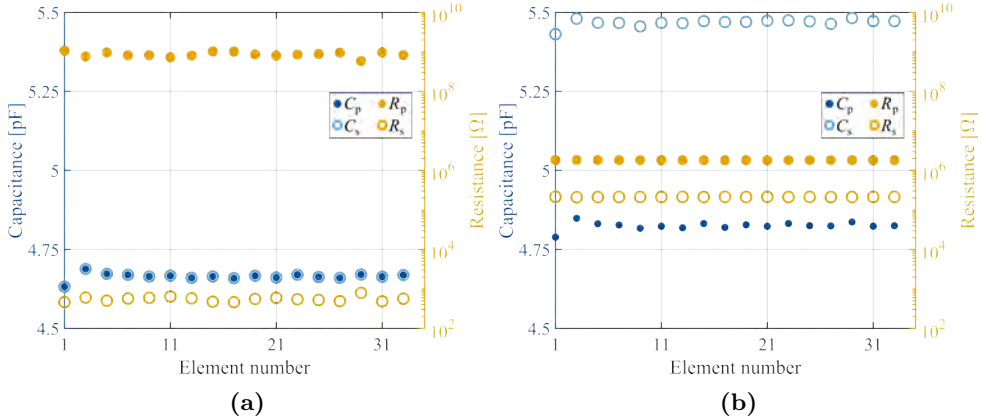


Figure 6.3: Overview plot based on CV data. On the right axis the parallel and series capacitances (C_p and C_s) are shown and on the left axis the parallel and series resistances are plotted (R_p and R_s). a) Shows the data obtained for the conventional bias configuration, while b) shows the results from the reversed bias. Remarkable changes are observed in both the capacitance and resistance levels, emphasizing the significance of correct probing convention for a conductive substrate.

Opposed to the impedance measurements performed using the parameter analyzer, the impedance analyzer offers a broader frequency range from 20 Hz to 120 MHz, which covers the resonance frequency of the currently fabricated devices in this research group. These ranges from approximately 3 MHz in immersion [40] to 65 MHz for transducers designed for airborne applications [41]. The impedance analyzer allows for a maximum of 1601 points per measurement and the setup currently offers up to three sweeps in different ranges to ensure good resolution. The three ranges utilized during initial screening using the impedance analyzer are presented in Table 6.2. The first range, spanning from 40 kHz to 1 MHz, is use to derived the capacitance. The second range, from 1 MHz to 50 MHz, is a wide range used to determine the region of the resonance frequency. The third range is a narrower range around the resonance peak (ranging from 17 MHz to 40 MHz in air for this design) to obtain better data resolution. When a small number of elements have been measured and the region covering the resonance frequency has been identified, it is possible to omit the second sweep in the impedance measurements sequence.

Furthermore, the source meter enables the application of high bias, which is used to determine the resonance frequency, the pull-in voltage, and the stability of the element over time. The applied bias range depends on the specific measurement purpose. When determining the resonance frequency, the bias is swept from 0 V to 240 V, corresponding to approximately 80 % of the pull-in voltage. For pull-in measurements, the applied bias voltage is incremented in steps of 5 V, up to 350 V, ensuring that the CMUT cells

Table 6.2: Sweep parameters for the measurement sequences performed for initial screening using the impedance analyzer.

	Frequency		**Bias**		**Oscillation level**
	start	stop	start	stop	
1st	40 kHz	1 MHz	0 V	240 V	200 mV
2nd	1 MHz	50 MHz	0 V	240 V	200 mV
3rd	17 MHz	40 MHz	0 V	240 V	200 mV

reach the collapse mode. The oscillation level is set to $V_{\mathrm{AC}} = 200\,\mathrm{mV}$ to enhance the distinctiveness of the resonance peak by increasing the SNR.

6.2 Visual Inspection

Prior to beginning the electrical characterization, a visual inspection of the wafers was performed using the optical microscope on the probe station. Table 6.3 presents a quantification of typical errors observed during this inspection. Examples of these errors are depicted in Fig. 6.4.

The first error type (E1) corresponds to missing top plates, which means that the elements are not functional and, consequently, they are not electrically characterized.

The second error type (E2) involves incomplete wet etching during the top electrode separation step, leading to short circuits between neighboring elements. Having a few connected top electrodes on an array is not necessarily a problem, as they still emit a ultrasound. However, the elements locally exhibit a higher pressure. Therefore arrays containing few E2 errors were still electrically characterized.

The third error type (E3) entails dislocated top plates, where fractured top plates are relocated on the wafer, resulting in short circuits between elements. Moreover, elements with missing top plates may exhibit non-capacitive behavior, and as a result, arrays with E3 errors were excluded from electrical characterization.

The fourth error type (E4) encompasses resist errors. In order to protect the wafer during characterization, and the subsequent dicing, a resist layer was spin-coated on top after finalizing the fabrication. Openings were created for the top and bottom electrode pads to enable electrical characterization. Errors in this layer, caused by an incomplete lithography process, can hinder electrical contact, which can appear as abnormal element behavior in the measurement results. This type of error is the only one out of the five, that can be eliminated by removing the resist, exposing the entire array. However, doing so would leave the wafer vulnerable to particles and scratches and it is therefore undesirable. As a result, this approach is only employed when the number of viable arrays is insufficient.

Table 6.3: Defining the types of errors found during visual inspection. Corresponding images are shown in Fig. 6.4.

Error number	Error type
E1	Missing top plate
E2	Connected top plate
E3	Top plate dislocated
E4	Resist error
E5	Miscellaneous

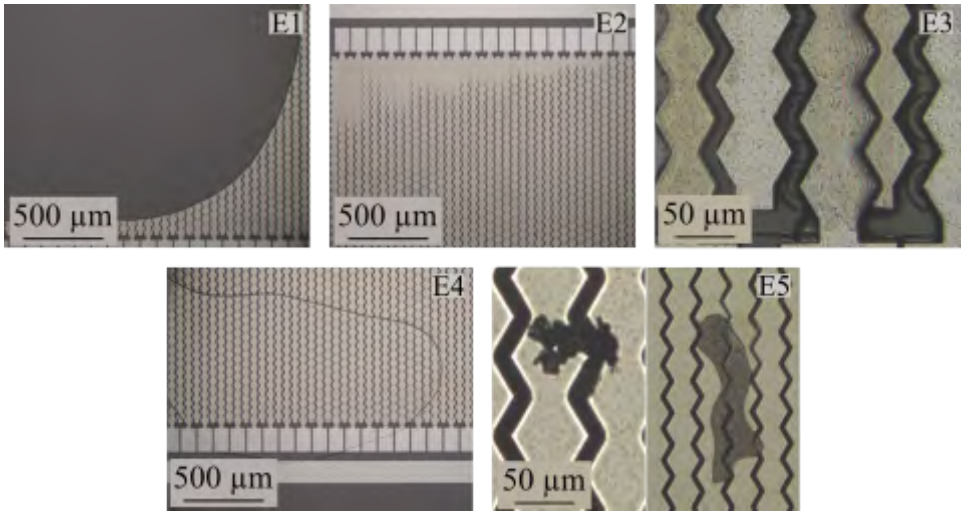


Figure 6.4: Images depicting various types of errors observed during the visual inspection. The arrays have a pitch of 51.33 µm, providing a scale reference. The subfigure numbers correspond to the error types listed in Table 6.3.

The final error type (E5) encompasses miscellaneous errors, such as particles, scratches, flakes and so on. Depending on the location, such errors can contribute to aberrant measurements or cause short circuits between elements. The decision to further characterize arrays containing this error type depends on the number of affected elements.

It should be noted that visual inspection serves as a preliminary screening method and may not detect all errors. Some errors, particularly small ones, can go unnoticed when inspecting an entire wafer. Additionally, certain errors may only become apparent when the objective is intentionally out of focus during inspection. In cases where there are tiny connections between top electrodes, these will appear during electrical characterization. Finally, not all detected errors are deemed significant when considering an entire array. As a result, such arrays are still included in the subsequent electrical characterization.

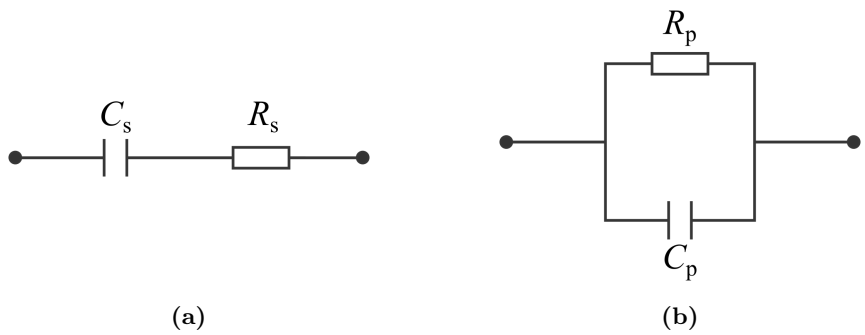


Figure 6.5: Illustrations of the two applied equivalent circuit models. (a) Shows the equivalent model for a capacitor in series with a resistor. (b) Shows the equivalent model for a capacitor in parallel with a resistor.

6.3 Impedance Measurements

The initial type of electrical measurements conducted involved varying the frequency and subsequently measure the resulting impedance (Zf), with an applied AC bias of 50 mV and no applied DC bias. These measurements were performed using the parameter analyzer at frequencies below 1 MHz, due to equipment limitations. The impedance is a crucial parameter used for the initial characterization of the array. In general, impedance refers to the electrical resistance a component offers to the alternating current at a specific frequency. It is represented as a complex number, where the real part corresponds to the resistance, R, and the imaginary part corresponds to the reactance, X. In polar coordinates, it is expressed as the magnitude and phase angle, given by

$$Z = R + iX = |Z|\angle\theta. \tag{6.1}$$

The unit of impedance is ohms ([Ω]). For an ideal capacitor, $R = 0$, thus the impedance and phase can be described as

$$Z_\mathrm{C} = \frac{1}{i\omega C}, \quad |Z_\mathrm{C}| = \frac{1}{\omega C}, \quad \theta_\mathrm{C} = -90^\circ. \tag{6.2}$$

By applying two distinct equivalent circuit models and performing fitting analysis on the measured impedance, it is possible to determine the values of series and parallel resistances (R_s, R_p) as well as the series and parallel capacitances (C_s, C_p). Fig. 6.5 illustrates the two utilized circuit models.

The impedance of the serial circuit, illustrated in Fig. 6.5a, is given by

$$Z_\mathrm{s} = Z_\mathrm{R} + Z_\mathrm{C} = R_\mathrm{s} + iX_\mathrm{s}, \tag{6.3}$$

where Z_R is the impedance of the resistance and Z_C is the impedance of the capacitor.

$$|Z| = \sqrt{R_\mathrm{s}^2 + X_\mathrm{s}^2}, \quad \theta_\mathrm{s} = \tan^{-1}\left(\frac{X_\mathrm{s}}{R_\mathrm{s}}\right), \quad C_\mathrm{s} = -\frac{1}{\omega X_\mathrm{s}}. \tag{6.4}$$

Here R_s is the series resistance and C_s is the serial capacitance derived from the serial reactance, X_s.

In the case of the parallel circuit, shown in Fig. 6.5b, the impedance is defined as

$$\frac{1}{Z_\mathrm{p}} = \frac{1}{Z_\mathrm{R}} + \frac{1}{Z_\mathrm{C}}, \tag{6.5}$$

$$Z_\mathrm{p} = \frac{iR_\mathrm{p}X_\mathrm{p}}{R_\mathrm{p} + iX_\mathrm{p}} = \frac{R_\mathrm{p}X_\mathrm{p}^2}{R_\mathrm{p}^2 + X_\mathrm{p}^2} + i\frac{R_\mathrm{p}^2X_\mathrm{p}}{R_\mathrm{p}^2 + X_\mathrm{p}^2}, \tag{6.6}$$

$$|Z_\mathrm{p}| = \frac{R_\mathrm{p}X_\mathrm{p}}{\sqrt{R_\mathrm{p}^2 + X_\mathrm{p}^2}}, \quad \theta_\mathrm{p} = \tan^{-1}\left(\frac{R_\mathrm{p}}{X_\mathrm{p}}\right), \tag{6.7}$$

where R_p is the parallel resistance and X_p is the parallel reactance defined as $1/\omega C_\mathrm{p}$. However, for the parallel circuit, it is often advantageous to use the reciprocal impedance, called the admittance, which is measured in siemens (S). The admittance is defined as

$$Y_\mathrm{p} = \frac{1}{Z_\mathrm{p}} = G_\mathrm{p} + iB_\mathrm{p}, \tag{6.8}$$

$$|Y_\mathrm{p}| = \sqrt{G_\mathrm{p}^2 + B_\mathrm{p}^2}, \quad \theta_\mathrm{p} = \tan^{-1}\left(\frac{B_\mathrm{p}}{G_\mathrm{p}}\right). \tag{6.9}$$

G_p is the conductance of the resistor and B_p is the susceptance of the capacitor. Based on these definitions the parallel resistance and capacitance can be derived as

$$R_\mathrm{p} = \frac{1}{G_\mathrm{p}} \quad \text{and} \quad C_\mathrm{p} = \frac{B_\mathrm{p}}{\omega}. \tag{6.10}$$

An example of an ideal capacitive element is depicted in Fig. 6.6a, which displays the impedance plotted against frequency on a double logarithmic scale. The phase angle is shown on the secondary y-axis. By assuming an ideal capacitor according to Eq. (6.2), the capacitance of the element can be determined through a linear regression on the measured data using the relation

$$\log(|Z_\mathrm{C}|) = \log\left(\frac{1}{\omega C}\right) = -\log(C) - \log(\omega). \tag{6.11}$$

In this case, since the Zf measurement is conducted without bias, C corresponds to C_0. Fig. 6.6b presents the element capacitance plotted against frequency, demonstrating an ideal behavior with a constant value across all frequencies. However, achieving the ideal case with $R_\mathrm{s} = 0$ or $R_\mathrm{p} = \infty$ is not possible in the measurement setup. As a result, the derived capacitance values C_s and C_p obtained using the models depicted in Fig. 6.5 are considered to be more representative and will be utilized for further data analysis.

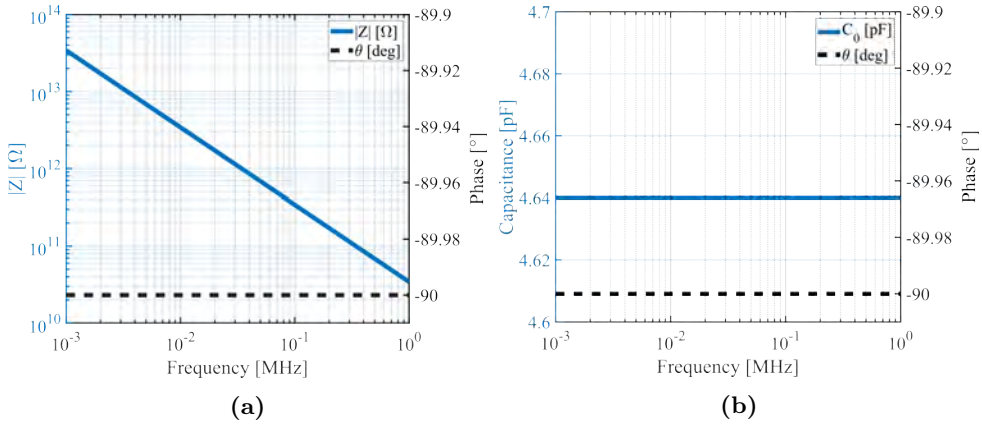


Figure 6.6: Illustration of an ideal capacitive element. (a) On the left y-axis, the magnitude of the impedance, $|Z|$, is plotted on a logaritmic scale, while the right y-axis represents the phase angle, θ. Both are plotted against the frequency on a logarithmic scale. (b) Shows the capacitance, C_0, obtained by Eq. (6.11) on the left y-axis and phase angle, θ on the right y-axis. Both as function of the frequency plotted on a logarithmic scale.

To provide an overview of the data from an entire array consisting of 384 elements, two summary plots have been created using data obtained from the maskless LOCOS wafer, array 4.3, as shown in Fig. 6.7. The first plot displays the derived parameters R_s, R_p, C_s, and C_p, obtained using the circuit models introduced above. Since the parallel resistance represents the resistance in the dielectric material, aiming to prevent leakage currents, the value should be very high ($R_\mathrm{p} \to \infty$). In contrast, the serial resistance describes the resistance in the electrode and connecting wires and is therefore expected to be small ($R_\mathrm{s} \to 0$). From Fig. 6.7a, it can be observed that R_p is approximately 10 GΩ, while R_s is around 10 kΩ, which aligns with the expected behavior.

Furthermore, based on the two introduced circuit models it can be deduced that for a small R_s value and a large R_p value, $C_\mathrm{s} = C_\mathrm{p} = C$, which is also observed in the figure.

The second plot, shown in Fig. 6.7b, provides an overview of the average phase angle, θ, for each element. Ideally, the phase angle should remain consistently around $-90°$, as indicated by Eq. (6.2). In this case, the data exhibit the expected behavior, with the phase angle maintaining a consistent level of approximately $-90°$.

However, the elements do not always exhibit ideal behavior. In the following subsection, some of the most common aberrations will be elaborated.

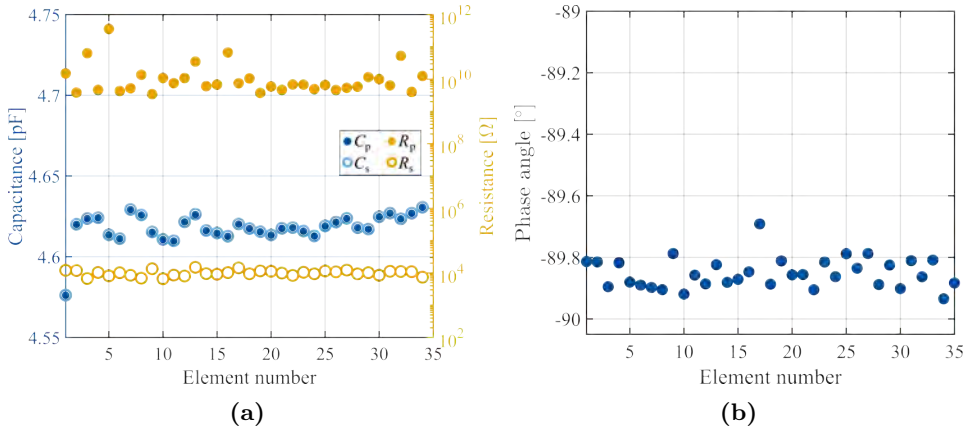


Figure 6.7: Two summary plots based on the Zf measurements are shown. (a) Summarizing the derive parameters C_p, C_s, R_p and R_s. (b) Presenting the average phase angle, θ, found across all frequencies. Both plots shows the data per element. The measurements were obtained from array 4.3 on the maskless LOCOS wafer. Only a selection of elements are shown to demonstrate the behavior.

6.3.1 Measurement Aberrations

During the analysis of the measured data, deviations from the expected capacitive behavior were observed. Some of these deviations were evident from the summary plots discussed earlier, while others could only be observed when examining the Cf curve. Both types of errors will be elaborated upon in the following subsection.

The first type of aberration that can occur is short-circuiting between the top and bottom electrodes. In this case, the element no longer exhibits its capacitive behavior and the phase angle approaches zero, indicating a resistive characteristic. Additionally, the parallel resistance of the element will decrease significantly to a level comparable with the serial resistance, R_s. However, since none of these types of errors were detected among the completed wafers, it is not possible to provide a concrete example of such an artifact.

The second type of aberration to consider is holes in the top plate. While most cases of missing top plates are typically identified and discarded during the visual inspection, it is possible for small holes to stay undetected. Fig. 6.8 illustrates an example of small holes which were not initially detected during the visual inspection but became apparent in the summary plot analysis. The capacitances for the two most affected elements did not fall within the defined acceptance range (4 pF-5 pF), and were therefore visually reinspected.

The third type of measurement aberration arises from short circuits occurring between two or more neighboring top electrodes. These elements

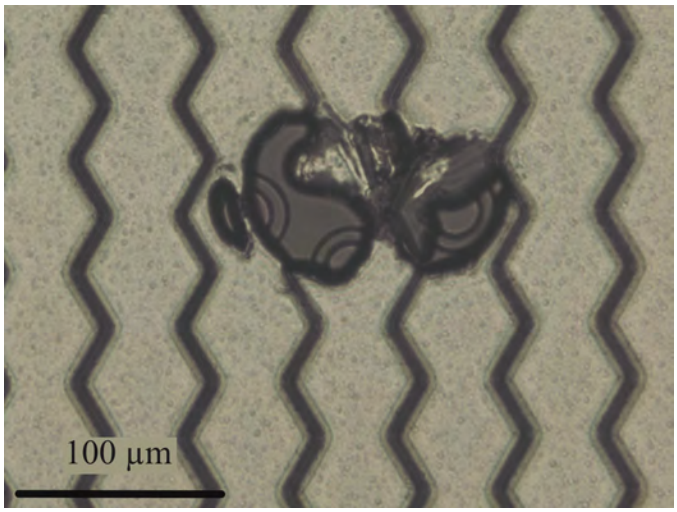


Figure 6.8: Optical microscope image showing a hole in top plate spanning across three elements. This fabrication error is also evident in the measurement.

will still show a capacitive behavior, but the capacitance of each affected element becomes equivalent to the product of the number of connected top electrodes and the capacitance of a single element, corresponding to the capacitors being in parallel. Fig. 6.9 illustrates distinct capacitance levels associated with different numbers of connected elements. The data originates from array 10.3 on the maskless LOCOS wafer. Only a selection of the elements are shown to demonstrate the tendency. The plot reveals a consistent capacitance level of approximately 9.1 pF for element pairs, while a level of around 13.6 pF occurs for three connected neighboring elements, and so on. The highest observed capacitance level is approximately 57.8 pF, representing 13 connected elements spanning from element number 344 to 356. It is worth noting that all these top electrode connections have been visually identified, and a more detailed analysis will be presented in Section 7.1.

The final category of measurement aberrations is a miscellaneous group, primarily identified from the Cf curve. As previously noted, the ideal capacitance curve remains constant over low frequencies, as shown in Fig. 6.6b. However, practical measurements often differ from this ideal behavior with slightly varying capacitance across the frequency range. Within this group of aberrations, Cf curves are found to exhibit bouncing behavior between discrete capacitance levels. Examples of such deviations are illustrated in Fig. 6.10. The common factor in these cases is the occurrence of two discrete capacitance levels, which in most cases corresponds to those of a single element, as well as two connected elements. Both wafers have been thoroughly examined, investigating all elements with abnormal Cf behav-

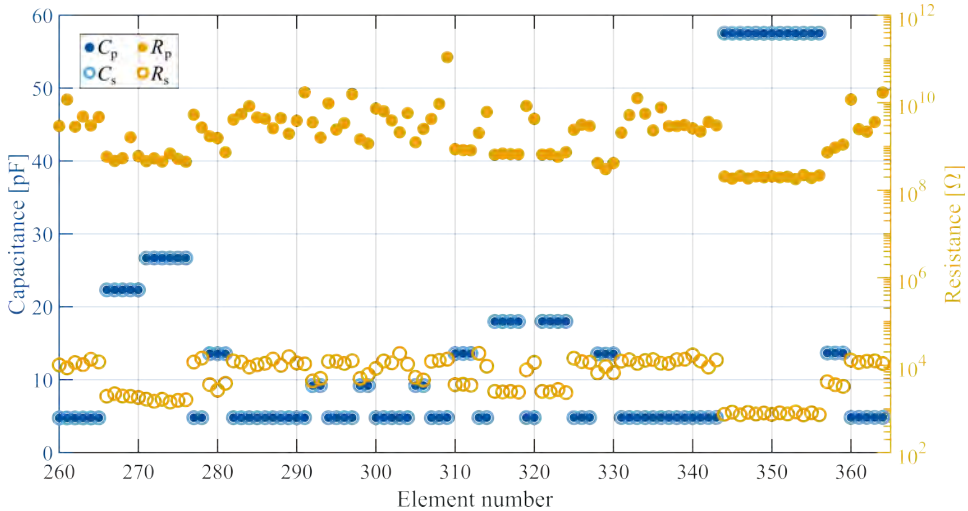


Figure 6.9: Summary plot showing different capacitance levels corresponding to connected top electrodes. The data is from array 10.3 on the maskless LOCOS wafer.

ior, which involved visual inspection and re-measurements. However, visual inspections revealed no visible defects, and most cases of aberrant behavior were resolved by subsequent re-measurements, which exhibited a consistent capacitance level. Furthermore, the majority of these aberrations could not be identified from the summary plot, as the capacitance level appeared unremarkable. Given the absence of recurrent aberrations and the satisfactory results of the re-measurements, these abnormalities are likely attributed to measurement artifacts. One plausible explanation is that during the automatic measurement setup, the needles may collect small particles, which occasionally contact neighboring elements, leading to a rise in capacitance. Alternatively, inconsistencies in the probe needle placement throughout the entire measurement series may account for some of these discrepancies. It is worth noting that only a few of these aberrations were observed, with 15 elements on the double LOCOS wafer and 3 on the maskless LOCOS wafer, representing only 0.2 % and 0.04 % of all measured elements, respectively. These negligible and inevitable measurement errors are typical in automated wafer-level characterizations and are attributed to technical measurement issues.

In summary, the Zf screening method proves effective in identifying significant and well-known errors, such as short circuits between the top and bottom electrodes, small holes in the plate, connected top electrodes resulting in higher discrete capacitance levels, and diverging capacitance spectra. However, due to its unbiased nature, the Zf measurements cannot reveal charging problems. To address this, a comprehensive array characterization

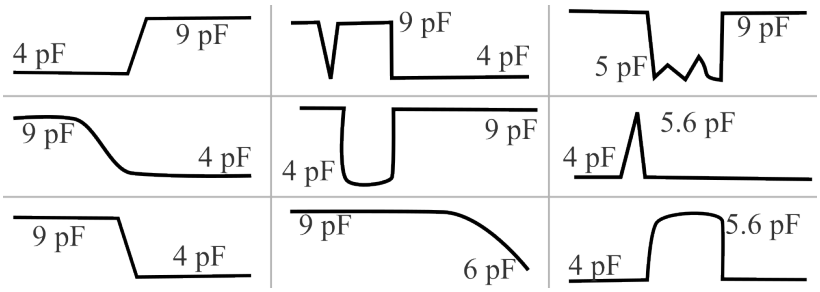


Figure 6.10: Sketches of different aberrant appearances observed in the Cf curves.

Table 6.4: The selection criteria used to identify the most promising arrays for further characterization.

Criteria	Indicator
Capacitive behavior of all elements	$\theta = -90°$, $R_\mathrm{p} \sim \mathrm{G\Omega}$, $R_\mathrm{s} \sim \mathrm{k\Omega}$
None connected top electrode	Constant capacitance level $= C_0$
None aberrant elements	Constant levels in C_s, C_p, R_p, R_s

using a CV measurement is necessary.

One notable advantage of this novel screening method is its ability to considerably reduce the characterization time while still achieving a complete wafer-level assessment. Acquiring Zf data from all elements of the 29 arrays can be completed in less than two days. This represents a remarkable reduction of approximately 93 % compared to the 31 days required for a complete wafer-level characterization. Nonetheless, it is important to note that for arrays selected for further post-processing and probe mounting, a thorough characterization using CV measurements remains essential. This process typically takes around half a day per chosen array.

Based on the acquired knowledge and the summary plots presented in Fig. 6.7, selection criteria for further characterization can be established. These criteria are listed in Table 6.4. However, the specific limits and criteria may vary depending on the overall characteristics of the wafer.

As an alternative to this proposed wafer-level characterization method, the paper "Performance assessment of CMUT arrays based on electrical impedance test results" [102] suggests to use the element frequency as a figure of merit. This method requires a biased Zf measurement, where the bias is adjusted for each design to achieve a distinct resonance peak. To reduce the measurement time, the authors of the article suggest measuring only the ten outer elements and every fifth element in-between. It should be noted that the Zf measurements in this approach were exclusively performed for frequencies around the first eigenfrequency. Despite the applied bias, this characterization method does not provide information about potential element charging effects. Furthermore, only 32 % of the elements

were measured leaving no information about failures in the remaining 68 % of the elements.

6.4 Voltage Measurements

This section elaborates on the subsequent set of measurements performed on a selection of arrays chosen from the Zf characteristics. Here a measurement sequence has been used were the current is first measured as function of the applied voltage followed by a capacitance measurement relative to the applied voltage. Recall, the parameters used in the measurements are shown in Table 6.1. The applied frequency should be adjusted according to a constant level in the Cf measurement, which is usually below 100 kHz. Both types of voltage sweeps are performed using the parameter analyzer.

6.4.1 IV Measurements

In previous studies conducted in this group, IV measurements have been used to detect short circuits between the top and the bottom electrode. These measurements used to be acquired in a sequence with Zf, IV, and CV. The characterization was performed on a limited number of elements, which were evenly distributed across different arrays on the wafer. The selection of these arrays was solely based on visual inspection.

However, with the new wafer-level characterization method, IV measurements may not provide additional information, since short circuits are already identified through the Zf measurements, and arrays containing numerous short circuits are already discarded during the previous selection step. Thus, the conventional use of IV characteristics in this group is not necessary for the newly proposed characterization method. In this thesis, the validity of this statement was verified through IV measurements. Two sets of IV measurements were conducted. The first set varying the voltage from 0 V to 100 V, and the second set varying the voltage from 0 V to −100 V.

Conventionally, the maximum current of each element have been used to categorize them into three groups: *short-circuited*, *not connected*, and *working* elements. The precise cutoff limits should be determined based on the design and fabrication process. In this study, the upper compliance level was set at 100 µA, and the lower compliance level was set at 0.2 pA. Elements with a maximum current between these values were considered *working* elements. Since all elements showed a current within the defined compliance levels, examples of *short-circuited* or *not connected* elements cannot be given.

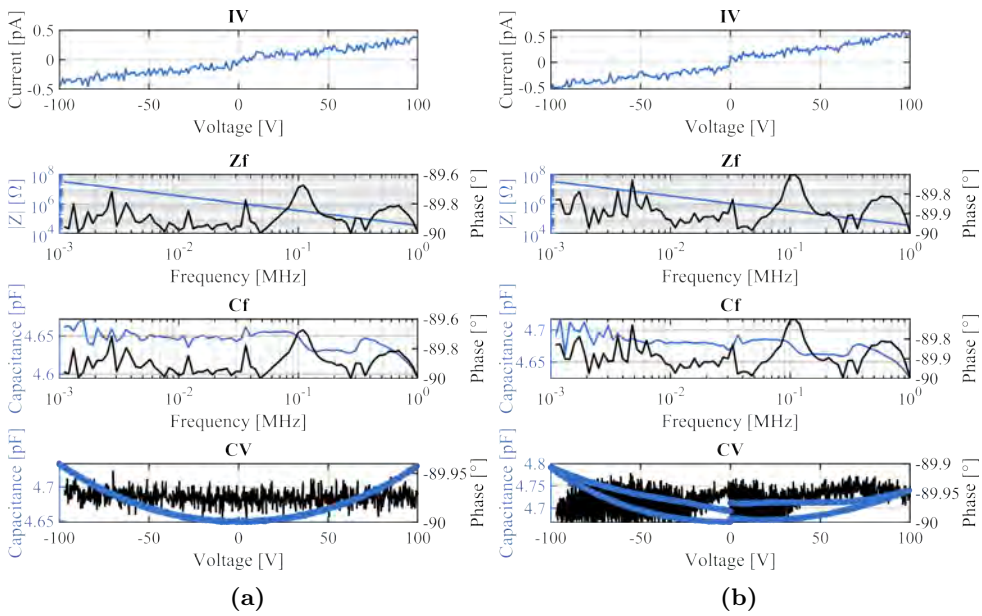


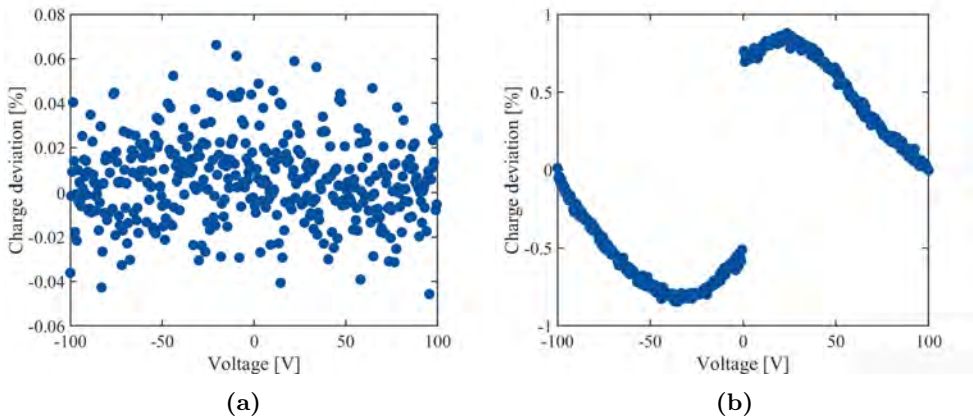
Figure 6.11: Comparison of data with and without hysteresis. (a) Ideal data set with low current, capacitive Zf behavior and no hysteresis in the CV curve. The data is from the maskless LOCOS wafer. (b) Data set with low current, ideal capacitive behavior in Zf curve, but hysteresis revealed in the CV curve. The data is from the double LOCOS processed wafer. Both data set are from array 2.2, center element number 192.

6.4.2 CV Measurements

The CV measurements were carried out subsequent to the IV measurements to assess the capacitive behavior of the elements under applied bias. Each CV sweep was comprised of four individual measurements, with the voltage being swept from 0 V to 100 V and back to 0 V in order to detect any undesired hysteresis effects. Similarly, two sweeps were performed with negative bias from 0 V to −100 V and back to 0 V. If the voltage sweeps in both directions are indistinguishable, indicating the absence of mobile charging effects, the element demonstrates optimal behavior. The measurements were conducted at a frequency of 50 kHz, determined by observing a constant level in the Cf curve.

Fig. 6.11 provides a comparison between two datasets: one obtained from a wafer processed using the maskless LOCOS method, and another obtained from a wafer processed using the double LOCOS process.

The CV curve in Fig. 6.11a from the maskless LOCOS processed wafer display no hysteresis, as the curves in both bias directions are indistinguishable. In contrast, Fig. 6.11b from the double LOCOS processed wafer clearly exhibits hysteresis in the CV curve, as the curves are distinguishable in both



(a) **(b)**

Figure 6.12: Relative charge deviation found on an element with hysteresis **(a)** and on an element with no charging **(b)**. The data in **(a)** is from the maskless LOCOS wafer, while **(b)** is from the double LOCOS wafer. Both data set are from array 2.2 element 192 on the respective wafer.

bias directions. This observation imply the presence of mobile charges in the CMUT element. Both datasets originates from array 2.2, specifically from element number 192.

The IV, Zf, and Cf curves exhibit similar behavior for both wafers, confirming that charging effects cannot be predicted based on the Zf and IV measurements. Therefore, a comprehensive array characterization necessitates the inclusion of CV measurements.

A way to quantify the hysteresis effects is by evaluating the relative deviation of charges with respect to the applied bias. The charge on the capacitor plates is given by the product of the capacitance and the voltage, expressed as

$$Q = CV.$$

To calculate the relative deviation in percent, the following equation is used for each applied voltage

$$Q_{\text{deviation}} = \frac{Q_{\text{down}} - Q_{\text{up}}}{Q_{\text{up}}} \times 100. \tag{6.12}$$

By applying this relation to the data presented in Fig. 6.11, the two plots in Fig. 6.12 are generated. Fig. 6.12a corresponds to the element without mobile charges, displaying only the inherent noise in the data. It is important to note that the maximum deviation observed in this case is 0.07 %. In contrast, Fig. 6.12b illustrates the relative charge deviation in percent for the element exhibiting hysteresis. Here a clear correlation can be observed in the data. Moreover, it is evident that the maximum deviation

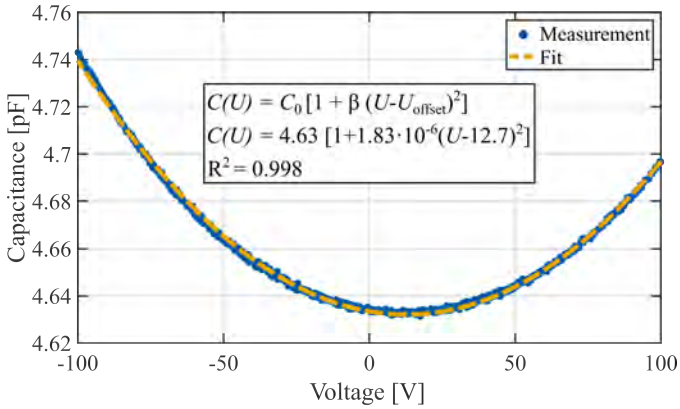


Figure 6.13: CV data obtained from array 4.3 on the maskless LOCOS wafer. The expression in Eq. (6.13) is fitted to the data revealing a voltage offset of 12.7 V.

for the hysteresis case is significantly larger in magnitude compared to the data without hysteresis. The maximum deviation is 0.9 % and is utilized as a measure of hysteresis. The specific threshold for accepting the element should be determined based on the overall characteristics of the measured arrays.

Furthermore, a fitting function for the capacitance, denoted as $C(V)$, can be derived using the Taylor expansion method, as described in [39]. This function enables the fitting of the CV curve at small voltages relative to the pull-in voltage (below 40 %), and is expressed by

$$C(V) = C_0[1 + \beta(V - V_{\text{offset}})^2], \tag{6.13}$$

where C_0 represents the minimum capacitance, β is a fitting constant, V corresponds to the applied potential, and V_{offset} denotes an offset that shifts the vertex, representing the minimum capacitance, away from $V = 0\,\text{V}$. This offset is a consequence of the built-in electrical field present in the CMUT structure, primarily originating from the bandgap difference between the heavily doped n-type substrate and the heavily doped p-type top plate. Fig. 6.13 is an example of a CV curve with a notable voltage offset. The data are acquired from array 4.3 on the maskless LOCOS wafer.

In summary, the newly developed wafer-level characterization method has successfully demonstrated the effectiveness of the Zf screening in detecting common and critical errors in the transducer arrays, including short circuits between the top and bottom electrodes, plate defects, and connected top electrodes. In contrast, the conventional screening tool, the IV measurement, does not provide additional insights for selecting the best arrays. Furthermore, it has been observed that neither Zf nor IV measurements can identify hysteresis effects in the arrays.

In comparison to the previous characterization method employed in this research group, which involved a sequential sweeping of Zf, IV, and CV, the new method requires only one sweep per element to obtain a comprehensive overview of the entire wafer. This represents a significant improvement over the previous approach, which necessitated seven sweeps per element. By utilizing the informative Zf sweep to detect various types of errors, the more time-consuming CV characterization can be focused on promising arrays only. However, it is important to note that the full wafer-level Zf sweep, covering 384 elements on 29 arrays, still requires approximately 37 hours to complete. Thus, alternative methods can be considered due to time constraints.

An alternative approach is suggested in [102], involving the measurement of the ten outer elements and every fifth element in-between, which accounts for approximately 32 % of the total number of elements. Although this approach will significantly reduces the measurement time to around 12 h for the design presented in this thesis, it may not detect certain errors, such as connected top electrode pairs or small plate defects covering less than five elements. Therefore, the available time and the choice of characterization method may have an impact on the results obtained.

6.5 Yield

The assessment of the wafer quality is commonly referred to as wafer yield, although different definitions of yield are often employed. In this thesis, the yield is categorized into distinct types: fabrication yield, capacitor yield, capacitance-level yield, and charging yield.

The fabrication yield is determined after finalizing the wafer fabrication in the cleanroom and relies solely on visual inspection and fabrication success. Section 6.2 provides an explanation of the most commonly observed errors and the inspection method. The yield is calculated by comparing the number of arrays that appear satisfactory for electrical characterization to the total number of arrays on the wafer. Arrays containing minor visual imperfections that are deemed insignificant for the overall array performance are estimated as acceptable, contributing positively to the visual yield.

The capacitor yield encompasses the number of elements exhibiting optimal capacitive behavior based on the initial electrical characterization. This is compared to the total number of elements screened using Zf measurements. An optimal capacitive element is defined by a phase angle of $-90°$ at low frequencies and an impedance curve consistent with that of a capacitor, as elaborated in Section 6.3 and illustrated in Fig. 6.6a. Additionally, these elements should demonstrate a high R_p value and a low R_s value.

The yield related to the capacitance-level is determined by comparing the

number of top electrodes that exhibit the expected capacitance according to the design with the total number of functioning capacitive elements that have been measured. An increase in capacitance level is often indicative of connections between neighboring top electrodes, which is explained in Subsection 6.3.1.

Lastly, the charging-related yield is defined as the number of elements that exhibit ideal capacitive behavior under bias, indicating the absence of hysteresis effects in either bias direction. This yield is calculated relative to the total number of elements measured using a CV sweep.

These definitions will serve as an overall measure for analysis of the wafers described in Chapter 7.

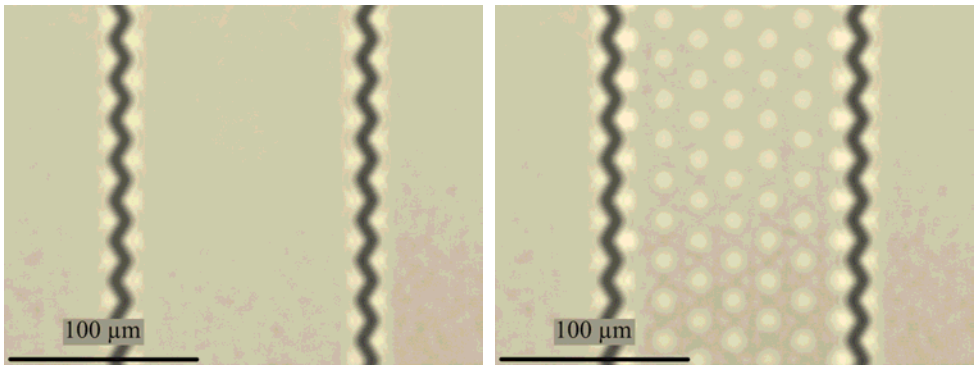
6.6 Pull-in and Frequency Analysis

After finalizing the characterization process using the parameter analyzer, identification of the best array should be based on the obtained results. Typically, only arrays intended for probe mounting undergo analysis using the impedance analyzer, as it currently does not offer semi-automatic measurements.

Initially, the pull-in voltage is determined. However, it is essential not to perform this measurement on the array designated for probe mounting to prevent potential damage. Instead, an array close to the optimal array is selected to obtain a reliable result. Alternatively, the test arrays placed around each 384-element array can serve this purpose.

The pull-in voltage is determined by applying a bias ramp with a high maximum voltage and conducting a Zf sweep. The initially applied maximum bias corresponds to the designed pull-in voltage. The voltage ramp starts with a coarse step size at low voltages and transitions to a finer step size near the expected pull-in voltage. The maximum voltage can then be adjusted until the pull-in voltage is found. For this design, the maximum applied voltage was 350 V.

The pull-in voltage is determined by analyzing the peak value of the phase angle relative to the applied bias. A decrease in the phase angle is observed when the cells reach the pull-in voltage. Additionally, the occurrence of pull-in can be visually observed as the cells gradually become more prominent when the plate is pulled down. This is illustrated by comparing the images in Fig. 6.14. It is evident that at zero applied bias (Fig. 6.14a), no cells are collapsed, while at a bias of 350 V (Fig. 6.14b), all the cells are in the collapse mode. It should be noted that the intentionally out-of-focus images serve to demonstrate this effect. The paper [71] presents and demonstrates an alternative approach using similar microscope images for



(a) **(b)**

Figure 6.14: Images illustrating the pull-in mode visually. The images are from test array F4. The images are intentionally out of focus, to show the collapsed cells. (a) Zero applied bias showing no collapsed cells. (b) An applied bias of 350 V results in collapsed cells.

a visual pull-in methodology. This method determines the pull-in voltage of individual CMUT cells, in contrast to the conventional method applied above, which provides in an average pull-in voltage across an element.

Once the pull-in voltage has been determined on a test array, the next step is to find the resonance frequency of the array intended for probe mounting. This is achieved through a biased Zf measurement. Due to the limitations of automatic stepping along the array, only a few elements were measured. For this purpose, the first six and last six elements, as well as the six center elements, were chosen.

To determine the element frequency, a bias is applied. As the bias approaches the pull-in voltage, the peak in both the impedance and in the phase curve becomes more pronounced. Therefore, a voltage sequence ranging from zero bias to 240 V, corresponding to 80 % of the pull-in voltage, V_{pi}, for the maskless LOCOS wafer, is selected. The applied parameters are summarized in Table 6.2. Additionally, the spring softening effect can be observed from this type of measurements. As the applied bias increases, the CMUT plate gradually moves closer to the bottom substrate, resulting in voltage-dependent spring softening, as explained by Eq. (2.23). This effect is evident through a peak shift towards lower frequencies with increasing bias, as depicted in Fig. 6.15.

Finally, the frequency peaks can be utilized to determine the electromechanical coupling coefficient, k_{em}^2, which quantifies the efficiency of the conversion between electrical and mechanical energy. The coupling coefficient, defined as a percentage, can be calculated using the resonance frequency

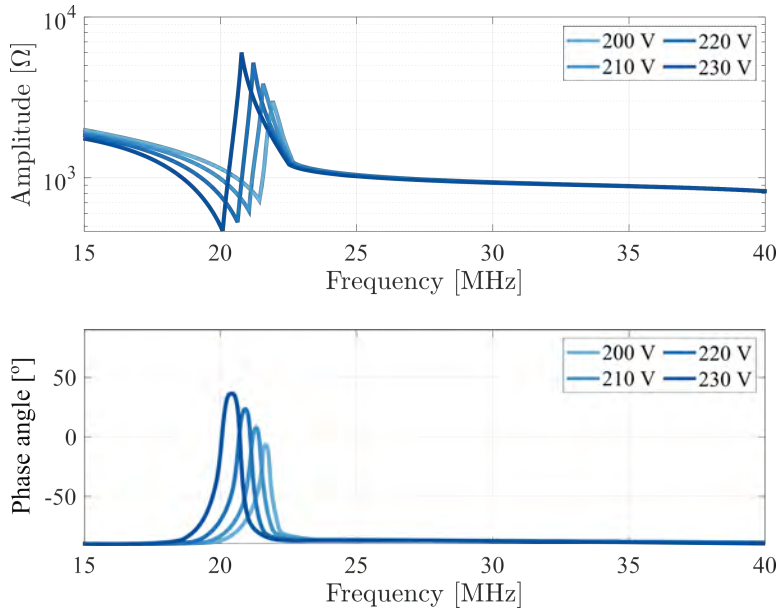


Figure 6.15: Illustration showing an ideal impedance measurement for various applied bias voltages. The spring softening effect is illustrated by the decreasing peak frequency with an increasing bias.

(f_{res}) and the anti-resonance frequency (f_{antires}) as follows [104]

$$k_{\text{em}}^2 = \left[1 - \left(\frac{f_{\text{res}}}{f_{\text{antires}}}\right)^2\right] \times 100\%. \tag{6.14}$$

6.7 Stability Measurements

Following the determination of the pull-in voltage and the resonance frequency, a continuous impedance measurement is conducted to assess the long-term performance of the CMUT. The DC bias is systematically varied between the positive and negative absolute maximum bias that can be applied by the commercial scanner available, which in this case corresponds to ±180 V. Each bias step is maintained for a duration of 15 min, resulting in a total measurement time of 2 h. The ramp function used for varying the bias is depicted in Fig. 6.16. Since this stability test is time-consuming, it is typically performed on a single element. However, it can be conducted on an element of the array designated for probe mounting, as it is non-destructive.

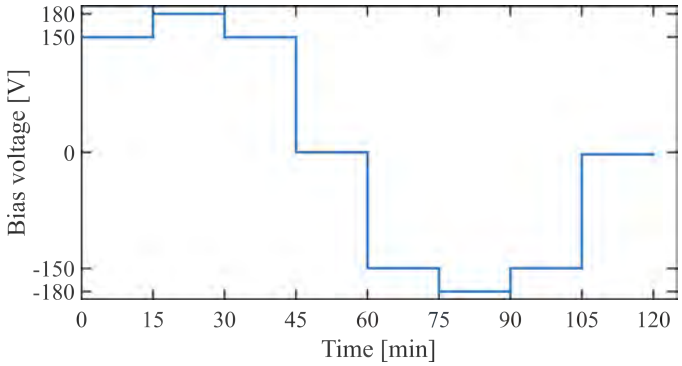


Figure 6.16: Plot showing how the bias is applied over time during a stability measurement.

6.8 Chapter Summary

A novel wafer-level characterization method for electrical analysis has been introduced. Two measurement setups were employed: one connecting the Cascade Summit 12K probe station to a B1500A Semiconductor Parameter Analyzer, and the other connecting the probe station to an Agilent E4990A Precision Impedance Analyzer.

The proposed wafer-level characterization method employs a step-wise selection approach, focusing only on the most promising arrays to save time compared to a comprehensive characterization of all arrays. Initially, a visual inspection were conducted, where any visibly damaged arrays were discarded and not subjected to electrical measurements. Subsequently, a Zf screening was performed on the remaining arrays retained during the visual inspection. This measurement type was employed to identify various issues, including shorts between the top and bottom electrodes, as well as connected top electrodes. Based on the Zf characterization results, the most promising arrays were selected for a comprehensive CV analysis to investigate any charging phenomena. The charging effects were quantified by the charges on the capacitor plates relative to the applied bias.

Following the CV analysis, one or two arrays designated for probe mounting were chosen for further characterization using the impedance analyzer. The initial parameter of interest was the pull-in voltage, which was determined on a neighboring test element to avoid damaging the actual array. The pull-in voltage could also be observed visually. Subsequently, the resonance frequency and electromechanical coupling coefficient were determined through biased Zf measurements. Furthermore, a long-time stability measurement was conducted on a single element to assess the performance of the CMUT over an extended period of time.

The newly proposed characterization method significantly reduces the characterization time compared to the previous method employed by this

research group. However, depending on the available time for characterization, additional selection criteria may need to be considered. One suggestion to reduce the required time is to decrease the number of elements characterized per array, following a similar approach as outlined in [102].

CHAPTER 7

Electrical Wafer-Level Characterization: Results

This chapter presents the results of the electrical characterization conducted on the two wafers successfully fabricated. To facilitate the analysis of the extensive datasets, a semi-automatic plotting tool was developed. This tool generates plots and output tables, streamlining the analysis process. The automatized script allows the user to define various limits, such as acceptable current range, capacitance fit, and hysteresis calculations. The output tables enables easier identification of the best arrays selected for further characterization.

The first section focuses on the characterization of the wafer fabricated using the maskless LOCOS process, while the second sections describes the wafer fabricated using a double LOCOS fabrication method. The two characterized wafers are the ones compared in Fig. 5.11, where the wafer fabricated using the double LOCOS process exhibited misalignment of approximately 3 µm, while the wafer from the maskless LOCOS batch show a misalignment of 1.5 µm.

Each section follows the methodology presented in Chapter 6, starting with a visual inspection to select the arrays for subsequent characterization. Following this, unbiased impedance measurements are performed to provide an overview of the wafer's performance and identify any anomalies, which are then classified into the groups defined in Subsection 6.3.1. The subsequent results pertain to voltage-based measurements, showcasing the capacitance, resistance, and current levels of the individual elements.

After presenting the results obtained from the measurements conducted on the parameter analyzer, the yield is discussed, calculated and categorized in the same manner as described in Section 6.5.

Finally, for the maskless LOCOS wafer, measurement results from the

Table 7.1: This overview presents the errors detected through visual inspection of the 384-element arrays. The error numbers correspond to those in Table 6.3. The arrays labeled in gray were not subjected to further characterization.

Array no.	Error	Array no.	Error	Array no.	Error
1.2	E5	5.3	E5	9.3	-
2.2	-	6.1	E2	10.1	E1, E2, E4
3.1	E5	6.2	E1, E3	10.2	-
3.2	-	6.3	E5	10.3	E2, E5
3.3	E1	7.2	E3	11.1	E2, E3
4.1	E5	8.1	E2, E4, E5	11.2	E3, E5
4.2	E4, E5	8.2	-	11.3	E2, E5
4.3	-	8.3	E5	12.2	E2, E5
5.1	E1, E2	9.1	E1, E2, E4	13.2	E2
5.2	-	9.2	E3		

impedance analyzer are presented. These measurements includes determining the center frequency, the pull-in voltage and conducting long-term stability tests.

7.1 Maskless LOCOS Wafer

This section describes the results obtained from the maskless LOCOS wafer in details.

7.1.1 Visual Inspection

Initially, the optical microscope integrated into the probe station was utilized to conduct a visual inspection of the wafer. The inspection findings for the 384-element arrays are summarized in Table 7.1. The analysis reveals that the most prevalent error observed is the interconnection of top plates, which is caused by incomplete metal etching. This issue should receive greater attention in future processes. Another category of errors frequently observed across multiple arrays is the miscellaneous group. These errors are more challenging to address as their specific causes remain unknown. However, it is advisable to increase focus in reducing particles present during the fabrication process. Arrays marked with gray exhibited significant errors and were consequently excluded from further characterization.

For the 16 element arrays the visual inspection results are provided in Appendix H. Here, Table H.1 presents the inspection outcome for the *Single* design, while Table H.2 summarizes the results for the *Filled* design. Out of

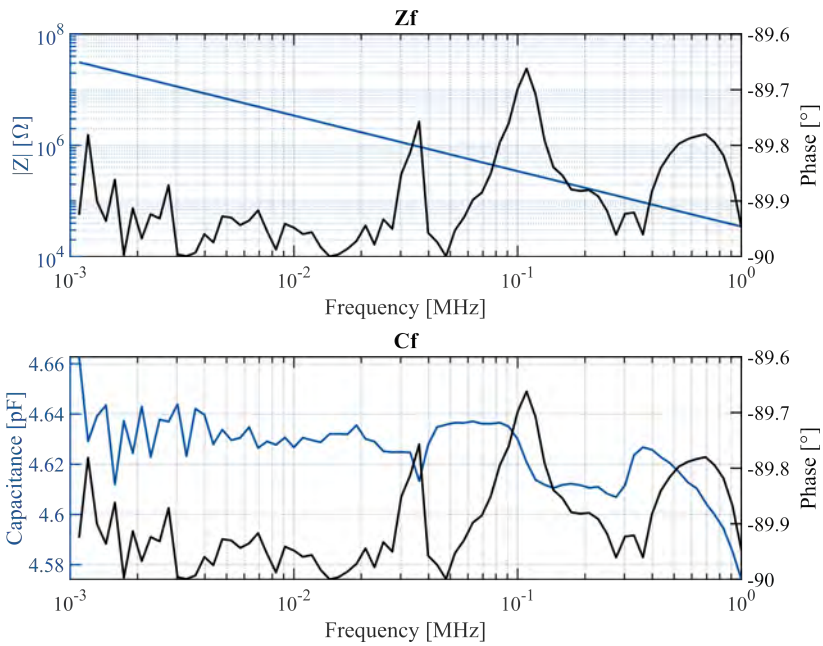


Figure 7.1: Data obtained from array 4.3 of the maskless LOCOS wafer, element number 192. The top graph illustrates the expected capacitive behavior, while the bottom plot demonstrates a consistent level of capacitance across the applied frequency range.

the total of 26 arrays, six were deemed unsuitable for further characterization and were consequently excluded.

7.1.2 Impedance Measurements

The Zf measurements were conducted on a total of 19 arrays consisting of 384 elements, along with an additional set of 20 arrays with 16 elements. An illustration of the obtained Zf and Cf data for the center element (element number 192) on array 4.3 is presented in Fig. 7.1. The figure demonstrates the expected capacitive behavior, revealing a linear relationship between the impedance and the frequency, when plotted on a double logarithmic axis. Additionally, the phase remains approximately $-90°$ across the entire frequency range, aligning with the expected behavior. The capacitance exhibits a nearly constant value of 4.58 pF, which corresponds to the theoretical value of 4.53 pF calculated by combining Eq. (2.9) and Eq. (2.10).

Figure 7.2 presents an overview of the parameters R_s, R_p, C_s, and C_p for the same array. The variation in C_p across the array is minimal, with a negligible difference of 0.08 pF between the maximum and minimum values. The serial resistance, R_s, constantly remains within the kΩ range, while the parallel resistance, R_pm is constant in the GΩ range. The chosen acceptance criteria for this design are R_s being less than 200 kΩ and R_p being greater

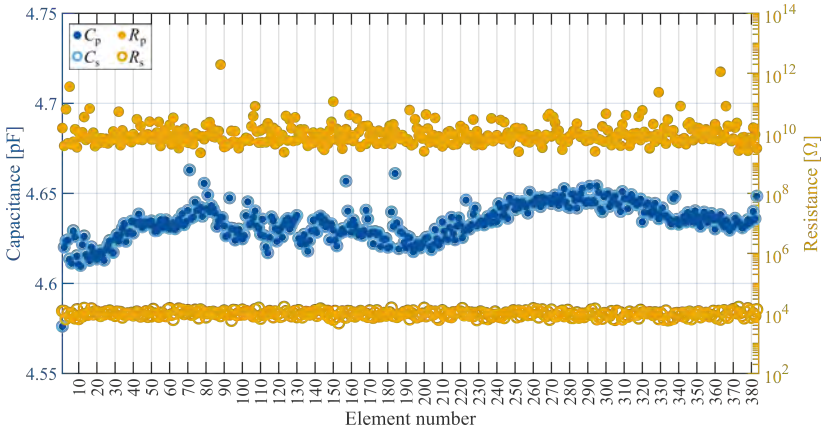


Figure 7.2: This plot provides a summary of the C_s, C_p, R_s, and R_p data for all elements on array 4.3 from the maskless LOCOS wafer. It reveals that all parameters exhibit constant levels, resembling those of an ideal array.

than 1 MΩ

The average phase angle for each element is displayed in Fig. 7.3, indicating an approximate phase angle of −90° for all elements. This phase angle corresponds to the characteristic behavior of a capacitor. Elements with a phase angle below −80° are considered capacitive elements. The combination of these two plots, utilizing the Zf data, demonstrates a very good initial array characteristic.

By conducting this analysis on all 19 arrays with the specified criteria, it was observed that all measured elements exhibited a phase angle of less than −80°. Additionally, all R_p values exceeded 1 MΩ, while all R_s values were below 200 kΩ. This confirms that all measured elements meet the first criteria of capacitive behavior outlined in Table 6.4.

The second criteria, which states that the array should exhibit a consistent level of capacitance, is determined based on the maximum variation of C_p observed across an array. These maximum deviation values are summarized in Table 7.2. Based on the table, the best arrays that satisfy the second criteria in Table 6.4 can be identified. A total of seven arrays demonstrated a maximum deviation below 0.5 pF.

The more significant deviations observed (being above 4 pF) often indicate instances of connected top plates, as seen in the case of array 10.3. As mentioned in Chapter 6, the levels depicted in Fig. 6.9 correspond to the number of connected top electrodes multiplied by the capacitance of a single element. Images showing these connections for certain examples found in array 10.3 are presented in Fig. 7.4. Specifically, subfigure a) illustrates the connections between elements 315 to 318, subfigure b) demonstrates the connection between elements 357 to 359, and subfigure c) depicts the thirteen connected elements resulting in a capacitance of 57.5 pF (with element

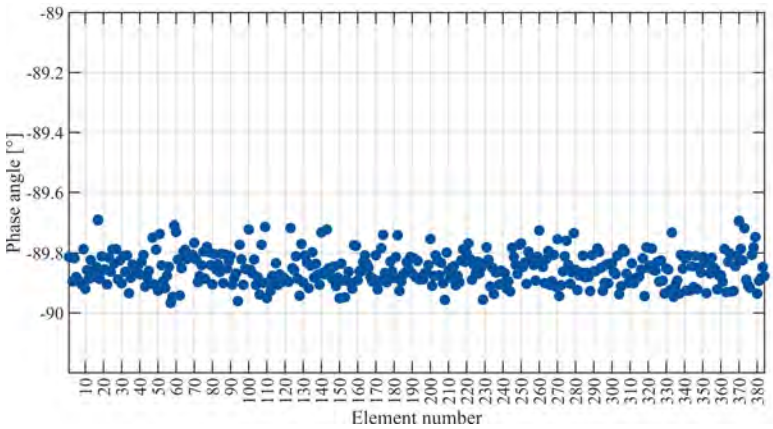


Figure 7.3: This plot provides a summary of the phase angle, θ, for all elements on array 4.3 of the maskless LOCOS wafer. A constant level is observed around $-90°$ across all elements, indicating ideal capacitive behavior.

Table 7.2: The table provides an overview of the maximum deviation in C_p of all arrays measured with Zf measurements on the maskless LOCOS wafer. The four arrays highlighted in blue were selected for further characterization.

Array no.	C **dev.** [pF]	**Array no.**	C **dev.** [pF]	**Array no.**	C **dev.** [pF]
1.2	0.08	5.2	0.10	9.2	4.34
2.2	0.08	5.3	0.12	9.3	0.15
3.1	0.19	6.2	14.02	10.2	4.37
3.2	8.59	6.3	0.11	10.3	53.72
4.1	8.81	7.2	4.34	11.2	11.10
4.2	0.10	8.2	4.33		
4.3	0.09	8.3	4.10		

number 344 to 356).

Due to time constraints, further characterization focused on four arrays out of the seven arrays, which showed a small capacitance deviation. These are marked in blue in Table 7.2. To select these four arrays, the final selection criterion from Table 6.4 was utilized. Among these seven array with a low maximum deviation, three of them exhibited a distinct trend in capacitance, where the capacitance increased with the element number. An example illustrating this behavior is shown in Fig. 7.5. However, the reason for this particular pattern has not yet been identified. As this characterization serves as a proof of concept, additional categorization has also been performed on the worst-performing array (array 10.3) based on the Zf measurements.

It should be noted that the selection criteria for further characterization depend on the number of arrays to be analyzed and the overall performance

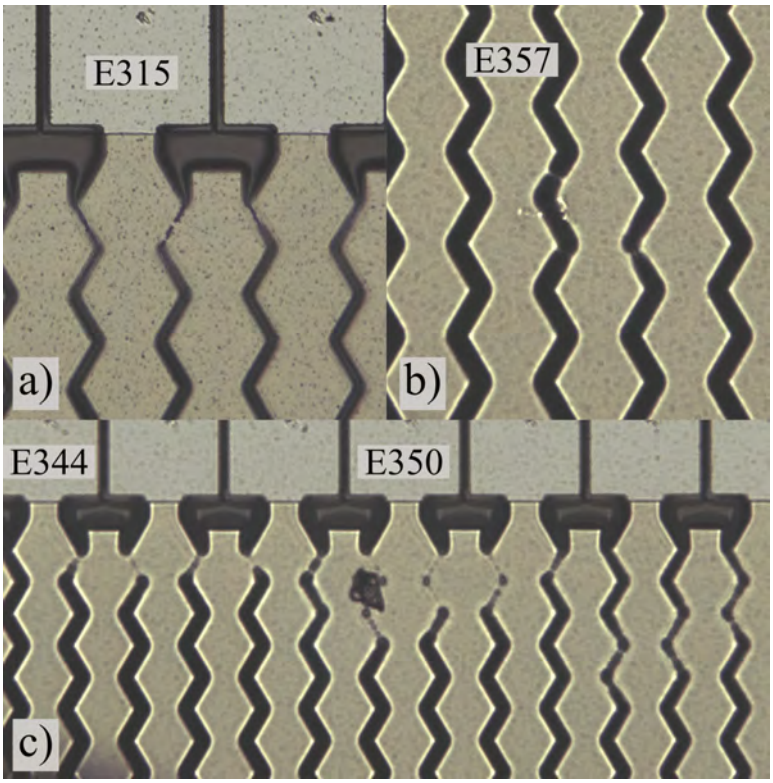


Figure 7.4: The images depict the visual representation of a selection of the top electrode connections identified through the Zf measurements. These images are from array 10.3 from the maskless LOCOS wafer.

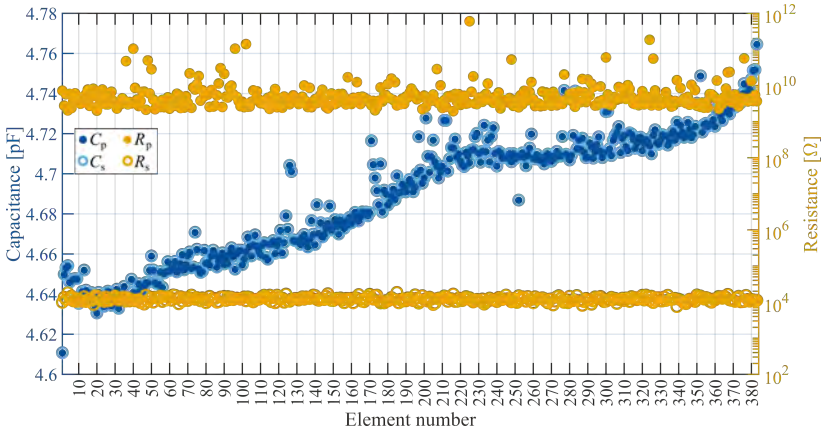


Figure 7.5: This example demonstrates a noticeable pattern in the capacitance levels observed across an array. The data presented here are from array 9.3 of the maskless LOCOS wafer.

of the wafer. In the case of a high-quality wafer, stricter criteria may be necessary, while a wafer with lower quality may allow for a wider acceptance range in the selection criteria.

Proceeding to the 16-element arrays, all 20 measured arrays satisfied the previously defined requirements, exhibiting capacitive behavior. In Table 7.3 the maximum deviation in capacitance is displayed. The array numbering utilizes a prefix to indicate either the *Single* design (S) or the *Filled* design (F), as explained in Section 3.2. The theoretical capacitance for the *Single* design was calculated to 6.27 pF, which aligns well with the measured data having values between 6.16 pF and 6.24 pF. For the *Filled* design the theoretical capacitance was calculated to 43.87 pF, which is slightly higher than the measured values ranging from 39.4 pF to 39.7 pF. The theoretical calculations were performed by combining Eq. (2.9) and Eq. (2.10). Based on the table, it is observed that array F11 stands out with a significantly larger maximum deviation compared to the others. The overview plot in Fig. 7.6 for this specific array reveals levels corresponding to connected top electrodes in 14 out of 16 elements. Despite this observation, due to the limited number of elements and the resulting shortened characterization time, all 20 arrays were subjected to further characterization with applied voltages.

Table 7.3: The table provides an overview of the maximum deviation in capacitance, C_{p}, for all 16-element arrays measured on the maskless LOCOS wafer and is based on Zf measurements. The voltage offset, V_{offset}, is also included and is based on the CV measurements described in the following section. The prefix S refers to the *Single* design with a designed capacitance of 6.27 pF, while F refers to the *Filled* design having an approximate capacitance of 43.87 pF

Array no.	C **dev.** [pF]	V **offset** [V]	**Array no.**	C **dev.** [pF]	V **offset** [V]
S1	0.04	6.64	F3	0.12	13.56
S3	0.02	6.64	F4	0.12	12.86
S4	0.02	3.91	F5	0.11	4.75
S5	0.03	-7.31	F7	0.13	-34.03
S6	0.03	-11.40	F8	0.12	-36.18
S7	0.02	0.93	F9	0.09	-26.90
S8	0.03	-15.55	F10	0.11	4.54
S9	0.03	-8.26	F11	157.4	14.19
S10	0.02	-1.93			
S11	0.03	5.86			
S12	0.03	7.91			
S13	0.07	7.66			

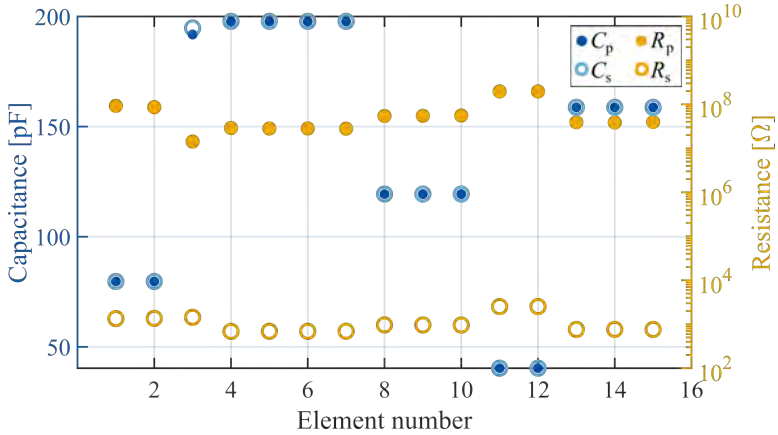


Figure 7.6: Shows data from the 16 element array F11 on the maskless LOCOS wafer. The plot reveals distinct levels in the capacitance corresponding to a specific number of connected top electrodes.

7.1.3 Voltage Measurements

In accordance with the details presented in Section 6.4, the voltage measurements comprise a sequential procedure of IV and CV measurements. The IV measurement is utilized to obtain the maximum current, $I_{\max}$, while the CV data was fitted using Eq. (6.13) to determine the minimum capacitance, C_0, and the bias offset, V_{offset}, which shifts the vertex position.

Fig. 7.7 illustrates a plot of the maximum current and the minimum capacitance as a function of element number for array 4.3. Additionally, Fig. 7.8 displays the voltage offset found for each individual element. In general, the majority of the elements exhibit a consistent current level of approximately 0.5 pA. However, nine elements deviate from this pattern, displaying higher values exceeding 10 pA. Despite these aberrant values, these elements remain functional within the acceptable range of current levels. A more detailed investigation of these elements is carried out in the subsequent subsection.

Comparing the C_0 values with the capacitance data depicted in Fig. 7.2, it is observed that five elements exhibit a distinct behavior, displaying a capacitance level of approximately 9.2 pF, which corresponds to two interconnected top electrodes. Treating these elements as outliers, the average capacitance for C_0 is determined to be 4.64 pF with a standard deviation of 0.01 pF. Moreover, the initial data obtained through a Zf sweep yields an average value of 4.63 pF with a standard deviation of 0.01 pF. Consequently, it can be concluded that there exists a correlation between the impedance and voltage data, which aligns with the expected behavior. The five elements displaying an altered capacitance level were further examined and will be elaborated upon in the subsequent subsection.

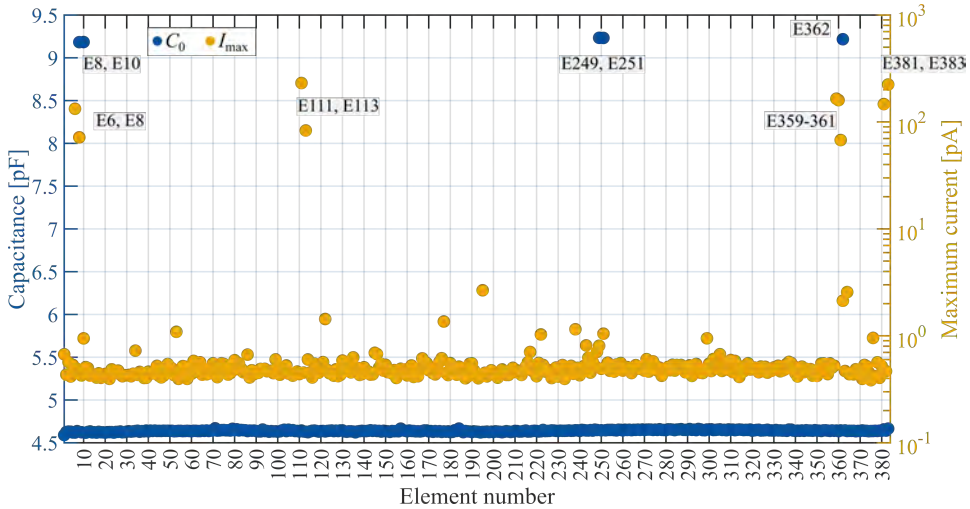


Figure 7.7: Summary of the initial CV and IV data obtained for array 4.3 from the maskless LOCOS wafer. The left y-axis represents C_0, which is determined by fitting Eq. (6.13) to the data. On the right y-axis, $I_{\max}$ for each element are displayed. Elements exhibiting aberrant behavior are highlighted, indicating their respective element numbers.

The voltage offset, V_{offset}, displayed in Fig. 7.8, indicates a built-in potential of approximately 2 V for the majority of the elements. This behavior is observed in all four characterized arrays, with an average value of V_{offset} ranging between 1.3 V and 2.2 V. This built-in potential aligns with the expected behavior considering the composition of the CMUT stack, which comprises a highly doped n-type substrate and a highly doped p-type top plate. The built-in potential is anticipated to correspond to the bandgap energy, with an additional contribution from the metal's work function.

A histogram of the maximum current values is presented in Fig. 7.9. To visualize the few exceptions, the data is plotted on a logarithmic scale. The insert provides a closer view of the majority of the data depicted on a linear scale. The data exhibit a normal distribution with a tail extending towards higher currents. Excluding the outliers, the mean value of the data is 0.52 pA with a standard deviation of 0.21 pA.

Now turning to the charging behavior across the five measured 384-element arrays, it is observed that the four best performing arrays, based on the Zf measurements, exhibited no hysteresis effects, resulting in a charging yield of 100 %. However, the array with the poorest performance (array 10.3) displayed mobile charging effects exclusively on the odd elements, while no charging was observed on the even elements. This distinction is illustrated

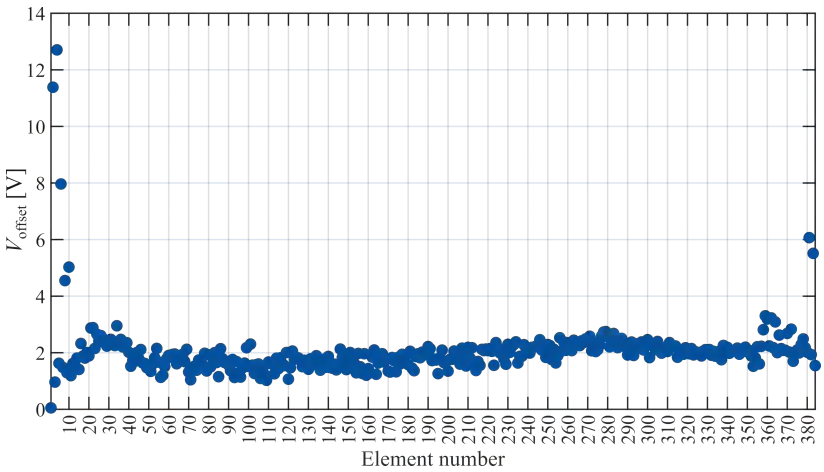


Figure 7.8: The offset potential of the CV data calculated by applying Eq. (6.13) to the data of each element. The data are obtained from array 4.3 on the maskless LOCOS wafer.

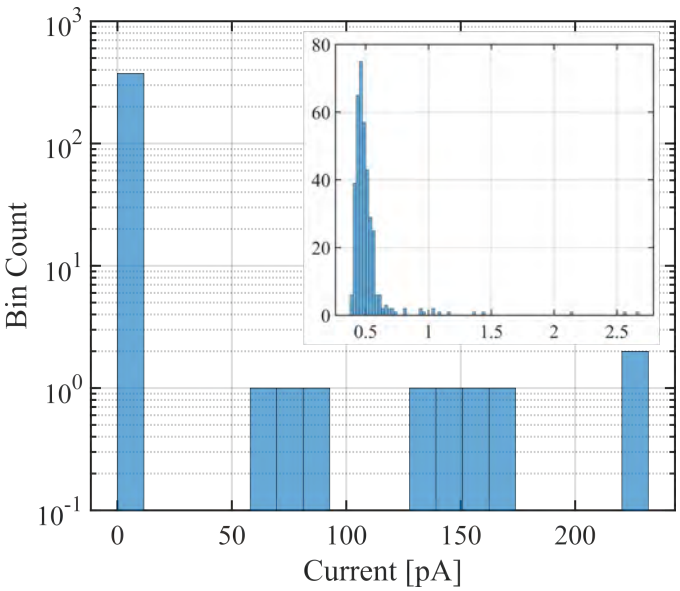


Figure 7.9: Histogram depicting the maximum current, with the bin count presented on a logarithmic scale. The insert provides a closer view of the majority of the data on a linear scale, revealing a normal distribution with a tail towards higher currents. The data are acquired from array 4.3 on the maskless LOCOS wafer.

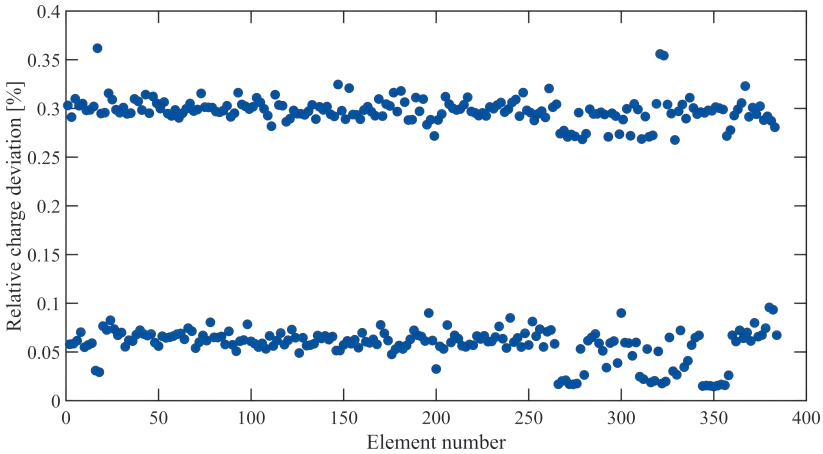


Figure 7.10: The relative charge deviation, expressed in percentage, for array 10.3 from the maskless LOCOS wafer.

in Fig. 7.10, revealing two separate levels of charge deviation. Although the exact mechanisms behind charging effects in CMUTs are not fully understood, is it attributed to undesired charges accumulated on the surface of the insulating dielectric oxide or nitride [105]. This phenomenon, as a material artifact, contradicts the observed alternating behavior of charging on odd elements only. Therefore, subsequent measurements using an impedance analyzer were conducted. A more detailed analysis of these findings is presented in the following subsection.

For the 16 element arrays, all arrays except one (array F11), exhibit capacitance levels corresponding to the expected value based on the design. Array F11 reveals connected top electrodes, which becomes evident from the observed capacitance levels in Fig. 7.6. A similar pattern is observed when examining the fitted capacitance, C_0, derived from the CV measurements. Furthermore, all measured arrays demonstrates consistent current levels across all elements, having an average value of 0.9 pA and a standard deviation of 0.8 pA. However, it should be mentioned that the offset potential caused by built-in charges in the dielectric layer is generally much larger for the 16 element array compared to the 384-element arrays. The values are presented in Table 7.3. Calculating the charge density per square centimeter based on the performed measurements results in a range of $3.8 \times 10^{10}\,\mathrm{cm}^{-}2$ to $6.8 \times 10^{12}\,\mathrm{cm}^{-}2$, which is consistent with the reported amount of fixed surface charges on the silicon/silicon oxide interface as documented in [106].

Among the arrays examined, only one array (array S7) displays hysteresis in the CV curve. Remarkably, this hysteresis effect is observed consistently across all elements of the array.

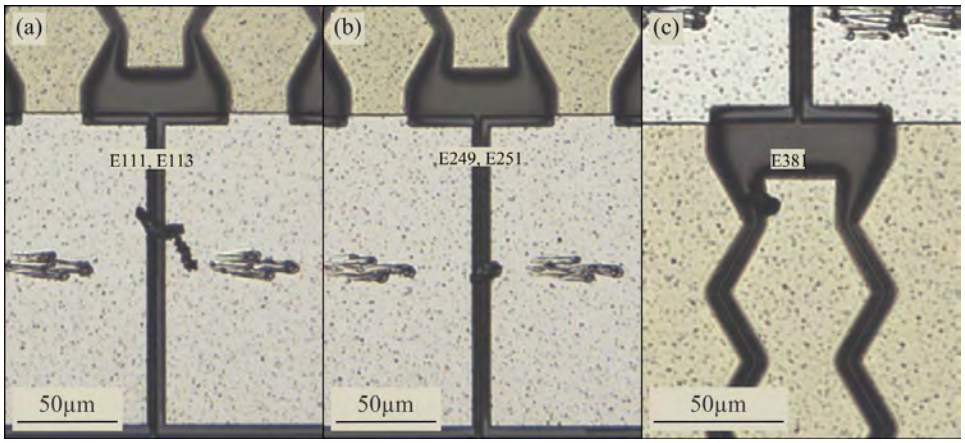


Figure 7.11: Visually found errors related to aberrant behavior in the C_0 and $I_{\max}$ values. The images are obtained from array 4.3 on the maskless LOCOS wafer.

Measurement aberrations

In the voltage-based measurements, a few elements exhibited deviating behavior in terms of either capacitance level or maximum current compared to the majority of elements. These deviating elements will be investigated in the this subsection. The analysis presented here is based on data obtained from array 4.3.

Initially, all elements were visually re-inspected using the optical microscope integrated into the probe station. During this inspection, particles connecting the top electrode wirebond pads were discovered. Examples of these particles are shown in Fig. 7.11. Figures (a) and (b) illustrate particles that visually appear similar, connecting element 111 with 113 and 249 with 251, respectively. However, based on the initial IV and CV characterization, these connected elements exhibit different behaviors. Element 111 and 113 have a normal capacitance level (approximately 4.6 pF), but they exhibit a relatively high current of approximately 80 pA. On the other hand, element 249 and 251 exhibit a capacitance of 9.2 pF, indicating two connected top electrodes, while $I_{\max}$ is low at around 1.67 pA. The correlation between these visual inspections and the results of electrical measurements is not yet fully understood.

Figure 7.11 (c) demonstrates a particle located at the end of element 381. For this particular element, the initial IV and CV measurements demonstrated a normal capacitance level but an increased $I_{\max}$ value of 147 pA. Similarly, all errors marked in Fig. 7.7 were visually detected, with the exception of element 6, where no visual errors were found.

Secondly, all of the highlighted elements were re-measured to validate

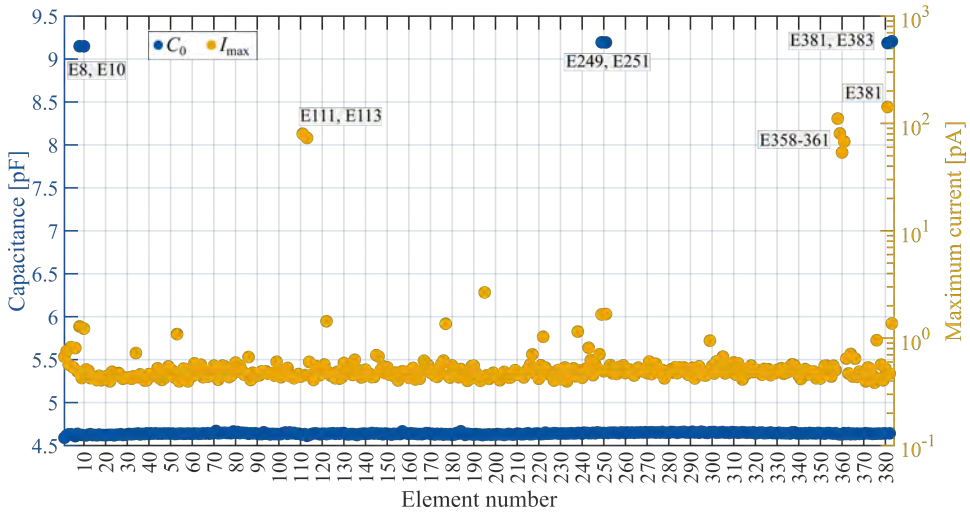


Figure 7.12: Summary of the CV and IV data for array 4.3 from the maskless LOCOS wafer, including the results from the re-measurements. The left y-axis represents C_0, obtained by fitting Eq. (6.13) to the data, while $I_{\max}$ for each element is displayed on the right y-axis.

their aberrant behavior. The results are presented in Fig. 7.12, were the elements of interest are marked by their element number. While some changes in the results were observed, the majority of the initial findings were confirmed. Notably, the increased $I_{\max}$ values for element 6 and 8 where not replicated, and $I_{\max}$ for element 111 decreased from 231 pA to 80 pA. Conversely, the current for element 358 increased from 0.5 pA to 111 pA. Based on visual inspection a particle was discovered between element 358 and 360, which may have contributed to the increased current. Another discrepancy in the measurements was observed for element 362, where the initial rise in C_0 was not validated by the re-measurement, which showed a capacitance of 4.6 pF.

Finally, element 381 and 383 initially exhibited a normal capacitance level and an increased current. The visual examination revealed a particle connecting the bond pads, and the re-measurement resulted in a C_0 value corresponding to double capacitance of 9.2 pF. However, only element 381 showed an increased current. An overview of the element behavior during the initial and subsequent measurements, along with the findings of a visual inspection, is provided in Table H.4.

In summary, all the deviations identified through the electrical voltage characterization were visually detected. While a few elements displayed an altered voltage characteristic, the underlying causes for these changes is not fully understood and requires further comprehensive investigation. Furthermore, the relationship between interconnecting particles and the resulting rise in current versus an increase in capacitance has yet to be understood,

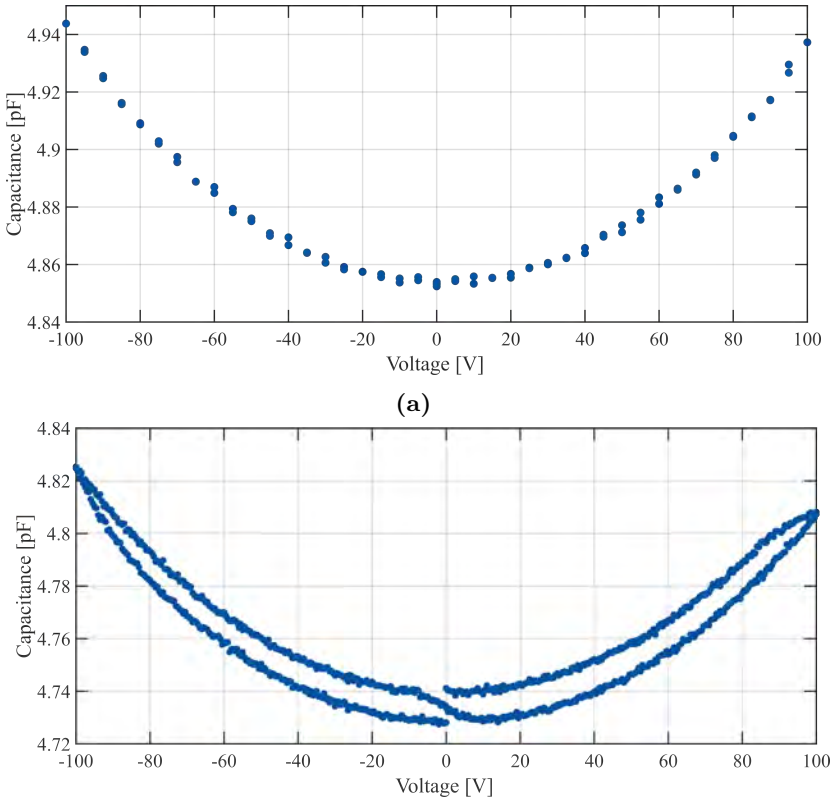
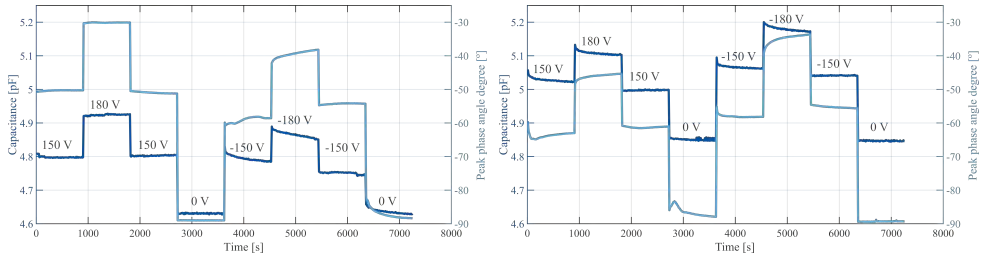


Figure 7.13: CV curves obtained from (a) the impedance analyzer, and (b) the parameter analyser. The data sets are acquired from array 10.3, element 191 on the maskless LOCOS wafer. The upper plot exhibit no hysteresis effects, while the lower plot shows hysteresis. Notice the vertical displacement.

too. However, it should be noted that the observed increase in current still falls within the acceptable range for functional elements. Attempts to remove the particles were performed with great success. Remeasurements of the affected elements showed a normal capacitance level around 4.6 pF. However, the increased current levels remained unresolved.

To investigate the observed charging effects in the odd elements of array 10.3 (shown in Fig. 7.10), further measurements were conducted using both the parameter analyzer and the impedance analyzer. The results obtained from these two measurement setups are compared in Fig. 7.13. Notice the vertical displacement.

Fig. 7.13a displays the data acquired from the impedance analyzer. A frequency range of $f = 100\,\text{kHz} - 150\,\text{kHz}$ was chosen to minimize noise from external sources. Additionally, an oscillation bias of 200 mV was applied. The bias voltage was swept from 0 V to 100 V in steps of 5 V, and the



(a) **(b)**

Figure 7.14: Stability measurements performed on (a) element 191 and (b) element 192 on array 10.3 from the maskless LOCOS wafer. Similar behavior is observed for both elements, however with a vertical displacement in capacitance. Furthermore, is the applied potential included. Please note that data from the parameter analyzer revealed charging effects for the measured element in (a).

same procedure was repeated for negative biases. Notably, no hysteresis is observed in the data obtained by impedance analyzer. For reference, the remeasurement performed on the parameter analyzer is shown in Fig. 7.13b. In this case, the frequency was set to $f = 50\,\mathrm{kHz}$ with an alternating bias of $50\,\mathrm{mV}$, and the bias step size was $0.5\,\mathrm{V}$. The graph clearly indicates the presence of mobile charges. Since these results are contradicting, further investigation was initiated performing a long-term stability measurement on one charging and one non-charging element.

The stability measurements were performed on two adjacent center elements of array 10.3 (element 191 and 192). The details in the measurement setup are provided in-depth in Section 6.7. The results are shown in Fig. 7.14. In both measurements, the positive bias was initially applied. Notably, no significant charging effects were observed in either case, and the graphs obtained from the measurements exhibit similar behavior, despite a slight vertical displacement in capacitance level. Based on this comprehensive study of element charging using the impedance analyzer, it is concluded that the hysteresis effects observed in the data obtained using the parameter analyzer are likely associated with measurement technicalities, when observed for alternating element number. The underlying cause of this behavior remains unknown and has not been further investigated due to time constraints.

7.1.4 Yield

As described in Section 6.5, the yield is divided into different categories. In the following there will be differentiated between the 384-element arrays and the 16-element arrays.

The fabrication yield is determined based on the information provided

in Table 7.1, H.1 and H.2. For the 384-element arrays, the yield is 65.5 %, whereas for the *Single* and *Filled* designs the yields are 92.3 % and 61.5 %, respectively.

The capacitor yield is defined by the criteria elaborated in Section 6.3, Table 6.4. Recall, a capacitive behavior is indicated by a phase angle smaller than $-80°$, a parallel resistance larger than mega-Ω, and a serial resistance smaller than 200 kΩ. For the maskless LOCOS wafer it was observed that all measured arrays exhibited capacitive behavior and met the specified criteria. As a result, both the 384-element arrays and the 16 element arrays achieved a capacitor yield of 100 %.

The capacitance-level yield represents the percentage of elements that exhibit a capacitance within the expected range defined by the design specifications. This yield is based on the initial Zf measurements, since aberrations occurring during the CV measurements are considered induced errors rather than inherent chip characteristic. Additionally, the majority of these errors can be resolved by manually removing the particles.

In the case of the 384-element arrays, the accepted capacitance range was set as $4\,\mathrm{pF} < C < 5\,\mathrm{pF}$. This criteria resulted in a yield of 98.8 %, indicating that the majority of measured elements fell within the acceptable capacitance range. Appendix H, Table H.3 provides an overview of the number of elements that deviated from the accepted capacitance range for each of the 384-element arrays.

For the *Single* design, the accepted capacitance level falls within the range of $6\,\mathrm{pF} < C < 7\,\mathrm{pF}$, resulting in a yield of 100 %. However, for the *Filled* design the capacitance range is $39.5\,\mathrm{pF} < C < 40.5\,\mathrm{pF}$, which leads to a yield of 89.1 %. The 14 elements outside the defined interval are found in 16-element array F11, as shown in Fig. 7.6. The observed levels refer to the product of the capacitance of a single element and the number of top electrodes that are interconnected.

Regarding the yield related to charging, the maximum accepted relative difference in charges is set to 0.1 %. By applying this criterion to the data obtained from the five measured 384-element arrays, the yield is determined to be 100 %, since the long term stability test did not show any charging effects. Additionally, one of the 12 measured 16 element arrays with the *Single* design shows hysteresis on all elements, while none of the eight measured 16-element arrays with a *Filled* design exhibit hysteresis effects, resulting in a yield of 91.7 % and 100 %, respectively.

A summary of the yields for both the 384-element arrays and the 16-element arrays are given in Table 7.4.

Table 7.4: Overview of the yield for the maskless LOCOS wafer including both the 384-element arrays and the 16-element arrays.

Yield type	384-element array	Single design	Filled design
Fabrication	65.5 %	92.3 %	61.5 %
Capacitor	100 %	100 %	100 %
C-level	98.8 %	100 %	89.1 %
Charging	100 %	91.7 %	100 %

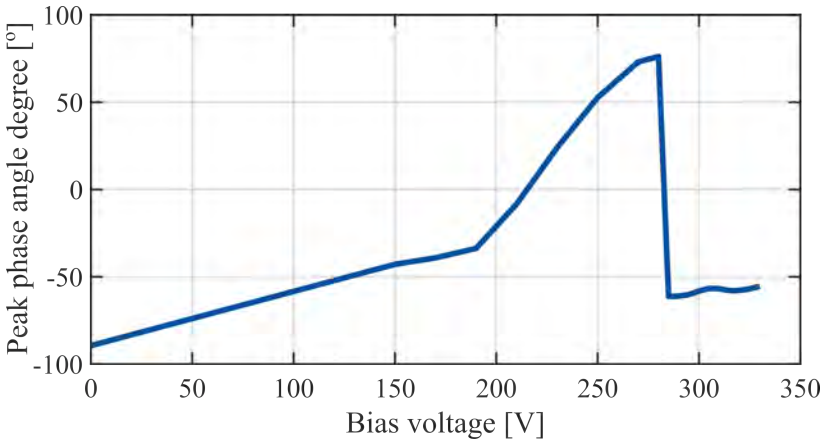


Figure 7.15: The peak phase angle degree plotted relative to the applied bias voltage to determine the pull-in voltage of element 29 on array 5.3 from the maskless LOCOS wafer.

7.1.5 Pull-in and Frequency Analysis

The best performing array, based on the measurements conducted on the parameter analyzer, was identified as array 4.3. To determine the pull-in voltage, the neighboring array, array 5.3, was utilized to prevent any potential breakdown or damage to the array intended for probe mounting. The measurement were performed following the principles outlined in Section 6.6. Element 29 of array 5.3 was chosen for the measurements, and a two-sweep frequency range was employed to ensure high data resolution across the entire range. The first range spanned from 40 kHz to 15 MHz, and the second range, around the frequency peak, ranged from 15 MHz to 40 MHz. The DC bias was systematically adjusted from $V_{\mathrm{DC}} = 0\,\mathrm{V}$ up to 330 V. Analysis of the peak phase angle degree for each applied bias voltage revealed a noticeable drop at 285 V. The corresponding results are depicted in Fig. 7.15. This exceeds the designed value of 220 V and the discrepancy is attributed to variations in the gap height.

The amplitude and phase curves for the applied bias voltages varying from 250 V to 285 V are depicted in Fig. 7.16. The curves clearly show a

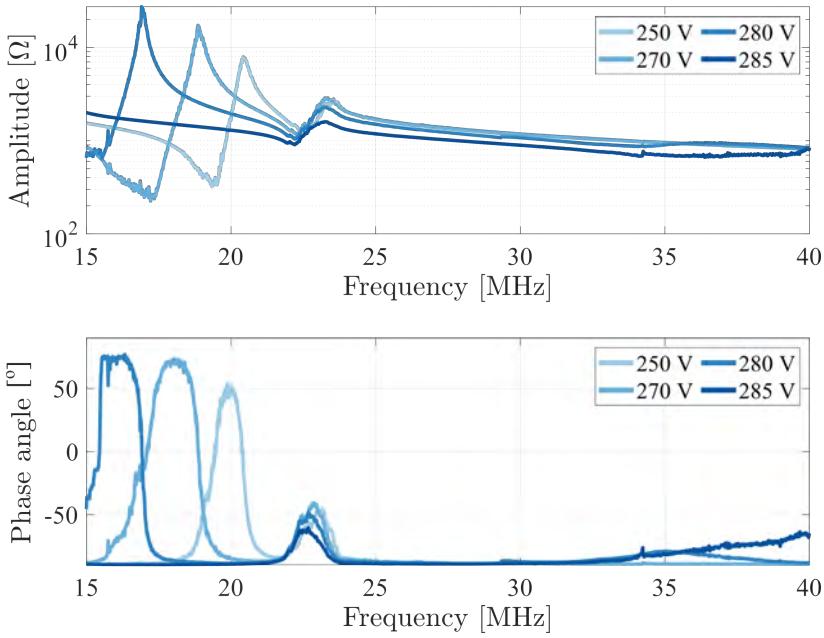


Figure 7.16: Impedance amplitude and phase spectra measured relative to the frequency at different biases. A drop in both the frequency and phase peak is seen for an applied bias of 285 V.

prominent peak in both the amplitude and phase plots at a bias of 280 V, corresponding to a frequency of 16.2 MHz. Furthermore, it is observed that when the bias is increased to 285 V, these peaks disappear, indicating that the element has reached the pull-in voltage. However, it should be noted that an unchanged peak is still observed at a frequency around 23 MHz. Since this peak remains constant for different applied biases, it is attributed to a measurement technicality rather than a characteristic of the element behavior. As described in Section 6.6, the CMUT plate undergoes a voltage-dependent spring softening effect, which would result in a change in frequency as function of applied bias. Although the exact cause of this peak is yet to be determined, it is evident that it is unrelated to the behavior of the element.

After determining the pull-in voltage, frequency measurements were conducted on array 4.3 using the same two frequency ranges. However, the applied bias range was adjusted to (0–240) V. The frequency measurements were performed on the first six, middle six, and last six elements of the array, both in increasing and decreasing order. The frequency was obtained by identifying the maximum phase angle degree. Furthermore, was the fitted capacitance derived from the impedance data measured at frequencies below 1.3 MHz. The results for an applied bias voltage of 240 V are presented in Fig. 7.17. Regardless of the measurement order, the array consistently ex-

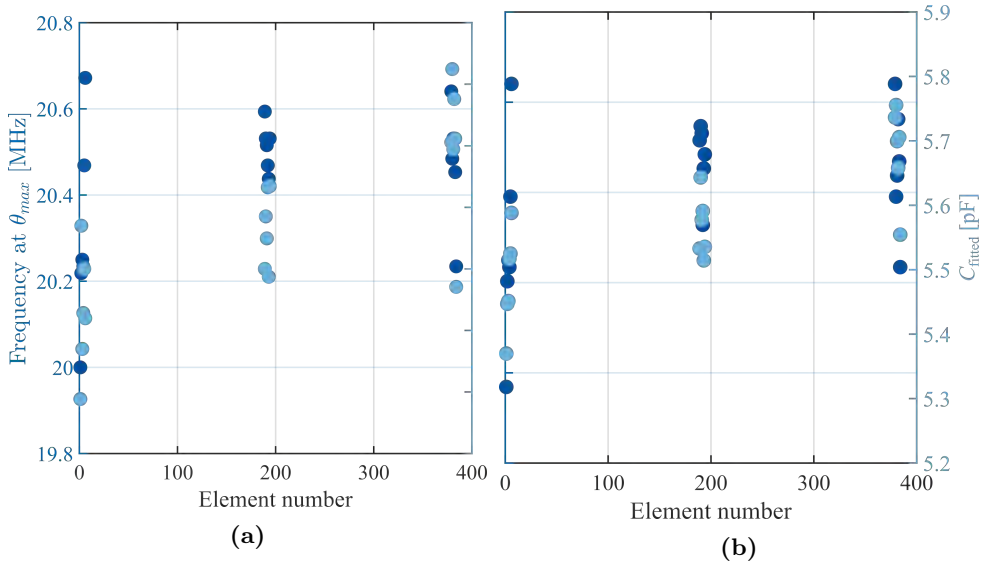


Figure 7.17: Data obtained from the frequency measurements of array 4.3 on the maskless LOCOS wafer with a bias of 240 V. The left axis shows the frequency determined at the maximum phase angle, while the right axis represents the capacitance found from the impedance amplitude data. **(a)** Present the data measured for increasing element number, while **(b)** displays the data measured for decreasing element numbers.

hibited an increasing trend in both frequency and capacitance with respect to the element number. However, the variation in frequency was found to be less than 1 MHz, and the variation in capacitance was less than 1 pF. The average resonance frequency for the array was determined to be 20.4 MHz in air.

Fig. 7.18 shows the biased impedance data obtained from array 4.3 for the center element (element 192). The plots illustrate the presence of a voltage-based spring softening effect in both the amplitude and phase measurements. Additionally, it can be observed that the magnitude of the amplitude and the phase angle degree both increase as the bias voltage is raised, which is consistent with the expected behavior of a CMUT. However, signal distortion is observed for frequencies around (23–25) MHz, similar to the observation made during the pull-in measurements of array 5.3. This distortion peak remains unaffected by the magnitude of the applied bias, suggesting it stems from a measurement or equipment-related factor.

The coupling coefficient was determined using Eq. (6.14), which involves extracting the resonance and antiresonance values from the amplitude plot as a function of the applied bias voltage. The calculated coupling coefficient is presented in Fig. 7.19. It is observed that the squared coupling coefficient increases with increasing bias voltage until reaching the pull-in voltage. At approximately 80 % of the pull-in voltage (230 V), the squared coupling

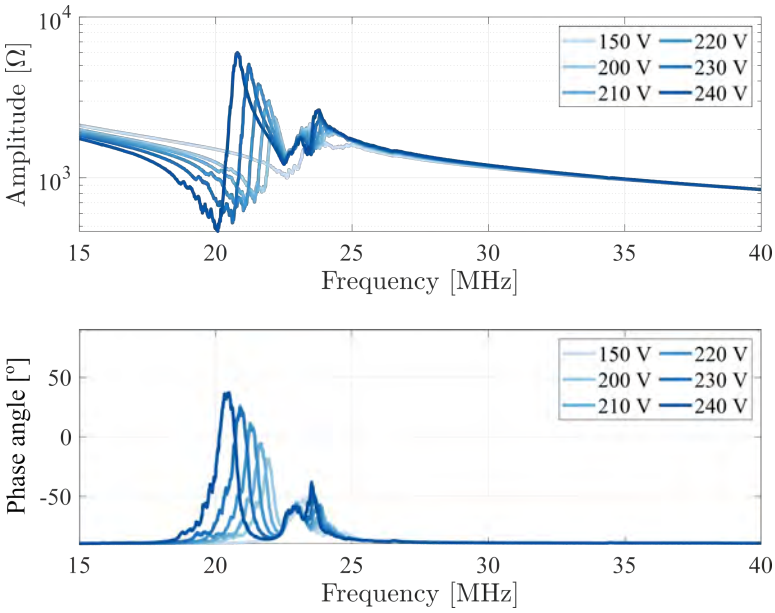


Figure 7.18: Biased impedance data was measured on array 4.3 from the maskless LOCOS wafer, specifically on the center element (element 192). Both the amplitude and phase plots clearly exhibit a spring softening effect, which is caused by the increasing bias voltage.

coefficient reaches 7.06 %. However, due to limitations of the scanner, the maximum applied voltage was restricted to 180 V, resulting in $k^2_{\text{em}} = 5.3\,\%$. In comparison, a previously fabricated linear transducer called Tabla IV, created in this research group, demonstrated a squared coupling coefficient of around 6 % at 80 % of the pull-in voltage [16]. This finding aligns with the results obtained in the current study, demonstrating similar performance in terms of the squared coupling coefficient.

Proceeding to the pull-in tests on the 16-element arrays, the results for the F4 array are presented in Fig. 7.20. The phase angle degree is plotted against the applied bias voltage. A noticeable decrease in the phase angle degree is observed at approximately 290 V, which correlates well with the findings from the 384-element array.

Frequency measurements and analysis were conducted on the four best performing arrays, consisting of two arrays with the *Single* design (S4 and S10) and two arrays with the *Filled* design (F5 and F10). The measurement setup employed was identical to that used for the 384-element array, including the same two frequency ranges and voltage range of (0–240) V. Given the limited number of elements, frequency measurements were carried out on all 16 elements of the four arrays. All elements exhibited the expected behavior of a CMUT, showing an increase in the magnitude of both phase angle degree and amplitude with increasing bias, as well as a

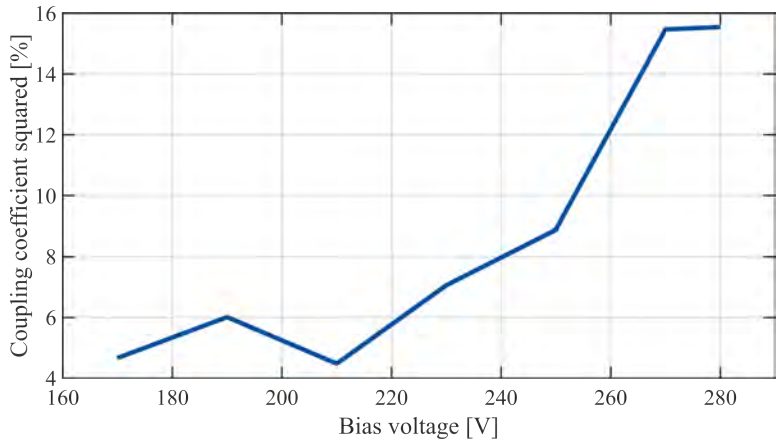


Figure 7.19: The coupling coefficient squared relative to the applied bias voltage. The data were obtain on array 5.3, element 29 from the maskless LOCOS wafer.

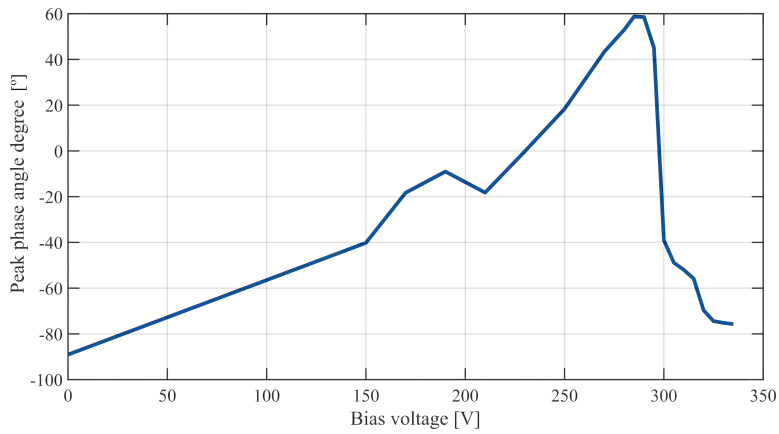


Figure 7.20: The peak phase angle degree plotted relative to the applied bias voltage to determine the pull-in voltage of the 16-element array F4 from the maskless LOCOS wafer.

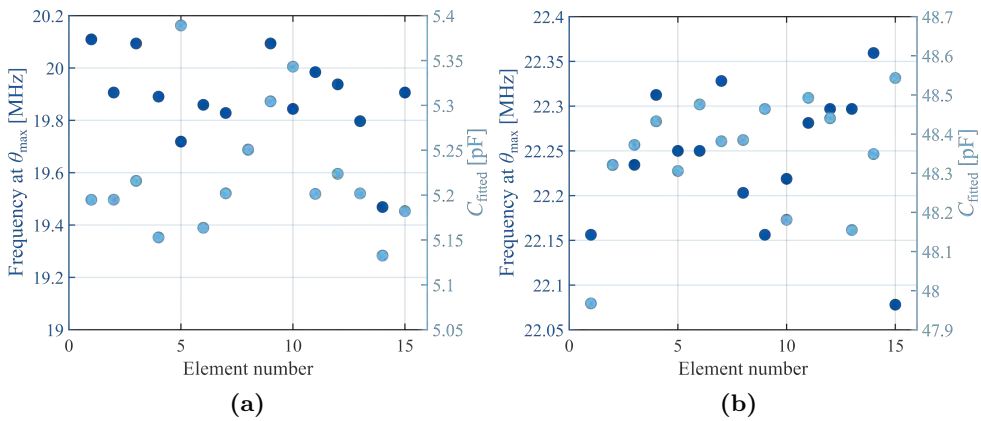


Figure 7.21: Summarizing the frequency and capacitance data obtained from biased impedance measurements performed on the 16-element arrays on the maskless LOCOS wafer. The data were extracted at a bias of 240 V. **(a)** Shows the data for array S10, while **(b)** presents the data from array F10.

frequency decrease due to spring softening effects. Similar to the observations made for the 384-element array, the 16-element arrays also exhibited a signal attributed to the measurement setup at around 23 MHz. Furthermore, all arrays demonstrated consistent levels of frequency and capacitance across all elements. The frequency data obtained at 240 V bias for array S10 is presented in Fig. 7.21a, while the results from array F10 are shown in Fig. 7.21b.

7.1.6 Stability Measurements

The long-term performance of the array was evaluated through stability measurements, as described in Section 6.7. Fig. 7.22 presents the results obtained from array 4.3, element 85. The peak phase angle degree and the capacitance fitted at low frequencies were monitored over time. The figure illustrates a highly stable element, with minimal variations of less than 10° in phase angle and less than 0.1 pF in fitted capacitance. Similar results were obtained when the stability test was conducted by applying a negative bias first followed by a positive bias, as shown in Appendix H, Fig. H.1. Due to the long-term nature of the stability measurements these were exclusively performed on one element per array.

The stability of the 16-element arrays was assessed on the center element (element 8). Similar to the measurements conducted on the 384-element array, stability tests were performed by applying a positive bias first, followed by a negative bias, and vice versa.

The results obtained from all four arrays demonstrated highly stable elements for both positive and negative bias. Figures illustrating the stability

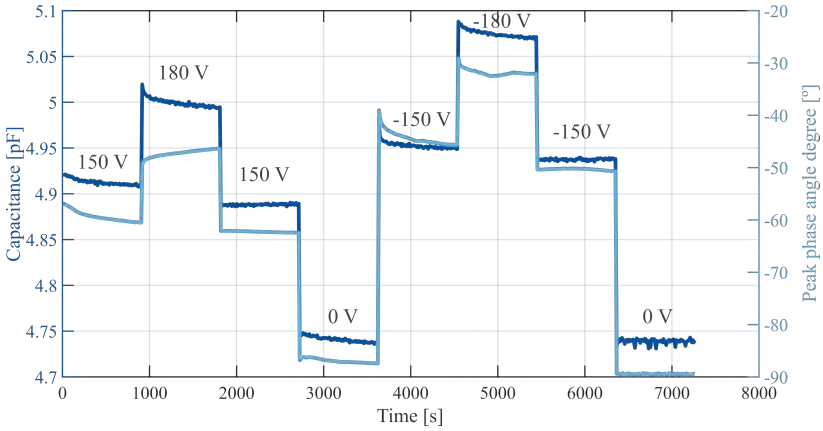


Figure 7.22: Stability plot obtained from array 4.3 on the maskless LOCOS wafer, element number 85. Initially a positive bias was applied, followed by a negative bias. The peak phase angle and the slope capacitance are derived over time.

for array S10 and F10 can be found in Appendix H, specifically Fig. H.2 and Fig. H.3, respectively.

7.2 Double LOCOS Wafer

This section presents the results obtained from the double LOCOS wafer. However, due to time constraints, the wafer was not characterized using the setup involving the impedance analyzer. Additionally, only the 384-element arrays were characterized.

While a comprehensive analysis of a well-performing array has already been conducted for the maskless LOCOS wafer, it is important, for the sake of completeness and future reference, to also investigate an array showing non-trivial performance. This analysis is performed in this section. This illustrates that electrical characterization of CMUT devices is not always a straightforward task.

7.2.1 Visual Inspection

Similarly to the maskless LOCOS wafer, the initial characterization of the double LOCOS wafer involved visual inspection using the optical microscope from the probe station. The findings are summarized in Table 7.5. The inspection revealed a majority of errors related to connected top electrodes and miscellaneous errors. This observation aligns with the tendency observed for the maskless LOCOS wafer. As earlier mentioned, the errors associated with connected top electrodes can potentially be reduced or eliminated through process optimization of the etching step. Out of the 29 arrays examined, a total of 19 arrays were considered suitable for further characterization, while

Table 7.5: This overview presents the errors detected through visual inspection on the 384-element arrays on the double LOCOS wafer. The error numbers correspond to those listed in Table 6.3. The arrays highlighted in gray were not subjected to further characterization.

Array no.	Error	Array no.	Error	Array no.	Error
1.2	-	5.3	-	9.3	-
2.2	-	6.1	E2, E5	10.1	E1, E2, E4, E5
3.1	-	6.2	-	10.2	-
3.2	-	6.3	-	10.3	-
3.3	-	7.2	-	11.1	E1, E2
4.1	E1	8.1	E2	11.2	-
4.2	-	8.2	-	11.3	-
4.3	E3	8.3	-	12.2	E2, E5
5.1	E2, E5	9.1	E2 - E5	13.2	E1, E4, E5
5.2	-	9.2	E4, E5		

the arrays marked with gray in the table were discarded.

7.2.2 Impedance Measurements

Automatic Zf measurements were performed on 19 arrays, using the parameters specified in the first row of Table 6.1. The majority of the elements exhibited the expected capacitive behavior, however, array 1.2 displayed strange behavior. Fig. 7.23 provides an overview of all elements of the array, showing C_s and C_p on the left y-axis, and R_s and R_p on the right y-axis. The plot shows that element 56 and 57 have the double capacitance, indicating connected top electrodes. Furthermore, the resistances, particularly the serial resistance, exhibit two distinct levels. The upper level corresponds to all the odd elements, while the lower level corresponds to the even elements. The reverse behavior is seen for the parallel resistance were the lower level is data from the odd elements, and the upper level is from the even elements. By calculating the average values for the serial and parallel resistances and capacitance separately for the odd and even elements, distinct levels for both resistances were observed, while no clear tendency emerged for the capacitances. These average values are shown in Table 7.6 along with the average phase angle. Despite the small change in phase angle degree, a histogram reveals two normal distributions centered around these average values. This is illustrated in Fig. 7.24. It is important to note that among the 19 characterized arrays, this behavior was only observed in array 1.2. The underlying reason for this behavior is currently unknown.

All arrays were subjected to analysis and performance verification based on the criteria specified in Table 6.4. The analysis showed that all mea-

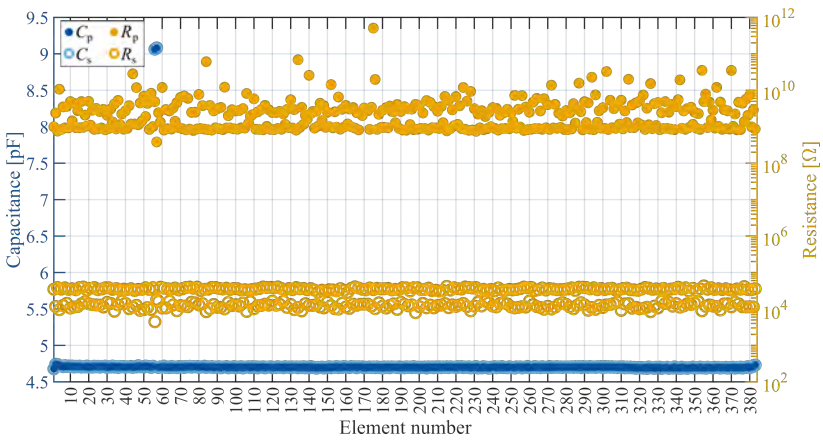


Figure 7.23: Providing a summary of the C_s, C_p, R_s, and R_p data for all elements on array 1.2 from the double LOCOS wafer. The data reveals to levels in R_s and one set of a connected top electrodes pair.

Table 7.6: Mean values found for different parameters calculated separately for the odd and even elements. Distinct levels are found for the resistances and the phase angle, while the capacitances are indistinguishable.

	R_s [kΩ]	R_p [GΩ]	C_s [pF]	C_p [pF]	θ [°]
Even elements	12.3	5.89	4.72	4.72	-89.84
Odd elements	35.4	3.77	4.73	4.73	-89.44

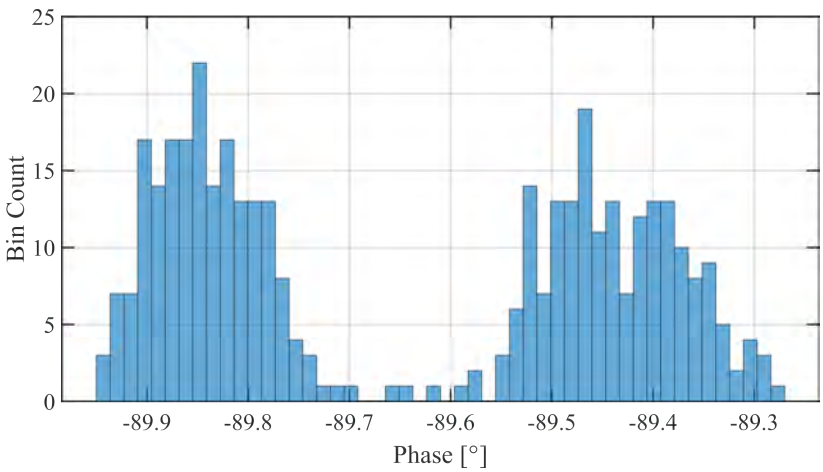


Figure 7.24: A histogram of the phase angle for all elements of array 1.2 from the double LOCOS wafer. Two normal distributions are revealed, where the left corresponds to the even elements and the right to the odd elements.

Table 7.7: The table provides an overview of the maximum deviation in C_p of the 19 arrays measured on the double LOCOS wafer. The four arrays highlighted in blue were selected for further characterization together with array 1.2 due to its aberrant behavior.

Array no.	C **dev.** [pF]	**Array no.**	C **dev.** [pF]	**Array no.**	C **dev.** [pF]
1.2	4.41	5.3	0.12	9.3	4.37
2.2	0.07	6.1	26.86	10.2	4.40
3.1	74.78	6.2	0.09	10.3	4.43
3.2	0.07	6.3	4.38	11.2	13.25
3.3	0.40	7.2	0.08	11.3	4.39
4.2	0.07	8.2	0.07		
5.2	0.07	8.3	1.14		

sured elements exhibited capacitive behavior with a phase angle below $-80°$, $R_p > \mathrm{M}\Omega$ and $R_s < 200\,\mathrm{k}\Omega$. The consistency of the capacitance levels was determined by evaluating the maximum deviation in capacitance within each array, which can identify potential instances of connected top electrodes. The results are summarized in Table 7.7. Visual inspection of the summary plots for arrays without top electrode connections was performed to identify the four arrays showing the most consistent levels in both capacitance and resistance. Based on this analysis, further characterization was conducted on array 2.2, 3.2, 4.2, and 7.2. Due to its deviating behavior array 1.2 was also subject to subsequent characterization.

7.2.3 Voltage Measurements

The results of the voltage measurements for array 1.2 are summarized in Fig. 7.25, providing an overview of the fitted capacitance (C_0) and maximum current (I_{max}). Similar to the induced particle errors observed on the maskless LOCOS wafer, a few errors are also observed for array 1.2 on the double LOCOS wafer. These bond pads connections are identified between element 2 and 4, 20 and 22, 65 and 67, and 84 and 86. Additionally, the connected top electrodes between elements 56 and 57 are also revealed from the CV data. In total six elements shows an increased I_{max}, however, these values are still within the acceptable range for well-functioning elements and based on the previous examination of these errors, they are not considered outliers.

Considering the offset potential, V_{offset}, which is obtained from the parabolic fit using Eq. (6.13), Fig. 7.26 depicts the results for all elements of array 1.2. Two distinct levels are observed in the data: one around 2.5 V corresponding to the odd elements and an elevated level at 11 V for all even elements. Relating this to the relative charge deviation depicted in Fig. 7.27, it is

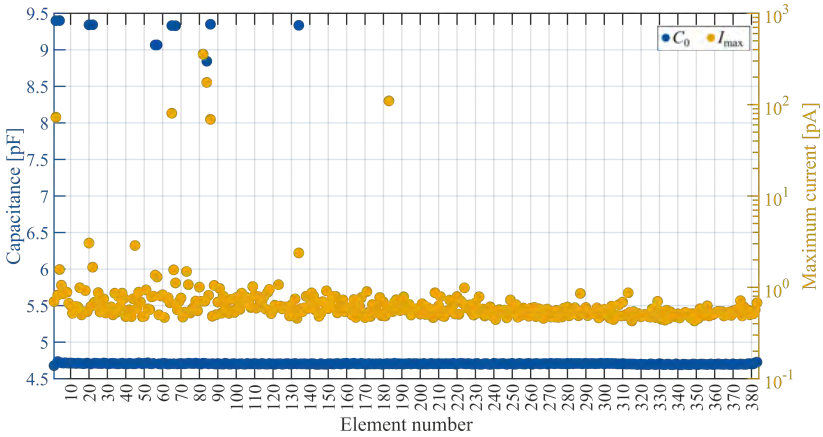


Figure 7.25: Summary plot showing the fitted capacitance, C_0, and the maximum current, $I_{\max}$, relative to the element number. The data are obtained from array 1.2 on the double LOCOS wafer.

observed that hysteresis is present in every second element (corresponding to the even elements), while none of the odd elements exhibit hysteresis. This indicates that an elevated level in V_{offset} reveals charging effects in an element.

However, it is important to note that the offset obtained from the fit using Eq. (6.13) is only valid when the data demonstrates a good parabolic behavior. As an example, Fig. 7.28, which presents data from element 2 on array 1.2, clearly shows hysteresis effects. The performed fit is included in the figure by a dashed line. Ideally, four separate fits should be performed, resulting in four different values for C_0 and V_{offset}. Fitting a single curve to all the data leads to a curve shifted to the right, resulting in an artificially large value for V_{offset}. The relatively low value of $R^2 = 0.70$ indicates a poor fit. Therefore, the exact bias offset for elements exhibiting hysteresis is not a physical parameter but can be used as a benchmark to identify charging effects. As previously mentioned, a small built-in charge can be attributed to the bandgap between the p- and n-doped materials. Additionally, the work function of the metals may contribute with an increased offset, although not to such a significant extent as observed for the even elements.

Besides an alternating hysteresis behavior of array 1.2, the four other arrays, characterized by voltage measurements showed hysteresis on all elements. To verify this, the first 10 elements of array 1.2, 2.2 and 3.2 were re-measured using the parameter analyzer, employing the same parameters again. The results confirmed element charging on all elements for array 2.2 and 3.2, while none of the elements on array 1.2 exhibited hysteresis. This contradicts the expectations based on the Zf measurements, where array 2.2, 3.2, 4.2, and 7.2 showed promising results. Once again, this emphasizes that charging phenomena cannot be detected through unbiased Zf measurement,

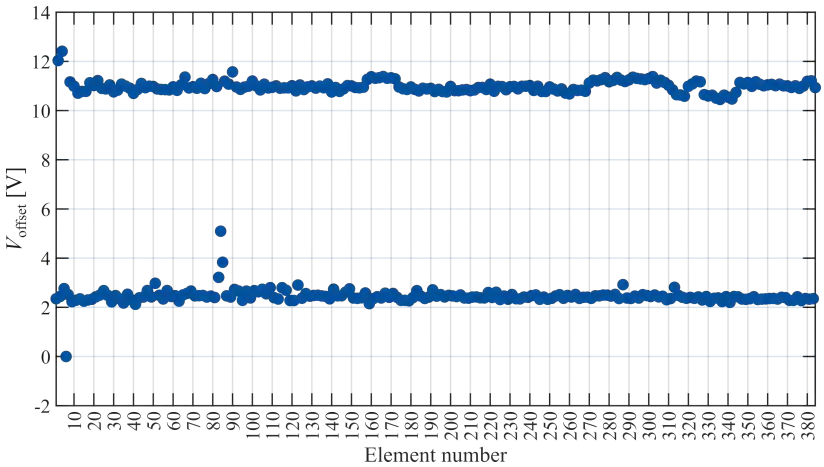


Figure 7.26: The offset bias, V_{offset}, found from fitting Eq. (6.13) to the element data from array 1.2 on the double LOCOS wafer. Two distinct levels are observed. For all odd elements, the offset bias is 2.5 V, while for the even elements it is 11 V.

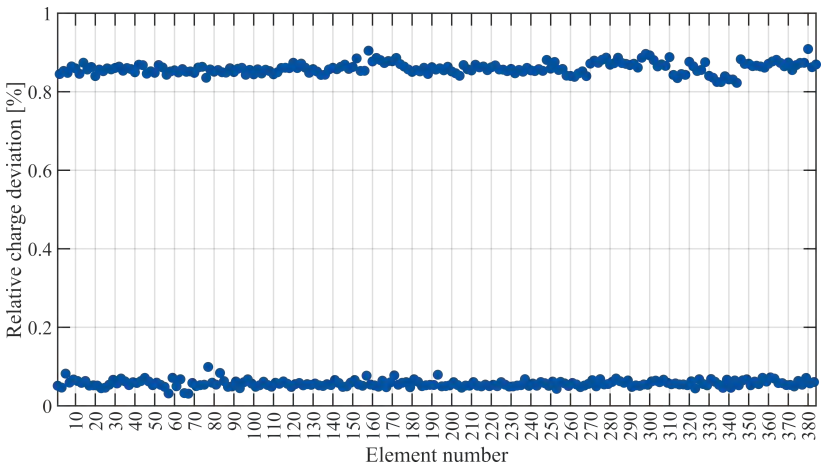


Figure 7.27: The relative charge deviation in percent found for each of the elements on array 1.2 from the double LOCOS wafer. Two levels are revealed, showing hysteresis on all even elements, while none of the odd elements shows hysteresis.

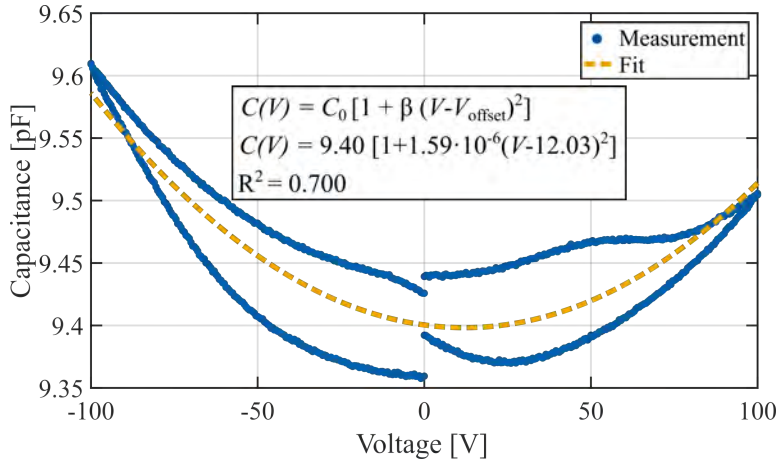


Figure 7.28: A CV curve from the charging element 2 on array 1.2 from the double LOCOS wafer. Eq. (6.13) is used to derive C_0 and V_{offset} and is shown in a dashed line.

but requires a CV sweep.

Considering the recent findings on the maskless LOCOS wafer, where the hysteresis measured using the parameter analyzer was not confirmed by the long-time stability measurements on the impedance analyzer, it becomes challenging to draw conclusions regarding whether the observed hysteresis is an actual charging effect or a measurement-related technicality. This demonstrates the non-trivial nature of performing this type of electrical measurements.

Furthermore, extensive discussion regarding dielectric charging effects in CMUTs are found in literature. A review paper on charging of CMUTs [105] provides insights into possible modifications to the basic structure of CMUTs to mitigate these effects. The paper also highlights that charging effects can often be attributed to multiple mechanisms, and emphasizes the significance of the dielectric layers, such as oxide and nitride, in the charging phenomenon. Factors such as deposition temperature, humidity, and layer thickness have been identified as influential for the dielectric charging effects. Despite considerable research efforts, the reliability issues associated with dielectric charging effects in CMUTs have not yet been completely resolved.

Due to time limitations and the aberrant behavior of the double LOCOS wafer, further characterization of was not pursued. Instead, the focus was on the best-performing arrays from the maskless LOCOS wafer that showed potential for integration into a probe handle.

7.2.4 Yield

As described in Section 6.5, the yield is divided into four categorize. First, the fabrication yield was determined through visual inspection and summa-

Table 7.8: Overview of the yield for the double LOCOS wafer.

Yield type	**384-element array**
Fabrication	65.5 %
Capacitor	100 %
C-level	98.6 %
Charging	10 %

rized in Table 7.5. This resulted in 65.5 % successfully fabricated arrays, which were all subsequently characterized using a Zf measurement.

The Zf measurement revealed that all measured elements exhibited capacitive behavior meeting the defined requirements of having a phase angle below $-80°$, $R_\mathrm{p} > \mathrm{M}\Omega$ and $R_\mathrm{s} < 200\,\mathrm{k}\Omega$. This translates to a capacitor yield of 100 %.

From the Zf measurement, a small number of elements exhibited a capacitance level that deviated from the theoretical value of 4.53 pF based on the design specifications. By applying a lower acceptance limit of 4 pF and an upper acceptance limit of 5 pF, the yield was determined to be 98.6 %. The number of deviating elements for each specific array can be found in Appendix H, Table H.5.

Considering the relative charge deviation for the five measured arrays revealed charging on all elements of four arrays. Additionally, the initial characterization revealed hysteresis on every second element of array 1.2, while the re-measurements did not find any mobile charging effects. Since a second full characteristic of the array was not performed only half the elements are considered to be performing well when calculating the charging yield. Therefore, the yield is only 10 %. However, given the discrepancy between the parameter and impedance analyzers, it is advisable to re-measure this finding using the impedance analyzer for clarification and better understanding of the performance.

In summary, both the initial visual inspection and the Zf measurement showed overall good results, similar to what was observed for the maskless LOCOS wafer. The occurrence of connected top electrodes was also comparable between the two wafers. However, further investigation of the worst-performing array (array 1.2) revealed distinct levels in R_s, R_p, and the phase angle. IV and CV measurements were conducted on four good arrays, along with array 1.2, which exposed induced interconnections between neighboring bond pads, similarly to the ones found for the maskless LOCOS wafer. Additionally, mobile charging effects were revealed in all

elements of the four well-performing arrays, and in every second element of array 1.2. Re-measurements confirmed this behavior for array 2.2 and 3.2, while array 1.2 did not exhibit any hysteresis. Consequently, it was decided not to proceed with further measurements on the double LOCOS wafer, as the focus was on identifying the best-performing array to be integrated in a probe handle.

7.3 Chapter Summary

This chapter presented the results of the electrical characterization conducted on two fabricated wafers. The first wafer was fabricated using the maskless LOCOS process, while the second wafer employed a double LOCOS fabrication method. The characterization procedure followed the methodology outlined in Chapter 6, starting with a visual inspection to select the arrays for subsequent characterization. Subsequently, the wafers underwent an initial impedance-based automatic screening, and the most promising arrays from both wafers were further analyzed using voltage-based measurements.

This newly introduced Zf based full wafer-level characterization method demonstrated promising results, successfully identifying various errors that were not initially detected during the visual inspection. These errors included connected top electrodes and small holes in the top plate. As a result, certain arrays were discarded, focusing the full voltage-based characterization only on the promising arrays, thereby minimizing the measurement time.

For the maskless LOCOS wafer, the four most promising arrays were subjected to a voltage-based characterization. Additionally, the worst performing array (array 10.3) based on the Zf data was further investigated as a proof of concept. The results revealed that none of the four best arrays exhibited any mobile charging behavior, while array 10.3 showed charging effects on all odd elements. However, these charging effects were not reproducible during CV measurements performed on the impedance analyzer. Consequently, stability measurements were conducted on both a charging element and a non-charging element, but no definitive conclusion could be reached based on these measurements.

Furthermore, all the discrepancies observed on array 4.3 between the Zf measurement and the CV/IV sweep were visually identified upon thorough inspection of the wafer. It was observed that particles were introduced on the neighboring bonding pads of the top electrodes for elements showing a significant change in capacitance. However, the relationship between the presence of interconnecting particles and an increase in capacitance, contrary to a rise in current, is not yet understood. It was demonstrated that manually removing these particles resulted in the element's performance

aligning with the expected values for the capacitance.

Regarding the double LOCOS wafer, the characterization process was discontinued after characterizing the array using the parameter analyzer due to abnormal behavior detected during voltage-based measurements. However, biased impedance measurements were performed on one 384-element array and four 16-element arrays from the maskless LOCOS wafer. These measurements involved determining the resonance frequency and conducting long-term stability tests. To prevent short circuiting the arrays of interest, pull-in measurements were conducted on neighboring arrays instead.

The pull-in voltage was measured on array 5.3 on the maskless LOCOS wafer and was found to be 285 V for the 384-element array, which exceeded the designed value of 220 V. The discrepancy is attributed to variations in the gap height. For array 4.3 on the same wafer, the biased impedance measurements revealed an average resonance frequency of 20.4 MHz across 18 elements, when measured in air at 240 V. Furthermore, the measurements confirmed the expected voltage-based spring softening effect. However, an additional peak at around 23 MHz was observed, which did not exhibit spring softening. Therefore, this peak was attributed to the measurement setup rather than the device itself.

For the long-term stability tests, positive and negative bias sequences were applied, and both measurements showed a stable element with a maximum phase angle variation of 7° for a single bias step. Similar behavior was observed for the four characterized 16-element arrays.

Based on the obtained results from the maskless LOCOS wafer, one 384 element array (array 4.3), along with four test arrays exhibiting potential for probe mounting, were selected for further use.

CHAPTER 8

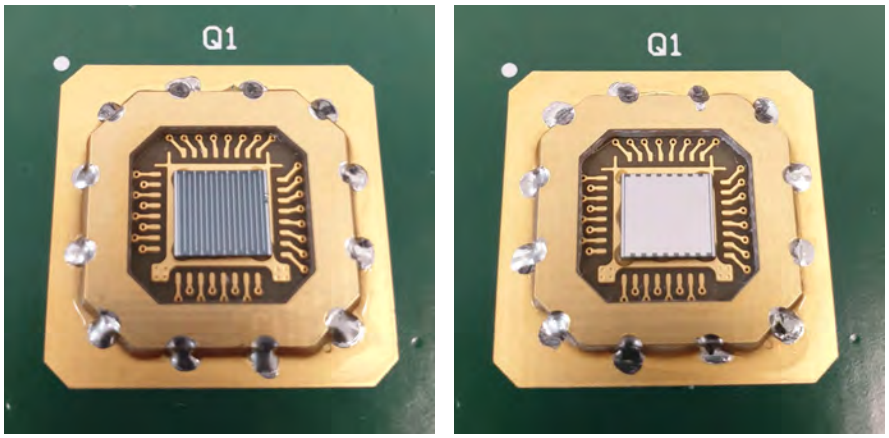
Assembly and Acoustic Characterization

This chapter presents the array assembly process, encompassing mounting, wire bonding, and casting procedures. Furthermore, details of the impedance measurements conducted after wafer mounting, are provided. Finally, the acoustical test setup and the obtained measurement results are described.

The assembly process was performed on four of the 16-element arrays, all from the wafer fabricated using the maskless LOCOS process. The packaged arrays were: two of the *Single* design (S4 and S10) and two of the *Filled* design (F5 and F10). The 16-element arrays were originally designed to fit a CCB test board already available. All processes were carried out in-house.

Currently, a CCB for the large 384-element arrays is being developed. It is anticipated to be completed within a few months from the time of writing, at which point the assembly process will be conducted similarly to the process described in this chapter. However, the CCB is being designed to fit into the prototype probe developed by Ph.D. student Kasper Fløng Pedersen [107]. For application purpose an electromagnetic shield will be mounted on top of the first layer of PDMS. It will subsequently be mounted in the custom made nose piece for the prototype probe, before the final PDMS layer will be casted on top. These steps are not described in the following, since the 16-element arrays exclusively serve the purpose of simple acoustical testing.

The second part of the chapter describes electrical impedance measurements. Initially, the employed measurement setup is described, followed by a presentation of the obtained results. Impedance measurements were performed after mounting and wire bonding (prior to PDMS casting), as well as after the casting process. These results were compared to the ones obtained



(a) **(b)**

Figure 8.1: Images showing successful mounting of two 16-element arrays from the maskless LOCOS wafer. **(a)** Depicts the *Single* design, array S10, while **(b)** shows the *Filled* design, array F5.

from the simulations presented in Chapter 3.

Finally, the acoustical measurement setup is described followed by an evaluation of the obtained results encompassing both transmit and receive measurements. The transducer performance is evaluated upon the frequencies and relative fractional bandwidths.

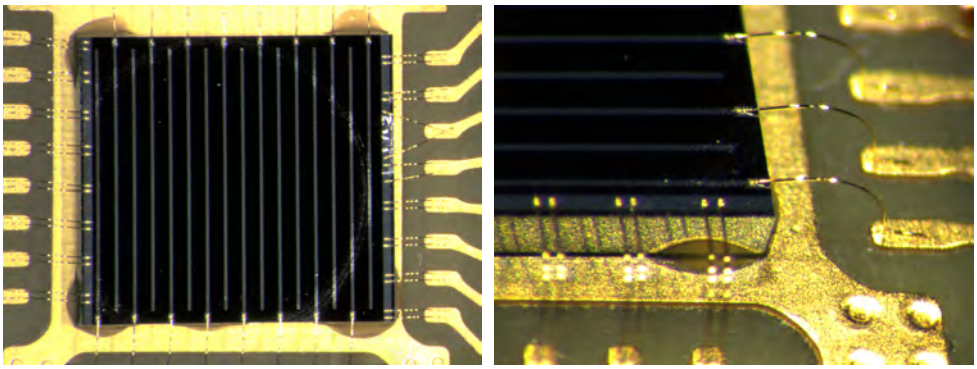
The work described in this chapter was conducted in collaboration with Postdoc Rune Sixten Grass and Ph.D. student Kasper Fløng Pedersen.

8.1 Assembly

The transducer assembly process involved three steps and had a total processing time of approximately four days. Prior to the assembly process, the arrays on the maskless LOCOS wafer were diced out and the protective layer of resist was removed by flushing them with acetone followed by isopropanol. The arrays were subsequently dried using an air gun.

8.1.1 Mounting and Wire Bonding

The first step was to mount the CMUT array onto the CCB. This step was performed using a Scorpion ARP-1200S rework station. Initially, the CCB was mounted on the Scorpion X-Y stage, while the array was placed in the Scorpion chip holder and rotated to align the array to the CCB. A UV-sensitive adhesive (Dymax 9801) was applied, and subsequently cured using a UV light for 15 s. A heating program was conducted applying a temperature of 85 °C for 30 min to finalize the mounting process. Fig. 8.1



(a) (b)

Figure 8.2: Showing successfully wire bonding of array S10 to the CCB. **(a)** Illustrates the entire array, while **(b)** provides an angled close up image of few of the wire bonds. A single wire bond is provide per element, while multiple wire bonds are applied to the bottom electrode for optimal grounding.

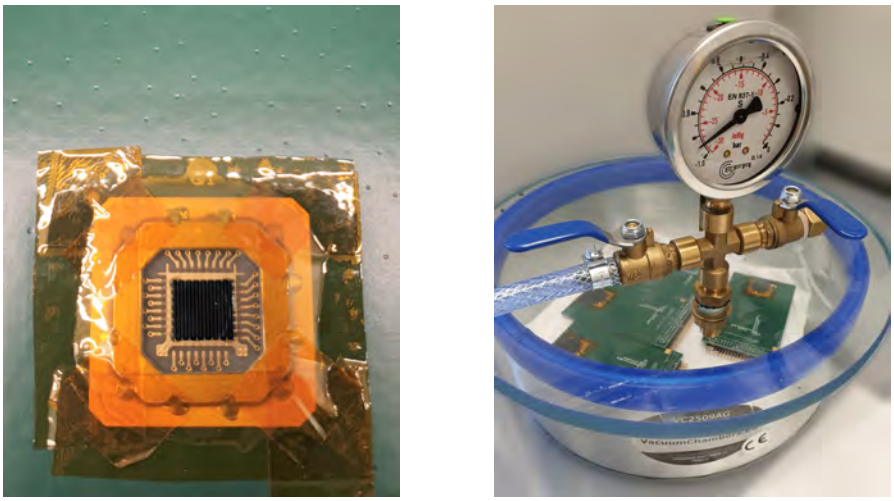
depicts two successfully mounted arrays, where Fig. 8.1a shows the S10 array and Fig. 8.1b depicts the F5 array.

After the adhesive was cured, the arrays were electrically connected to the CCBs. Various bonding methods are available for establishing electrically contact between the CMUT array and the CCB. In this case, the wire bonding method was chosen due to the design and fabrication approach employed, which involved separate top electrodes and a pre-designed CCB. Wire bonding is a well-established, commercially available technique that offers advantages such as flexibility, cost-effectiveness compared to flip chip bonding, and high reliability [108].

An automatic wire bonder (TPT HB100) was employed to facilitate the wire bonding process. More specifically, a wedge bonding method was performed. The applied bonding parameters involved an ultrasonic power of 90 and a force of 200. The process was carried out with a stage temperature of 110 °C. A 25 µm thick gold tread was utilized. The bond strength was tested on two test bonds positioned from the ground pad to the CCB, to avoid damaging the element bonding pads. The resulting pull bond strength was measured to 13.5 g, which is high compared to the standard of 3 g for a similar wire [109]. Fig. 8.2 displays two images of array S10 after a successfully bonding process. A single wire bond is provide per element, while multiple wire bonds are applied to the bottom electrode for optimal grounding.

8.1.2 PDMS Casting

The final step in the assembly process involved encapsulating the array using a PDMS layer. Initially, a layer of Kapton tape was applied to ensure

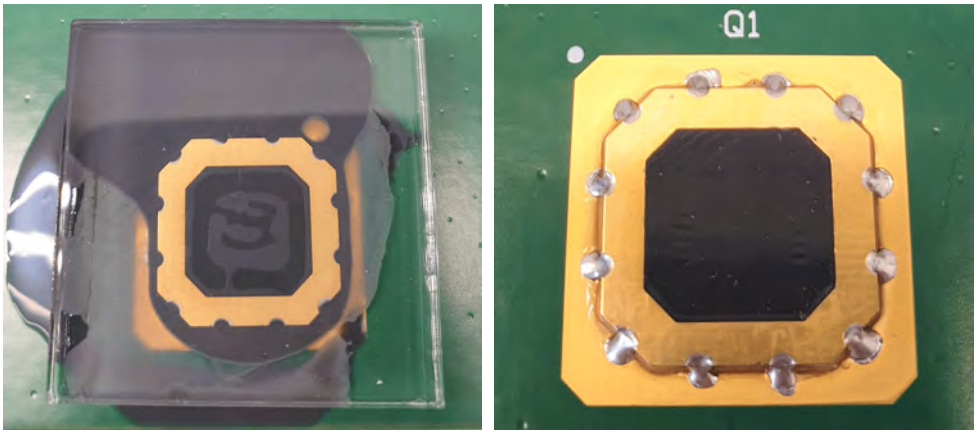


(a) **(b)**

Figure 8.3: **(a)** Image of the CCB with a mounted and wire bonded array (S10) on top. Kapton tape was applied prior to dispersing the primer. **(b)** Showing the degassing chamber containing the mounted arrays. The purpose of the degassing process was to eliminate any bubbles trapped inside the PDMS layer.

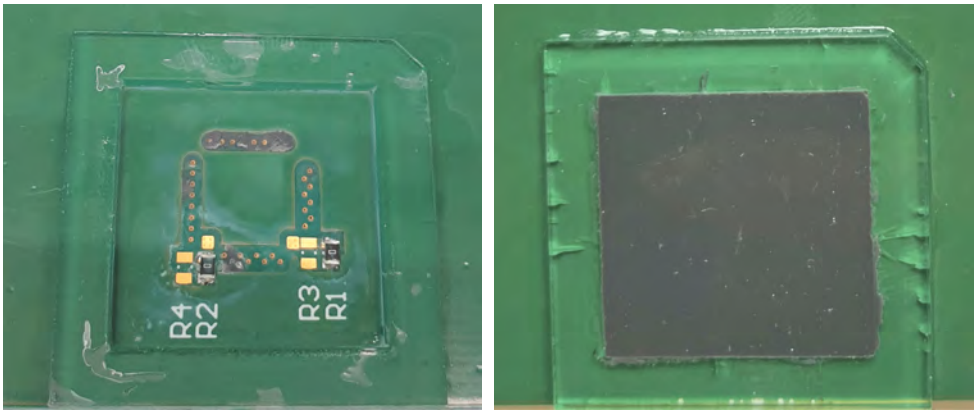
that primer was exclusively applied to the array and wire bonding area, as visualized in Fig. 8.3a. The primer was cured under raised humidity conditions at 45 °C for one hour. The subsequent layer consisted of a two-component PDMS (Sylgard 170) which was applied on top of the primer. It was then degassed in a vacuum chamber for approximately 10 min, as shown in Fig. 8.3b. The purpose of the degassing process was to eliminate any bubbles trapped inside the PDMS layer, which could potentially disrupt the signal during operation. After degassing, the PDMS was planarized to the frame level using a flat PMMA plate secured by a clamp, which also served as a pressure divider. This process (without the clamp) is illustrated in Fig. 8.4a. The pressure was maintained for approximately 20 h at a temperature of 45 °C. An image of array S10 after finalizing the casting process is provided in Fig. 8.4b.

Following PDMS casting on the front side of the CCB, a similar sealing process was performed on the backside. This was conducted in order to protect the electronics when immersing the chip into the water tank. Initially, a custom made PMMA frame was glued to the backside of the CCB using a cyanoacrylate. Subsequently, primer and PDMS were applied and cured applying the same parameters as for the front side. Images of the backside before and after applying the PDMS are provided in Fig. 8.5a and Fig. 8.5b, respectively.



(a) **(b)**

Figure 8.4: **(a)** Depicting the levelling of the PDMS layer using a planar PMMA plate. **(b)** Image of a finalized encapsulated array. Both images shows the casting process for array S10.



(a) **(b)**

Figure 8.5: Images illustrating the sealing process of the backside of the CCB. **(a)** Shows a PMMA frame mounted on the board, while **(b)** shows the backside after a successful PDMS casting process.

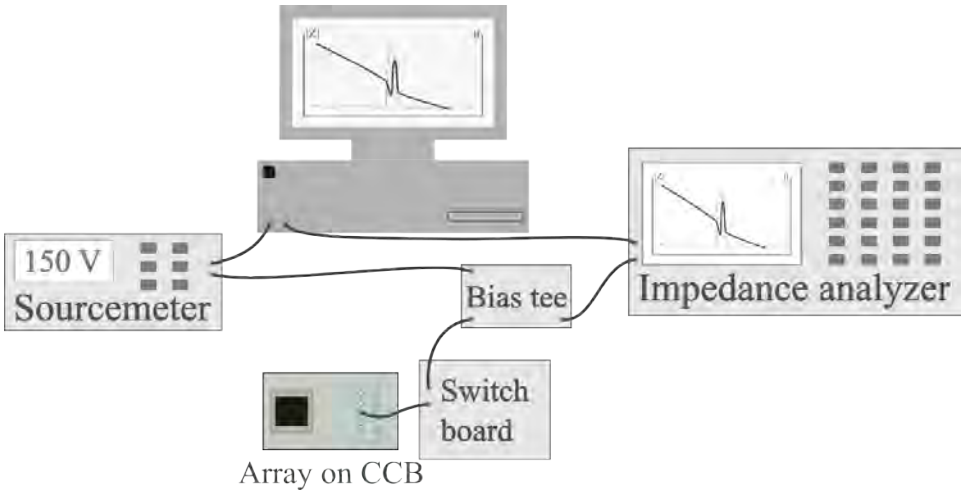


Figure 8.6: Illustration of the impedance measurement setup used after array assembly. A sourcemeter provides the DC potential to a bias tee, which is connected to a switch board. The switch board is directly connected to a channel on the CCB corresponding to a single element on the array. Furthermore, the bias tee is connected to the impedance analyzer, which performs the measurement and sends the data back to the control computer.

8.2 Impedance Measurements

After mounting and wire bonding of the four arrays, new impedance measurements were performed using the Agilent E4990A Precision Impedance Analyzer. The measurement setup had similarities with the one describe in Section 6.1.2, however, the probe station was not utilized during these measurements. An illustration of the setup is provided in Fig. 8.6. In this setup, a Keithley 2410 sourcemeter, providing the DC potential is connected to the bias tee. The bias tee is further connected to a switch board, which is directly connected to a channel on the CCB corresponding to an element. Each element is individually connected to a channel on the CCB, which enables characterization and operation of a single element. Calibration was performed on the entire system including the CCB prior to measurements to exclusively measure a signal from the element.

The impedance measurements were conducted applying similar parameters as those employed before the arrays were mounted and packaged. To enhance the SNR, an AC voltage of 200 mV was applied. Two frequency ranges were utilized: the first range spanned from 40 kHz to 15 MHz, while the second range covered frequencies from 15 MHz to 40 MHz. The DC potential was varied up to 240 V. The measurement results for the center element (element 8) on array S10 are shown in Fig. 8.7. This clearly illustrates the spring softening effect when increased bias. However, the peak of the phase angle is wider compared to the measurement results before mount-

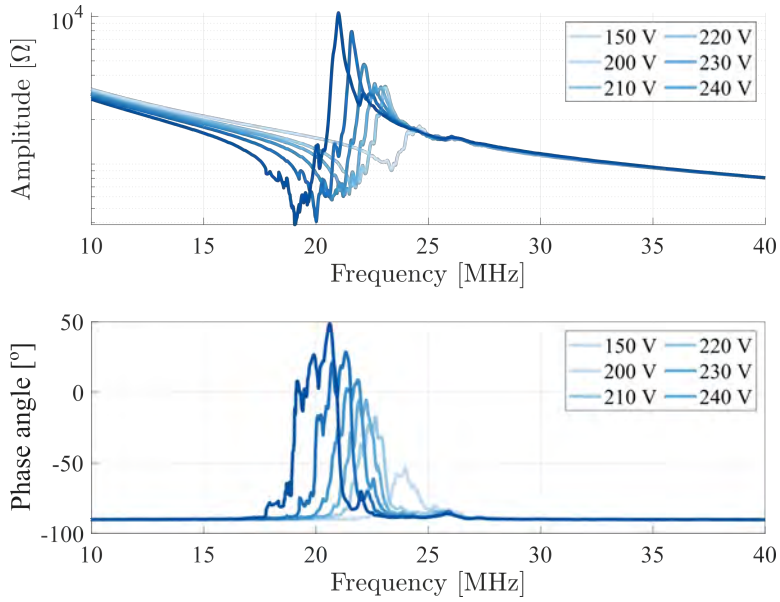


Figure 8.7: Biased impedance measurement on array S10, element 8 after mounting and wire bonding to a CCB. The spring softening effect is observed from both the impedance amplitude and the phase angle, as expected.

ing. The element frequency is unchanged, which is in accordance with the expected behavior.

The impedance measurements were performed on four elements on each array: element 1, 8, 9, and 16. Summary plots for array S10 and F10, similar to the ones obtained before mounting (Fig. 7.21a and 7.21b), are provided in Fig. 8.8. For both arrays it is observed that the frequency remained unchanged by the mounting process with an approximate value of 20 MHz for array S10, while an increase of approximately 1 MHz is observed for array F10. A slight increase in capacitance corresponding to approximately 2 pF is observed for both arrays. This is ascribed to the capacitance of the wire bonds.

The measurements were repeated after encapsulation of the arrays. The result for array S10, element 8 is shown in Fig. 8.9, for a measurement performed in air. From the amplitude spectrum it is observed that the resonance and anti-resonance peaks are very suppressed. Furthermore, a shift in frequency is observed. For an applied DC potential of 240 V the center frequency yields approximately 14 MHz, while before the PDMS casting the center frequency was around 20.6 MHz at the same bias voltage. This verifies the behavior predicted by the OnScale simulations performed during the design phase. For reference see Section 3.1.2. The wavy appearance in the phase plot is expected to originate from poor coupling between the PDMS layer and the ambient air. Similar appearance were observed in the pressure

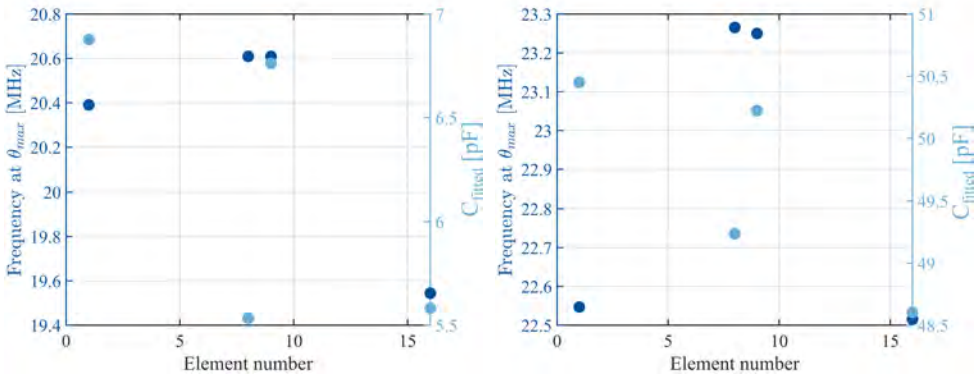


Figure 8.8: Data summary for the impedance measurements after mounting and wire bonding to the CCBs. The results are obtained for measurements with an applied DC potential of 240 V. **(a)** Shows the results for array S10, while **(b)** are the results for array F10.

output simulated in OnScale (see Appendix D, Fig. D.2).

Finally, the board was submerged into a small water tank and the measurement was repeated. The result is shown in Fig. 8.10. This output is very similar to the measurement in air, showing a center frequency of 14 MHz. However, it is worth noting that the wavy outline of the phase angle has vanished. This demonstrates that the acoustic coupling from the PDMS to the water eliminate the interface ringing due to good acoustical coupling from the PDMS to the water. This behavior has also been observed in the output pressure maps from the OnScale simulations provided in Appendix D, Fig. 3.5b. By comparing the three impedance measurements it is observed that the main frequency shift appears when casting the PDMS on top of the array. The frequency is unchanged when submerged in water, thereby validating the expectations from Section 3.1.2.

8.3 Acoustic Characterization

Following the electrical impedance measurements, the acoustical array performance was investigated. Fig. 8.11 presents an illustration of the acoustical measurement setup used during transmission measurements. At the top center of the image, a control computer can be seen. The AC signal is created by a Tektronix (AFG3102C) function generator with a maximum signal amplitude of 10 V. To amplify the signal, it is passed through an RF amplifier (Acquitek A300) capable of amplifying the signal up to 54.5 times. Next, the signal passed through a terminal load with an impedance of 50 Ω to ensure a consistent amplifier output. The AC signal is then directed through a bias tee to a switch board, which is connected to a single element

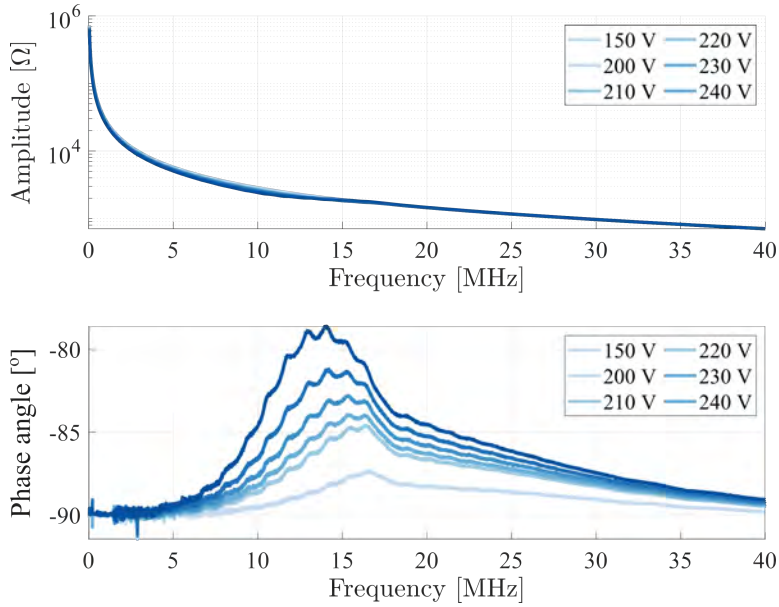


Figure 8.9: Biased impedance measurement performed on array S10, element 8 after mounting, wire bonding and PDMS casting. The wavy appearance is caused by interface reflections due to poor coupling between the PDMS and the ambient air.

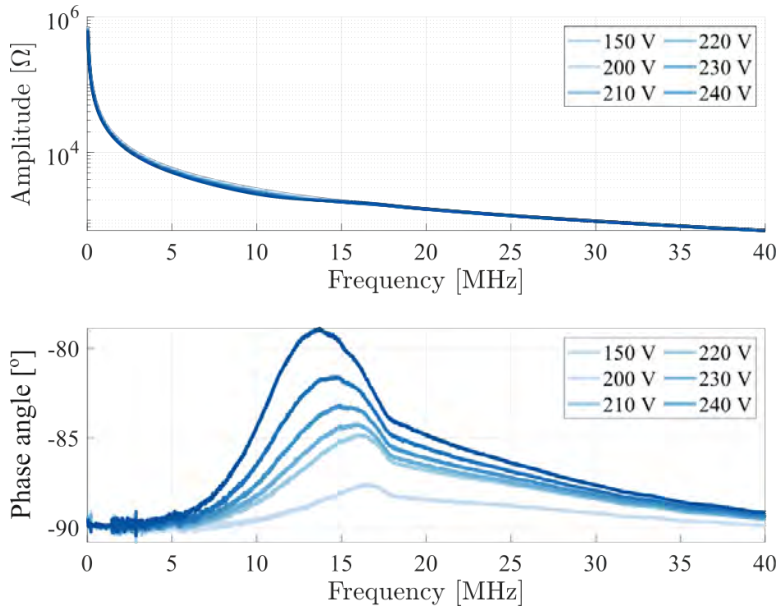


Figure 8.10: Biased impedance measurement performed on array S10, element 8 after mounting, wire bonding and PDMS casting. The measurement were performed in water, eliminating the interface ringing. This verifies good acoustic coupling between the PDMS and water, as anticipated.

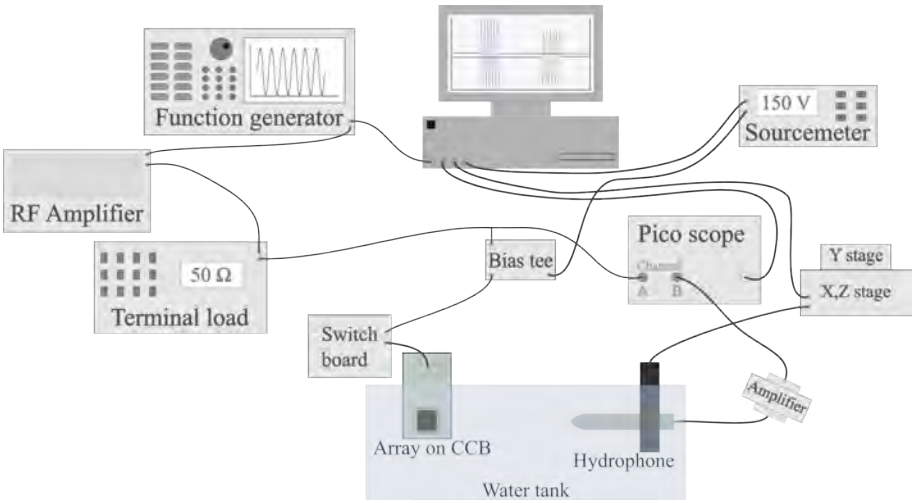


Figure 8.11: Illustration of the acoustical measurement setup used for transmission measurements. A function generator provides the AC signal, which is amplified before passed to the CCB through a terminal load, a bias tee and a switch board. The DC bias is generated by a sourcemeter. The hydrophone signal is amplified before going through a pico scope to the control computer. The hydrophone position is controlled using an XYZ-stage.

of the array through the CCB. Additionally, the AC signal is connected to channel A on the pico scope (Picotech 5000 Series) before being read by the computer. On the right side of the figure, a Keithley 2410 sourcemeter is depicted, which generates the DC potential. This DC potential is subsequently passed through the bias tee to the switch board and the CCB. The bottom center of the figure shows the hydrophone (Onda HGL-0400) located in a holder and submerged into a water tank. The holder is controlled by an Standa XYZ-stage, which is connected and controlled from the computer. The hydrophone signal is amplified and then passed through channel B on the pico scope before entering the computer.

For the pulse-echo measurements, a setup similar was utilized. However, instead of the hydrophone, a reflector was employed. To mitigate the noise from the Acquitec A300 RF amplifier, a different amplifier with a gain of 5 was used. This limited the AC voltages that could be applied to approximately 20 V peak-to-peak. The received signal from the CMUT was directed through the bias tee to a built in Low-Noise Amplifier (LNA) to channel B on the pico scope.

The measurements were performed for various AC potentials investigating the influence on the emitted signal. Since the output from the RF amplifiers varied based on the frequency, the passed signal was continuously adjusted for each frequency to achieve a constant AC potential for all measurements. A DC bias of 230 V was utilized. The obtained results for array

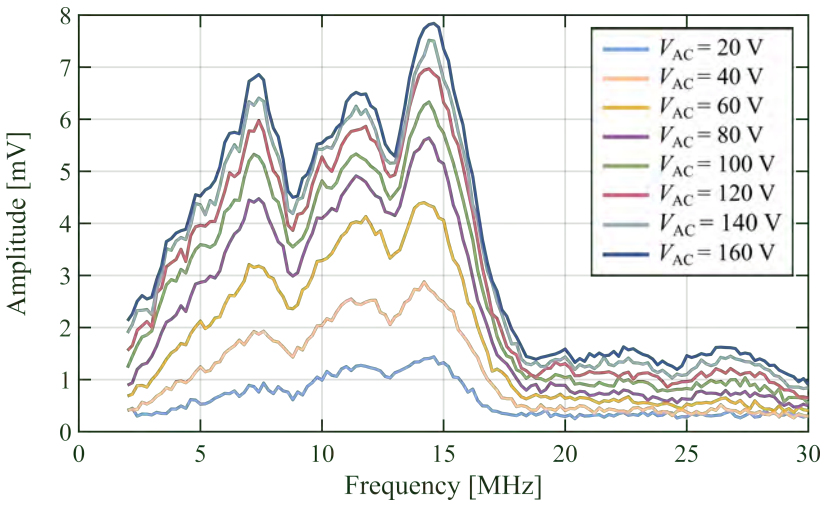


Figure 8.12: Transmitted signal measured by the hydrophone, showing a peak frequency of 14.6 MHz and a center frequency of 10.6 MHz. The measurements were performed on array S10, element 8. The measurements were performed applying a DC potential of 230 V.

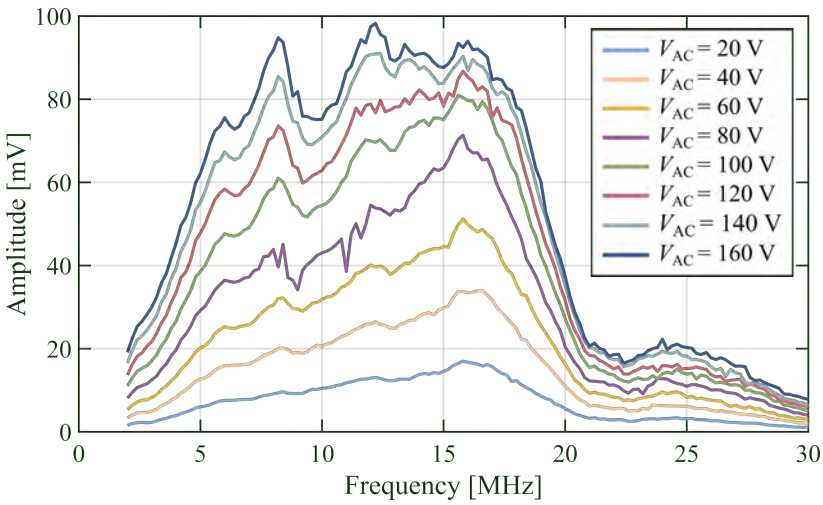


Figure 8.13: Transmitted signal measured by the hydrophone, showing a peak frequency of 12.2 MHz and a center frequency of 11.6 MHz. The data are obtained from array F10, element 9. The measurements were performed applying a DC potential of 230 V.

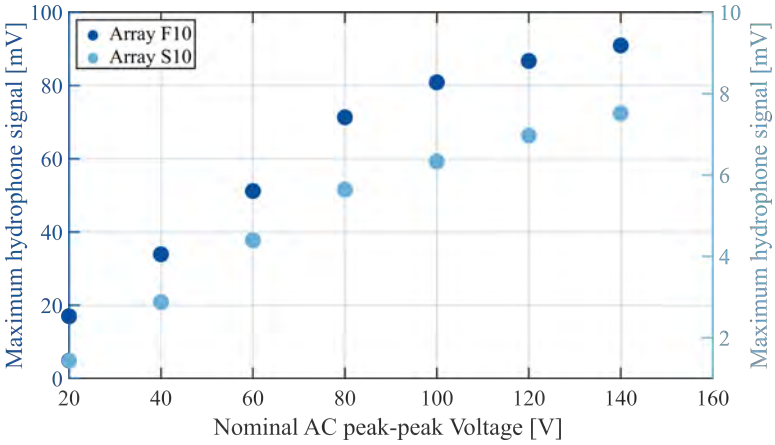


Figure 8.14: Maximum amplitude of the measured signal transmitted using array S10 and F10. The peak signal is shown relative to the applied nominal peak-to-peak AC voltage. The applied DC potential was 230 V.

S10 and F10 are presented in Fig. 8.12 and 8.13, respectively. Due to the shape of the spectra two frequencies were derived: the first, referred to as the center frequency was calculated from the weighted mean [42], while the second was the maximum frequency and is referred to as the peak frequency. Array S10 showed a center frequency of 10.6 MHz, and a peak frequency of 14.6 MHz, which aligns well with the impedance measurements presented in Fig. 8.10. The center frequency of array F10 was derived to be 11.6 MHz, and the maximum peak frequency to 12.2 MHz. Both values are slightly lower than indicated by the impedance measurements. However, the shape of the amplitude of the transmitted signal, makes determination of the center frequency more complicated. For both arrays a signal drop was observed at approximately 9.5 MHz. This is attributed to the substrate ringing, however, with a slightly higher frequency than the predicted value of 8.03 MHz.

Subsequently, the peak values for each applied AC voltage were extracted. These are shown relative to the AC voltage for both arrays in Fig. 8.14. It is evident that the maximum signal increases as the AC bias is raised, which is consistent with the expected behavior. For both array designs, a linear relation is observed between the hydrophone signal and AC voltages up to 80 V. However, beyond 80 V, the slope of the hydrophone signal versus the AC voltage diminishes.

The resulting frequency spectra for array S10 and F10 are shown in Fig. 8.15 and 8.16, respectively. The fractional bandwidth was determine for both the center frequency and the peak frequency. Furthermore, both were calculated for the −3 dB and −6 dB limit. The calculations were performed by utilizing

$$\text{fractional bandwidth} = \frac{f_{\text{upper}} - f_{\text{lower}}}{f} \times 100, \tag{8.1}$$

Table 8.1: Summary of the resulting relative fractional bandwidths from the two measured arrays, S10 and F10.

	Frequency		Bandwidth, center		Bandwidth, peak	
	f_c [MHz]	f_p [MHz]	−3 dB	−6 dB	−3 dB	−6 dB
S10	10.6	14.6	135.8	139.6	94.5	98.6
F10	11.6	12.2	143.1	150.0	134.4	141.0

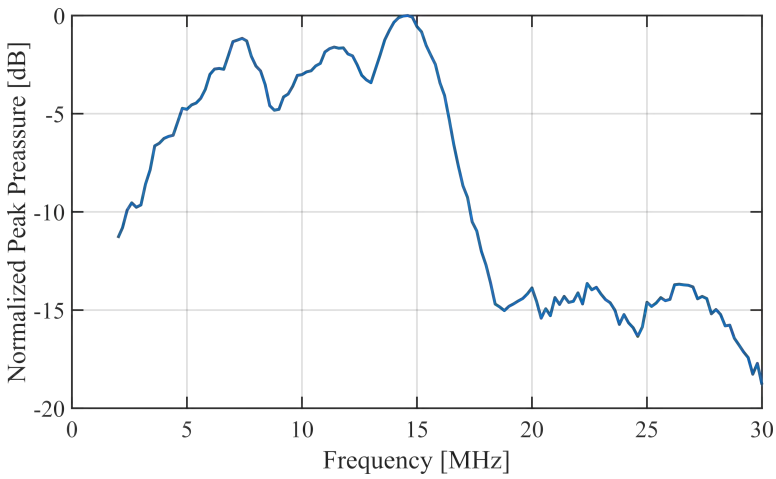


Figure 8.15: Frequency spectrum for the transmit measurement performed on array S10, element 8, normalized to the peak value. The data were obtained using a DC potential of 230 V and an AC potential of 160 V.

where f_{upper} is the upper frequency at the desired dB-level, while f_{lower} is the corresponding lower limit. Here f denotes either the center frequency or the peak frequency. The results for the two arrays are listed in Table 8.1. Based on the results it can be seen that the lowest bandwidth is the peak bandwidth for array S10. When consulting the spectrum this can be caused by the two pronounced drops in signal. The first can, as mentioned be attributed to substrate ringing. However, the reason for the peak drop at 13 MHz remains unknown. The remaining bandwidth results, the outcomes are highly satisfying when compared to other linear arrays fabricated within this research group. Notably, the largest the largest reported bandwidth was 116.8 % for a transducer with a center frequency of 6.6 MHz [16].

Following the transmission characterization, pulse-echo measurements were performed. This was only conducted on array F10, due to the lack of receive sensitivity on the low-capacitance array (S10). As earlier mentioned the RF amplifier was changed due to noise problems, leading to a maximum AC peak-to-peak signal of 20 V. The applied DC potential was 200 V. The measured amplitude spectrum is shown in Fig. 8.17. The center frequency

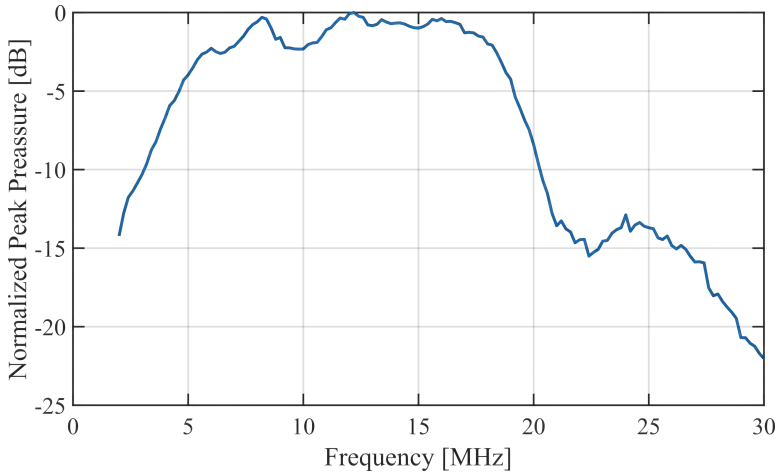


Figure 8.16: Frequency spectrum for the transmit measurement performed on array F10, element 9, normalized to the peak value. The applied DC bias was 230 V, while the AC potential was 160 V.

was derived to 12.2 MHz, while the peak frequency was found at 15.2 MHz. During the measurements, a noise floor of 100 mV was observed, and it was subsequently subtracted as a baseline from the spectrum. It is worth noting that the amplitude appears larger in comparison to the transmit measurements, primarily due to the use of the LNA in receive mode.

The normalized pulse-echo spectrum is shown in Fig. 8.18. Similar to the transmission spectra, a signal drop is observed around 10 MHz. The −6 dB bandwidth related to the center frequency was calculated to 119.7 %, while the −6 dB peak related bandwidth resulted in 85.5 %. These values are an improvement of the previously reported fractional bandwidths for pulse-echo measurements [16].

Based on these measurements it can be concluded that the performance of the fabricated CMUTs is satisfactory, with center and peak frequencies slightly lower than the designed value of 15 MHz and with a bandwidth of more than 100 % in transmit mode and larger than 85 % in pulse-echo. Furthermore, it was validated that both array designs performed as expected for potentials comparable to those delivered by the scanner system.

Finally, it should be noted that the acoustical measurement setup was built for measurements at lower frequencies of 5 MHz to 8 MHz. The transducer fabricated during this Ph.D. project is the first within the research group aimed and fabricated with a center frequency around 15 MHz. Acoustical measurements become increasingly difficult with increasing frequency, which among others are indicated by the applied hydrophone, which according to the available data can only be calibrated up to 20 MHz. Therefore, a comprehensive update of the acoustical measurement setup, including a hy-

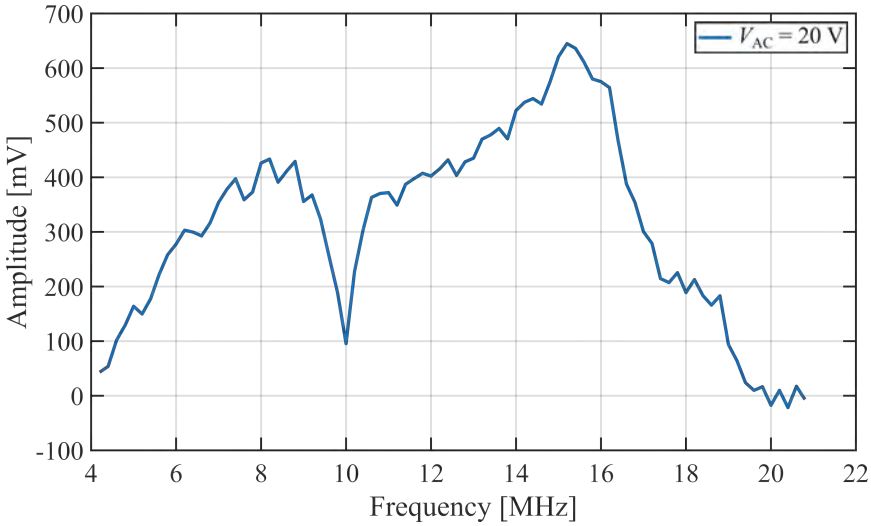


Figure 8.17: Pulse-echo signal obtain from array F10, element 9. An inherent noise floor of 100 mV was subtracted from the spectrum. The measurement was performed using a DC bias of 200 V and a peak-to-peak AC potential of 20 V.

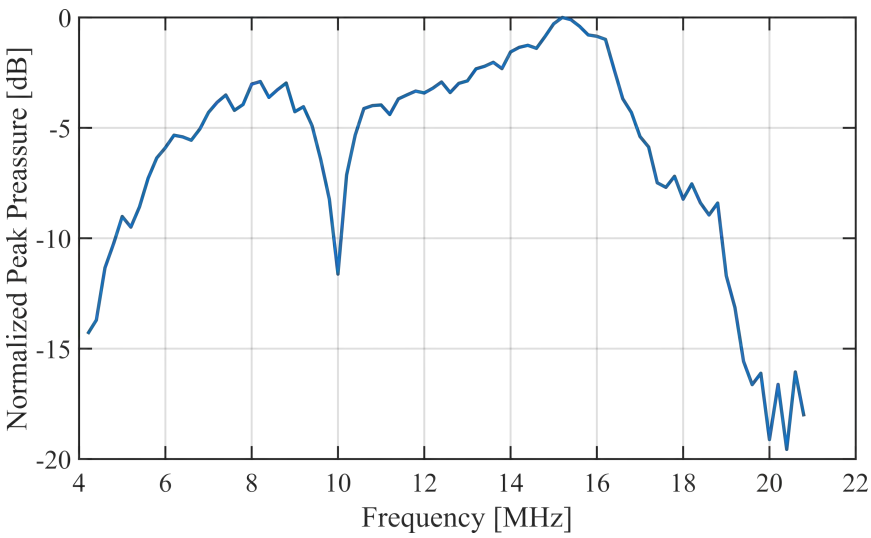


Figure 8.18: Normalized frequency spectrum for the pulse-echo measurement obtained from array F10, element 9. The measurement was performed using a DC bias of 200 V and a peak-to-peak AC potential of 20 V.

drophone centered around 15 MHz, is required to optimize the measurement conditions for future transducer generations.

8.4 Chapter Summary

This chapter presented the array assembly process, along with the impedance and acoustical measurements performed during and after the packaging phase. Mounting, wire bonding, and casting of four 16-element arrays from the maskless LOCOS wafer were successfully conducted. The packaged arrays involved two of the *Single* design and two with the *Filled* design. Initially, the arrays were mounted on CCBs using a UV-sensitive adhesive. Following the curing process, a heating program with a temperature of 85 °C was employed to finalize the mounting process. The arrays were then wire bonded using an ultrasonic power of 90 and a force of 200 at an elevated stage temperature of 110 °C. This resulted in a pull bond strength of 13.5 g, which exceeds industrial standards and is highly satisfactory [109]. To ensure precise placement of the primer before the PDMS casting step, Kapton tape was applied to the CCBs. The PDMS was applied and subsequently degassed in a vacuum chamber for approximately 10 min before the layer was planarized under pressure for 20 h. The casting step was also carried out on the backside to prevent potential damage, when submerged into the water tank.

Biased impedance measurement were conducted before and after the casting step to monitor the element performance throughout the process. The impedance and phase angle exhibited a clear spring softening effect as the bias was increased. Additionally, the frequency remained constant throughout the mounting process for array S10, while a slight increase of 1 MHz was observed for array F10. An increase of 2 pF was observed in the capacitance for both designs, which was attributed to the wire bond capacitance. Following the PDMS casting, the biased impedance measurements were repeated. It was observed that the applied PDMS layer resulted in a frequency shift from 20.7 MHZ to 14 MHz, consistent with the predictions from the OnScale simulations discussed Section 3.1.2. A comparison of the impedance measurements in air and water revealed a significant improvement in acoustical coupling from the PDMS to the ambient medium when submerged in water, which was also reflected in the simulated pressure data.

Finally, two arrays underwent acoustical characterization. The arrays showed a center frequency of 10.6 MHz and 11.6 MHz for array S10 and F10, respectively. The related bandwidths for the −6 dB limit both exceeded 139 %. The peak frequency was slightly higher for both arrays with values of 14.6 MHz and 12.2 MHz, respectively. Here the fractional bandwidth for the −6 dB limit were 98.6 % for the *Single* design and 141.0 % for the *Filled* design. The pulse-echo measurements resulted in a center

frequency of 12.2 MHz with and bandwidth of 119.7 %, while the peak frequency was found to be 15.2 MHz with a fractional bandwidth of 85.5 %. The measurements validated that both array designs performed as expected for potentials comparable to those delivered by the scanner system.

CHAPTER 9

Conclusion and Outlook

The main objective for this project was to design and fabricate a linear CMUT-based transducer for the SURE-project, operating at 15 MHz in immersion with a pitch of $\lambda/2$. The project successfully achieved this objective by utilizing a structural layout that combined LOCOS and fusion bonding techniques. To improve the understanding of CMUT behavior, simulation tools were developed and studies were conducted on clamping conditions and shear effects. This was of increasing interest due to the high frequency and small pitch requirements. Furthermore, a novel electrical wafer-level characterization method was developed and tested on two successfully fabricated wafers.

In Chapter 2 central parameters for CMUTs were derived and described using CPT as a foundation for the subsequent transducer modeling. An improved analytical expression was derived for the resonance frequency in immersion, employing the equation of motion and an optimized approximation for the radiation impedance. The error of the radiation impedance was reduced from 24 % to 2.5 % for $ka = 1.0$ (where k is the wavenumber and a defines the cell radius) by introducing the Padé approximant. The analytical derived expression showed improved validity for a broader range of plate aspect ratios. However, FEM simulations revealed the need to encounter shear stresses in the plate for lower aspect ratios. Secondly, a heuristic model introducing an effective radius of $a_{\text{eff}} = a + \mathcal{C}h$ was proposed. This model incorporated stress distributions in the bonding region and reduced the error with up to 7 % for a plate of $h/a = 0.1$ for various parameters. Based on FEM results $\mathcal{C}$ were approximated to be 0.68 for thin plates. Finally, shear effects were examined in relation to the derived CPT expressions through FEM simulations for various plate aspect ratios. For a plate aspect ratio

of 4, the error compared to the CPT expressions exceeded 15 % for both the plate deflection, the resonance frequency in vacuum and immersion, and pull-in voltage. Furthermore, incorporating shear effects into the plate deflection equation reduced the error from 22.2 % to 0.21 %. These findings emphasized the necessity of including shear effects in analytical analysis for high-frequency, small pitch transducers.

Chapter 3 outlined the design phase for LOCOS-based CMUT designs, following an iterative methodology combining analytical calculations and FEM simulations. Three probe designs were created: Lin384, a linear array comprising 384 elements operating at 15 MHz and $\lambda/2-$pitch, and two designs for laparoscope integration with 192 elements and a resonance frequency of 9.3 MHz. Here the first design, LapMUT-A, utilized the entire laparoscope space, while the second design, LapMUT-B, had a pitch of $\lambda/2$. A simulation based study investigated problems related to nitride protruding above the bonding surface, hindering the fusion bonding process for a single LOCOS process. It was concluded that the greatest impact originated from the combination of the masking nitride thickness and the gap height, which significantly affected fabrication feasibility. A related fabrication study utilizing the LapMUT-B design revealed the critical role of process control as even minor aberrations can result in processing failure. Finally, it was established that the three proposed methods for silicon bump fabrication all showed an increase in cell radius with values varying from 1.3 µm to 2.2 µm. These findings were essential to incorporate into the lithography mask design, which was accordingly decreased by 1.3 µm.

Chapter 4 investigated two processes to enable backside contacting of CMUTs for laparoscope integration. A deep silicon trenches of 140 µm with a width varying from 3.2 µm at the top to 1.1 µm at the bottom were successfully created. Subsequently, thermal oxide provided electrical insulation, while poly-silicon plugs reinforced the structure. However, optimization was needed as the trench plugging occurred on the top of the trench before the middle and bottom sections, compromising mechanical stability. Due to termination of the laparoscope project, further optimization was not conducted. However, suggestions for further optimization included adjusting the etching recipe to achieve a more tapered trench outline and incorporate additional oxidation to increase the trench opening. Secondly, lapping was employed for substrate thinning. It was showed that decreasing the abrasive grain size from 20 µm to 9 µm, reduced the average surface roughness from 318 nm to 163 nm. However, to enable subsequent bonding, polishing was required. A combination of the two processes was successfully employed for fabrication of a CMUT-based row-column design similar to the one presented in Paper C, demonstrating a wider feasibility than the intended laparoscopic transducer integration.

Chapter 5 provided a detailed description of the fabrication process utilizing the Lin384 design. Three different methods were tested for fabricating

the silicon bumps, and two wafers were successfully finalized: one utilizing the double LOCOS process and the other utilizing the maskless LOCOS method. The RIE-based method resulted in a surface roughness of 1.26 nm, which posed challenges during the fusion bonding process. Nevertheless, AFM measurements of the cavities validated the simulations, showing an increased cell radius of 1.3 µm for all three processes. Due to the reduction in cell radius in the lithography mask layout, the resulting cell radius was 22.3 µm, which aligned with the design specifications.

Chapter 6 presented a novel wafer-level characterization method for electrical analysis, utilizing two measurement setups. The method employed a step-wise selection approach, exclusively focusing on the most promising arrays to save time compared to a comprehensive characterization of all arrays. Visual inspection was initially conducted, followed by unbiased impedance measurements on the selected arrays to check for capacitive behavior and short circuits. The best arrays underwent a comprehensive CV analysis to investigate potential charging phenomena. The charging effects were successfully quantified by the charges on the capacitor plates relative to the applied bias. Finally, a full biased impedance analysis was conducted, including resonance frequency determination, pull-in voltage measurement, and long-term stability assessment of a few elements.

The method was subsequently applied on the two successfully fabricated wafers, and the results were presented in Chapter 7. The first wafer, utilizing the maskless LOCOS process, showed a fabrication yield of 65.5 % based on the visual inspection. All 19 arrays characterized using unbiased impedance measurements demonstrated capacitive behavior, and 98.8 % of the measured elements exhibited a capacitance corresponding to the design. No dielectric charging was observed from the performed CV measurements. The center frequency in air was measured to 20.4 MHz before assembly. The double LOCOS wafer showed a similar yield based on the visual inspection and the capacitive behavior. The yield based on the capacitance level was 98.6 %, indicating few short circuits between neighboring top electrodes. However, during the CV characterization the majority of the elements exhibited dielectric charging effect resulting in a yield of only 10 %. The reason for this remains unknown. Subsequent to the bump definition the two wafers underwent the exact same processing. Therefore, the charging should not be attributed a quality difference in the oxide and nitride layers. However, a more pronounced misalignment of approximately 3 µm was observed on double LOCOS wafer compared to the maskless LOCOS wafer with a maximum misalignment of 1.5 µm. Such misalignment of the cavity relative to the bump skew the transverse electrical field, which potentially can result in charging effects. This is subject to further investigation. The novel wafer-level characterization method showed promising results, however a drawback is its ability to detect charging effects in the initial characterization phase.

Finally, four 16-element arrays from the maskless LOCOS wafer were suc-

cessfully assembled and measured using an acoustical measurement setup. These processes were described in Chapter 8. The arrays were mounted on a CCB and electrically connected through wire bonds, having a pull strength of 13.5 g. Biased impedance measurements were conducted before and after the PDMS casting process. The arrays exhibited a slight increase in capacitance (around 2 pF), attributed to the wire bond capacitance. The predictions from simulations conducted during the design phase was confirmed illustration that the main shift in center frequency originated from the PDMS casting process. Acoustical measurements were successfully conducted on two arrays in transmit mode, showing center frequencies of 10.6 MHz and 11.6 MHz for array S10 and F10, respectively. The related bandwidths for the −6 dB limit both exceeded 139 %. Only array F10 was measured in pulse-echo mode due to lack of receive sensitivity for array S10. However, array F10 showed a center frequency of 12.2 MHz with and bandwidth of 119.7 %. The measurements validated that both array designs performed as expected for potentials comparable to those delivered by the scanner system. It was concluded that for future high-frequency transducer generations, a comprehensive update of the acoustical measurement setup is required.

Future investigation built on the work presented in this thesis includes further research on charging effects. An initial experiment includes intentionally misalignment of the cavity relative to the bump incorporated into the mask design. Applying varying degrees of misalignment on the same wafer is expected to reveal a potential relation.

Furthermore, when the CCB for the Lin384 array has been finalized, the next natural step is mounting and packaging of the best performing array into a nose piece for the prototype probe [48]. Based on the performance, design and process optimization can be included in a second generation of the linear transducer for super resolution imaging.

Bibliography

[1] Piezo.com. The history of piezoelectricity. Accessed: 30/06-2023. [Online]. Available: https://piezo.com/pages/history-of-piezoelectricity

[2] I. Edler and K. Lindström, "The history of echocardiography," *Ultrasound in medicine & biology*, vol. 30, no. 12, pp. 1565–1644, 2004.

[3] Butterfly networks. Accessed: 20/07-2023. [Online]. Available: https://www.butterflynetwork.com/

[4] J. A. Jensen, *Estimation of Blood Velocities Using Ultrasound: A Signal Processing Approach.* New York: Cambridge University Press, 1996.

[5] G. H. Haertling, "Ferroelectric ceramics: history and technology," *Journal of the American Ceramic Society*, vol. 82, no. 4, pp. 797–818, 1999.

[6] T. R. Shrout and S. J. Zhang, "Lead-free piezoelectric ceramics: Alternatives for pzt?" *Journal of Electroceramics*, vol. 19, pp. 113–126, 2007.

[7] A. Ergun, S. Barnes, and E. Gardner, "An assessment of the thermal efficiency of capacitive micromachined ultrasonic transducers," in *2007 IEEE Ultrasonics Symposium Proceedings.* IEEE, 2007, pp. 420–423.

[8] T. X. Misaridis, K. Gammelmark, C. H. Jørgensen, N. Lindberg, A. H. Thomsen, M. H. Pedersen, and J. A. Jensen, "Potential of coded excitation in medical ultrasound imaging," *Ultrasonics*, vol. 38, no. 1-8, pp. 183–189, 2000.

[9] M. H. Pedersen, T. X. Misaridis, and J. A. Jensen, "Clinical evaluation of chirp-coded excitation in medical ultrasound," *Ultrasound in medicine & biology*, vol. 29, no. 6, pp. 895–905, 2003.

[10] M. I. Haller and B. T. Khuri-Yakub, "Surface micromachined electrostatic ultrasonic air transducer," in *Proceedings of the IEEE Ultrasonics Symposium*, vol. 2, 1994, pp. 1241–1244.

[11] ——, "A surface micromachined electrostatic ultrasonic air transducer," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 43, no. 1, pp. 1–6, 1996.

[12] R. Maity, N. Maity, S. Rao Karumuri, G. Sravani, and K. Guha, "Design of single cell membrane shape and array configuration for mems based micromachined ultrasonic sensor to improve the performance: A three dimensional model characterization," *Transactions on Electrical and Electronic Materials*, pp. 1–12, 2021.

[13] A. Caronti, G. Caliano, R. Carotenuto, A. Savoia, M. Pappalardo, E. Cianci, and V. Foglietti, "Capacitive micromachined ultrasonic transducer (cmut) arrays for medical imaging," *Microelectronics Journal*, vol. 37, no. 8, pp. 770–777, 2006.

[14] O. Oralkan, A. S. Ergun, J. A. Johnson, M. Karaman, U. Demirci, K. Kaviani, T. H. Lee, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: Next-generation arrays for acoustic imaging?" *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 49, no. 11, pp. 1596–1610, 2002.

[15] B.-H. Kim, S. Lee, Y. Kim, K. Cho, T. Jeon, K. Kim, and J. Song, "An experimental study on coded excitation in cmut arrays to utilize simultaneous transmission multiple-zone focusing method with frequency divided sub-band chirps," in *2013 IEEE International Ultrasonics Symposium (IUS)*. IEEE, 2013, pp. 1428–1431.

[16] S. E. Diederichsen, "Micromachined Integrated Transducers for Ultrasound Imaging," Ph.D. Thesis, Technical University of Denmark, Department of Micro- and Nanotechnology, 2019.

[17] O. Oralkan, X. Jin, K. Kaviani, A. Ergun, F. Degertekin, M. Karaman, and B. Khuri-Yakub, "Initial pulse-echo imaging results with one-dimensional capacitive micromachined ultrasonic transducer arrays," in *2000 IEEE Ultrasonics Symposium. Proceedings. An International Symposium (Cat. No. 00CH37121)*, vol. 1. IEEE, 2000, pp. 959–962.

[18] O. Oralkan, A. S. Ergun, C.-H. Cheng, J. A. Johnson, M. Karaman, T. H. Lee, and B. T. Khuri-Yakub, "Volumetric ultrasound imaging using 2-d cmut arrays," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 50, no. 11, pp. 1581–1594, 2003.

[19] K. Karadayi, R. Managuli, and Y. Kim, "Three-dimensional ultrasound: from acquisition to visualization and from algorithms to systems," *IEEE Reviews in Biomedical Engineering*, vol. 2, pp. 23–39, 2009.

[20] A. S. Savoia, G. Caliano, and M. Pappalardo, "A cmut probe for medical ultrasonography: From microfabrication to system integration," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 59, no. 6, pp. 1127–1138, 2012.

[21] S. Holbek, T. L. Christiansen, M. B. Stuart, C. Beers, E. V. Thomsen, and J. A. Jensen, "3-d vector flow estimation with row–column-addressed arrays," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 63, no. 11, pp. 1799–1814, 2016.

[22] J. Jensen, M. B. Stuart, and J. A. Jensen, "Optimized plane wave imaging for fast and high-quality ultrasound imaging," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 63, no. 11, pp. 1922–1934, 2016.

[23] M. F. La Cour, M. B. Stuart, M. B. Laursen, S. E. Diederichsen, E. V. Thomsen, and J. A. Jensen, "Investigation of pdms as coating on cmuts for imaging," in *2014 IEEE International Ultrasonics Symposium*. IEEE, 2014, pp. 2584–2587.

[24] J. Due-Hansen, K. Midtbø, E. Poppe, A. Summanwar, G. Jensen, L. Breivik, D. Wang, and K. Schjølberg-Henriksen, "Fabrication process for cmut arrays with polysilicon electrodes, nanometre precision cavity gaps and through-silicon vias," *Journal of Micromechanics and Microengineering*, vol. 22, no. 7, p. 074009, 2012.

[25] X. Zhuang, A. S. Ergun, Y. Huang, I. O. Wygant, O. Oralkan, and B. T. Khuri-Yakub, "Integration of trench-isolated through-wafer interconnects with 2d capacitive micromachined ultrasonic transducer arrays," *Sensors and Actuators A: Physical*, vol. 138, no. 1, pp. 221–229, 2007.

[26] G. Caliano, A. Caronti, A. Savoia, C. Longo, M. Pappalardo, E. Cianci, and V. Foglietti, "Capacitive micromachined ultrasonic transducer (cmut) made by a novel" reverse fabrication process"," in *IEEE Ultrasonics Symposium, 2005.*, vol. 1. IEEE, 2005, pp. 479–482.

[27] P. Zhang, G. Fitzpatrick, T. Harrison, W. A. Moussa, and R. J. Zemp, "Double-soi wafer-bonded cmuts with improved electrical safety and minimal roughness of dielectric and electrode surfaces," *Journal of microelectromechanical systems*, vol. 21, no. 3, pp. 668–680, 2012.

[28] J. Joseph, B. Ma, and B. Khuri-Yakub, "Applications of capacitive micromachined ultrasonic transducers: A comprehensive review," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 69, no. 2, pp. 456–467, 2021.

[29] A. Erguri, Y. Huang, X. Zhuang, O. Oralkan, G. G. Yarahoglu, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: Fabrication technology," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 52, no. 12, pp. 2242–2258, 2005.

[30] J. Joseph, S. G. Singh, and S. R. K. Vanjari, "Fabrication of su-8 based capacitive micromachined ultrasonic transducer for low frequency therapeutic applications," in *2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. IEEE, 2015, pp. 1365–1368.

[31] F. Y. Yamaner, X. Zhang, and O. Oralkan, "A three-mask process for fabricating vacuum-sealed capacitive micromachined ultrasonic transducers using anodic bonding," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 62, no. 5, pp. 972–982, 2015.

[32] A. S. Ergun, Y. Huang, C.-H. Cheng, O. Oralkan, J. Johnson, H. Jagannathan, U. Demirci, G. G. Yaralioglu, M. Karaman, and B. T. Khuri-Yakub, "Broadband capacitive micromachined ultrasonic transducers ranging from 10 khz to 60 mhz for imaging arrays and more," in *2002 IEEE Ultrasonics Symposium, 2002. Proceedings.*, vol. 2. IEEE, 2002, pp. 1039–1043.

[33] Y. Huang, A. S. Ergun, E. Haeggstrom, M. H. Badi, and B. T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology," *Journal of microelectromechanical systems*, vol. 12, no. 2, pp. 128–137, 2003.

[34] M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation," *Proceedings of the IEEE*, vol. 86, no. 8, pp. 1575–1585, 1998.

[35] K. Park, H. Lee, M. Kupnik, O. Oralkan, and B. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with direct wafer-bonding and locos technology," in *2008 IEEE 21st International Conference on Micro Electro Mechanical Systems*. IEEE, 2008, pp. 339–342.

[36] K. K. Park, H. Lee, M. Kupnik, and B. T. Khuri-Yakub, "Fabrication of capacitive micromachined ultrasonic transducers via local oxidation and direct wafer bonding," *Journal of microelectromechanical Systems*, vol. 20, no. 1, pp. 95–103, 2011.

[37] K. Steenberg, "Micromachined 2d transducers for 3-d super-resolution ultrasound real-time imaging of erythrocytes," Ph.D. Thesis, Technical University of Denmark, Department of Health Technology, 2023.

[38] A. S. Havreland, M. Engholm, B. G. Tomov, J. A. Jensen, O. Hansen, and E. V. Thomsen, "Cmut electrode resistance design: Modeling and experimental verification by a row-column array," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 66, no. 6, pp. 1110–1118, 2019.

[39] A. S. Havreland, "Micromachined integrated 2d transducers for ultrasound imaging," Ph.D. Thesis, Technical University of Denmark, Department of Health Technology, 2019.

[40] M. Engholm, "Capacitive Micromachined Ultrasonic Transducers for 3-d imaging," Ph.D. Thesis, Technical University of Denmark, Department of Micro- and Nanotechnology, 2018.

[41] M. J. G. Mølgaard, "Capacitive Micromachined Ultrasonic Transducers for gas sensing," Ph.D. Thesis, Technical University of Denmark, Department of Micro- and Nanotechnology, 2018.

[42] R. S. Grass, "Micromachined integrated 2d transducers for super resolution ultrasound imaging," Ph.D. Thesis, Technical University of Denmark, Department of Health Technology, 2022.

[43] H. Himal, "Minimally invasive (laparoscopic) surgery," *Surgical Endoscopy And Other Interventional Techniques*, vol. 16, pp. 1647–1652, 2002.

[44] BK Medical. Laparoscope specifications. Accessed: 30/06-2023. [Online]. Available: https://www.bkmedical.com/transducers/4-way-laparoscopic-8666-rf/

[45] D.-S. Lin, R. Wodnicki, X. Zhuang, C. Woychik, K. E. Thomenius, R. A. Fisher, D. M. Mills, A. J. Byun, W. Burdick, P. Khuri-Yakub *et al.*, "Packaging and modular assembly of large-area and fine-pitch 2-d ultrasonic transducer arrays," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 60, no. 7, pp. 1356–1375, 2013.

[46] R. Wodnicki, C. G. Woychik, A. T. Byun, R. Fisher, K. Thomenius, D.-S. Lin, X. Zhuang, O. Oralkan, S. Vaithilingam, and B. T. Khuri-Yakub, "Multi-row linear cmut array using cmuts and multiplexing electronics," in *2009 IEEE International Ultrasonics Symposium.* IEEE, 2009, pp. 2696–2699.

[47] B. Chang, P. Leussink, F. Jensen, J. Hübner, and H. Jansen, "Drem: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed bosch drie process," *Microelectronic Engineering*, vol. 191, pp. 77–83, 2018.

[48] K. F. Pedersen, M. Engholm, A. S. Havreland, L. N. Moesner, C. Beers, B. G. Tomov, J. A. Jensen, and E. V. Thomsen, "384 channel modular ultrasonic cmut probe for rapid prototyping," in *2020 IEEE International Ultrasonics Symposium (IUS).* IEEE, 2020, pp. 1–3.

[49] H. Lamb, "On the vibrations of an elastic plate in contact with water," *Proceedings of the royal society of London. Series A, containing papers of a mathematical and physical character*, vol. 98, no. 690, pp. 205–216, 1920.

[50] S. S. Kumar and B. Pant, "Design principles and considerations for the 'ideal'silicon piezoresistive pressure sensor: a focused review," *Microsystem technologies*, vol. 20, pp. 1213–1247, 2014.

[51] G. Fragiacomo, K. Reck, L. Lorenzen, and E. V. Thomsen, "Novel designs for application specific mems pressure sensors," *Sensors*, vol. 10, no. 11, pp. 9541–9563, 2010.

[52] K. Reck, E. V. Thomsen, and O. Hansen, "All-optical frequency modulated high pressure mems sensor for remote and distributed sensing," *Sensors*, vol. 11, no. 11, pp. 10 615–10 623, 2011.

[53] W. P. Eaton and J. H. Smith, "Micromachined pressure sensors: review and recent developments," *Smart Materials and Structures*, vol. 6, no. 5, p. 530, 1997.

[54] S. Timoshenko, S. Woinowsky-Krieger *et al.*, *Theory of plates and shells.* McGraw-hill New York, 1959, vol. 2.

[55] E. Ventsel, T. Krauthammer, and E. Carrera, "Thin plates and shells: theory, analysis, and applications," *Appl. Mech. Rev.*, vol. 55, no. 4, 2002.

[56] M. F. la Cour, T. L. Christiansen, J. A. Jensen, and E. V. Thomsen, "Electrostatic and small-signal analysis of cmuts with circular and square anisotropic plates," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 62, no. 8, pp. 1563–1579, 2015.

[57] I. O. Wygant, M. Kupnik, and B. T. Khuri-Yakub, "Analytically calculating membrane displacement and the equivalent circuit model of a circular cmut cell," in *2008 IEEE ultrasonics symposium.* IEEE, 2008, pp. 2111–2114.

[58] M. Kwak, "Vibration of circular plates in contact with water," 1991.

[59] J. Powell and J. Roberts, "On the frequency of vibration of circular diaphragms," *Proceedings of the physical society of London*, vol. 35, no. 1, p. 170, 1922.

[60] M. Amabili and M. Kwak, "Free vibrations of circular plates coupled with liquids: revising the lamb problem," *Journal of fluids and structures*, vol. 10, no. 7, pp. 743–761, 1996.

[61] S. E. Diederichsen, J. M. F. Hansen, M. Engholm, E. V. Thomsen *et al.*, "Output pressure and pulse-echo characteristics of cmuts as function of plate dimensions," in *2017 IEEE International Ultrasonics Symposium (IUS).* IEEE, 2017, pp. 1–4.

[62] M. Greenspan, "Piston radiator: Some extensions of the theory," *The Journal of the Acoustical Society of America*, vol. 65, no. 3, pp. 608–621, 1979.

[63] C. M. Bender, S. Orszag, and S. A. Orszag, *Advanced mathematical methods for scientists and engineers I: Asymptotic methods and perturbation theory.* Springer Science & Business Media, 1999, vol. 1.

[64] I. Senjanović, N. Vladimir, and M. Tomić, "An advanced theory of moderately thick plate vibrations," *Journal of Sound and Vibration*, vol. 332, no. 7, pp. 1868–1880, 2013.

[65] W. Weaver Jr, S. P. Timoshenko, and D. H. Young, *Vibration problems in engineering.* John Wiley & Sons, 1991.

[66] S. H. Hashemi and M. Arsanjani, "Exact characteristic equations for some of classical boundary conditions of vibrating moderately thick rectangular plates," *International Journal of Solids and Structures*, vol. 42, no. 3-4, pp. 819–853, 2005.

[67] R. Gregory and F. Wan, "Boundary conditions at the edge of a thin or thick plate bonded to an elastic support," *Journal of elasticity*, vol. 36, pp. 155–182, 1994.

[68] E. V. Thomsen, K. Reck, G. Skands, C. Bertelsen, and O. Hansen, "Silicon as an anisotropic mechanical material: Deflection of thin crystalline plates," *Sensors and Actuators A: Physical*, vol. 220, pp. 347–364, 2014.

[69] P. J. Ryan, G. G. Adams, and N. E. McGruer, "Modeling of a one-sided bonded and rigid constraint using beam theory," 2008.

[70] D. Hu and G. G. Adams, "A boundary condition correction for the clamped constraint of elastic plate/beam theory," *International Journal of Solids and Structures*, vol. 124, pp. 229–234, 2017.

[71] A. S. Havreland, M. Engholm, C. V. SØrensen, and E. V. Thomsen, "Pull-in analysis of cmut elements," in *2020 IEEE International Ultrasonics Symposium (IUS)*. IEEE, 2020, pp. 1–4.

[72] C. Chinwuba Ike, "Mathematical solutions for the flexural analysis of mindlin's first order shear deformable circular plates," *Mathematical Models in Engineering*, vol. 4, no. 2, pp. 50–72, 2018.

[73] A. Logan and J. T. Yeow, "Fabricating capacitive micromachined ultrasonic transducers with a novel silicon-nitride-based wafer bonding process," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 56, no. 5, pp. 1074–1084, 2009.

[74] O. Oralkan, A. S. Ergun, J. A. Johnson, M. Karaman, U. Demirci, K. Kaviani, T. H. Lee, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: Next-generation arrays for acoustic imaging?" *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 49, no. 11, pp. 1596–1610, 2002.

[75] F. Y. Yamaner, S. Olcum, H. K. Oguz, A. Bozkurt, H. Koymen, and A. Atalar, "High-power cmuts: design and experimental verification," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 59, no. 6, pp. 1276–1284, 2012.

[76] A. E. H. Love, *A treatise on the mathematical theory of elasticity*. University press, 1927.

[77] J. Hutchinson, "Shear coefficients for timoshenko beam theory," *J. Appl. Mech.*, vol. 68, no. 1, pp. 87–92, 2001.

[78] S. Vlachoutsis, "Shear correction factors for plates and shells," *International Journal for Numerical Methods in Engineering*, vol. 33, no. 7, pp. 1537–1552, 1992.

[79] G. G. Yaralioglu, S. Ergun, and B. T. Khuri-Yakub, "Finite-element analysis of capacitive micromachined ultrasonic transducers," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 52, no. 12, pp. 2185–2198, 2005.

[80] Y. Roh and B. T. Khuri-Yakub, "Finite element analysis of underwater capacitor micromachined ultrasonic transducers," *IEEE transactions*

on ultrasonics, ferroelectrics, and frequency control, vol. 49, no. 3, pp. 293–298, 2002.

[81] A. Caronti, A. Savoia, G. Caliano, and M. Pappalardo, "Acoustic coupling in capacitive microfabricated ultrasonic transducers: Modeling and experiments," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 52, no. 12, pp. 2220–2234, 2005.

[82] B. Bayram, M. Kupnik, G. G. Yaralioglu, O. Oralkan, A. S. Ergun, D.-S. Lin, S. H. Wong, and B. T. Khuri-Yakub, "Finite element modeling and experimental characterization of crosstalk in 1-d cmut arrays," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 54, no. 2, pp. 418–430, 2007.

[83] M. Engholm, A. Tweedie, J. Jensen, G. Harvey, E. V. Thomsen *et al.*, "Simulating cmut arrays using time domain fea," in *2017 IEEE International Ultrasonics Symposium (IUS)*. IEEE, 2017, pp. 1–4.

[84] K. Howard, L. Ramirez, B. H. You, and I.-H. Song, "Design analysis of capacitive micromachined ultrasonic transducers," in *2022 IEEE 17th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*. IEEE, 2022, pp. 296–300.

[85] B. E. Deal and A. Grove, "General relationship for the thermal oxidation of silicon," *Journal of applied physics*, vol. 36, no. 12, pp. 3770–3778, 1965.

[86] S. W. Gjaldbæk, "Process development, fabrication and characterisation of capacitive micromachined ultrasonic transducers," Master's Thesis, Technical University of Denmark, Department of Micro- and Nanotechnology, 2022.

[87] I. Ladabaum, P. Wagner, C. Zanelli, J. Mould, P. Reynolds, and G. Wojcik, "Silicon substrate ringing in microfabricated ultrasonic transducers," in *2000 IEEE Ultrasonics Symposium. Proceedings. An International Symposium (Cat. No. 00CH37121)*, vol. 1. IEEE, 2000, pp. 943–946.

[88] C. Gui, H. Albers, J. G. E. Gardeniers, M. Elwenspoek, and P. V. Lambeck, "Fusion bonding of rough surfaces with polishing technique for silicon micromachining," *Microsystem Technologies*, vol. 3, no. 3, pp. 122–128, 1997.

[89] M. J. Mølgaard, J. M. Hansen, M. H. Jakobsen, and E. V. Thomsen, "Sensitivity optimization of wafer bonded gravimetric cmut sensors," *Journal of Microelectromechanical Systems*, vol. 27, no. 6, pp. 1089–1096, 2018.

[90] W. Runyan and K. Bean, *Semiconductor integrated circuit processing technology.* Addison Wesley Publishing Company, 1990.

[91] DTU Nanolab. (2023) Etch. Internal information, available upon request. Accessed: 15/07-2023. [Online]. Available: https://labadviser.nanolab.dtu.dk/index.php/LabAdviser

[92] Y. B. Castillo-Sánchez and L. A. González, "Chemically deposited pbs thin films by reaction media with glycine for use in photovoltaics," *Materials Science in Semiconductor Processing*, vol. 121, p. 105405, 2021.

[93] G. Elssner, H. Hoven, G. Kiessler, and P. Wellner, *Ceramics and ceramic composites: materialographic preparation.* Elsevier, 1999.

[94] A. S. Havreland, M. Engholm, R. S. Grass, J. Arendt Jensen, and E. V. Thomsen, "Wafer bonded cmut technology utilizing a poly-silicon-on-insulator wafer," in *2019 IEEE International Ultrasonics Symposium*, 2019, pp. 758–761.

[95] B. Asmus. how to do slag microscopy – sample lapping. Accessed: 05/07-2023. [Online]. Available: https://en.archaeometallurgie.de/slag-miscroscopy-sample-lapping/

[96] D. L. Mathine, "The integration of iii-v optoelectronics with silicon circuitry," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 3, no. 3, pp. 952–959, 1997.

[97] Z. J. Pei, G. R. Fisher, and J. Liu, "Grinding of silicon wafers: a review from historical perspectives," *International Journal of Machine Tools and Manufacture*, vol. 48, no. 12-13, pp. 1297–1307, 2008.

[98] E. E. Aktakka, R. L. Peterson, and K. Najafi, "Wafer-level integration of high-quality bulk piezoelectric ceramics on silicon," *IEEE transactions on electron devices*, vol. 60, no. 6, pp. 2022–2030, 2013.

[99] S. Bhagavat, J. C. Liberato, C. Chung, and I. Kao, "Effects of mixed abrasive grits in slurries on free abrasive machining (fam) processes," *International Journal of Machine Tools and Manufacture*, vol. 50, no. 9, pp. 843–847, 2010.

[100] U. Gosele and Q.-Y. Tong, "Semiconductor wafer bonding," *Annual Review of Materials Science*, vol. 28, no. 1, pp. 215–241, 1998.

[101] A. S. Ergun, Y. Huang, X. Zhuang, O. Oralkan, G. G. Yaralıoglu, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: Fabrication technology," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 52, no. 12, pp. 2242–2258, 2005.

[102] M. Klemm, A. Unamuno, L. ElsäSSer, and W. Jeroch, "Performance assessment of cmut arrays based on electrical impedance test results," *Journal of Microelectromechanical Systems*, vol. 24, no. 6, pp. 1848–1855, 2015.

[103] K. Technologies, *The Parametric Measurement Handbook 4th Edition*, 4th ed., Keysight Technologies, 2018.

[104] G. G. Yaralioglu, A. S. Ergun, B. Bayram, E. Haeggstrom, and B. T. Khuri-Yakub, "Calculation and measurement of electromechanical coupling coefficient of capacitive micromachined ultrasonic transducers," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 50, no. 4, pp. 449–456, 2003.

[105] J. Munir, Q. Ain, and H. J. Lee, "Reliability issue related to dielectric charging in capacitive micromachined ultrasonic transducers: A review," *Microelectronics Reliability*, vol. 92, pp. 155–167, 2019.

[106] W. R. Runyan and K. E. Bean, *Semiconductor integrated circuit processing technology*. Addison-Wesley Publishing Company, 1990.

[107] K. F. Pedersen, M. Engholm, A. S. Havreland, L. N. Moesner, C. Beers, B. G. Tomov, J. A. Jensen, and E. V. Thomsen, "384 channel modular ultrasonic cmut probe for rapid prototyping," in *2020 IEEE International Ultrasonics Symposium (IUS)*. IEEE, 2020, pp. 1–3.

[108] P. Elenius and L. Levine, "Comparing flip-chip and wire-bond interconnection technologies," *Chip Scale Review*, vol. 4, no. 6, 2000.

[109] Xyztec. Mil-std-883 method 2011.9 – bond strength (destructive bond pull test). Accessed: 21/07-2023. [Online]. Available: https://www.xyztec.com/knowledgecenter/guidelines/mil-std-883-method-2011-9-bond-strength-destructive-bond-pull-test/

[110] Silvaco, *Athena User's Maniual*, Silvaco, 2010.

[111] Silicon dioxide/nitride color vs. film thickness and viewing angle calculator. Accessed: 10/07-2023. [Online]. Available: https://cleanroom.byu.edu/color_chart

Appendices

Papers

APPENDIX A

Paper A - Accurate Radiation Impedance Analysis for CMUT Design

Accurate Radiation Impedance Analysis for CMUT Design

Stine Løvholt Grue Pedersen[1], Andreas Spandet Havreland[1], Ole Hansen[2], and Erik Vilain Thomsen[1]
[1]Department of Health Technology, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark
[2]DTU Nanolab, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark

2022 IEEE International Ultrasonics Symposium (IUS) | 978-1-6654-6657-8/22/$31.00 ©2022 IEEE | DOI: 10.1109/IUS54386.2022.9957628

***Abstract*—The transducer resonance frequency is a key parameter for the field of ultrasound. The resonance frequency in vacuum is well understood, and an analytical expression for the center frequency in immersion was derived by Lamb in 1920 [1], however this expression has limited validity. Importantly, the model fails to cover plate aspect ratios needed by imaging requirements and met by recently fabricated medical Capacitive Micromachined Ultrasonic Transducers (CMUTs). Based on the equation of motion a new expression for the resonance frequency in immersion is derived. The influence of the immersion medium is included via the radiation impedance, which is approximated using the well-known Taylor expansion, yielding results similar to Lamb's. For precision at smaller aspect ratios, this work proposes using the Padé approximant instead. Comparing the frequency ratio to FEM simulations, the Padé approximant shows a fourfold reduction in error from $12.0\,\%$ to $3.0\,\%$.**

I. Introduction

When designing Capacitive Micromachined Ultrasonic Transducers (CMUTs), FEM simulations are often used. However, these are often complicated, time consuming and do not reveal any scaling relations. For this reason precise analytic solutions are often desired and provides a good starting point for the design phase.

A key parameter for CMUTs, and the field of ultrasound in general, is the transducer center frequency in immersion. Back in 1920 Lamb [1] proposed an analytic solution for the resonance frequency in immersion of a clamped circular plate. This model assumes that the diameter of the plate is much smaller than the wavelength in the fluid, corresponding to $ka \ll 2\pi$, with k being the wavenumber and a the radius of the plate. In practice this corresponds to $ka \leq 0.5$. CMUTs found in literature has ka values ranging from 0.3 to 0.6 [2], [3] and with recent interest of $\lambda/2$-pitch [4] designed CMUTs the ka product increases up to 1.35 [5], showing the need for a more accurate solution valid for larger ka, hence even small aspect ratios.

The scope of this work is to provide a more accurate analytic expression for the resonance frequency in immersion covering the plate aspect ratios relevant for medical CMUTs. Furthermore, this work provides an alternative way to calculate the resonance frequency in immersion based on the equation of motion, where the interaction between the plate and the medium is modeled using the radiation impedance. This means that an expression for the radiation impedance is required. Since the full expression for the radiation impedance is very complicated it is only possible to solve for the resonance frequency in immersion numerically. Therefore, to provide a simple analytical solution, the radiation impedance is approximated.

II. Theory

A. Lamb's expression

The well-known theory proposed by Lamb [1] establishes the relation between the resonance frequency in immersion, ω_r, and vacuum, ω_0, for a clamped circular plate as

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1 + \Gamma_{\text{Lamb}} \frac{a}{h} \frac{\rho_m}{\rho_p}}} \tag{1}$$

where a and h are the plate radius and thickness, respectively. ρ_p is the density of the plate and ρ_m is the density of the medium. Γ_{Lamb} is a dimensionless constant that depends on the boundary conditions of the plate; for a clamped circular plate $\Gamma_{\text{Lamb}} = 0.6689$ is found. This factor is also known as the non-dimensionalized added virtual mass incremental (NAVMI) factor [6]. The exact first resonance frequency in vacuum is given by [7]

$$\omega_0 = 10.2158 \sqrt{\frac{Y}{12(1-\nu^2)\rho_p}} \frac{h}{a^2} \tag{2}$$

Here Y is Young's modulus and ν is Poisson's ratio. Knowing Y, ν and the dimensions of the CMUT plate the resonance frequency in immersion, for the case of $ka < 0.5$, can be found by combining (1) and (2).

B. The Harmonic Oscillator model

To derive an expression for the resonance frequency in immersion valid for devices with large ka we map the clamped circular plate onto a concentrated element harmonic oscillator, which has the equation of motion

$$F_{\text{ext}} = m_0 \frac{d^2x}{dt^2} + K_0 x + F_w \tag{3}$$

where F_{ext} is the total external force on the plate, x the deflection, d^2x/dt^2 the acceleration, m_0 the geometric mass, K_0 the spring constant given by $K_0 = \omega_0^2 m_0$ and F_w is the force from the fluid acting on the CMUT. This force is most easily expressed in the frequency domain, where $\hat{F}_w = Z\hat{v}_a$ is the product of the radiation impedance Z and the plate velocity $\hat{v}_a$. The equation of motion then becomes

$$\hat{F}_{\text{ext}} = -m_0\omega^2\hat{x}_m + K_0\hat{x}_m + iZ\omega\hat{x}_a \tag{4}$$

$\hat{F}_{\text{ext}}$ and $\hat{x}$ refers to the force and position in the frequency domain, respectively, which are complex numbers. Furthermore, the subscripts on $\hat{x}$ refers to the mechanic, m, and acoustic, a, domains. In order to couple between the two domains a scaling factor $\Lambda = \hat{x}_a/\hat{x}_m$ is required. This is introduced through a lumped model. Rewriting the equation of motion in (4) leads to

$$\hat{F}_{\text{ext}} = -m_0\omega^2\hat{x}_m + K_0\hat{x}_m + iZ\omega\Lambda\hat{x}_m \tag{5}$$

Resonance occurs when the real part of (5) equals zero, thus the resonance frequency in immersion can be calculated from

$$0 = m_0(\omega_0^2 - \omega_r^2) - \Im(Z)\Lambda\omega_r \tag{6}$$

showing the need of the radiation impedance, which is further described in the following subsection.

In order to couple between the mechanic and the acoustic domain a lumped model is now introduced. First the static deflection curve for a circular clamped plate is defined [7]

$$w(r) = w_0\left(1 - \left(\frac{r}{a}\right)^2\right)^2, r \leq a \tag{7}$$

where w_0 is the center deflection and r is the position along the radius.

Considering the mechanic domain, the kinetic energy for a harmonic vibrating top plate is found by integration. The dynamic velocity at distance r is

$$\hat{v}(r,t) = i\omega w(r)e^{i\omega t} \tag{8}$$

The peak kinetic energy is

$$U_{\text{kin}} = \int_0^a \frac{1}{2}\omega^2 w^2(r)\rho_p h\, 2\pi r dr \tag{9}$$

$$= \frac{1}{2}m_0\left(\frac{\omega w_0}{\sqrt{5}}\right)^2 \tag{10}$$

The lumped velocity amplitude can then be identified as $v_m = \omega w_0/\sqrt{5}$, which corresponds to a lumped position amplitude of $x_m = w_0/\sqrt{5}$.
The peak elastic potential energy with the same lumped position amplitude is given by

$$U_{\text{ela}} = \frac{1}{2}K_0 x_m^2 = \frac{1}{2}m_0\omega_0^2 x_m^2 \tag{11}$$

such that $K_0 = m_0\omega_0^2$ by definition.

Now considering the acoustic domain, the radiation impedance is a complex number that describes the "back action" on the transducer through the imaginary part, while the real part describes the radiated power. The radiation impedance is calculated based on the volume velocity, V, of the radiating CMUT. The volume velocity is

$$V = \int_0^a \dot{w}(r)\, 2\pi r dr = \pi a^2\langle\dot{w}(r)\rangle \tag{12}$$

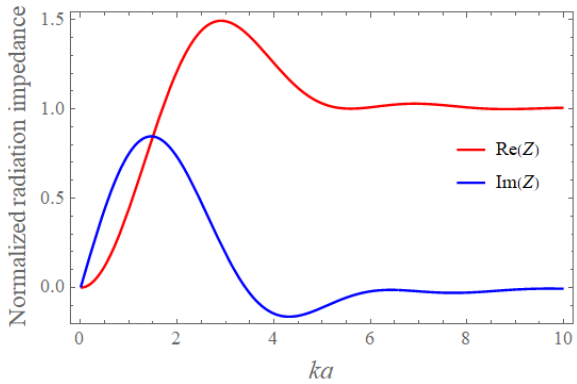


Fig. 1. The normalized radiation impedance (15) showing the real and imaginary part in a large interval for the wavenumber-radius product, ka.

where $\langle\dot{w}(r)\rangle$ is the area average velocity. The lumped position amplitude in the acoustic domain to be used in connection with the radiation impedance is thus

$$x_a = \langle w(r)\rangle = \int_0^a w(r)\, 2\pi r dr \Big/ \int_0^a 2\pi r dr = \frac{w_0}{3} \tag{13}$$

In summary, the lumped position amplitudes are $x_m = w_0/\sqrt{5}$ and $x_a = w_0/3$ for the mechanic and acoustic domains, respectively. The scaling factor needed when transforming from one domain to the other then becomes

$$\Lambda = \frac{x_a}{x_m} = \frac{\sqrt{5}}{3} = 0.745356 \tag{14}$$

which can be used for both the position and the velocity based on the harmonic assumption. Now having found the scaling parameter, Λ, the resonance frequency can be calculated from (6).

C. Radiation impedance

The radiation impedance for a clamped circular plate is derived in [8] and expressed in terms of a hypergeometric function the expression becomes

$$\begin{aligned} Z_{\text{plate}} = \Bigg(& \frac{1}{(ka)^5}(12(-3 + 2(ka)^2)J_1(2ka) \\ & + ka(36 + (ka)^4 - 84J_2(2ka))) \\ & + i\frac{512ka}{175\pi}\,{}_2F_3\left(2, \frac{5}{2}; \frac{3}{2}, \frac{7}{2}, \frac{9}{2}; -(ka)^2\right)\Bigg)\rho_m c_m \pi a^2 \end{aligned} \tag{15}$$

where c_m is speed of sound in the medium. J_1 and J_2 are Bessel functions of first and second order and ${}_2F_3$ is a hypergeometric function. The exact normalized radiation impedance is shown in Figure 1 for the real and the imaginary part. The normalized radiation impedance is plotted as function of ka, which is the wavenumber-radius product. For large ka values the radiation resistance approaches the constant used for normalization; $\rho_m c_m \pi a^2$, while the radiation reactance asymptotic approaches zero.
Now combining (6) and (15) the resonance frequency can be solved numerically for any CMUT design. However, to

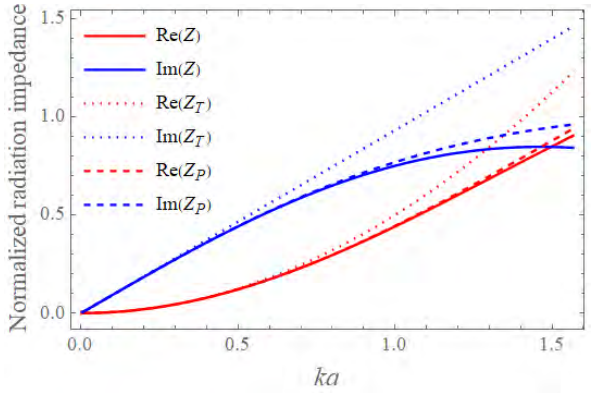


Fig. 2. Showing the full expression for the radiation impedance together with the Taylor and Padé approximations in the interval relevant for medical CMUTs.

obtain an analytical expression for the resonance frequency in immersion an approximation for the radiation impedance is needed. For small ka the Taylor expansion of (15) can be used. The real part then becomes

$$\Re(Z_{\text{Taylor}}) = \frac{1}{2}a^2 c_m (ka)^2 \pi \rho_m + O(ka)^3 \tag{16}$$

and the imaginary part becomes

$$\Im(Z_{\text{Taylor}}) = \frac{512}{175}a^2 c_m ka \rho_m + O(ka)^3 \tag{17}$$

Notice, that the reactance is linear for small ka while the resistance is parabolic. The results are shown in Figure 2. It is seen that the approximation is only useful for $ka < 0.4$ for the imaginary part and $ka < 0.5$ for the real part.

Due to increasing interest for $\lambda/2$-pitch transducers the ka product increases, which requires an alternative method also valid for $ka > 0.5$. For this purpose the Padé approximant [9] is used to the simplest order, hence (2,2), which is a rational function. Applying the Padé approximation on (15) the real part becomes

$$\Re(Z_{\text{Pade}}) = \frac{a^2 c_m (ka)^2 \pi \rho_m}{2\left(1 + \frac{(ka)^2}{8}\right)} + O(ka)^5 \tag{18}$$

and the imaginary part becomes

$$\Im(Z_{\text{Pade}}) = \frac{512 a^2 c_m ka \rho_m}{175\left(1 + \frac{40(ka)^2}{189}\right)} + O(ka)^5 \tag{19}$$

Notice, the results found by the Padé approximant is the same as the Taylor results multiplied by a correction factor.
From Figure 2 it is seen that the Padé approximation is valid for ka values up till $ka = 1.0$ for the imaginary part, while it is valid $ka = 1.4$ for the real part. The error between the exact solution and the second order Taylor expansion for $ka = 1.0$ is $24\,\%$ while for the simplest possible Padé approximant the error is $2.5\,\%$. Thus, the Padé approximation provides a better approximation for the normalized radiation impedance compared to the Taylor expansion for $ka > 0.4$, which allows a more simple expression for the resonance frequency in immersion. Another strength of the Padé approximant is that it is physically correct, meaning that for large ka values the real part approaches a constant and the imaginary part goes towards zero in a similar way as the full radiation impedance expression. In comparison the Taylor expansion will always, independent on approximation order, diverge to either plus or minus infinity for large ka values, which is not physically correct.

D. Resonance frequency in immersion

To verify the derivation method using the harmonic oscillator model together with the radiation impedance, the Taylor expansion in (16) and (17) are combined with (6) resulting in an expression for the ratio between the resonance frequency in immersion and vacuum (using $k = \omega_r/c_m$)

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1 + \Gamma_{\text{Taylor}} \frac{a}{h} \frac{\rho_m}{\rho_p}}} \tag{20}$$

where $\Gamma_{\text{Taylor}} = \frac{512}{175\pi}\Lambda$ is the NAVMI factor. This equation has the same form as the well-known expression provided by Lamb in (1). The NAVMI factor is slightly different from $\Gamma_{\text{Lamb}} = 0.6689$ to $\Gamma_{\text{Taylor}} = 0.6941$. This verifies the derivation method.
In order to cover a wider range of ka values relevant for medical CMUTs, the Padé approximation in (18) and (19) are used for the radiation impedance. Solving (6) for the resonance frequency in immersion and using that $k = \omega_r/c_m$ gives

$$\frac{\omega_r^2}{\omega_0^2} = -\frac{c_1 - \sqrt{c_1^2 + 4c_2}}{2c_2} \tag{21}$$

with

$$c_2 = \frac{40\,(k_0 a)^2}{189} = \frac{40\,(\omega_0 a/c_m)^2}{189} \tag{22}$$

$$c_1 = 1 + \Gamma_{\text{Taylor}} \frac{a\rho_m}{h\rho_p} - c_2 \tag{23}$$

This is the analytical expression for the resonance frequency in immersion using the Padé approximant we set out to derive.

III. FEM ANALYSIS

Finite Element Model (FEM) simulations have been made using the program OnScale (Ansys). The simulated structure is a simple CMUT cell, shown in Figure 3. The structure consist of a bottom substrate and a flexible top plate both of silicon. In-between a layer of insulating silicon oxide and a vacuum cavity is found. The top plate is fixed at the edge of the cavity indicated by a vertical line. Furthermore, the simulations are conducted in both vacuum and water having an absorbing boundary away from the CMUT. This is shown as a black horizontal line in the figure. The axis of rotational symmetry is indicated with a dashed line. The cell radius and the plate thickness have been varied to obtain different aspect

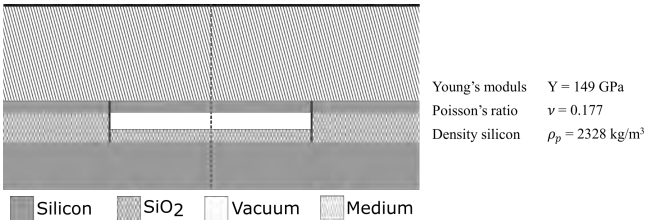


Fig. 3. Structural outline for a simple 2D CMUT model used in the FEM simulation together with the material parameters used. The structure consist of two silicon plates with an insulating silicon oxide and a vacuum gap in-between. The fixed boundary is marked as well as the absorbing boundary at the far end of the medium. The axis of rotational symmetry is shown with a dashed line.

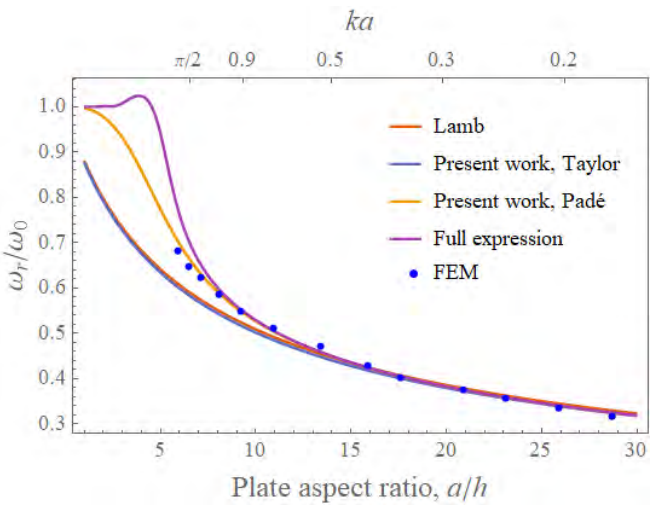


Fig. 4. The analytic solution shown together with the solutions derived using the Taylor and Padé approximations as alternative to the radiation impedance. The FEM data are also shown as well as the full numeric solution.

ratios, a/h. Accordingly the vacuum gap has been adjusted to keep a constant pull-in voltage of 220 V. The simulations were performed without bias to find the natural resonance frequency. The results from the FEM simulations are shown in Figure 4 together with the well-known Lamb model, the one derived using a Taylor expansion and one found from the Padé approximation of the radiation impedance. The full numeric solution is also shown. The results are shown as function of both the plate aspect ratio a/h and the wavenumber-radius product, ka, where ka was calculated numerically accepting the Padé approximation for the resonant frequency.

IV. Discussion

As seen from both the equations ((1) and (20)) and Figure 4 the model derived using the Taylor expansion is almost exactly the same as the expression given by Lamb [1]. Comparing to the solution derived using the Padé approximation they give the same result for large plate aspect ratios, hence small ka values. However, for plate aspect ratios below ≈ 13 the models start to deviate. The FEM data show that the Padé model correctly predicts the increase in relative resonance frequency for small aspect ratios. Thus, this model covers a larger range of the plate parameters relevant for medical CMUTs. Comparing the Taylor and the Padé model for $a/h = 10.9$ the error between the FEM data and the Taylor is $4.1\,\%$, while for the Padé it is $1.5\,\%$. Looking at $a/h = 5.9$ instead, the error between the FEM data and the Taylor model is $12.0\,\%$, while the Padé only has an error of $3.0\,\%$. This confirms that the Padé model covers a larger range of CMUT designs with aspect ratios down to $a/h = 5$. The full solution actually overestimates the resonance frequency relation at small aspect ratios, where shear deformation becomes important.

V. Conclusion

This paper presents an alternative way to derive an analytic expression for the resonance frequency in immersion based on the equation of motion and the radiation impedance. The radiation impedance is approximated using a Taylor expansion verifying the method against Lambs expression [1]. Compared to the full expression for the radiation impedance this solution gives an error of $24\,\%$ for $ka = 1.0$. Furthermore, it is shown that by using the Padé approximant as a more accurate approximation to the radiation impedance gives an error of $2.5\,\%$ for $ka = 1.0$.

Comparing the two derived models for the resonance frequency in immersion to FEM data simulated in OnScale the error is reduced from $12.0\,\%$ using the resonance frequency found using the Taylor expansion to $3.0\,\%$ using the Padé model. Thus, it can be concluded that a more accurate model using the radiation impedance to derive the resonance frequency in immersion have been found for CMUTs giving a great starting point for the design phase.

Acknowledgment

This work is supported by the European Research Council's (ERC) Synergy Grant 854796.

References

[1] H. Lamb, "On the vibrations of an elastic plate in contact with water," *Proceedings of the royal society of London. Series A, containing papers of a mathematical and physical character*, vol. 98, no. 690, pp. 205–216, 1920.

[2] Y. Huang, A. S. Ergun, E. Haeggstrom, M. H. Badi, and B. T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology," *Journal of microelectromechanical systems*, vol. 12, no. 2, pp. 128–137, 2003.

[3] S. E. Diederichsen, "Micromachined integrated transducers for ultrasound imaging," Ph.D. dissertation, Technical University of Denmark, 2019.

[4] J. Jensen, M. B. Stuart, and J. A. Jensen, "Optimized plane wave imaging for fast and high-quality ultrasound imaging," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 63, no. 11, pp. 1922–1934, 2016.

[5] S. E. Diederichsen, J. M. F. Hansen, M. Engholm, E. V. Thomsen *et al.*, "Output pressure and pulse-echo characteristics of cmuts as function of plate dimensions," in *2017 IEEE International Ultrasonics Symposium (IUS)*. IEEE, 2017, pp. 1–4.

[6] M. Kwak, "Vibration of circular plates in contact with water," 1991.

[7] E. Ventsel and T. Krauthammer, *Thin Plates & Shells: Theory, Analysis, & Applications*, 1st ed. CRC Press, Aug. 2001.

[8] M. Greenspan, "Piston radiator: Some extensions of the theory," *The Journal of the Acoustical Society of America*, vol. 65, no. 3, pp. 608–621, 1979.

[9] C. M. Bender, S. Orszag, and S. A. Orszag, *Advanced mathematical methods for scientists and engineers I: Asymptotic methods and perturbation theory*. Springer Science & Business Media, 1999, vol. 1.

APPENDIX B

Paper B - Electrical Insulation of CMUT Elements Using DREM and Lapping

Electrical Insulation of CMUT Elements Using DREM and Lapping

Stine Løvholt Grue, Mathias Engholm and Erik Vilain Thomsen
Department of Health Technology, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark

***Abstract*—This paper demonstrates a novel fabrication process to implement a capacitive micromachined ultrasound transducer (CMUT) into a laparoscope. Due to the limited space in the laparoscope, a new method for electrically contacting the transducer elements is required. Using a state-of-the-art high aspect ratio dry etching process called Deposit, Remove, Etch, Multistep (DREM), it is possible to separate the bottom electrodes and use a common grounded top electrode, which allows for back side contacting of the device and mitigates the use of wire-bonds and external electromagnetic interference shielding to thereby reduce the footprint. DREM trenches that are 6.7 µm wide and approximately 143 µm deep have been etched into the substrate. The trenches are insulated using a thermally grown dry oxide before they are plugged through deposition of a high uniformity poly-silicon layer. To finalize the structure, the excess substrate is removed from the back side of the wafer until the bottom of the trenches are reached, and the elements become completely separated. This is done using lapping followed by polishing to reduce the surface roughness.**

I. Introduction

A laparoscope can guide the surgeon during surgery while minimizing the harm on the patient. Implementation of an ultrasound transducer into the laparoscope can be utilised to visualise internal body structures, for instance liver metastases. Using a laparoscope reduces the required penetration depth of the transducer. Thus, a high frequency transducer can be used to achieve high resolution images of deep lying organs without requiring a large penetration depth. It has been shown that a $\lambda/2$-pitch between transducer elements is beneficial as it reduces the grating lobes artifacts in the ultrasonic image [1]. When fabricating a high frequency transducer the dimensions therefore downsize accordingly. For this reason, capacitive micromachined ultrasound transducers (CMUTs) are a suitable choice since the fabrication is based on micro- and nano-fabrication. Thus, the cell width is not limited by the dimensions of a saw blade which is the case for conventional piezo-based transducers. Miniaturisation of the elements is not only necessary to create a high frequency transducer fullfilling the $\lambda/2$-pitch requirement, but it is also needed for the implementation in the laparoscope. Based on the limited space in a laparoscope it is desired to have the bottom electrodes separated and to have a common top electrode connected to ground. This allows for a smaller footprint compared to conventional methods of having a common bottom electrode and separated top electrodes, as it eliminates the need for wire-bonds and external electromagnetic interference shielding. In the literature, back side contacting of CMUTs has been shown feasible using through-silicon vias filled with poly-silicon or using air-filled trenches as insulation [2], [3].

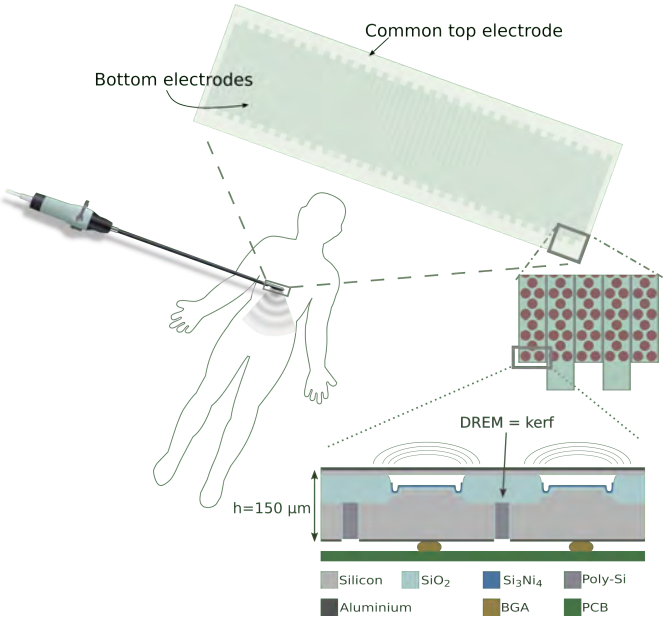


Fig. 1. A conceptual overview of the end goal of the project: a CMUT based ultrasound transducer implemented into a laparoscope. An overview of the array, elements and cell structure is given.

This work demonstrates a novel fabrication process that allows for element insulation using a dry etch with aspect ratios of more than 1:50. This ratio is feasible due to the high etch selectivity towards conventional photoresist. The process is called Deposit, Remove, Etch, Multistep (DREM) and is based on Reactive Ion Etching (RIE) [4]. Furthermore, it allows for integration using the substrate as a via architecture and contact point for ball grid array bonding. This bonding technique mitigates parasitic contributions from wire-bonds and is suitable for large scale production. A conceptual overview of the integration of the CMUT based probe into a laparoscope is shown in Fig. 1.

II. Fabrication

A. Process flow of the element separation

The CMUT fabrication is based on a local oxidation of silicon (LOCOS) process [5]. The bottom electrodes are separated using the dry etch method optimized for high aspect ratio trenches, DREM. The elements are insulated from one-another by a thin oxide and the trenches are filled with poly-silicon.

978-1-7281-5448-0/20/$31.00 © 2020 IEEE

The trenches need to be plugged to ensure mechanical stability of the substrate throughout the remaining processing. A cross section of the final structure is shown in Fig. 1. The element separation and insulation process is illustrated in Fig. 2 and consists of six main steps. The process proceeds as follows: a) conventional photolithography is used to define the width of the DREM trenches, which is designed to be 5.0 µm. Trenches with a depth of approximately 143 µm are etched into the silicon substrate using the DREM process. The process parameters are further discussed in section II-B. b) After etching the trenches, the resist is stripped in a plasma leaving only the silicon substrate. The corners of the trenches are rounded by growing a 500 nm thick wet thermal oxide at 1100 °C. This oxidation also decreases the scallop depth caused by the Bosch based DREM process [6]. c) The SiO_2 is subsequently removed using BHF with a wetting agent to enable etching of high aspect ratio structures. d) The next step is to thermally grow a 200 nm thick insulating dry oxide at 1100 °C. This is designed to withstand the applied voltages, thus avoiding breakdown. e) The trenches are then plugged using undoped poly-silicon. After finalising the fabrication of the plugged DREM trenches, the CMUTs can be fabricated using a LOCOS process similar to the one used in [5]. Hereafter, the substrate is fusion bonded to an SOI wafer, that acts as both mechanical support throughout subsequent processing and eventually as the CMUT top plate. These steps are not included in Fig. 2. f) The back side of the substrate is thinned down until the elements are visibly separated. The substrate thinning is done by removing 375 µm of bulk silicon in a lapping process. One should be aware that Fig. 2 is not to scale, hence the trenches are only etched approximately 1/5 into the wafer. A polishing step is subsequently introduced to lower the surface roughness. In this process, the surface roughness can be reduced from 318 nm to 1.4 nm. Lastly, the SOI wafer is thinned down, leaving only the device layer, on which the top metal contact can be added, forming the flexible top plate for the CMUTs.

B. The DREM process

The development of the high aspect ratio dry etch, DREM, facilitates separation of the bottom electrodes for back side contacting without increasing the kerf [4]. The process is based on RIE and the Bosch process. An overview of the gas flow, the platen power and the process time in the three main steps is illustrated in Fig. 3. Throughout processing, the chuck temperature should be the smallest value allowed by the equipment, here −19 °C. In the *deposition* step, the platen power is minimized to avoid erosion. A C_4F_8 plasma is used to deposit a fluorocarbon (FC) passivation layer. The deposition takes 2.8 s. In the *remove* step, the FC passivation layer is removed at the bottom of the trench. The remove step takes 2.5 s in total. A low pressure (5 mTorr) Argon plasma is used with a bias power of 75 W with 325 V DC for 1.6 s to clear the FC passivation layer in the bottom of the trenches. Finally, in the *etch* step, an SF_6 based plasma is used. The gas flow is increased to 600 sccm during the etch step. The total processing time is 36 min and 10 sec, which includes 308 cycles. The *etch* time is gradually increased from 2.5 s to 6 s which results in similar scallop sizes along the entire trench.

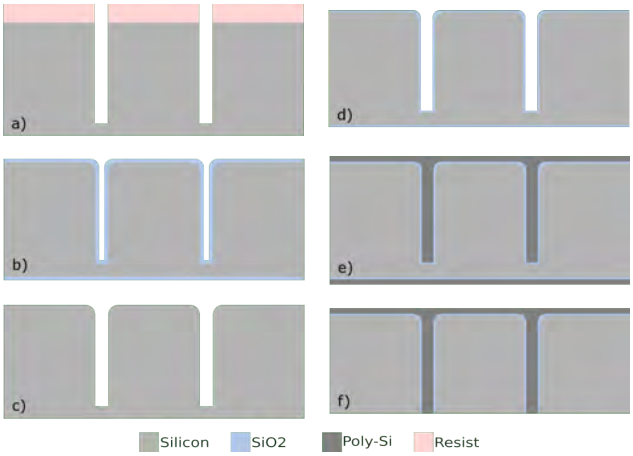


Fig. 2. Overview of the fabrication of the trenches insulating the elements using oxide and poly-silicon plugs. Be aware that the figure is not to scale and the trenches are only etched approximately 1/5 into the bulk substrate.

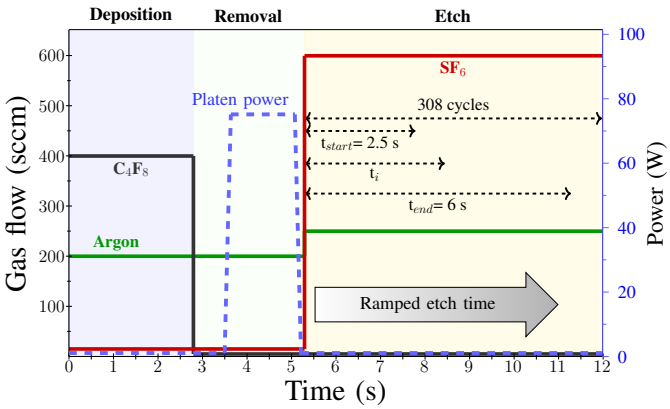
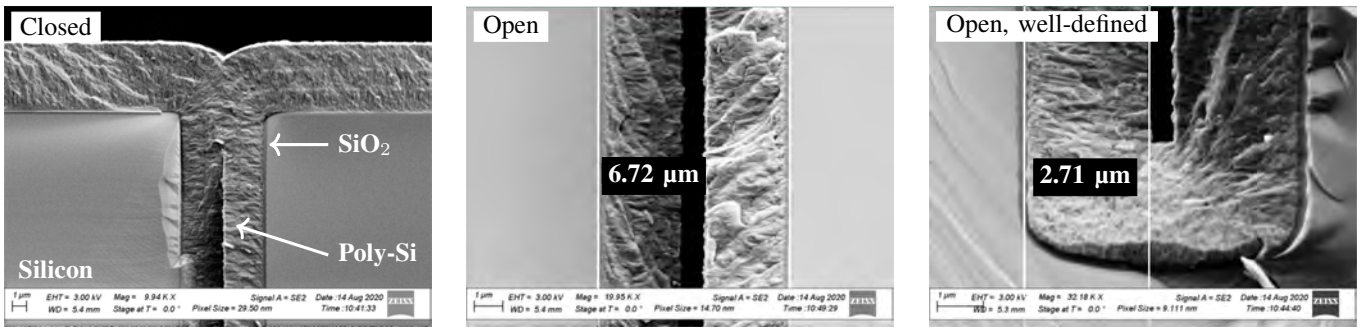


Fig. 3. Overview of DREM parameters in the three individual steps; Deposit, Remove, Etch.

III. Results

Fig. 4 shows three SEM images of a trench, one of the top, one of the middle, and one of the bottom, respectively. A full trench is visualised in Fig. 5. Table I shows measurements of the trench width, thickness of the oxide and thickness of the poly-silicon measured at three locations along the trench; the top, the middle, and the bottom, corresponding to the images in Fig. 4.

The width of the trenches is designed to be 5.0 µm in the photolithography process (Fig. 2a). During both the first oxidation to round the corners and smoothen the scallops from the DREM process (Fig. 2b), and the second oxidation to grow an insulating oxide (Fig. 2d), 44% of the oxide thickness is grown in the silicon [7], thus widening the trench. In theory



(a) (b) (c)

Fig. 4. SEM images of the trench with an insulating oxide and deposited poly-silicon. The images show a) the top, b) the middle, and c) the bottom of the trench.

the trench should be 5.66 µm wide. However, in Fig. 4b it can be seen that the trench is measured to be around 6.7 µm, which is 18.4% wider than expected. This must be due to the etch process etching scallops wider than what is defined by the resist mask. The depth of the trench is measured to be 143.0 µm. Furthermore, Fig. 4 shows that the top of the trench is plugged before the bottom and middle part of the trench is filled. This results in a structure that is not mechanical stable as desired, since the elements are not physically connected throughout the trench. A suggestion on how to solve the problem with the top of the trench closing before the remaining of the trench is filled, is to decrease or even remove the gradually increased etch time in the DREM process. This will create a tapered etch profile which together with additional corner rounding is expected to result in a trench that plugs from the bottom of the trench towards the top of the trench. This will ensure mechanical stability which is needed for subsequent processing.

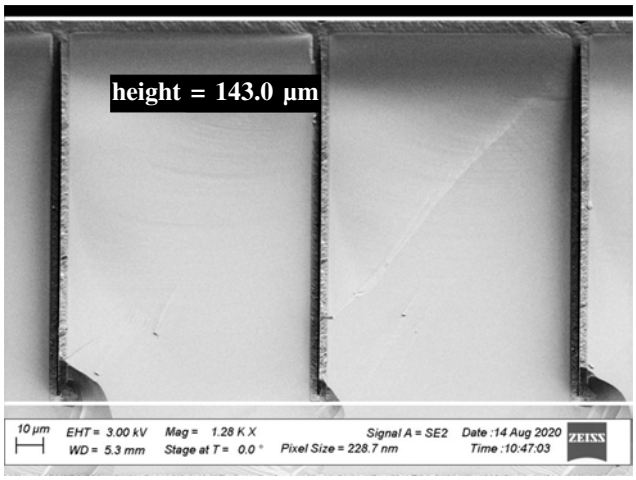


Fig. 5. SEM image showing a full trench with insulating oxide and deposited poly-silicon. The trench depth is measured to be 143.0 µm.

	Trench width	Silicon oxide thickness	Poly-silicon thickness
Top	6.70 µm	-	2.82 µm
Middle	6.72 µm	195 nm	2.71 µm
Bottom	6.34 µm	228 nm	2.71 µm

TABLE I
MEASUREMENTS OF THE TRENCH WIDTH, THICKNESS OF THE INSULATING OXIDE AND THICKNESS OF THE DEPOSITED POLY-SILICON.

IV. CONCLUSION

Successful fabrication of the insulated electrode design has been presented by forming insulated vias in the substrate. The trenches have been etched using an etching technique, DREM, that allows for a high aspect ratio, creating trenches with a width of 6.7 µm and a depth of 143.0 µm. An insulating oxide has successfully been grown and poly-silicon with a thickness varying from 2.71 µm to 2.82 µm has been deposited in an attempt to plug the trenches. The top of the trench was plugged before the bottom and the middle part of the trench was completely filled, which obstructed the trench filling, leaving a structure which is not mechanically stable.

Further studies will include to change the etch recipe/etch cycles so the profile becomes tapered. This will enable the bottom part of the trench to fill before the top of the trench closes. An alternative solution would be to modify the corner rounding procedure to mitigate this problem. The next step is to implement the LOCOS defined CMUT cells on a substrate with isolated and plugged elements.

REFERENCES

[1] J. Jensen, M. B. Stuart, and J. A. Jensen, "Optimized Plane Wave Imaging for Fast and High-Quality Ultrasound Imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 11, pp. 1922–1934, 2016.

[2] J. Due-Hansen, K. Midtbo, E. Poppe, A. Summanwar, G. U. Jensen, L. Breivik, D. T. Wang, and K. Schjølberg-Henriksen, "Fabrication process for CMUT arrays with polysilicon electrodes, nanometre precision cavity gaps and through-silicon vias," *Journal of Micromechanics and Microengineering*, vol. 22, no. 7, 2012.

[3] X. Zhuang, A. S. Ergun, Y. Huang, I. O. Wygant, O. Oralkan, and B. T. Khuri-Yakub, "Integration of trench-isolated through-wafer interconnects with 2d capacitive micromachined ultrasonic transducer arrays," *Sensors and Actuators, A: Physical*, vol. 138, no. 1, pp. 221–229, 2007.

[4] B. Chang, P. Leussink, F. Jensen, J. Hübner, and H. Jansen, "DREM: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed Bosch DRIE process," *Microelectronic Engineering*, vol. 191, pp. 77–83, 2018. [Online]. Available: https://doi.org/10.1016/j.mee.2018.01.034

[5] K. K. Park, H. Lee, M. Kupnik, and B. T. Khuri-Yakub, "Fabrication of capacitive micromachined ultrasonic transducers via local oxidation and direct wafer bonding," *Journal of Microelectromechanical Systems*, vol. 20, no. 1, pp. 95–103, 2011.

[6] Z. A. Syed Mohammed, M. A. Olimpo, D. P. Poenar, and S. Aditya, "Smoothening of scalloped DRIE trench walls," *Materials Science in Semiconductor Processing*, vol. 63, no. January, pp. 83–89, 2017. [Online]. Available: http://dx.doi.org/10.1016/j.mssp.2017.02.006

[7] *Semiconductor Devices*, 3rd ed. John Wiley & Sons, 2013, pp. 395-400.

APPENDIX C

Paper C - A Hand-Held 190+190 Row-Column Addressed CMUT Probe for Volumetric Imaging

IEEE Open Journal of Ultrasonics, Ferroelectrics, and Frequency Control

Received 23 May 2022; revised 18 August 2022; accepted 1 October 2022.
Date of publication 10 October 2022; date of current version 28 October 2022.

Digital Object Identifier 10.1109/OJUFFC.2022.3213013

A Hand-Held 190+190 Row–Column Addressed CMUT Probe for Volumetric Imaging

RUNE SIXTEN GRASS[1], (Member, IEEE), MATHIAS ENGHOLM[1], ANDREAS SPANDET HAVRELAND[1], CHRISTOPHER BEERS[2], (Member, IEEE), MARTIN LIND OMMEN[1], STINE LØVHOLT GRUE PEDERSEN[1], (Graduate Student Member, IEEE), LARS NORDAHL MOESNER[3], MATTHIAS BO STUART[1], MUDABBIR TUFAIL BHATTI[1], (Student Member, IEEE), BORISLAV G. TOMOV[1], JØRGEN ARENDT JENSEN[1], (Fellow, IEEE), AND ERIK VILAIN THOMSEN[1], (Member, IEEE)

[1]Department of Health Technology, Technical University of Denmark, 2800 Lyngby, Denmark
[2]BK Medical, State College, PA 16801 USA
[3]BK Medical, 2730 Herlev, Denmark

CORRESPONDING AUTHOR: R. S. GRASS (rungra@dtu.dk)

This work was supported by the European Research Council Synergy Grant ERC 854796.

ABSTRACT This paper presents the design, fabrication, and characterization of a 190+190 row-column addressed (RCA) capacitive micromachined ultrasonic transducer (CMUT) array integrated in a custom hand-held probe handle. The array has a designed 4.5 MHz center frequency in immersion and a pitch of 95 μ m which corresponds to $\approx \lambda/4$. The array has a 2.14 $\times$ 2.14 cm^2 footprint including an integrated apodization scheme to reduce ghost echoes when performing ultrasound imaging. The array was fabricated using a combination of fusion and anodic bonding, and a deposit, remove, etch, multistep (DREM) etch to reduce substrate coupling and improve electrode conductivity. The transducer array was wire-bonded to a rigid-flex printed circuit board (PCB), encapsulated in room temperature vulcanizing (RTV) silicone polymer, electromagnetic interference (EMI) shielded, and mounted in a 3D-milled PPSU probe handle. The probe was characterized using the SARUS experimental scanner and 3D volumetric imaging was demonstrated on scatter and wire phantoms. The imaging depth was derived from tissue mimicking phantom measurements (0.5 dB MHz^{-1} cm^{-1} attenuation) by estimating the SNR at varying depths. For a synthetic aperture imaging sequence with 96+96 emissions the imaging depth was 3.6 cm. The center frequency measured from the impulse response spectra in transmit and pulse-echo was 6.0 $\pm$ 0.9 MHz and 5.3 $\pm$ 0.4 MHz, and the corresponding relative bandwidths were 62.8 $\pm$ 4.5 % and 86.2 $\pm$ 10.4 %. The fabrication process showed clear improvement in relative receive sensitivity and transmit pressure uniformity compared to earlier silicon-on-insulator (SOI) based designs. However, at the same time it presented yield problems resulting in only around 55 % elements with a good response.

INDEX TERMS Ultrasonic transducers, ultrasonic transducer arrays, electric resistance, probes, ultrasonic imaging, fabrication, microfabrication, silicon, wafer bonding, glass.

I. INTRODUCTION

IN the recent years, there has been a growing interest in developing 2D ultrasonic transducer arrays for performing 3D volumetric imaging with resolution comparable to conventional 2D imaging made with linear 1D arrays.

For good focusing and high resolution 3D ultrasound imaging a large probe with a significant number of elements, N, is needed. 2D arrays with elements in both the azimuthal and elevation direction are typically fabricated as fully populated matrix (FPM) arrays, where the number of elements and therefore also the number of individual connections each scale with N^2. A linear probe might have 190 elements, which for a matrix array having the same resolution in both directions would result in 190 $\times$ 190 = 36,100 connections. This

would require highly impractical bulky cables connecting the probe to the scanner in addition to electronics capable of handling the data rates, which would be several terabytes per second for such an array.

The focusing ability of ultrasound probes is proportional to the wavelength and the ratio of the imaging depth to the width of the probe. The width is equal to the pitch times the number of elements N. Maintaining the same resolution in both dimensions necessitates the same number of elements, hence N^2 connectors. Also maintaining a good resolution demands large probes to maintain the ratio between depth and width.

State-of-the-art FPM array probes based on lead zirconium titanate (PZT) crystal materials can already be acquired commercially from e.g., Philips (X6-1 xMATRIX array transducer with 9212 elements) and for research solutions through Verasonics (Matrix Array Transducer with 1024 elements (32×32)). To achieve a higher channel count an effort has been made to design electronics performing pre-beamforming that fit inside the probe handle [1], [2], [3], which has also been made possible in the Philips X6-1 xMATRIX probe. Integrated electronics and the use of PZT materials, however, still have problems concerning probe heating under continuous use [4], [5].

A. ROW-COLUMN ARRAYS

Recently, a new type of array scheme has been developed which can reduce the number of channels needed for imaging and keep the same array footprint without resorting to e.g., using sparse arrays [6], [7]. This is the so-called row-column addressed (RCA) array which was proposed by Morton and Lockwood in 2003 [8] and reiterated by Démoré et al. in 2009 [9]. An RCA transducer is composed of two 1D arrays placed orthogonal to each other, with sub-elements in overlapping segments. Imaging sequences are likewise different, in the sense that instead of actuating each single sub-element and selecting sub apertures in the matrix array, entire row or column elements encompassing potentially hundred of sound emitting sub-elements are excited simultaneously. Row or column elements are used for transmitting a line focus, while the orthogonal elements are grounded. For receiving, opposite elements are often used to focus in a perpendicular line while the previously transmitting elements are grounded. This creates a focus point in the volume where the two lines overlap, which can be used for volumetric imaging. Since only $2 \times N$ elements are used this significantly reduces the number of connections needed. Morton and Lockwood [8] state that beamforming two perpendicular planes with an RCA array results in a loss of signal strength compared to an $N \times N$ FPM array, and that $4 \times N$ elements are needed to get a comparable resolution. It has, however, been shown by Rasmussen and Jensen [10] that RCA arrays always have a higher resolution than FPM arrays for the same number of matrix elements ($32 + 32$ rows and columns compared to 8×8 matrix elements). More details about the imaging abilities of RCA arrays can be found in [11].

Row-column arrays have been fabricated using PZT or other piezoelectric materials, including a 1-3 ceramic RCA 64×64 array [12], an RCA 256×256 array [13], and a 7.5 MHz dual-layer transducer with 256 PZT elements used for transmit combined with 256 orthogonal P[VDF-TrFE] copolymer elements for receive [14]. An alternative version of the row-column scheme named top-orthogonal-to-bottom electrode (TOBE) using an electrostrictive ceramic PNM-PT was presented in [15]. Recently, a 62+62 PZT row-column array integrated in a hand-held probe was demonstrated [16]. Commercial row-column probes using PZT are available from Vermon and Verasonics (RC6gV Row-Column Array Transducer), using 128+128 rows and columns with a 6 MHz center frequency. A similar prototype probe with 128+128 rows and columns with a 12 MHz center frequency was introduced by Daxsonics.

PZT probes are often fabricated using the dice-and-fill method [17], where the kerf is limited by the width of the dicing blade to around 15 μm [18]. This imposes restrictions on the transducer design, especially at higher frequencies where the element width becomes comparable to the kerf for small pitch probes. Furthermore, high frequency probes require a small thickness of the PZT material, which makes such probes increasingly difficult to fabricate. Therefore, alternatives to fabricating probes using PZT are needed.

B. CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

One alternative to the piezoelectric transducer is the capacitive micromachined ultrasonic transducer (CMUT) based on silicon microfabrication. It was first demonstrated using sacrificial release methods [19], and later with fusion bonding (also called direct bonding) [20]. This structure uses a thin vibrating plate or membrane for transmit and receive. CMUTs, when compared to conventional PZT based transducers, do not have any significant self-heating due to low internal loss and high thermal conductivity [21], [22] and also provides higher frequency bandwidth [23]. These transducers can be made with microfabrication and the single CMUT units, referred to as cells, can be defined through the use of simple lithographic processes. The devices can therefore be made smaller, and the pitch can more easily be controlled than what is usually possible with dicing for piezoelectric transducers. This allows a pitch of $\lambda/2$, which minimises grating lobes [24], to be more easily kept for higher center frequencies, and easier integration with integrated circuits on chip.

Since the first use for imaging [25] CMUTs have been successfully used for 1D linear array probes by several academic and industrial research groups [23], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35] and more recently such probes have become commercially available. The first 2D array using CMUTs based on the row-column addressing scheme had 32+32 elements fabricated using wafer fusion bonding, where the cavities and membranes were both made with silicon nitride. Since then several row-column CMUTs

have been designed and fabricated with a variety of different methods, such as sacrificial release [36], [37] using a TOBE array architecture, adhesive wafer bonding [38], [39], fusion bonding [16], [40], [41], [42], [43] and anodic bonding [44], [45], [46]. Some of these arrays have been integrated in hand-held probes, presented in [16] as a 62+62 RCA 2D CMUT probe together with a corresponding PZT probe for comparison, and in [43] where two 92+92 RCA 2D CMUT probes with and without integrated diverging lenses are presented. These probes showed the potential for using CMUTs for RCA arrays and demonstrated that such probes can attain similar performances as a PZT probe made using the same dimensions. However, it was found that capacitive substrate coupling [47] and the resistance of the electrodes [48] used for the CMUT devices is important for the performance of large CMUT arrays and needs to be optimized.

C. REQUIREMENTS FOR LARGE ARRAY DESIGNS

When designing large RCA arrays there are a number of important criteria to ensure optimal performance. The pressure emitted along each element, rows and columns, and across neighbouring elements should be uniform. If this is not the case, the pressure field of the array when performing imaging will not match simulated fields and can be detrimental to the image quality. Likewise, the receive sensitivity of both rows and columns should be equal to ensure even performance.

Considering the first requirement, the distribution of the electric potential along the CMUT elements becomes important. When a high frequency excitation (AC) signal is applied on a long element the electrode resistance can have significant influence on the transmit pressure uniformity. If the resistance is too high the system will behave as a low-pass filter and attenuate the applied signal along the element. This effect can be modelled as a delay line [48]. The value of the dimensionless product ωRC, being a combination of the angular excitation frequency, ω, the element electrode resistance, R, and the total capacitance of the element, C, can be used as a criterion to minimise adverse attenuation. To keep a uniform pressure distribution, the potential drop along the element is set to a maximum of 1 %. This corresponds to an ωRC value of

$$\omega RC \leq 0.35. \tag{1}$$

This can also be expressed in terms of the sheet resistance, $R_{\square}$, the element or electrode length, L, and the capacitance per area, C'

$$\omega R_{\square} C' L^2 \leq 0.35. \tag{2}$$

This allows one to predict the signal drop and adjust the design parameters without the need to directly measure the electrode resistance. It furthermore shows that the choice of $R_{\square} = \rho/t$, which depends on the electrode resistivity, ρ, and thickness, t, becomes much more crucial for larger arrays as the effect scales with the area, L^2.

The second requirement regarding the sensitivity depends on how well the substrate coupling or cross-talk between elements [47] can be suppressed. CMUT elements which are fabricated with a silicon substrate often utilise a silicon-on-insulator (SOI) wafer during fabrication with an insulating layer to separate bottom electrodes from the handling substrate [36], [41], [49], [50]. This allows the elements to capacitively couple to each other through the substrate, giving rise to parasitic capacitance which will lower the receive sensitivity of the array [47]. A way to mitigate this could be to increase the signal path length between the elements by partially separating them with an etching process [51]. An alternative solution could be removing the electrical path through the substrate completely [38], [52], which can be realized by utilising an insulating handling substrate as an alternative to silicon.

For the first effect, the ωRC criterion sets requirements for the resistivity and thickness of the material used to fabricate the top and bottom electrodes and the fabrication techniques needed. Two main types of electrodes determines which techniques that can be used; metal electrodes, which will require processes with a low processing temperature or thermal budget, and silicon-based electrodes allowing for a higher thermal budget.

If silicon is used as bottom electrode material, a limit of around 10^{21} cm^{-3} is set as the highest doping level, which can be achieved, corresponding to a resistivity of 10^{-4} Ω cm [53]. This can prove problematic for long arrays when considering ωRC. CMUTs fabricated with a silicon substrate using fusion/direct bonding process [54], [55] requires a high temperature post annealing step at $>$ 1000 °C to fuse the dielectric insulation layer with a top plate. Such a device is illustrated in Fig. 1(a) fabricated on an SOI wafer. The temperature step makes this technique incompatible with metal bottom electrodes, and one has to rely on the low resistivity of doped silicon for the bottom electrodes and increase the electrode thickness to keep the resistance sufficiently low.

Bottom electrodes made of metal are typically fashioned e.g., in Al, Cr, or Au. In comparison to doped silicon, metal electrodes have a resistivity on the order of 10^{-6} Ω cm [56], which being two magnitudes lower than doped silicon, will reduce resistance problems and be sufficient for most applications, depending on the electrode shape. The low thermal budget limits the number of techniques which can be used for CMUTs to mainly three types. 1) Adhesive polymer bonding [57] using e.g., BCB [38], see Fig. 1(b). This is a versatile method for joining different types of substrates and top plates with a polymer spacer, which can be patterned as a standard UV-sensitive resist and used with both silicon and metal bottom electrodes. 2) Sacrificial release methods [58], which can be used with both metal and silicon electrodes, see Fig. 1(c). For this technique an intermediate sacrificial layer between the substrate and a dielectric layer is dissolved, leaving CMUT cavities covered by a dielectric plate. 3) Finally, anodic bonding [59] can be used, where bottom electrodes are made by etching CMUT cavities into a glass substrate,

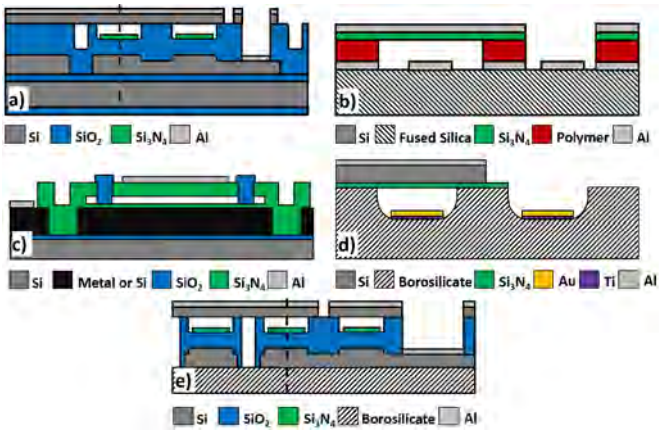


FIGURE 1. Cross-sectional view of five different RCA CMUT fabrication technologies. (a) Fusion bonding of a silicon top plate to a LOCOS structure grown on a doped SOI substrate. Figure is adapted from [50]. (b) Adhesive polymer bonding of a silicon nitride membrane to a fused silica wafer with metal electrodes using polymer [38]. (c) Sacrificial release method using a metal or doped silicon bottom electrode, where cavities are formed by etching of a sacrificial layer encapsulated in silicon nitride. (d) Anodic bonding of an insulated top plate to a structured borosilicate glass substrate with metal electrodes [44]. (e) A combination of a silicon top plate fusion bonded to a LOCOS structure and a borosilicate glass plate anodically bonded to the backside. A doped silicon substrate separated with a trench etch is utilised as bottom electrodes.

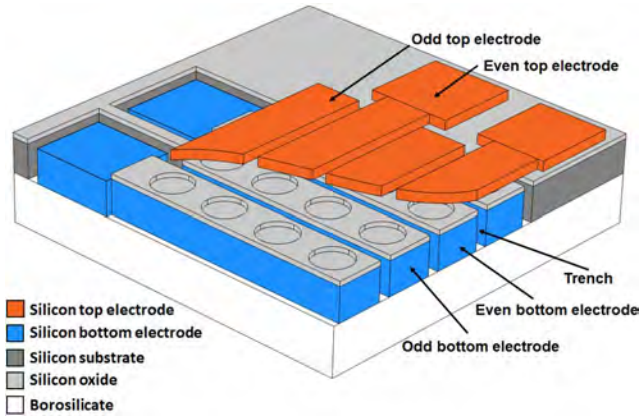


FIGURE 2. A 3D sketch of the corner of an RCA array. The orthogonal blue bottom electrodes and orange top electrodes, made of silicon, are shown encapsulating the structured oxide layer with the circular CMUT cells. A wide trench is shown separating the bottom electrodes laterally, and a glass substrate (borosilicate) is shown bonded to the backside of the structure.

metal electrodes are deposited, and the substrate is bonded to a silicon top plate, see Fig. 1(d). This has a maximum processing temperature of 375 °C.

In contrast, CMUT top electrodes are typically made using a wafer-bonded plate of silicon, which is then covered with a thick metal layer of low resistivity. For typical electrode designs the electrode resistance will not affect the pressure field [51]. The metal deposition happens as one of the last process steps and is not affected by previous high temperature processes. It can therefore be used in combination with various types of CMUTs.

Ideal structures for low resistance signalling would be combining a glass wafer patterned with CMUT cells, using a metal bottom electrode [44], [46], [59]. Such devices using dielectrics for the membrane or etching for structuring cell cavities can, however, display stability issues and dielectric charging of the device [60], [61], [62]. However, a fabrication process based on an SOI substrate together with the local oxidation of silicon (LOCOS) technique [55] and fusion bonding have been shown to exhibit little to no charging [50]. The structure is illustrated in Fig. 1(a). The LOCOS process, when used for CMUT fabrication, allows for reduced parasitic capacitance, high dielectric strength, good uniformity and tightly controllable CMUT dimensions and vacuum gap height down to under 10 nm precision due to the predictability of the oxide thickness [63].

D. NEW CMUT DESIGN

In this paper, we present a hand-held RCA CMUT based probe for volumetric imaging with a potential use in medical applications. This device is based on a LOCOS process fabricated on a doped silicon wafer, in combination with fusion bonding to an SOI wafer and a physical separation of the bottom electrodes to reduce cross-talk between the elements [52]. This is realised using a deep reactive-ion etching (RIE) based process. For improved mechanical stability, while also providing element-to-element insulation and low capacitive substrate coupling, a borofloat glass wafer is anodically bonded to the backside of the elements after the separation process. The separated electrodes have a cross-section of almost $100 \times 100\ \mu m^2$ which combined with a highly doped silicon substrate will mitigate delay-line effects.

The fusion-anodic double bonded structure is illustrated in Fig. 1(e) and as a cross-sectioned 3D sketch in Fig. 2. This device should benefit from stable high-performing CMUTs while also exhibiting low element-to-element coupling and high transmit pressure uniformity.

The paper is organized as follows: Section II is divided into a part *A* and *B*. The first part introduces the general design parameters of the presented CMUT array. The second part describes in detail the cleanroom fabrication of the device. Section III describes the assembly of the transducer probe. Results from the thermal, electrical and acoustical characterizations are presented in Section IV and discussed in Section V. Ultrasound imaging and measurements of sensitivity and penetration depth performed with the probe is described in Section VI. Finally, a conclusion is drawn in Section VII.

II. DESIGN & FABRICATION

A. DESIGN

The RCA array design is a symmetrical square with 190 row elements and 190 column elements used for beamforming, divided into rectangular segments of 95 odd and even elements of alternating pad numbering on each side of the array.

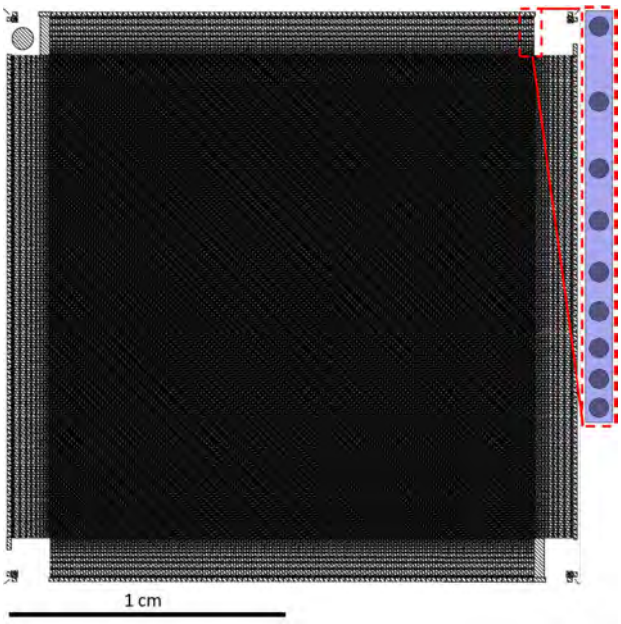


FIGURE 3. **Design overview of the 190+190 RCA CMUT array. The integrated apodization region designed to roll-off the signal towards the edge is seen in the inset.**

A 3D sketch of the corner of an array is shown in Fig. 2. This cut-off of the array shows four orthogonal top and bottom electrodes highlighted in orange and blue, respectively, as well as the underlying cells and element separation. Bordering the central region of the array are four apodization regions as shown in the boxed section in Fig. 3, which each are accessible from a single contact pad in the corners of the array not shown in Fig. 2. This raises the total channel count to 192+192. The apodization is incorporated into the design to round off the signal towards the edges of the array with a Hann window function. This reduces the relative signal amplitude from 1 to 0 at the edge of the apodization region and thereby suppresses side lobes and ghost echoes. The signal is decreased over nine cells with an increasing inter-cell distance. The RCA CMUT array is designed with an element pitch of 95 μm. The elements are 92.5 μm wide and contains a single row of circular cells which are 70 μm in diameter. If the plate thickness is chosen as 4.0 μm and the vacuum gap height is 196 nm this will give a center frequency of 9.15 MHz in air and $\approx$ 4.5 MHz in immersion using a pull-in voltage of 190 V. The center frequency in immersion was found using the following equation

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1+\beta}} = \frac{1}{\sqrt{1+\Gamma\frac{\rho_m}{\rho_p}\frac{a}{h}}} \tag{3}$$

obtained by Lamb [64] and revisited by Amabili and Kwak [65]. Here, ω_r/ω_0 is the ratio between the resonant frequency in water and vacuum, β is the added virtual mass incremental factor (AVMI) consisting of the medium to plate density ratio, ρ_m/ρ_p, the radius, a, and the thickness of the plate, h. Γ is the non-dimensionalised added virtual mass incremental (NAVMI) factor which can take multiple values depending on the clamping conditions. The value stated by Lamb [64] of $\Gamma = 0.6689$ is chosen. The center frequency in immersion is predicted to be around 49 % of the center frequency in air (9.15 MHz at 80 % of $V_{\text{pull-in}}$).

TABLE 1. **Designed transducer parameters.**

Design parameter		Unit
Array		
Number of elements	190+190	
Element pitch	95	µm
Element width	92.5	µm
Kerf	2.5	µm
Element length	20.95	mm
Element thickness	100	µm
Apodization length	1.45	mm
Apodization cell length	9	
Array side length	2.14	cm
Center frequency in air	9.15	MHz
Center frequency in immersion	4.5	MHz
CMUT cell		
Cell diameter (round)	70	µm
Distance to cell kerf	11.25	µm
Plate thickness	4.0	µm
Al electrode thickness	400	nm
Vacuum gap	196	nm
Nitride thickness	55.6	nm
Insulation oxide thickness	375	nm
Post oxide thickness	825	nm
Pull-in voltage	190	V

The center frequency, gap height, and plate thickness were determined using the finite element method (FEM) simulators OnScale and COMSOL.

The remaining design parameters are stated in Table 1. The previously discussed delay-line effect above in Section I, will theoretically for one element of the 190+190 RC array, using $C = 23.6$ pF and $R = 556\,\Omega$, approximately equal

$$\omega RC \approx 0.38 \tag{4}$$

at a frequency of 4.5 MHz. This corresponds to a drop in signal along the element of approximately 1.2 %. This is deemed an acceptable loss considering that the silicon substrate used for fabrication has a resistivity of 0.025 Ω cm or less. For the top electrodes, the resistance is $R = 15\,\Omega$ and an ωRC value of less than 0.01 is found showing that metal electrodes are efficient in suppressing this effect.

The four inch wafer design features eight RCA arrays each with a footprint measuring $2.14 \times 2.14\,\text{cm}^2$. Furthermore, 16 smaller 16+16 RCA arrays as well as linear arrays are included for electrical and acoustical testing.

B. FABRICATION

The fabrication of the CMUT array was based primarily on the LOCOS process [55] for structuring the cells and fusion bonding for encapsulation. As mentioned in Section II-A a physical trench separation was used to isolate the bottom elements of the array. The separation etching process used was developed at DTU Nanolab and is a modified 3-step Bosch process called deposit, remove, etch, multistep (DREM) [66].

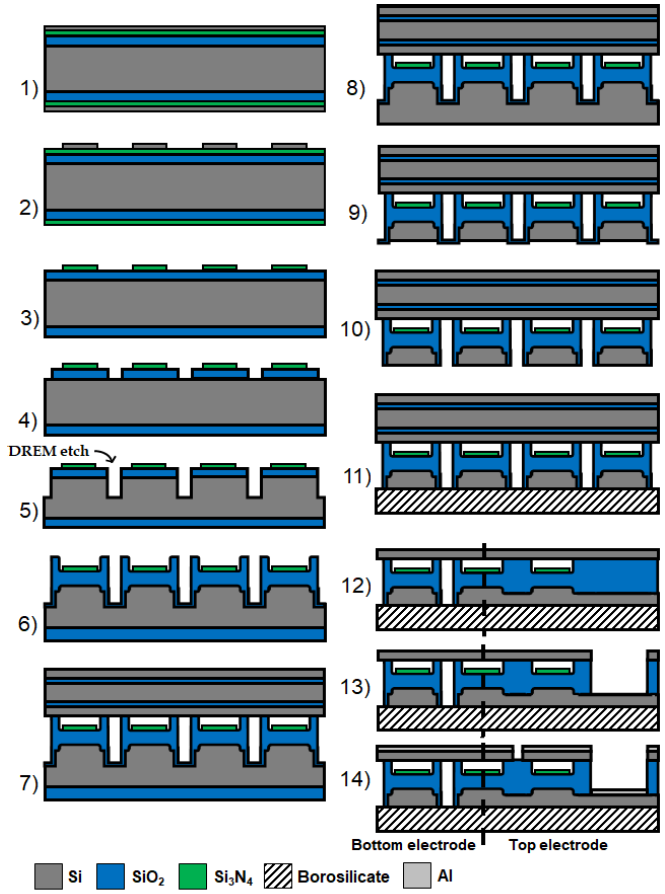


FIGURE 4. Fabrication process flow for the row-column CMUT array. The dashed line in drawings 12) through 14) represents a shift in perspective between a cross-section of the bottom electrode (to the left) and the top electrode (to the right).

The multiple steps have been fine-tuned to eliminate mask-erosion during etching (achieving so-called "infinite" selectivity [66]) and preserve scallop and hole uniformity even for high aspect ratios.

The fabrication process illustrated in Fig. 4 started with a highly doped 525 μm thick silicon wafer having a resistivity of $\rho < 0.025\,\Omega\,\text{cm}$ corresponding to a donor doping level, N_d, of $10^{19}\,\text{cm}^{-3}$. First a silicon dioxide layer of 375 nm, used for insulation, was grown in a dry thermal oxidation process at 1100 °C, then a low pressure chemical vapour deposition (LPCVD) silicon nitride of 55.6 nm and an LPCVD polycrystalline silicon (poly-Si) layer was deposited on top (using Tempress horizontal furnaces), see step 1). The poly-Si layer was then patterned with circles representing cells in a photolithography step with the diameter stated in Table 1 and etched using a poly-Si etching solution (HNO_3:BHF:H_2O (20:1:20)), step 2). The pattern was transferred into the nitride using hot phosphoric acid (H_3PO_4 at 160 °C) and the poly-Si masking layer was stripped using RIE (SPTS Pegasus). This will leave the nitride masking pads on top of the oxide in place of the cavities, step 3).

At this point the oxide surface was patterned with resist and trenches were etched using RIE (advanced oxide etcher (AOE) STS MESC Multiplex ICP) into the oxide in the kerf between the elements to expose the underlying silicon substrate, step 4). Then, the DREM process was performed at a temperature of −19 °C using the SPTS Pegasus for a trench etch depth of around 100 μm, step 5). These can be seen in Fig. 5, where deep straight trenches have been etched in silicon.

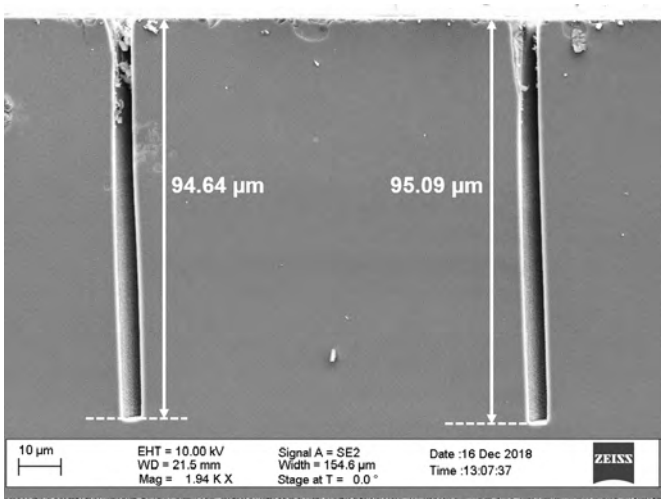


FIGURE 5. Scanning electron microscope image illustrating the DREM trench etched in step 5) of the fabrication process.

The wafer was then cleaned in RCA cleaning solution, and a second thermal oxidation process was performed in a wet oxidizing environment at 1100 °C to grow the post oxide to a total thickness of 825 nm, step 6). This formed the cavities through the LOCOS process with a gap height of 196 nm, excluding the nitride pad thickness. The device wafer was RCA cleaned again together with a poly-silicon-on-insulator (PSOI) wafer [67], which has been custom made to match the desired plate thickness. The structured device wafer and the PSOI wafer were then fusion bonded together, illustrated in step 7), at 400 °C with a tool pressure of 4 bar (performed on a Süss SB6 wafer bonder) and then subsequently annealed at 1100 °C for 70 min to form permanent silane bonds.

The oxide layer on the backside of the bonded wafer stack was removed with a BHF solution, step 8). Most of the silicon substrate was removed using lapping (Logitech PM5 Lapping & Polishing System), leaving approximately 150 μm to 180 μm. To completely separate the bottom electrodes from the backside the remaining 50 μm to 80 μm was etched using RIE (advanced silicon etcher (ASE) STS MESC Multiplex ICP)), step 9), exposing the trenches and oxide from step 6), seen in Fig. 6.

The backside surface was then polished to remove the free-standing oxide and to reduce the roughness necessary for anodic bonding, step 10). This was performed using a Logitech CM62 Orbis CMP (Chemical Mechanical Polishing) machine. A 500 μm thick borosilicate glass wafer was anodically bonded to the 100 μm thick electrodes on the backside using a four step voltage ramp (200 V/400 V/600 V/800 V) at an elevated temperature of

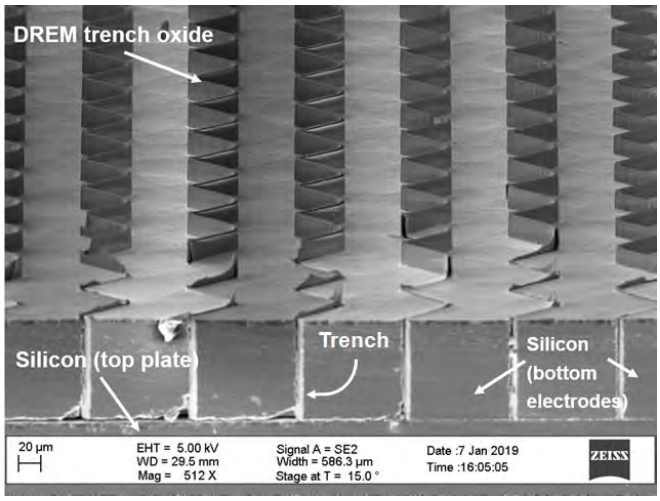


FIGURE 6. Scanning electron microscope image of a test structure illustrating the cross-section of the backside of the wafer after step 9), before polishing. The exposed DREM trench oxide walls separating the bottom electrodes are clearly visible. This was also previously presented in [52].

375 °C, step 11). The top poly-Si layer, two buried oxide (BOX) layers and the bulk of the PSOI handle wafer were then removed in a combination of dry and wet etching using RIE, BHF, KOH at 80 °C, and BHF, which left only the poly-Si top plate, step 12). The dashed line illustrates a shift in the perspective between the cross-section of the bottom electrode to the left of the line and the top electrode to the right, respectively.

Holes for contacting the bottom electrode pads were made by etching through the poly-Si plate and post oxide using a resist mask with a RIE ASE process tool, step 13). During this process it was discovered that not all post oxide was etched for some of the contact pads due to the formation of a sulphur compound, see Fig. 7. Multiple cleaning steps with RCA, HCl, HNO_3, and Piranha were tried without success. As a result, this prevented a complete access to the incomplete pads making wire bonds unreliable and lowering the electrode yield. The wafer surface was then coated in 400 nm aluminium (utilizing a Temescal FC-2000 e-beam evaporator), which was patterned using a PES Al etching solution [68] to form the top metal electrodes. Finally, the plate was etched through on the ASE to separate the top electrodes completely, step 14).

The last step was dicing the wafer using a (DISCO DAD-321) dicing saw.

III. ASSEMBLY

The diced array chip was mounted and glued to a rigid-flexible four-armed printed circuit board (PCB), and wire bonding was performed to connect the individual element contact pads on the chip to the PCB. The top and bottom electrodes were designated as rows and columns, respectively, and each of the four sides of the chip, of either odd or even elements, were wire bonded to each PCB arm for a total of 384 channel connections, depicted in Fig. 8. The

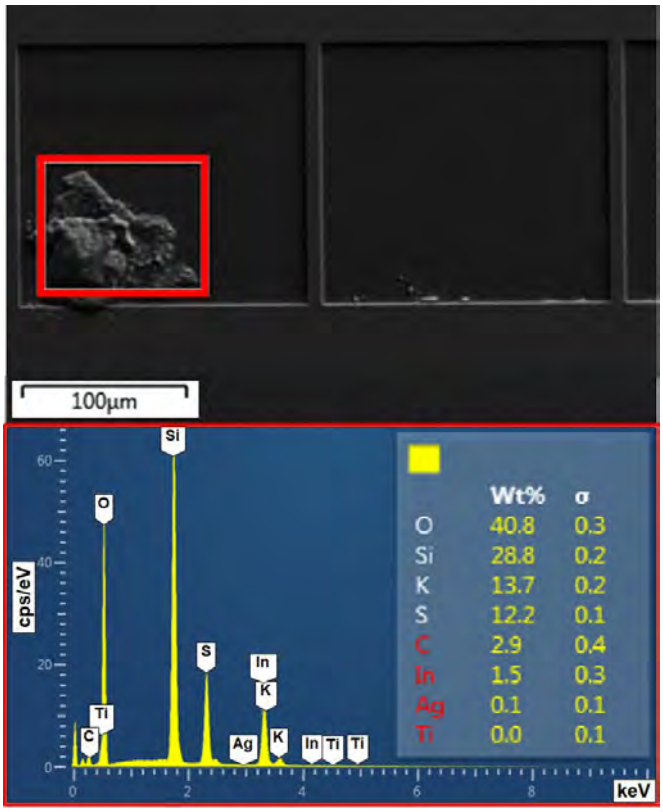


FIGURE 7. Scanning electron microscope image showing an example of a particle consisting of a sulphur compound. This partially blocks the SiO_2 etching process in step 13) in Fig. 4 which prevents the opening to some of the bottom electrodes, and leads to problems in the definition of top electrodes in step 14), thus reducing the yield. The inset represents an EDX spectrum of the area marked in red, showing a high concentration of sulphur and potassium which is not observed in particle-free areas.

assembly of the transducer probe was done at the facilities of BK Medical (State College, PA, USA). A tall glob-top dam was glued to the edges of the rigid PCB to ensure that neither the wire bonds or the chip were damaged by external mechanical stresses during scanning or assembly. The array was then encapsulated by filling the dam with room temperature vulcanizing (RTV) silicone, RTV664, described in more detail in [16], [69]. The thickness of the RTV directly on top of the chip was 0.485 mm on average. On top of the shield, the final layer of RTV was 0.595 mm on average. The attenuation of the RTV was 2.3 dB/mm at 4.5 MHz, so the total one-way attenuation is 2.5 dB for this array. An aluminised polymer film (12.5 μm polypropylene with a sub-micron thick aluminium layer), used as electromagnetic interference (EMI) ground shielding, was applied before the silicone cures and the PCB was mounted in a 3D milled PPSU probe nose-piece. Another layer of silicone was applied to the array surface and levelled to the probe edge, thus completely sealing and insulating the array.

The four sections of the rigid-flexible PCB were folded and connected to four preamplifier boards. The boards are each equipped with six MAX14822 16-channel high voltage

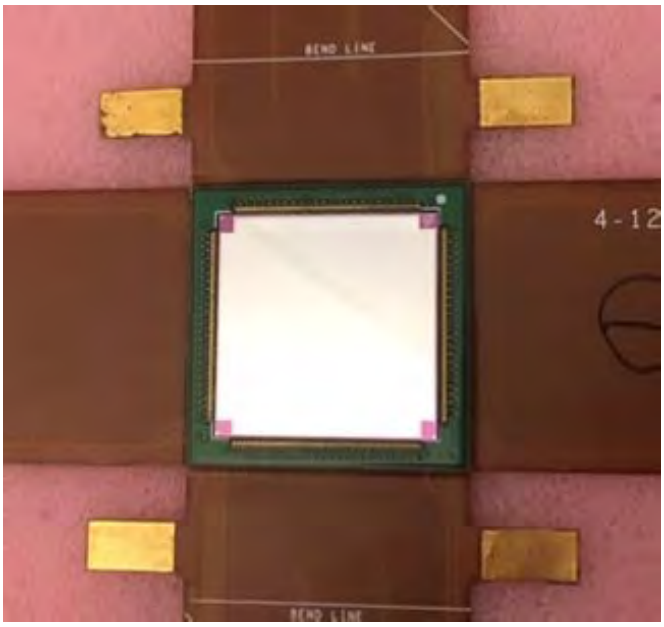


FIGURE 8. Flex rigid PCB with the mounted and wire bonded chip. Each arm of the PCB is connected to a section of the array; north and south, east and west, corresponding to even and odd rows or columns, respectively.

(HV)-protected transimpedance low noise active amplifier ICs with a bandwidth of 45 MHz. These amplifiers are capable of supplying high voltage AC in transmit (TX) and receive (RX) individually on each channel of the probe superimposed on a DC bias. Each board has support for 96 channels, and two boards, pairing either the odd or even element, are connected with board-to-board connectors. Each pair of amplifier boards were connected to a 192 odd or even channel coaxial scanner cable (BK Medical, Herlev, Denmark). The board pairs were then shielded in Kapton and copper tape. Two cooling hoses for inlet and outlet were then encapsulated along with the boards within the probe shell by two 3D milled shell pieces, effectively sealing the transducer probe handle. The assembled probe is seen in Fig. 9.

IV. CHARACTERIZATION

A. THERMAL

The probe handle is fitted with an inlet and outlet tube for air cooling of the amplifier boards during scanning. An experiment was performed to evaluate the cooling capability during idle mode and when emitting a suitable imaging sequence. Temperature measurements were performed in air, see Fig. 10, on the side of the assembled probe body and on the front sole of the nose piece using two FLIR C2 thermal imaging system cameras mounted on a frame. These measurements showed that the idling temperature of the probe when supplied with a DC voltage of 190 V, corresponding to 160 V at the chip level, gives an average temperature at $\approx$ 31 °C on the sole (blue) and $\approx$ 36.5 °C on the side (red) after 25 min. An imaging sequence with a synthetic aperture (SA) using 18 elements, 192 emissions, a pulse repetition frequency of 12 kHz, and 75 V peak-to-peak was then used

FIGURE 9. Assembled three-part custom 3D milled PPSU probe handle. The RCA CMUT array is buried underneath the stack of RTV silicone, aluminium polymer foil and silicone covering the nose piece. The two cooling hoses can be seen protruding beside the scanner cables.

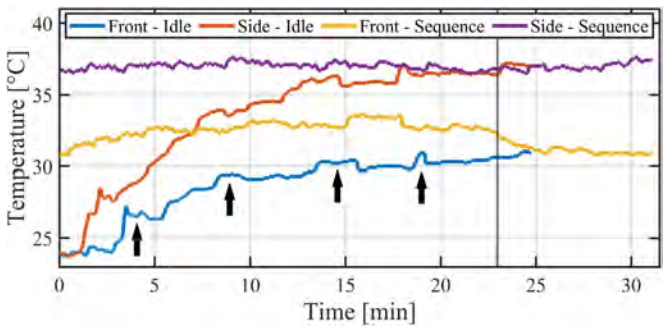


FIGURE 10. Thermal measurements performed on the assembled probe body using a setup with two FLIR C2 thermal imaging system cameras. These were mounted on a frame to measure the temperature on the probe from the side and the front. Measurements were performed in idle mode with an applied bias voltage and when using an imaging sequence. The vertical line at 23 min indicates when the sequence used for excitation is stopped. The slight variations in the dataset, illustrated by the black arrows for the blue curve, are caused by the thermal cameras performing automatic re-calibration during the measurements.

as excitation signal. The surface temperature of the sole rose $\approx$ 2 °C during the measurement, reaching a maximum average of 32.8 °C (yellow) after 5 min. The probe side had a stable surface temperature of $\approx$ 36.5 °C (purple) throughout the measurement which is caused by the underlying voltage regulator on the amplifier boards. The temperature rise and surface temperature of the transducer body and sole when idling and imaging were both found acceptable for experimental external use below the FDA and DS/EN limits for scanning [70]. The airflow inside the current probe design is, however, likely restricted by the preamplifier boards and their shielding and the internal temperature is probably higher than what is measured on the surface.

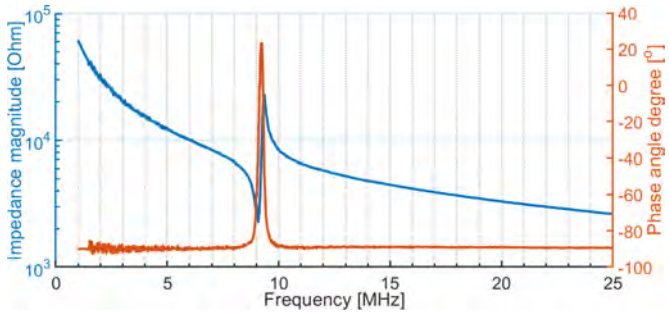


FIGURE 11. Impedance measurement of a CMUT test element at 150 V DC bias and 50 mV AC. The resonance and anti-resonance peaks are seen at 9.1 MHz and 9.3 MHz, respectively.

B. ELECTRICAL

The electrical response of the CMUT array has been characterized before it was mounted in the probe handle using impedance measurements. These were performed using an Agilent 4294A Precision Impedance Analyzer. During the measurements the bias voltage was supplied through a bias tee by a Keithley 2410 sourcemeter.

Measurements were performed on separate linear test arrays and single test elements located in the corners of the 192+192 arrays to provide an accurate pull-in voltage for the array. The DC voltage supplied by the sourcemeter was varied between 0 V to 200 V while a 50 mV AC voltage from the impedance analyser was superimposed on top. The voltage sweep could then be used to find the pull-in voltage. With a constant supplied DC bias the array showed a stable performance and exhibited no charging. This showcases the effectiveness of the LOCOS fabrication process.

Fig. 11 shows measurements, performed on a test element, of the impedance magnitude and phase from 1 MHz to 25 MHz for an applied voltage of 150 V. A pull-in voltage of 186 V was measured which compares well with the designed pull-in voltage of 190 V.
The measured center frequency was 9.25 MHz at a bias of $\approx$ 80 % of the pull-in voltage which is in good agreement with the COMSOL simulated value of 9.15 MHz in air. Using the same bias voltage the electromechanical coupling factor is calculated to be $k^2 = 4.5\,\%$.

C. ACOUSTICAL

Acoustical characterization of the assembled probe was performed on the experimental research scanner SARUS [71] using the approach in [72] and the transducer impulse responses were determined as described in [73].

1) IMPULSE RESPONSE

The one-way impulse and two-way pulse-echo responses were measured by submerging the probe in deionized (DI) water with either a hydrophone or a planar steel reflector placed 35 mm from the transducer surface, respectively. Emitting and receiving was done with one element at a time for all rows and columns, respectively. The DC bias was set to 160 V and the AC excitation voltage up to 150 V peak-to-peak (±75 V). The voltage levels were set to reflect the measured pull-in voltage mentioned in Section IV-B. The hydrophone used to measure the pressure in immersion was an Onda HGL-0400 hydrophone connected to an Onda AH-2010 amplifier.

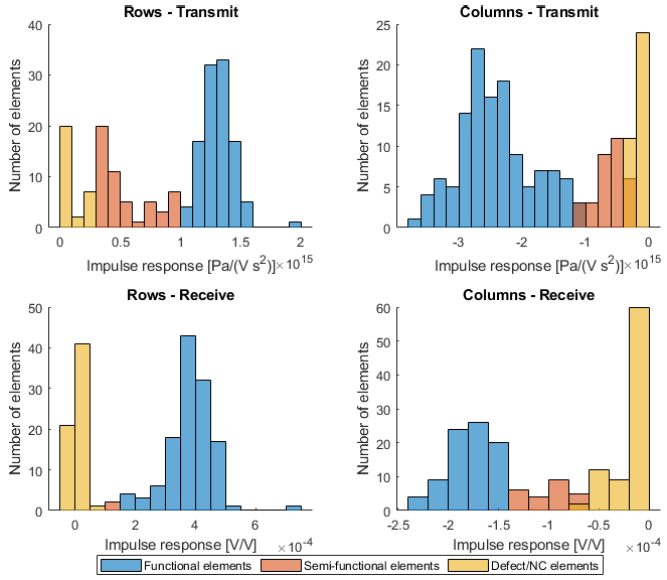


FIGURE 12. Histogram of impulse response of all row and column elements. The elements are grouped into three categories depending on their maximum impulse response values.

The elements have been grouped into three categories depending on their maximum impulse response values from the acoustic measurements in transmit and in receive, see Fig. 12. The overall element yield of the finished array in transmit has been measured to 109 (57.4 %) for the rows and 123 (64.7 %) for the columns. This was based on elements with an impulse response maximum value over $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$, designated as functional elements. The semi-functional elements have a lower response between $2.9 \times 10^{14}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ and $1.1 \times 10^{15}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (52 rows and 32 columns) and the defect or not connected (NC) elements have less than $2.9 \times 10^{14}\,\mathrm{Pa\,V^{-1}\,s^{-2}}$ (29 rows and 35 columns). Only the functional elements have been used for further acoustic characterization. The element yield measured in receive (pulse-echo) was 65.8 % and 43.7 % for functional rows and columns, respectively, with a cut-off at $1.4 \times 10^{-4}\,\mathrm{V\,V^{-1}}$. For semi-functional elements it was 1.1 % and 12.6 % for rows and columns, respectively, with a cut-off at $6.5 \times 10^{-5}\,\mathrm{V\,V^{-1}}$, and for NC elements the yield was 33.2 % for rows and 43.7 % for columns. The yield problems seem to be related to the formation of the sulphur compound mentioned in Section II-B.

The average transmit impulse response of the functional rows and columns can be seen in Fig. 13. The solid blue and red lines represent the response measured in $\mathrm{Pa\,V^{-1}\,s^{-2}}$ of the rows and columns, respectively, and the dashed lines in the same colour represent the envelope of the signal. The maximum impulse response values are between

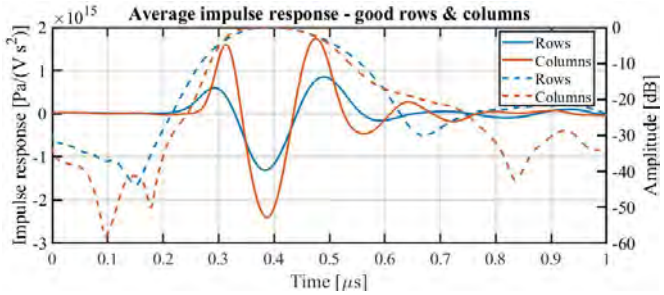


FIGURE 13. Average impulse response (TX) and the normalized envelope of the functional row and column elements with amplitudes above 1.1 x 10^{15} Pa V^{-1} s^{-2}.

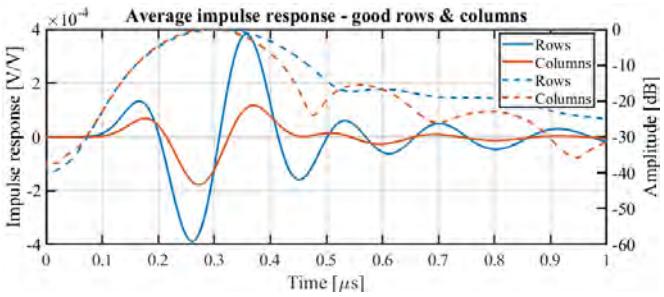


FIGURE 14. Average impulse response (PE) and the normalized envelope of the functional row and column elements with amplitudes above 1.4 x 10^{-4} V V^{-1}.

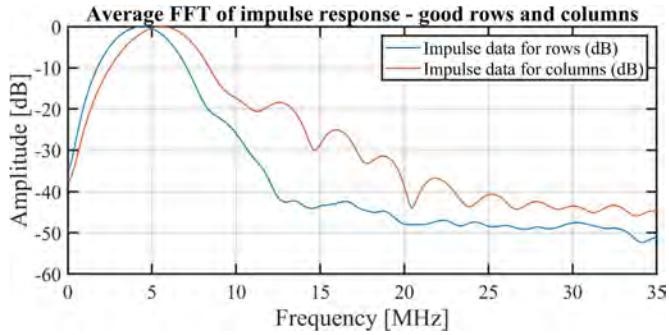


FIGURE 15. Average spectra of the impulse response in transmit (TX) of the functional row and column elements with amplitudes above 1.1 x 10^{15} Pa V^{-1} s^{-2}.

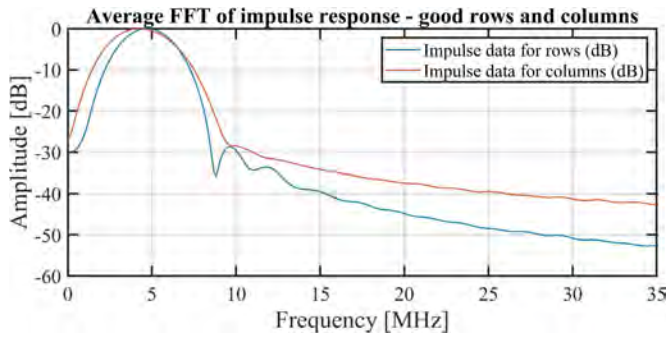


FIGURE 16. Average spectra of the impulse response in pulse-echo (PE) of the functional row and column elements with amplitudes above 1.4 x 10^{-4} V V^{-1}.

1.3 × 10^{15} Pa V^{-1} s^{-2} to 2.5 × 10^{15} Pa V^{-1} s^{-2}. It can be seen from the data that the signal transmitted from the rows is ≈ 55 % of the response of the columns. The received pulse-echo signal in Fig. 14 shows a longer pulse with a more pronounced ringing for the rows compared to the transmit measurements. The ratio between the row and column main peaks is around 2.4 with the rows now having a higher amplitude than the columns. The average transmit sensitivity of the rows and columns was found to be $1.3 \pm 0.1 \times 10^{15}$ Pa V^{-1} s^{-2} (rows) and $2.4 \pm 0.6 \times 10^{15}$ Pa V^{-1} s^{-2} (columns), with a total average of $1.9 \pm 0.7 \times 10^{15}$ Pa V^{-1} s^{-2}. The sensitivity for the pulse-echo measurements was $3.8 \pm 0.7 \times 10^{-4}$ V V^{-1} (rows) and $1.8 \pm 0.2 \times 10^{-4}$ V V^{-1} (columns), with a total average of $3.0 \pm 0.2 \times 10^{-4}$ V V^{-1}.

2) CENTER FREQUENCY AND UNIFORMITY

The center frequencies of the rows and columns were found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses of the transmit and pulse-echo signals plotted in Fig. 15 and Fig. 16 using the expression:

$$f_c = \frac{\sum_{i=0}^{N/2} S(if_s/N) \cdot if_s/N}{\sum_{i=0}^{N/2} S(if_s/(N))} \tag{5}$$

with f_s being the sample frequency of 70 MHz and N the number of frequency bins in the spectrum, S. In Fig. 17 the extracted center frequency f_c is plotted for each element showing the uniformity across the array in transmit (Fig. 17(a)) and pulse-echo (Fig. 17(b)). The average center frequencies of the functional row- and column elements were 5.0 ± 0.1 MHz (rows) and 6.85 ± 0.30 MHz (columns) with the total average being 6.0 ± 0.9 MHz in transmit, and 5.3 ± 0.2 MHz (rows) and 5.5 ± 0.5 MHz (columns) with the total average of 5.3 ± 0.4 MHz in pulse-echo. The peak frequency was also extracted from the spectral data and gave an average of 5.0 ± 0.6 MHz and 4.5 ± 0.5 MHz in transmit and pulse-echo, respectively, also seen in Table 2.

These values correspond reasonably well with the predicted resonance frequency in immersion of 4.5 MHz in both transmit and pulse-echo. However, the center frequency of the columns in transmit and the rows in pulse-echo both lie between 1 MHz to 1.5 MHz higher when biased at 86 % of $V_{\text{pull-in}}$.

3) BANDWIDTH

The frequency bandwidth (BW) of each element was found at the −3 dB and −6 dB points of the Fourier transformed impulse responses of the transmit and pulse-echo measurements, respectively. The mean BW for the functional rows and columns in transmit was 3.3 ± 0.2 MHz and 4.2 ± 0.4 MHz, respectively, with a total mean of 3.7 ± 0.5 MHz. In pulse-echo the mean BW was 4.2 ± 0.1 MHz and 5.3 ± 0.8 MHz for rows and columns, respectively, with a total average of 4.6 ± 0.7 MHz.

TABLE 2. Results obtained from acoustical measurements of the probe in transmit and pulse-echo.

Parameter	Transmit Row	Transmit Column	Transmit Total	Pulse-echo Row	Pulse-echo Column	Pulse-echo Total
Center frequency [MHz]	5.03 ± 0.11	6.85 ± 0.30	5.99 ± 0.94	5.25 ± 0.19	5.45 ± 0.54	5.33 ± 0.38
Peak frequency [MHz]	4.38 ± 0.16	5.59 ± 0.25	5.02 ± 0.64	4.70 ± 0.09	4.21 ± 0.39	4.50 ± 0.35
Center frequency bandwidth [MHz]	3.28 ± 0.19	4.16 ± 0.37	3.74 ± 0.53	4.17 ± 0.13	5.27 ± 0.80	4.61 ± 0.74
Relative fractional bandwidth [%]	65.23 ± 3.69	60.68 ± 3.98	62.82 ± 4.47	79.47 ± 3.66	96.40 ± 8.77	86.23 ± 10.37
Sensitivity $[\mathrm{PaV^{-1}s^{-2}}]/10^{15}$	1.3 ± 0.1	2.4 ± 0.6	1.9 ± 0.7	—	—	—
Sensitivity $[\mu\mathrm{VV^{-1}}]$	—	—	—	380 ± 70	180 ± 20	300 ± 20

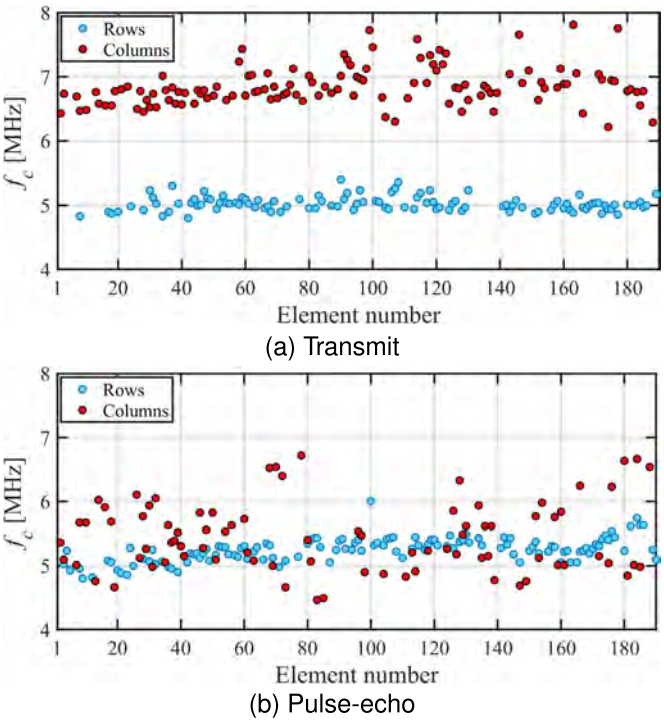


FIGURE 17. Extracted center frequencies across the array for each element in transmit (a) and pulse-echo (b). The frequencies were found by calculating the weighted mean of the frequencies in the Fourier transformed impulse responses. The average center frequency of functional row and column elements in the probe is 6.0 ± 9 MHz in transmit and 5.3 ± 4 MHz in pulse-echo.

The relative fractional bandwidth for the rows and columns in transmit was $65.2 \pm 3.7\,\%$ and $60.7 \pm 4.0\,\%$ with a total mean of $62.8 \pm 4.5\,\%$. In pulse-echo this was $79.5 \pm 3.7\,\%$ and $96.4 \pm 87.7\,\%$ for the rows and columns, respectively, with a total mean of $86.2 \pm 10.4\,\%$.

4) ωRC - PRESSURE UNIFORMITY

The effect of the electrode resistance on the transmit uniformity has been estimated by measuring the pressure field along the top and bottom electrodes. The pressure field was mapped in immersion by moving the Onda HGL-0400 hydrophone in the x-y plane in steps of 0.5 mm with a distance of 5 mm from the transducer surface. This creates a grid of 49×49 measurements with an area of 24.5 mm × 24.5 mm which completely captures the array. A 4-cycle sinusoidal 6.5 MHz pulse with an amplitude of $V_{\mathrm{AC}} = \pm 75\,\mathrm{V}$ has been used to excite three evenly spaced row elements and three column elements.

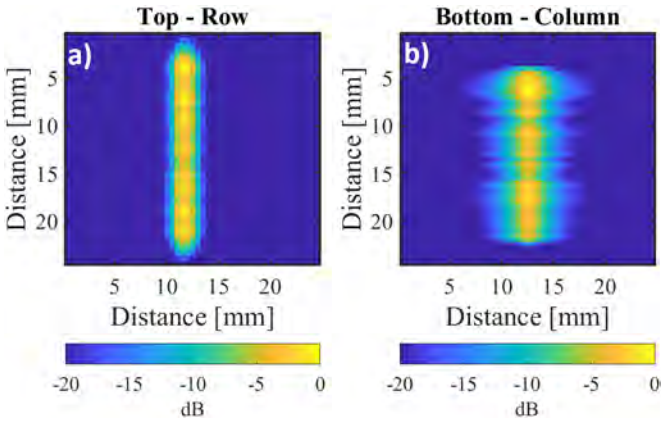


FIGURE 18. Average peak pressure field of elements excited at 6.5 MHz. The pressure is mapped for three different top and bottom electrodes using a hydrophone and an average is shown in (a) for top electrodes (rows) and in (b) the bottom electrodes (columns). The pressure is uniform along the top electrodes. The pressure measured along the bottom electrodes shows a clear maximum value in the top of the contact but remains mostly uniform along the element. The measured pressures have been normalized to 489.8 kPa and 554.7 kPa for the rows and columns, respectively.

The pressure maps shown in Fig. 18 are each an average of three elements and the plots have been normalized to their maximum value and log compressed. In Fig. 18(a) for the top electrodes (rows), it is seen that the pressure distribution is even along the elements. The mean value of the first and last 1/4 part of the element has been calculated as an estimate of the uniformity as −2.4 dB and −2.9 dB. Fig. 18(b) depicts the bottom electrodes (columns) for which similar values have been calculated as −1.9 dB near the contact pads and −3.0 dB near the end of the elements. This corresponds to a drop to $88 \pm 16\,\%$ of the initial amplitude, or 12 % attenuation. The ωRC value for the measurement frequency is 0.55, which corresponds to a drop to 97.6 % of the initial value or 2.4 % attenuation. The measured attenuation is larger than the predicted value which could be caused by the low yield of the orthogonal elements providing the grounding during the measurement.

This value can be compared to an attenuation of 74 % measured on a previously fabricated 92+92 RCA array with a center frequency of 4.5 MHz and a bottom electrode resistivity of $< 0.1\,\Omega\,\mathrm{cm}$ [48].

The data depicted in Fig. 18, which is an average of three emitting row and column elements, exhibited large variations

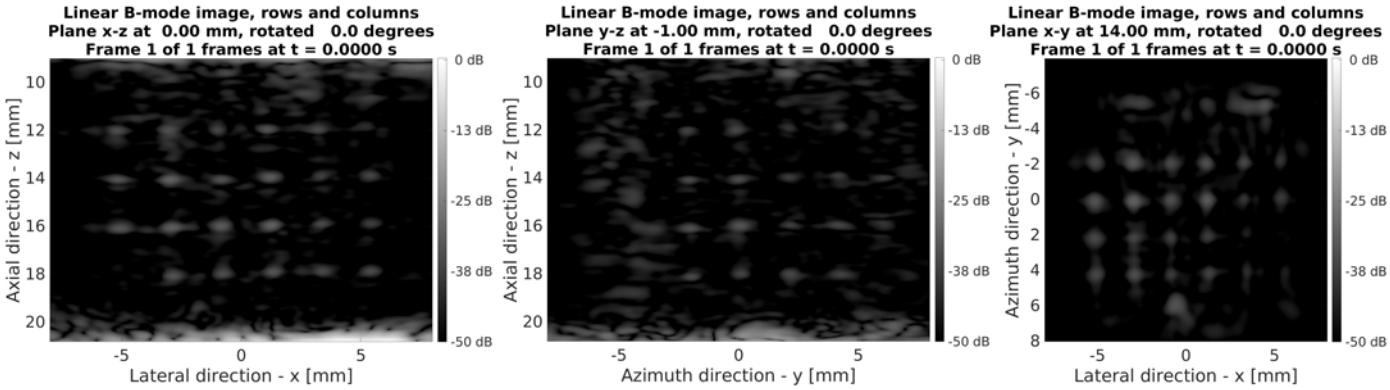


FIGURE 19. Point spread functions in three orthogonal planes obtained from a stereolithography 3D printed hydrogel phantom using the 190+190 transducer probe. The phantom has a grid of 6 x 4 x 4 isolated 205 x 205 x 80 μm^3 embedded cavities, which function as scattering point targets.

in the recorded pressure and this likely causes the large standard deviations of the attenuation.

V. IMAGING

The imaging capabilities of the probe was evaluated using the SARUS system by scanning a wire phantom, a cyst phantom, and a stereolithography 3D printed hydrogel phantom with isolated 205 × 205 × 80 μm^3 embedded cavities, which function as point scatter targets [74]. The scatterers were placed in a 6 × 4 × 4 grid with a spacing of 2.05 mm. 3D imaging was performed using a SA sequence with 96 row and 96 column emissions and three orthogonal planes are shown in Fig. 19. From this the resolution of the point spread function (PSF) could be determined in the axial direction as 0.82 λ (0.1880 mm) and in the lateral direction as 1.72 λ (0.3936 mm). The side-to-main lobe level was fairly high at −11.90 dB due to scattering from the phantom surrounding the point cavities.

The resolution is visualized in Fig. 20, which depicts three different planes from the volumetric scan of a wire phantom. The phantom is a matrix of wires immersed in water with little attenuation. The x-z (lateral) plane shows the wires as horizontal lines, the $y - z$ (azimuthal) plane shows two columns of wire cross-sections as dots, and the $x - y$ (transverse) plane depicts a single wire. The resolution in this phantom was in the axial direction 1.16 λ (0.2654 mm) and in the lateral direction 1.56 λ (0.3562 mm). The contrast was −16.90 dB due to the many missing elements.

The penetration depth was found at the point when the signal to noise ratio (SNR) attains a value of 0 dB, shown in Fig. 21, and was experimentally obtained by imaging a tissue mimicking cyst phantom with an attenuation of 0.5 dB/[MHz cm] using a SA sequence with 96+96 emissions at 6.5 MHz. This excitation frequency was chosen to use the full bandwidth of the probe to gain the best possible resolution. The transducer reaches a depth of 150 λ, where the wavelength λ in this phantom is 0.2375 mm. This corresponds to a penetration depth of 3.6 cm again due to the many missing elements.

VI. DISCUSSION

The amplitude of the impulse response of the row elements during pulse-echo measurements was found to be a factor of 2.4 times higher than the columns. This reduction in receive sensitivity for columns is likely due to the aforementioned parasitic capacitance in Section I-C. Since a glass wafer is used as the substrate instead of an SOI wafer during fabrication this effect was hypothesised to be lower as the coupling should be significantly reduced. However, the 100 μm thick and ≈ 2.1 cm long bottom electrodes separated by a 2.5 μm wide trench can potentially contribute to an increased parasitic capacitance, which ultimately will lower the sensitivity. During the transmit measurements, a reduction in the transmit sensitivity for the rows by a factor of 1.92 compared to the columns was observed. It is also observed that in transmit, the columns have a higher center frequency than the rows even though all CMUT cells have the dimensions, and the plate thickness is uniform across the array. These effects are currently not understood and is the subject for future work.

A previously fabricated 92+92 RCA CMUT probe [75], which is based on an SOI wafer substrate with a 20 μm device layer, exhibited a reduction of the bottom electrode receive sensitivity by a factor of around 3.3. The presented 190+190 fusion-anodic bonded probe shows a clear improvement in receive sensitivity over the previous SOI wafer based fusion bonded design. The presented probe has, however, shown problems with element yield and demonstrated only around 55 % working elements. This is believed to be due the formation of a sulphur compound in the processing chamber when etching an opening to the bottom electrodes. Ultimately, this prevented some wire bonds from making proper contact and lowered the overall yield and performance of the probe. Solving this problem requires further investigation and tuning of the cleaning processes, the chamber conditioning, and the gas composition used when performing the silicon oxide etching process on the samples.

Ultrasound imaging showed that the probe is capable of performing 3D volumetric imaging, but the low SNR limits the penetration depth to 150 λ corresponding to 3.6 cm. The

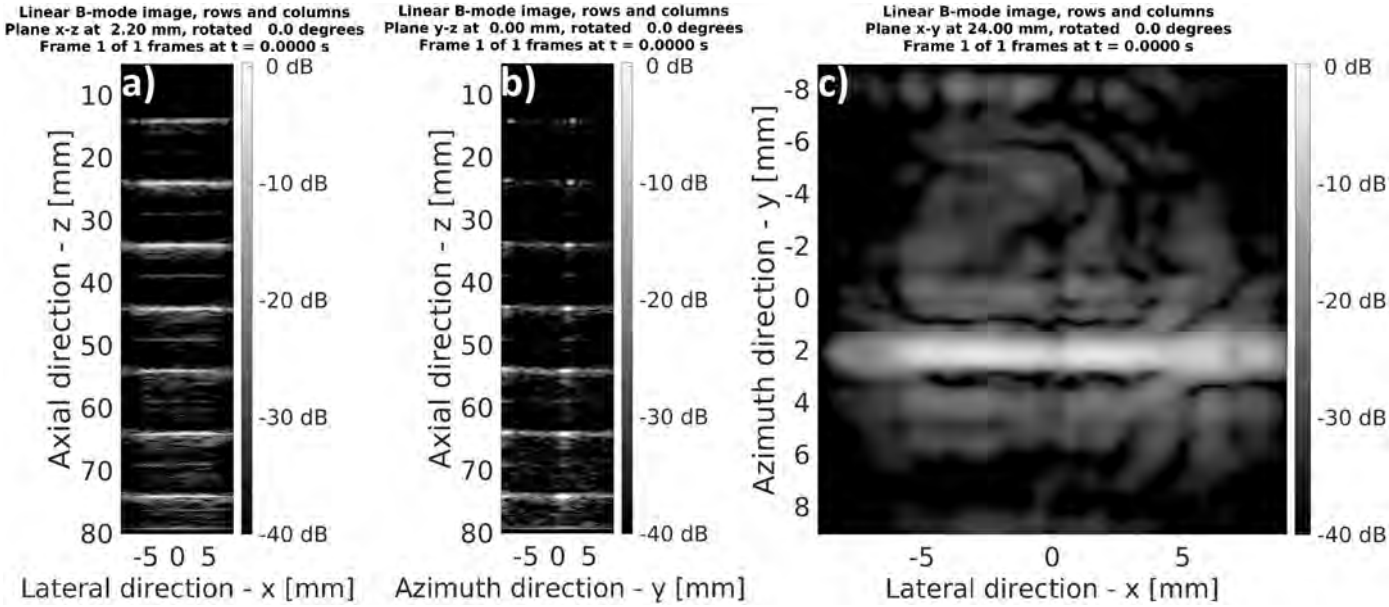


FIGURE 20. Imaging planes of a wire phantom obtained using the 190+190 transducer probe. The three different planes depict (a) the horizontal wires along in the x-direction (x-z plane), (b) two columns of wire cross-sections (y-z plane) and (c) the top of a single wire (x-y plane).

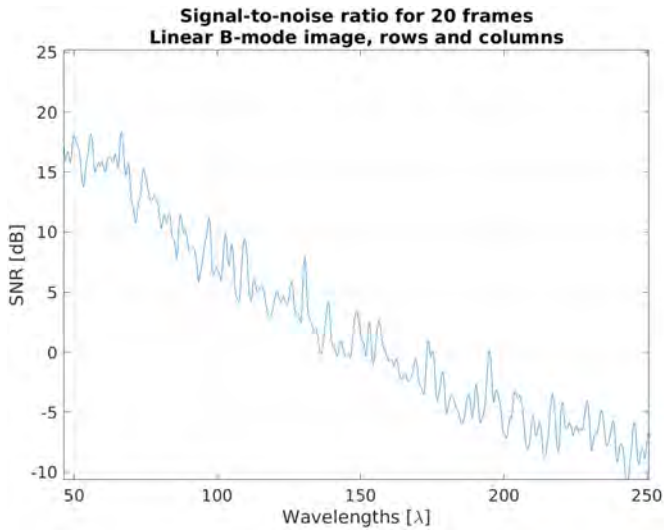


FIGURE 21. SNR of the 190+190 RCA probe for a tissue mimicking phantom with an acoustical attenuation of 0.5 dB/[MHz cm]. The penetration depth is roughly 150 λ when the SNR reaches 0, corresponding to 3.6 cm as the wavelength in this phantom is 0.2375 mm when imaging with a frequency of 6.5 MHz.

imaging performance of the probe is naturally also limited by the low number of working elements, which affects the main-to-side lobe levels. It is, however, demonstrated that full volumetric imaging is possible, and the point spread function is isotropic in all three directions with a volume rate comparable to normal 2D imaging with a linear array probe.

The probe has sub-$\lambda/2$ pitch and normally there would be no advantage in linear array imaging, but for second harmonic imaging grating lobes could be avoided at the double center frequency. Such measurements have, however, not yet been conducted.

VII. CONCLUSION

The developed hand-held 190+190 RCA CMUT ultrasound probe with integrated edge apodization and active cooling was fabricated using a standard fusion bonding process utilizing LOCOS in combination with an anodic bonding process and an etch separating the bottom electrodes. The array was wire bonded and mounted in a 3D milled PPSU probe handle. The element yield of the elements with an impulse response higher than 1.1×10^{15} Pa V^{-1} s^{-2} and 1.4×10^{-4} V V^{-1} in transmit and pulse-echo, respectively, was a total of 61.1 % and 54.7 %. This was in part due to the formation of a sulphur compound in the bottom electrode contact holes during fabrication. To improve the yield the microfabrication process can be further optimised. The formation of the sulphur compound can be avoided by further optimising the process conditions including temperature control, chamber pre-conditioning and gas flow. Characterization of the probe in transmit showed that the maximum value of the averaged impulse responses of the columns was a factor of 1.8 times higher than the rows in transmit. In pulse-echo the maximum value of the averaged impulse responses of the rows was a factor of 2.4 times higher than the columns due to the substrate coupling effect. Compared to a previously fabricated probe, where the averaged maximum impulse response of the rows were a factor of 3.3 times higher than the columns, the substrate coupling effect has been reduced. The weighted center frequencies were 6.0 ± 0.1 MHz in transmit and 5.3 ± 0.5 MHz in pulse-echo with relative fractional bandwidths of 62.8 ± 4.5 % and 86.2 ± 10.4 %, which is

close to the designed center frequency of 4.5 MHz. The attenuation of the transmit pressure along the top electrodes was found to be insignificant. For the bottom electrodes the transmit pressure was attenuated by 12 %, which is a clear improvement when compared to previous results where an attenuation of 74 % was measured. This demonstrates that using a highly doped ($< 0.025\,\Omega$ cm) 100 μm thick substrate in the fabrication process can solve the previously mentioned problems concerning high electrode resistances and the formation of delay lines.

The imaging performance of the probe was determined using a 3D printed point scatter phantom, a wire phantom, and a cyst phantom showing for the first two a reasonable contrast of -11.90 dB to -16.90 dB, considering the many missing elements, and the resolution was $0.82\,\lambda$ to $1.72\,\lambda$ (axial) and $1.56\,\lambda$ to $1.72\,\lambda$ (lateral), demonstrating the 3D volumetric capabilities with a near isotropic point spread function. The SNR measured on the tissue mimicking cyst phantom was low, resulting in a penetration depth of around 3.6 cm due to many missing elements. In conclusion, the fabrication process using thick highly doped silicon bottom electrodes and an insulating glass substrate has improved the pressure uniformity when emitting with the bottom electrodes and reduced the substrate coupling effect.

REFERENCES

[1] B. Savord and R. Solomon, "Fully sampled matrix transducer for real time 3D ultrasonic imaging," in *Proc. IEEE Symp. Ultrason.*, vol. 1, Oct. 2003, pp. 945–953.

[2] T. Halvorsrod, W. Luzi, and T. S. Lande, "A log-domain μbeamformer for medical ultrasound imaging systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2563–2575, Dec. 2005.

[3] S. Blaak et al., "Design of a micro-beamformer for a 2D piezoelectric ultrasound transducer," in *Proc. IEEE Int. Ultrason. Symp.*, Sep. 2009, pp. 1338–1341.

[4] Y. Chen, Y. Wen, and P. Li, "Loss mechanisms in piezoelectric transducers and its response to stress," in *Proc. Int. Conf. Inf. Acquisition*, 2004, pp. 213–219.

[5] M. Stewart and M. G. Cain, "Measurement and modelling of self-heating in piezoelectric materials and devices," *Characterisation of Ferroelectric Bulk Materials and Thin Films*. Dordrecht, The Netherlands: Springer, 2014, pp. 147–189, doi: 10.1007/978-1-4020-9311-1_7.

[6] S. W. Smith, H. G. Pavy, and O. T. von Ramm, "High-speed ultrasound volumetric imaging system. I. Transducer design and beam steering," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 38, no. 2, pp. 100–108, Mar. 1991.

[7] A. Austeng and S. Holm, "Sparse 2-D arrays for 3-D phased array imaging–design methods," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 49, no. 8, pp. 1073–1086, Aug. 2002.

[8] C. E. Morton and G. R. Lockwood, "Theoretical assessment of a crossed electrode 2-D array for 3-D imaging," in *Proc. IEEE Symp. Ultrason.*, vol. 1, Oct. 2003, pp. 968–971.

[9] C. E. M. Démoré, A. Joyce, K. Wall, and G. R. Lockwood, "Real-time volume imaging using a crossed electrode array," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 56, no. 6, pp. 1252–1261, Jan. 2009.

[10] M. F. Rasmussen and J. A. Jensen, "3-D ultrasound imaging performance of a row-column addressed 2-D array transducer: A measurement study," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Jul. 2013, pp. 1460–1463.

[11] J. A. Jensen et al., "Anatomic and functional imaging using row-column arrays," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 69, no. 10, pp. 2722–2738, Oct. 2022.

[12] C. H. Seo and J. T. Yen, "64×64 2-D array transducer with row-column addressing," in *Proc. IEEE Ultrason. Symp.*, Jun. 2006, pp. 74–77.

[13] C. H. Seo and J. T. Yen, "A 256×256 2-D array transducer with row-column addressing for 3-D rectilinear imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 56, no. 4, pp. 837–847, Apr. 2009.

[14] Y. Chen, M. Nguyen, and J. T. Yen, "7.5 MHz dual-layer transducer array for 3-D rectilinear imaging," *Ultrason. Imag.*, vol. 33, no. 3, pp. 205–216, Jul. 2011.

[15] C. Ceroici, K. Latham, R. Chee, J. A. Brown, and R. J. Zemp, "Bias-sensitive crossed-electrode relaxor 2D arrays for 3D photoacoustic imaging," *Proc. SPIE*, vol. 10494, Feb. 2018, Art. no. 1049420.

[16] M. Engholm et al., "Probe development of CMUT and PZT row–column-addressed 2-D arrays," *Sens. Actuators A, Phys.*, vol. 273, pp. 121–133, Apr. 2018.

[17] H. P. Savakus, K. A. Klicker, and R. E. Newnham, "PZT-epoxy piezoelectric transducers: A simplified fabrication procedure," *Mater. Res. Bull.*, vol. 16, no. 6, pp. 677–680, Jun. 1981. [Online]. Available: https://www.sciencedirect.com/science/article/pii/0025540881902671

[18] L. Changgeng, F. T. Djuth, Q. Zhou, and K. K. Shung, "Micromachining techniques in developing high-frequency piezoelectric composite ultrasonic array transducers," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 60, no. 12, pp. 2615–2625, Dec. 2013.

[19] M. I. Haller and B. T. Khuri-Yakub, "A surface micromachined electrostatic ultrasonic air transducer," in *Proc. IEEE Ultrason. Symp.*, vol. 2, Oct./Nov. 1994, pp. 1241–1244.

[20] A. S. Ergun et al., "Broadband capacitive micromachined ultrasonic transducers ranging from 10 kHz to 60 MHz for imaging arrays and more," in *Proc. IEEE Ultrason. Symp.*, vol. 2, Oct. 2002, pp. 1039–1043.

[21] S. H. Wong, M. Kupnik, K. Butts-Pauly, and B. T. Khuri-Yakub, "Advantages of capacitive micromachined ultrasonics transducers (CMUTs) for high intensity focused ultrasound (HIFU)," in *Proc. IEEE Ultrason. Symp.*, Oct. 2007, pp. 1313–1316.

[22] B. T. Khuri-Yakub and Ö. Oralkan, "Capacitive micromachined ultrasonic transducers for medical imaging and therapy," *J. Micromech. Microeng.*, vol. 21, no. 5, 2011, Art. no. 054004.

[23] D. M. Mills and L. S. Smith, "Real-time in-vivo imaging with capacitive micromachined ultrasound transducer (cMUT) linear arrays," in *Proc. IEEE Symp. Ultrason.*, Oct. 2003, pp. 568–571.

[24] T. L. Szabo, "Array beamforming," in *Diagnostic Ultrasound Imaging: Inside Out*, 2nd ed., T. L. Szabo, Ed. Boston, MA, USA: Academic, 2014, ch. 7, pp. 209–255.

[25] O. Oralkan et al., "Initial pulse-echo imaging results with one-dimensional capacitive micromachined ultrasonic transducer arrays," in *Proc. IEEE Ultrason. Symp. Int. Symp.*, vol. 1, Oct. 2000, pp. 959–962.

[26] O. Oralkan et al., "Capacitive micromachined ultrasonic transducers: Next-generation arrays for acoustic imaging?" *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 49, no. 11, pp. 1596–1610, Nov. 2002.

[27] G. Caliano, R. Carotenuto, E. Cianci, V. Foglietti, A. Caronti, and M. Pappalardo, "A cMUT linear array used as echographic probe: Fabrication, characterization, and images," in *Proc. IEEE Ultrason. Symp.*, vol. 1, Aug. 2004, pp. 395–398.

[28] G. Caliano et al., "Design, fabrication and characterization of a capacitive micromachined ultrasonic probe for medical imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 12, pp. 2259–2269, Dec. 2005.

[29] B. T. Khuri-Yakub et al., "Miniaturized ultrasound imaging probes enabled by CMUT arrays with integrated frontend electronic circuits," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol. (EMBC)*, Aug. 2010, pp. 5987–5990.

[30] A. Bhuyan, J. W. Choe, B. C. Lee, P. Cristman, O. Oralkan, and B. T. Khuri-Yakub, "Miniaturized, wearable, ultrasound probe for on-demand ultrasound screening," in *Proc. IEEE Int. Ultrason. Symp.*, Oct. 2011, pp. 1060–1063.

[31] A. S. Savoia, G. Caliano, and M. Pappalardo, "A CMUT probe for medical ultrasonography: From microfabrication to system integration," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 59, no. 6, pp. 1127–1138, Jun. 2012.

[32] D. Gross, C. Coutier, M. Legros, A. Bouakaz, and D. Certon, "A cMUT probe for ultrasound-guided focused ultrasound targeted therapy," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 62, no. 6, pp. 1145–1160, Jun. 2015.

[33] D. Zhao, S. Zhuang, and R. Daigle, "A commercialized high frequency CMUT probe for medical ultrasound imaging," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2015, pp. 1–4.

[34] J. L. Sanders et al., "A handheld 1D transparent CMUT array probe for photoacoustic imaging: Preliminary results," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Sep. 2017, pp. 1–4.

[35] T. Otake, H. Tanaka, A. Sako, M. Fukada, K. Imagawa, and M. Sato, "Development of 4G CMUT (CMUT linear SML44 probe)," *Adv. Ultrasound Diagnosis Therapy*, vol. 4, no. 4, pp. 379–382, 2020.

[36] A. Sampaleanu, P. Zhang, A. Kshirsagar, W. Moussa, and R. J. Zemp, "Top-orthogonal-to-bottom-electrode (TOBE) CMUT arrays for 3-D ultrasound imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 61, no. 2, pp. 266–276, Feb. 2014.

[37] R. K. W. Chee, A. Sampaleanu, D. Rishi, and R. J. Zemp, "Top orthogonal to bottom electrode (TOBE) 2-D CMUT arrays for 3-D photoacoustic imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 61, no. 8, pp. 1393–1395, Aug. 2014.

[38] A. Havreland, M. Ommen, C. Silvestre, M. Engholm, J. Jensen, and E. Thomsen, "BCB polymer based row-column addressed CMUT," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Sep. 2017, pp. 1–4.

[39] A. K. Ilkhechi, C. Ceroici, Z. Li, and R. Zemp, "Transparent capacitive micromachined ultrasonic transducer (CMUT) arrays for real-time photoacoustic applications," *Opt. Exp.*, vol. 28, no. 9, pp. 13750–13760, Apr. 2020.

[40] X. Zhuang, I. O. Wygant, D. S. Lin, M. Kupnik, O. Oralkan, and B. T. Khuri-Yakub, "Wafer-bonded 2-D CMUT arrays incorporating through-wafer trench-isolated interconnects with a supporting frame," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 56, no. 1, pp. 182–192, Jan. 2009.

[41] A. S. Logan, L. L. P. Wong, A. I. H. Chen, and J. T. W. Yeow, "A 32×32 element row-column addressed capacitive micromachined ultrasonic transducer," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 58, no. 6, pp. 1266–1271, Jun. 2011.

[42] T. L. Christiansen, M. F. Rasmussen, J. A. Jensen, and E. V. Thomsen, "Row-column addressed 2-D CMUT arrays with integrated apodization," in *Proc. IEEE Int. Ultrason. Symp.*, Sep. 2014, pp. 600–603.

[43] M. Engholm, A. S. Havreland, E. V. Thomsen, C. Beers, B. G. Tomov, and J. A. Jensen, "A row-column-addressed 2D probe with an integrated compound diverging lens," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2018, pp. 1–4.

[44] R. S. Grass, K. Steenberg, A. S. Havreland, M. Engholm, and E. V. Thomsen, "Large scale high voltage 192+192 row-column addressed CMUTs made with anodic bonding," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Sep. 2020, pp. 1–4.

[45] J. L. Sanders et al., "A row-column (RC) addressed 2D capacitive micromachined ultrasonic transducer (CMUT) array on a glass substrate: Preliminary results," in *Proc. 40th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc. (EMBC)*, Jul. 2018, pp. 1–4.

[46] J. L. Sanders, A. O. Biliroglu, X. Wu, O. J. Adelegan, F. Y. Yamaner, and O. Oralkan, "A row-column (RC) addressed 2-D capacitive micromachined ultrasonic transducer (CMUT) array on a glass substrate," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 68, no. 3, pp. 767–776, Mar. 2021.

[47] M. Engholm, H. Bouzari, J. A. Jensen, and E. V. Thomsen, "Capacitive substrate coupling of row-column-addressed 2-D CMUT arrays," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Sep. 2016, pp. 1–4.

[48] A. S. Havreland, M. Engholm, B. G. Tomov, J. A. Jensen, O. Hansen, and E. V. Thomsen, "CMUT electrode resistance design: Modeling and experimental verification by a row-column array," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 66, no. 6, pp. 1110–1118, Jun. 2019.

[49] T. L. Christiansen, M. F. Rasmussen, J. P. Bagge, L. N. Moesner, J. A. Jensen, and E. V. Thomsen, "3-D imaging using row–column-addressed arrays with integrated apodization—Part II: Transducer fabrication and experimental results," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 62, no. 5, pp. 959–971, May 2015.

[50] M. Engholm et al., "A hand-held row-column addressed CMUT probe with integrated electronics for volumetric imaging," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2015, pp. 1–4.

[51] A. S. Havreland, O. Hansen, K. F. Pedersen, M. Engholm, and E. V. Thomsen, "Delay line separation of CMUT elements," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Sep. 2020, pp. 1–4.

[52] R. S. Grass, A. S. Havreland, M. Engholm, J. A. Jensen, and E. V. Thomsen, "188+188 row–column addressed CMUT transducer for super resolution imaging," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2019, pp. 746–749.

[53] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (Prentice-Hall Electronics and VLSI Series). Upper Saddle River, NJ, USA: Prentice-Hall, 2000. [Online]. Available: https://books.google.dk/books?id=TsmmAQAACAAJ

[54] Y. Huang, A. S. Ergun, E. Haeggström, M. H. Badi, and B. T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology," *J. Microelectromech. Syst.*, vol. 12, no. 2, pp. 128–137, Apr. 2003.

[55] K. K. Park, H. J. Lee, M. Kupnik, O. Oralkan, and B. T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with direct wafer-bonding and LOCOS technology," in *Proc. IEEE 21st Int. Conf. Micro Electro Mech. Syst.*, Jan. 2008, pp. 339–342.

[56] C. Kittel, *Introduction to Solid State Physics*. Hoboken, NJ, USA: Wiley, 2004. [Online]. Available: https://books.google.dk/books?id=kym4QgAACAAJ

[57] Z. Li, L. L. P. Wong, A. I. H. Chen, S. Na, J. Sun, and J. T. W. Yeow, "Fabrication of capacitive micromachined ultrasonic transducers based on adhesive wafer bonding technique," *J. Micromech. Microeng.*, vol. 26, no. 11, Nov. 2016, Art. no. 115019.

[58] A. S. Erguri, Y. Huang, X. Zhuang, Ö. Oralkan, G. G. Yarahoglu, and B. T. Khuri-Yakub, "Capacitive micromachined ultrasonic transducers: Fabrication technology," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 12, pp. 2242–2258, Dec. 2005.

[59] F. Y. Yamaner, X. Zhang, and Ö. Oralkan, "A three-mask process for fabricating vacuum-sealed capacitive micromachined ultrasonic transducers using anodic bonding," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 62, no. 5, pp. 972–982, May 2015.

[60] Y. Huang, E. O. Haeggstrom, X. Zhuang, A. S. Ergun, and B. T. Khuri-Yakub, "A solution to the charging problems in capacitive micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 4, pp. 578–580, Apr. 2005.

[61] S. Machida et al., "Analysis of the charging problem in capacitive micro-machined ultrasonic transducers," in *Proc. IEEE Ultrason. Symp.*, Nov. 2008, pp. 383–385.

[62] K. Midtbo and A. Ronnekleiv, "Analysis of charge effects in high frequency CMUTs," in *Proc. IEEE Ultrason. Symp.*, Nov. 2008, pp. 379–382.

[63] M. J. G. Molgaard, J. M. F. Hansen, M. H. Jakobsen, and E. V. Thomsen, "Sensitivity optimization of wafer bonded gravimetric CMUT sensors," *J. Microelectromech. Syst.*, vol. 27, no. 6, pp. 1089–1096, Dec. 2018.

[64] H. Lamb, "On the vibrations of an elastic plate in contact with water," *Proc. Roy. Soc. London A, Containing Papers Math. Phys. Character*, vol. 98, no. 690, pp. 205–216, 1920.

[65] M. Amabili and M. K. Kwak, "Free vibrations of circular plates coupled with liquids: Revising the Lamb problem," *J. Fluids Struct.*, vol. 10, no. 7, pp. 743–761, Oct. 1996.

[66] B. Chang, P. Leussink, F. Jensen, J. Hübner, and H. Jansen, "DREM: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed Bosch DRIE process," *Microelectron. Eng.*, vol. 191, pp. 77–83, May 2018.

[67] A. S. Havreland, M. Engholm, R. S. Grass, J. Arendt Jensen, and E. V. Thomsen, "Wafer bonded CMUT technology utilizing a poly-silicon-on-insulator wafer," in *Proc. IEEE Int. Ultrason. Symp. (IUS)*, Oct. 2019, pp. 758–761.

[68] Microchemicals GmbH. *Aluminium Etching*. Accessed: Sep. 16, 2020. [Online]. Available: https://www.microchemicals.com/technical_information/aluminium_etching.pdf

[69] M. F. la Cour, M. B. Stuart, M. B. Laursen, S. E. Diederichsen, E. V. Thomsen, and J. A. Jensen, "Investigation of PDMS as coating on CMUTs for imaging," in *Proc. IEEE Int. Ultrason. Symp.*, Sep. 2014, pp. 2584–2587.

[70] *Medical Electrical Equipment—Part 2–27: Particular Requirements for the Basic Safety and Essential Performance of Ultrasonic Medical Diagnostic and Monitoring Equipment*, document DS/EN 60601-2-37:201.11.1.3.1, May 2008.

[71] J. A. Jensen et al., "SARUS: A synthetic aperture real-time ultrasound system," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 60, no. 9, pp. 1838–1852, Sep. 2013.

[72] J. A. Jensen et al., "Safety assessment of advanced imaging sequences I: Measurements," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 63, no. 1, pp. 110–119, Jan. 2016.

[73] J. A. Jensen, "Safety assessment of advanced imaging sequences II: Simulations," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 63, no. 1, pp. 120–127, Jan. 2016.

[74] M. L. Ommen, M. Schou, C. Beers, J. A. Jensen, N. B. Larsen, and E. V. Thomsen, "3D printed calibration micro-phantoms for super-resolution ultrasound imaging validation," *Ultrasonics*, vol. 114, Jul. 2021, Art. no. 106353.

[75] A. S. Havreland, "Micromachined integrated 2D transducers for ultrasound imaging," Ph.D. thesis, Dept. Health Technol., Tech. Univ. Denmark (DTU), Lyngby, Denmark, 2019.

RUNE SIXTEN GRASS (Member, IEEE) received the B.Sc. and M.Sc. degrees in physics and nanotechnology engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2016 and 2018, respectively, where he is currently pursuing the Ph.D. degree with the Department of Health Technology. His current research interests include micro and nanofabrication in general, in particular the development and fabrication of capacitive michomachined ultrasonic transducers (CMUTs) for super-resolution and 3-D imaging.

MATHIAS ENGHOLM received the B.Sc. and M.Sc. degrees in engineering physics and nanotechnology and the Ph.D. degree with a focus on micromachined ultrasonic transducers for 3-D imaging from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2012, 2015, and 2018, respectively. He worked as a Post-Doctoral Researcher at the Technical University of Denmark until 2020. His research interests include all facets of ultrasonic imaging transducers.

ANDREAS SPANDET HAVRELAND received the B.Sc. and M.Sc. degrees in engineering physics and nanotechnology and the Ph.D. degree with focus on development of CMUTs (capacitive micromachined ultrasonic transducers) for three-dimensional imaging from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2014, 2016, and 2020, respectively. He is currently working as an Engineer at Höttinger Brüel & Kjaer (HBK), where he is developing accelerometers.

CHRISTOPHER BEERS (Member, IEEE) received the M.S. degree in acoustics from Pennsylvania State University, State College, PA, USA, in 2007. His M.S. thesis research explored end-element anomalies in medical ultrasound transducer arrays. He has been with BK Medical (formerly Sound Technology), State College, since 2007, where he has been developing transducer technology and designs commercial medical ultrasound probes.

MARTIN LIND OMMEN received the M.Sc. and Ph.D. degrees in physics and nanotechnology from the Biomedical Engineering Section, Department of Health Technology, Technical University of Denmark, Kongens Lyngby, Denmark, in 2017 and 2020, respectively. His work consists of fabrication capacitive micromachined ultrasonic transducers (CMUTs), and ultrasound phantom fabrication, using stereolithographic 3D printing to create micro flow and scatter phantoms with a current focus on stereolithographic fabrication of microflow and scatter phantoms.

STINE LØVHOLT GRUE PEDERSEN (Graduate Student Member, IEEE) received the M.Sc. degree in physics and nanotechnology from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2019, where she is currently pursuing the Ph.D. degree with the Ultrasound and Biomechanics Section, Department of Health Technology. Her current research interests include microstructure fabrication in general, and in particular the fabrication of capacitive micromachined ultrasonic transducers (CMUTs), as well as analytic and simulation studies of the theory behind.

LARS NORDAHL MOESNER was born in 1964. He received the M.Sc. degree in electronics engineering from the Technical University of Denmark (DTU) in 1989. He was employed by Bruel & Kjaer in 1989. He started as a Technical Writer but quickly moved on the Development Department, writing embedded software with Bruel & Kjaer's Ultrasound Division. He continued as a Hardware Designer with BK Medical after Analogic Corporation's acquisition, primarily working with digital hardware and FPGA firmware. After a two-year detour to the telecom industry, he was re-employed as a Hardware Architect with BK Medical in 2001 and is currently a part of BK Medical's Research and Development Applications and Technologies (RDAT) Group.

MATTHIAS BO STUART received the M.Sc. and Ph.D. degrees in computer engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2006 and 2010, respectively. He worked as an Associate Professor with the Biomedical Engineering Section, Department of Health Technology, Technical University of Denmark, until 2022. His research interests include synthetic aperture methods for both anatomical and flow imaging in both 2-D and 3-D, ultrasound systems, and real-time implementations of ultrasound processing algorithms.

MUDABBIR TUFAIL BHATTI (Student Member, IEEE) received the M.Sc. degree in biomedical engineering from the Aachen University of Applied Sciences, Aachen, Germany, in 2019. He is currently pursuing the Ph.D. degree with the Center for Fast Ultrasound Imaging, Department of Health Technology, Technical University of Denmark. His research interests include coded ultrasound imaging.

BORISLAV G. TOMOV received the M.Sc. degree in electronics engineering from the Technical University of Sofia, Sofia, Bulgaria, in 1996, and the Ph.D. degree in medical electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2003. He is currently a Senior Researcher with the Center for Fast Ultrasound Imaging, Department of Health Technology, Technical University of Denmark. His research interests include medical ultrasound signal processing and ultrasound scanner architectures and implementations.

JØRGEN ARENDT JENSEN (Fellow, IEEE) received the Master of Science, Ph.D., and Dr.Techn. degrees in electrical engineering from the Technical University of Denmark in 1985, 1989, and 1996, respectively. Since 1993, he has been a Full Professor of biomedical signal processing with the Department of Health Technology, Technical University of Denmark. He has been the Head of the Center for Fast Ultrasound Imaging since its inauguration in 1998. He is also the Developer and Maintainer of the Field II Simulation Program. He has been a Visiting Scientist at Duke University, Stanford University, and the University of Illinois at Urbana–Champaign. He was the Head of the Biomedical Engineering Group from 2007 to 2010. In 2003, he was one of the Founders of the Biomedical Engineering Program in Medicine and Technology, which is a Joint Degree Program between the Technical University of Denmark and the Faculty of Health and Medical Sciences, University of Copenhagen. The degree is one of the most sought-after engineering degrees in Denmark. He was the Chairperson of the study board from 2003 to 2010 and an Adjunct Professor with the University of Copenhagen from 2005 to 2010. He has given a number of short courses on simulation, synthetic aperture imaging, and flow estimation at international scientific conferences and teaches biomedical signal processing and medical imaging at the Technical University of Denmark. He has published more than 500 journals and conference papers on signal processing and medical ultrasound and the book *Estimation of Blood Velocities Using Ultrasound* (Cambridge University Press, 1996). His research interests include simulation of ultrasound imaging, synthetic aperture imaging, vector blood flow estimation, construction of ultrasound research systems, and 3-D super resolution imaging. He has given more than 60 invited talks at international meetings and received several awards for his research, most recently the Grand Solutions Prize from the Danish Minister of Science, the Order of Dannebrog by his Majesty the Queen of Denmark, and the Rayleigh Award from the IEEE UFFC.

ERIK VILAIN THOMSEN (Member, IEEE) was born in Aarhus, Denmark, in 1964. He received the M.Sc. degree in physics from the University of Southern Denmark, Odense, Denmark, in 1992, and the Ph.D. degree in electrical engineering from the Technical University of Denmark (DTU), Kongens Lyngby, Denmark, in 1998.

He is currently a Professor with the Department of Health Technology, DTU, where he is also the Head of the MEMS Applied Sensors Group and the Head of the Division with responsibility for the education in healthcare engineering. He teaches classes in solid-state electronics, microtechnology, and nanofabrication and microfabrication. His current research interests include all aspects of capacitive micromachined ultrasonic transducers (CMUTs), general MEMS technology, and piezoelectric MEMS.

Dr. Thomsen received the Danish National Advanced Technology Foundation's Grand Solution Prize in 2017, the AEG Electron Prize in 1995, and several teaching awards at DTU.

APPENDIX D

OnScale Simulations

OnScale simulation results for a single CMUT cell with a radius of 22.3 µm and a plate thickness of 4.5 µm.

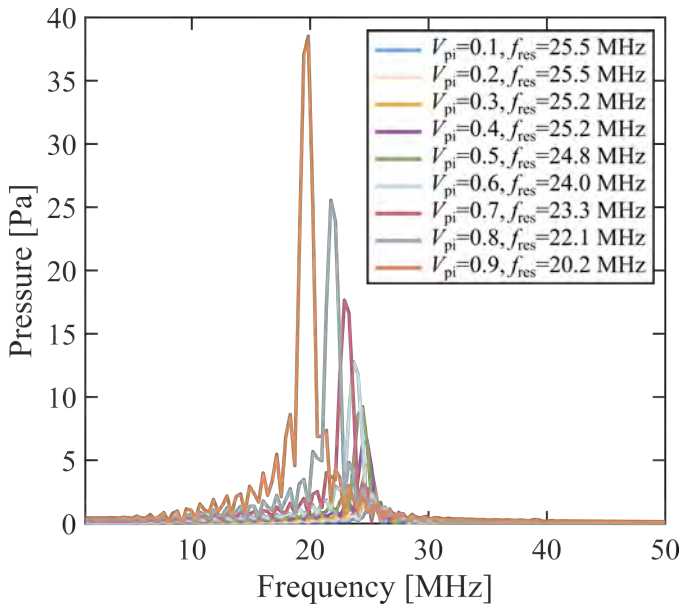


Figure D.1: OnScale simulation results for a CMUT cell with a radius of 22.3 µm and a plate thickness of 4.5 µm. The figure shows the output pressure in air without applied PDMS for varying applied potentials.

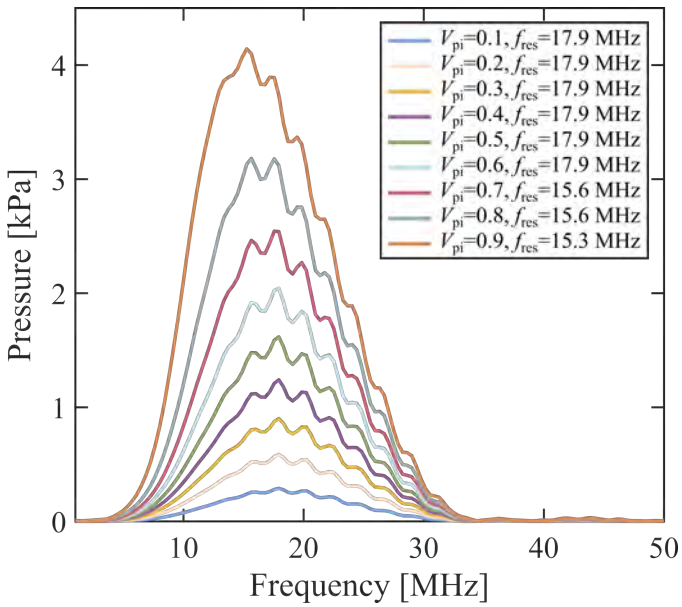


Figure D.2: OnScale simulation results for a CMUT cell with a radius of 22.3 µm and a plate thickness of 4.5 µm. The figure shows the output pressure in air after PDMS casting for varying applied potentials.

APPENDIX E

Mask Layout LapMUT

E.1 LapMUT-A Design

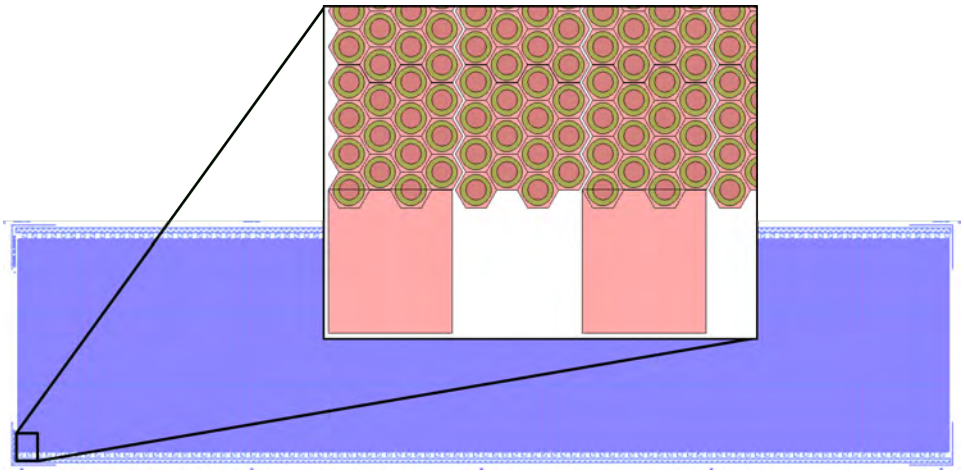
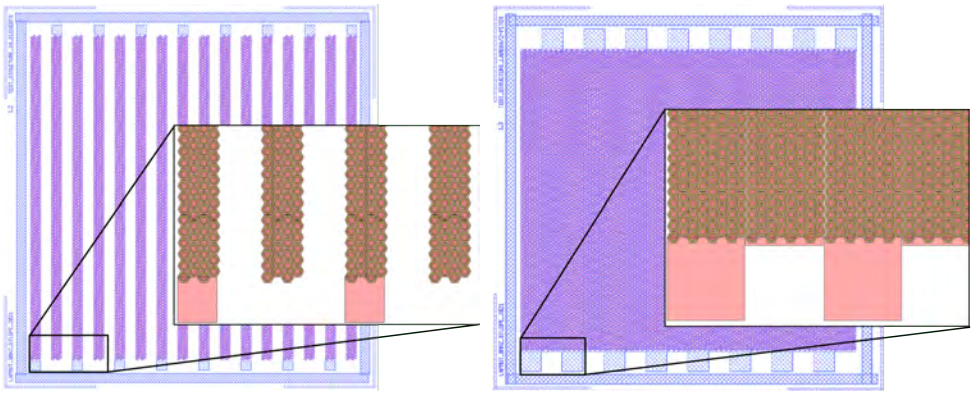


Figure E.1: Illustration of the linear array comprising 192 elements with LapMUT-A relative to the stated criteria, with a close-up showing the cell packaging.



(a) **(b)**

Figure E.2: Images depicting the design of (a) the *Single* test array and (b) the *Filled* test array. Both designs are developed based on the bond pad pitch of a pre-existing CCB. The two close-ups shows the cell packaging.

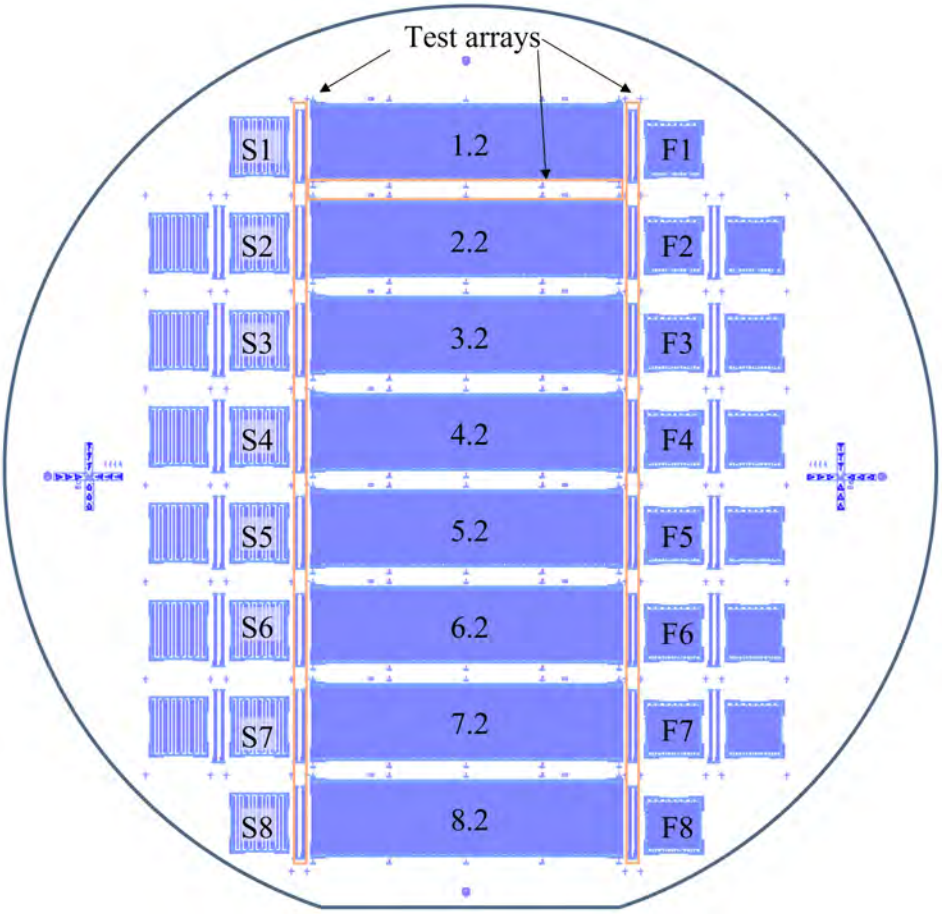


Figure E.3: Overview of the wafer map and naming convention employed for the 192 element transducer design with the design LapMUT-A for the laparoscopic probe.

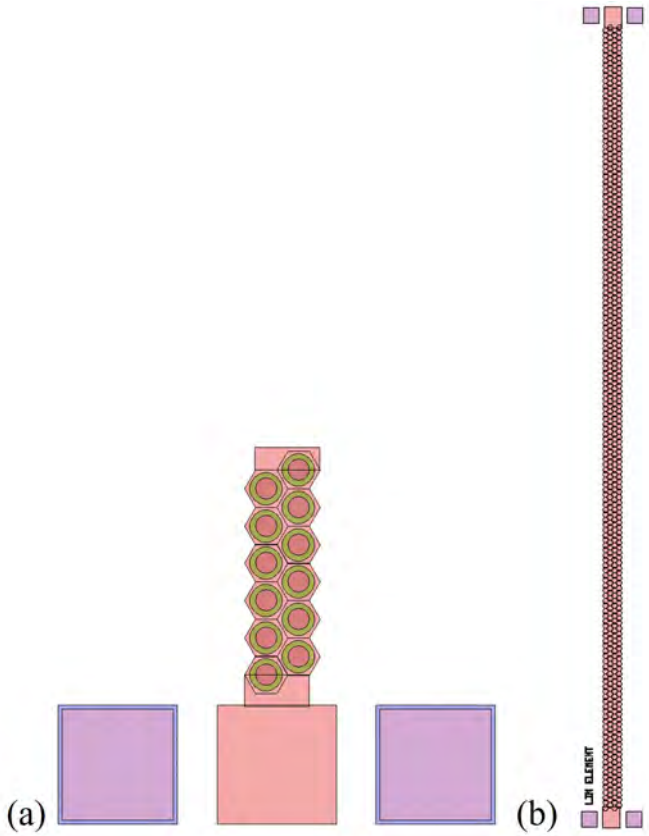


Figure E.4: Illustration of the two types of test elements added to the mask layout. (a) Shows the twelve-cell test array located around the large transducer arrays, while (b) shows a test element identical to a single element from the 192 element array. These are located around the center column.

E.2 LapMUT-B Design

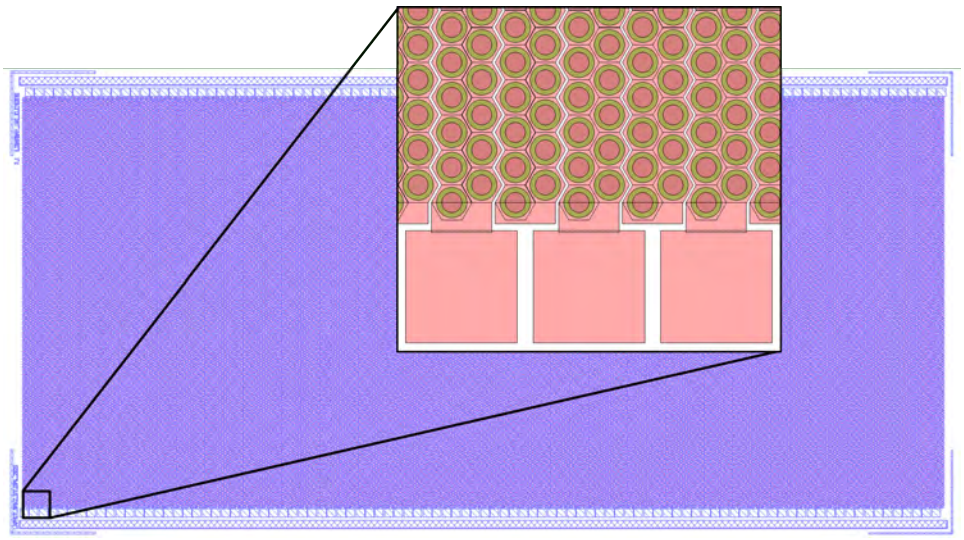
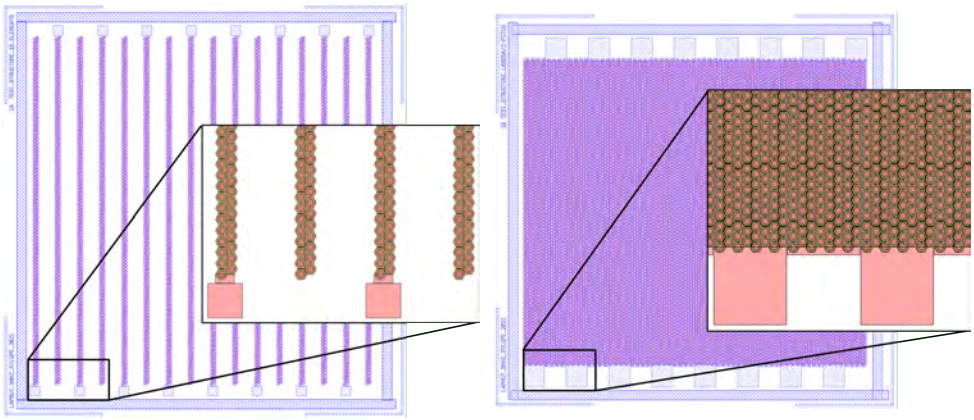


Figure E.5: Illustration of the linear array comprising 192 elements with LapMUT-B design, and a close-up showing the cell packaging.



(a) **(b)**

Figure E.6: Images depicting the design of (a) the *Single* test array and (b) the *Filled* test array. Both designs are developed based on the bond pad pitch of a pre-existing CCB. The two close-ups shows the cell packaging.

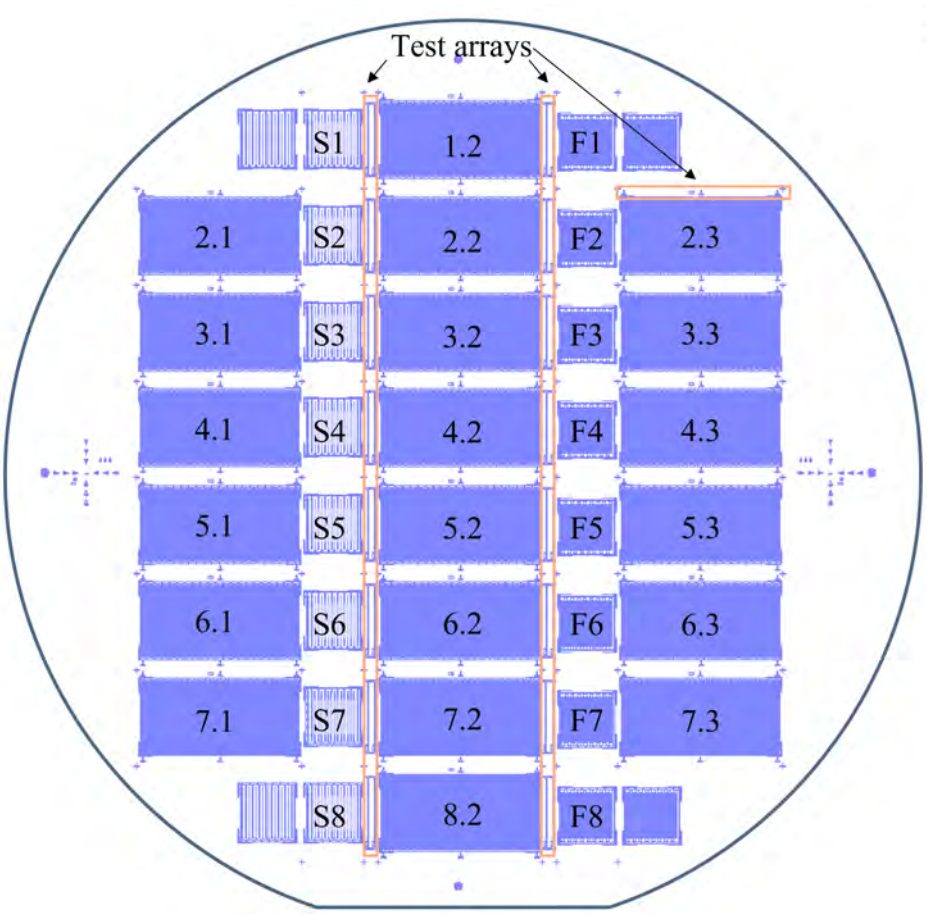


Figure E.7: Overview of the wafer map and naming convention employed for the 192 element transducer design for the laparoscopic probe with the design LapMUT-B.

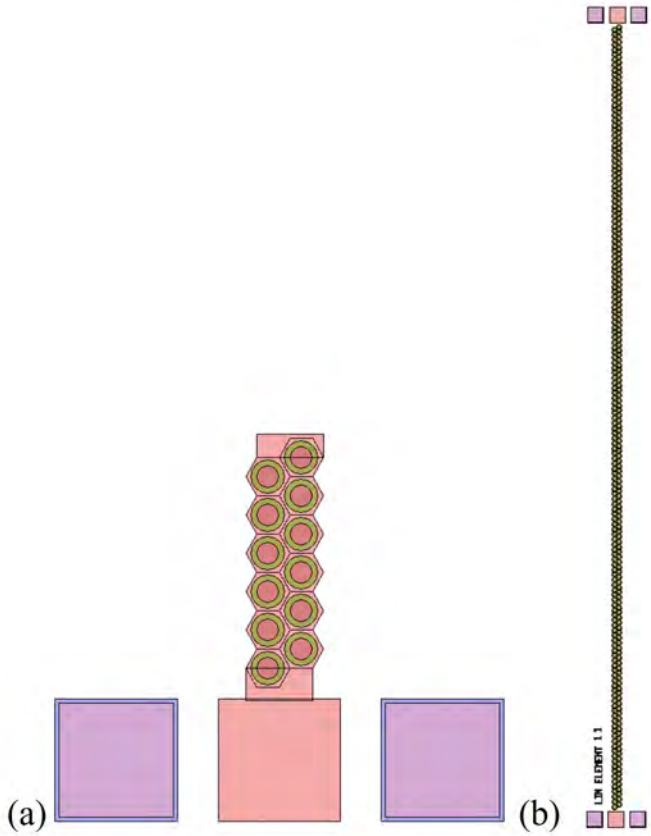


Figure E.8: Illustration of the two types of test elements added to the mask layout. (a) Shows the five-cell test array located around the large transducer arrays, while (b) shows a test element identical to a single element from the 384 element array. These are located around the center column.

APPENDIX F

Athena Oxidation Models Study

Athena (Silvaco, CA, USA) has two main built-in oxidation models. One employs a *compressed* model and the other one a *viscous* model. Based on the user manual [110] the *compressed* model is "recommended for simulations of planar and non-planar structures, where stress effects play a minor role in determining the oxide shape." Whereas the *viscous* model is used "when stress effects are important. The model calculates stresses in the growing oxide and creates almost the same shape for the silicon/oxide interface as does the *compress* model".

The *compressed* model was employed by the command

```
method compress.
```

For the viscous model, the following optimized code was utilized

```
material oxide visc.0=5.1 visc.E=3.48;
material nitride visc.0=5.96e5 visc.E=2.5625.
```

The two oxidation models were examined through two studies, all focusing on a single LOCOS structure. In the first study, the thickness of the deposited nitride was varied. The insulting oxide layer had a thickness of 400 nm, the LOCOS step was carried out at an oxidation temperature of 1100 °C. The target gap height was set to 150 nm. The nitride thickness was varied from 40 nm and to 200 nm, to investigate the influence of stress caused by thicker nitride layers.

Fig. F.1 verifies the results described in Section 3.3, showing a thicker nitride layer resulted in a higher peak relative to the oxide surface. However, no significant difference between the two oxidation models was observed, regardless of the nitride thickness. Additionally, the simulation times for both

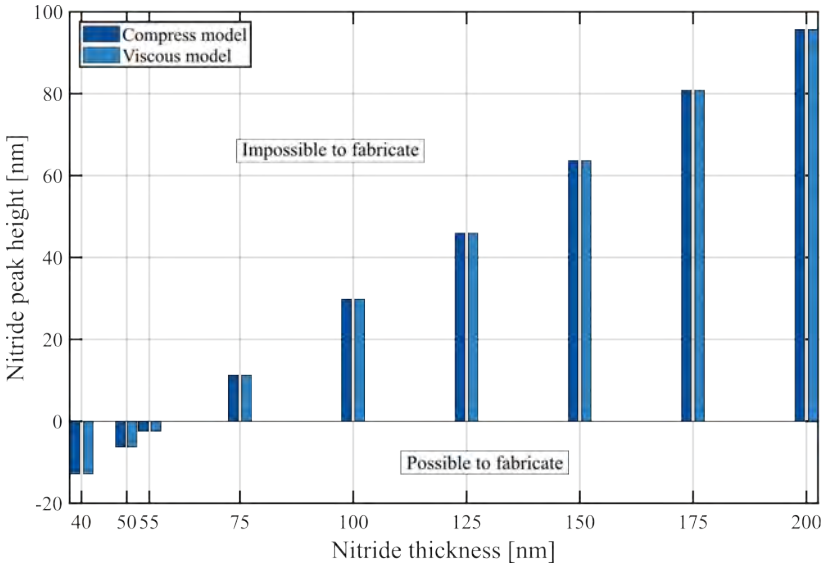


Figure F.1: Study of the *compressed* oxidation model compared with the *viscous* model for varying nitride thicknesses. The insulating oxide height was 400 nm and the oxidation temperature was 1100 °C.

models were approximately the same, making them both applicable for this purpose.

The second study investigated the impact of the applied oxidation model on the oxidation temperature. The simulations were conducted using 400 nm insulation oxide and a target gap height of 150 nm. Two different nitride thicknesses, 40 nm and 55 nm, were considered in this study.

Fig. F.2 shows the nitride peak height relative to the oxidation temperature for a deposited nitride thickness of 40 nm. It can be seen that the nitride peak height decreases with higher temperature. However, fabrication remains feasible at all temperatures, consistent with the findings discussed in Section 3.3. Furthermore, small differences between the model results can be observed, however, both models exhibit the same tendency of decreasing nitride peak height with increasing temperature. Therefore, it can be concluded that the choice of model has no impact for this geometry.

In the last study, a nitride thickness of 55 nm was employed. Fig. F.3 shows variations in nitride peak height depending on the oxidation temperature. The y-axis scale indicates small variations, and no definitive conclusion can be drawn regarding the fabrication feasibility of these processes.

However, the results indicate that, for a gap height of 150 nm and an insulating oxide thickness of 400 nm, a nitride layer of 55 nm represents the boundary of feasibility. Furthermore, the results suggest that the oxidation temperature can be used for fine adjustments when the other parameters

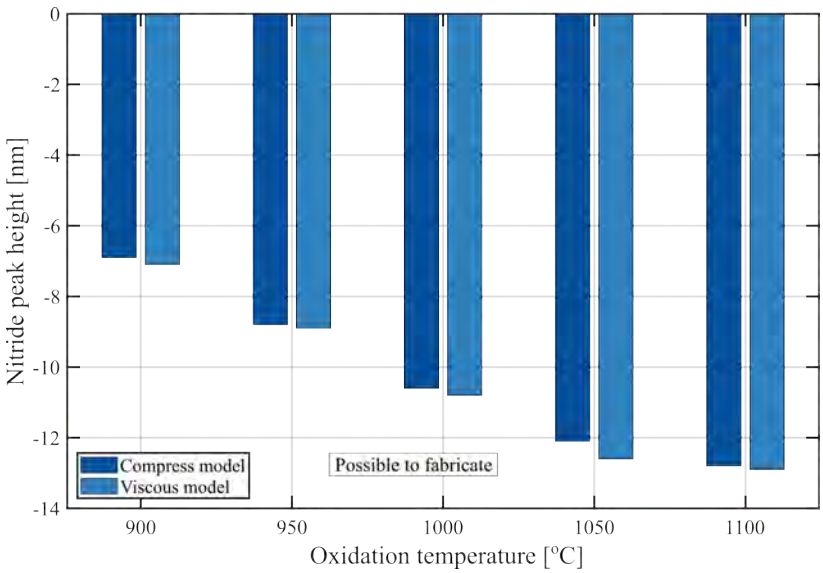


Figure F.2: Study of the *compressed* oxidation model compared with the *viscous* model for varying oxidation temperatures. The insulating oxide thickness was 400 nm, while the nitride thickness was 40 nm.

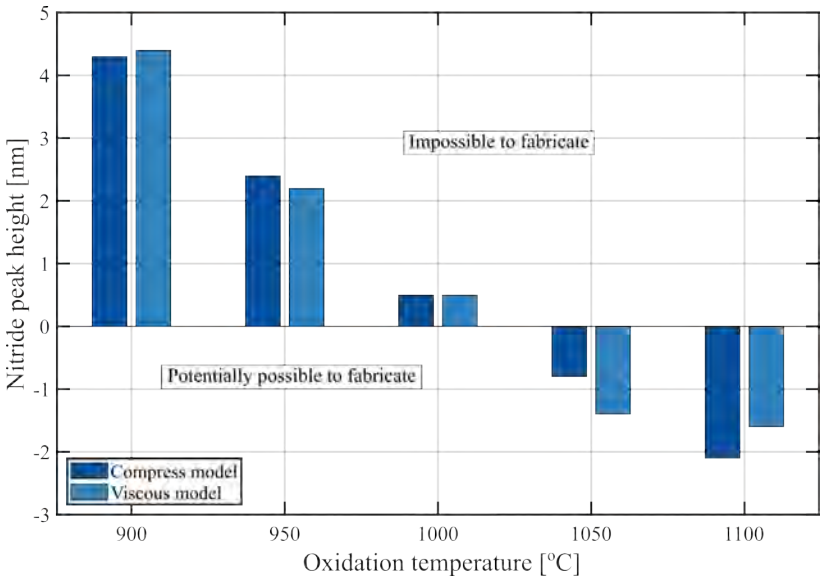


Figure F.3: Study of the *compressed* oxidation model compared with the *viscous* model for varying oxidation temperatures. The insulating oxide thickness was 400 nm, while the nitride thickness was 55 nm.

are in a gray-zone. Comparing the two models reveals small variations, but both models exhibit the same tendency and do not impact the general conclusion on the fabrication feasibility.

In conclusion, when comparing the two models for this single LOCOS structure with these dimensions, no significant differences were observed, and both models can be confidently utilized.

APPENDIX G

Oxide Thickness

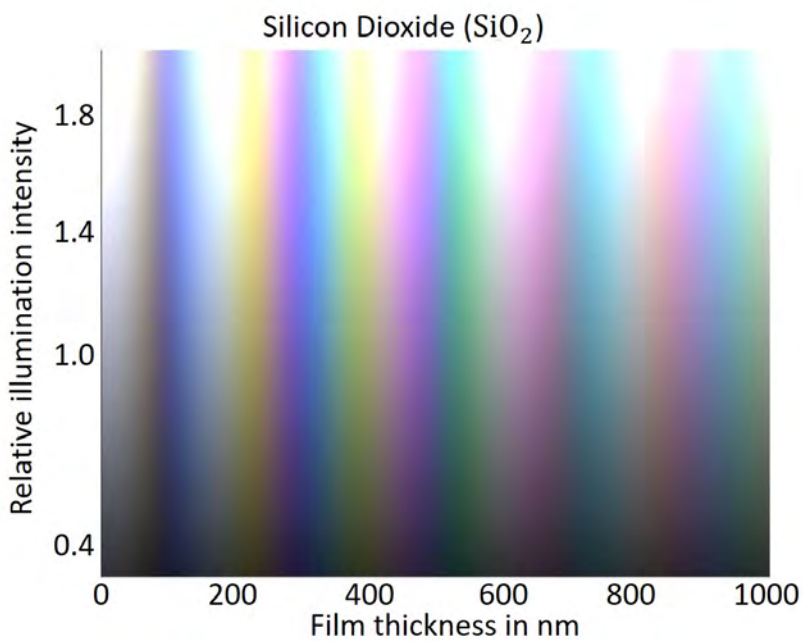


Figure G.1: Color chart defining the film thickness of silicon dioxide. The chart is reprinted from [111].

APPENDIX H

Characterization: Results

H.1 Maskless LOCOS Wafer

Table H.1: Summary of the visual inspection of the *Single* design test arrays from the maskless LOCOS wafer. Only one array, marked in gray, was discarded for further characterization.

Array no.	Error	Array no.	Error
S1	-	S8	-
S2	E1	S9	-
S3	-	S10	-
S4	-	S11	-
S5	-	S12	-
S6	-	S13	E5
S7	-		

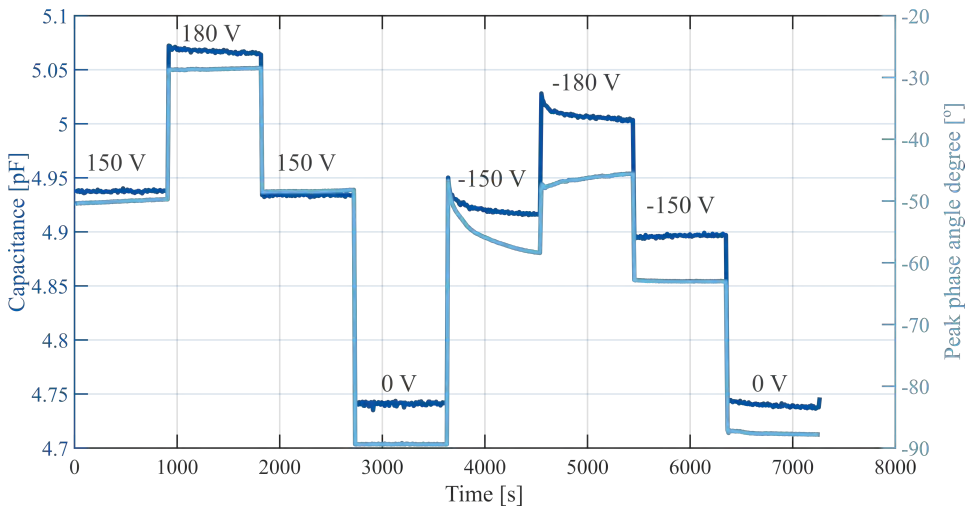


Figure H.1: Stability plot obtained from array 4.3 on the maskless LOCOS wafer, element number 85. Initially a negative bias was applied, followed by a positive bias. The peak phase angle and the slope capacitance are derived over time.

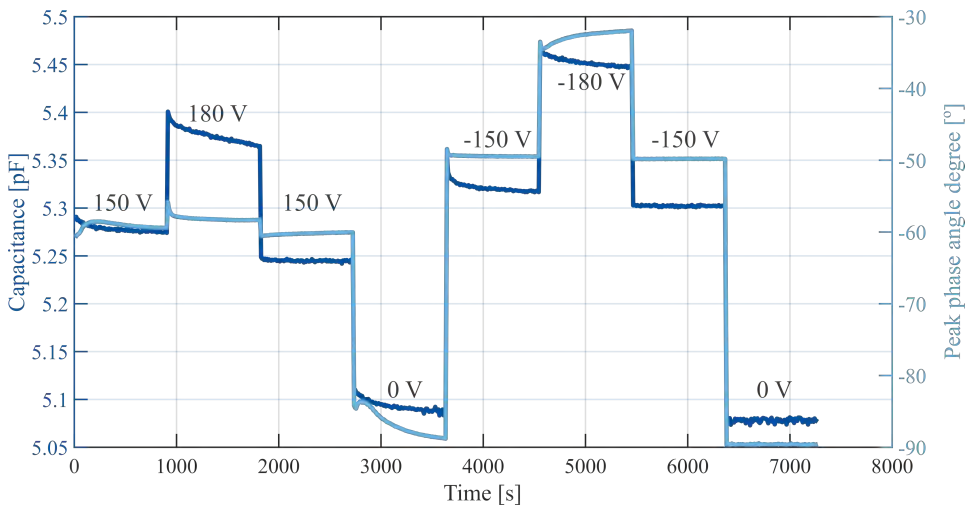


Figure H.2: Stability plot obtained from array S10 on the maskless LOCOS wafer, element number 8. Initially a positive bias was applied, followed by a negative bias. The peak phase angle and the slope capacitance are derived over time.

Table H.2: Summary of the visual inspection of the *Filled* design test arrays from the maskless LOCOS wafer. Five arrays, marked in gray, were discarded for further characterization.

Array no.	Error	Array no.	Error
F1	E1	F8	-
F2	E1	F9	-
F3	-	F10	-
F4	-	F11	E2
F5	-	F12	E2
F6	E5	F13	E2
F7	-		

Table H.3: Summery of the number of elements per array with a capacitance $C_\mathrm{p} < 4\,\mathrm{pF}$ or $C_\mathrm{p} > 5\,\mathrm{pF}$, which aberrates from the acceptance range. The data are from the maskless LOCOS wafer.

Array no.	Number of elements	Array no.	Number of elements
1.2	0	6.3	0
2.2	0	7.2	2
3.1	0	8.2	2
3.2	3	8.3	2
4.1	3	9.2	2
4.2	1	9.3	0
4.3	0	10.2	2
5.2	0	10.3	57
5.3	0	11.2	9
6.2	6	Total:	89 elements

Table H.4: Summary of the elements showing aberrating behavior from the voltage measurements. Differencies between the first and the second measurement is mapped. The data are from array 4.3 on the maskless LOCOS wafer.

Element #	**Visually found**	**High C** (before/after)	**High I** (before/after)
6	No	No/No	Yes/No
8	Yes	Yes/Yes	Yes/No
10	Yes	Yes/Yes	No/No
111	Yes	No/No	Yes/Yes
113	Yes	No/No	Yes/Yes
249	Yes	Yes/Yes	No/No
251	Yes	Yes/Yes	No/No
358	Yes	No/No	No/Yes
359	Yes	No/No	Yes/Yes
360	Yes	No/No	Yes/Yes
361	Yes	No/No	Yes/Yes
362	Yes	Yes/No	No/No
381	Yes	No/Yes	Yes/No
383	Yes	No/Yes	Yes/Yes

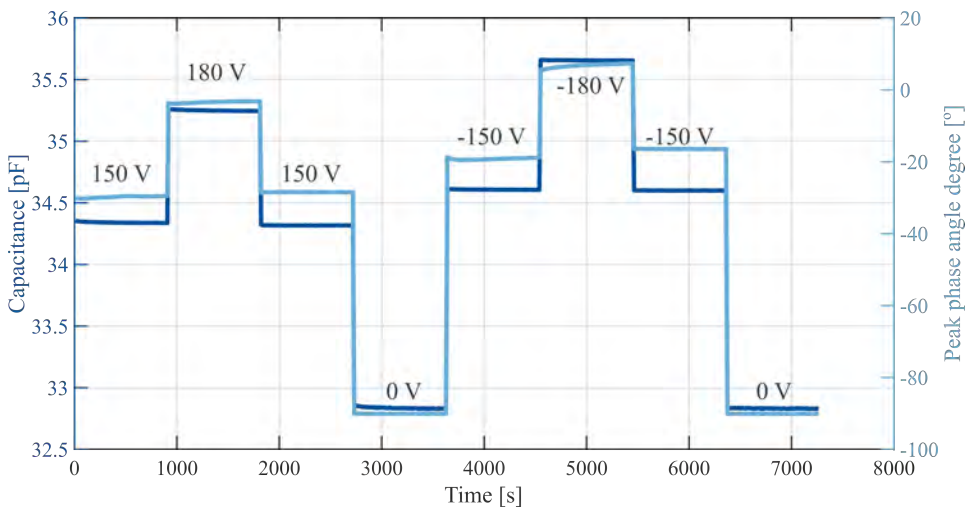


Figure H.3: Stability plot obtained from array F10 on the maskless LOCOS wafer, element number 8. Initially a positive bias was applied, followed by a negative bias. The peak phase angle and the slope capacitance are derived over time.

H.2 Double LOCOS Wafer

Table H.5: Summery of the number of elements per array with a capacitance $C_\mathrm{p} < 4\,\mathrm{pF}$ or $C_\mathrm{p} > 5\,\mathrm{pF}$, which aberrates from the acceptance range. The data are from the double LOCOS wafer.

Array no.	**Number of elements**	**Array no.**	**Number of elements**
1.2	2	6.3	2
2.2	0	7.2	0
3.1	37	8.2	0
3.2	0	8.3	2
3.3	15	9.3	2
4.2	0	10.2	2
5.2	0	10.3	8
5.3	0	11.2	14
6.1	7	11.3	14
6.2	0	Total:	105 elements

APPENDIX I

Athena Simulation Code

I.1 Single LOCOS Cavity Design

Used for the single LOCOS cavity design elaborated in Section 3.3.

```
go athena
#TITLE: LOCOS for CMUT cavity formation

# Define layer thickness
set tinsulation=0.400
set tfield=0.9
set tnitride=0.055

# Target for gap in Angstroms !!!
set gapTarget=1500

# Oxidation times in minutes
set Initialoxtime=40

# Oxidation temperature in deg. C
set TempLOCOS=1100

# Set read out parameters
set strucCenter = 0
set readOut = -9

# Define mesh in um
set xmin=-10
set xmax=10

# Substrate mesh definition
line y loc=0    spac=0.1
line y loc=0.6  spac=0.5
```

```
line y loc=1

line x loc=-10  spac=1
line x loc=-6   spac=0.1
line x loc=-3   spac=0.1

line x loc=0    spac=1
line x loc=3  spac=0.1
line x loc=6  spac=0.1
line x loc=10   spac=1

# substrate is (100) orientation
init orient=100

# Viscous oxidation for LOCOS process - parameters from Silvaco
    material on LOCOS
material oxide visc.0=5.1 visc.E=3.48
material nitride visc.0=5.96e5 visc.E=2.5625
# Compressed oxidation model
#method compress

structure outfile=LOCOS_01.str

# Grow pad oxide
method fermi

deposit oxide thickness=$tinsulation
structure outfile=LOCOS_02.str

extract name="T_oxide_pad" thickness oxide mat.occno=1 x.val=
    $strucCenter
extract name="T_silicon_pad" thickness silicon mat.occno=1 x.
    val=$strucCenter

# Deposit & Pad nitride mask
deposit nitride thick=$tnitride
structure outfile=LOCOS_03.str

# Define cell
etch    nitride left p1.x=-5
etch    nitride right p1.x=5
structure outfile=LOCOS_04.str

# Field oxidation with structure file output for movie
method fermi

# LOCOS oxidation
# Run LOCOS until the gap is ok
# Uses an adaptive timestep

set tgap = 0     # Current gap height
set tpost = 0    # Current post height
set stepLOCOS = 0  # Number of oxidation steps
set timestepLOCOS=1      # Initial time step in minutes
```

```
set minimumTimestep=0.2  # Minimum time step

set timeLOCOS=$Initialoxtime

# Grow thick oxide
diffuse time=$Initialoxtime temp=$TempLOCOS wetO2 pres=1
structure outfile=LOCOS_05.str

# find current thickness of oxide
  extract name="t_ox_post" thickness material="oxide" mat.occno
    =1 x.val=$readOut
  extract name="t_si_post" thickness material="silicon" mat.
    occno=1 x.val=$readOut
  extract name="t_si_insulation" thickness material="silicon"
    mat.occno=1 x.val=$strucCenter
  extract name="t_ox_isolation" thickness material="oxide" mat.
    occno=1 x.val=$strucCenter
  extract name="t_nitride" thickness material="nitride" mat.
    occno=1 x.val=$strucCenter
  extract name="gap" $t_ox_post+$t_si_post-($t_ox_isolation+
    $t_si_insulation+$t_nitride)

# Loop with small step to reach gap
loop steps = 1000 print
 # initial oxidation
  diffuse time=$timestepLOCOS temp=$TempLOCOS wetO2 pres=1

 # calculate cummulative oxidation time
  set timeLOCOS=$timeLOCOS + $timestepLOCOS

 # find current thickness of oxide
  extract name="t_ox_post" thickness material="oxide" mat.occno
    =1 x.val=$readOut
  extract name="t_si_post" thickness material="silicon" mat.
    occno=1 x.val=$readOut
  extract name="t_si_insulation" thickness material="silicon"
    mat.occno=1 x.val=$strucCenter
  extract name="t_ox_isolation" thickness material="oxide" mat.
    occno=1 x.val=$strucCenter
  extract name="t_nitride" thickness material="nitride" mat.
    occno=1 x.val=$strucCenter
  extract name="gap" $t_ox_post+$t_si_post-($t_ox_isolation+
    $t_si_insulation+$t_nitride)

  # calculate change in gap thickness since previous step
 set deltagap = ($gap - $tgap)
 set deltapost = ($t_ox_post - $tpost)

 # calculate the post oxide growth rate (Angstrom/min)
 set rate = $deltapost / $timestepLOCOS

 # calculate how much gap we still need to grow (Angstrom)
  set missingpost = ($gapTarget - $gap)

```

```
 # estimate new timestep - add 0.1 min to ensure that we do not get stuck in an infinite loop
  set timestepLOCOS=$missingpost/$rate

 # Avoid to small time steps
  if cond = ($timestepLOCOS < $minimumTimestep)
    set timestepLOCOS = $minimumTimestep
  if.end

 # save current thickness of gap and post oxide
  set tgap =  $gap
  set tpost = $t_ox_post

 # check if we have reached desired gap height and leave the loop if this is the case
  if cond = ($gap > $gapTarget)
    l.modify break
  if.end
l.end
structure outfile=LOCOS_06.str

# Remove the nitride
strip nitride
structure outfile=LOCOS_07.str

# Extract CMUT characteristics
extract name="T_oxide_field" thickness oxide mat.occno=1 x.val=$readOut
extract name="T_silicon_field" thickness silicon mat.occno=1 x.val=$readOut
extract name="T_oxide_pad2" thickness oxide mat.occno=1 x.val=$strucCenter
extract name="T_silicon_pad2" thickness silicon mat.occno=1 x.val=$strucCenter
extract $T_silicon_pad-$T_silicon_field
extract name="gap" $T_oxide_field-$T_oxide_pad-$T_silicon_pad+$T_silicon_field

# Plot all structure files

# tonyplot -st LOCOS_*.str
# tonyplot -st LOCOS_05.str
tonyplot -st LOCOS_06.str

# Extract the surface of the nitride, oxide and silicon regions
Go internal

# As infile we use structure with the nitride still on
Extract init infile="LOCOS_06.str"

# set x-axis starting point [um]
set ibegin=$xmin

# set resolution - number of points per micron (std er 100)
```

```
set res=100

# set length along x-axis [um]
set length=$xmax-$xmin

# Extract top most silicon layer - notice that "min_y" corresponds to surface
# Delete file surface_silicon.dat before use else results will be appended
set i=$ibegin
loop steps=$res*$length
extract name="min_y" min.bound material="silicon" x.val=$i mat.occno=1 datafile="surface_silicon.dat"
set i=1/$res+$i
l.end

# Extract top most oxide layer - notice that "min_y" corresponds to surface
# Delete file surface_oxide.dat before use else results will be appended
set i=$ibegin
loop steps=$res*$length
extract name="min_y" min.bound material="oxide" x.val=$i mat.occno=1 datafile="surface_oxide.dat"
set i=1/$res+$i
l.end

# Extract top most nitride layer - notice that "min_y" corresponds to surface
# Delete file surface_nitride.dat before use else results will be appended
set i=$ibegin
loop steps=$res*$length
extract name="min_y" min.bound material="nitride" x.val=$i mat.occno=1 datafile="surface_nitride.dat"
set i=1/$res+$i
l.end

quit
```

I.2 Double LOCOS Process

Used for fabrication feasibility check applying the design parameters. Furthermore, it was used for the cavity study elaborated in Section 3.4.

```
go athena

# Define grid
line x loc=-12 spac=0.05
line x loc=0  spac=0.05
line x loc=8  spac=0.05

line y loc=0 spac=0.012
line y loc=1 spac=0.2
line y loc=3 spac=2

# Define substrate
init silicon orient=100 c.boron=1E14
struct outf=2xLOCOS_00.str

material oxide visc.0=5.1 visc.E=3.48
material nitride visc.0=5.96e5 visc.E=2.5625

method viscous
oxide STRESS.DEP=t

# Step 1: Make a thick oxide
# We use deposit to save calculation time.
# In real lift this step would be a thernal oxidation.
# Thickness in um
#First LOCOS:
#Oxide
deposit oxide thick=0.1
struct outf=2xLOCOS_01.str

# Deposit & Pad nitride mask
deposit nitride thick=0.055
structure outf=2xLOCOS_02.str

# Make opening in the nitride
etch nitride right p1.x=-4
structure outf=2xLOCOS_03.str

# Grow field oxide
diffus time=193 minutes temp=1100 pressure=0.85 wet
struct outf=2xLOCOS_04.str

# Extract oxide thickness
extract name="OxideCenter" thickness material="SiO~2" mat.occno
    =1 x.val=7.5
extract name="OxideSide"   thickness material="SiO~2" mat.occno
    =1 x.val=-11.5

# Step 4: Remove oxide and nitride
```

```
etch nitride all
etch oxide all
struct outf=2xLOCOS_05.str

# Extract bump values
extract name="SiliconCenter" thickness material="Silicon" mat.occno=1 x.val=0
extract name="SiliconSide"   thickness material="Silicon" mat.occno=1 x.val=-11.5
extract name="SiliconUsedCenter" 1*10^4 - $SiliconCenter
extract name="SiliconUsedSide"   1*10^4 - $SiliconSide
extract name="Step" $SiliconSide - $SiliconCenter
extract name="Ratio" $SiliconSide/$SiliconCenter

# Insulation oxide
deposit oxide thick=0.4
struct outf=2xLOCOS_06.str

# Deposit & Pad nitride mask
deposit nitride thick=0.055
structure outf=2xLOCOS_07.str

# Step 2: Make opening in the oxide
etch nitride right p1.x=+4
structure outf=2xLOCOS_08.str

# Grow field oxide
diffus time=290 minutes temp=1100 pressure=0.85 wet
struct outf=2xLOCOS_09.str

# Extract gap height
# Values to the left
extract name="FinalSiliconLeft" thickness material="Silicon" mat.occno=1 x.val=-12
extract name="FinalOxideLeft"   thickness material="Oxide" mat.occno=1 x.val=-12
extract name="FinalNitrideLeft"   thickness material="Nitride" mat.occno=1 x.val=-12

# Values to the right
extract name="FinalSiliconRight" thickness material="Silicon" mat.occno=1 x.val=8
extract name="FinalOxideRight"   thickness material="Oxide" mat.occno=1 x.val=8

# Gap height
extract name="Gap" $FinalSiliconRight + $FinalOxideRight - ($FinalSiliconLeft + $FinalOxideLeft + $FinalNitrideLeft)

# Plot results
tonyplot -st 2xLOCOS*.str
tonyplot -st 2xLOCOS_05.str
tonyplot -st 2xLOCOS_09.str

```

```
quit
```

I.3 RIE Process

Used as part of the cavity study elaborated in Section 3.4.

```
go athena

# Define grid
line x loc=-12 spac=0.05
line x loc=0  spac=0.05
line x loc=8  spac=0.05

line y loc=0 spac=0.012
line y loc=1 spac=0.2
line y loc=3 spac=2

# Define substrate
init silicon orient=100 c.boron=1E14
struct outf=RIE_LOCOS_00.str

material oxide visc.0=5.1 visc.E=3.48
material nitride visc.0=5.96e5 visc.E=2.5625

method viscous
oxide STRESS.DEP=t

# Step 1: Make a thick oxide
# We use deposit to save calculation time.
# In real lift this step would be a thernal oxidation.
# Thickness in um
# Etch the bumps in the using RIE
deposit photoresist thick=1.5
struct outf=RIE_LOCOS_01.str

etch photoresist right p1.x=-4

struct outf=RIE_LOCOS_02.str
# 2D etching
#etch oxide left p1.x=0
#etch oxide DRY thick=0.1
etch silicon DRY thick=0.5
strip photo
struct outf=RIE_LOCOS_03.str

# Extract values
extract name="SiliconCenter" thickness material="Silicon" mat.
    occno=1 x.val=0
extract name="SiliconSide"   thickness material="Silicon" mat.
    occno=1 x.val=-11.5
extract name="SiliconUsedCenter" 1*10^4 - $SiliconCenter
extract name="SiliconUsedSide"   1*10^4 - $SiliconSide
extract name="Step" $SiliconSide - $SiliconCenter
extract name="Ratio" $SiliconSide/$SiliconCenter

# Grow field oxide
```

```
diffus time=27.5 minutes temp=1100 pressure=0.85 wet
extract name="OxideLeft"   thickness material="Oxide" mat.occno
    =1 x.val=-11.5
struct outf=RIE_LOCOS_04.str

# Deposit & Pad nitride mask
deposit nitride thick=0.055
structure outf=RIE_LOCOS_05.str

# Step 2: Make opening in the oxide
etch nitride right p1.x=+4
structure outf=RIE_LOCOS_06.str

# Grow field oxide
diffus time=291 minutes temp=1100 pressure=0.85 wet
struct outf=RIE_LOCOS_07.str

# Extract gap height
# Values to the left
extract name="FinalSiliconLeft" thickness material="Silicon"
    mat.occno=1 x.val=-12
extract name="FinalOxideLeft"   thickness material="Oxide" mat.
    occno=1 x.val=-12
extract name="FinalNitrideLeft"   thickness material="Nitride"
    mat.occno=1 x.val=-12

# Values to the right
extract name="FinalSiliconRight" thickness material="Silicon"
    mat.occno=1 x.val=8
extract name="FinalOxideRight"   thickness material="Oxide" mat
    .occno=1 x.val=8

# Gap height
extract name="Gap" $FinalSiliconRight + $FinalOxideRight - (
    $FinalSiliconLeft + $FinalOxideLeft + $FinalNitrideLeft)

# Plot results
tonyplot -st RIE_LOCOS*.str
tonyplot -st RIE_LOCOS_03.str
tonyplot -st RIE_LOCOS_07.str

quit
```

I.4 Maskless LOCOS Process

Used as part of the cavity study elaborated in Section 3.4.

```
go athena

# Define grid
line x loc=-12 spac=0.05
line x loc=0  spac=0.05
line x loc=8  spac=0.05

line y loc=0 spac=0.012
line y loc=1 spac=0.2
line y loc=3 spac=2

# Define substrate
init silicon orient=100 c.boron=1E14
struct outf=MaskLessLOCOS_00.str

material oxide visc.0=5.1 visc.E=3.48
material nitride visc.0=5.96e5 visc.E=2.5625

method viscous
oxide STRESS.DEP=t

# Step 1: Make a thick oxide
# We use deposit to save calculation time.
# In real lift this step would be a thernal oxidation.
# Thickness in um

deposit oxide thick=2
struct outf=MaskLessLOCOS_01.str

# Step 2: Make opening in the oxide
etch oxide right p1.x=-4

#to simulate an overetch in the AOE
etch silicon DRY thick=0.05
struct outf=MaskLessLOCOS_02.str

# Step 3: Grow bump oxide
method fermi
diffus time=450 minutes temp=1100 pressure=0.85 wet
struct outf=MaskLessLOCOS_03.str

# Extract oxide thickness
extract name="OxideCenter" thickness material="SiO~2" mat.occno
    =1 x.val=0
extract name="OxideSide"   thickness material="SiO~2" mat.occno
    =1 x.val=-11.5

# Step 4: Remove oxide
etch oxide all
struct outf=MaskLessLOCOS_04.str
```

```

# Extract values
extract name="SiliconCenter" thickness material="Silicon" mat.occno=1 x.val=0
extract name="SiliconSide"   thickness material="Silicon" mat.occno=1 x.val=-11.5
extract name="SiliconUsedCenter" 1*10^4 - $SiliconCenter
extract name="SiliconUsedSide"   1*10^4 - $SiliconSide
extract name="Step" $SiliconSide - $SiliconCenter
extract name="Ratio" $SiliconSide/$SiliconCenter

# Step 5: Insulation oxide
# Grow field oxide
diffus time=26.5 minutes temp=1100 pressure=0.85 wet
extract name="OxideLeft"   thickness material="Oxide" mat.occno=1 x.val=-11.5
struct outf=MaskLessLOCOS_05.str

# Deposit & Pad nitride mask
deposit nitride thick=0.055
structure outf=MaskLessLOCOS_06.str

# Step 6: Make opening in the oxide
etch nitride right p1.x=+4
structure outf=MaskLessLOCOS_07.str

# Grow field oxide
diffus time=293 minutes temp=1100 pressure=0.85 wet
struct outf=MaskLessLOCOS_08.str

# Extract gap height
# Values to the left
extract name="FinalSiliconLeft" thickness material="Silicon" mat.occno=1 x.val=-12
extract name="FinalOxideLeft"   thickness material="Oxide" mat.occno=1 x.val=-12
extract name="FinalNitrideLeft"   thickness material="Nitride" mat.occno=1 x.val=-12

# Values to the right
extract name="FinalSiliconRight" thickness material="Silicon" mat.occno=1 x.val=12
extract name="FinalOxideRight"   thickness material="Oxide" mat.occno=1 x.val=12

# Gap height
extract name="Gap" $FinalSiliconRight + $FinalOxideRight - ($FinalSiliconLeft + $FinalOxideLeft + $FinalNitrideLeft)

# Plot results
tonyplot -st MaskLessLOCOS*.str
tonyplot -st MaskLessLOCOS_02.str
tonyplot -st MaskLessLOCOS_03.str
tonyplot -st MaskLessLOCOS_08.str
```

```

quit
```

APPENDIX J

Fabrication Processes

J.1 Single LOCOS Process

Process notes

This document contains a full process flow for fabrication CMUTs using a LOCOS process. Names for the equipment and the recipes are all from the Nanolab cleanroom at DTU.

The process steps are numerated chronologically. When step number is denoted with a floating number (e.g 1.0,1.1,1.2,...) each step should be conducted immediately after the previous step, whereas steps that are numbered with integers (e.g 2,3,4) can be conducted at any given time.

The LOCOS process has shown to be a robust fabrication process for linear CMUT arrays. The intended substrate is a highly doped n-type silicon substrate. Reducing the resistivity or equivalently increasing the doping level is desirable. Previously, functional linear arrays have been fabricated using a silicon substrate with a resisitivty of $\rho = 0.025\Omega$cm or equivalently $N_d \approx 10^{19}\text{cm}^{-3}$. Hence, the chosen substrate should be equal or better than these values.

Step	Equipment	Recipe	Comments
Clean			
1.0	RCA Bench	Full RCA clean	Remember test wafer
Thin film deposition			
1.1	Furnace: Phosphorus Drive-in (A3)	DRY1100 Time: 8 h 20 min Anneal: 20 min 00 s Thickness: 400 nm	$\approx$ 400 nm to ensure protection for CMUTs with a pull-in voltage of 220 V.
1.1a	Filmtek	Measure oxide thickness	Measured: 394 nm.
1.2	Furnace: LPCVD Nitride (4") (B2)	nitride4 Time: 18 min 30 s Thickness: 55 nm	*14 minute deposition yielding a thickness of $\approx$ 55 nm.*
1.2a	Filmtek	Measure nitride thickness	Measured: 63 nm.
1.3	LPCVD Poly-Si (4") (B4)	POLY620 Time: 11 min 30 s Thickness: 100 nm	*11 minute deposition yielding a thickness of $\approx$ 100 nm.*
1.3a	Filmtek	Measure poly-si thickness	Measured: 97 nm.
Lithography			
2	Spin Coater: Gamma UV	1421 DCH 100mm MIR701 2um HDMS	Run a dummy wafer first without HDMS to check coverage.
3	Aligner: Maskless 03 (MLA3)	Dose: 320 Defocus: 0 Exposure mode: Fast	**Cavity mask** has to be inverted if using MIR701 and MLA3.
4	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	-
5.0	Developer: TMAH UV-lithography	2001-DCH PEB 110C 60s	Bake step prior to the wet poly etch.
5.0a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
5.0b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and cavity width
Etch			
5.1	Wet Poly Si etch	Etch rate: $\approx$ 100-200 nm/min Etch rate SiO2: $\approx$ 6 nm/min	Etch until pattern is fully developed and the poly on the backside is removed as well. Etch rate depends heavily on when the BHF was added to the solution, so check that on Labmanager before etching.
5.1a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
5.1b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and cavity width
6	Plasma Asher 2	Manual	45 minutes. O_2 flow 400 ml/min and N_2 flow 70 ml/min.
6a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
6b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and cavity width
7	Wet Nitride etch: H3PO4	Etch rate: $\approx$ 2.6 nm/min Time: 45 min Temp.: 160°	Etch 45 minutes to ensure a good over etch.
7a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
7b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and cavity width
8	Wet Poly Si etch	Etch rate poly-si: $\approx$ 100-200 nm/min Etch rate SiO2: $\approx$ 6 nm/min	Etch until all poly-si is stripped from the cavities.
8a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
8b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and cavity width
Clean			
9	Piranha	-	10 min (wafer cleaner can also be used).
10.0	RCA Bench	Full RCA clean	(Consider to skip the HF dips to avoid removing more SiO2.)
LOCOS oxidation			
10.1	Furnace: Phosphorus Drive-in (A3)	WET1100 Time: 1h 13 min Anneal: 20 min 00 s Thickness: 670 nm	The LOCOS post oxide thickness is determined by the design. Use the Furnace MatLab script for accurate and precise calculations of the resulting thickness.
10.1a	Filmtek	Measure oxide thickness	Measured: 663 nm.
10.1b	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
10.1c	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and cavity width

[a] A clean consisting of only the RCA1 solution have shown to leave the surface with the lowest particle count. However, this can change! Unfortunately, the particle counter inside the cleanroom has been decommissioned, and therefore no option to verify or test the particle density on the surface.

[b] The PES solution is originally designed for silicon rich aluminum, but, in this application the PES solution is better than

J.2 Double LOCOS Process

Process notes

This document contains a full process flow for fabrication CMUTs using a double LOCOS process. Names for the equipment and the recipes are all from the Nanolab cleanroom at DTU.

The process steps are numerated chronologically. When step number is denoted with a floating number (e.g 1.0,1.1,1.2,...) each step should be conducted immediately after the previous step, whereas steps that are numbered with integers (e.g 2,3,4) can be conducted at any given time.

The LOCOS process has shown to be a robust fabrication process for linear CMUT arrays. The intended substrate is a highly doped n-type silicon substrate. Reducing the resistivity or equivalently increasing the doping level is desirable. Previously, functional linear arrays have been fabricated using a silicon substrate with a resisitivty of $\rho = 0.025\Omega$cm or equivalently $N_d \approx 10^{19}\text{cm}^{-3}$. Hence, the chosen substrate should be equal or better than these values.

Step	Equipment	Recipe	Comments
Clean			
1.0	RCA Bench	Full RCA clean	Remember 1 test wafer and 1 dummy wafer (to be re-included later in the process).
Thin film deposition for first LOCOS			
1.1	Furnace: Phosphorus Drive-in (A3)	DRY1100 Time: 50 min Anneal: 20 min 00 s Target thickness: 100 nm	Padding oxide. The final thickness is not critical but the oxidation time in step 10.1 should be adapted. Include a dummy wafer that is taken out at this step and paused until step 10.0.
1.1a	Filmtek/Ellipsometer	Measure oxide thickness on test wafer and the dummy wafer	Measured:
1.2	Furnace: LPCVD Nitride (4") (B2)	nitride4 Time: 14 min 00 s Thickness: 55 nm	Oxidation mask.
1.2a	Filmtek/Ellipsometer	Measure nitride thickness on test wafer	Measured:
1.3	LPCVD Poly-Si (4") (B4)	POLY620 Time: 11 min 30 s Thickness: 100 nm	Hard mask for wet nitride etch.
1.3a	Filmtek/Ellipsometer	Measure poly-si thickness on test wafer	Measured:
1.3b	Camera	-	Photo of the wafer.
Lithography for bump definition			
2	Spin Coater: Gamma UV	1421 DCH 100mm MIR701 2um HDMS	Run a dummy wafer first without HDMS to check coverage.
3	Aligner: Maskless 03 (MLA3)	Dose: 320 Defocus: 0 Exposure mode: Fast	**Bump mask** has to be inverted if using MIR701 and MLA3 (remember to increase exposure area). Alternatively, use nLOF 2020 2um and MLA2 (check dose in logbook).
4	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	
4a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
4b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the resist bump and check it is in agreement with the expected height.
4c	Camera	-	Photo of the wafer.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
5.0	Developer: TMAH UV-lithography	2001-DCH PEB 110C 60s	Bake step prior to wet poly etch.
Wet etch for first LOCOS			
5.1	Wet Poly Si etch	Etch time: ≈ 4-5 min Etch rate poly-si: ≈ 100-200 nm/min Etch rate SiO2: ≈ 6 nm/min	The etch time can vary and the etch rate depends heavily on when the BHF was added to the solution, so check that on Lab-manager before etching. Etch until pattern is fully etched and the poly on the backside is removed as well.
5.1a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
5.1b	Camera	-	Photo of the wafer.
5.1c	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structure and check it is in agreement with the expected height. If not then return to step 5.1 and continue the poly-si etch and check with the Dektak again.
6	Plasma Asher 2	Recipe: Manual Time: 45 min O_2 flow 400 ml/min N_2 flow 70 ml/min.	
6a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
6b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the poly-si bump and check it is in agreement with the expected height.
6c	Camera	-	Photo of the wafer.
7	Wet Nitride etch: H3PO4	Etch rate: ≈ 2.6 nm/min Time: 45 min Temp.: 160°	Etch 45 minutes to ensure a good over etch.
7a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
7b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structure and check it is in agreement with the expected height.
7c	Camera	-	Photo of the wafer.
8	Wet Poly Si etch	Etch time: 4-6 min Etch rate: ≈ 100-200 nm/min Etch rate SiO2: ≈ 6 nm/min	The etch time can vary and the etch rate depends heavily on when the BHF was added to the solution, so check that on Lab-manager before etching. Etch until the poly-si is fully stripped.
8a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
8b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the nitride bump.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
8c	Camera	-	Photo of the wafer.
Clean			
9	Piranha	Time: 10 min	Cleaning wafers due to possible contamination by potassium ions from the nitride and poly baths. (Alternatively, the wafer cleaner can also be used.)
10.0	RCA Bench	Full RCA clean	Re-include the dummy wafer from step 1.1. Skip the HF dips to avoid removing SiO2.
1xLOCOS oxidation			
10.1	Furnace: Phosphorus Drive-in (A3)	WET1100 Time: 3 h 53 min Anneal: 20 min 00 s Target thickness: 1230 nm (on new test wafer)	Target thickness on dummy wafer is 1237 nm.
10.1a	Filmtek	Measure oxide thickness	Measured:
10.1b	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
10.1c	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structure.
10.1d	Camera	-	Photo of the wafer.
Strip oxide and nitride			
11	Wet oxide etch 2: BHF (clean w. wetting agent)	Etch time: 13 min Etch rate: 75-80 nm/min	To strip oxynitride. Etch time based on total oxide etch time minus 3 min (from Seldi).
11a	Microscope	-	Check the radius of the cavities/bumps and all structures are all well-defined.
11b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structures.
11c	Camera	-	Photo of the wafer.
12	Wet Nitride etch: H3PO4	Etch rate: $\approx$ 2.6 nm/min Etch time: 45 min Temp.: 160°	Etch 45 minutes to ensure a good over etch.
12a	Microscope	-	Check the radius of the cavities/bumps and all structures are all well-defined.
12b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structures.
12c	Camera	-	Photo of the wafer.
13	Piranha	Time: 10 min	Cleaning wafers due to possible contamination by potassium ions from the nitride bath. (Alternatively, the wafer cleaner can also be used.)
14	Wet oxide etch 2: BHF (clean w. wetting agent)	Etch time: 5 min Etch rate: 75-80 nm/min	To strip remaining oxide. An over etch of 2 min is included to ensure all oxide is removed.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
14a	Microscope	-	Check the radius of the bumps and all structures are all well-defined.
14b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height and bump width.
14c	AFM	Measure surface roughness	Measured:
14d	Camera	-	Photo of the wafer.
Clean			
15.0	RCA Bench	Full RCA clean	Remember 1 test wafer and 2 dummy wafers (to be used later in the process).
Thin film deposition for second LOCOS			
15.1	Furnace: Phosphorus Drive-in (A3)	DRY1100 Time: 8 h 20 min Anneal: 20 min 00 s Target thickness: 400 nm	Insulating oxide. Include a dummy wafer that is taken out at this step and paused until step 24.0.
15.1a	Filmtek/Ellipsometer	Measure oxide thickness on test wafer and the dummy wafers.	Measured:
15.1b	Break down voltage		Outside the clean room, check the routine for break down measurements on the wiki. Use one of the dummy wafers.
15.2	Furnace: LPCVD Nitride (4") (B2)	nitride4 Time: 14 min 00 s Thickness: 55 nm	Oxidation mask.
15.2a	Filmtek/Ellipsometer	Measure nitride thickness on test wafer	Measured:
15.3	LPCVD Poly-Si (4") (B4)	POLY620 Time: 11 min 30 s Thickness: 100 nm	Hard mask for wet nitride etching.
15.3a	Filmtek/Ellipsometer	Measure poly-si thickness on test wafer	Measured:
15.3b	Camera	-	Photo of the wafer.
Lithography for cavity definition			
16	Spin Coater: Gamma UV	1421 DCH 100mm MIR701 2um HDMS	Run a dummy wafer first without HDMS to check coverage.
17	Aligner: Maskless 03 (MLA3)	Dose: 320 Defocus: 0 Exposure mode: Fast	**Cavity mask** has to be inverted if using MIR701 and MLA3 (remember to increase exposure area). Alternatively, use nLOF 2020 2um and MLA2 (check dose in logbook).
18	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	
18a	Microscope	-	Check the alignment is successful. Check radius of the cavities and all structures are all well-defined.
18b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the resist bump and check it is in agreement with the expected height.
18c	Camera	-	Photo of the wafer.
19.0	Developer: TMAH UV-lithography	2001-DCH PEB 110C 60s	Bake step prior to wet poly etch.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
Wet etch for second LOCOS			
19.1	Wet Poly Si etch	Etch time: ≈ 4-5 min Etch rate poly-si: ≈ 100-200 nm/min Etch rate SiO2: ≈ 6 nm/min	The etch time can vary and the etch rate depends heavily on when the BHF was added to the solution, so check that on Lab-manager before etching. Etch until pattern is fully etched and the poly on the backside is removed as well.
19.1a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
19.1b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structure and check it is in agreement with the expected height.
19.1c	Camera	-	Photo of the wafer.
20	Plasma Asher 2	Recipe: Manual Time: 45 min O_2 flow 400 ml/min N_2 flow 70 ml/min.	
20a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
20b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the poly-si bump and check it is in agreement with the expected height.
20c	Camera	-	Photo of the wafer.
21	Wet Nitride etch: H3PO4	Etch rate: ≈ 2.6 nm/min Time: 45 min Temp.: 160°	Etch 45 minutes to ensure a good over etch.
21a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
21b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the structure and check it is in agreement with the expected height.
21c	Camera	-	Photo of the wafer.
22	Wet Poly Si etch	Etch time: 4-6 min Etch rate: ≈ 100-200 nm/min Etch rate SiO2: ≈ 6 nm/min	The etch time can vary and the etch rate depends heavily on when the BHF was added to the solution, so check that on Lab-manager before etching. Etch until the poly-si is fully stripped.
22a	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
22b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the nitride bump.
22c	Camera	-	Photo of the wafer.
Clean			

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
23	Piranha	Time: 10 min	Cleaning wafers due to possible contamination by potassium ions from the nitride and poly baths.
24.0	RCA Bench	Full RCA clean	Re-include the dummy wafer from step 15.1. Skip the HF dips to avoid removing SiO2.
2xLOCOS oxidation			
24.1	Furnace: Phosphorus Drive-in (A3)	WET1100 Time: 6 h 16 min Anneal: 20 min 00 s Target thickness: 1575 nm (on new test wafer)	Creating the post oxide. Target thickness on dummy wafer is 1636 nm.
24.1a	Filmtek	Measure oxide thickness	Measured:
24.1b	Microscope	-	Check the radius of the cavities and all structures are all well-defined.
24.1c	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure cavity height on one of the test structures and check nitride edge is below the bonding surface.
24.1e	AFM	Measure surface roughness	Measured:
24.1f	AFM	Measure nitride bump	Make sure the nitride edge is below the bonding surface.
24.1g	Camera	-	Photo of the wafer.
Pre bond clean			
25.0	RCA Bench	Only RCA1[a]	Remember to clean SOI/PSOI wafers in this step as well. It is a good idea to position the wafers in bonding pairs, meaning the bond interface face towards each other. A pre bonding can then be performed under the RCA HEPA filter using a vacuum tweezer, to obtain to smallest possible particle contamination.
Fusion bonding			
25.1	Wafer Bonder 02	CMUT fusion bonding standard	To protect the surface from undesired particles (from the top piston in the wafer bonder) use a dummy silicon wafer on top of the bonded stack. Remember to have the unpolished side towards to the bonded stack.
25.2	Furnace: Anneal-bond (C3)	ANN1100 Time: 1 h 10 min	
25.2a	PL mapper	Detector: Si + InGaAs Gain: x10	Check bond for voids.
25.2b	Camera	-	Photo of the wafer.
Dry etch for PSOI layer removal			
26	ASE	Recipe: 1shalolr Etch rate: 3-4 um/min Etch time:	Etching the poly-si on the back of the PSOI. Etch rate in silicon/poly-silicon is approximately 600 nm per bosch cycle.
27a	Camera	-	Photo of the wafer.
28	AOE	Recipe: SiO2_res Etch rate: 200 nm/min Etch time:	Etching the oxide on the back of the PSOI.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
28a	Camera	-	Photo of the wafer.
Etch - Handle removal			
29.0	ASE	Recipe: Etchaway Etch time:	If the PSOI has a BOX oxide thicker than 600 nm you can use dry etch all the way through the handle layer. If the BOX layer is less than 600 nm etch until 1 cm of the wafer edge become visible in the chamber.
29.1	Si Etch 2: KOH	Etch time: ≈ 30 min Temp.: 80°C.	This step should not be conducted if the handle is completely removed in the ASE (step 29.0).
Post KOH clean			
30	Piranha	Time: 10 min	This step can be omitted if the handle is completely removed in the ASE and the wafer has not been in the KOH bath (step 29.0).
30a	Camera	-	Photo of the wafer.
BOX removal			
31	Oxide etch 2: BHF (clean w. wetting agent)	Etch rate: ≈ 80 nm/min Etch time:	Etch until the oxide is removed on the front side. The etch time will vary dependent on the thickness of the BOX layer. If the CMUT design for some reason is sensitive to wafer bow or it is ideal to have an oxide on the backside, this step should be substituted with a dry etch step in the AOE.
31a	Camera	-	Photo of the wafer.
Lithography for bottom electrode definition			
32	Spin Coater: Gamma UV	1421 DCH 100mm MIR701 2um HDMS	Run a dummy wafer first without HDMS to check coverage.
33	Aligner: Maskless 03 (MLA3)	Dose: 320 Defocus: 0 Exposure mode: Fast	**Bottom electrode mask**
34	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	
34a	Microscope	-	Check the alignment is successful. Check all structures are all well-defined.
34b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the resist bump and check it is in agreement with the expected height.
34c	Camera	-	Photo of the wafer.
Dry etch - opening to bottom electrode			
35	ASE	Recipe: 1shalolr Etch rate: 3-4 um/min Etch time:	Etch through device layer. Etch rate in silicon/poly-silicon is approximately 600 nm per bosch cycle.
36	AOE	Recipe: SiO2_res Etch rate: 200 nm/min Etch time:	Etch through the post oxide.
36a	Microscope	-	Check the alignment is successful. Check all structures are all well-defined.
36b	Camera	-	Photo of the wafer.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
37	Plasma Asher 2	Recipe: Manual Time: 45 min O_2 flow 400 ml/min N_2 flow 70 ml/min.	
Metal deposition			
38	E-Beam Evaporator (Temescal)	Material: Al Thickness: 400 nm	
Lithography for the top electrode			
39	Spin Coater: Gamma UV	1421 DCH 100mm MIR701 2um HDMS	Run a dummy wafer first without HDMS to check coverage.
40	Aligner: Maskless 03 (MLA3)	Dose: 320 Defocus: 0 Exposure mode: Fast	**Top electrode mask** Notice the design has (typically) to be inverted when MLA3 is used, remember then to extend the boarders to ensure exposure over the entire wafer.
41	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	
41a	Microscope	-	Check the alignment is successful. Check all structures are all well-defined.
41b	Dektak XTA	Range: 6.5 μm Stylus Force: 5 μm Length: 300 μm Duration: 33 s	Measure height of the resist bump and check it is in agreement with the expected height.
41c	Camera	-	Photo of the wafer.
42.0	Developer: TMAH UV-lithography	2001-DCH PEB 110C 60s	Bake step prior to the wet Al etch.
Etch - top electrode definition			
42.1	PES Al etch[b]	-	
42.1a	Microscope	-	Check the alignment is successful. Check all structures are all well-defined. Remember inspection of the elements and check the aluminium is etched between the elements.
42.1b	Camera	-	Photo of the wafer.
43	ASE	Recipe: 1shalolr Etch rate: 3-4 um/min Etch time:	Etch through device layer. Etch rate in silicon/poly-silicon is approximately 600 nm per bosch cycle.
44	Plasma Asher 1	Recipe: Manual Time: 45 min O_2 flow 400 ml/min N_2 flow 70 ml/min.	
44a	Microscope	-	Check the alignment is successful. Check all structures are all well-defined.
44b	Camera	-	Photo of the wafer.
Lithography for chip protection			
45	Spin Coater: Gamma UV	1421 DCH 100mm MIR701 2um HDMS	Run a dummy wafer first without HDMS to check coverage.

Continued on next page

Table 1 – continued from previous page

Step	Equipment	Recipe	Comments
46	Aligner: Maskless 03 (MLA3)	Dose: 320 Defocus: 0 Exposure mode: Fast	**Final resist** Notice the design has (typically) to be inverted when MLA3 is used, remember then to extend the boarders to ensure exposure over the entire wafer.
47	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	
47a	Camera	-	Photo of the wafer.

[a] A clean consisting of only the RCA1 solution have shown to leave the surface with the lowest particle count. However, this can change! Unfortunately, the particle counter inside the cleanroom has been decommissioned, and therefore no option to verify or test the particle density on the surface.

[b] The PES solution is originally designed for silicon rich aluminum, but, in this application the PES solution is better than conventional H_3PO_4 since it etches aluminium without bubble formation, which makes the element separation much easier.

J.3 RIE Process

Process flow title: SURE: 1D CMUT – 1xLOCOS with predefined bumps (oxide)				Revision: 1.0
DTU Danchip National Center for Micro- and Nanofabrication	Contact Email		Contact Person	Contact phone
	Labmanager group: MEMS	Batch name: SURE 1D CMUT	Date of Creation	Date of revision

Objectives

Batch name: SURE 1D CMUT LOCOS

The purpose of this project is to fabricate a high frequency 1D linear Capacitive Ultrasonic Transducers using LOCOS to define the cavities

There two design with different radii and top plate thickness. Both designs have a frequency of 15 MHz and a pitch of λ/2
The hexagonal design have a cavity radius of 17.4 um and top plate thickness of 1.77 um silicon
The cubic design have a cavity radius of 14.7 um and top plate thickness of 1.14

This LOCOS is a "2xLOCOS" structure but the bumbs are defined by matching an oxide growth so the bumbs will be 500nm. This is done by simply etching the bumps with a RIE into the Si wafer (substrate). The target bump height is 500 nm +/- 10 nm

Charging investigation along with the fabrications of the CMUT

Substrates

Substrate	Orient.	Size	Doping/type	Polish	Thickness	Box	Device layer thickness	Purpose	#Sample ID
Si	<100>	4''	n (Phos.) High doping	SSP	525±25			Bottom Electrode	
Si	<100>	4''	n (Phos.) Low doping	DSP	350+25			Top electrode	

Process flow title:	Revision:	Date if revision:	Contact email
SURE: 1D CMUT - RIExLOCOS	1.0		stlope@dtu.dk

Step	Heading	Equipment	Procedure	Comments
1	Preparation			Bottom electrode wafer
1.1	Wafer selection	Wafer box		
2	Lithography 1.5 µm – Bump mask			Bottom electrode wafer
2.1	Coat wafer	Spin coater: Gamma UV	nLOF negative resist Recipe: 1.5 µm with HMDS	
2.2	Exposure	MLA 2	Align to flat Dose 340 Defocus 0 Laser 375 nm Autofocus Optical Mask: Cavity	
2.3	Develop	TMAH UV developer	Recipe: 3008 120s PEB and 60s puddel develop	
2.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
3	Dry etch – Bump definition			
3.1	RIE etch	Pegasus	Target height 500 nm	
3.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	Test the uniformity of the etch.
3.3	Resist strip	Plasma asher 2	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
3.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
4	Oxidation-Insulating oxide			Bottom electrode wafer
4.1	RCA	RCA bench		All wafers
4.2	SiO2 dry oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and test wafers for equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Dry1100, time: ?? Target thickness: ?? Annealing time: 20 min	1-3 Dummies
4.3	Thickness measure	Filmtek	Measure oxide thickness on dummy wafer	Dummy wafer
4.4	Break down voltage		Out of clean room	Dummy
5	Nitride deposition-LOCOS nitride			Bottom electrode wafer
5.1	Si3Ni4 Deposition	Furnace: LPCVD Nitride (4") (B2)	Deposit nitride Recipe: Nitride4 Time: 14 min Target thickness: 56 nm ±5nm	
5.2	Break down voltage		Out of clean room	Dummy
6	Polysilicon deposition – Nitride etch mash			Bottom electrode wafer

6.1	Polysilicon deposition	Furnace: LPCVD Poly-Si (4") (B4)	Recipe: Poly620 Time: 11 min Target thickness: 100nm	
7	Lithography 1.5 µm – Polysilicon etch/nitride etch			Bottom Electrode wafer
7.1	Coat wafer	Spin coater: Gamma UV	nLOF negative resist Recipe: 1.5 µm with HMDS	
7.2	Exposure	MLA 2	Align to flat Dose 340 Defocus 0 Laser 375 nm Autofocus Optical Mask: Cavity	
7.3	Develop	TMAH UV developer	Recipe: 3008 120s PEB and 60s puddel develop	
7.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
8	Poly etch			Bottom Electrode wafer
8.1	Polysilicon etch	Wet PolySi etch	Strip PolySi for 2 min	
8.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
8.3	Strip Resist	Plasma asher 2	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
8.4		Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks
9	Nitride wet etch-LOCOS nitride			Bottom electrode wafer
9.1	Nitride etch	Wet bench	Wet silicon nitride etch H3PO4 @ 160 C Time: 45 min	
9.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
9.3	Wafer clean	Wafer clean	Process time: 10 min Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH	
9.4	Strip polysilicon mask	DRIE Pegasus/ Poly wet etch	Recipe: 100nmPoly_SOI Process time: 12s (2 cycles) Wet poly etch: approx 4 min (remember to move the carrier)	**If Poly wet etch is done be mindful that is also etches the oxide!!!**
10	Oxidation-LOCOS			Bottom electrode wafer
10.1	RCA	RCA bench	Only first HF for half the time (10 sec)	
10.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and placed device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Wet1100, time: 68.4 min Target thickness (post oxide): 750 nm	1-3 dummies. Note the time in the logbook

10.3	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
11	Wafer Bonding			All wafers
11.1	RCA	RCA bench	RCA of all wafers	
11.2	Fusion Bonding	Wafer bonder 02	Recipe: CMUT Transport wafers in dedicated box from RCA. Minimize ambient exposure and handling time. Use RCA cleaned tweezers	
11.3	Annealing	Anneal-bond furnace	Recipe: Ann1100 Time: 1h 10min	
11.4	Inspection	Pl mapper	Inspect post anneal voids Detector: Si + InGaAs Gain: x10 (corr.) Filter: 1100nm HP	
12	Handle layer and box oxide etch			Bonded wafers
12.1	Polysilicon etch (Si etch)	Si Etch 2: KOH	Etch the top polysilicon layer away	
12.2	Oxide Etch	BHF	Etch box oxide away, Time: check oxide is gone.	There should be plenty of oxide on the backside for the removal of both BOX'es
12.3	Wafer clean	Wafer clean	Process time: 10 min Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH and BHF	
12.4	Si etch	Pegasus	Recipe: etchaway1 time: 24 min	Etch until the oxide become visible at the circumference of the wafer. The time matches
12.5	Si wet etch	KOH	Etch handle layer away: Time: till the bubbles are gone	For the rest of the handle layer of silicon
12.6	Oxide Etch	BHF	Etch box oxide away, Time: check oxide is gone.	There should be plenty of oxide on the backside for the removal of both BOX's
12.7	Wafer clean	Wafer clean	Process time: 10 min Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH and BHF	
13	Lithography - Access to bottom electrodes			Bonded wafers
13.1	Coat wafer	Spin coater: Gamm UV	Mir 701 positive resist Recipe: 1.5 µm with HMDS	
13.2	Exposure	MLA	Dose 275 Focus 0 Laser 375 Mask: Access to bottom electrode	
13.3	Develop	TMAH UV developer	Recipe:3008, 120s PEB and 60s puddle	

13.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
16	Etch - Access to bottom electrodes			Bonded wafers
16.1	Etch Si	DRIE-Pegasus	Etch all device layer Recipe: 2 um SOI Temp: 20C Time: 1 min	
16.2	Oxide etch	AOE	Recipe: SiO2_res Oxide height: Hex oxide: 750 nm Cubic oxide: 811 nm Time: ~4 min (230 µm/min) Temp: 0C	Wait 30 min for temp to stabilize
16.3	Strip resist	Plasma Asher 1	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
16.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
17	Metallization			Bonded wafers
17.1	Al deposition	Wordentec/ Temescal	Target Al thickness: 400nm	
18	Lithography – Top electrode			Bonded wafers
18.1	Coat wafer	Spin coater: Gamma UV	nLOF negative resist Recipe: 1.5 µm	No HDMS
18.2	Exposure	MLA2	Align to flat Dose 340, defocus 0, Laser 375 nm Mask: Top electrode	Same exposure as for the first nLOF resist
18.3	Develop	TMAH UV developer	Recipe: 3008 120s PEB and 60s puddel develop	
18.4	Inspection	Optical microscope	Check pattern and alignment marks	
19	Etch top electrode			Bonded wafers
19.1	Al etch	Wet Al etch	Etch rate:~60-100 nm/min time: ~4-7 min	
19.2	Etch Si	ASE or DRIE-pegasus	Depending on the machine	
19.3	Inspection	Optical microscope	Make sure the etch is all the way through the Silicon device layer.	
19.4	Strip resist	Plasma Asher 1	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
20	Lithography – Protection layer			Bonded wafers
20.1	Coat wafer	Spin coater: Gamm UV	Mir 701 positive resist Recipe: 1.5 µm with HMDS	
20.2	Exposure	MLA	Dose 275 Focus 0	

			Laser 375 Mask: Access to bottom electrode	
20.3	Develop	TMAH UV developer	Recipe:3008, 120s PEB and 60s puddle	
20.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
16	Dicing/ Lapping			Bonded wafers
16.1	Coat wafers	Spin coater: Gamma UV	Recipe: 3441 DCH100 5214E 4.2 µm	
16.2	Dice out chips	Disco Saw	Dicing out chips	

J.4 Maskless LOCOS Process

Process flow title:				Revision:
SURE: 1D CMUT – 1xLOCOS with predefined bumps (oxide)				1.0
DTU Danchip National Center for Micro- and Nanofabrication	Contact Email		Contact Person	Contact phone
	Labmanager group: MEMS	Batch name: SURE 1D CMUT	Date of Creation	Date of revision

Objectives

Batch name: SURE 1D CMUT LOCOS

The purpose of this project is to fabricate a high frequency 1D linear Capacitive Ultrasonic Transducers using LOCOS to define the cavities

There two design with different radii and top plate thickness. Both designs have a frequency of 15 MHz and a pitch of λ/2
The hexagonal design have a cavity radius of 17.4 um and top plate thickness of 1.77 um silicon
The cubic design have a cavity radius of 14.7 um and top plate thickness of 1.14

This LOCOS is a "2xLOCOS" structure but the bumbs are defined by matching an oxide growth so the bumbs will be 500nm. This is done by first growing a thick oxide on the Si wafer (substrate). The oxide defined with the structures for the bumbs with photoresist and a short dip in BHF. The resist is striped, and wafer clean in RCA before going into the A1/A3 oven. The old oxide will slow the new oxide for diffusing into the surface where the exposed Si will start growing SiO2. At some point the bump heights are 500 nm

Charging investigation along with the fabrications of the CMUT

Substrates

Substrate	Orient.	Size	Doping/type	Polish	Thickness	Box	Device layer thickness	Purpose	#Sample ID
Si	<100>	4''	n (Phos.) High doping	SSP	525±25			Bottom Electrode	
Si	<100>	4''	n (Phos.) Low doping	DSP	350+25			Top electrode	

Process flow title:	Revision:	Date if revision:	Contact email
SURE: 1D CMUT - MLxLOCOS	1.0		stlope@dtu.dk

Step	Heading	Equipment	Procedure	Comments
1	Preparation			Bottom electrode wafer
1.1	Wafer selection	Wafer box		
2	Oxidation- Bump definition oxide			Bottom electrode wafer
2.1	RCA	RCA bench		All wafers
2.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and test wafers for equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Wet1100, time A1: 93.6 min Target thickness: 750 ± 10 nm Annealing time: 20 min	1-3 Dummies
2.3	Thickness measure	Filmtek	Measure oxide thickness on dummy wafer	Dummy wafer
2.4	Break down voltage		Out of clean room	Dummy
3	Lithography 1.5 µm – Bumbs definition			Bottom electrode wafer
3.1	Coat wafer	Spin coater: Gamma UV	nLOF negative resist Recipe: 1.5 µm with HMDS	
3.2	Exposure	MLA 2	Align to flat Dose 340 Defocus 0 Laser 375 nm Autofocus Optical Mask: Cavity	
3.3	Develop	TMAH UV developer	Recipe: 3008 120s PEB and 60s puddel develop	
3.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
4	BHF - Bump definition mask			
4.1	Oxide etch	BHF	Time: depends on layer thickness	
4.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
4.3	Resist strip	Plasma asher 2	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
4.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
5	Oxidation- Bump growth oxide			
5.1	RCA	RCA bench		
5.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and test wafers for equally distributed on each side of the test wafer. No spacing between wafers.	

			Recipe WET1100, Time: ???, Target thinkness: ??? Annealing time: 20 min	
5.3	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
6	BHF - Bump definition mask			
6.1	Oxide etch	BHF	Remove all oxide leaving only the Si bumps	
6.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
7	Oxidation- Insulating oxide			Bottom electrode wafer
7.1	RCA	RCA bench		All wafers
7.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and test wafers for equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Dry1100, time: ?? Target thickness: ?? Annealing time: 20 min	1-3 Dummies
7.3	Thickness measure	Filmtek	Measure oxide thickness on dummy wafer	Dummy wafer
7.4	Break down voltage		Out of clean room	Dummy
8	Nitride deposition-LOCOS nitride			Bottom electrode wafer
8.1	Si3Ni4 Deposition	Furnace: LPCVD Nitride (4") (B2)	Deposit nitride Recipe: Nitride4 Time: 14 min Target thickness: 56 nm ±5nm	
8.2	Break down voltage		Out of clean room	Dummy
9	Polysilicon deposition – Nitride etch mash			Bottom electrode wafer
9.1	Polysilicon deposition	Furnace: LPCVD Poly-Si (4") (B4)	Recipe: Poly620 Time: 11 min Target thickness: 100nm	
10	Lithography 1.5 µm – Polysilicon etch/nitride etch			Bottom Electrode wafer
10.1	Coat wafer	Spin coater: Gamma UV	nLOF negative resist Recipe: 1.5 µm with HMDS	
10.2	Exposure	MLA 2	Align to flat Dose 340 Defocus 0 Laser 375 nm Autofocus Optical Mask: Cavity	
10.3	Develop	TMAH UV developer	Recipe: 3008 120s PEB and 60s puddel develop	
10.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
11	Poly etch			Bottom Electrode wafer
11.1	Polysilicon etch	Wet PolySi etch	Strip PolySi for 2 min	

11.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
11.3	Strip Resist	Plasma asher 2	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
11.4		Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks
12	Nitride wet etch-LOCOS nitride			Bottom electrode wafer
12.1	Nitride etch	Wet bench	Wet silicon nitride etch H3PO4 @ 160 C Time: 45 min	
12.2	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
12.3	Wafer clean	Wafer clean	Process time: 10 min Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH	
12.4	Strip polysilicon mask	DRIE Pegasus/ Poly wet etch	Recipe: 100nmPoly_SOI Process time: 12s (2 cycles) Wet poly etch: approx 4 min (remember to move the carrier)	**If Poly wet etch is done be mindful that is also etches the oxide!!!**
13	Oxidation-LOCOS			Bottom electrode wafer
13.1	RCA	RCA bench	Only first HF for half the time (10 sec)	
13.2	SiO2 wet oxidation	Phosphorus Drive-in (A3)	Place a test wafer in the center of the boat and placed device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Recipe: Wet1100, time: 68.4 min Target thickness (post oxide): 750 nm	1-3 dummies. Note the time in the logbook
13.3	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
14	Wafer Bonding			All wafers
14.1	RCA	RCA bench	RCA of all wafers	
14.2	Fusion Bonding	Wafer bonder 02	Recipe: CMUT Transport wafers in dedicated box from RCA. Minimize ambient exposure and handling time. Use RCA cleaned tweezers	
14.3	Annealing	Anneal-bond furnace	Recipe: Ann1100 Time: 1h 10min	
14.4	Inspection	Pl mapper	Inspect post anneal voids Detector: Si + InGaAs Gain: x10 (corr.) Filter: 1100nm HP	
15	Handle layer and box oxide etch			Bonded wafers

15.1	Polysilicon etch (Si etch)	Si Etch 2: KOH	Etch the top polysilicon layer away	
15.2	Oxide Etch	BHF	Etch box oxide away, Time: check oxide is gone.	There should be plenty of oxide on the backside for the removal of both BOX'es
15.3	Wafer clean	Wafer clean	Process time: 10 min Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH and BHF	
15.4	Si etch	Pegasus	Recipe: etchaway1 time: 24 min	Etch until the oxide become visible at the circumference of the wafer. The time matches
15.5	Si wet etch	KOH	Etch handle layer away: Time: till the bubbles are gone	For the rest of the handle layer of silicon
15.6	Oxide Etch	BHF	Etch box oxide away, Time: check oxide is gone.	There should be plenty of oxide on the backside for the removal of both BOX's
15.7	Wafer clean	Wafer clean	Process time: 10 min Clean wafers after wet nitride etch due to possible contamination by potassium ions from people stripping nitride after KOH and BHF	
16	Lithography - Access to bottom electrodes			Bonded wafers
16.1	Coat wafer	Spin coater: Gamm UV	Mir 701 positive resist Recipe: 1.5 µm with HMDS	
16.2	Exposure	MLA	Dose 275 Focus 0 Laser 375 Mask: Access to bottom electrode	
16.3	Develop	TMAH UV developer	Recipe:3008, 120s PEB and 60s puddle	
16.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
17	Etch - Access to bottom electrodes			Bonded wafers
17.1	Etch Si	DRIE-Pegasus	Etch all device layer Recipe: 2 um_SOI Temp: 20C Time: 1 min	
17.2	Oxide etch	AOE	Recipe: SiO2_res Oxide height: Hex oxide: 750 nm Cubic oxide: 811 nm Time: ~4 min (230 µm/min) Temp: 0C	Wait 30 min for temp to stabilize
17.3	Strip resist	Plasma Asher 1	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
17.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	

Process flow title: SURE: 1D CMUT - MLxLOCOS	Revision: 1.0	Date if revision:	Contact email stlope@dtu.dk

18	Metallization			Bonded wafers
18.1	Al deposition	Wordentec/ Temescal	Target Al thickness: 400nm	
19	Lithography – Top electrode			Bonded wafers
19.1	Coat wafer	Spin coater: Gamma UV	nLOF negative resist Recipe: 1.5 µm	No HDMS
19.2	Exposure	MLA2	Align to flat Dose 340, defocus 0, Laser 375 nm Mask: Top electrode	Same exposure as for the first nLOF resist
19.3	Develop	TMAH UV developer	Recipe: 3008 120s PEB and 60s puddel develop	
19.4	Inspection	Optical microscope	Check pattern and alignment marks	
20	Etch top electrode			Bonded wafers
20.1	Al etch	Wet Al etch	Etch rate:~60-100 nm/min time: ~4-7 min	
20.2	Etch Si	ASE or DRIE-pegasus	Depending on the machine	
20.3	Inspection	Optical microscope	Make sure the etch is all the way through the Silicon device layer.	
20.4	Strip resist	Plasma Asher 1	Process time: 45 min O_2: 400 ml/min N: 70 ml/min Power: 1000W	
21	Lithography – Protection layer			Bonded wafers
21.1	Coat wafer	Spin coater: Gamm UV	Mir 701 positive resist Recipe: 1.5 µm with HMDS	
21.2	Exposure	MLA	Dose 275 Focus 0 Laser 375 Mask: Access to bottom electrode	
21.3	Develop	TMAH UV developer	Recipe:3008, 120s PEB and 60s puddle	
21.4	Inspection	OM+DEKTAK +OW image	Check pattern and alignment marks	
22	Dicing/ Lapping			Bonded wafers
22.1	Coat wafers	Spin coater: Gamma UV	Recipe: 3441 DCH100 5214E 4.2 µm	
22.2	Dice out chips	Disco Saw	Dicing out chips	