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Micromachined 2D Transducers for 3-D Super-Resolution Ultrasound Real-Time Imaging of Erythrocytes

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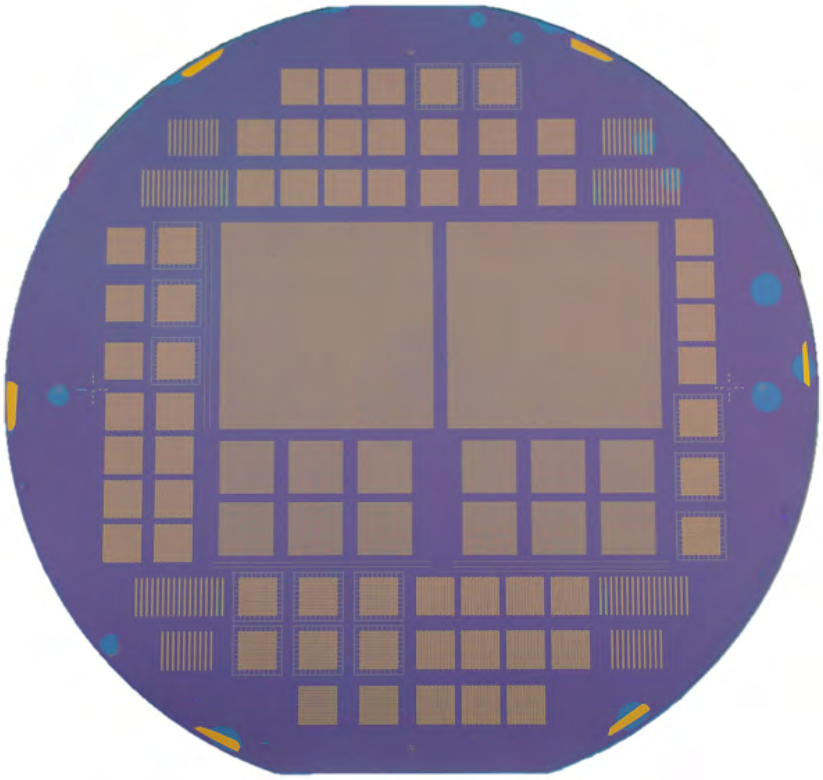


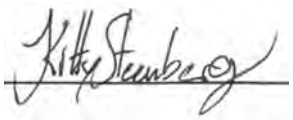
31th May 2023

Kgs. Lyngby, Denmark

Preface

This Ph.D. thesis has been submitted to the Technical University of Denmark as a partial fulfillment of the requirements for the degree of Doctor of Philosophy. The research work presented in this thesis spans from March 2020 to May 2023 and was conducted at DTU Health Tech, Technical University of Denmark, under the supervision of Professor Erik Vilain Thomsen and co-supervision of Professor Jørgen Arendt Jensen.

Capacitive Micromachined Ultrasonic Transducer (CMUT) has been researched at the MEMS Applied-Sensors group since 2012 and a comprehensive knowledge within the field had already been developed prior to my Ph.D. project.



Kitty Steenberg
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Kgs. Lyngby, May 2023

Summary

2D ultrasound is a conventional medical diagnostic tool preferred for its real-time, noninvasive and radiation-free imaging technique at low cost compared to other imaging modalities.
Since human anatomy is inherently 3D, reducing it to 2D will inevitably be at a cost of insufficient understanding of the complexity of the body and its diseases. Naturally, the interest in 3D ultrasound has risen. The transducer complexity increases immensely when transitioning from 2D to 3D imaging. For 3D imaging in real-time, using the row-column (RC) addressing scheme, the number of elements scale linearly with the electrical interconnections. In contrast to the fully populated matrix array with a squared dependency, rendering it infeasible for large arrays. The row-column architecture was chosen for this project to facilitate 3D ultrasound, super-resolution, imaging in real-time. In order to achieve super-resolution many elements are required with a high yield, furthermore, a wide aperture or a large probe surface area is advantageous for maintaining a good focus throughout the human body.
The primary goal of this Ph.D. project is to develop large-scale 2D row-column-addressed (RC) arrays of capacitive micromachined ultrasonic transducers (CMUTs) for 3D super-resolution ultrasound imaging in real-time of the erythrocytes to ultimately detect cancer and diabetes earlier. The CMUT platform was chosen for the development of row-column arrays due to its design flexibility offered by microfabrication technology, low self-heating, and wide bandwidth, all of which are advantageous for advanced imaging applications. This aim was accomplished through the successful design and fabrication of two large-scale chips resulting in an RC190+190 array and an RC512+512 array. The 2D CMUT arrays were achieved utilizing the anodic bonding fabrication technique with metal bottom electrodes to ensure a uniform pressure output even for large-scale arrays combined with an insulating substrate minimizing cross-talk between the elements. The process optimization performed in this Ph.D. study has resulted in the achievement of high-quality and void-free chip area of 7 cm × 7 cm, enabling the realization of future RC1024+1024 chips. However, the electrical yield is limited by vertical short circuits between the top and bottom electrodes due to the formation of gold defects, and future work should focus on eliminating the reaction forming the defects. One of the RC190+190 arrays was integrated into a modular prototype ultrasound probe designed for rapid prototyping within this research group. The electrical and preliminary acoustical performance of the RC190+190 CMUT was characterized. Further development is needed for optimal performance to be achieved. Additionally, the introduction, exploration and fabrication of a novel process flow of quartz fusion titanium disilicide CMUT was demonstrated with the potential to realize large-scale 2D CMUT arrays. Furthermore, specialized 3D-printed hydrogel phantoms were fabricated to validate the resolution and assess the performance of the advanced imagining algorithms. These phantoms, which are not commercially available, play a crucial role in

achieving the objectives of the SURE project, namely, enabling 3D super-resolution ultrasound through large-scale RC CMUT probes and advanced imaging algorithms.

Resumé

2D ultralyd er et konventionelt medicinsk diagnosticeringsværktøj foretrukket for sin realtids-, ikke-invasive og strålingsfri billedteknik til lavere omkostninger sammenlignet med andre billedmodaliteter. Da menneskets anatomi er tredimensionel, vil reduktionen til 2D uundgåeligt medføre en utilstrækkelig forståelse af kroppens kompleksitet og sygdomme. Derfor er interessen for 3D ultralyd er naturlig. Ultralydstransducerens kompleksitet stiger markant ved overgangen fra 2D til 3D-billeder. Til 3D ultralydsbilleddannelse i realtid skalerer antallet af elementerne lineært i et række-søjle-adresseret array med de elektriske forbindelser, i modsætning til det fuldt adresseret 2D matrix-array med en kvadratisk afhængighed, hvilket gør det uegnet til store prober da antallet af elementer og probens overfladeareal skalerer. Række-søjle-arkitekturen blev valgt til dette projekt for at realisere 3D-ultralyd med superopløsning i realtid. For at opnå superopløsning kræves mange elementer, og det resulterer i prober med stort overfladeareal, hvilket er en fordel for at opretholde et godt fokus igennem hele menneskekroppen. Det primære mål for dette ph.d.-projekt er at udvikle store 2D-række-søjle-adressede (RC) array af kapacitive mikrofabrikerede ultralydstransducere (CMUT'er) til 3D-ultralyd med superopløsning i realtid af erytrocytter for at kunne detektere kræft og diabetes tidligere. CMUT-platformen blev valgt til udvikling af række-søjle-arrays på grund af dens designmuligheder og fleksibilitet baseret på mikrofabrikation, lav selvopvarmning og bred båndbredde, hvilket er fordelagtigt for avanceret billededdannelse. Dette mål blev opnået gennem design og vellykket fabrikation af to store CMUT-chips: en RC190+190-array og en RC512+512-array. De 2D CMUT-arrays blev fabrikeret med anodisk bonding-fabrikationsteknik med metalbundelektroder for at sikre et ensartet tryk, selv for store arrays, kombineret med et isolerende substrat, der minimerer krydstale mellem elementerne. Processoptimeringen, der blev udført i dette ph.d.-studie, har resulteret i opnåelsen chip-områder på 7 cm × 7 cm uden defekter, hvilket muliggør realiseringen af fremtidige RC1024+1024-chips. Et RC190+190-array blev integreret i en modulær prototype-ultralydsprobe designet til hurtig prototyping i forskningsgruppen. Elektriske og præliminære akustiske målinger blev udført som en del af karakterisering. Yderligere udvikling er nødvendig for at opnå optimal ydeevne. Derudover blev et nyt procesflow af CMUT'er baseret på kvartsfusion og titandisilicid bundelektroder introduceret med potentialet til at realisere store CMUT-arrays. Desuden blev der fremstillet specialiserede 3D-printede hydrogel-phantomer til validering af opløsningen og vurdering af ydeevnen af de avancerede billedalgoritmer. Disse phantomer, som ikke er kommercielt tilgængelige, spiller en afgørende rolle i at opnå målene for SURE-projektet, nemlig at muliggøre 3D ultralyd med superopløsning ved brug af store RC CMUT-prober og avancerede billedalgoritmer.

Acknowledgments

Firstly, I would like to thank my supervisor Professor Erik V. Thomsen and my co-supervisor Professor Jørgen Arendt Jensen for your guidance and the opportunity to be a part of this cutting-edge research project, which I believe will impact the world for the better. Erik, you are truly inspiring with your profound knowledge within the CMUT and semiconductor field and your exceptional leadership. You cultivate a passion for learning and encourage us to aspire to greater goals within the field. I feel privileged to have had the opportunity to learn from you and develop under your guidance. I am sincerely grateful for the interesting professional discussion we have had within the MEMS group. The positive environment you have cultivated within the MEMS group makes it not only an exceptional research team but also a remarkable workplace.
I would like to thank my colleagues at DTU Health Technology Rune Sixten Grass, Mélanie Audoin, Stine Løvholt Grue Pedersen, Kasper Fløng Pedersen, Andreas Spandet Havreland and Martin Lind Ommen. To both past and present, PhD students or postdocs, I am humbled by the immense knowledge that I have had the privilege of learning from each of you. I am truly grateful for the invaluable professional support and collaboration we have shared and proud of what we have achieved. Furthermore, thank you to the students I have supervised, your dedication and contribution are an important part of the CMUT development.
Additionally, a special thank you to the staff at DTU Nanolab without your help and fabrication knowledge this project would not have been possible.
Finally, I would like to thank my close friends and my father for the endless love and support, words fall short.

Contents

Chapter 1

Introduction

1.1 Introduction

Ultrasound imaging for medical diagnostics is the utilization of acoustic pressure waves in the frequency range of 2-18 MHz for visualization of the internal structures of the human body. The basic principle of ultrasound imaging is to transmit ultrasound waves into the body, which are then partially reflected back by the tissues and organs to create an image. The reflected wave is called the echo and the ultrasound transducer receives the echo which enables imaging by converting it into electrical signals, which are processed by a scanner to create an image. A transducer is a contraption that converts energy from one form to another. How efficiently, the transducer converts from one domain to another is measured in a quantity called the electromechanical coupling coefficient.

Since the 1950s ultrasound has been known as an important diagnostic tool and point-of-care device in hospitals. The portability, low cost, and ease of use have made ultrasound probes a fundamental tool for standard health examinations, screening and primary care at hospitals, physicians and rural clinics. Compared to the other imaging modalities used to image the human body like X-ray, CT, and MRI, ultrasound is non-invasive, radiation-free, easy to use, shown in real-time and less expensive. However, ultrasound has lower resolution and penetration depth and is unable to image through bones and air. Due to the significant acoustic impedance mismatch between the two media, the ultrasound wave is primarily reflected and prevents imaging beyond this interface.
Probes in clinics are predominately made of piezoelectric ceramic (PZT). PZT stand for lead zirconate titanate, $Pb[Zr_xTi_{1-x}]O_3$. Ultrasound waves are made by using the piezoelectric effect: applied mechanical deformation results in the material generating an electric field and vice versa. Thus, inducing an alternating electric signal with the desired frequency will make the piezo crystal mechanically contract and expand transmitting pressure waves. The resonance frequency of the PZT transducer is described by

$$f = \frac{c_{\text{pzt}}}{2t_{\text{pzt}}}, \tag{1.1}$$

where the speed of sound, c_{pzt} and the thickness of the piezoelectric crystal, t_{pzt} determines the center frequency of the transducer. Maintaining the uniformity of the PZT for thinner layers is problematic, creating challenges for the realization of high-frequency probes. Most PZT transducers are fabricated using the dice and fill

method, where the elements are sawed out in the crystal [1]. The spacing (kerf) between the elements is directly limited by the dicing blade width of 15-40 µm [2]. This blade width limitation can cause a problem with high center frequencies if a $\lambda/2$-pitch is desired, which has been shown to increase image quality [3, 4]. Since the active pressure emitting area is decreased the penetration depth of the probe is decreased as well. The reduction in the active pressure emitting area, due to the dicing blade width, results in a corresponding decrease in the probe's penetration depth.
PZT are preferred for their high piezoelectric constants $d_{33} \approx$ 200-750 pC/N [5] and high electromechanical coupling coefficient ($k_{33} \approx 0.6$ to 0.75) making them highly efficient transducers. Their high dielectric constant, ϵ ensures good electrical impedance matching with the transition circuitry to the scanner [6].
Since the Restriction of Hazardous Substances Directive (RoHS), legislated the use of lead (Pb) to $<$ 1000 ppm due to the toxicity and environmental degradation, a lead-free piezoelectric ceramic for ultrasound transducers has been sought. Despite this, diagnostic medical devices such as PZT (Pb $\approx$ 60 wt % [5]) ultrasound scanners are exempted until it is technologically probable to replace the PZT [7]. Alternative lead-free ceramics like KNN ($(K,Na)NbO_3$), NBT ($Na_{1/2}Bi_{1/2}TiO_3$) and BCTZ ($(Ba,Ca)(Ti,Zr)O_3$) have been presented [7]. Potassium sodium niobate, KNN-based ceramics having a piezoelectric constant of d_{33} = 171-490 pC/N [5], Barium Titanate based piezoelectrics show d_{33} = 350-500 pC/N [8] and also $(Ba_{0.95}Ca_{0.05})(Ti_{0.94}Zr_{0.06})O_3$ textured ceramic with piezoelectric constant $d_{33} = 570$ pC/N [9] are potential lead-free piezoelectric candidates. On the contrary, the Capacitive micromachined ultrasonic transducer (CMUT) is an entirely different lead-free technique based on semiconductor technology, described in the section below which facilities sub-micron control superior and essential for high frequencies and small structures.

1.2 CMUT

In its simplest form, a CMUT is a parallel plate capacitor with a movable top plate enabling it to transmit and receive ultrasound waves, see Fig. 1.1. This is a cleanroom-fabricated device. Microfabrication provides versatile techniques and enables flexibility of the process and micrometer precision. CMUTs are made as cavities in the substrate where the bottom electrode is defined as well as the dielectric here comprised of the vacuum-filled cavity called the gap, g. The shape and size of the CMUT cell is marked by either the radius a for circular cells or the half-side length L for square cells. The top plate typically consists of the silicon plate with a top electrode on top. The thickness of the top plate is denoted h. To emit ultrasound waves with the CMUT first a DC bias is applied between the two electrodes, see Fig. 1.1 b), the top plate is electrostatically attracted to the bottom electrode and starts deflecting inwards. Secondly, an alternating AC signal is superimposed on top of the DC signal making the plate oscillate and transmit pressure waves. A transducer utilizes hundreds to thousands of these cells to transmit ultrasound. In receive, see Fig. 1.1 c), the external pressure from the echo deforms the plate and is transformed into an electric signal. It is this coupling from the kinetic mechanical energy of the plate into the electric signal that makes the transducer part of the CMUT. When increasing the applied DC bias, the spring constant of the plate will soften, known as spring softening. As the voltage increases, the spring force of the plate starts to counteract the electrostatic force. At an unstable point, known as

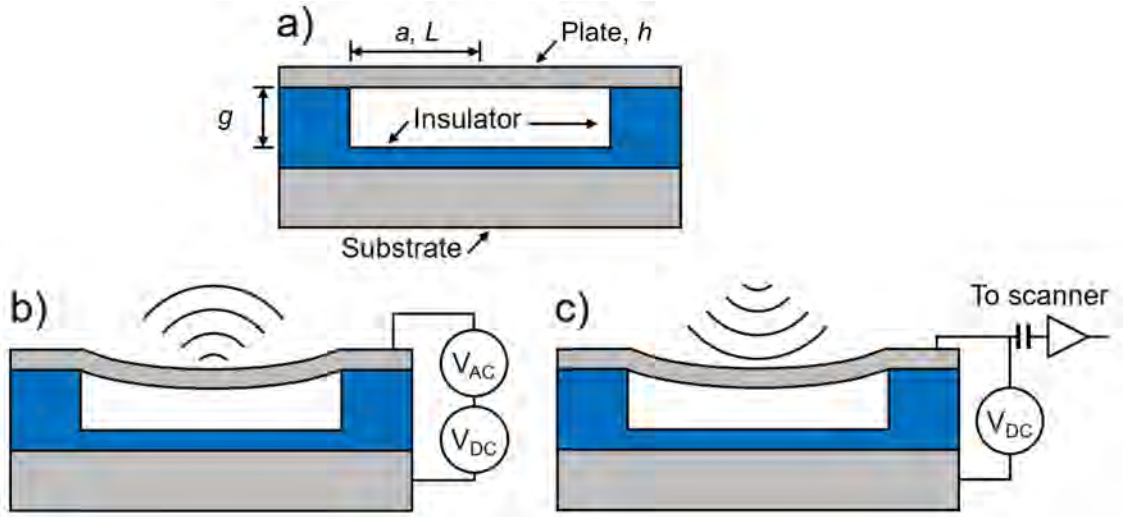


Figure 1.1: The figure shows a cross-sectional sketch of a single CMUT cell. a) The vibrating plate, of thickness h with a radius a or half side length L, is separated from the substrate and insulating dielectric by a vacuum gap g. b) When the CMUT operates as a transmitting device, a DC voltage bias is applied along with a superimposed AC signal between the top and bottom electrodes (vibrating plate and substrate, respectively) to emit an ultrasound wave. c) When the CMUT operates as a receiving device, a DC voltage bias is applied while the incoming ultrasound wave (the echo) is converted into an AC signal for the scanner. Due to the high aspect ratio all sketches of CMUT cells are not drawn to scale.

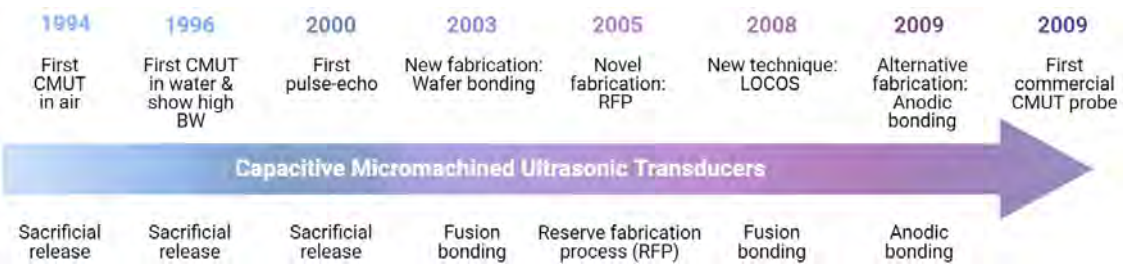


Figure 1.2: Timeline of the early CMUT evolution with a focus on the fabrication technique also stated below the gradient arrow. All of these highlights are described in more detail and cited in the text referencing this illustration. Created using Biorender.

the pull-in voltage, where the plate is pulled in or collapsed down onto the bottom of the cavity. To avoid short-circuiting of the capacitor if the CMUT cell goes into pull-in, an insulation layer between the electrodes is typically implemented. The quality of this dielectric is crucial for the performance of the CMUT. It requires a high breakdown voltage and negligible defects or impurities as these can cause dielectric charging, detrimental to the functionality of the CMUT. For a CMUT the electromechanical coupling is non-linear, which is used to improve the Signal to Noise Ratio (snr) with increasing bias while staying below the pull-in voltage. Furthermore, this non-linearity is used to increase the generated pressure as well as the receive sensitivity of the CMUT.

1.2.1 CMUT evolution

A timeline for the CMUT evolution can be seen in Fig. 1.2 with a focus on the development of fabrication techniques indicated below the gradient arrow. The concept

of CMUTs for medical ultrasound was first published by Haller and Khuri-Yakub in 1994 at Stanford University [10]. They demonstrated an electrostatic transducer fabricated with standard silicon surface micromachining using a sacrificial release process with a silicon dioxide layer. They presented a 1.9 MHz transducer designed for air-coupled applications with a 750 nm thick nitride membrane and describe the fabrication process, characterization and theory of operation. In 1996, the same authors published an extended version of their work on CMUTs in a journal article [11]. Ladabaum et al. from Siemens also worked on developing what they referred to as Micromachined Ultrasonic Transducers (MUTs) and published a conference proceeding in 1995 on the fabrication and modeling of MUTs with transmission experiments in the range from 3.1-11.4 MHz in air [12]. In the field, these papers are considered the foundation stones and start of the CMUT-era. The first demonstration of CMUTs generating ultrasound in water was presented by Soh et al. in 1996 [13], also from the same group at Stanford University. Operating at frequencies of 4 MHz, 6 MHz, and 8 MHz in immersion, exhibiting a broad bandwidth between 1 and 20 MHz and snr proving that CMUTs could rival piezoelectric transducers. The broader bandwidth is advantageous for examining the diverse parts of the human body. Oralkan and Khuri-Yakub presented the first experimental pulse-echo results in immersion on a wire phantom using a 16-element 1D CMUT array in 2000 [14] with further development to the first pulse-echo phased array using a 128-element 1D CMUT array in 2002 [15]. And the first real-time *in vivo* ultrasound images were made in 2003 by Mills and Smith at General Electric Global Research Center [16]. The very first volumetric imaging was demonstrated in 2002 with a 2D CMUT array also by Oralkan and Khuri-Yakub [17]. They fabricated a 128 $\times$ 128 element array, however, due to the large number of interconnections needed a smaller portion of 8 $\times$ 16 element was used in the experiments.

Over the years, researchers have continued to develop and improve fabrication methods for CMUTs. In 2002, Ergun et al. presented a new method for fabricating CMUTs using a wafer bonding technique. The same research group from Stanford University described this fusion bonding technique in more detail in a journal paper from 2003, see Fig. 1.2 reducing the turnaround time by 30 % for the fabrication process [18]. The CMUT cell cavities are created through etching in thermally grown silicon dioxide on a silicon wafer. This silicon wafer is fusion bonded (direct bonding) to a silicon-on-insulator (SOI) wafer, which is subsequently thinned down to the device layer constituting the top plate. The direct bonding is performed in a vacuum, thereby ensuring vacuum sealing of the cavities.

In 2004 and 2005, Caliano et al. from the Roma Tre University presented the design, fabrication and characterization of a 3 MHz 64-element 1D CMUT probe using the sacrificial release method and compared it to a standard PZT probe showing improved axial resolution, however lower sensitivity [19,20]. In the same year, Caliano et al. published a novel reserve fabrication process (RFP), a variation of the sacrificial release method [21]. Compared to the previous CMUT processing where the cavities and bottom electrodes are made first, RFP as the name implies is an inversion of this. Here the top plate is defined first by depositing a nitride layer on top of the silicon wafer determining the thickness of the CMUT plate. Afterward, the cavities are defined through a sacrificial release. An advantage of this process is that the contact pads of the array are placed on the backside enabling the use of ball grid bonding which allows for easier packing. In 2012 this RFP technique was used to realize a 12 MHz 192-element 1D CMUT probe presented by Savoia et al [22].

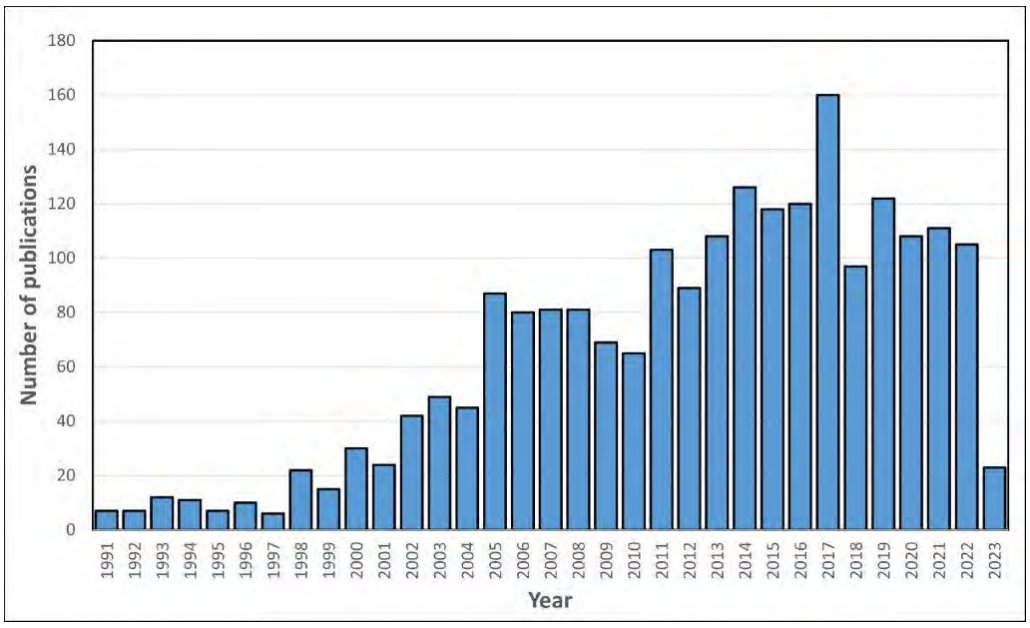


Figure 1.3: Publications between 1990-2023 for the CMUT field. This graph is created from the search string: "Capacitive Micromachined Ultrasonic Transducer* OR CMUT OR CMUTs OR Electrostatic Ultrasonic Air Transducer OR Capacitive Transducer* OR Surface Micromachined Transducer" OR Surface Micromachined Transducer" found using *Scopus* with a total of 2298 publications at the date of hand-in for this thesis.

In 2008, Park et al. first presented the use of a local oxidation of silicon (LOCOS) process for forming the CMUT cavities combined with fusion bonding [23]. LOCOS is the selective oxidation of silicon in specific regions, while the regions not intended for oxidation are coated with a thin usually nitride film that prevents the diffusion of oxygen. A comprehensive journal paper on CMUTs fabricated using a LOCOS process in combination with the fusion bonding technique was reported by the same group in 2011 [24]. local oxidation of silicon (LOCOS) is well-known for the tight gap control through thermal oxidation $\leq 10\,\text{nm}$, unparalleled uniformity across the wafer and low parasitic capacitance. Demonstrated by the gap height of 40 nm with a 2 nm uniformity across the wafer.
In 2009 Olcum et al. from Bilkent University presented an alternative wafer bonding technique by fabricating CMUTs with anodic bonding both tested in air and water [25]. In this technique, a glass wafer is structured for the cavities and bonded to a silicon substrate, which is then thinned to a specified plate thickness. Following that several 1D CMUT arrays utilizing anodic bonding have been published in which the group from North Carolina State University has been a front runner [26–28]. Some of the benefits of anodic bonding are the glass substrate minimizes cross-talk between the elements compared to silicon substrates. Also, in contrast to fusion bonding significantly less sensitive to particles or roughness at the bonding interface.
The first commercial CMUT probe was brought to the market by Hitachi in 2009 seen at the end of Fig. 1.2. A high-frequency 15 MHz 256-element 1D CMUT probe was announced in a collaboration between Kolo Medical Inc. and Verasonics in 2015 [29]. Since then more have followed, with the most influential being Butterfly Network, Inc. (Guilford, CT, USA) which launched an inexpensive and user-friendly CMUT probe named Butterfly iQ in 2019, which can be plugged directly into your phone and used for imaging. The progression of the CMUT research field can be observed in the graph in Fig. 1.3 with the number of publications per year.

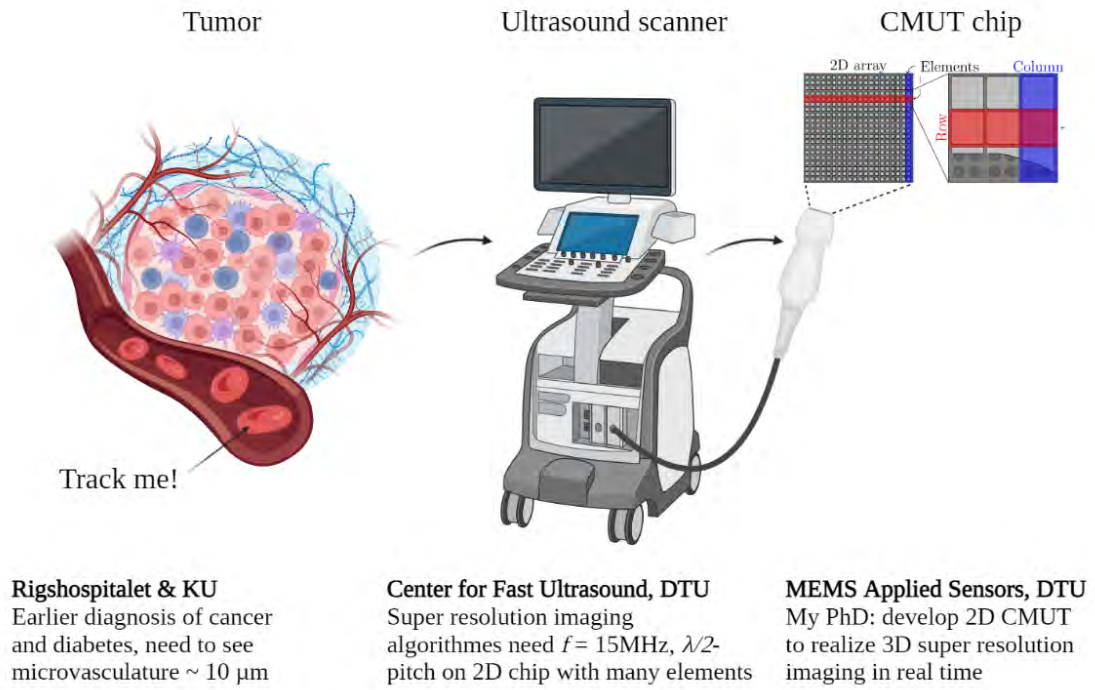


Figure 1.4: The goal of the SURE project and purpose of my Ph.D., is to develop a 2D CMUT array for 3D super-resolution ultrasound imaging in real-time, to hopefully detect cancer earlier by tracking the red blood cells. The aim of the SURE project is to disrupt the diagnosis of cancer and diabetes at a microvasculature level and impact current ultrasound.

1.3 The SURE project, motivation

This Ph.D. project is part of the Super Resolution Ultrasound Real Time Imaging of Erythrocytes in 3-D (SURE) project. An ERC-funded research project that aims to develop super-resolution non-invasive 3D ultrasound imaging without contrast agents by tracking the red blood cells in real time. This super-resolution visualization down to the smallest capillaries will be a paradigm shift in medical ultrasound and hopefully disrupt the diagnosis and treatment of especially cancer and diabetes. Evidently, any cardio vasculature disease in fact and true for all is that earlier diagnosis time is pivotal for the prognosis of the patients. This project is an interdisciplinary and iterative process and a collaboration between four research groups: Our own MEMS Applied-Sensors group at DTU developing state-of-the-art micro-fabricated transducers, Center for Fast Ultrasound Imaging (CFU) also at DTU researching advanced imaging systems and Rigshospitalet and Københavns Universitet (KU) with clinical expertise within rat models and human radiology for diabetes and cancer diagnoses. An overview of the goal of the SURE project, the research groups and my Ph.D. can be seen in Fig. 1.4. My part is essentially explained by the title of my Ph.D., the development of the "Micromachined 2D Transducers for 3-D super-resolution Ultrasound Real-Time Imaging of Erythrocytes". This thesis is on the development and fabrication of a large-scale special type of 3D-imaging array called a row-column CMUT. Furthermore, validating super-resolution entails highly specialized phantoms, which have also been part of this Ph.D. The end goal of the SURE project on the transducer side is to create an RC 1024+1024 CMUT probe or the so-called one million cell CMUT probe.

1.4 Super-resolution large scale arrays for 3D imaging

1.4.1 Achieving high resolution imaging

In order to achieve super-resolution imaging firstly requires a high frequency, f to obtain a high axial resolution and secondly, a wide aperture width of the ultrasound array to obtain a high lateral resolution, see Eq. 1.4.1.

Axial resolution **Lateral resolution** (1.2)

$$\lambda = \frac{c}{f} \qquad \text{FWHM} = \lambda \frac{\text{depth}}{\text{aperature width}} = \lambda \frac{Z}{N \times pitch}, \tag{1.3}$$

where λ is the wavelength, c is the speed of sound in the medium, and f is the emitted frequency. A wide aperture is necessary since the full-width half maximum (FWHM) of the point-spread-function (PSF) scales with the wavelength, λ times the ratio of the imaging depth, Z over the width of the aperture. The width of the aperture is equal to the pitch times the number of elements, N. Therefore, to achieve a higher resolution it is essential to have a high frequency, f and many elements N, hence large arrays. Furthermore, maintaining a good resolution throughout the human body requires a large array probe to maintain the ratio between imaging depth and width.
The periodicity of the array gives rise to constructive interference, which results in image artifacts in the form of grating lobes appearing as ghost echoes of off-axis objects. This degrades the image quality and contrast. In order to avoid this, a $\lambda/2$-pitch requirement is implemented to suppress the grating lobes by shifting them to -90°, thereby eliminating them from the transducer's field of view [3,4]. For example, with a center frequency of $f = 15\,\text{MHz}$ in immersion where the speed of sound is $c = 1450$ m/s the $\lambda/2$-pitch requirement is $51.33\,\mu\text{m}$. This is a fine pitch which is why semiconductor technology is the ideal fabrication choice.

1.5 3D imaging

Human anatomy is inherently 3D, reducing it to 2D will inevitably be at a cost of insufficient understanding of the complexity of the body. Naturally, the interest in 3D ultrasound has risen. 2D images are made using 1D arrays, while 3D images are typically made using 2D arrays. The utilization of a 1D array to create 3D images is not discussed here as it is impractical to create real-time volumetric images. The technique relies on sweeping a 1D array to create 3D images and requires stitching of the 2D image slices into a 3D image and it is unable to resolve fast out-of-plane motion used for i.e. blood flow estimation. The focus of this thesis is on the 2D arrays. The structure of a CMUT array from an element down to a cell is sketched in Fig. 1.5. An array is made up of elements, which consist of several CMUT cells. 1D arrays only have one set of N elements oriented in one direction, horizontally as seen in the top of Fig. 1.5. 2D arrays have two sets of elements orthogonal to each other, that is a matrix consisting of N rows and N columns. The overlap between a row and a column element is called a sub-element.

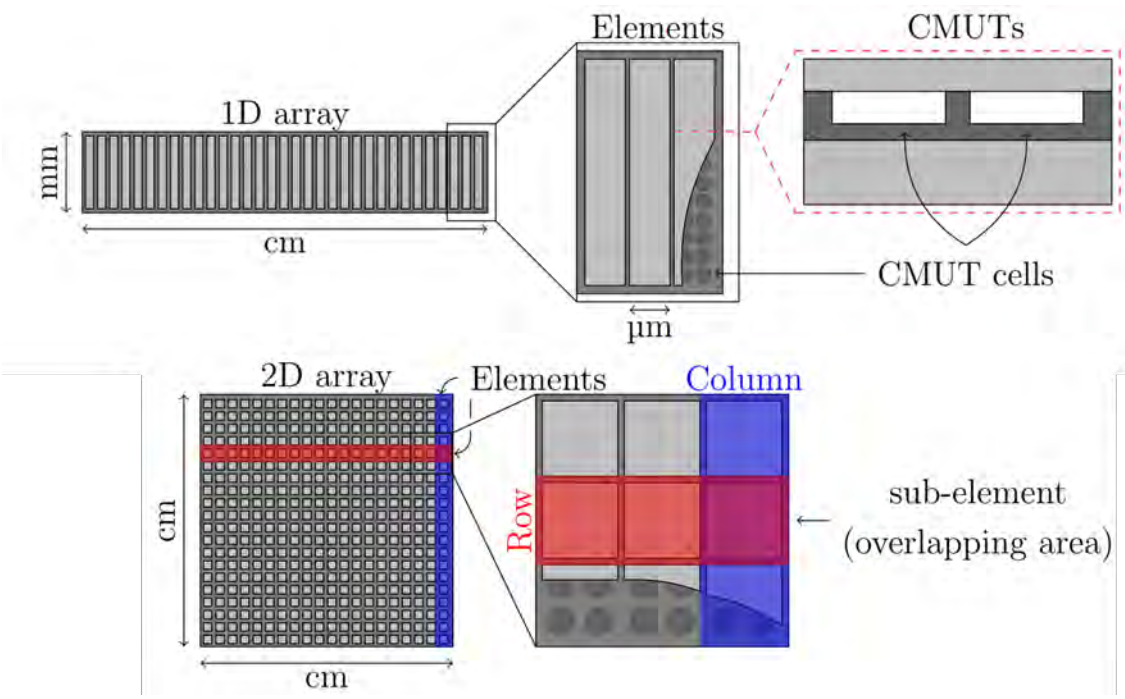


Figure 1.5: The structure of a 1D and 2D array, top and bottom respectively. 1D arrays consist of N elements that subsequently consist of CMUT cells that are the foundation stone. CMUT cells are shown in a cross-sectional view outlined by the red dashed line. 2D arrays are comprised of rows and columns elements. A sub-element is the overlap between a row and a column element. In the zoom-in, nine sub-elements are shown, where the top plate has been partially removed over the bottom row to show the structure and the placement of the CMUT cells. The 2D grey matrix array is the classical direct expansion of a 1D array which is an FPM array. The orthogonal overlapping red and blue marked rows and columns indicate another type of 2D array, namely the RC addressing scheme. Sketch kindly reprinted from [30].

1.5.1 Large-scale 2-D transducers

The chosen transducer scheme for achieving high-resolution, 3D imaging large-scale arrays in real-time has to meet the stated requirements described above. To create 3D images in real-time 2D transducers are used. First, there is the conventional fully populated matrix (FPM) array with $N \times N$ elements. This is an expansion of a 1D array N times in the orthogonal direction, seen as the grey array in the bottom of Fig. 1.5. Each sub-element needs to be individually connected amounting to N^2 interconnections. For a 512-element FPM array that is >262.000 electrical connections. This is an infeasible task. Secondly, there is also, the row-column array, which is essentially two orthogonal 1D arrays on top of each other. Where the elements overlap, marked as blue and red in Fig. 1.5, and thereby only creating $2 \times N$ connections which are just 1024 electrical connections. That is less than 1 % of the connections that are required for FPM, which seems possible to realize.
Some of the advantages that come with only having $2N$ electrical connections in the RC scheme are smaller and more manageable cables, simpler electronics, a higher frame rate which is a necessity for real-time imaging and easier packaging. Also, RC automatically has an equal number of elements in both directions that ensures the same resolution in both directions. The row-column addressing scheme was invented in 2003 by Morton (later Démoré) and Lockwood [31]. Rasmussen and Jensen showed through a simulation study that for the same amount of interconnections, RC will have a higher resolution than FPM [32]. RC shows promising results with high resolution in all three dimensions, making it a good candidate for real-time 3D imaging at high resolution throughout the whole of the human body [33]. On the basis of this, a row-column addressed array is utilized for this project.

1.5.2 Row-Column Addressed Arrays

As stated above, the row-column (RC) array was originally presented by Morton and Lockwood in 2003 [31]. In the following two decades until the time of writing, several research groups, as well as the industry, have explored the potential of the RC addressing scheme of several fabrication techniques, materials and array sizes.
Vermon and Verasonics offer commercially available row-column probes utilizing PZT, such as the RC6gV Row-Column Array Transducer probe featuring 128+128 rows and columns, operating at a center frequency of 6 MHz. Additionally, Daxsonics has recently introduced a prototype probe with 128+128 rows and columns, operating at a center frequency of 12 MHz. In academia, Seo et al. were the first to demonstrate a row-column array with the use of PZT material in constructing 64×64 and 256×256 arrays, in 2006 and 2009 respectively [34,35]. In another study, Chen et al. utilized a combination of PZT and a P[VDF-TrFE] copolymer for a 7.5 MHz transducer [36]. Latham et al. demonstrated the utilization of a PNM-PT electrostrictive ceramic to implement a 128+128 RC array [37]. In 2018, Engholm et al. presented two research probes, from our group in collaboration with BK Medical, that featured Two RC62+62 arrays, one based on PZT technology and the other on CMUT technology [38].

Row-Column Addressed CMUTs

In this section, only Row-Column Addressed CMUTs are considered and an overview of the fabrication techniques and research groups is presented in Table 1.1.

Table 1.1: This table provides an overview of fabrication techniques and groups involved in the development of Row-Column CMUT probes, but it is not an exhaustive compilation of all papers in the field.

Row-Column CMUT arrays

Technique	Last author	References
Sacrificial release method	R. Zemp	[39, 40]
Adhesive wafer bonding	E. Thomsen	[43]
Fusion bonding	J. Yeow, J. Jensen and E. Thomsen	[44, 45], [38, 47–49],
Anodic bonding	Ö. Oralkan, D. Certon, E. Thomsen	[52, 53], [50, 56], [54, 55]

The row-column addressing scheme has also been presented with a different more intuitive terminology called Top-orthogonal-to-bottom-electrode (TOBE) introduced by R. Zemp. for CMUT for 3D imaging in 2014 [39] using the sacrificial release method and demonstrated a 40+40 TOBE CMUT [40]. Furthermore, the research group presented adhesive BCB polymer-bonded 1D CMUT in 2020 [41]. Additionally, stated in [42] the long-term research aim is to fabricate 2D RC CMUTs that are flexible and transparent to enable 3D photoacoustic imaging. This research group fabricated a row-column BCB bonded CMUT array in 2017 [43].
Yeow and Logan were the first to present row-column arrays utilizing CMUT technology and demonstrated two RC32+32 fusion bonded CMUTs with a silicon nitride plate, with resonance frequencies in air with one at 15 MHz and one at 28 MHz in 2009 [44]. In the following years, a 32-element RC array with 110 % relative bandwidth [45] was shown in 2011 and a flexible 2D CMUT 32 + 32 elements row-column array in 2016 [46]. Our own research group showed a fusion bonded RC32+32 CMUT array utilizing fusion bonding in 2014 [47], a 62+ 62 row-column CMUT probe in 2015 [48] and two RC92+92 CMUT probes based on LOCOS and fusion bonding in 2018 [49] one with a diverging lens. Recently, a combination of fusion and anodic bonding was utilized to fabricate an RC190+190 CMUT probe for 3D ultrasound imaging by Grass. et. al in 2022 [50].
A 32+32 RC anodically bonded CMUT was introduced by Ö. Oralkan in 2016 [51] and characterization of an RC32+32 CMUT in 2018 [52] with further development in [53]. Certon demonstrated an RC64+64 CMUT probe fabricated with wafer bonding on borosilicate substrate [54] with a −6 dB bandwidth of 55 % [55] in 2022. An RC192+192 CMUT fabricated with anodic bonding was published in 2020 from this research group, where the author is the second author [56].
An overview of the publications on Row-Column, or TOBE, CMUT is found using the *Scopus* and seen in Fig. 1.6 as this is the topic of this thesis. The tendency resembles that of the overall CMUT publication graph in Fig. 1.3 observing from 2009. It should be noted that this graph is prior to the annual International Ultrasound Symposium (IUS), which serves as a major platform for publishing a significant number of CMUT papers.

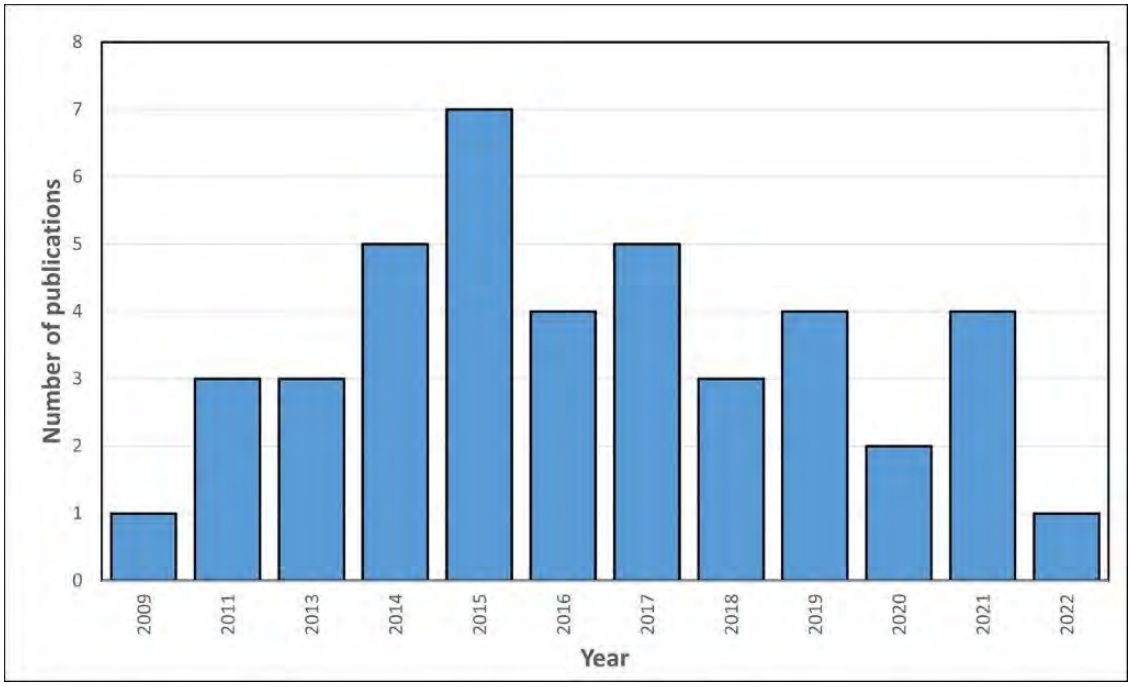


Figure 1.6: Number of annual publications over the years 2009-2022 for the Row-Column CMUT research field. This graph is created from the search string: "CMUT*" OR "Capacitive Micromachined Ultrasonic Transducer*" AND "Row-Column" OR "Row-Column Addressed*" OR "Row-Column Addressing" OR "TOBE" OR "Top-orthogonal-to-bottom-electrode" found using *Scopus* with a total of 42 publications at the date of hand-in for this thesis, May 31. 2023.

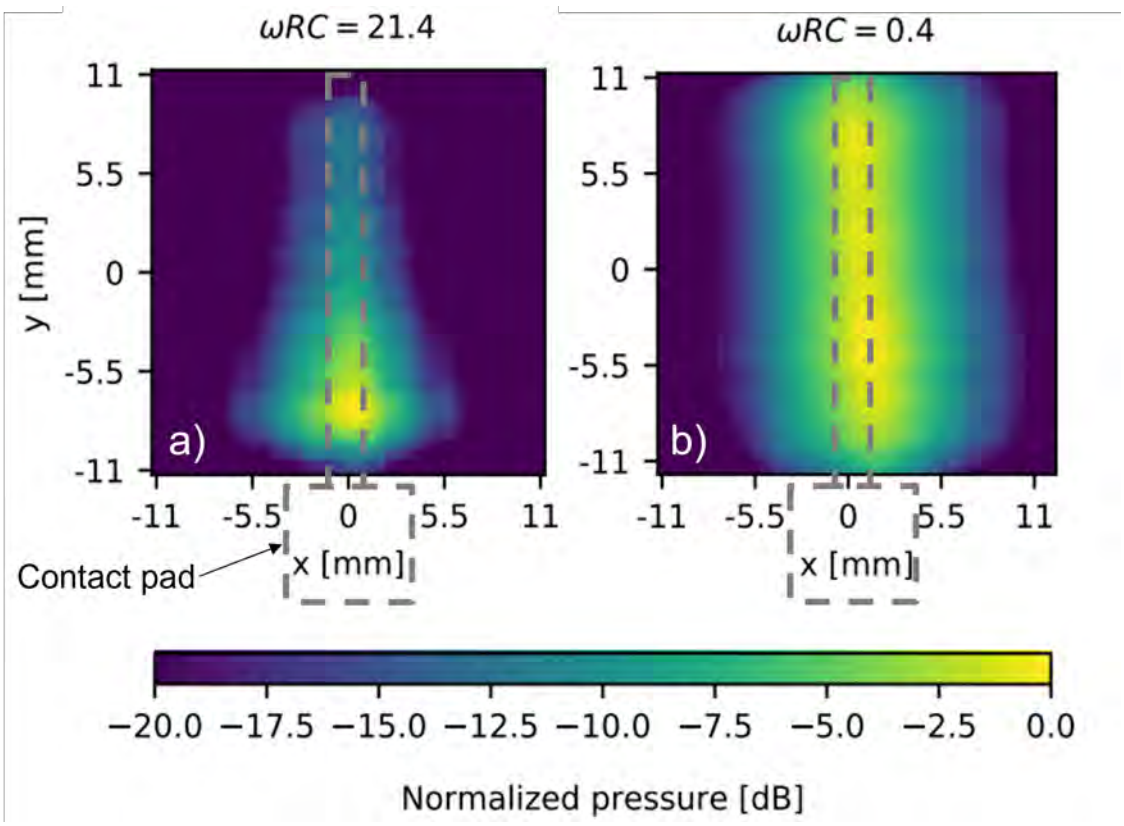


Figure 1.7: The average peak-to-peak pressure field for a 4.5 MHz probe is shown with the contact pad and element outlined by the dashed line. The pressure field was measured separately for the single bottom a) and top b) electrode. For the top electrode, the pressure distribution is uniform along the element. However, for the bottom electrode, the pressure reaches its maximum value near the contact pad, and then gradually decreases along the element. This attenuation is due to the high resistivity of the material, which causes the pressure to decay as it travels along the element. This discovery led to the formulation of the ωRC design criterion, which can be used to minimize this adverse attenuation of the pressure and thereby image quality. Kindly reprinted from [30].

1.6 Electrode resistance and the ωRC-criterion

1.6.1 Pressure uniformity for large-scale arrays

One of the challenges with large-scale arrays is that the elements become long thus increasing the resistance. This results in a voltage drop along the element which decreases the pressure output along the element. This was observed and visualized on the pressure map along the element seen in Fig. 1.7 reprinted from [30]. Therefore, the array design must ensure that the signal does not drop towards the end of the element and that uniform pressure is maintained for the image quality not to suffer. To address the issue of the acoustical attenuation of the signal along the element, especially long elements, a delay line model was developed previously in the group to explain this decreasing pressure field and a design criterion was formulated. The design criterion, denoted as $\omega RC < 0.35$, ensures that the attenuation along the element remains below 1 %. The ωRC product is a parameter that accounts for the electrical resistance R and capacitance C of the electrodes and the frequency of the excitation $\omega = 2\pi f$. This criterion helps in selecting the appropriate top and bottom electrode material and dimensions for large-scale arrays.
To mathematically describe how the AC signal along a CMUT element is attenuated,

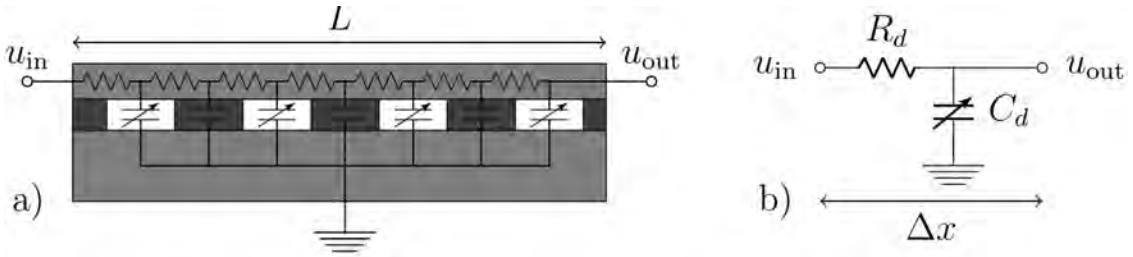


Figure 1.8: The Row-Column addressed CMUT array can be modeled as follows. In a) each Row-Column element can be idealized as a circuit with resistors representing the resistance through the element, variable capacitors representing the CMUT cells, and constant capacitors representing the parasitic capacitance. In b) when the capacitance of the CMUT cells and the parasitic capacitance are combined, the circuit can be described as a Resistor Capacitor (RC) delay line. Here, R_d and C_d represent the resistance and capacitance of a distributed segment of length Δx, and they are related to the total resistance and capacitance by $R_d = R/L\Delta x$ and $Cd = C/L\Delta x$, respectively. Kindly reprinted from [57].

a delay line model is utilized [57]. The model represents the element as a distributed network of resistors and capacitors, as shown in Fig. 1.8 a) for an equivalent circuit sketched on top of a CMUT element. The resistivity of the electrode determines the resistance of the resistors in the model, while the variable capacitors represent the CMUT cells and the constant capacitors represent the parasitic capacitance. By lumping the electrical components together, the electronic circuit can be described using a resistor-capacitor delay line model, as shown in Fig. 1.8 b). The element resistance R and capacitance C can be found by considering the contribution of each individual CMUT cell in the element. The resistance and capacitance of a length segment Δx of the entire element length L are represented by R_d and C_d, respectively

$$R_d = \frac{R}{L}\Delta x \qquad C_d = \frac{C}{L}\Delta x. \tag{1.4}$$

For each CMUT cell, the electrode resistance and the capacitance of the CMUT can be described by

$$R = \frac{\rho L}{hw} \qquad C = \frac{\epsilon A}{g}. \tag{1.5}$$

Where ρ is the resistivity, h and w are the thickness and width of the electrode and ϵ the relative permittivity, A is the cross-sectional area of the CMUT, and g is the gap height. The voltage distribution $u(x,t)$ along an element is described by the diffusion equation

$$\frac{\partial u(x,t)}{\partial t} = \frac{L^2}{RC}\frac{\partial^2 u(x,t)}{\partial x^2} \tag{1.6}$$

which depends on position x and time t in the limit where Δx approaches zero. The CMUT element is subject to the following two boundary conditions and initial condition [30]

$$u(0,t) = U_0 g(\omega t) \tag{1.7}$$

$$\frac{\partial u(x,t)}{\partial x}|_{\mathrm{x=L}} = 0 \tag{1.8}$$

$$u(x,0) = 0. \tag{1.9}$$

The first boundary condition gives the amplitude of the AC excitation voltage, U_0 along with the input excitation function $g(\omega t)$ applied at the contact pad, $x = 0$. The second boundary condition states that there is no current density at the end of the electrode, $x = L$. The initial condition states that no voltage is applied in the beginning, that is zero AC voltage at the time $t = 0$. Although the diffusion equation Eq. 1.6 does not have a closed-form solution, it can be solved analytically in the frequency domain with similar boundary conditions. This gives an expression for the voltage, $U(x,\omega)$ that can be represented as the product of the input excitation function $G(\omega)$ and the transfer function $H(x,\omega)$

$$U(x,\omega) = U_0 G(\omega) \cdot H(x,\omega) \tag{1.10}$$

$$H(x,\omega) = \frac{\cosh \kappa(1 - \frac{x}{L})}{\cosh \kappa}, \tag{1.11}$$

where $\kappa^2 = i\omega RC$. The signal preservation is found by taking the absolute magnitude of the transfer function H at the end of an element

$$|H(L,\omega)| = \frac{1}{|\cosh \kappa|} = \frac{1}{|\cosh(\sqrt{i\omega RC})|}. \tag{1.12}$$

To achieve a uniform acoustic pressure, a guideline based on an ωRC criterion of

$$\omega RC < 0.35 \tag{1.13}$$

corresponding to a 1 % potential drop at the end of an element is utilized as a design criterion. The magnitude of the transfer function, $|H(L,\omega)|$ describes the percentage of preserved signal strength and the 99 % is marked in green in Fig. 1.9 a) corresponding to $\omega RC < 0.35$ with a phase of $-9.7°$ seen in b). Designs are also feasible with attenuation of 10 % or preserving a signal strength of 90 %, then $\omega RC < 1.18$ which is also indicated in the figure.

1.6.2 The importance of ωRC for large arrays

Proceeding with the design considerations to ensure uniform pressure along the element by utilizing this ωRC-design criterion. The ωRC product is proportional to the resistivity, ρ times the length of the electrode squared, L^2 divided by the thickness of the electrode, h which can be described by this proportionality

$$\omega RC \propto \frac{\rho L^2}{h}. \tag{1.14}$$

The frequency, ω and capacitance, C are more or less locked by requirements and other design parameters, but the resistance R can be minimized. The optimal electrode design to minimize resistance and thereby the signal attenuation can be achieved by: decreasing the length, L increasing the thickness, h and reducing the

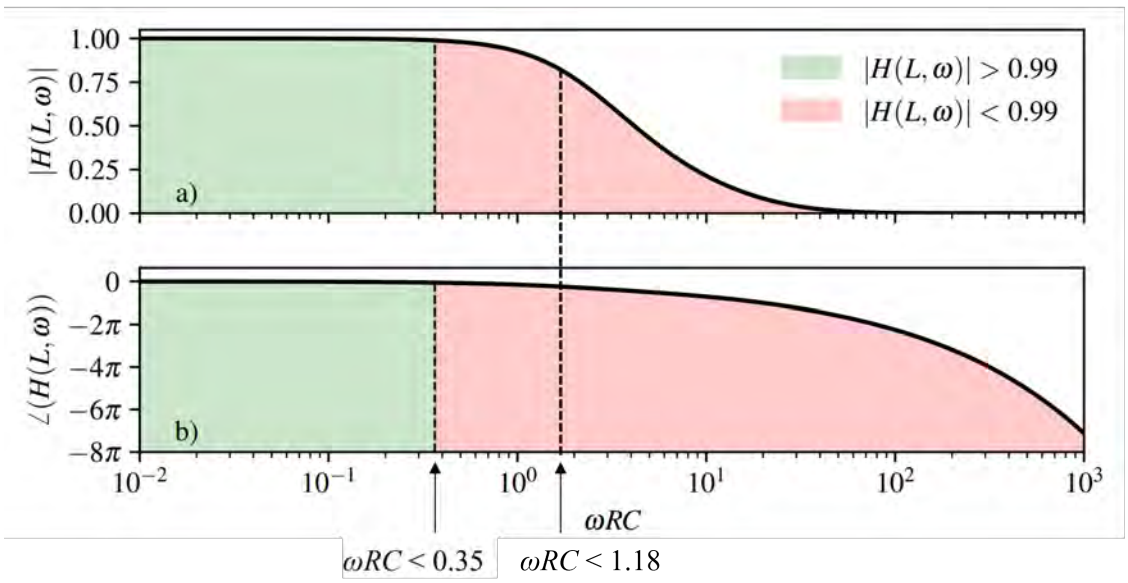


Figure 1.9: Illustration of the transfer function H at the end of the element (x = L) as a function of the ωRC product. The green region indicates that the magnitude of the transfer function is above 0.99 and the red region indicates a magnitude less than 0.99. a) shows the absolute magnitude at the end of an element, where the first dashed line indicates the 0.99 magnitude threshold and the second line the 0.9 thresholds. Corresponding to 1 % and 10 % attenuation, respectively. b) shows the phase delay at the end of an element, with the 0.99 and 0.90 magnitude threshold also indicated on this plot. The criterion corresponds to a delay at the end of -0.17 radians or -9.7 degrees for the 1 % attenuation. This plot is reprinted from [57].

resistivity of the electrode, ρ. Now with this squared dependency, L^2 the ωRC criterion becomes especially important for large-scale row-column arrays, as they become long. The consequence of a large-scale array is easily shown by a short example.

In Table 1.2 three arrays ranging from 1 cm to 5 cm in length, with element numbers utilized in the project, are shown for bottom electrodes made of gold, Au and chromium, Cr, titanium disilicide, $TiSi_2$ and doped silicon, Si with a varying electrode thickness, h. All values are calculated for a 15 MHz, $\lambda/2$-element pitch array. The element consists of a single cell per sub-element. For simplicity, the capacitance is estimated from that of a metallic structured bottom electrode. This is a coarse assumption, however, it will help illustrate the point. The detailed calculations for the values presented in Table 1.2 are described in Section 2.6. If realized for a 512-row-column element in chromium it would result in only 57 % of the signal reaching the end of the element, whereas if the electrode was made of gold a total of 95 % of the signal would be preserved at the end of the element. This effect is not prominent for small-scale arrays as the RC190+190 obtain a signal strength of 98 % to 100 % independent of materials, but undeniable for large-scale arrays as the RC1024+1024 only reach 14 % with 20 µm doped silicon and 95 % with 1 µm gold. This is only a problem for bottom electrodes as they are restricted in thickness, and material and have to account for later processing which all need to be compatible with each other. Whereas, the top electrodes are fabricated at the end of the process where the metal can be readily implemented without consideration of the thermal budget. Furthermore, there is no limit to the thickness of the top electrodes, as they can just be increased as needed to achieve an acceptable level of pressure uniformity.

Having emphasized the impact of the length that is automatically going to increase when fabricating large-scale arrays will have on the pressure uniformity, it becomes important to consider which materials and methods are viable to achieve this goal of ultimately a 1024+1024 RC probe. Three materials for the bottom electrodes are considered: doped silicon, titanium disilicide and gold, to determine the best choice to achieve high-performance large-scale arrays.

To create the CMUT cavities with a bottom electrode made of highly doped silicon a technique known as LOCOS is typically used in combination with fusion bonding to a Silicon-on-Insulator (SOI) wafer as top wafer with a thick layer of deposited metal as the top electrodes. Previously, doped silicon has been used for bottom electrodes for the first row-column arrays fabricated in this group. It was here the delay line attenuation was discovered and the ωRC criterion formulated. The results of using doped silicon electrodes are shown in Fig. 1.7 where the consequence of the electrode resistance, described in terms of ωRC and pressure map is evident. Utilizing doped silicon electrodes can only bring us so far as to the RC190+190 array as seen in Table 1.2 with a reasonable electrode thickness of 20 µm. Reaching an RC1024+1024 with doped silicon would require the use of bottom electrodes as thick as a normal silicon wafer which is highly impractical.
Consequently, other materials with lower resistivity, namely titanium disilicide, $TiSi_2$ and metals are explored. Titanium disilicide, $TiSi_2$ has a high thermal stability up to 980 °C. Therefore, bottom electrodes made of titanium disilicide can be realized with a slight temperature altered LOCOS in combination with fusion bonding. Furthermore, another and novel CMUT fabrication technique with titanium disilicide bottom electrodes is explored in this Ph.D. and presented in chapter Section 8.1. As observed in Fig. 1.10 titanium disilicide facilitates RC512+512 at a thickness of just 250 nm and even RC1024+1024 at 1 µm, this promising aspect is why a considerable part of this Ph.D. study was dedicated to investigating the potential of this technology.
Finally, examining the metals. Comparing chromium, Cr with an ideal low resistivity titanium disilicide, $TiSi_2$-C49 the resistivity is almost equivalent. However, utilizing metal limits the thermal budget substantially usually to below 400 °C and the CMUT fabrication technique available to implement metal is anodic bonding. Anodic bonding utilizes a borosilicate glass substrate with etched cavities using deposited metal as the bottom electrodes. The top plate will be composed of a poly-silicon-based SOI wafer with a thick layer of deposited metal as the top electrodes. On the contrary, comparing gold, Au with titanium disilicide, $TiSi_2$-C49 the resistivity is approximately 4 times lower and when compared to doped silicon it's even 3 orders of magnitude lower. The low resistivity of gold is a substantial advantage. In pursuit of ultimately realizing the RC1024+1024 probe a 1 µm gold bottom electrode obtains a satisfactory signal at the end of such a long element as seen in Table 1.2. Therefore, gold electrodes are utilized, which limits the thermal budget, thus the robust anodic bonding process is chosen and will be described in chapter Section 3.2.

Table 1.2: Signal strength at the end of an element for three row-column array sizes of 190+190, 512+512 and 1024+1024 elements. All are calculated at 15 MHz and an element capacitance in the increasing order: 12 pF, 34 pF and 68 pF.

		Signal strength at the end of the element in %								
		Gold, Au		Chromium, Cr		Titanium silicide, $TiSi_2$-C49		Doped Silicon, varying h		
		$\rho = 3.15\,\mu\Omega$cm		$\rho = 15\,\mu\Omega$cm		$\rho = 13\,\mu\Omega$cm		$\rho = 4.3 \times 10^{-3}$		Ωcm
Array size	**Elements, N**	250 nm	1 µm	250 nm	1 µm	250 nm	1 µm	250 nm	20 µm	500 µm
0.97 cm^2	190+190	100	100	98	100	100	100	2.4	98	100
2.61 cm^2	512+512	95	100	57	94	94	99	0.001	31	99
5.22 cm^2	1024+1024	58	95	14	57	57	94	8.5 $\times 10^{-9}$	14	97

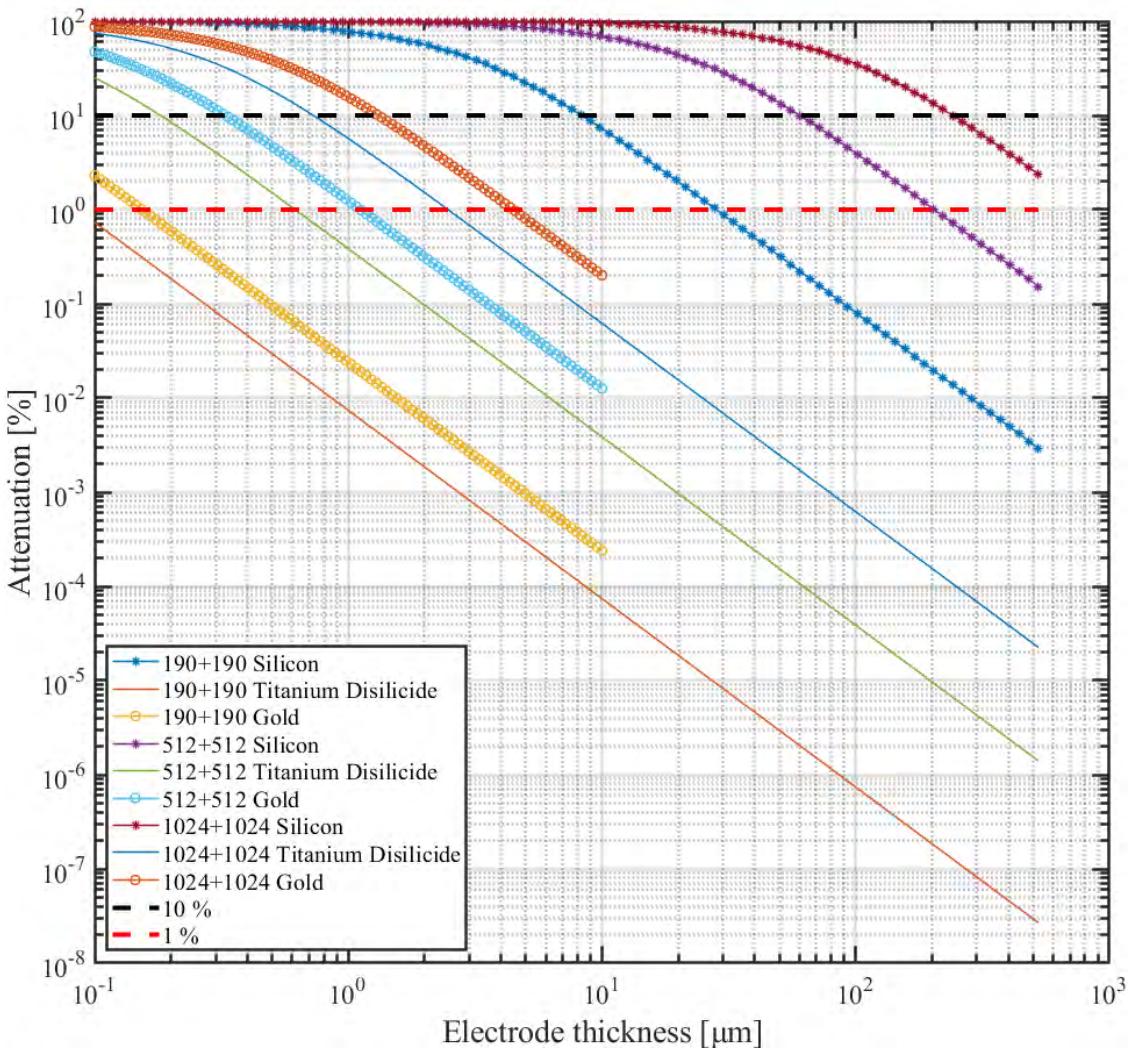


Figure 1.10: An attenuation plot based on the ωRC-criterion for thicknesses of three different bottom electrode materials silicon, titanium disilicide and gold. This plot is calculated the same way as Table 1.2.

1.7 Main challenges with large-scale chips

With the aim of realizing this large-scale 2D RC1024+1024 CMUT array, several challenges are met which will be summarized briefly. The requirements for the RC CMUT array are a center frequency of 15 MHz and a $\lambda/2$-pitch with 1024+1024 elements to achieve 3D super-resolution ultrasound imaging in real-time. This results in an element pitch of 51 µm and a chip area of 5.3 cm× 5.3 cm with a single cell with a side-length of 37 µm per sub-element.

In terms of the cleanroom fabrication process, this entails fabricating 1.000.000 error-free CMUT cells i.e. top-to-bottom short circuits have to be eliminated. One short circuit per 1.000.000 cells corresponds to 0.001 ‰. A disadvantage of the row-column addressing scheme is that a vertical short affects both the row and the column element and any other elements that may be connected to either one, accelerating the complexity and consequence of these vertical shorts immensely. To give an example a smaller RC16+16 array, with the same cell size of 37 µm and a total of 9216 cells, was characterized. Impedance measurements showed 7 short circuits between the top and bottom elements. The location of these 7 short-circuited cells was sporadically scattered across the array and resulted in a 40 % loss of functional elements. Transferring this to shorts per cell, as the cell size is identical, it amounts to only 0.08 % shorted CMUT cells reducing the element yield to almost half.

Following the discussion above, the bottom electrodes must adhere to the specified ωRC-design criterion to avoid adverse attenuation and the electrode material should be process compatible and feasible within microfabrication technology.

The structural yield requires a void-free area of at least 28 cm^2. To accomplish this high-quality and voids-free bonding, it is necessary to maintain a high level of cleanliness, perform precise polishing, and ensure uniformity control with smoothness at the sub-nanometer level. The particle level should ideally be a class 10 cleanroom or better, particle size $\leq$ 0.5 µm and surface roughness below 50 nm [58,59]. As a larger area is required, that means that the demands for consistency increase. That means that processing across the wafer needs to be uniform for example the etching of the glass cavities need to be uniform so that the pull-in voltage does not deviate across the array risking that some cells or even entire elements go into pull-in during operation. A similar problem is true for the top plate, where the thickness uniformity is determined mainly by the polishing process which was optimized in this thesis to have a minimal removal rate and a sub-nanometer surface roughness. Discrepancies in the plate thickness ultimately result in variations in the resonance frequency. For the electrical properties of the top PSOI wafer, the thickness of the dielectric layers as well as the breakdown voltage and amount of impurities are equally important.

Additionally, fabricating a 5 µm wide and a total of 51 µm $\times$ 1024 $\times$ 1024 = 53 m long top electrode kerf without any errors is necessary to avoid top to top short circuits. The equivalent of half an American football field needs to be inspected by a microscope with 5 µm resolution in order to localize defects. Acquiring this manually would take more than 100 days, hence automatic visual inspection is required for front-side defect detection. Moreover, backside inspection for the RC190+190 generates above 9000 images which need to be inspected for around 5 µm $\times$ 5 µm sized defects underlining the need for automated imaging recognition. Similarly, for electrical characterization, at least 2048 measurements should be performed assuming that all knowledge can be achieved by just impedance, Zf measurements prior

to wire bonding. After wire bonding another 2048 measurements and accordingly, after mounting, casting and probe assembly yet another 2048 measurements at the minimum to ascertain the functionality of the finalized ultrasound probe. The bare minimum would be 6144 electrical measurements to fully describe the impact each part of the probe assembly process might have, if any, on the performance of the array.

1.8 The three parts of this thesis

Part I is the main part of my Ph.D. work regarding the development and fabrication of anodically bonded row-column CMUTs for both the RC 190+190 and the scaling to the RC 512+512.
Part II concerns the 3-D printing of specialized hydrogel phantoms used to validate super-resolution ultrasound imaging at our collaborators at CFU.
Part III is the investigation and first attempt at fabricating a novel process flow of quartz fusion titanium disilicide CMUTs.

1.9 Publications

The work done in this thesis has contributed to the following publications of which the author is either a main or co-author listed below:

Paper A *Anatomic and Functional Imaging using Row-Column Arrays*, Jensen, J. A., Schou, M., Jørgensen, L. T., Tomov, B. G., Stuart, M. B., Traberg, M. S., Taghavi, I., Øygard, S. H., Ommen, M. L., Steenberg, K., Thomsen, E. V., Panduro, N. S., Nielsen, M. B. and Sørensen, C. M., 1 Jan 2022, In: IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control. 69, 10, p. 2722-2738 9830770.

Paper B *Compensation for Velocity Underestimation in 2D Super-Resolution Ultrasound*, Taghavi, I., Amin-Naji, M., Schou, M., Ommen, M. L., Steenberg, K., Larsen, N. B., Thomsen, E. V. and Jensen, J. A., 2022, Proceeding of 2022 IEEE International Ultrasonics Symposium (IUS). IEEE, 3 p.

Paper C *Synthetic Aperture High Quality B-mode Imaging with a Row-Column Array Compared to Linear Array Imaging*, Jensen, J. A., Schou, M., Ommen, M. L., Steenberg, K., Thomsen, E. V., Tomov, B. G., Panduro, N. S., Sorensen, C. M. and Stuart, M. B., 2022, Proceedings of 2022 IEEE International Ultrasonics Symposium. IEEE, 4 p.

Paper D *Polysilicon on Quartz Substrate for Silicide Based Row-Column CMUTs* Steenberg, K. and Thomsen, E. V., 2021, Proceedings of 2021 IEEE International Ultrasonics Symposium. IEEE, 4 p.

Paper E *Large Scale High Voltage 192+192 Row-Column Addressed CMUTs Made with Anodic Bonding* Grass, R. S., Steenberg, K., Havreland, A. S., Engholm, M. and Thomsen, E. V., 2020, 2020 IEEE International Ultrasonics Symposium (IUS). IEEE, 4 p.

Furthermore, the author participated in the IEEE International Ultrasonics Symposium (IUS) in 2020 and 2021 online due to the Corona pandemic and gave a virtual poster presentation on "Polysilicon on Quartz Substrate for Silicide Based Row-Column CMUTs" (Paper D) and this novel fabrication technique is presented in Chapter 8. Finally, in 2022 the author participated physically at the conference and held an oral lecture on "Design and Process Development for Large-Scale Row-Column CMUT Arrays" presenting the work performed on the RC 512+512 CMUT array. The findings and outcomes, discussing the design and process development for large-scale row-column CMUT arrays, are documented in the chapters Chapter 2, Chapter 3, Chapter 4 and Chapter 5.

Articles in preparation

Two articles are presently in preparation, both were planned for the last half year of this PhD study.

An article presenting the RC190+190 implemented in a prototype probe was scheduled for the last six months, however, wire bonding proved immensely difficult and unexpected challenges emerged. The article would present the very first prototype probe where every aspect from the design, cleanroom fabrication, electrical characterization as well as wire bonding, mounting and casting into a complete ultrasound probe with acoustic measurement and safety testing was performed entirely within this research group.

The article concerning the RC512+512 was planned to be written in the spring of 2023, unfortunately, due to the ion beam etcher being out of operation for the last five months, the article has been postponed. The article would contain the fabrication and optimization of this unprecedented RC512+512 CMUT array.

Chapter 2

Design

In the previous introduction chapter for the thesis, the argument for utilizing the row-column addressing (RCA) scheme to achieve super-resolution 3D imagining in real time was given. As discussed, this necessitates a 2D row-column CMUT array with numerous elements to achieve high-resolution 3D volume capture with a $\lambda/2$-element pitch. Consequently, the natural progression entails the utilization of large arrays to accommodate these elements. When designing such large RCA arrays, several essential criteria need to be considered to achieve optimal performance which will be described in this chapter. Starting with the requirements and calculation of the design parameters for the cell design, and progression towards the mechanical and electrical properties of the array. Finalized with an overview of the wafer map.

2.1 Introduction

Designing a CMUT array is a complex process where everything from available tools and materials to electrical characterization and probe implementation needs to be taken into account. Although many of the design parameters can be determined by relying solely on the analytical expressions, the equations used for calculating the plate thickness, h depend on the deflection model for single-layer, thin plates. Most arrays previously presented in this research group, including the author's arrays, fall under the category of thick plates, $h/a \geq 0.1$ where a is the half side length of the CMUT cell. Therefore, the use of thin plate models may lead to some degree of uncertainty. Consequently, analytical expressions combined with FEM simulations are used to determine the design parameters.

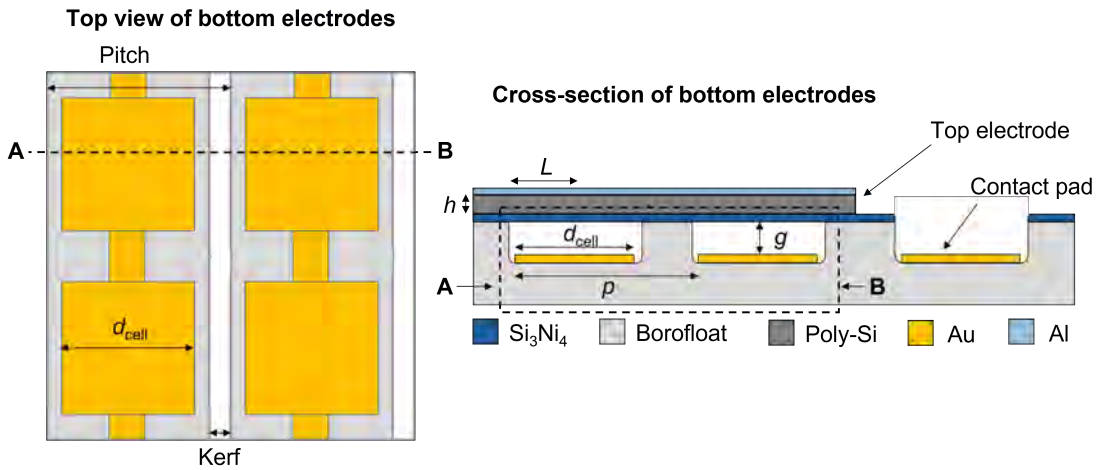


Figure 2.1: Sketch of the top view and cross-sectional view of the bottom electrodes. The top view shows two elements with the element pitch, p and the kerf, d_{eff} together with the cell size and the dashed cut-line marked A-B for the cross-sectional view. The cross-section shows the complete RC CMUT with the side length of the cell, d_{cell}, the vacuum gap g along with the top plate thickness h and the pitch, p. Furthermore, the different materials are color-coded and the top electrode and contact pad are labeled.

2.2 CMUT design methodology

The important points in the design process are listed below, and each point will be elaborated in the following sections. These parameters are to be calculated:

- 1) The $\lambda/2$-element pitch from the given center frequency in immersion
- 2) The sub-element layout: kerf, bonding width, cell size
- 3) Number of CMUT cells, a trade-off between pressure and bandwidth
- 4) Fit cells into the element, determine the cell size
- 5) Find the plate thickness, h to match the immersion frequency
- 6) Select pull-in voltage, V_{pi} compatible with the scanner
- 7) Adjust gap, g to reach the pull-in voltage
- 8) FEM simulations to ensure all specifications are met
- 9) Adjust electrode thickness and dimensions to meet the ωRC criterion.

2.3 CMUT array design

In Fig. 2.1 an overview of the array design is sketched for both a top and cross-sectional view of the bottom electrodes as a help for the reader to give a visual representation of some of the listed parameters in the CMUT design methodology.

Table 2.1: Requirements for the 2D CMUT arrays from our collaborators at CFU to realize super-resolution real time ultrasound imaging.

Array	Elements	Frequency	$\lambda/2$ pitch	Apodization
RC	190+190	8 MHz	95 µm	Yes
RC	512+512	15 MHz	51 µm	No

2.4 Requirements and specifications

Requirements from our collaborators at CFU, developing the imaging algorithms, are stated in Table 2.1 from which the transducer is designed. Two different 2D arrays have been developed by the author during the Ph.D., for 8 MHz and 15 MHz, respectively. The restriction of a $\lambda/2$ pitch pushes back the directionality of the grating lobes to -90°, eliminating them from the transducer surface. Grating lobes are a result of constructive interference of the periodicity of the array, which can be described by diffraction and create image artifacts of off-axis objects generating ghost echos in the ultrasound image [3]. The specification of apodization is a question of edge waves. The objective is to roll off or gradually reduce edge waves in signal amplitude from 1 to 0, usually done with a Hanning window to suppress the side lobes. The reason why there is no apodization on the RC 512+512 array is based on the simulations done in Field II by Associate Professor Mathias Bo Stuart at CFU. The task is now to determine the sub-element layout, the kerf, the cell size and number, the bonding width, and the plate thickness.

2.5 Calculating design parameters

The specifications from Table 2.1 predetermine the number of elements, the center frequency f, and the $\lambda/2$-pitch. Thereby, locking the design as the frequency combined with the $\lambda/2$-requirement directly gives the element pitch and impacts the realizable half-side length, L of the CMUT cell. The definitions of the element pitch, p, kerf, d_{eff} and the side length, d_{cell} can be seen in Fig. 2.2 for a sub-element with multiple cells. The sketch also shows the bonding width, $d_{\text{bondWidth}}$ which is the required clamping width of the cell to be able to emit sound. If there are multiple cells in a sub-element, the separation between the cells $d_{\text{cellSeparation}}$ should be at least twice the minimum bonding width to ensure enough area for bonding. The definition of the minimum bonding width is explained in Eq. 2.2. The sub-element parameters can be found from the equation [60]

$$p = nd_{\text{cell}} + d_{\text{eff}} + (n-1)d_{\text{cellSeparation}} + 2d_{\text{bondWidth}}, \tag{2.1}$$

where n is the number of cells in the vertical direction. A trade-off between the number of cells, n, and plate thickness, h is to be made in regard to pressure output and bandwidth and is explained in Section 2.5.2.
The bonding width is calculated from the effective radius theory developed by Ph.D. student Stine L. G. Pedersen and Prof. Erik V. Thomsen, see appendix A [61]. Traditionally, it is assumed that the plate is clamped to the edge of the cell. Contrary to this, the effective radius theory takes into account the stress distributed out into the plate region beyond the cavity. The effective radius is $a_{\text{eff}} = a + ch$, where a is the radius for circular cells or the half-side length for square cells, h is the thickness of the plate and c is a constant found from simulations of varying the clamping point

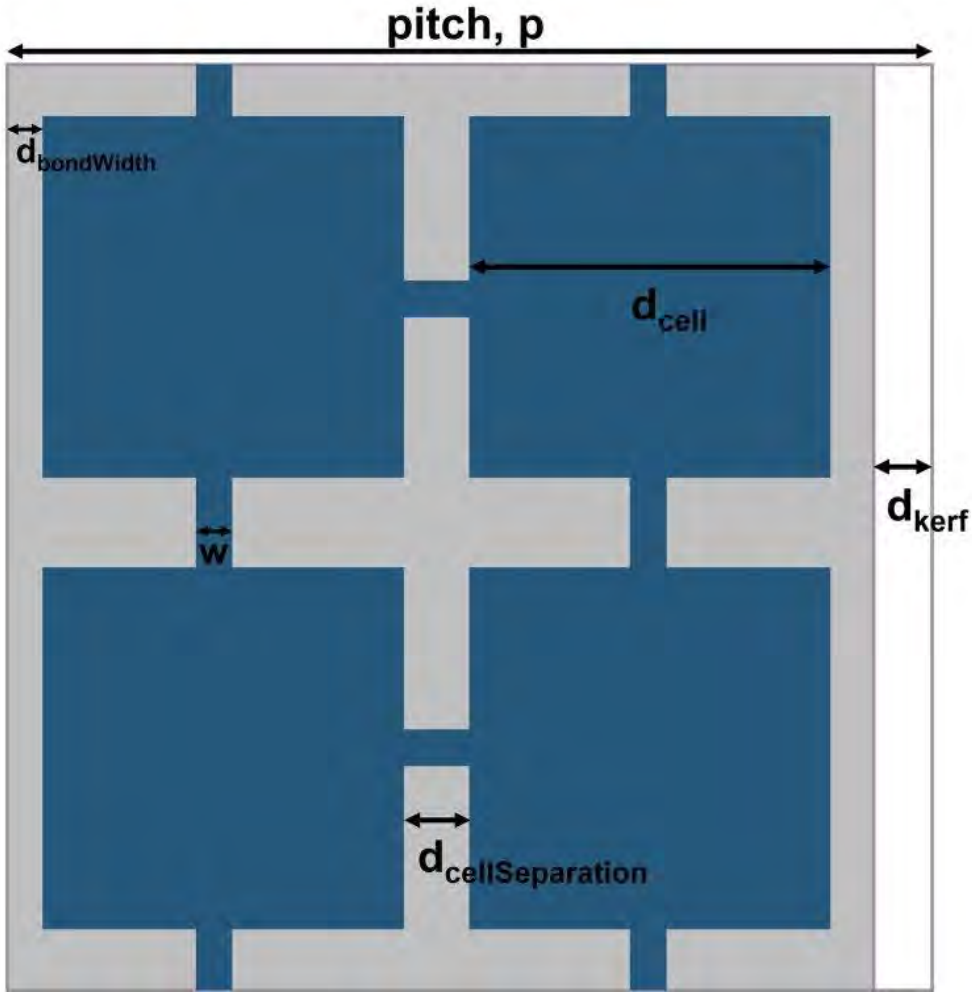


Figure 2.2: Sketch of sub-element parameters outlining the element pitch, p , kerf, d_{eff}, the side length of the cell, d_{cell}, and the cell separation $d_{\text{cellSeparation}}$ of at least twice the minimum bonding width to ensure enough area for bonding. The number of cells, n in the vertical direction in this case two, resulting in 4 cells per sub-element.

of the cell comparing clamping to the inner edge and elastic clamping into the outer edge in COMSOL. The fitted value is $c = 0.6$, giving the restraint of a minimum bonding width and cell separation of

$$d_{\text{bondWidth}} \geq c \cdot h = 0.6 \cdot h \quad \text{and} \quad d_{\text{cellSeparation}} \geq 2 \cdot d_{\text{bondWidth}}. \tag{2.2}$$

To calculate the mnimum bonding width, $d_{\text{bondWidth}}$ it is necessary to know the plate thickness, h.

2.5.1 Plate thickness h

To reach the desired frequency in immersion, the thickness of the plate h is the decisive factor as the half-side length is fixed by the width of the element. In this section, it is assumed that the top plate consists of single material typically a silicon plate and for our CMUTs a polysilicon (poly-Si) plate is used. Later, multiple layers are used in the FEM simulations for the top plate. Calculating the plate thickness is done from an energy consideration using a Rayleigh-Ritz method by Lamb [62]

$$\frac{\omega_r}{\omega_0} = \frac{1}{\sqrt{1+\beta}} = \frac{1}{\sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}}} \tag{2.3}$$

giving the relationship of the resonance frequency ratio ω_r/ω_0, in immersion over that in vacuum. The medium in front of the vibrating plate can be modeled as an added mass of the plate described by the proportionality non-dimensionalized added virtual mass incremental factor (NAVMI), Γ depending on the clamping conditions. The plate's behavior is also influenced by the aspect ratio of the plate radius over the plate thickness, a/h and the ratio of densities between the immersion medium and the plate material, ρ_m/ρ_p. This is valid for thin plates i.e. $h/a \leq 0.1$. The values are $\Gamma = 0.6689$ calculated by Lamb for circular plates, for silicon $\rho_p = 2.330$ g/cm^{-3} and for water $\rho_{m,water} = 1.000$ g/cm^{-3}. However, the added mass that oscillates with the plate is actually the encapsulating material, Polydimethylsiloxane, polymer (PDMS) of $\rho_{m,PDMS} = 1.300$ g/cm^{-3}. The resonance frequency of a clamped plate in a vacuum, ω_0 is well-described in mechanical engineering as [63]

$$\omega_0 = 10.328\sqrt{\frac{D}{a^4 h \rho_p}} = 10.328\sqrt{\frac{Y}{12(1-\nu^2)\rho_p}}\frac{h}{a^2}, \tag{2.4}$$

where Y is Young's modulus and ν is Poisson's ratio of the plate material. For which an average of $Y = 148$ GPa is taken for poly-Si and $\nu_{[100]} = 0.3$ for silicon [100], however a mean value between the [100] and [110] direction gives $\nu_{poly-Si} = 0.117$ [64], which is more accurate for poly-Si. Combining Eq. 2.3 and Eq. 2.4 an expression for the resonance frequency is found

$$\omega_r\sqrt{1+\Gamma\frac{a}{h}\frac{\rho_m}{\rho_p}} = 10.328\sqrt{\frac{Y}{12(1-\nu^2)\rho_p}}\frac{h}{a^2}. \tag{2.5}$$

From this the plate thickness can be determined by using a = a_{eff} along with the center frequency, $f = 2\pi\omega_r$. This was a purely analytical approach, realistically it is a multi-parameter decision.

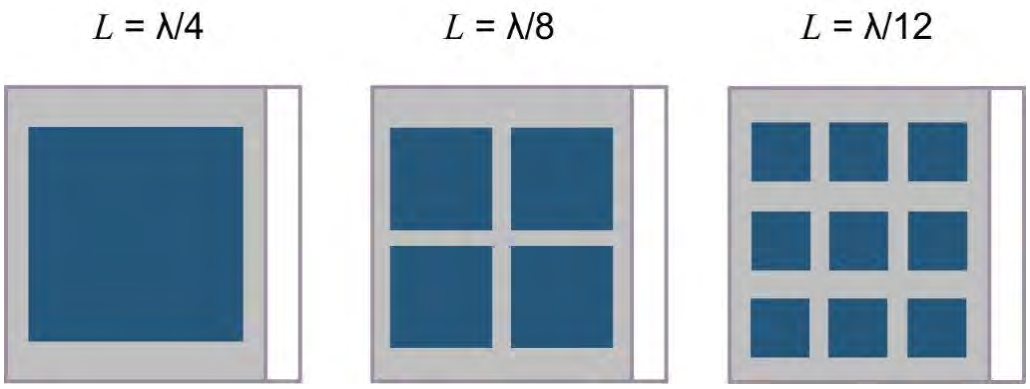


Figure 2.3: A sketch of the cell sizes that can be chosen based on the wavelength assuming a $\lambda/2$ pitch and that all other sub-element parameters are ignored. Also presented in Eq. 2.6.

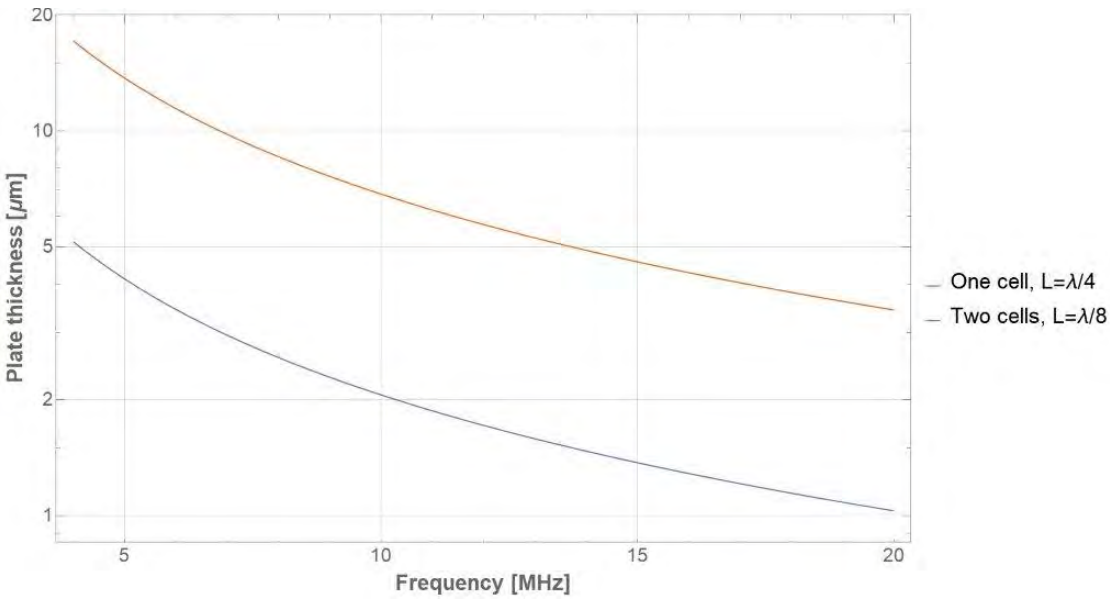


Figure 2.4: This plot is kindly reprinted from the lecture material made by Prof. Erik V. Thomsen and Ph.D. student Stine L. G. Pedersen. Plate thickness over frequencies for one cell with a half-side length of $\lambda/4$ and two cells with a half-side length of $\lambda/8$.

2.5.2 Number of cells and plate thickness

The pitch is ultimately locked by the $\lambda/2$-requirement and within that space, a half-side length of $L = \lambda/m$ can be chosen, where $\lambda/m = \lambda/4, \lambda/8...$ as illustrated on Fig. 2.3. If all other sub-element layout parameters (kerf, etc.) are ignored, the largest possible half-side length of the cell is $L = \lambda/4$ occupying the entire space. For n cells the half-side length L will be

$$n = 1 \quad L = \lambda/4 \tag{2.6}$$
$$n = 2 \quad L = \lambda/8 \tag{2.7}$$
$$n = 3 \quad L = \lambda/12. \tag{2.8}$$

A visual representation of this is sketched in Fig. 2.3.
A plot of plate thickness versus frequency can be drawn from Eq. 2.5 for the case of 1 and 2 cells in Fig. 2.4. For the two designs in this thesis, a frequency of 8 MHz and 15 MHz is desired. Within this window, the plate thicknesses are visually represented

Table 2.2: An overview of the plate thickness h for the two frequencies in this thesis for a sub-element with one cell with a half-side length of $L = \lambda/4$ and a two cell design with a half-side length of $L = \lambda/8$. These half-side lengths are based on the assumption that all other sub-element layout parameters like kerf, bonding width and cell separation are set to zero. Therefore, this is only a preliminary guideline to get a feel of the design space.

	Plate thickness h	
Cells per sub-element	**8 MHz**	**15 MHz**
One cell, $L = \lambda/4$	8 µm	4.1 µm
Two cells, $L = \lambda/8$	2.5 µm	1.3 µm

by Table 2.2. The plate thickness needed for these frequencies should be realizable with the polysilicon-on-insulator (PSOI) technique [65], where 1-5 µm thick poly-Si plates can be obtained after polishing. As well as being thick enough to endure handling in the cleanroom i.e. withstand a vacuum suction and a 1 bar back pressure on the membrane. Also, the plate should be able to endure an accidental drop test. Furthermore, choosing one or two cells is a trade-off between pressure and bandwidth where the thickness of the plate will have to be adjusted accordingly to maintain the specified center frequency. Choosing a single large cell yields a thicker plate resulting in a large pressure amplitude at the cost of a smaller bandwidth. Contrary, having two smaller cells will require a thinner plate giving a wider bandwidth, but this lowers the amplitude of the output pressure. Having multiple cells per sub-element has two advantages. First, if a connecting wire is etched over the element is still functional. Second, if there is a short circuit between the top and bottom electrode, the cell containing this could be ablated by FIB-SEM and the rest of the sub-element could still receive and transmit. Unfortunately, for a single cell sub-element this would result in the entire element being electrically isolated or shorted.
However, returning to the plot in Fig. 2.4 and Table 2.2 the half-side lengths are calculated with the assumption that all other sub-element layout parameters, such as kerf, bonding width, and cell separation, are ignored. Hence, this serves as an initial guide to understanding the design possibilities. At this point, we resume with the original design Eq. 2.1 reprinted here for convenience

$$p = nd_{\text{cell}} + d_{\text{eff}} + (n-1)d_{\text{cellSeparation}} + 2d_{\text{bondWidth}}. \tag{2.9}$$

For the RC190+190 at 8 MHz the element pitch is predetermined to $p = 95$ µm. The RC190+190 array in this thesis is the third generation of the large-scale array in development in the group. In order to prevent short circuits between the top electrodes, the kerf width was increased from 2.5 µm to $d_{\text{eff}} = 6$ µm, based on the previous process experience. The cell design was chosen to be square cells of side length, $d_{\text{cell}} = 37$ µm with 4 cells per sub-element, $n = 2$ with a cell separation of $d_{\text{cellSeparation}} = 8$ µm. The bottom electrodes are connected through metal wires of a width of $w = 3$ µm. Calculating the plate thickness h from Eq. 2.5 yields a thickness of $h = 1.8$ µm using the effective radius theory. Knowing the plate thickness it is possible to determine the minimum bonding width from Eq. 2.2 resulting in 1.08 µm. Based on the minimum bonding width of 1.08 µm the bond width was set to $d_{\text{bondWidth}} = 3.5$ µm. The chosen cell separation also complies with the requirement of being at least twice the minimum bonding width. All the parameters are stated in Table 2.3.

For the RC512+512 the same calculations are performed with a 15 MHz center

Table 2.3: Geometry specifications of the two designed arrays. The side length of 33/37 µm is the length of the gold metal bottom electrode and the cavity, respectively. Likewise, the wire width of 3/7 µm is the width of the gold wire and the width of the glass cavity, respectively.

Array	**Side length,** d_{cell}	**Wire width,** w	**Cells per sub-element**	**Kerf,** d_{kerf}	**Bond width,** $d_{\text{bondWidth}}$	**Pull-in voltage,** V_{pi}	**Gap,** g
RC190+190	33/37 µm	3/7 µm	4	6 µm	3.5 µm	160 V	135 nm
RC512+512	33.24/37.34 µm	8/12 µm	1	5.66 µm	4 µm	160 V	135 nm

frequency resulting in a $\lambda/2$-pitch of $p = 51$ µm. As the cell design of the RC190+190 had proven robust the RC512+512 is designed to be nearly identical in order to utilize the already developed and successful fabrication process and to have a higher probability of realizing this largest-of-its-kind RC array. The specifications are seen in Table 2.3. Besides minor deviations, the only difference is that the pitch is now almost half of that of the RC190+190 so to preserve the side length of the cell a single cell sub-element was chosen. Furthermore, the wire width of the RC190+190 proved to be too thin during the etching of the bottom electrodes as a result of this the width was increased from 3 µm to $w = 8$ µm. To avoid disrupting the intended mode of operation by widening the wires, it was estimated from [66] that a wire width of 1/3 of the diameter would be sufficient for the CMUT to function properly. Thus, increasing the wire width in the glass cavity to 12 µm out of 37 µm was deemed appropriate to maintain the desired mode shape. Likewise, the plate thickness of the RC512+512 at $f = 15$ MHz was calculated using effective radius theory together with Eq. 2.5 giving a plate thickness of $h = 3.1$ µm. The minimum bonding width determined from Eq. 2.2 to 1.86 µm and the chosen bond width of $d_{\text{bondWidth}} = 4$ µm comply with this. These are the preliminary design parameters together with the electrical specifications they are simulated in a FEM model with the full design parameters of the CMUT to ensure that the center frequency is achieved, then the plate thickness or the cell size is altered and it is reiterated. The complete FEM model is described in detail in [60]. Subsequently, the array can be drawn in L-Edit layout designer (Tanner Tools), CAD software (L-Edit) and the sub-element of the RC190+190 and RC512+512 are seen in Fig. 2.5 and Fig. 2.6, respectively.

2.5.3 Gap and pull-in voltage

The vacuum gap, g is determined from the pull-in voltage, V_{pi} and the other geometrical parameters of the CMUT. The CMUT cells are typically either circular or square, in this project, a square cell geometry has proven to be robust and the calculations are performed for a square cell geometry. The applied bias on the CMUT during operation is 80-90 % of the pull-in voltage. The chosen pull-in voltage has to be compatible with the scanner i.e. the scanner supplies ± 95 V DC thus a total of 190 V, hence the operating voltage can be set to around 190 V. A pull-in voltage of $V_{\text{pi}} = 160$ V was defined as previously 220 V was used, but it was observed in the laboratory that dielectric charging occurred at higher voltages. The effective gap g_{eff}, that is the vacuum gap and the dielectric layers of the CMUT combined see Eq. 2.11, is found from [64] for square cells

$$V_{\text{pi,sq}} = \sqrt{\frac{2.95118 g_{\text{eff}}^2 h^3 \xi_s}{C_0 d_{\text{cell}}^2}} = \sqrt{\frac{2.95118 g_{\text{eff}}^3 h^3 \xi_s}{\epsilon_0 d_{\text{cell}}^4}} \quad \Rightarrow \quad g_{\text{eff}} = \sqrt[3]{\frac{V_{pi}^2 \epsilon_0 d_{\text{cell}}^4}{2.95118 h^3 \xi_s}}. \quad (2.10)$$

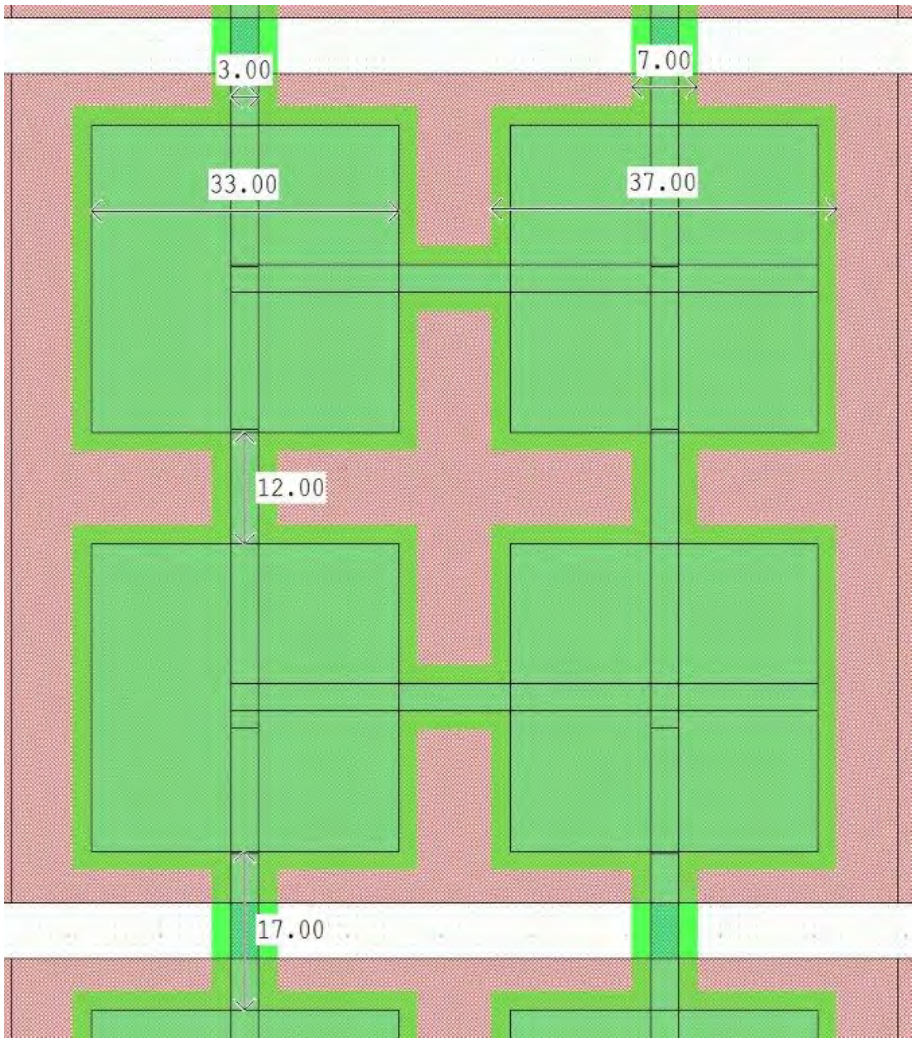


Figure 2.5: Overview of the sub-element of a RC190+190 array taken from L-Edit with a $\lambda/2$-pitch of 95 µm where all dimensions in the figure are in micrometer. The bottom electrode is shown in green and the top electrode is shown in red. The sub-element consists of 4 cells and connecting wires, all parameters are marked here and stated in Table 2.4. There is a 2 µm margin between the glass cavity and the metal.

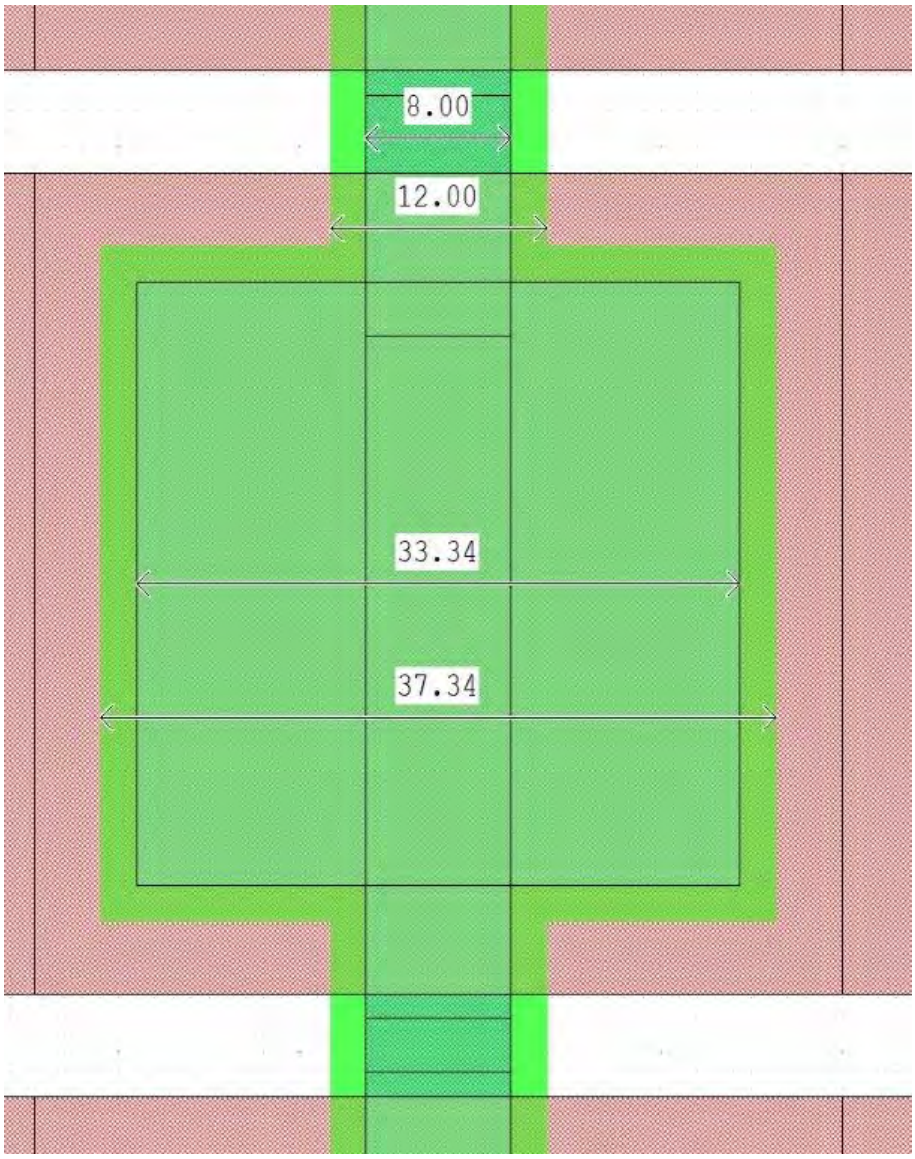


Figure 2.6: Overview of the sub-element of an RC512+512 array taken from L-Edit with a $\lambda/2$-pitch of 51 µm where all dimensions in the figure are in micrometer. The bottom electrode is shown in green and the top electrode is shown in red. The sub-element consists of 1 cell a connecting wire, all parameters are marked here and stated in Table 2.5. There is a 2 µm margin between the glass cavity and the metal.

The cell size, plate thickness and pull-in voltage are known from the design parameters. The vacuum permittivity is $\epsilon = 8.85$ pF/m and the constant $\xi_s = 385.637$ GPa [64]. The effective gap may be described additively by the thickness, t and permittivity, ϵ of the insulating layers

$$g_{\text{eff}} = g + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} + \frac{t_{\text{ni}}}{\epsilon_{\text{ni}}}, \tag{2.11}$$

for anodic bonding there is the vacuum gap g, the oxynitride layer consisting of oxide, t_{ox} and nitride, t_{ni}. These dielectrics are integrated to prevent short-circuiting, if the CMUT cell should go into pull-in, that is the event when the top plate collapses to the bottom of the cavity. Hence, the thickness of these dielectric layers is partly determined by the pull-in voltage, $V_{\text{pi}} = 160\,\text{V}$ combined with their breakdown voltage. The breakdown voltage has been measured in our own MEMS lab by postdoc Rune S. Grass to 0.9 V/nm for both the nitride and the oxide. The minimum thickness of the dielectric is

$$t_{\text{dielectric}} \geq \frac{V_{\text{pi}}}{0.9\frac{\text{V}}{\text{nm}}} = 177\,\text{nm}, \tag{2.12}$$

for a pull-in voltage of 160 V. In the fabrication of the oxynitride layer, an adhesive dry oxide layer of 20 nm was grown prior to the low pressure chemical vapor deposition (LPCVD) nitride of 190 nm followed by oxidation of this. Sufficient, for biases up to 189 V for a CMUT in collapse mode.

2.5.4 Capacitance

Having specified the geometry, the capacitance, C and the signal-preserving constant, ωRC are calculated in the following. The simplest form of capacitance is that of a parallel plate capacitor

$$C = \frac{\epsilon_0 L^2}{g_{\text{eff}}}. \tag{2.13}$$

The transducing ability from electrical to mechanical energy of the CMUT is facilitated by the deflection of the top plate. The deflection profile for an isotropic circular clamped plate is denoted

$$w(r) = w_0 \left[1 - \left(\frac{r}{a}\right)^2\right]^2 \tag{2.14}$$

varying with the radial position, r and the radius, a. The center deflection, w_0 for a circular and square plate is given by

$$w_{0,\text{circ}} = \frac{p_0 a^4}{64D} \qquad \text{and} \qquad w_{0,\text{sq}} = 0.020245\frac{p_0 L^4}{D} \tag{2.15}$$

where p_0 is the uniform pressure load and D is the flexural rigidity of the plate with the constants for circular and square plates differing only 4 % [64]. Incorporating this into the capacitance for a CMUT in operation gives

$$C = \frac{\epsilon_0 L^2}{g_{\text{eff}} - w(r)}. \tag{2.16}$$

Typically, the capacitance at zero bias C_0 is used for estimating the ωRC-product calculated for the individual element. Fundamentally, the ωRC-product needs to

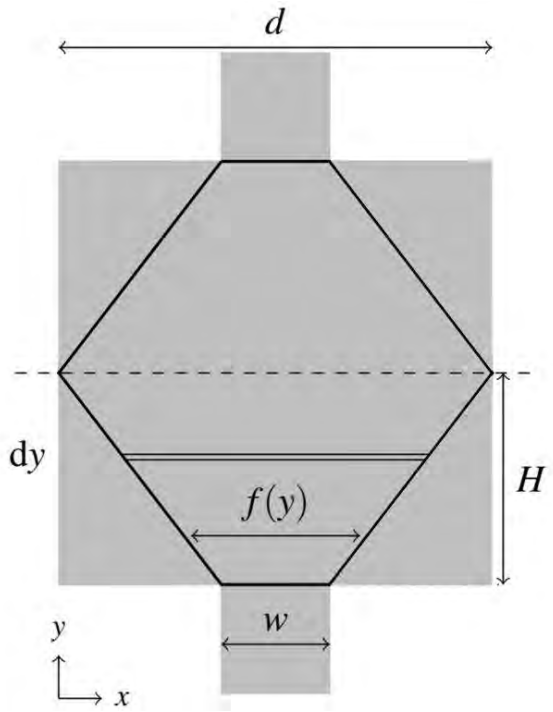


Figure 2.7: Sketch from [57]. The series resistance from a cell can be calculated using the finite element method (FEM) for any given geometry and is approximated by two trapezoidal resistance elements in series depicted here and derived in appendix C of the article [57].

be as low as possible to avoid signal attenuation along the element as described in the introduction Section 1.6. The angular frequency ω is given from the center frequency, f and the element capacitance, C can be calculated using Eq. 2.13 for the entire bottom electrode area of cells and wires A and the effective gap

$$C_{\text{element}} = \frac{\epsilon_0 A^2}{g_{\text{eff}}} = \left(\left(\frac{\epsilon_0 A^2}{g} \right)^{-1} + \left(\frac{\epsilon_0 \epsilon_{\text{OxyNi}} A^2}{t_{\text{OxyNi}}} \right)^{-1} \right)^{-1}. \tag{2.17}$$

That leaves the resistance, R which should be minimized for optimal imaging capabilities and is described in the following Section 2.6. This design requirement, ωRC, was presented by postdoc Andreas S. Havreland [57]. Conclusively, the thickness of the dielectrics together with the determined pull-in voltage is simulated using the aforementioned FEM model using multiple layers for the top plate consisting of the dielectrics, poly-Si and the aluminum top electrode. The simulation yields a gap of $g = 135\,\text{nm}$ to meet a $V_{\text{pi}} = 160\,\text{V}$ both are stated in the design Table 2.3.

2.6 Resistance in the bottom electrode, ωRC

In this section, the calculations of the resistance in the bottom electrodes and the ωRC-product for an RC element are presented for the RC190+190 and RC512+512, respectively. The contribution from the square cell to the resistance is modeled as a trapezoidal resistor element, as the current takes the shortest path while the electric field lines also spread out, described by the sketch in Fig. 2.7 and by the equation [57]

$$R_{\text{Cell}} = \frac{\rho}{h} \sqrt{\frac{d+w}{d-w}} \ln \frac{d}{w}. \tag{2.18}$$

Table 2.4: Design parameters for cell layout of an RC190+190 element with gold bottom electrodes.

Symbol	Design parameter		Unit
N	Number of elements	190	
f	Frequency in immersion	8	MHz
C	Element capacitance	52	pF
h	Bottom electrode thickness	234	nm
ρ	Electrode resistivity, gold	3.15	Ω cm
d	Cell side length	33	µm
w	Connector wire width	3	µm
L_1	Short connector wire length	12	µm
L_2	Long connector wire length	17	µm

The square cell has a side length of d and a connector wire of width w and length L and an electrode thickness of h and resistivity of ρ. The resistance from the connectors is described by a simple line resistance

$$R_{\text{Connector}} = \frac{\rho}{h}\frac{L}{w}, \tag{2.19}$$

while also taking into account the resistance contribution from the contact pad connector of length, L_C

$$R_{\text{ContactPad}} = \frac{\rho}{h}\frac{L_C}{w}. \tag{2.20}$$

The complete contribution has to be evaluated for the size of the array i.e. how many row or column elements, N there are in the array

$$\omega RC = \omega(NR_{\text{Sub-element}} + R_{\text{ContactPad}})C_{\text{element}}. \tag{2.21}$$

2.6.1 RC190+190 ωRC Design

Calculating the ωRC-product or the signal preservation of an RC190+190 bottom electrode element is done from the sub-element design. Where each sub-element as seen in Fig. 2.5, is a unit cell consisting of 4 cells, 4 vertical and 2 horizontal connecting wires, respectively. All the design parameters for the bottom electrodes are shown in Table 2.4. The bottom electrodes are made with a 234 nm thick gold layer, with a 10 nm titanium adhesion layer whose contribution is negligible.
Inspecting the sub-element it is evident that it is asymmetrical across the horizontal axis as the connectors have two different lengths of $L_1 = 12$ µm and $L_2 = 17$ µm. Dividing the sub-element into a left and right side, the two connectors are connected in series with two cells

$$R_{\text{Left}} = 2 \times R_{\text{Cell}} + R_{\text{Connector,L}_1} + R_{\text{Connector,L}_2} \tag{2.22}$$

The left and right side of the sub-element is identical and connected in parallel therefore the total resistance of the sub-element is

$$\frac{1}{R_{\text{Sub-element}}} = \frac{1}{R_{\text{Left}} + R_{\text{Right}}}. \tag{2.23}$$

The resistance of the entire element is made up of how many elements, $N = 190$ that are in total

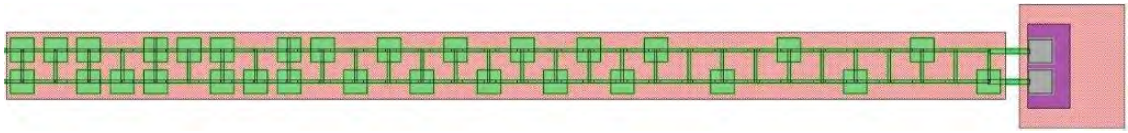


Figure 2.8: Image from L-Edit of the apodization region for the bottom electrodes (green) and the contact pad at the end. The top electrode is colored red and the purple square above the contact pads is the opening in the oxynitride insulation layer on the top plate. The apodization consists of a gradually decreasing number of cells starting from 3 cells/sub-element and ending with 1 cell. In total, there are 30 cells.

$$R_{\text{Element}} = N \times R_{\text{Sub-element}} = 190 \times R_{\text{Sub-element}} = 190.81\,\Omega. \tag{2.24}$$

For the RC190+190 there is also the apodization region, which has a more intricate pattern seen in Fig. 2.8 with the number of cells gradually decreasing. The apodization is likewise divided into an identical left and right side. The resistance contribution is calculated as the full length of the apodization, $L_{\text{Total,Apo}}$ subtracting the 15 cells to get the complete connector wire lengths and then adding the resistance from the 15 cells and the resistance of the contact pad connectors

$$R_{\text{Apo}} = \frac{\rho}{h}\frac{L_{\text{Total,Apo}} - 15d}{w} + 15R_{\text{Cell}} + R_{\text{ContactPad}} = 48.05\,\Omega. \tag{2.25}$$

There is quite a contribution to the ωRC-product from just the resistance, R, in the apodization region as the number of cells gradually decreases. The apodization makes up 25 % of the total resistance in the complete element. The measured capacitance of an element is $C = 52$ pF and the excitation frequency was designed for 8 MHz. Calculating the ωRC-product and the absolute magnitude of the transfer function, as described in Section 1.6, gives the preserved signal measured at the end of the element

$$\omega RC = 2\pi 8\,\text{MHz} \cdot 238.86\,\Omega \cdot 52\,\text{pF} = 0.62 \qquad |H| = 0.97 \tag{2.26}$$

For the current bottom electrode of the RC190+190 design 97 % of the signal should be preserved at the end of an element, this is viable and should produce a uniform pressure field for optimal imaging.

2.6.2 RC512+512 ωRC design

The cell layout is an element with a single line of cells and connectors as seen in Fig. 2.6. The CMUT array is designed with $N = 512$ row and column elements with a cell size of $d = 33.24$ µm and a connector width of $w = 8$ µm and a connector length of $L = 17.66$ µm. Besides the sub-element, only the resistance of the contact pad connector needs to be taken into account of $L_{\text{C}} = 68.83$ µm and all parameters are presented in Table 2.5. For the sub-element the resistance is

$$R_{\text{Sub-element}} = R_{\text{cell}} + R_{\text{Connector}} = 512 \times (R_{\text{Cell}} + R_{\text{Connector}}). \tag{2.27}$$

The total resistance of the element is then

$$R_{\text{Element}} = N \times R_{\text{Sub-element}} + R_{\text{ContactPad}} = 271.98\,\Omega. \tag{2.28}$$

Now the ωRC-product and the absolute magnitude of the transfer function can be calculated

Table 2.5: Design parameters for cell layout of an RC512+512 element with gold bottom electrodes.

Symbol	Design parameter		Unit
N	Number of elements	512	
f	Frequency in immersion	15	MHz
C	Element capacitance	34	pF
h	Bottom electrode thickness	240	nm
ρ	Electrode resistivity, gold	3.15	Ω cm
d	Cell side length	33.24	µm
w	Connector wire width	8	µm
L	Connector wire length	17.66	µm
L_{C}	Contact pad wire length	68.83	µm

Table 2.6: Overview of all the arrays included on the wafer map for the RC190+190 wafer.

Row-Column	Total	Purpose	Linear	Total	Purpose
RC190+190	4	Probe	Long test element, RC190 element	20	Lin element of RC190+190
RC16+16	38	Acoustic test	Short test element, RC16 element	100	Lin element of RC16+16
Top frame	14	Single element test	Deflection study, decreasing metal area	8	Impact on deflection
Bottom frame	14	Single element test	Small test element, corner of RC190	48	Pull-in and impedance

$$\omega RC = 2\pi 15\,\mathrm{MHz} \cdot 271.98\,\Omega \cdot 34\,\mathrm{pF} = 0.88 \qquad |H| = 0.94. \tag{2.29}$$

For the RC512 element, with a theoretically calculated capacitance of 34 pF using Eq. 2.17, at the end of the element 94 % of the signal is maintained and should generate a homogeneous pressure distribution to achieve optimal imaging.

2.7 Wafer Map

In this section, the wafer map which is a graphical representation of the locations of the different chips and test elements of first the RC190+190 wafer and then the RC512+512 wafer is presented. Microfabrication is a costly and time-consuming process, hence the wafer is densely packed with chips to optimize the potential yield. Prior to fabricating the RC190+190 probe chips, it is crucial to predetermine and plan all the necessary tests and studies and incorporate them into the wafer layout. This ensures that all required evaluations are performed after the realization of the chips.

Following the calculations from Section 2.4 specifying the geometrical parameters the arrays are designed and drawn in L-Edit. An overview of the wafer map and all the arrays included in the design can be seen in Fig. 2.9 and Table 2.6.

The RC190+190 arrays are to be implemented in a first-of-its-kind prototype probe handle developed by Kasper F. Pedersen [67] with interchangeable nose pieces, reducing the turnaround time from chip to probe immensely. RC16+16 are included specifically for measuring both electrical impedance and acoustics in a water tank in our own MEMS laboratory. The top and bottom frames, are RC16+16 arrays where either the top or bottom elements have been short-circuited to allow single-element probing within a row-column scheme.

For the linear elements, the long test elements are single elements of the RC190+190 to assess the electrical properties with true top-bottom measurements, which include impedance characterization. The small test elements in the corners of the

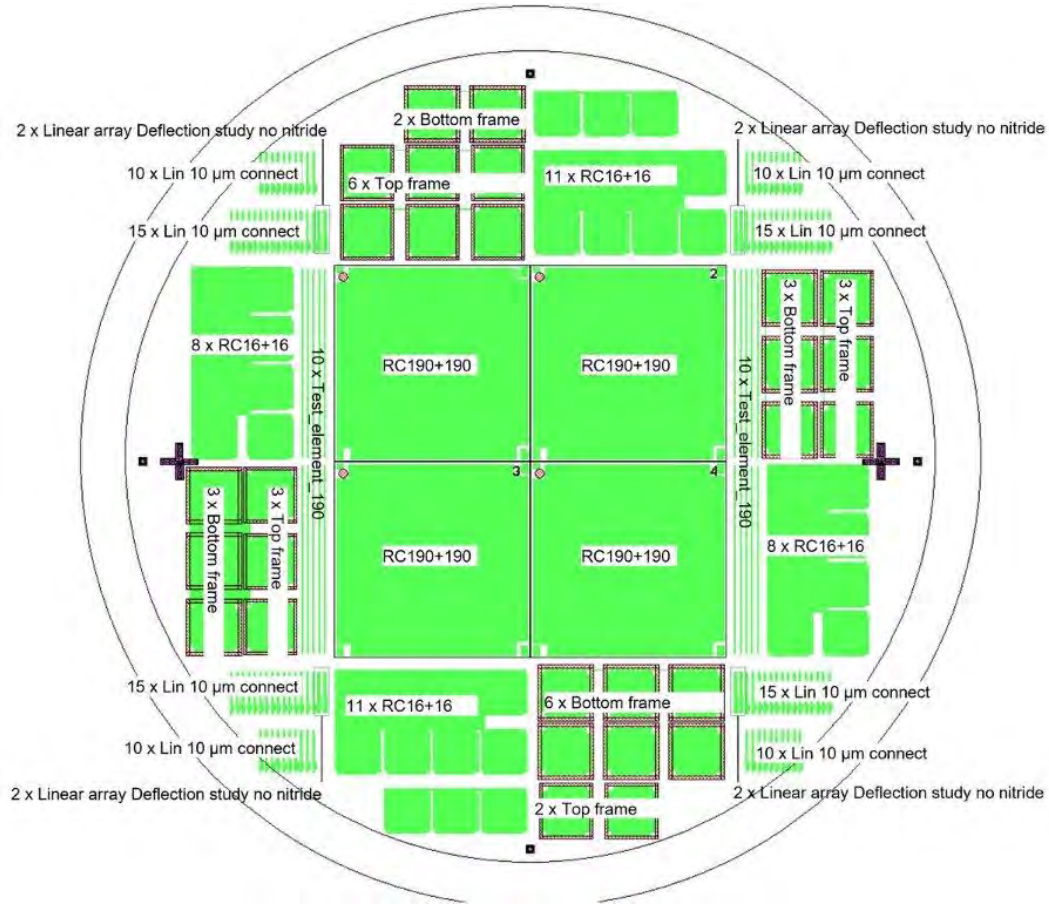


Figure 2.9: The wafer layout designed in L-Edit includes four large RC190+190 arrays placed in the center. Additionally, ten long test elements with the same number of cells as the 190+190 arrays are included beside all the main arrays. The north, south, east, and west sections of the wafer also contain several RC16+16 arrays for acoustical characterization, some of which have a metal frame connected as explained to either connect all the bottom electrodes (bottom frame) or all the top electrodes (top frame). Two rows of linear test elements of the same size as the RC16+16 arrays are included at the corners of the wafer. All the arrays on the wafer map and their purpose are presented in Table 2.6.

large RC190+190 chip are easily accessible and meant for determining impedance and destructive pull-in voltage tests without probing the RC190+190 chips. Linear elements with cavities with decreasing metal area were made to study the impact of the deflection of the top plate. The short test element also named the linear test element is a single element equivalent of that in an RC16+16. Linear elements have been studied for a long time in CMUT history and will bring a succinct insight into the viability of the design, process and operation described in Chapter 5.

For the wafer layout of the RC512+512 seen in Fig. 2.10 the difference from the RC190+190 wafer map is the two largest RC512+512 arrays made with 15 MHz $\lambda/2$-pitch. The 51 µm element pitch comes with new challenges in order to enable wire bonding. In order to wire bond the pitch between bonding pads should be approximately 200 µm. Already in the RC190+190 with a 95 µm pitch alternating contact pads are employed to obtain this requirement. For the RC512+512 with a 51 µm pitch in collaboration with Kasper F. Pedersen the design was made with a fan-out, seen in Fig. 2.11 to meet this criterion. In addition, the bonding pads should be no less than 100-120 µm wide for wire bonding and they were increased to

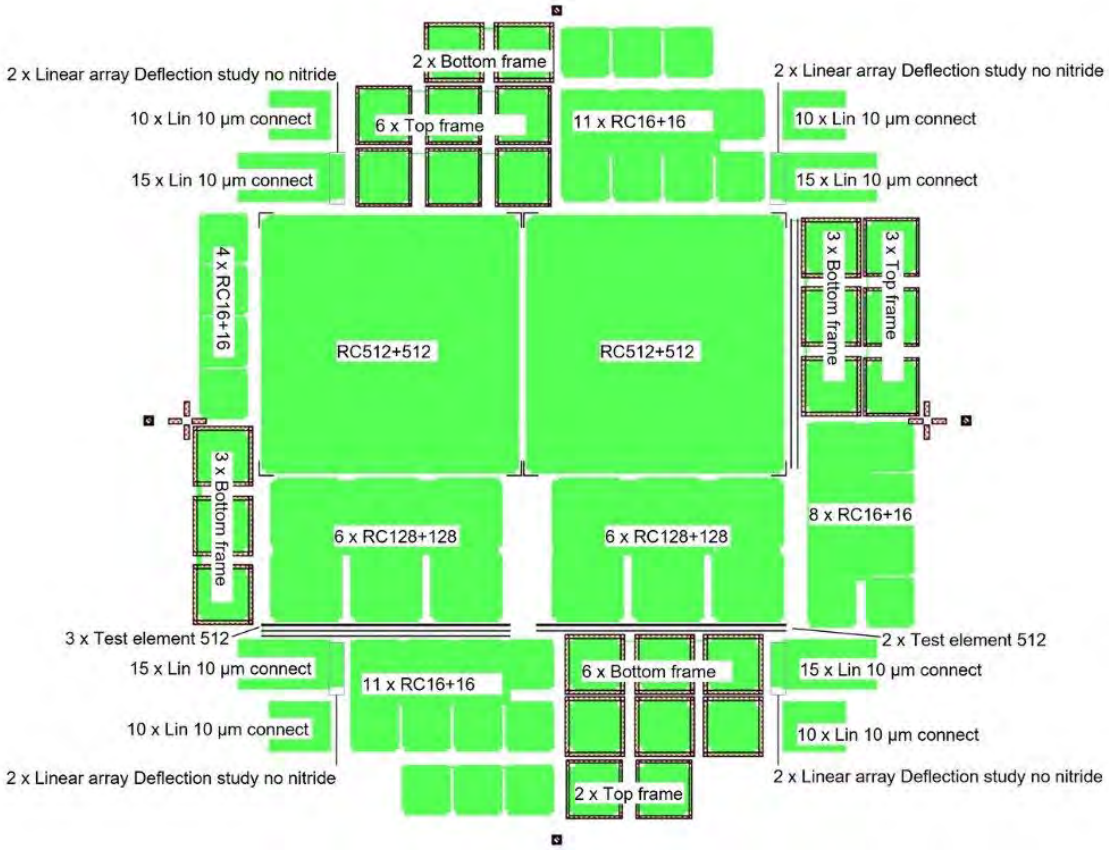


Figure 2.10: The wafer map of the RC512+512 wafer made in L-Edit is almost identical to that of the RC190+190 Fig. 2.9. The difference is of course that two large RC512+512 arrays are located at the center of this wafer layout. Additionally to up-scaling the largest RC arrays to 512+512, twelve RC128+128 arrays are included also made with a $\lambda/2$-pitch for 15 MHz transmission to be compared with a commercial Row-Column probe at our collaborators at CFU. Analogous to the previous wafer map, to test the individual RC512+512 elements single long elements made as linear elements are placed below the RC128+128 array.

200 µm × 100 µm. In addition to saw marks, alignment marks for wire bonding were created to enable automatic wire bonding programs, making the implementation from chip to probe smoother and streamlined. Notice that all elements have been numbered to facilitate faster characterization.

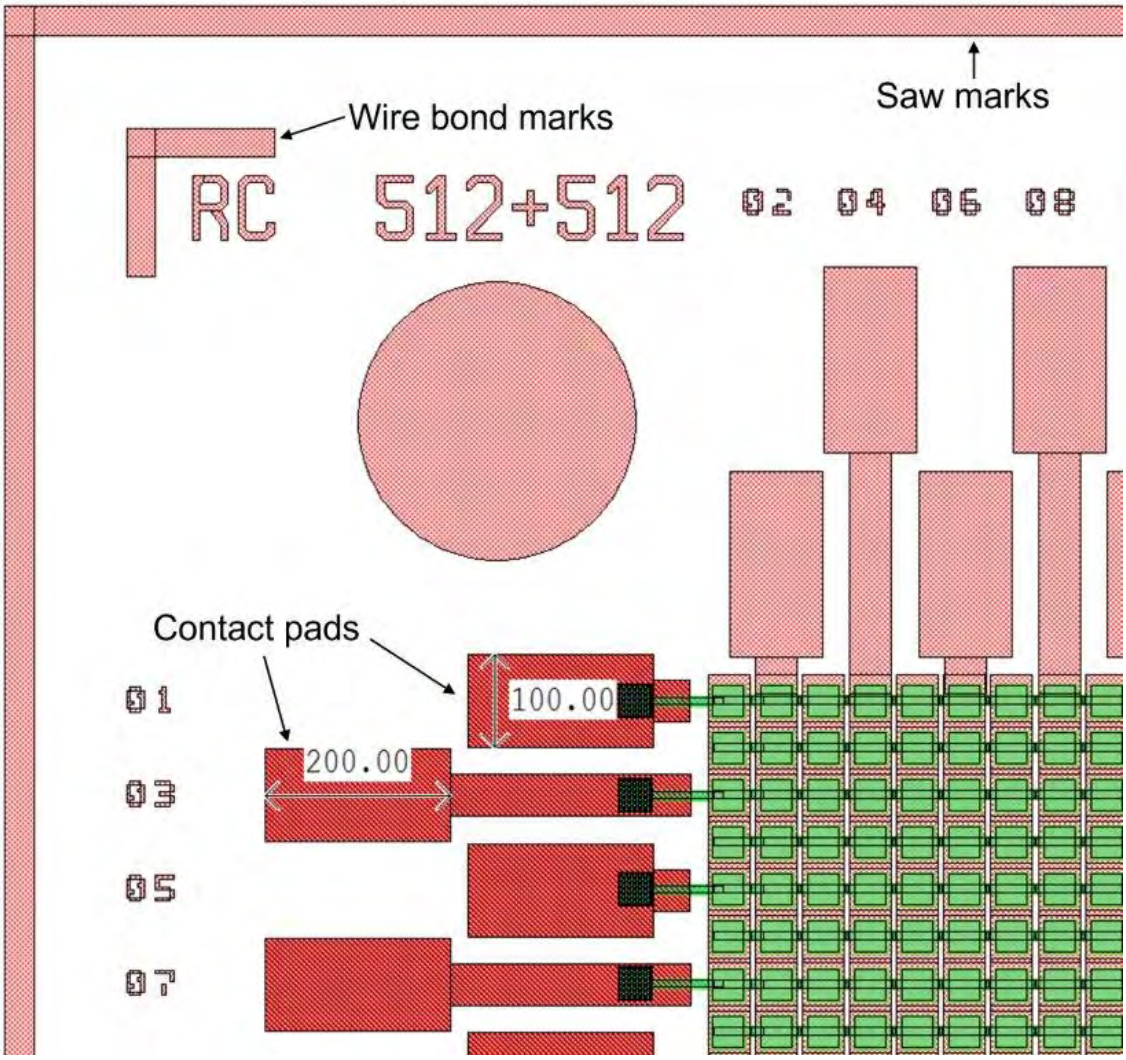


Figure 2.11: L-Edit image of the northeastern corner of the RC512+512 array to demonstrate the new implementations of alignment marks for wire bonding as well as the fan out of the contact pads combined with the alternating pattern giving a wire bonding pitch of 204 µm. This pitch of 204 µm enables wire bonding and enables the RC512+512 to be implemented into an ultrasound probe. The contact pads are also elongated to 200 µm × 100 µm to allow for electrical characterization probing and accommodate different wire bonding types such as wedge, ribbons and ball bonds. Furthermore, all elements are numbered to facilitate organized characterization during fabrication, electrical measurements and wire bonding.

2.8 Chapter summary

In this chapter, an analytical approach to CMUT design was presented and verified with FEM simulation. Initially, the element pitch of the array and the lateral dimensions of the element and cell were determined based on the center frequency in immersion. Once these parameters were determined, the plate thickness was derived using the relationship between the resonance frequency of the plate in vacuum and in immersion, as described by Lamb's theory. Additionally, expressions for pull-in voltages and center deflections were provided, allowing for the calculation of the vacuum gap and capacitance of the CMUT cell. The analytically obtained geometric parameters of the CMUT cell served as initial estimates, which were further adjusted using a finite element method (FEM) simulation model implemented in COMSOL. Conclusively, an analysis of the electrode resistance and its influence on signal uniformity was calculated utilizing the ωRC-design criterion. Wafer maps of the RC190+190 wafer and RC512+512 wafer were shown and the introduction of numbered elements, wire bonding alignment marks and fan-out combined alternating contact pad design were presented.

Chapter 3

Fabrication

3.1 Introduction

This chapter describes the fabrication process of the RC190+190 array wafer and the RC512+512 array wafer, respectively. The array designs were covered in the previous chapter. This chapter commences with an overview of the process flow and provides both visual and textual descriptions of the fabrication process. A detailed explanation of the process for the RC190+190 is given, followed by a description of the optimizations and modifications made to the process flow for the RC512+512. Both wafers are based on the anodic bonding technique, which will be elaborated below. The fabrication of the RC190+190 wafer involved numerous process iterations and individual studies conducted during this Ph.D. project, which will be discussed in the next chapter. The presented RC512+512 array is the largest of its kind. All microfabrication was carried out within the DTU Nanolab clean room.

3.2 Fabrication of RC190+190

Fabrication techniques for Capacitive Micromachined Ultrasonic Transducers (CMUTs) vary depending on the desired electrode material and the thermal constraints. Several different methods have been researched over the years among these are fusion bonding, adhesive polymer bonding, sacrificial release and anodic bonding. Anodic bonding was chosen in this project as substantiated in Section 1.6.2.
Anodic bonding utilizes a borosilicate substrate wherein CMUT cavities are etched into the glass substrate, followed by deposition and structuring of metal electrodes within the CMUT cell cavities. The glass substrate is preferable to reduce cross-talk between the elements compared to a silicon substrate. The bottom substrate with defined CMUT cells is anodically bonded to a silicon-based top wafer. The top wafer consists of an insulating layer as well as the poly-silicon layer used as the top plate in the final device.
The fabrication of these 2D RC CMUTs is carried out inside the DTU Nanolab clean room. The actual fabrication of a finalized wafer deviates from the well-thought-out process flow, described in Table 3.1 and shown in Fig. 3.1. The complete process flow for the DTU Nanolab Cleanroom can be found in Section A.1. The actual processing nearly always presents new challenges to be solved with the arsenal of readily available machines and engineering ingenuity.

Table 3.1: The general overview of fabricating a Row-Column array using anodic bonding. The process flow is also depicted in the same order in the diagram shown in Fig. 3.1.

Step	Process description	Optimization
1	A borofloat 33 (borosilicate) glass wafer is used for the substrate	
2	Cr deposition on a borosilicate wafer, patterned through lithography and used as an hard etch mask defining CMUT cavities	
3	Cr is removed, leaving a pure glass wafer with cavities	
4	Gold is evaporated and the bottom electrodes are defined by lithography and etched with IBE	X
5	The PSOI wafer is fabricated and openings in the oxynitride are etched in the mirror image of the bottom wafer	X
6	Anodic alignment bonding of the bottom glass wafer and the structured top PSOI wafer is performed	X
7	Thinning down the PSOI layers: Oxynitride, poly-Si, Oxide (BOX), Silicon handle, BOX layer to reach and define the top poly-Si plate	X
8	The 1st aluminum layer is deposited and lithography used to define openings over the contact pads of the bottom electrodes	
9	Opening up through the poly-Si top plate over the contact pads through dry etching and stripping the resist	
10	The 2nd aluminum layer plugs up the contact pads and is used for both top electrodes and contact pads, patterned with lithography and etched with IBE and dry etching	X

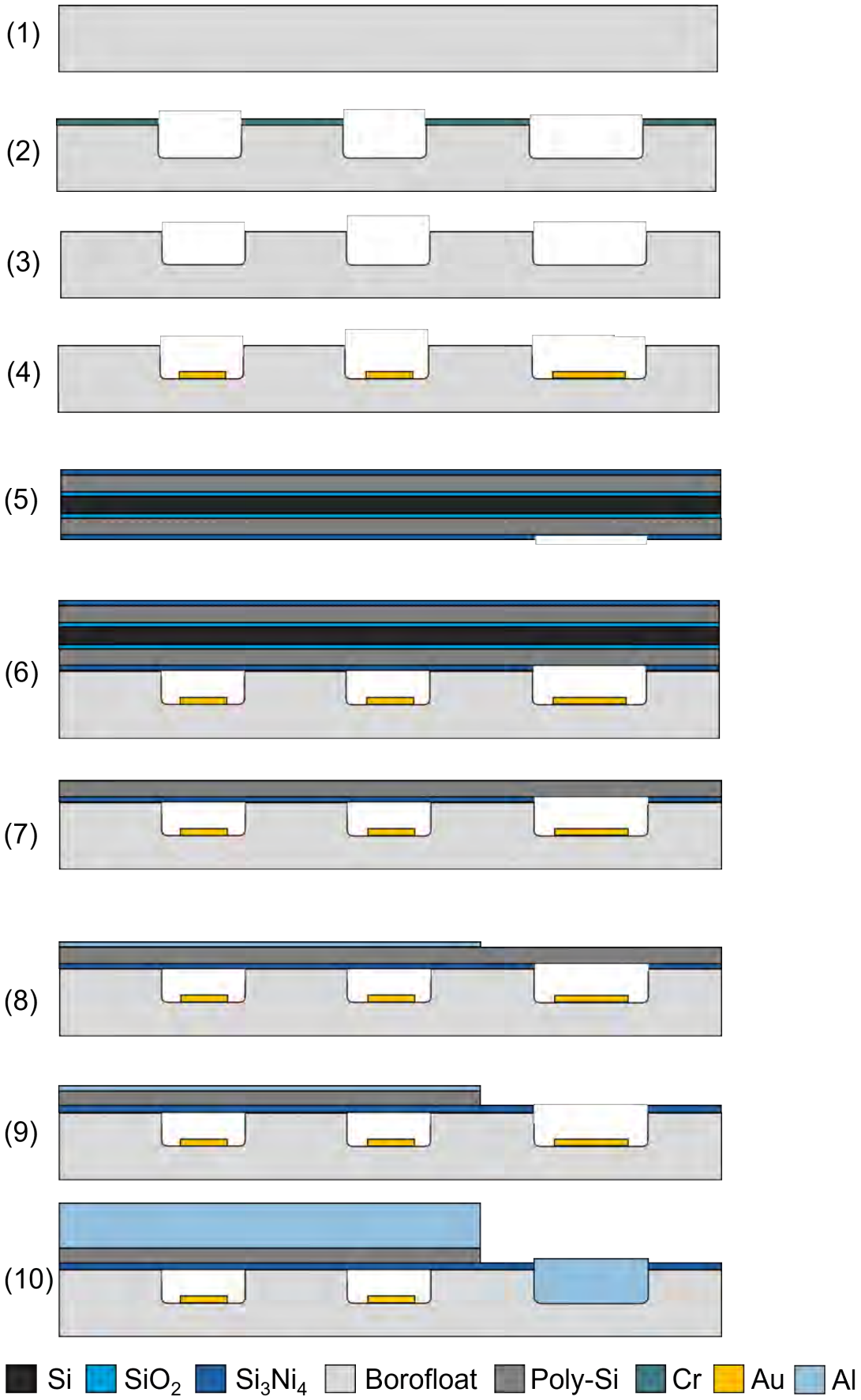


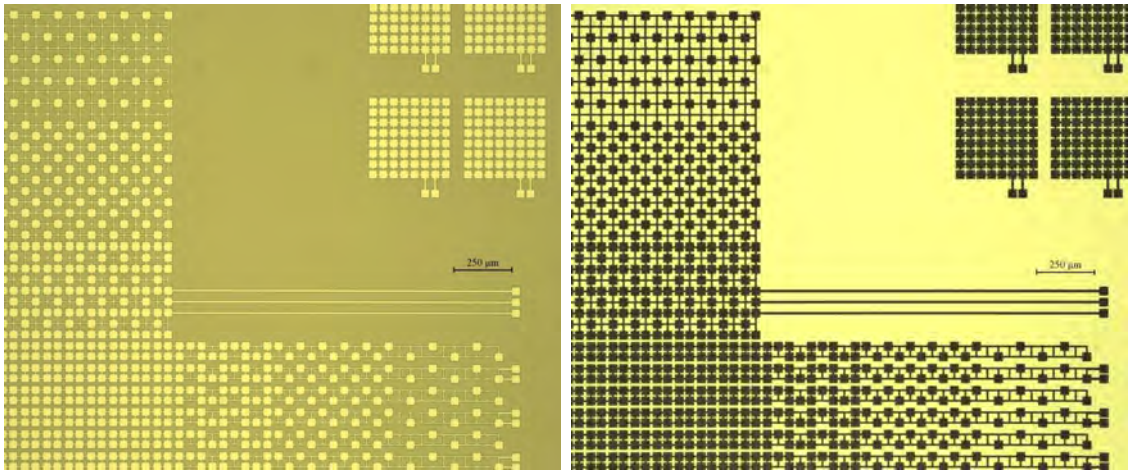
Figure 3.1: Process flow of anodic bonded RC CMUT.

3.2.1 Bottom substrate

In step 1) in Fig. 3.1, a borosilicate glass wafer is used for the bottom substrate as the wafer bonding technique used for the fabrication of these RC CMUT is anodic bonding. Structures in the bottom substrate are formed during steps 1) to 4). Anodic bonding relies on the principle of utilizing a glass wafer with movable alkali ions like Na^+ bonding it to a silicon wafer through the application of an electric field. The glass substrate used is a SCHOTT Borofloat ® 33 with a chemical composition of 81% SiO_2 silicon dioxide, 13% B_2O_3 boron trioxide, 4% Na_2O/K_2O sodium oxide or potassium oxide and 2% Al_2O_3 aluminum oxide [68]. The bonding is performed at an increased temperature of 350 °C where the resistivity of the glass becomes $10^{6.5}$ Ωcm, compared to 10^{15} Ωcm at room temperature [69]. Applying the bias at an elevated temperature allows the ions in the glass to drift toward the anode creating an electric field between the two wafers pulling them together and allowing the formation of covalent bonds. A comprehensive description of the anodic bonding mechanism is given in a lecture note in Section B.1.

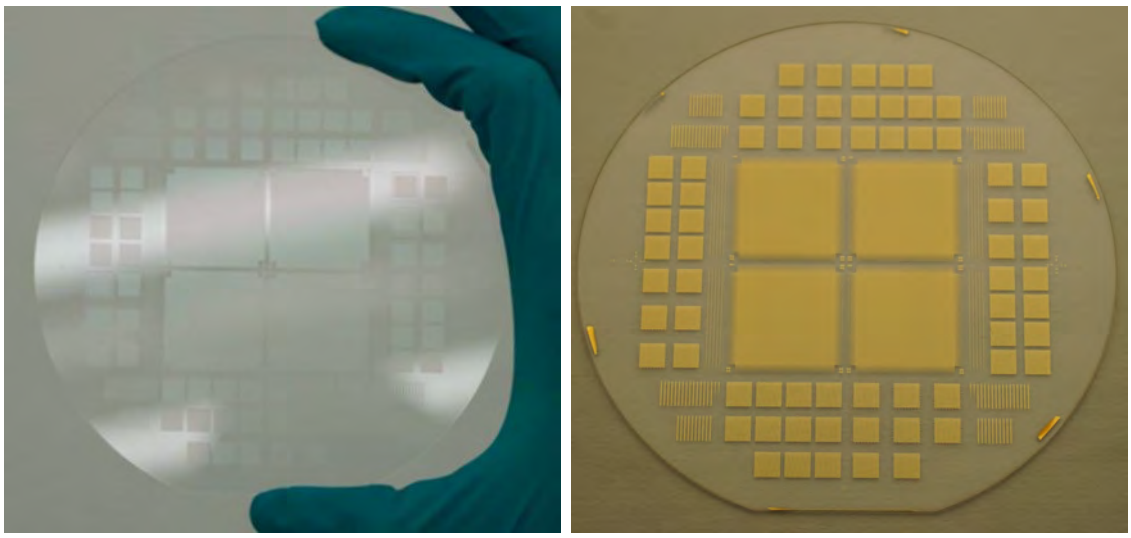
3.2.2 Cavities

Firstly, the glass wafer is deposited with a 50 nm chromium, Cr layer which is patterned with the first lithography mask, *Cavity* see Fig. 3.2 a) using a positive photoresist to open up over the cavities. The chromium is structured as a hard mask for etching out the CMUT cavities. The openings in the chromium are wet etched in the Chrome etch 18 [70] by the following reaction [71]: $3\,Ce(NH_4)_2\,(NO_3)_6 + Cr \rightarrow 3\,Cr(NO_3)_3 + 3\,Ce(NH_4)_2(NO_3)_5$, by transforming chromium into soluble chromium nitrate The progression of the etching process can easily be observed through the increasing clarity and transparency of the glass substrate, as the chromium layer is gradually removed. This allows for a clear visual indication of the completion of the etching process as the glass becomes completely transparent. The hard chromium mask is inspected in a microscope, see Fig. 3.2 b) to ensure that there is no under-etch broadening of the mask and where the chromium is etched the glass appears black in the microscope giving a good contrast for inspection. Then the glass cavities are etched in 12.5 % buffered ammonium fluoride, BHF in step 2) in Fig. 3.1 with an etch rate of 24 nm/min timed to obtain a specified vacuum gap and metal thickness to achieve a pull-in voltage of 160 V and an $\omega RC \leq 1.18$, respectively. Wet removal of the photoresist is done in MICROPOSIT™remover 1165 for 10 min with agitation. The hard chromium mask is stripped with Chrome etch 18, leaving a pure glass wafer with cavities as seen in step 3) in Fig. 3.1 and Fig. 3.3 a). The glass cavities are measured with a stylus profilometer ($KLA - TencorP17$) to determine the gap height, measured multiple times to get an average, then the metal layer thickness is adjusted accordingly with nanometer precision using the e-beam evaporator ($TemescalFC - 2000$) in step 4) in Fig. 3.1. The step height measurements are presented in Table 3.2 and are uniform across the wafer. With an average glass cavity height of 387 nm and a target vacuum gap of $g = 135$ nm to reach the desired pull-in voltage of 160 V a bottom electrode metal layer of 243 nm is required. Furthermore, the surface roughness of the bonding interface of the glass is scanned with an AFM ($BrukerDimensionIcon - Pt$) at North, East, South, West (NESW) and measured to an average roughness of $R_{\mathrm{a,\ PreIBE}} = 0.59$ nm. This is measured to evaluate the impact of the ion beam etching (IBE), used later in the process, on the surface roughness to assess the effect on the bonding strength i.e. if the surface is significantly roughened.



(a) (b)

Figure 3.2: Microscopy images of the northeastern corner of an RC190+190 array. a) shows the 1st lithography mask *Cavity* on the 50 nm chromium layer, defining the openings in the resist over the chromium. b) After the chromium mask etch, where the chromium has been etched by Chrome etch 18 over the cavities exposing the glass which appears black as the chromium mask reflects most of the light from the microscope. The hard chromium mask is now defined for etching out the cavities of the arrays.



(a) (b)

Figure 3.3: Picture of the bottom borosilicate wafer with a) glass cavities etched out into arrays corresponding to step 3) in the process flow in Fig. 3.1 and b) with gold bottom electrodes defined by Ion-Beam-Etching (IBE) inside the cavities finalizing the CMUT cells in the arrays corresponding to step 4) in Fig. 3.1.

Table 3.2: Stylus profilometer measurement, where the apodization contact in the north-eastern corner of the RC190+190 arrays consisting of three cells are scanned 3 times and then an average of the step height is calculated and stated in this table. For the glass cavities, the step height is very uniform. After the metal deposition, there is a bit larger discrepancy in the obtained vacuum gap with a 1.5 % and 6.7 % deviation from the target of $g = 135$ nm.

	Step height stylus profilometer measurement				
	RC1	**RC2**	**RC3**	**RC4**	**Avg. [nm]**
Cavity	376	379	378	377	377
	380	381	380	380	380
Vacuum gap	138,89	137,68	135,55	138,22	137
	142,50	145,86	143,68	144,54	144

3.2.3 Bottom electrodes

To obtain the cleanest possible result the wafer was piranha cleaned in a 4:1 ratio of H_2SO_4 and H_2O_2 for 10 min prior to metallization. Customarily a bake-out in a 250 °C oven can be done to remove absorbed water and decrease the pump-down time for the metallization tool to reach ultra-high vacuum 10^{-6} Torr, this was excluded due to particle concerns. The gold bottom electrode with a thickness of 234 nm is subsequently e-beam evaporated at 3 Å/s with an adhesion layer of 10 nm titanium underneath at 5 Å/s to reach the specified 243 nm to obtain a vacuum gap of 135 nm. The resistivity of the exact bottom electrode stack of 10 nm Ti + 234 nm Au on a glass substrate was measured using a four-point probe from Jandel at NESW to an average of $3.15 \times 10^{-6}\,\Omega$cm since the resistivity is crucial for the ωRC calculations, see Section 2.6. The bottom electrode metal is then patterned by the second lithography mask, *Bottom electrode* see Fig. 3.4. This exposure was optimized and described in Section 4.2.1, due to the reflective 3D structure it is non-trivial to obtain the specified pattern.
The gold is masked by an image reversal photoresist as seen in Fig. 3.5 a). Originally, this lithography step was done with a negative resist which is ideal as the challenges with the reflective 3D structure are circumvented. Unfortunately, the maskless aligner compatible with negative resist has had innumerable problems and proven an unreliable tool in the last two years and constant service from DTU Nanolab's process specialist and Heidelberg's own service engineers is required. An ordinary chrome shadow mask could be utilized, however, this technique has a less accurate alignment and it is challenging to align accurately with the 2 µm margin of the metal inside the glass cavities. Inaccurate alignment of the metal will cause a distortion of the electric field and in the worst case be misaligned enough to be on the sidewall of the cavity. Inverting the mask was also tested, regrettably with inadequate results. Therefore, the solution was to implement an image reversal process where the AZ5214E resist is used like a positive resist and exposed in the pattern of the bottom electrodes. Then a reversal bake is done for 2 min at 120 °C which makes the exposed areas insoluble by cross-linking them. This step is followed by a flood exposure that in turn makes the previously unexposed area soluble in the developer thereby reversing the polarity of the mask.
The definition of the bottom electrodes Ion Beam Etching (IBE) using the *Ionfab 300* is performed, see Fig. 3.3 b). IBE is an inherently physical etching technique where ions are used to bombard the material that should be removed. Combining this, with the fact that the bottom electrodes are located down in the trenches of the glass cavities creates quite a steep angle which causes back sputtering of the metal

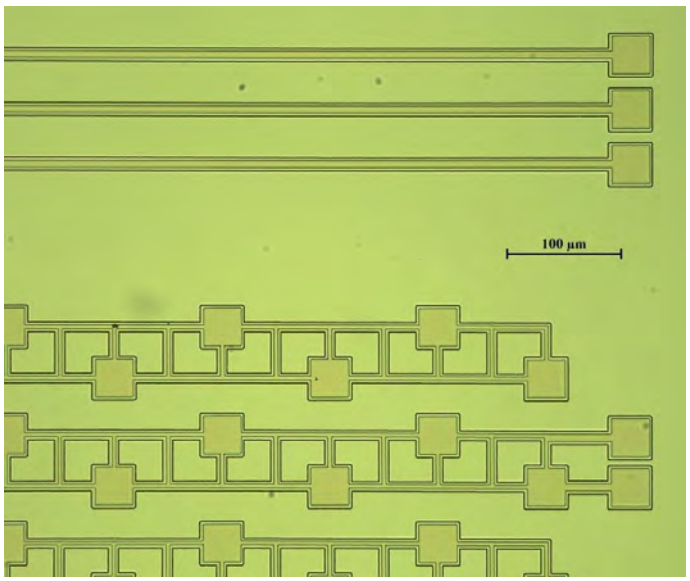


Figure 3.4: Microscope image of gold covering the entire wafer with the second lithography mask structured on top outlining the bottom electrodes. Here the northeast (NE) apodization contact is seen together with the first three bottom electrodes. Notice the alternating pattern of the contact pads such that odd-numbered elements are located on the west side and the even contact pads are located on the east side, hence the two contact pads of element no. 2 are seen here.

back upon the resist [72]. When stripping the resist, the back sputtered metal outlining the bottom electrodes is left as free-standing walls see Fig. 4.9 that due to their waviness are called ribbons. These ribbons can cause vertical short circuits between both the top and bottom electrodes as well as horizontal bottom-to-bottom electrode shorts after bonding. The solution that was tested and implemented for removing the ribbons was a short 2 s gold etch dip prior to stripping the resist in order to preserve the bottom electrodes and only etch the gold ribbons, see Fig. 3.5 c). The gold etch is a potassium iodine solution in the ratio of $KI:I_2:H_2O$ at 200 g:50 g:1000 ml, which was premixed and standard at DTU Nanolab. The chemical reaction is that gold and iodine are converted into gold iodide like $2\,Au + I_2 \longrightarrow 2\,AuI$, where the solubility of AuI is improved by the addition of KI [73]. This breakthrough of ribbon removal increased the yield and is detailed in Section 4.2.3.

However, Argon ion bombarding the photoresist during the IBE etch combined with reduced cooling due to the thermal insulation of the glass substrate results in a hardening of the top of the resist making it difficult to remove. A gentle 10 min plasma ashing at 500 W is used to remove this hardened topmost layer of the resist, see Fig. 3.5 d-e) where the slightly curved walls of resist are visible on top of the gold. Both a brightfield and a darkfield microscope image are taken at this point to inspect that the resist is still protecting the gold because the IBE also etches the resist it will not be the original 1.5 µm height as before and if the metal is exposed to the plasma it will be damaged. The remaining photoresist is removed by a wet resist strip in remover 1165 for 25 min, seen in Fig. 3.5 f). According to the measurements in a)-f), this process reduces the width of the bottom electrodes by 1 µm. Regrettably, a reduction of the connector wire width will increase the resistance of the bottom electrodes. On the contrary, it is a better option than having short circuits. The gap height over the bottom electrodes is measured with a stylus profilometer to determine the vacuum gap with a target of $g = 135$ nm. The

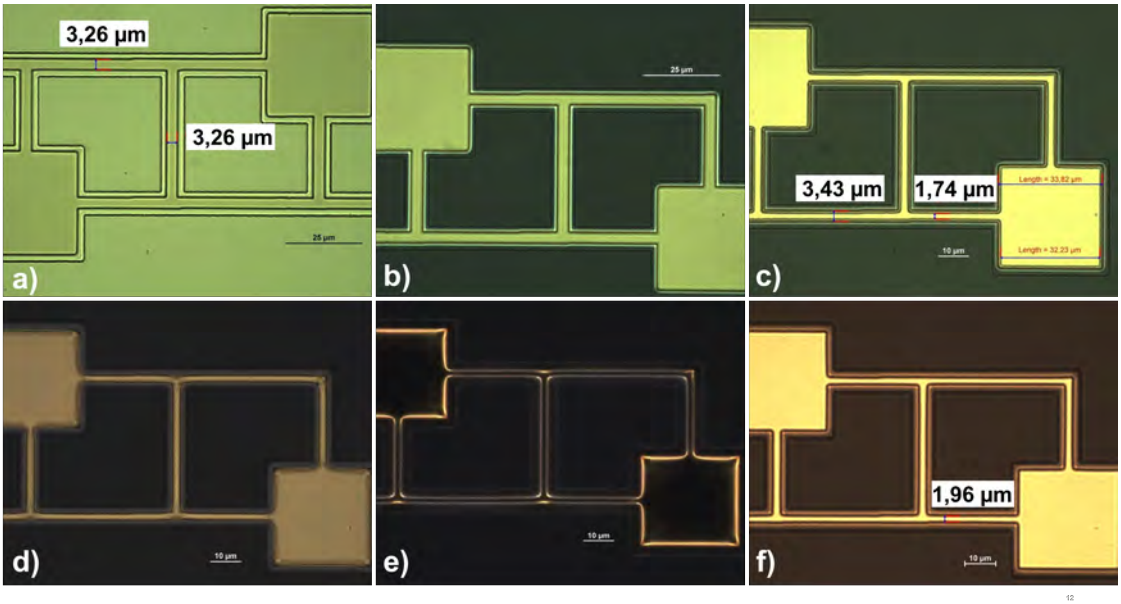


Figure 3.5: A sequential microscope image series depicting the definition of the bottom electrodes. Starting with a) the second lithography mask, *Bottom electrode* on top of gold protecting the areas that are to be the bottom electrode inside the glass cavities. An IBE etch is performed b) where a halo around the bottom electrode is observed due to the angle. This halo is a known phenomenon of the IBE. c) A short 3 s gold etch dip is performed before removing the resist to etch the metal that is back sputtered upon the resist walls as a solution to the short circuit problems in the previous chip. As a consequence of the physical IBE etch the resist is hardened and a combination of plasma ashing d-e) and wet removal f) of the resist is necessary. d) Brightfield image of the gentle plasma ashing of the topmost layer of the resist together with a dark field image e) to ensure that the resist is still protecting the metal as the plasma can damage and even strip the resist. Finally, all of the resist is removed and a reduction of the metal width of 1 µm is measured, unfortunately, but this option is still preferred as it mitigates the risk of short circuits with the ribbons.

average gap heights are stated in Table 3.2 and deviates with 1.5 % and 6.7 %, this is acceptable. After having defined the bottom electrodes the surface roughness of the glass bonding interface was measured to $R_{\mathrm{a,PostIBE}} = 0.8$ nm. Then a 30 s piranha clean mixed in the ratio of 4:1 of H_2SO_4 and H_2O_2 stirred well before submerging the wafers is used to remove organic particles and metal traces. Particles causing voids in the bonding interface are detrimental to the wafer for achieving a high yield as they compromise subsequent processing steps. The short piranha cleaning is based on prior experience gained in the fabrication run of the TH1-B (20210527) array. In that run, the concern of under-etching the gold electrode by etching the titanium adhesion layer led to the proposed time of the piranha cleaning step to be tens of seconds to a maximum of 1 minute [60]. This cleaning step was tested and optimized and explained in Section 4.2.4.

3.2.4 Top wafer

The top wafer is a self-manufactured SOI wafer named a PSOI wafer [65]. The PSOI wafer is based on a silicon (100) substrate of 350 µm and is fabricated with a 500 nm Buried Oxide layer (BOX) layer by wet oxidation and a thickness-tailored boron doped LPCVD poly-silicon layer of 2.3 µm with a resistivity of $< 0.062\,\Omega$cm seen in step 5) in Fig. 3.1. Chemical mechanical polishing (CMP) is employed to achieve a sub-nm surface roughness of the poly-Si, measured by AFM, as it is crucial to enable anodic bonding as a higher surface roughness could prevent the bonding. Anodic bonding requires a minimum surface roughness of ≤ 50 nm [59] compared to fusion bonding which necessitates ≤ 1 nm [74], thus anodic bonding is less sensitive to particles trapped at the bonding interface. However, lower surface roughness yields higher bond strength and reduces the number of possible voids. To remove the polishing slurry an iterative cleaning process of piranha, BHF, and piranha is conducted and verified with a particle scan, see Section 4.2.5. To avoid short-circuiting the CMUT if it should go into pull-in a dielectric layer is deposited onto the polished top plate and the thickness can be calculated according to Eq. 2.12. A nitride is chosen as the dielectric insulation layer to prevent growing the poly-Si grains through an oxidation process as discovered during the quart fusion process described in Section 8.3. For optimal bonding conditions [75] an oxidized LPCVD nitride, henceforth called oxynitride, of 180 nm is deposited. First, a dry oxide buffer layer of 20 nm is grown for increased adhesion. Secondly, the LPCVD nitride of 190 nm is deposited and immediately wet oxidized for 3 hours creating the oxynitride of 180 nm, see Fig. 3.6 for a cross-sectional SEM image displaying all the layers of the PSOI wafer.

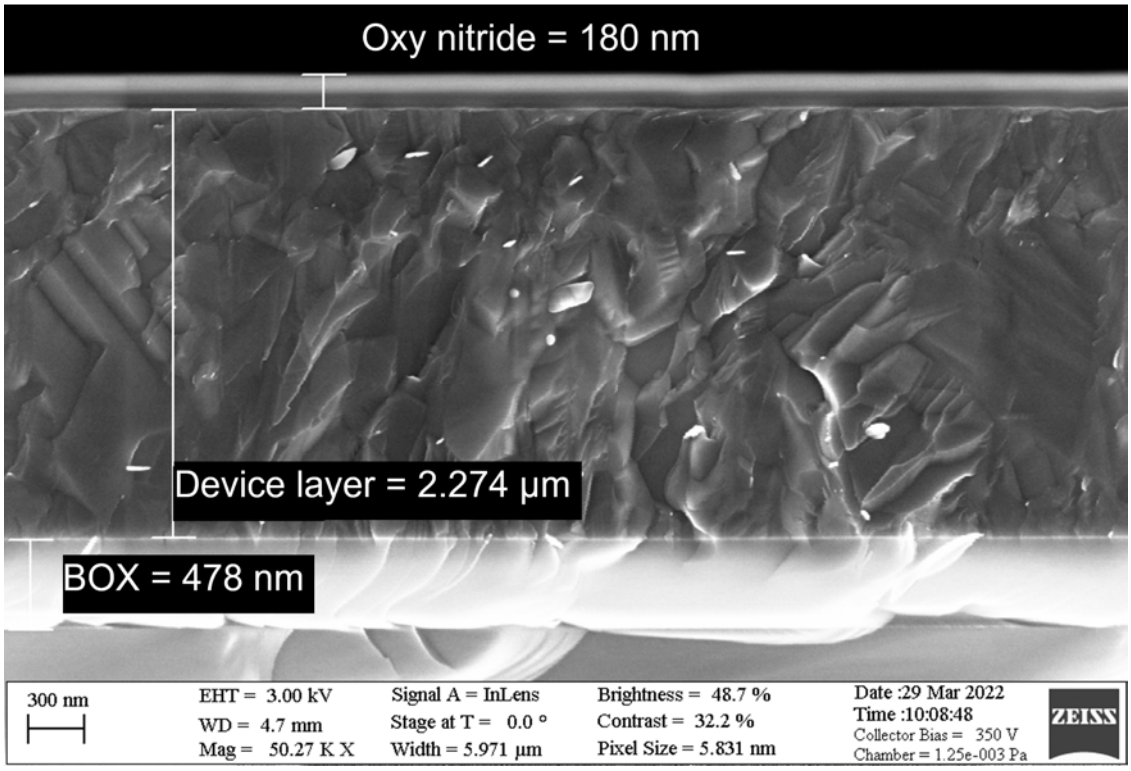
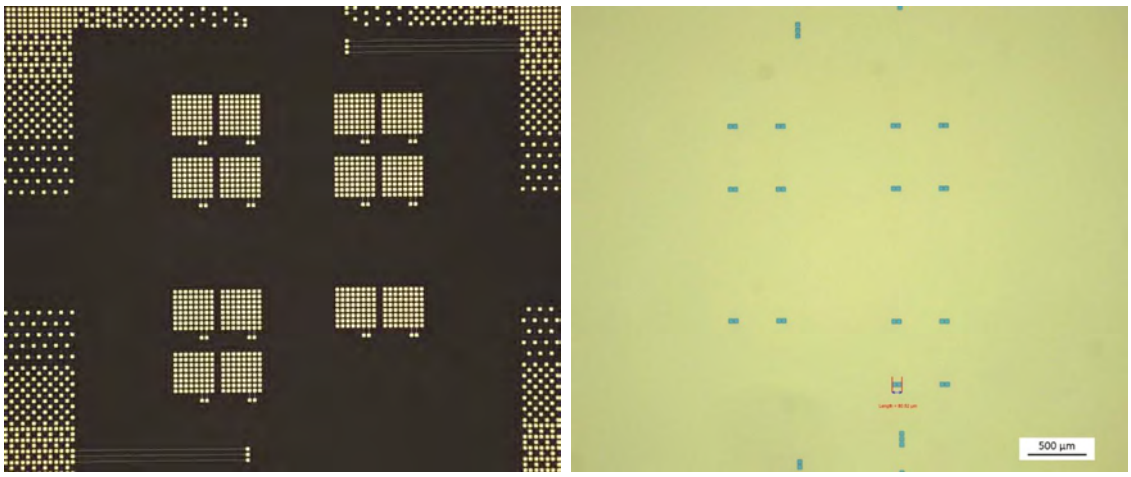


Figure 3.6: Cross-sectional SEM image of a PSOI wafer for characterization, showing the different layers. From the bottom up the layers are: the silicon handle wafer, the BOX layer, the poly-Si device layer which has been polished by CMP to constitute the first part of the top plate, followed by the oxynitride layer which is the other part of the top plate. The oxynitride is formed through oxidation of first 20 nm adhesion dry oxide, then an LPCVD nitride of 200 nm immediately followed by a wet oxidation for 3 hours creating the oxynitride of 180 nm.



(a) **(b)**

Figure 3.7: Microscope images taken at the center of (a) the bottom wafer with the gold bottom electrodes structured inside the glass cavities and (b) the center of the PSOI wafer showing the openings in the oxynitride over the contact pads. Notice that the openings in the oxynitride are made in the mirror images of the contact pads of the bottom electrodes as the two wafers are to be alignment bonded.

The oxidation of nitride is done with a wet thermal oxidation at 1100 °C for 3 hours that should result in a thickness of the oxide of 60 nm [76], and observing Fig. 3.6 this is the case of the two-layered 180 nm oxynitride. Prior to alignment bonding, the PSOI is structured with a mirrored mask compared to the bottom electrode see Fig. 3.7 a), opening up over the contact pads, see Fig. 3.7 b). This is the third lithography mask, *Opening to bottom - SiN*. Openings are etched in the oxynitride over the contact pads by dry etching using an advanced oxide etcher (AOE), then the resist is removed by plasma ashing and the PSOI wafer is ready for alignment bonding. The reason for pre-opening the nitride membrane over the contact pads and performing alignment bonding, which is a more difficult process than regular anodic bonding, was due to dry etching issues with oxynitride that hindered the proper opening of the contact pads after bonding. Also, one of the critical obstacles encountered involved the oxynitride membrane, which had a tendency to burst during the thinning process of the top plate. This bursting phenomenon imposed limitations on the contact pad area and posed challenges in removing the resulting pieces without causing damage to the contact pads, this issue was solved with alignment bonding. An AFM scan of the surface roughness gave an average roughness of $R_{\mathrm{a,PSOI}} = 0.6$ nm, which is acceptable and combined with the surface roughness of the bottom glass wafer of $R_{\mathrm{a,PostIBE}} = 0.8$ nm this factor indicates conditions for a successful anodic bond. The top PSOI wafer is cleaned prior to bonding by means of an RCA1 cleaning step consisting of NH_4OH, H_2O_2 and H_2O (DI water) mixed in a ratio of 1:1:5 parts and heated to 70 °C. A previous particle study performed in the group showed that only using RCA1 gave the smallest number of particles compared to using the full RCA process. Also, the HF dip following the RCA clean used to remove the generated oxide layer is omitted to preserve the oxynitride.

3.2.5 Anodic alignment bonding of the top and bottom wafer

The two wafers are aligned with the alignment bonder *(Süss MicroTec MA6/BA6)* through a fixture that allows them to be separated by a gap of 100-150 µm. This is a rather large distance compared to regular chrome glass mask alignment distance as low as a couple of microns, 100-150 µm is chosen as a precaution due to the wafer bow present in both wafers and is necessary not to scratch the bonding surfaces. Alignment is done with backside cameras looking through the 500 µm thick glass substrate. Once alignment is satisfactory, the wafers are put into contact and a pattern of newton rings can be observed through the glass wafer and the fixture is transferred from the aligner to the wafer bonder *(Süss Microtec Substrate Bonder SB6 Gen2)*. Then, in step 6) in Fig. 3.1 the wafer stack is anodically bonded at 350 °C with a tool force of 1000 mbar in three voltage ramps of 150 V, 300 V, and 600 V applied until the current is 10 % of the initial value. A total of 1145 mAs accumulated charge was obtained, which is one of the indicators for a successful bond that we rely on. In anodic bonding, there are several parameters such as applied voltage, the set current limit, pressure and temperature which can be adjusted. A substantial part of this work has been focused on optimizing this crucial point and the findings for anodic bonding are partly explained in the lecture note, see Section B.1, co-authored by the Ph.D. student.

Bonding success can be readily inspected through the transparent glass substrate, see Fig. 3.8. Only smaller voids along the periphery of the wafer show a successful hermetic seal. The alignment is also quite precise seen on Fig. 3.9 as the exact alignment of the green openings in the oxynitride over the contact pads of the gold

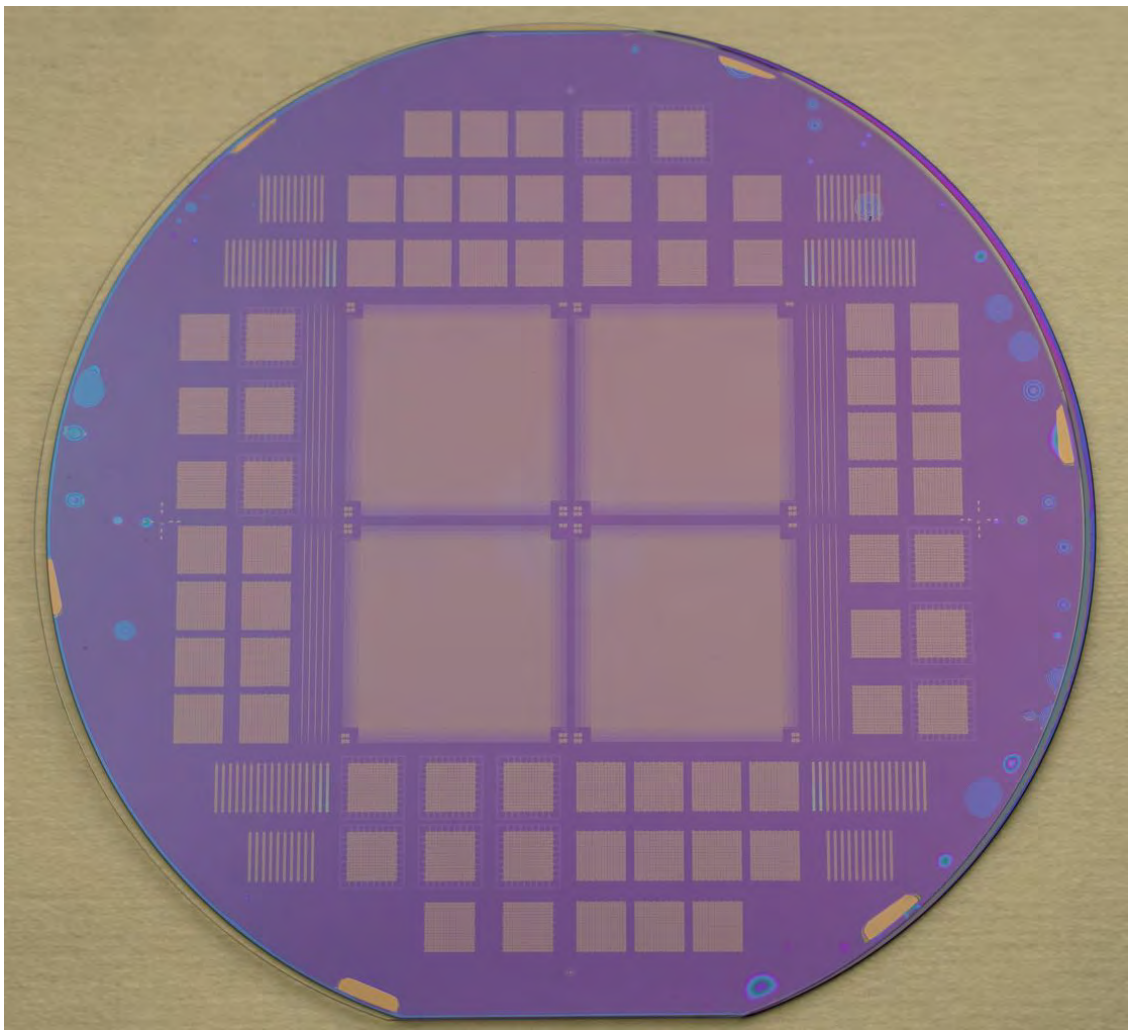
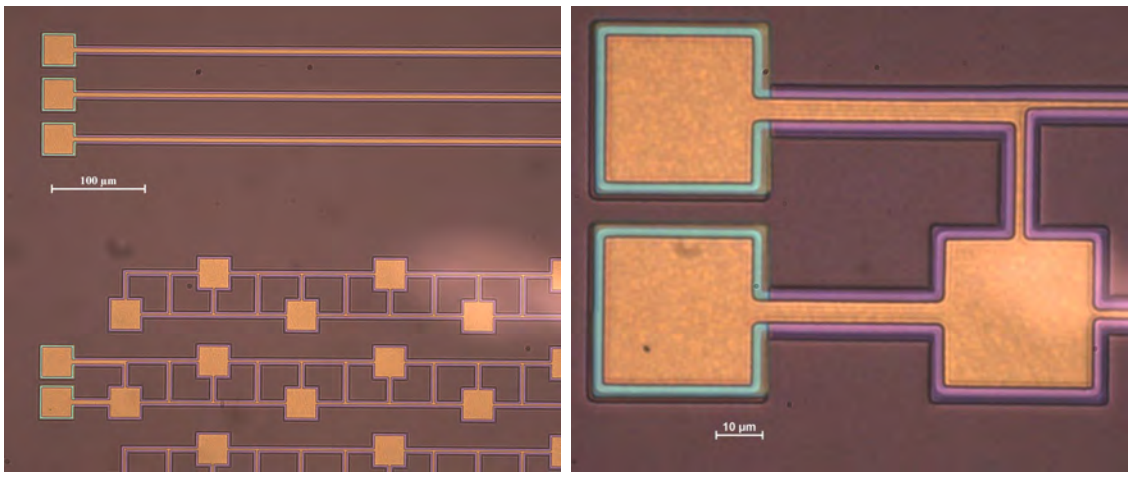


Figure 3.8: Picture after anodic bonding of a successful alignment bonded wafer. The bond is readily inspected through the transparent glass substrate as seen here looking through the backside up on the bottom electrodes and through the glass onto the oxynitride interface.



(a) **(b)**

Figure 3.9: Microscope image after alignment bonding showing a successful alignment of the green openings in the oxynitride directly over the contact pads to the bottom electrodes with a zoom-in b). This corresponds to step 6) in the process flow in Fig. 3.1 and the interfacing of the two microscope images seen in Fig. 3.7. Notice, the apodization and contact pad are flipped in this image compared to Fig. 3.4.

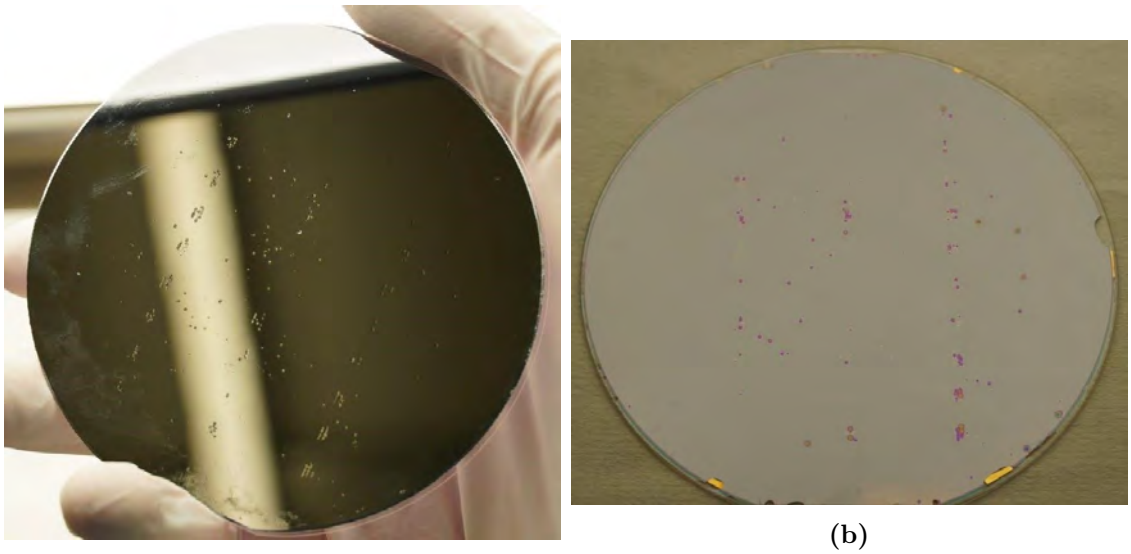
Table 3.3: Dry etching recipes used in the process flow performed on the ASE (Advanced Silicon Etcher, STS MESC Multiplex ICP).

Recipe	KITOXYSI	MAENGSIN	KITISO	SHALLOLR	Unit
Etched	Oxynitride	Nitride	Silicon	Silicon	
Platen Power	200	150	0	16	[W]
Coil Power	1300	25	2800	2800/1000 (Passivate)	[W]
Platen Temperature	20	20	20	0-10	[°C]
C_4F_8 flow	13	20			[sccm]
H_2 flow		0			[sccm]
He flow		100			[sccm]
SF_6			230	260	[sccm]
O_2			23	26	[sccm]
Pressure	4	2.5	6		[mTorr]

bottom electrodes in a microscope image taken through the glass from the backside. Essentially, the interfacing of the two images seen in Fig. 3.7.

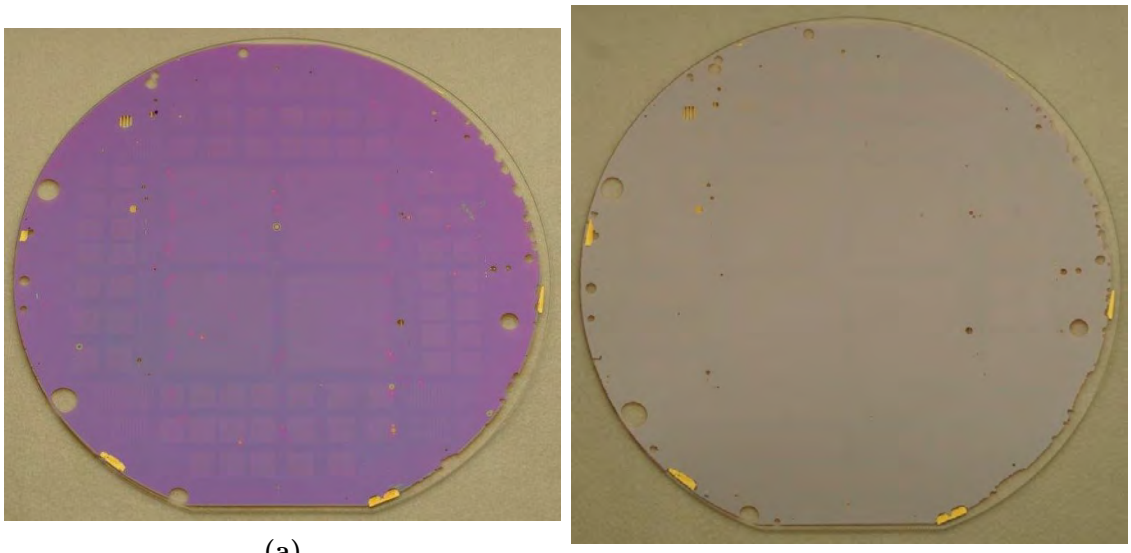
3.2.6 Thinning down to the top plate

Thinning the handle layers of the PSOI wafer down to just the plate of the CMUT, see step 7) in Fig. 3.1, is done with consecutive etching of dry etching of the oxynitride, KOH etching of the non-usable device layer, BHF etching of the first BOX layer followed by a 3-hour long KOH etch of the entire 350 µm thick silicon wafer (handle layer) before reaching the second BOX layer etched by BHF. A new recipe for dry etching the oxynitride was developed called KITOXYSI, see Table 3.3, with an almost tenfold increase in etch rate compared to the previous MAENGSIN etching recipe.
The poly-Si layers and the silicon wafer can be removed by either dry etching using the SHALLOLR recipe in Table 3.3 or wet etching with KOH. Both methods have been employed in this research group. However, wet etching with KOH is preferred for batch processing, higher uniformity and the dissolution of rupturing plate pieces due to voids. During the etching process, any voids that were created from the bonding process or poorly bonded regions of the top plate are likely to rupture and detach from the surface. In dry etching the silicon flakes rupturing from the plate can adhere to the surface while submerged in a wet etchant the dislodged flakes will be dissolved instead. Silicon flakes adhering to the plate are a problem for later processing as well as it being a possible short circuit if they are not removed. Based on this, the wet anisotropic 28 %wt KOH etch is chosen. The chemical etching occurs as follows: $Si + 2\,OH^- + 2\,H_2O \longrightarrow Si(OH_4) + H_2(g)$ and is performed at 90 °C for a faster etch rate determined by the author to 1.7 µm/min. At this etch rate the silicon handle layer of 350 µm should be etched in 1 h and 26 min.The standard recipe at Nanolab is heated to 80 °C with an etch rate of 1.3 µm/min. At this temperature, for a duration of 3 hours, water addition is necessary as the water evaporates and increases the concentration and etch rate. As silicon is etched hydrogen bubbles are released, reducing the visibility of the etching process so the wafers have to be routinely checked and lifted from the bath for inspection.



(a) (b)

Figure 3.10: Pictures taken during the long KOH etch of the silicon handle layer after a) 1 hour and b) 3 hours. Since the last batch was completely ruined during the KOH etch and the plate either completely or partially torn off see Section 4.3.2, this batch was continuously monitored which led to the discovery of these isotropic holes that emerged after 1 hour a) and initially believed to be impurities in this specific wafer batch and the KOH etch was continued and stopped after 3 hours as these fast etching holes reached the final BOX layer prematurely, see b). A more detailed description along with a study of this peculiarity is found in Section 4.3.2.



(a) (b)

Figure 3.11: Picture of a) the purple final BOX layer being reached through etching the last micrometers of the handle layer with the highly selective dry etch recipe KITISO devised for this specific purpose without breaching through the oxide is the isotropic hole pattern. Picture of b) the 2.3 µm poly-Si device layer reached by etching the BOX layer in a) with BHF, the goal of preserving most of the plate in spite of the fast etching isotropic hole pattern from Fig. 3.10 was successful.

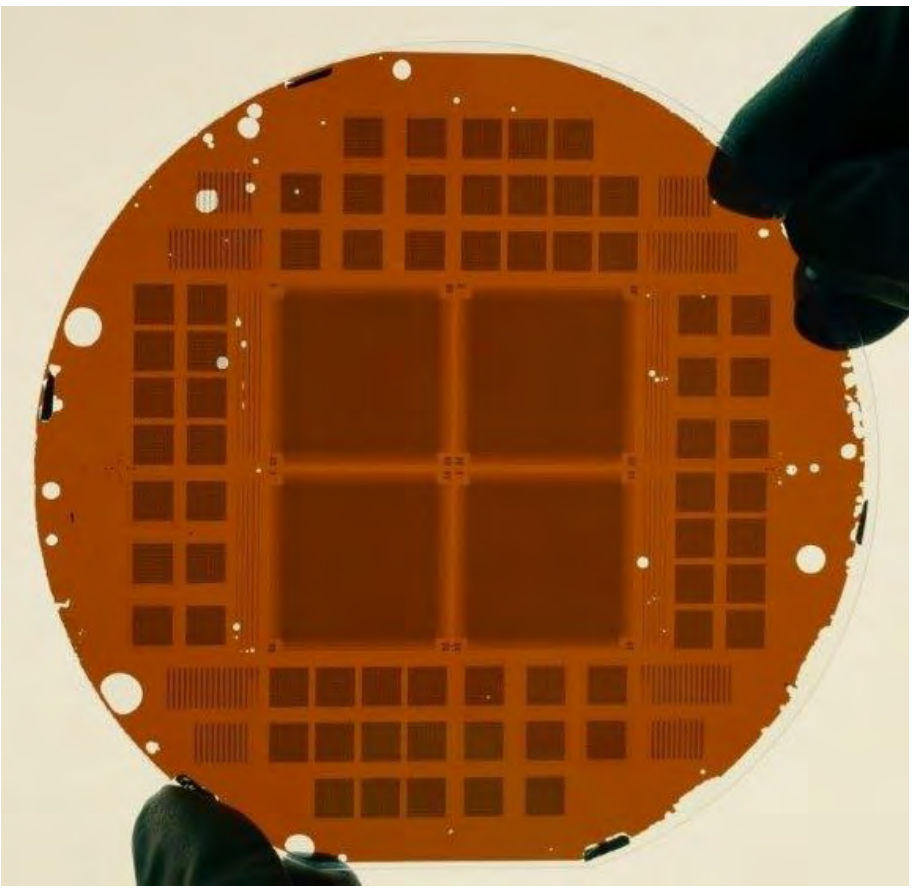


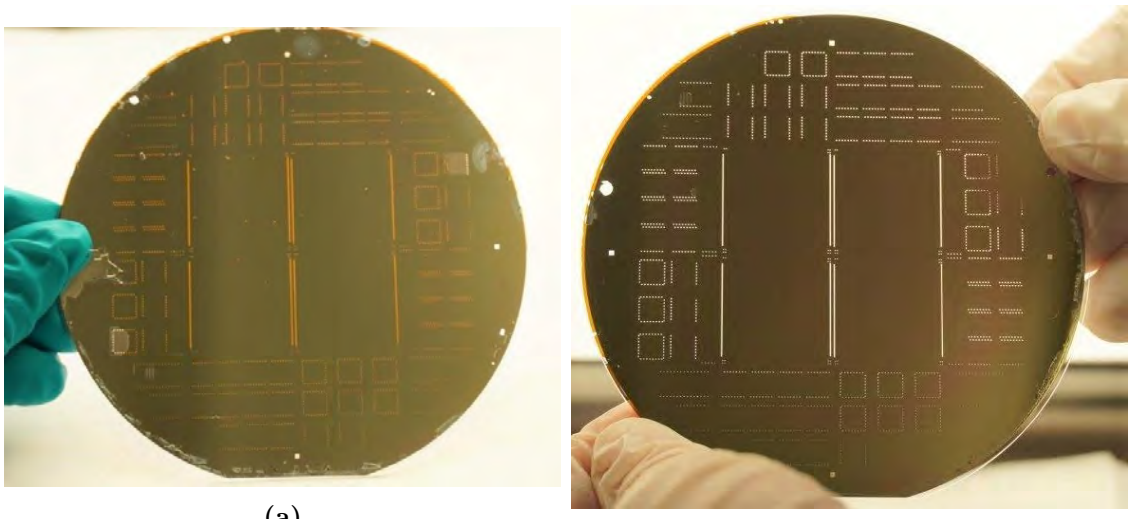
Figure 3.12: A backlit picture of the wafer thinned down to just the poly-Si plate, enabling immediate void inspection. The voids at the periphery have a direct translation to the voids formed at the anodic bonding in Fig. 3.8. The smaller voids over the long RC190 individual test elements stem from the isotropic hole pattern discovered in the KOH, explained in Section 4.3.2. A successful anodic bond with only 7 % of the row-column arrays affected by voids and all four large RC190+190 arrays intact.

Because the previous batch of RC190+190 wafers was over-etched and ruined during the KOH etch of the handle layer, the subsequent batch was continuously monitored for the entire three-hour etching process. After one hour, a pattern of isotropic holes began to emerge see Fig. 3.10 a). This peculiar discovery was examined in an individual study, see Section 4.3.2. These holes, which were observed to have a faster etching rate than the rest of the silicon layer, reached the second BOX layer several micrometers before the handle layer was etched completely seen as the purple holes in Fig. 3.10 b). As a consequence of this, a gentle isotropic dry silicon etch was devised to have a high selectivity of silicon to silicon dioxide to preserve the oxide, see KITISO in Table 3.3, to prevent ruptures of the plate. The wafers were safely etched using this dry etch reaching the second oxide layer seen in Fig. 3.11 a) where the hole pattern is still visible. The final BOX layer covering the poly-Si plate was etched in BHF revealing the plate, see Fig. 3.11 b) where most of the plate is intact despite the pattern of fast etching holes. Due to the top plate thickness of only 2.3 µm, the wafer stack is partially transparent when held up towards the light, as depicted in Fig. 3.12. The blue-colored voids seen in the periphery of the just bonded wafer in Fig. 3.8 correspond directly to the holes in the thinned-down plate in Fig. 3.12. The rupturing of these voids can be highly problematic and elaborated in Section 4.3.3.

3.2.7 Accessing the bottom electrodes

Having arrived at the top plate the 4th lithography mask, *Open alignment*, is used to open up over the four alignment marks in the NESW in order to facilitate alignment for the remaining processing steps. The openings in the poly-Si are dry-etched with SHALLOLR and the resist is removed by plasma ashing. With the plate exposed a 200 nm aluminum layer is evaporated with the Temescal at 10 Å/s onto the surface and patterned by the 5th lithography mask, *Opening to bottom*, to open up over the contact pads to the bottom electrodes from the front, see step 8) in Fig. 3.1.

Aluminum is wet etched for 5 min with Aluminium etchant Phosphoric Acid mixture, PES-77-19-4 (PES) at an etch rate of $\approx 40\,\mathrm{nm/min}$ [77], opening up over the poly-Si plate above the contact pads to the bottom electrodes, see Fig. 3.13 a) where the openings appear orange due to the 2.3 µm plate as it did in Fig. 3.12. The aluminum is used as a hard mask for dry etching the poly-Si with SHALLOLR in step 9) in Fig. 3.1. The etch is timed so that corresponds to the thickness of the top plate. A comparative picture is taken after the plate has been etched see Fig. 3.13 b), where the openings appear white. Afterward, the photoresist is stripped by plasma ashing. A sequential microscope image series of these three steps can be seen in Fig. 3.14. Previously, chromium bottom electrodes were employed until it was discovered that chromium failed to meet the ωRC-design criterion as described in Chapter 1. The chromium could not endure the plasma ashing resulting in damage to the bottom electrodes, however, this is not an issue with gold bottom electrodes as observed in Fig. 3.14.



(a) **(b)**

Figure 3.13: Camera images of the wafer during the process of accessing the contact pads of the bottom electrodes. The aluminum layer is wet etched using PES for 5 minutes. This etching procedure results in the removal of the aluminum layer, revealing openings over the poly-Si plate above the contact pads to the bottom electrodes. These openings can be observed in image a), where they appear orange due to the 2.3 µm thickness of the plate. After dry etching open the poly-Si top plate above the contact pads the openings appear white as seen in b). This process is also illustrated with microscope images in Fig. 3.14.

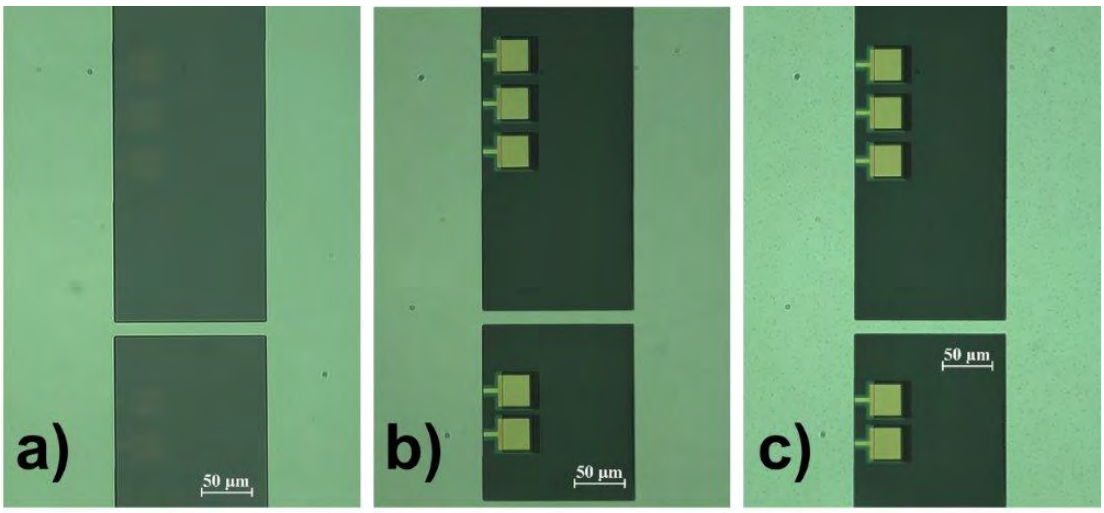


Figure 3.14: Microscope images of the apodization contact in the northeastern corner of an RC190+190 array corresponding to the process flow steps 8)-9). a) Shows the opening of aluminum by wet etching in PES, b) shows the opening dry etching through the poly-Si top plate and thereby opening down to the bottom electrodes contact pads. c) After stripping the resist by plasma ashing, inspect that the gold electrodes are intact. The microscope image a) correspond to Fig. 3.13 a) and likewise for b) and Fig. 3.13 b).

3.2.8 Definition of top electrodes

The final layer of 800 nm thick aluminum is e-beam evaporated and is used for the top electrodes and also to plug up the contact pads and ensure a vacuum inside the CMUT cavities. This air-tight sealing of the 3D structured contact pads requires a thick layer which is why a thickness larger than two times the cavity depth (given in Table 3.2) is deposited and good step coverage is obtained. E-beam evaporation is not usually utilized for high conformal coatings due to the line-of-sight deposition, however, the Temescal is equipped with a rotating sample holder with a planetary motion that improves the step coverage compared to a stationary holder. Inspection of the plugged contact pads has been performed with SEM on a previous batch, 2nd generation of the RC190+190 run, showing that the entrance from contact pads to connecting wire is indeed sealed [60]. The top electrode aluminum layer is now 1 µm thick and the step height down to the bottom electrode contact pad is around 3 µm, spin coating the regular 2 µm resist resulted in some inconsistency around the contact pads. As a result of this, the thickness of the photoresist was doubled to 4 µm and could be combined with a slower spin out to completely cover the step height. This final and 6th lithography mask, *Top electrode*, utilizes the aluminum both as contact pads for the bottom electrodes and simultaneously as top electrodes as seen in Fig. 3.15 a). The aluminum is etched by IBE with the *Al etch with resist* recipe, developed by my colleague Rune S. Grass where the etch rate for the bulk regions is 25 nm/min. Based on this the etch should be finished after 40 min, although there is a slower etch rate in the trenches between the top electrodes due to the aspect ratio and 15 min of over-etch is necessary to separate them. Process experience with the IBE ($Ionfab300$) has shown that due to the physical nature of the ion bombardment combined with the poor thermal insulation of the glass substrate, this etching process has to be done in steps. For this batch, the etch was divided into 5 steps and after etch step the entire wafer chuck with the wafer still mounted and turned upside down is transported to the microscope for inspection.

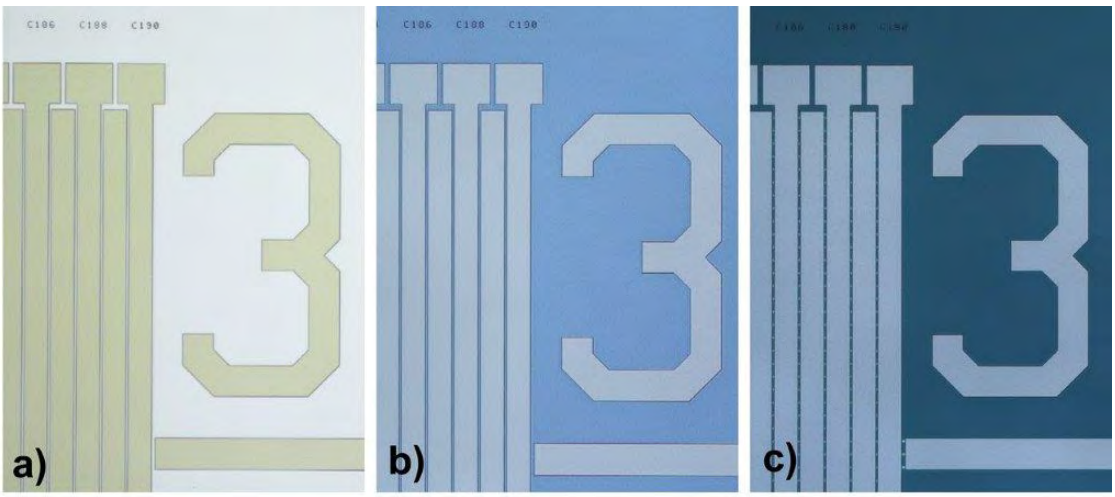
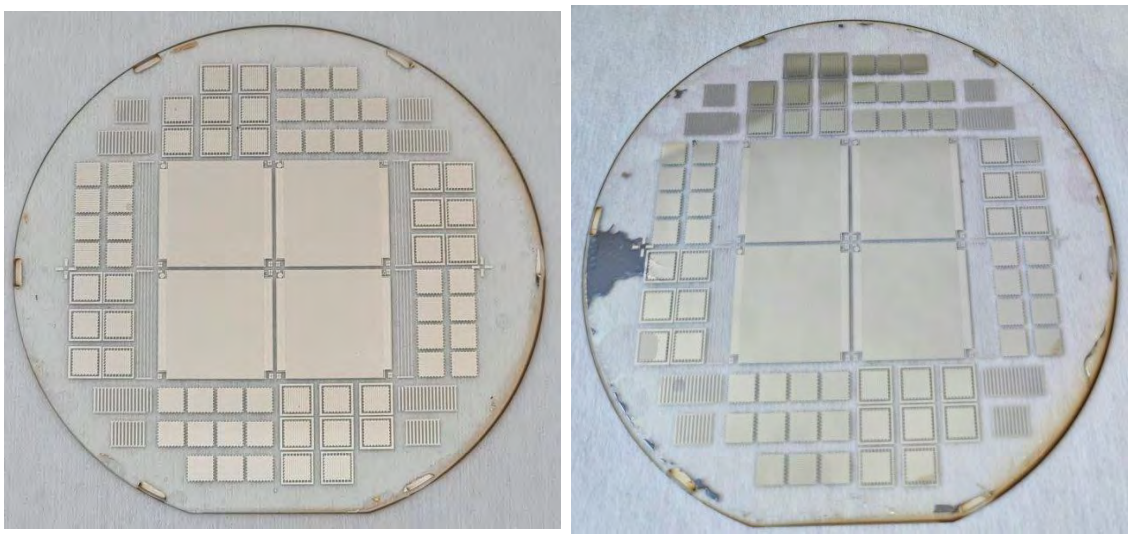


Figure 3.15: Microscope images showing a) the final lithography mask on top of the 800 nm aluminum layer, b) the completed 55 min IBE etch and c) the dry etching of the poly-Si top plate separating the contact pads and top electrodes and revealing the orthogonal connecting wires in the kerf beneath the oxynitride layer.

The wafer is kept mounted as the clamps that hold the wafer down to the chuck are also etched by the physical etch and become brittle over time and when a satisfactory clamping is obtained it is best to detain it. The microscope inspection is to check that the sample is being sufficiently cooled and the scorching of the arrays isn't present along with inspecting the progress of the etch, especially the 18.05 mm long and only 6 µm wide kerf between the top elements. The completed IBE etch of the aluminum can be seen in Fig. 3.15 b). Lastly, the poly-Si is dry-etched with the ASE tool separating the top electrodes and revealing the connecting wires of the bottom electrodes beneath the oxynitride layer see Fig. 3.15 c) seen as the connecting wires orthogonal to the top electrodes. The photoresist is stripped by plasma ashing. This finalizes the wafers and corresponds to step 10) in Fig. 3.1. A stitching microscope was utilized to take high-resolution images of the four large RC190+190 arrays for characterization purposes which can be seen together with a zoom-in on a finalized contact pad for both the top and bottom electrodes with dimensions of 150 µm and 175 µm required for wire bonding. Images of the finalized wafers are shown in Fig. 3.16 displaying the two wafers, TH1_20220302 a) 01 and b) 04. A stitched microscope image of a finalized RC190+190 array is seen in Fig. 3.17.



(a) (b)

Figure 3.16: Picture of the two finalized wafers with a combined 8 RC190+190 arrays. For future processing reference, the identifying name of these wafers are TH1 20220302 a) 01 and b) 04. A leftover silicon piece, as a result of non-uniform etching.

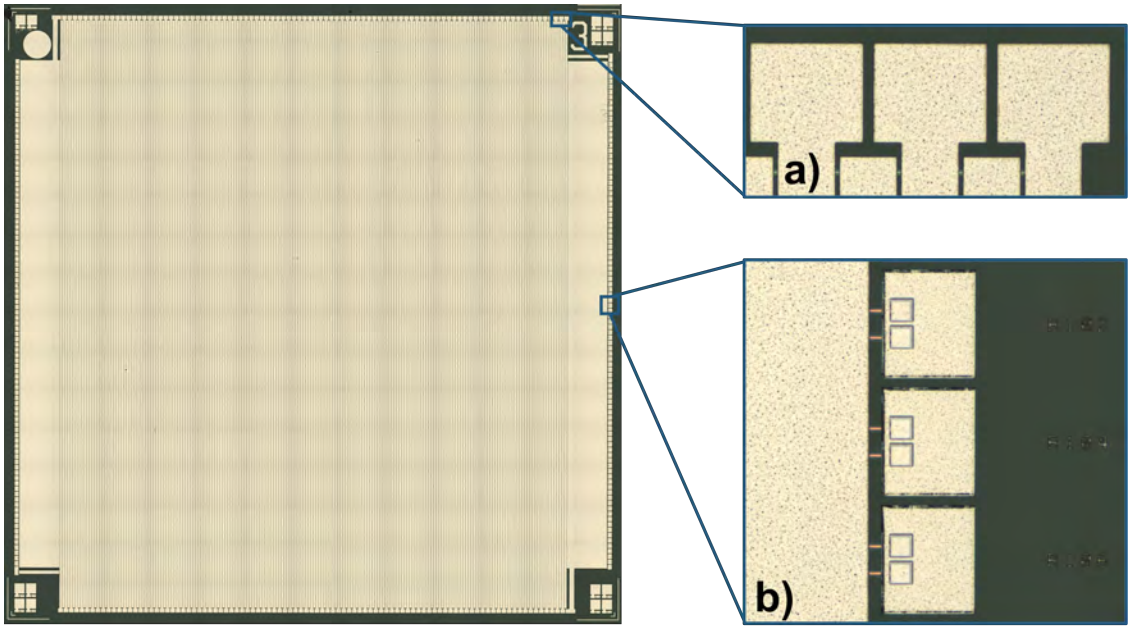
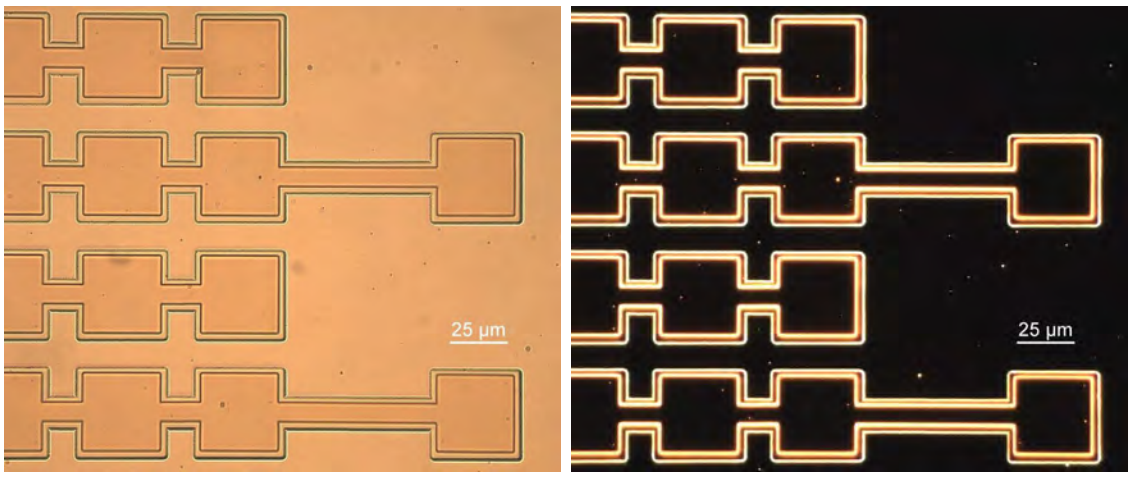


Figure 3.17: High-resolution microscope image of the 3rd RC190+190 array named, RC3. Taken with a stitching microscope. Zoom in on a) the contact pads of the top electrodes and b) the contact pads of the bottom electrodes. The purpose is to do visual characterization together with electrical and in the future take high-resolution stitching microscope images at every key step of the fabrication to trace back steps and pinpoint where the issue arose.



(a) (b)

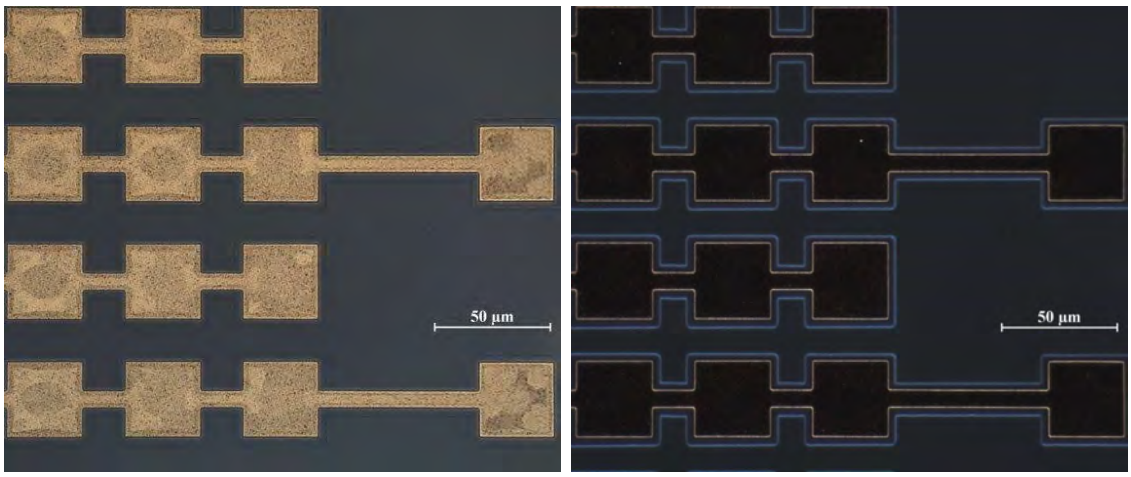
Figure 3.18: Brightfield a) and darkfield b) at the same location on the same location of an RC512+512 array after the gold has been evaporated with patterned resist on top to define the bottom electrodes. In the brightfield image a) some particles are observed and by having the exact same image taken with darkfield b) it is easy to distinguish gold particles from dust or resist residue particles as the metal lights up comparatively more in the darkfield image. Tracking the particles is important to determine the consequences for later processing and electrical characterization of the CMUT.

3.3 Fabrication of RC512+512

The RC512+512 wafers are also fabricated utilizing anodic bonding and based on the same process flow as the RC190+190 wafer just presented in Section 3.2. In this section, only the improvements made to the RC512+512 wafers based on the processing experience from the RC190+190 batch are presented. Throughout the description, references are made to several process optimization studies which are covered in full detail in Chapter 4.

3.3.1 Bottom electrodes

In accordance with a study done by DTU Nanolab on particle formation during metal deposition that showed a direct correlation between the evaporation rate and the number of particles after metal evaporation the evaporation rate was decreased from 3 Å/s to 1 Å/s for the gold bottom electrodes. As an initiative to track the particle distribution a bright and darkfield microscope image of the same location is captured, see Fig. 3.18. Darkfield microscope images are especially good for distinguishing metal particles and as observed in Fig. 3.18 b) there are considerable amounts of particles. The topic of gold particles is treated in Section 4.2.2.
To utilize the etching processes already proven robust for the RC190+190 with a metal stack of 10 nm Ti adhesion and 234 nm gold, the RC512+512 was designed with a 10 nm Ti adhesion layer and a 240 nm gold layer. The definition of the bottom electrodes was performed with the same procedure as the RC190+190 wafers i.e. first IBE, then 1 s of potassium iodine etch followed by a gentle plasma ashing of the hardened topmost layer of the resist. Unfortunately, the subsequent wet chemical resist strip in remover 1165 proved inefficient at the normal submersion time of 25 min. The wafers were pulled from the remover and the wettability was showing that the resist persisted after 35 min. Therefore, after having checked multiple times



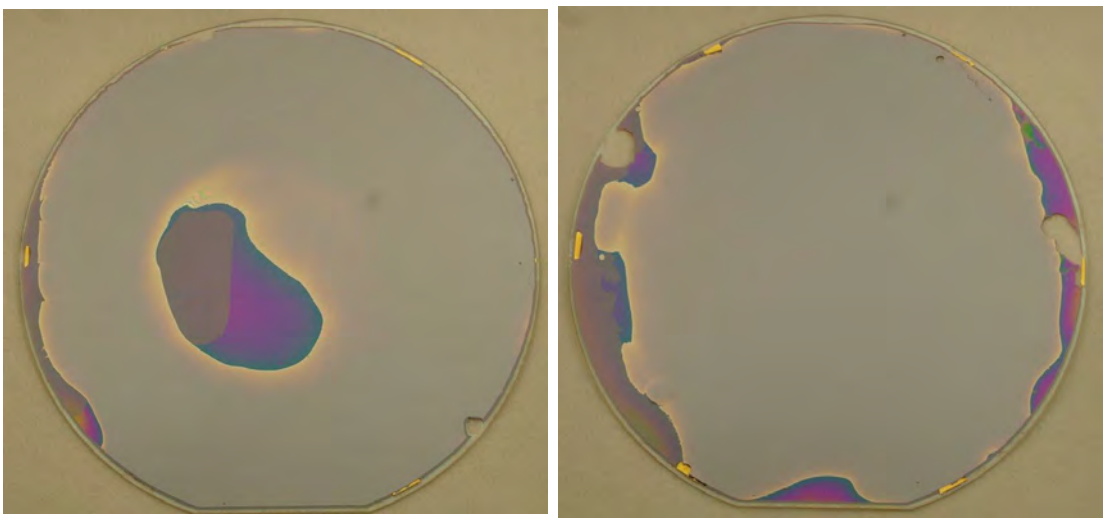
(a) (b)

Figure 3.19: In a) a brightfield image of the bottom electrodes after resist strip in remover 1165 for 4 h 30 min with ultrasonic agitation to remove the stubborn resist after the IBE etch. Unfortunately, this resulted in cavitation of the metal and the discoloration and roughening of the gold bottom electrodes show the pattern where the resist was stuck. However, after the stylus profilometer the gold is measured to be uniform, which is also indicated by the dark field image as edges in the metal would light up.

after 60 min with minor progression, however, in some places the resist was removed and the gold appeared shiny metallic. Thus, the wafers were submerged for another 90 min followed by yet another 2 hours in total 4 hours and 30 min, which finally removed the remaining resist. Customarily during resist striping ultrasonic agitation is applied, unfortunately, that resulted in cavitation of the metal as the resist had been removed sometime within the 90 min submersion. It was discovered during the stylus profilometer measurements that the vacuum gap varied between 160 nm to 165 nm, where the target vacuum gap was $g = 135$ nm and it deviates 25-30 nm. Also, a microscope image of the bottom electrodes, see Fig. 3.19, shows a pattern of where the resist was stuck as the gold has discoloration in the pattern. Fortunately, the discoloration does not show a height difference when examined with the profilometer. The pattern showed where the resist exhibited strong adhesion and required significant effort to remove.
In accordance with the piranha etch test described in Section 4.2.4 the piranha cleaning time of the bottom electrodes was increased from 30 s to 5 min. Piranha cleaning is performed to remove resist residues, organic particles from handling and also trace metals. Microscope inspection was done pre and post-piranha and showed no etching of the metal consisting of a 10 nm titanium adhesion layer and a 240 nm thick gold layer.

3.3.2 Anodic bonding

In a study conducted in collaboration with DTU Nanolab, see Section 4.3.2, the isotropic hole pattern was determined to originate from the wafer bonder chuck. Furthermore, the test showed that even after replacing the old chuck with a new chuck sporadic isotropic holes with a faster etch rate in KOH occurred and in increased numbers. As a test a blank silicon wafer was anodically bonded to a borosilicate glass wafer with an intermediate graphite sheet between the silicon wafer and the wafer chuck with the exact same recipe as for the RC190+190 and etched for 1 hour



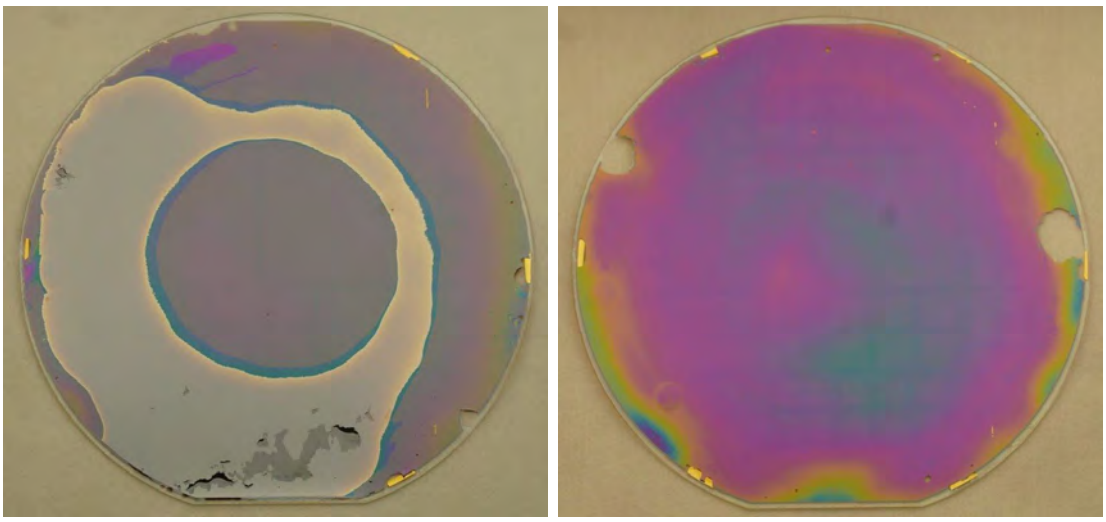
(a) (b)

Figure 3.20: Two RC512+512 wafers after 3 hours 15 min in KOH at 90 °C where the non-uniformity of the etch can be observed. Often, the KOH will begin to clear the silicon from the center seen in a), however, this is not always the case as seen in b). As this last step is not equal for all wafers in the batch, the completion of the etching for each wafer should be performed individually in order not to severely over-etch other wafers in the batch.

in KOH at 80 °C and showed 1-2 isotropic holes. As a result, the RC512+512 wafers were anodically bonded with the graphite sheet as an intermediate layer between the PSOI wafer and the cathode. The process flow still relies on alignment bonding, hence a square hole was cut in the graphite sheet in order to keep a vacuum suction for the wafers to be aligned prior to bonding. The alignment was successful and the vacuum was maintained.

3.3.3 Thinning down to the top plate

To prevent flakes of poly-Si plates from adhering to the exposed wafer surface when the voids burst, the wet chemical KOH etch was selected. This decision was made despite concerns about the fast etching of isotropic holes, which were mitigated by the use of a graphite sheet as an intermediate layer during anodic bonding. Nevertheless, the final BOX layer should work as an etch stop, due to the high selectivity of 1:200. However, it is important to note that the etching process may not be completely uniform, necessitating regular inspections of the wafers. Often, the etching solution will initially penetrate the silicon from the center as seen in Fig. 3.20 b), causing the silicon front to gradually advance towards the wafer's edge. This final step may not be the same for every wafer in the batch as observed in Fig. 3.20 a), and it is crucial not to over-etch individual wafers. Careful attention is paid to this process. To ensure, that the BOX layer endures the KOH while also keeping the voids likely to burst submerged the wafer was held manually half-submerged in the KOH and rotated accordingly to the silicon clearing and the BOX layer emerging for the last hour, see Fig. 3.21 a). This way as the plate becomes thin and burst, the dislodged flakes will be dissolved in the etchant without adhering to the wafer surface and simultaneously preserving the BOX layer.
Furthermore, the solution to implement the graphite sheet as a shielding intermediate layer during anodic bonding was successful since as little as 4 isotropic holes



(a) (b)

Figure 3.21: A picture of a half-etched silicon handle layer is seen in a) as the wafer was manually held in a half-submerged position in the KOH solution and rotated according to the silicon clearing and emergence of the BOX layer. This is to ensure that as the plate becomes thinner and voids burst, any dislodged flakes would be dissolved by the etchant without sticking to the wafer surface while not over-etching the BOX layer where the isotropic holes are. In b) the silicon handle layer is completely etched and the BOX layer is exposed and successfully etching away the burst voids without leaving flakes at the wafer surface.

were observed, see Fig. 3.22. These microscope images were taken with the stitching microscope, as described in Section 3.2, these high-resolution stitching images were taken for all key fabrication steps for the RC52+512. The BOX was reached without perforating the oxide layer, yet the four holes are still noticeable see Fig. 3.21 b). Finally, the BOX was etched in BHF, and the top plate reached showing a successful thinning of the PSOI layers, see Fig. 3.23.

In the pursuit of eliminating the short-circuiting poly-Si flakes from the void ruptures a designated void removal step was introduced. For the RC512+512 wafers, concurrently with the photoresist used for opening over the alignment marks a manual microscope exposure over the voids was carried out. Prior to conducting this on the RC512+512 wafers, the microscope exposure and development processes were tested on a blank dummy wafer to determine the appropriate dose and assess the development results. In this way when dry etching through the top plate to access the alignment marks the voids are intentionally etched or, as discovered, burst when pumping to vacuum in the ASE tool and landing on top of the resist, see Fig. 3.24 a). To ensure that the flakes are removed from the most important areas a manual resist strip was done using a spray bottle to direct the removal away from the two large RC512+512 arrays. The resist strip consisted of Remover 1165, Acetone and IPA in that order. A stitched microscope image of the exposed poly-Si top plate shows only a few stray flakes compared to the RC190+190. The challenges and considerations of the plate ruptures and the poly-Si flakes adhering and ultimately shorting between elements are presented in Section 4.3.3. The RC512+512 wafers are at the time of writing at step 9) in Table 3.1 where aluminum over the contact pads has been etched, see Fig. 3.24. The wafer shows a structural yield and a void-free area of 7 cm × 7 cm demonstrating the viability to fabricate future RC1024+1024 chips. Unfortunately, the IBE has been out of use since Jan 2023 and was first back in use

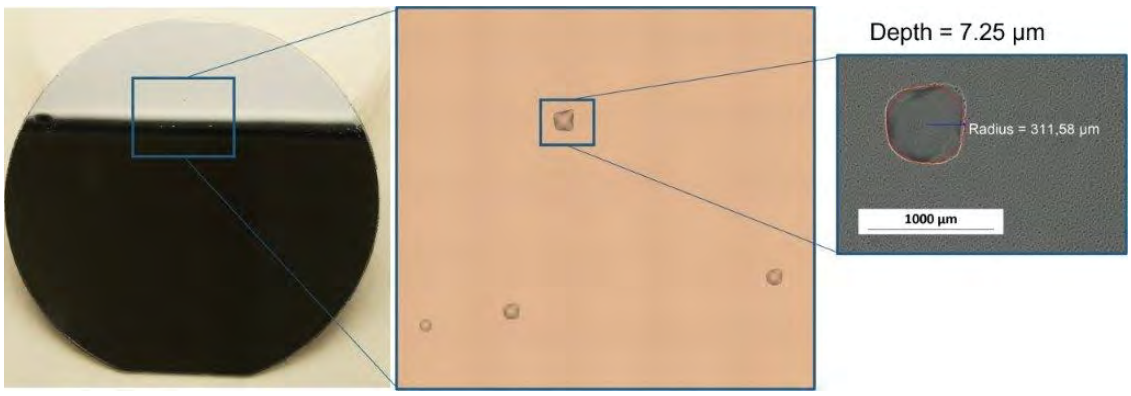
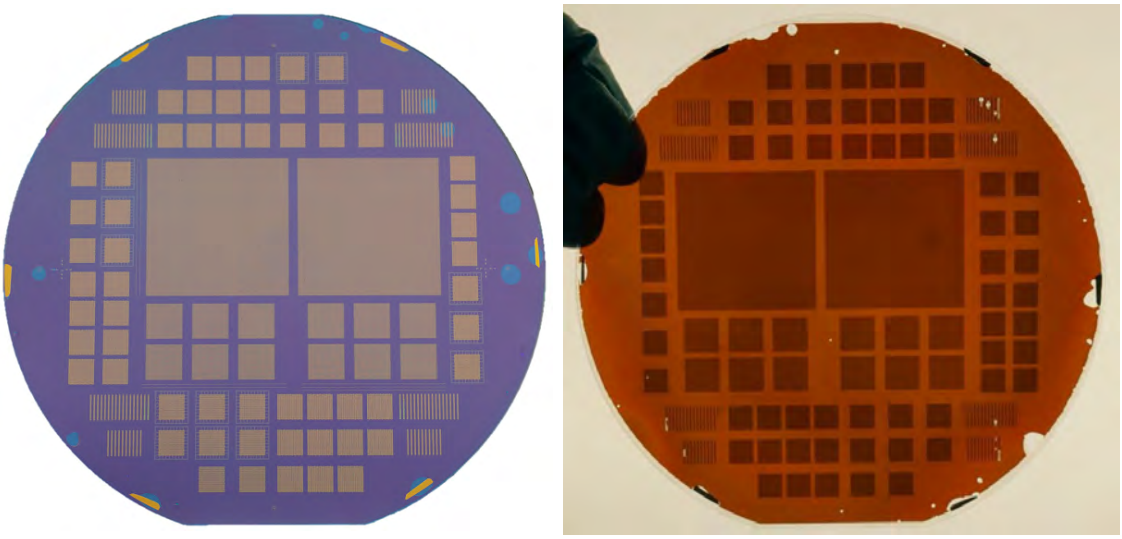
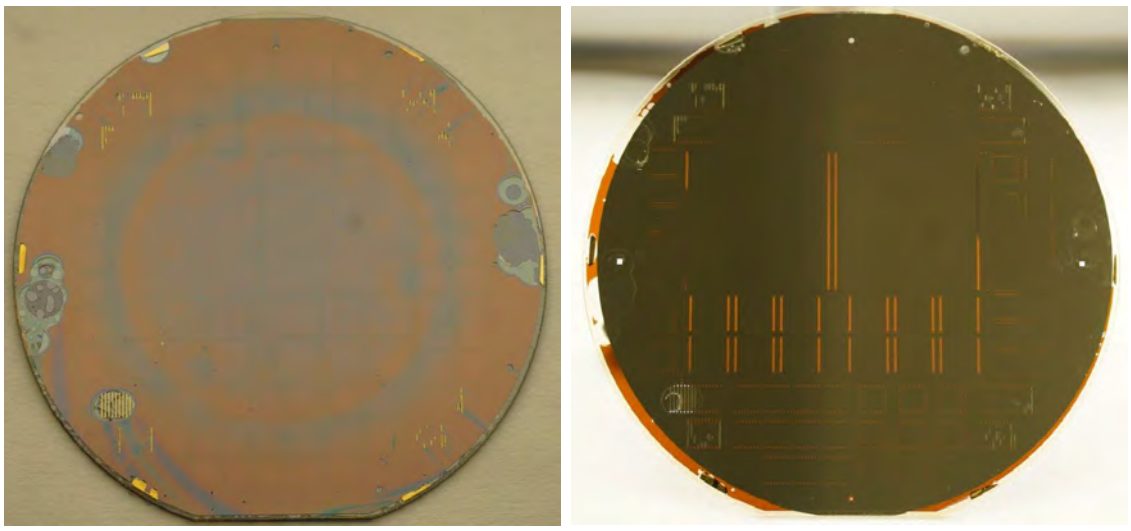


Figure 3.22: Picture of the RC512+512 wafer after 90 min KOH etch showing only 4 isotropic holes after the graphite sheet was implemented as an intermediate layer in anodic bonding. A stitched high-resolution microscope image was taken for the full wafer with a cut-out here showing the four isotropic holes. A zoom-in on the largest show a radius of 311 µm with a depth of 7.25 µm.



(a) **(b)**

Figure 3.23: In a) is a picture of an anodic bonded RC512+512 wafer which has just been bonded and in b) the layers of the PSOI wafer has been etched away and thinned down to the poly-Si top plate. It is clear that the increased piranha cleaning time from 30 s to 5 min compared to the RC190+190 wafer, reduced the number of voids observed after bonding, see Fig. 3.12.



(a) **(b)**

Figure 3.24: In a) the poly-Si top plate is covered with a photoresist. The marks from the microscope exposure, which are located over the voids along the periphery, have been exposed. Additionally, openings over the alignment marks are also exposed, and all of these areas have been dry etched in the ASE tool. The flakes from the burst voids are seen lying on top of the resist as either grey flakes for the poly-silicon side facing upwards or purple-blue when the oxynitride side is facing upwards. The flakes are primarily located in the bottom left corner. In b) the first aluminum layer has been deposited and openings over the contact pads to the bottom electrodes have been etched out in the aluminum still covered by the poly-Si top plate which is why the contact pads appear orange in the backlight, this step corresponds to step 8) in the process flow Fig. 3.1.

in May 2023 and consequently, the wafers have not yet been finalized.

3.4 Chapter summary

In this chapter, a comprehensive explanation of the fabrication process of the anodically bonded RC190+190 array was presented along with a subsequent description of the optimizations and modifications implemented in the process flow for the RC512+512 array. The entire fabrication procedure was outlined for the RC190+190 wafer, providing specific details for each step. The chapter concluded with the presentation of the resulting wafers containing the eight large-scale RC190+190 arrays. Brief descriptions of the areas requiring optimization were also provided and referred to in the following chapter which will cover the process optimization. The finalization of the RC512+512 wafer was hindered as the Ion Beam Etcher (IBE) was out of use in the last 5 months of this Ph.D. project, however, fabrication was halted at step 10) in the process flow so it is nearly finalized. All fabrication was conducted within the cleanroom facilities of DTU Nanolab and with the help for optimization by the process specialist. The next chapter will give a thorough description of the process optimizations made to finalize the RC190+190 wafer and to realize the RC512+512 wafer.

Chapter 4

Process optimization

4.1 Introduction

The task of optimization of the fabrication process is presented in this chapter, while the fabrication of the RC190+190 wafer and RC512+512 wafer was discussed in the previous chapter. The structure of this chapter starts with the bottom wafer and bottom electrode definition followed by the wafer bonding and thinning of the layers to define the CMUT. In this chapter the challenges during fabrication are described and the consequences they impose on the realization of a fully functional row-column CMUT array. In addition, the experiments and characterization that were performed to solve the challenges and finally, the solutions that were implemented are elaborated. An overview of the challenges encountered, the time of discovery and the corresponding solutions are presented in Table 4.1. The processes that were characterized and targeted for optimization, as described in Table 4.1, are listed below in the order in which they are presented in the chapter:

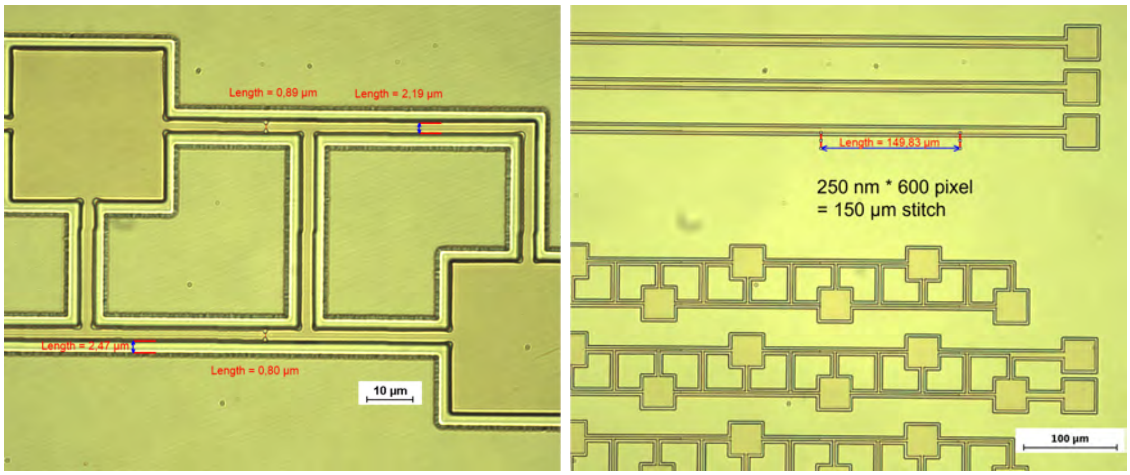
- **Bottom wafer:**
  - Stitching error for the bottom electrode lithography process
  - Gold particles at metal evaporation
  - Formation of gold ribbons during IBE
  - Piranha clean prior to bonding
- **Anodic bonding:**
  - Aluminum as bottom electrode metal
  - Damages to the metal during anodic bonding
  - Short circuits between the top and bottom electrodes
  - Reduced voltage during anodic bonding
- **Thinning down of the top PSOI wafer:**
  - Isotropic holes in KOH
  - Voids causing top plate ruptures and flakes.

The unresolved issues are discussed in an open-ended manner. The author encourages engagement and welcomes any inquiries or contributions pertaining to especially the unresolved issues discussed. Valuable insights, alternative perspectives,

or additional research findings are highly appreciated in order to further advance understanding and address these challenges. The RC190+190 wafers presented in Section 3.2 have the batch named, (TH1_2022022) and the RC512+512 wafers presented in Section 3.3 have the batch named, (TH1_20220607) for future Ph.D., masters and bachelor students that would like to examine and track the logbooks among other documentation and characterization. Two of the larger general initiatives to optimize the process implemented by the author are microscope images taken at the exact same location and particle scans throughout the fabrication steps. The same location microscope images allow for reverse engineering and pinpointing where the challenges arise. The key fabrication steps were documented using high-resolution full-array scale images obtained with a stitching microscopy technique. This stitching microscope was kindly borrowed from NILT, a nanotechnology engineering company operating within the DTU Nanolab clean room. The continuous particle scans are performed either on the PSOI wafer or on a clean silicon dummy wafer included in the processing step to determine the contamination degree of the step to minimize particle contamination as this is a limiting factor in successful wafer bonding. The silicon dummy wafer is utilized as the particle scanner is unable to scan structured wafers.

Table 4.1: Overview of the process optimization aligned with the fabrication steps.

Step	Process flow	RC190+190 Implemented	RC190+190 Discovered	RC512+512 Implemented	RC512+512 Discovered
3	Cr is removed, leaving a pure glass wafer with cavities	Multiscan step height measurements Piranha post step height measurements			
4	Gold is evaporated and the bottom electrodes are defined by lithography and etched with IBE	Overexposure avoid stitching error Wet gold etch of ribbons before resist strip	Gold particles correlation with backside image after anodic bonding		Form of the day metal - particle scan + darfkfield image Cavitation during resist strip
5	The PSOI wafer is fabricated and openings in the oxynitride are etched in the mirror image of the bottom wafer	Particle study, removal rate and roughness Dry etch for oxynitride, KITOXYSI		5 min piranha for fewer voids in bond	
6	Anodic alignment bonding of the bottom glass wafer and the structured top PSOI wafer is performed	Larger connecting wires, avoid burning in bonding	Explosions and burning on bottom electrode contact pads	Graphite sheet intermediate layer during anodic bonding	
7	Thinning down the PSOI layers: Oxynitride, poly-Si, Oxide (BOX), Silicon handle, BOX to reach and define the top poly-Si plate	Constant survilance of KOH	Isotropic holes in KOH with faster etch rate	Holding wafer for KOH etch manually, preserve the BOX layer keep voids submerged	
8	The 1st aluminum layer is deposited and lithography used to define openings over the contact pads of the bottom electrodes		Opening alignment marks with dry etch, leading to voids that burst poly-Si flakes	Avoid dry etching, etch voids manually to avoid poly-Si flakes adhering to surface	Voids burst during pump down to vacuum, exposed intentionally to land on protective resist stripped manually
9	Opening up through the poly-Si top plate over the contact pads through dry etching and stripping the resist		Electrode damage of bottom electrodes opening up over contact pads through dry etching originates from bonding not plasma exposure	Microscope inspection of all steps at the same location allows back tracking	
10	The 2nd aluminum layer plugs up the contact pads and is used for both top electrodes and contact pads, patterned with lithography and etched with IBE and dry etching	4 µm photoresist, 2x thicker for better coverage at contacts			



(a) (b)

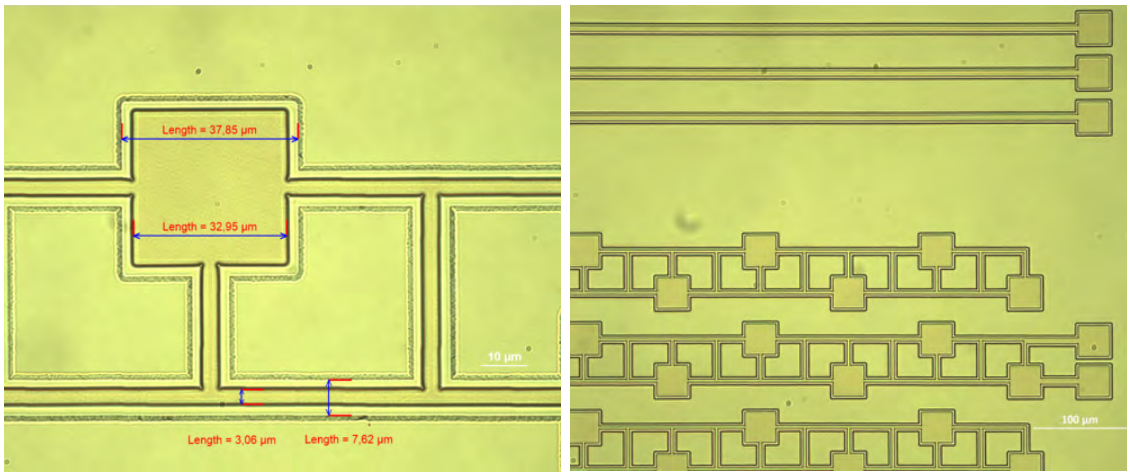
Figure 4.1: Stitching error of the MLA, observed every 150 µm due to 600 pixels at a grid of 250 nm in fast mode seen in b). This stitching error resulted in a narrowing of the connecting wires to 0.8-0.9 µm only 30% of the designed width as seen in a).

4.2 Bottom wafer

4.2.1 Stitching error

The lithography process of the bottom electrodes is an image reversal process using a positive resist, as the preferred negative resist can not be exposed with the maskless aligner (MLA) 2 having the 375 nm laser as it suffered from innumerable hardware and software failures as well as focusing errors. Additionally, the mask polarity was also tried inverted but suffered from overexposure. Therefore, an image reversal lithography step was devised, For the RC190+190 (TH1_20220322) step 3), in Table 4.1, the dose of the bottom electrodes was doubled for overexposure to avoid stitching error of the MLA, see Fig. 4.1 and Fig. 4.2. It is hypothesized that this narrowing resulted in too high a current passing through the metal connecting wires during bonding causing the wires to overheat and burn up, see Fig. 4.14 addressed in subsubsection 4.3.1.2. When the wires are etched with IBE to define the bottom electrode, they could at worst be severed or as seen in Fig. 4.3 become so narrow that the elements have a large increase in resistance.

Stitching refers to the process of overlapping multiple exposures and requires alignment of the substrate and the exposure system to ensure that each section of the pattern is accurately aligned. The term stitching error is used to describe a non-seamless overlap. The stitching error is here seen as the narrowing of the vertical line appearing at the multiplication of the pixels times the addressing grid. In this case, stitching appears at every 100 µm, 150 µm and 250 µm depending on the mode, either *fast mode* with a 250 nm grid or *quality mode* with a 100 nm grid as the DMD width of the MLA can be either 600 or 1000 pixels. For example, using *fast mode* with a 250 nm grid with the 600 pixels that gives 250 nm $\times$ 600 = 150 µm as seen in Fig. 4.1 b). The stitching error and narrowing of the wires were tested by varying the number of pixels, doses and modes of the MLA. The dose test on flat metal wafers coated with resist showed no stitching error, indicating that this issue is correlated with the 3D structure of the CMUT cavities. Increasing the dose from 50 mJ/cm^2 to 80 mJ/cm^2 solved the stitching problem, see Fig. 4.2 where the wires are 3 µm wide and the bottom electrode 33 µm long as specified in the mask.



(a) (b)

Figure 4.2: Microscope images captured at the same location as seen in Fig. 4.1. Overexposure from 50 mJ/cm^2 to 80 mJ/cm^2 solving the stitching problem for the bottom electrode lithography yielding the mask specifications of 3 µm wide wires and 33 µm side lengths, seen in a) and *no* narrowing in a vertical line in b).

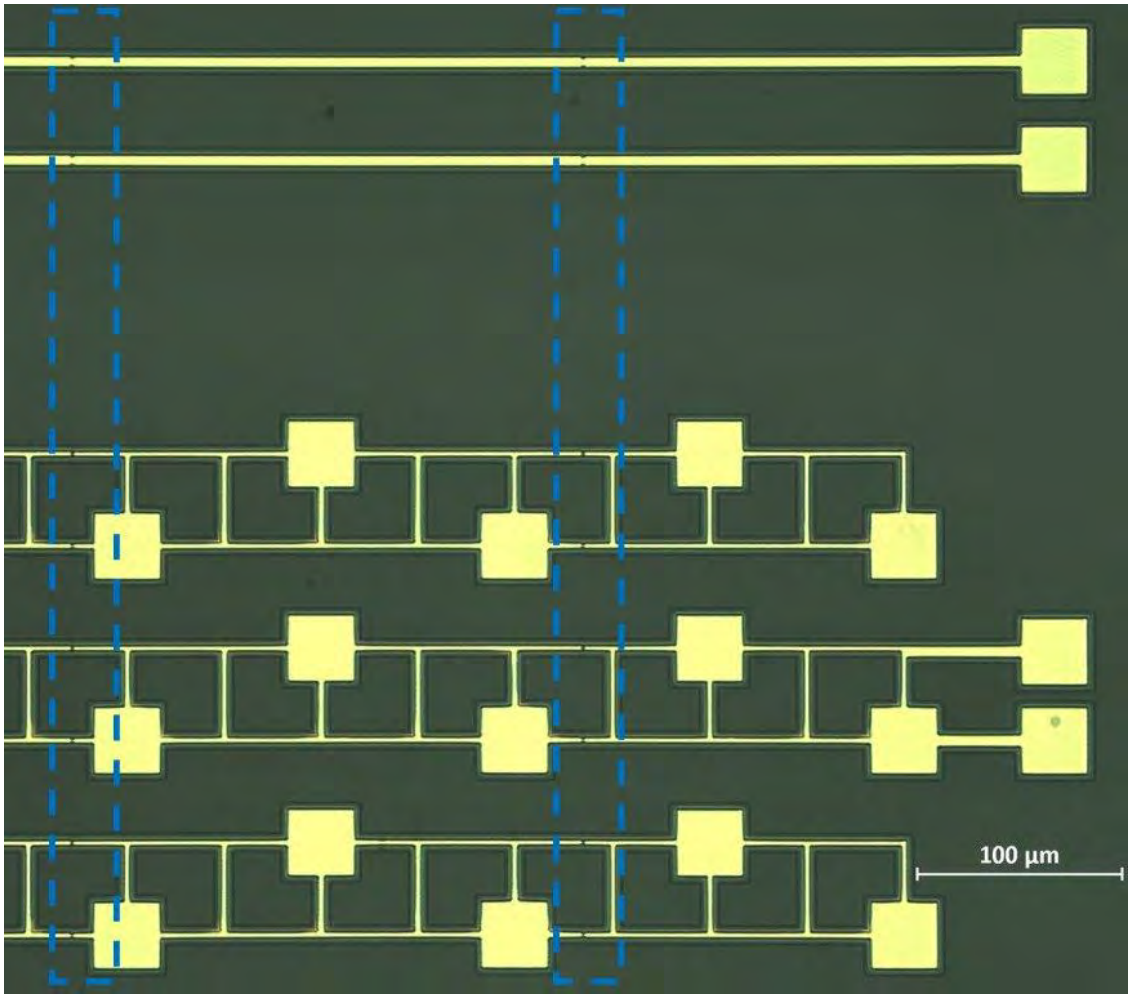


Figure 4.3: Microscope image of stitching error consequences for an ion beam etched bottom electrode, resulting in a narrowing of the connecting wires every 250 µm.

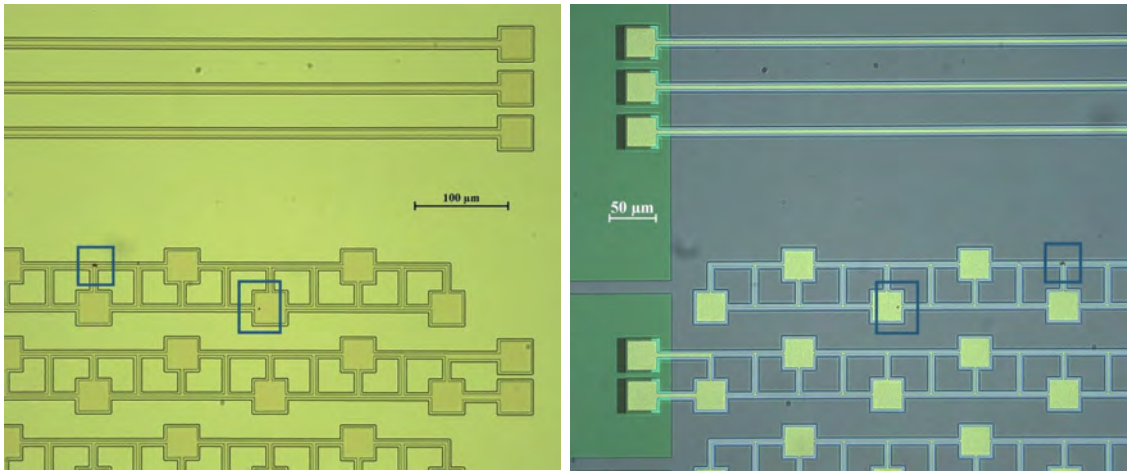
4.2.2 Gold particles at metal evaporation

For the CMUT to have the expected electrical behavior and performance a plane uniform bottom electrode metal layer is required. Since the beginning of this Ph.D., there has been a hypothesis that metal particles in the vacuum gap cause the short circuits that have been measured between the top and bottom electrodes. These short circuits, if present in more than a few elements (preferably none), are detrimental to achieving high electrical yield large-scale arrays. Several different metals and etching techniques have been tested, see Section B.3. On account of the damages observed on the bottom electrode contact pads after bonding, which looked like particles as seen later in Fig. 4.16 the hypothesis was revived again. By comparing particles observed directly after metal evaporation, see Fig. 4.4 a) and after anodic bonding b), it is seen that the exact same gold particles directly after evaporation cause black spots at the center and at the connecting wires after anodic bonding. These dark spots observed from the backside in the bottom electrodes correspond to a short circuit between the top and bottom electrodes and are described in subsubsection 4.3.1.4.

The gold particles larger than the vacuum gap of 135 nm will cause burns and shorts through the top plate of the CMUTs if the breakdown voltage of the insulation layers is not sufficient. The gold particles increase in number with increasing deposition rate during the e-beam evaporation shown by a study made by DTU Nanolab using the Temescal. In the study, the soak and rise time of the e-beam power applied to the metal target was also studied to minimize particles. To limit the number of gold particles, the deposition rate is decreased from 3 Å/s to 1 Å/s for the fabrication of the RC512+512. A Scanning Electron Microscope (SEM) image of gold droplets on an e-beam evaporated gold thin film during the study by DTU Nanolab can be seen in Fig. 4.5 and show the largest spherical gold particle of 2 µm in diameter. This phenomenon is called spitting referring to the liquid droplets ejected from the molten metal target rather than the smooth transfer of material through evaporation, especially pronounced for gold [78].

Particle scans and complimentary darkfield images compared with bright field images of the metal were used to determine the optimal parameters for metallization. Ordinarily, e-beam evaporation with the Temescal *FC-2000* is utilized for metallization. However, a sputtering system from Kurt J. Lesker is also available in the DTU Nanolab Cleanroom. These were tested and particle scans of metallized blank dummy wafers can be seen in Fig. 4.6. This resulted in two evident observations; lower deposition rate gives fewer particles and sputtering produces fewer particles than e-beam evaporation.

A new RC190+190 batch was fabricated where the gold bottom electrode was sputtered, see Fig. 4.7 a) whereas b) is the evaporated bottom electrode for the RC512+512 at the lower evaporation rate of 1 Å/s. The darkfield image of the sputtered metal in a) is pitch black at the flat surfaces, whereas the particles light up all over the flat surfaces of the e-beam evaporated bottom electrode in b). In spite of the lowered deposition rate of 1 Å/s for the evaporated metal, there is still an abundance of particles. This observation led to a hypothesis that the particle level of the metal deposition tool is a form on the day that depends on multiple parameters such as target quality, target height (usage) prior to deposition, prior depositions, chamber conditions and the rise and soak program of the evaporated metal for e-beam evaporation. The particles are usually generated as the e-beam ray heats up the metal target in the crucible it can spit boil if not thoroughly heated, a star pattern for heating the gold target showed the minimum particle generation. For future ref-



(a) **(b)**

Figure 4.4: In a) gold evaporated on top of the wafer and then patterned with a resist to define the bottom electrodes in the cavities is shown. Gold particles are seen on the first element at the intersection and at the center of the cavity marked by the blue boxes. In b) after anodic bonding the particles are still observed from the backside looking through the 500 µm glass wafer upon the Ti adhesion layer. These gold particles are believed to be precursors for the electrode damages discussed in the process optimization and at worst cause shorts if the insulation layer breaks down.

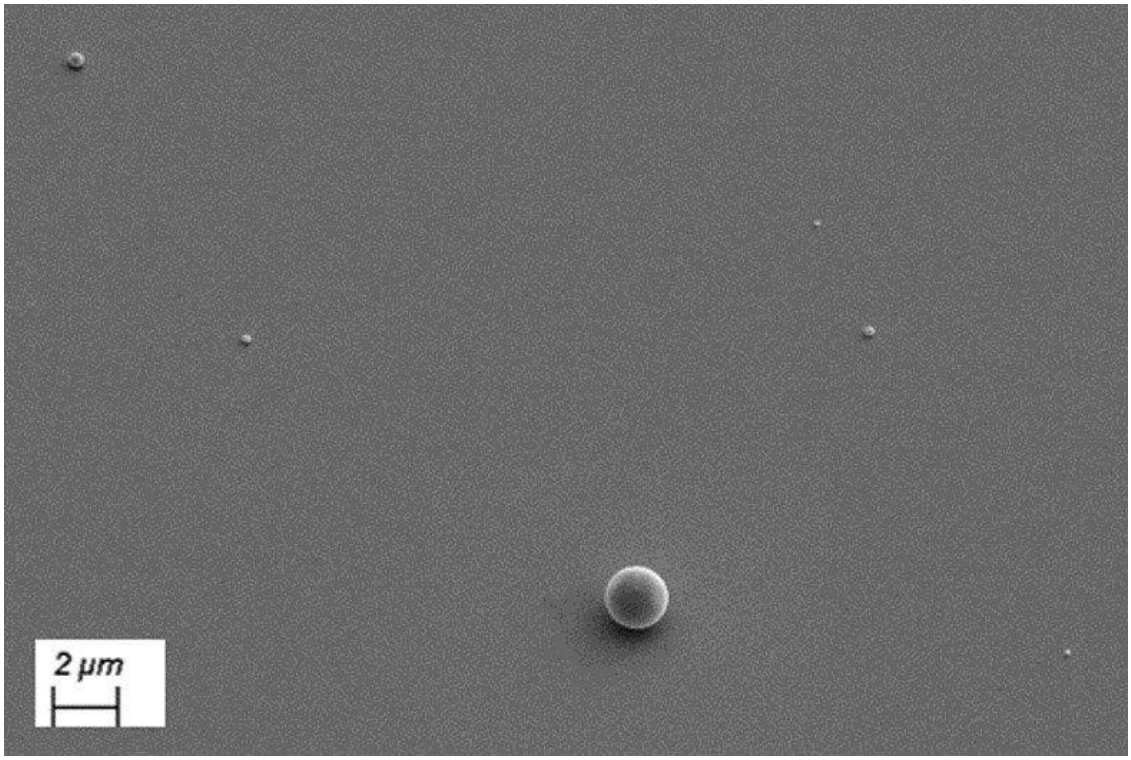


Figure 4.5: SEM image of gold particles on a gold e-beam evaporated layer taken by Evgeniy Shkondin, Au identified by Energy-Dispersive X-ray spectroscopy (EDX). This shows a large gold particle with a 2 µm diameter along with five smaller gold particles or droplets. Picture courtesy of DTU Nanolab.

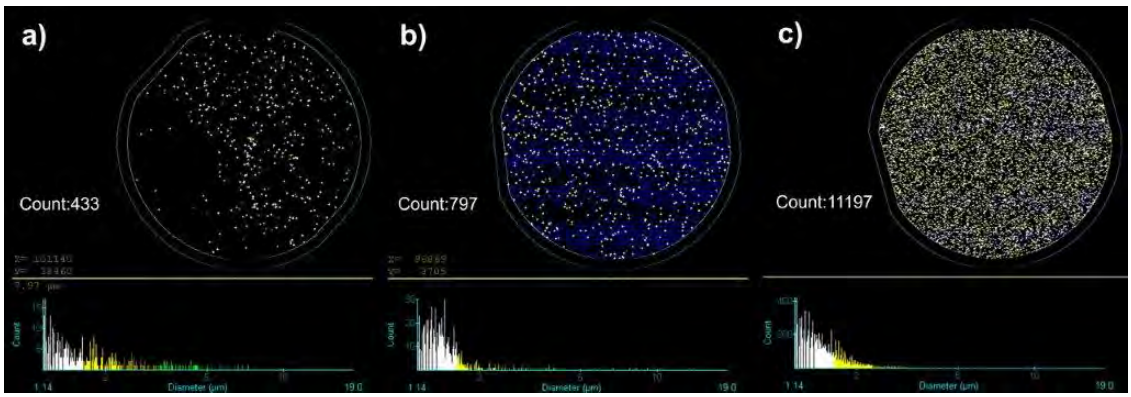
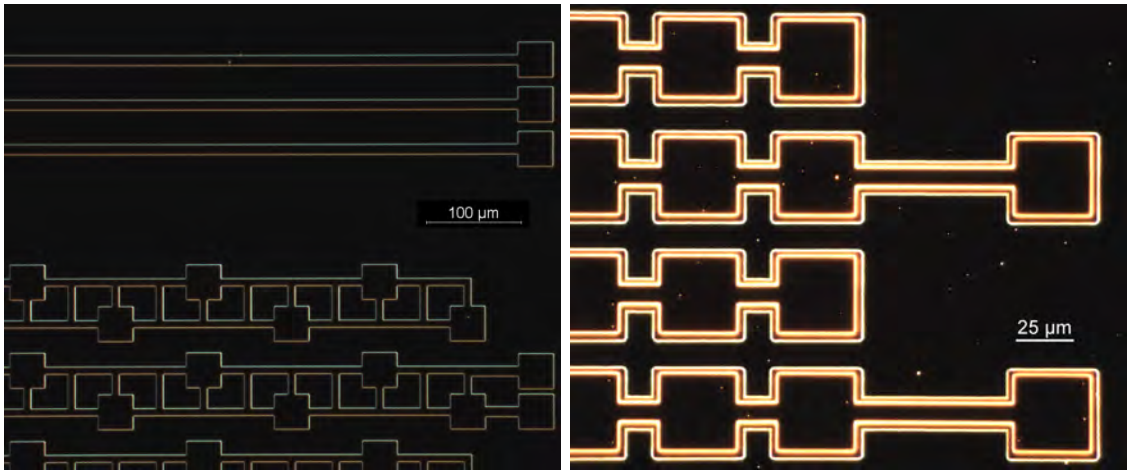


Figure 4.6: Particle scans of gold deposited wafers measured on a scale from 1 µm to 19 µm from left to right a) sputtering of 10 nm Cr and 150 nm Au, b) e-beam evaporation of 10 nm Ti and 90 nm Au at 2 Å/s and 3) e-beam evaporation of 10 nm Ti and 90 nm Au at 10 Å/s. Particle count is as follows: a) 433, b) 797, c) 11197, consequently the sputtering tool is preferred for fewer particles and low deposition rate reduces the number of particles for e-beam evaporation. The particle count of 797 particles is to the date of 1st Sep. 2022 the lowest obtained number of particles, The number of particles is usually around 2000-3000 according to DTU Nanolab.

erence, a blank dummy wafer should be run immediately before metallization and a particle scan and darkfield image should determine if the metal meets the standard of this process. A future study should investigate how few gold particles could be achieved using the metal deposition tools available at DTU Nanolab. Ideally, there should be less than one gold particle per 5 cm × 5 cm. If there is no viable method in-house achieving the goal of an RC1024+1024 probe with anodic bonding should investigate possibilities of metal deposition from outside manufacturers. A deep cavity experiment is to be performed by MS.c student Nikolai Ronnenberg Kirk etching out glass cavities with a depth of 850 nm and evaporating 290 nm gold. Subsequently, anodically bonded to a silicon wafer in order to determine if this eliminates the occurrence of dark spots in the bottom electrodes through a microscope examining the backside of the bonded wafer.

4.2.3 Formation of gold ribbons during IBE

Due to the physical nature of the IBE, metal is back sputtered up onto the sidewalls of the resist, see Fig. 4.8 a) and Fig. 4.9. These thin metal walls are released when stripping the resist, causing them to form a serpentine structure which is why they were named ribbons. The free-standing metal ribbons can cause direct short circuits between top and bottom electrodes after bonding and also when they are torn off they can cause shorting between two neighboring elements as well, shown in Fig. 4.9. The solution was to implement a short wet gold etch prior to stripping the resist to remove the approximately 1.5 µm high and 100 nm wide metal ribbons. This is sketched in Fig. 4.8. The gold etch is a potassium iodine solution that is pitch black, making it impossible to visually observe the etch rate while the wafer is submerged. Tests with bottom wafers from the previous batch, which have had the resist removed and have ribbons, were etch tested and showed that the gold connecting wires were almost completely removed after 10 s. A 2 s dip was found to be sufficient to remove the ribbons and only etches approximately 1 µm of the width. The stated etch rate is 100 nm/min, however, the experience has been that the etch rate is faster and approximately 1 µm/min.



(a) (b)

Figure 4.7: Dark field microscopy images of the bottom electrode made of gold. In a) the gold is sputtered on by the sputter system from Lesker and in b) the gold is e-beam evaporated in the Temescal. There is a clear excess amount of gold particles in the e-beam evaporated gold thin film compared to the sputtered gold thin film.

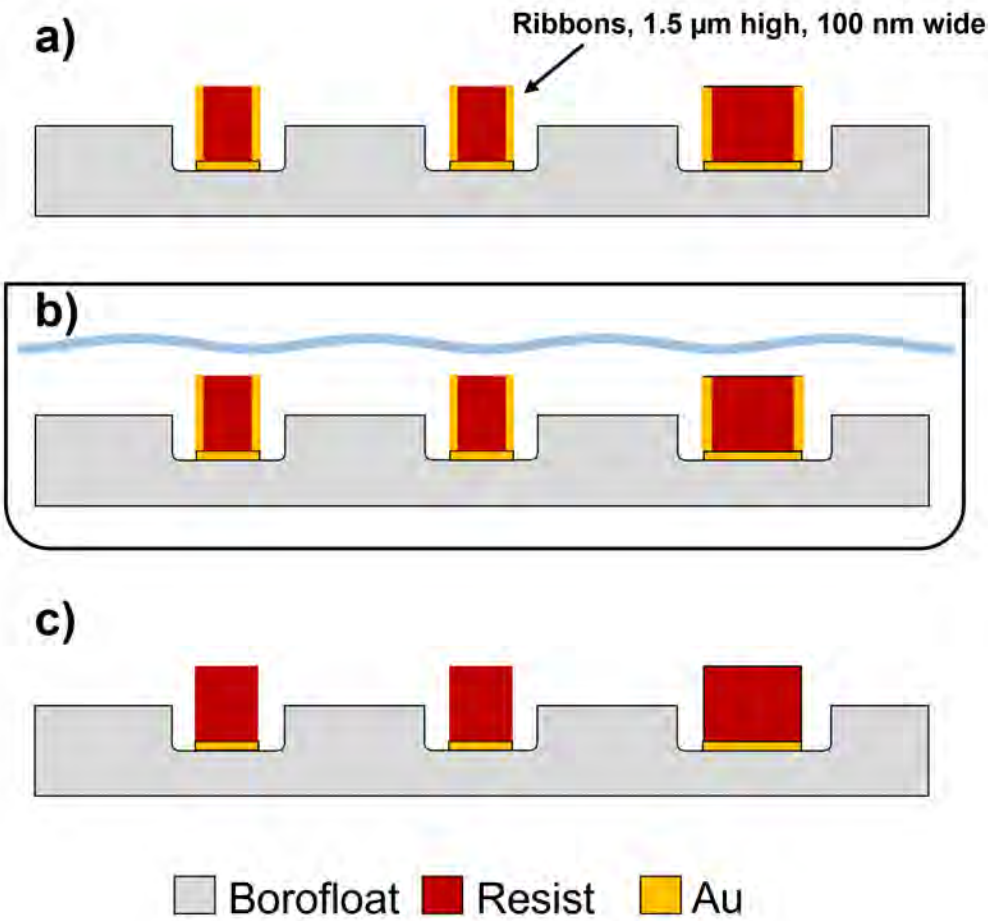
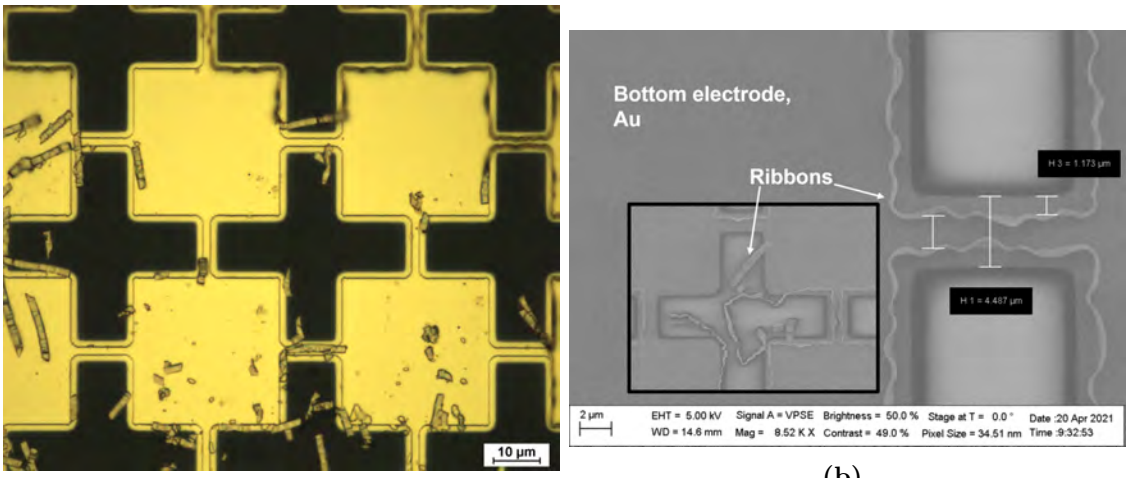


Figure 4.8: Sketch of the gold ribbon removal process. a) The gold ribbons created by back sputtering in the IBE. b) Showing a gold etch (potassium iodine solution) prior to stripping the resist in order only to remove the gold ribbons and c) the final structure after the gold etch of the ribbons.



(a) (b)

Figure 4.9: Microscopy image a) of ribbons created by back-sputtering of the IBE of the gold bottom electrodes back upon the resist and when stripping the resist these are left as free-standing ribbons, causing them to form a serpentine structure. They may fall over causing short circuits between top-bottom electrodes or neighboring bottom electrodes. b) Shows a SEM image of the ribbons, giving a 3D perspective of the ribbons.

To overcome the problem of reduced wire width due to the removal of ribbons, which leads to increased resistance, the connection wire width of RC512+512 was increased from 3 µm of the RC190+190 wafer to 8 µm, while maintaining a 2 µm margin to the glass side walls.

4.2.4 Piranha clean prior to bonding

In order to obtain a successful bond, it is imperative to thoroughly clean both the top and bottom wafers prior to anodic bonding as a clean bonding interface is necessary to achieve a successful bond. The top wafer is usually cleaned in an RCA solution. Customarily, a piranha or piranha clean mixed in the ratio of 4:1 of sulfuric acid (98 %) H_2SO_4 and hydrogen peroxide (30 %) H_2O_2 is used to clean the bottom wafer, which self-heat to 80 °C within seconds and is used to remove organics and metal residues. However, depending on the metal utilized for the bottom electrodes caution of etching or under-etching these is necessary. Several different piranha procedures have been tested in the MEMS group, see Table 4.2. For the RC190+190 wafer, the time of a piranha cleaning was kept to a maximum of 30 s to avoid under-etching the gold bottom electrode by etching the titanium adhesion layer, this resulted in 3 successful wafer bonds. Based on previous fabrication runs made by postdoc Rune S. Grass a piranha clean made without stirring the solution resulted in layer separation and etching of the metal causing the piranha to turn yellow by the reaction of titanium with hydrogen peroxide: $Ti^{4+} + H_2O_2 \longrightarrow Ti(H_2O_2)^{4+}$(orange) at pH below 3 [79]. Due to concerns about etching the Ti which is etched in piranha and thereby detaching the gold from the glass, the piranha cleaning time was advised to be between tens of seconds to a maximum of 1 minute.
The etch rates for gold and titanium in piranha solution have been obtained from [80] to be 0 nm/min for gold and 240 nm/min for titanium. These etch rates have been used in the decision-making process for the process flow development in the MEMS-Applied Sensors Group. If the 10 nm titanium adhesion layer was completely exposed to the piranha solution it would be etched in 2.5 s. Fortunately, the titanium

Table 4.2: Piranha cleaning time and treatment for the last 5 anodic bonded batches. The first batch used chromium, Cr as the adhesion layer however electrode damage was observed during plasma ashing and dry etch steps using the ASE. Therefore, titanium was implemented as an adhesion layer, unfortunately, a concern for under etch of the Ti was observed and the piranha time was advised to be from seconds to 1 minute. This relied on the etch rate of 240 nm/min of Ti in piranha, where an exposed titanium adhesion layer of 10 nm would be etched in 2.5 seconds.

Wafer	Bottom electrode	Piranha time	Procedure	Notes for progress
TH1-A	Cr/Au	10 min	NOT stirred, one half of wafer etched more	Stir to avoid layer separation
TH1-B	Ti/Au	5 min	Stirred prior to submerging	Concerns for etching Ti and thereby under-etching Au, immerse for 10 s-1 min
RC190+190	Ti/Au	30 s	Stirred prior to submerging	
RC190+190 with ribbons	Ti/Au	5 min	Etch rate test on actual device wafer	Increase to 5 min, only 1 µm underetch of Ti
RC512+512	Ti/Au	5 min	Stirred prior to submerging	

is covered by gold and only the edges are exposed, yet this could cause the etch to accelerate due to capillary forces which is why caution with prolonged submersion is exercised. The piranha mixture specified in the paper [80] consists of 50 parts 96% H_2SO_4:1 parts 30% H_2O_2 and heated on a hot plate to 120 °C, however, the piranha in this process flow is not heated on a hot plate. Therefore, etch rate experiments were performed on blank metal wafers to determine etch rate for titanium and gold in piranha mixed in a ratio of 4:1 of H_2SO_4 and H_2O_2 self-heating to 80 °C. A blank wafer was deposited with 50 nm titanium and submerged and the titanium was etched in 20 s, giving an etch rate of 150 nm/min.

Likewise, 50 nm gold was evaporated onto the blank wafer without an adhesion layer to prevent any interference from other metals. However, this approach only led to partial delamination of the gold layer. In order to ensure that the gold remains firmly bonded and to accurately observe the etch rate, it is recommended to include a chromium adhesion layer. The addition of a chromium adhesion layer will prevent delamination of the gold and provide a more reliable substrate for the experiment, since Cr is slowly etched in piranha (16 nm/min) compared to Ti, allowing for a true measurement of the etch rate.

The author tested structured RC190+190 wafers with ribbons, see Table 4.2 with complete bottom electrodes of the design, see Fig. 4.10. Microscopy images and width measurements of the bottom electrodes before and after piranha are seen in Fig. 4.10 which show that the gold is not etched and that 1 µm of the titanium is under etched after 5 min and is still usable for CMUT arrays and could result in stronger bonds.

After the etch rate experiment illustrated in Fig. 4.10, which showed that the structured bottom electrodes of the 10 nm Ti adhesion layer and 234 nm Au could endure a 5 min piranha clean, this was tested on the next generation. For the RC512+512 batch, the effect on bonding success between with and without piranha cleaning for 5 min of the bottom electrodes is seen in Fig. 4.11. Without piranha cleaning the bottom wafer there is a major void covering 1/3 of the wafer and is discarded, see Fig. 4.11 a). With a 5 min piranha clean of the bottom wafer, a near-perfect bond is obtained with only minor voids at the periphery, see Fig. 4.11 b). Henceforth, a 5 min piranha cleaning of the bottom electrode with a titanium adhesion and gold electrode stack should be performed immediately before bonding.

The number of particles at the bonding surfaces of the top and bottom wafer before bonding is crucial to minimize to achieve a successful uniformly sealed bond in

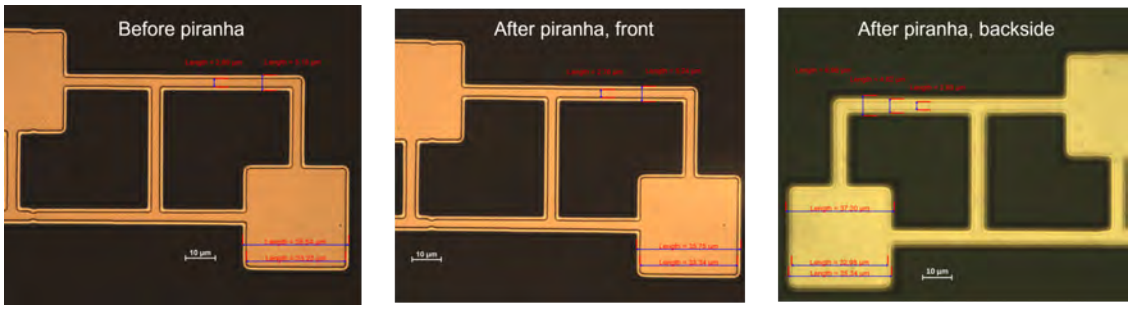
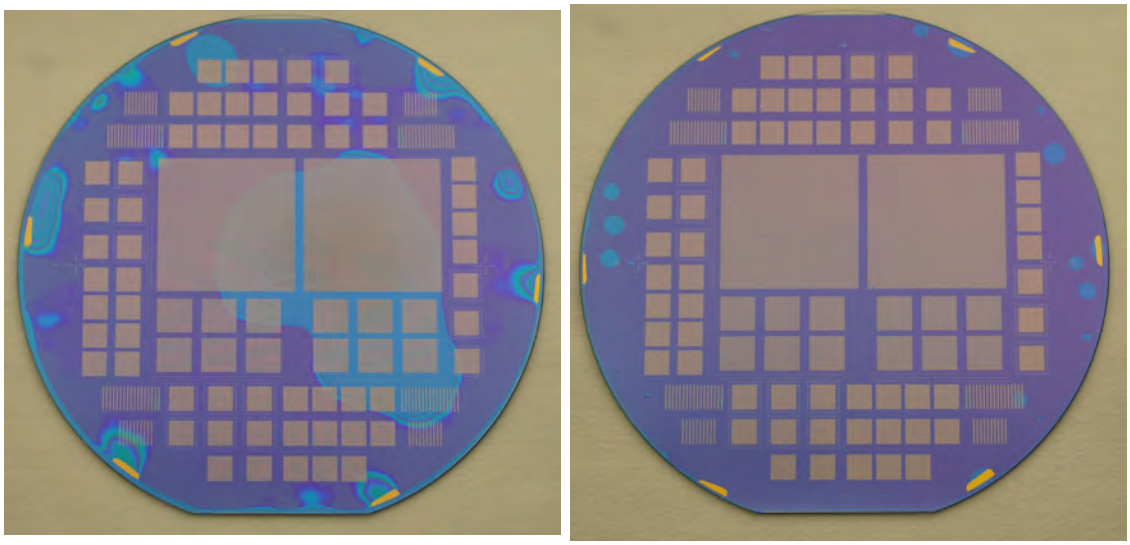


Figure 4.10: Prior and post 5 min piranha clean microscope images of the front and backside of the bottom electrode of Ti/Au. The Ti adhesion layer is under etched by 1 µm acceptable for this process, hence a 5 min piranha clean is possible and could improve bonding.



(a) **(b)**

Figure 4.11: a) With and b) without piranha cleaning prior to bonding for the RC512+512 batch. Without piranha cleaning the bottom wafer, a major void in the center of the wafer ultimately stops the wafer from being realized. With a 5 min piranha clean there are just smaller voids at the edge of the wafer and none over the arrays, a successful bond.

order to finalize the CMUT arrays. Nonetheless, the number of particles on the wafer varies sporadically and depends on the user, the processes, the conditions in the cleanroom and the machines as well as other users. This led to a larger particle study, see section Section 4.2.5. Here a particle scanner from KLA-Tencor *Surfscan 6420* was used, which unfortunately does not allow scans of structured nor non-reflective wafers which is why the bottom wafer could not be inspected.

4.2.5 Particle study, cleaning procedure

As a result of varying bonding success, preventing the realization of the CMUT.A comprehensive particle study was undertaken during the process optimization with meticulous inspection in the pursuit of obtaining full void-free wafer-scale bonding. Generally, the amount of particle contamination is proportional to the number of fabrication and handling steps, thus with an extensive process flow such as this, steps to minimize this is imperative. All particle scans were performed with the KLA surfscan wafer scanner. An overview of the particle contamination study is seen in Table 4.3. P1 is the first piranha clean of 10 min mixed in a 4:1 ratio, followed by a 10 min BOE and finally P2 the second piranha clean of 10 min mixed in a 3:1 ratio. The findings of the particle study found that a cleaning of the PSOI wafers after CMP should be performed in our own beakers and that RCA prior to wafer bonding should only use the RCA1 mixture without an HF dip. Most importantly, the beakers for mixing RCA and the heating baths of the RCA wet bench should be flushed two times prior to cleaning. The furnaces used to form the oxynitride layer were subsequently tested and only the LPCVD nitride furnace contaminates the wafers. Clean Si, that is clean silicon wafers taken directly from the wafer stock contain the smallest and least amount of particles. The presence of silica grains in the polishing slurry makes CMP a naturally unclean process, necessitating thorough cleaning to enable successful fusion bonding. A step-by-step cleaning procedure involving a 10-minute piranha clean, followed by a 5-minute buffered hydrofluoric acid (BHF) clean, and another 10-minute piranha clean effectively eliminates particles, as confirmed by particle scan tests conducted before and after the cleaning process.

Table 4.3: Particle study overview.

Particle Study	Particle Count	Particle Size Range	Notes
P1/BHF bath/P2	3000-6000	300 nm to 8 µm	Old BHF bath - use own beaker with BOE
P1/BOE	711	300 nm to 3 µm	Pre P2
P1/BOE/P2	114	300 nm to 3 µm	Post P2, use own beaker to reduce particle count
Clean Si pre RCA no water flush	2	100 nm - 1.2 µm	
Clean Si post RCA no water flush	4293	100 nm - 1.2 µm	Regular RCA smeared wafer in 100-200 nm sized particles
PSOI cleaned in P1/BOE/P2 pre RCA no water flush	76	300 nm to 3 µm	
PSOI cleaned in P1/BOE/P2 post RCA no water flush	261	300 nm to 3 µm	
Clean Si post C1 Oxide furnace DRY1000	1	300 nm to 3 µm	Not contaminated by C1 furnace
Clean Si post C1 Oxide furnace DRY1000	10	100 nm - 1.2 µm	Not contaminated by C1 furnace
Clean Si post LPCVD Nitride furnace	77	300 nm to 3 µm	Particle contamination by LPCVD furnace, ¡ 500 particles is OK for QC in Nanolab
Clean Si post LPCVD Nitride furnace	354	100 nm - 1.2 µm	Particle contamination by LPCVD furnace, ¡ 500 particles is OK for QC in Nanolab
Clean Si post C1 Oxide furnace WET1100	6	300 nm to 3 µm	Not contaminated by C1 furnace
Clean Si post C1 Oxide furnace WET1100	4	100 nm - 1.2 µm	Not contaminated by C1 furnace
Post CMP cleaner on oxide wafer	6	300 nm to 3 µm	7 oxidized wafers tested with CMP cleaner 4IN recipe
Post CMP cleaner on PSOI wafer	2597	300 nm to 3 µm	2 wafers were tested with CMP cleaner 4IN recipe, PSOI is not cleaned
Post CMP cleaner on PSOI wafer	113	300 nm to 3 µm	2 wafers were tested with CMP cleaner MEMSCLEAN recipe
Post CMP cleaner on PSOI wafer	16	4 µm to 8 µm	2 wafers were tested with CMP cleaner MEMSCLEAN recipe
Clean Si pre RCA1 with water flush	2	100 nm - 1.2 µm	
Clean Si post RCA1 with water flush	800	100 nm - 1.2 µm	800 particles post RCA1 no HF dip, BUT they are ¡ 300 nm, ok for anodic bonding
Clean Si pre RCA1+RCA2 with water flush	2	100 nm - 1.2 µm	
Clean Si post RCA1+RCA2 with water flush	4626	100 nm - 1.2 µm	Full RCA significantly increase particle count, BUT they are ¡ 300 nm

4.3 Bonded wafer stack

4.3.1 Anodic bonding

Anodic bonding is performed with the Süss Microtec Substrate Bonder SB6 Gen2. The wafer stack is anodically bonded at 350 °C in a vacuum chamber pressure of 5×10^{-3} mbar under a tool force of 1000 mbar. With a three-step voltage ramps of −150 V, −300 V, and −600 V applied until the current is 10 % of the initial value. A thorough description of anodic bonding and pre-treatments is presented in a lecture note in Section B.1 written by the author in equal collaboration with my colleague Rune S. Grass. The requirement that has posed the greatest challenges in wafer bonding, generally, is the achievement of particle-free bonding [81]. Interface voids resulting from particles can be prevented by employing thorough cleaning techniques and utilizing a high-standard cleanroom, ideally, class 10 or better [58]. A 1 µm particle can cause a millimeter-sized void at the bonding interface.Unfortunately, the particle scanner was repaired in the USA and was out of use for 11 months within the second year of this 3-year Ph.D. project.

4.3.1.1 Aluminum as bottom electrode metal

Different metals and etching techniques were tested for the bottom electrodes in the anodic bonding process. Among these were aluminum, Al, which has a low resistivity of 2.7 µΩcm and could be etched with the chemical PES [77], preferred for the possibility of batch etching at room temperature with resist masks. During anodic bonding of the structured aluminum bottom electrodes a dendrite pattern appeared, at first observed as holes emerging in the metal after bonding, see Fig. 4.12. A study of the correlation between the hole formation and voltage in the anodic bonding process was tested by the author. It was found that the number of holes forming fractals or dendrite structures increased with increasing the applied voltage in the anodic bonding, see Fig. 4.12. For a bias of 200 V, a few fractals are observed. Whereas for 600 V the holes evolve into fractal patterns and the edges of the metal are frayed.
From the literature, two phenomena are known for anodically bonding Pyrex/Al/silicon. First, is the fractal formation in the aluminum [82, 83] and second, is the dendritic growth at the aluminum glass interface [84].
Fractals are formed by the diffusion of Si atoms into the aluminum film and above 300 °C the following reaction between SiO_2 and Al is possible: $4\,Al + 3\,SiO_2 \longrightarrow 2\,Al_2O_3 + 3\,Si$ [82]. It is hypothesized that this reaction also occurs with the SiO_2 in the glass since there is no direct physical contact between the silicon and the aluminum in the cavities of the CMUT. Fractals increase in size with increasing bonding temperature from 300-375 °C [83]. The dendritic growth occurs at the Al-glass interface in the sodium (Na^+) depleted region as Al diffuses into the glass substrate creating this nanostructure. The diffusion rate of Al into the glass is field-assisted and the dendritic growth was shown for aluminum films ranging from 40-230 nm at 350 °C at 400 V reaching 600-650 nm into the Pyrex [84].
A diffusion barrier layer of titanium was tested and samples without electric fields were also tested, an overview of the study can be seen in the table in Section B.2. From the study, it can be concluded that no fractals occurred without bias annealing for 30 min at 350 °C independent of the presence of a Ti diffusion layer. First a 10 nm titanium layer was tested at 350 °C biased with −600 V, and hole formation and the beginning of fractal formation was observed, despite the titanium diffusion layer.

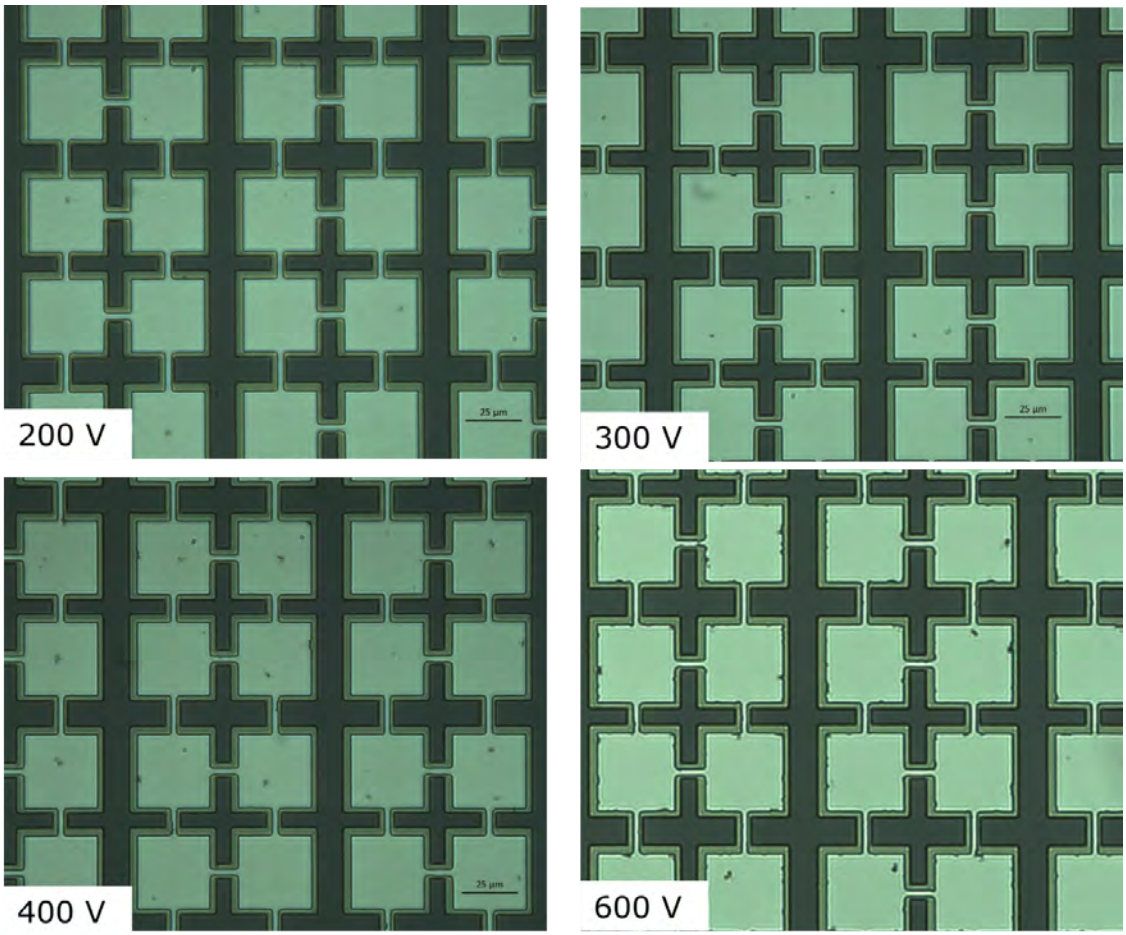


Figure 4.12: Anodic bonding of a borosilicate substrate, with cavities embedded with aluminum, to a silicon wafer. The wafer stack has been anodically bonded at 350 °C in four voltage ramps of 200, 300, 400 and 600 V and inspected in an optical microscope after each voltage step. From the microscopy images, it is clear that the amount of fractals or holes increases with bias voltage. Furthermore, frayed edges of the aluminum are observed at 600 V.

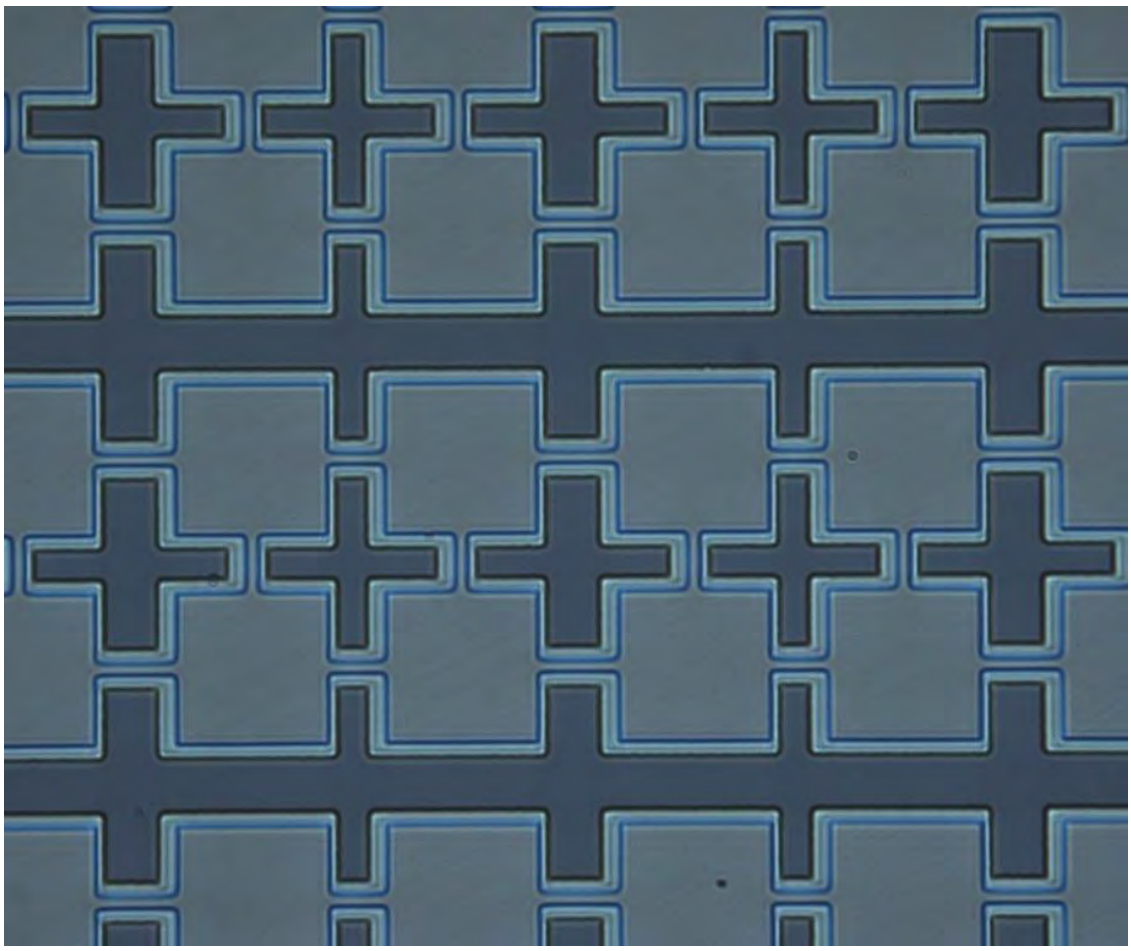
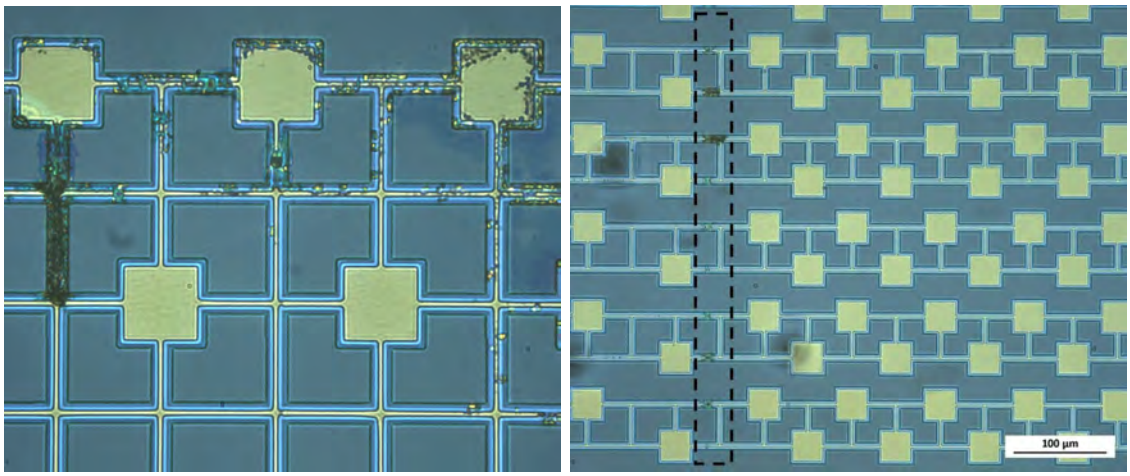


Figure 4.13: Backside microscope image of borosilicate substrate with CMUT cavities etched out and bottom electrodes defined with 30 nm titanium adhesion layer under 250 nm aluminum anodically bonded at 350 °C polarized with 600 V to a silicon wafer without fractal formation. Indicating that a 30 nm titanium diffusion barrier prevents the fractal formation.

Secondly, the thickness of the titanium diffusion layer was increased to 30 nm with the same bonding conditions and for these wafers, no hole nor fractal formation was observed, see Fig. 4.13. This indicates that a 30 nm titanium diffusion barrier prevents the fractal formation observed in Fig. 4.12 for 250 nm aluminum bottom electrodes even at 600 V. These results suggest that aluminum with at least 30 nm titanium layer could be a viable bottom electrode. However, at the time of the experiments, the knowledge of ribbon formation had not been established, as a consequence of this the results were deemed inconclusive and no further studies were made. At the time of writing this thesis, studies have yet to be regarding utilizing aluminum with titanium adhesion as a bottom electrode in anodic bonding.

Bottom electrodes made of chromium, Cr, were also tested with a similar fabrication process and wet etching with chrome etch 18 [70]. Chromium is etched in plasma processes containing oxygen, such as plasma ashing resist and plasma etching silicon, see Table 3.3. The plug-up method utilized in this alignment bonding process uses the aluminum hard mask instead of a resist mask and avoids a resist plasma ashing to protect the Cr bottom electrode in step 9) Table 3.1 making it process compatible. However, as presented in the introduction, see Table 1.2, chromium exhibits higher ωRC values and would result in 57 % signal preservation for an RC1024+1024 element at a thickness of 1 µm, and was disregarded as a bottom electrodes material.



(a) (b)

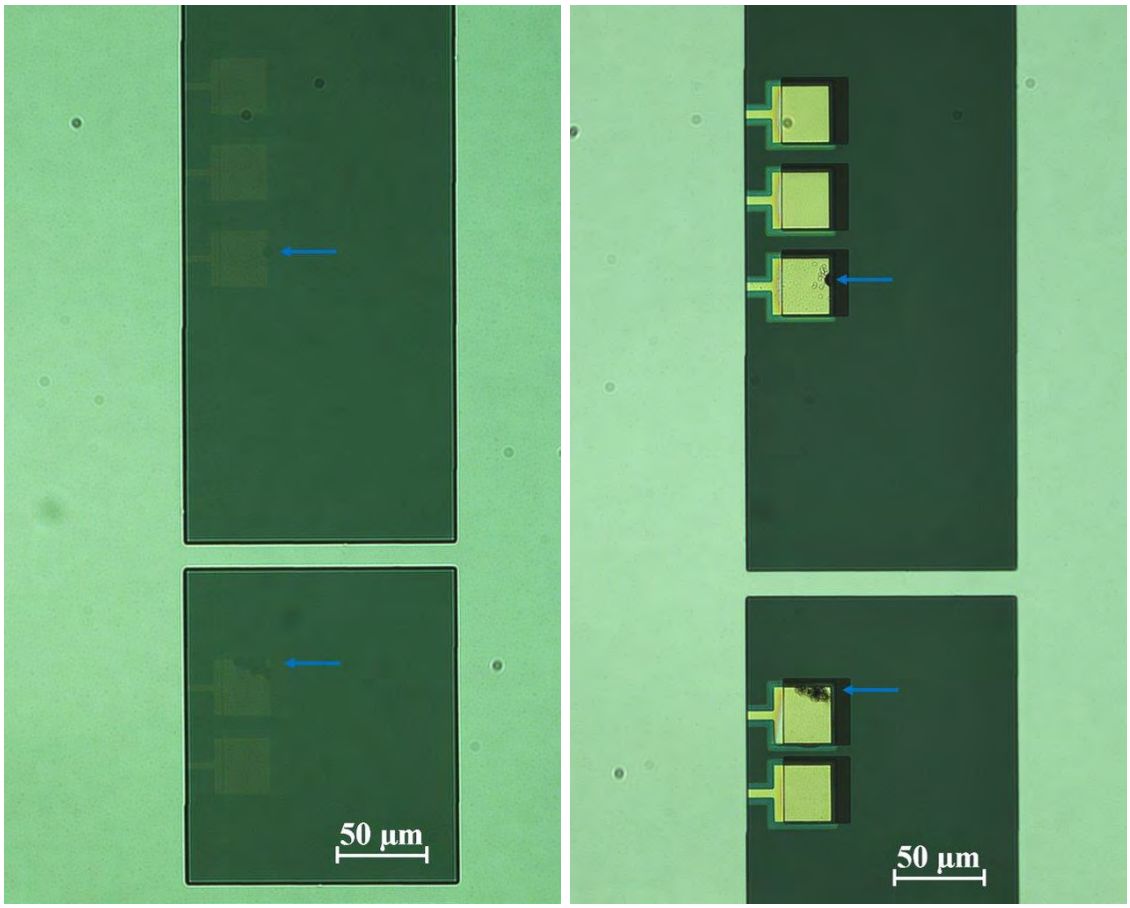
Figure 4.14: Damages to the gold bottom electrodes observed after anodic bonding with a voltage ramp of 150 V, 300 V and 600 V which is the standard procedure. In a) the gold electrode has dispersed widely for all entities of the design, both wires and cells, suggesting lower voltages should be used as it is hypothesized that this effect is caused by too high a current dissipated in the metal. In b) this issue is amplified by the stitching problem (before the dose was increased) where the thin wires gave too high resistance for the dissipated current causing them to burn over. The stitching error is apparent as it all occurs at the same vertical line indicated by the black dashed box.

4.3.1.2 Damages to the metal during anodic bonding

In the preceding RC190+190 batch (TH1_20211122) various damages were identified on the gold bottom electrodes, see Fig. 4.14, during the inspection following anodic bonding using the standard bonding recipe as described in Section 4.3.1. In the images the gold bottom electrodes have been dispersed widely inside the cavities and in some places the wires have been completely severed. It is hypothesized that this phenomenon is a result of too high a current within the metal during anodic bonding. It appears that the high dissipated power caused the gold wire to burn over, suggesting that the bonding voltage should be reduced. This phenomenon is exacerbated by the stitching error, seen in Fig. 4.14 b) where all the wires have burned over in the same vertical line due to inaccurate stitching reducing the width of the wire. These concerns led to a study with possible lower voltage ramps, see subsubsection 4.3.1.5. To circumvent this issue and the reduction in wire width due to the ribbon removal process, as mentioned in Section 4.2.3, the width was increased for the RC512+512 design. The connecting wire width was increased to 8 µm from 3 µm with a preserved 2 µm margin to the glass side walls. This modification was implemented to counter the unfavorable increase in resistance and increase the robustness of the wires during anodic bonding to avoid the damages observed in Fig. 4.14.

4.3.1.3 Damage formation on the contact pads of the bottom electrodes

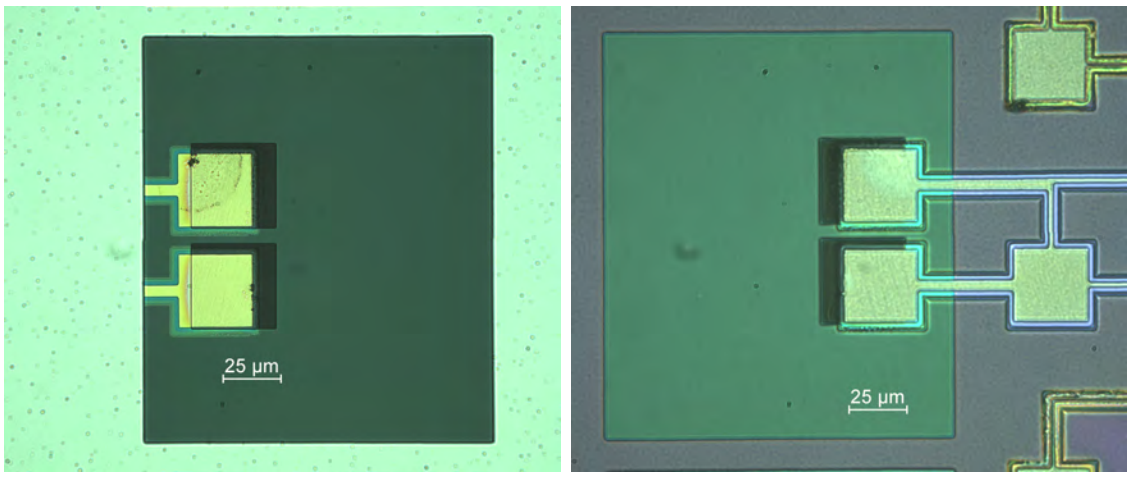
After anodic bonding, damage on the bottom electrodes was observed as described above. Opening up to the bottom electrodes contact pads by etching through the poly-Si revealed more insight into the damages to the metal during anodic bonding. Previously, there was a debate about whether the damage that occurred to the metal came during dry etching with plasma to open up over the contact pads. However,



(a) (b)

Figure 4.15: The first image a) shows the opening in the aluminum layer over the contact pads still covered with the 2.3 µm poly-Si plate, through which the bottom electrodes can be seen vaguely together with a dark spot on the contact pads, marked with the arrows. The second image b) is after dry etching through the poly-Si plate, where the electrode damages are clearly seen on the gold electrodes marked out with the arrows. This same location microscope inspection reveals that the damage to the bottom electrode occur prior to the plasma exposure of the dry etch of the poly-Si top plate as previously expected to cause the damage. The damages are presumably from the anodic bonding as they are observed prior to opening up through the poly-Si plate.

the images in Fig. 4.15 demonstrate that the damages to the contact pads were already present prior to the plasma exposure during the dry etching of the poly-Si plate. In Fig. 4.15 a) prior to the dry etch a dark spot is seen on the contact pads indicated by the arrows through the 2.3 µm poly-Si plate, thus it was not created during the plasma exposure of the dry etch. After opening up over the contact pad by dry etching the poly-Si, see Fig. 4.15 b) the dark spots are clearly seen as damage to the gold electrodes. This finding was only possible due to the implementation of the inspection technique of taking the microscope picture at the same location throughout the fabrication process. Also, this discovery led to an individual inspection of all contact pad openings to document the nature of these damages and if they occurred on all contact pads. A compilation of the variation of electrode damages can be seen in Fig. 4.16 and Fig. 4.17 with the appertaining backside image. The backside images are of equal importance since the entire array can only be inspected from the back once bonded and before top electrode deposition. Inspection of the bottom electrodes from the front is only possible at the contact



(a) **(b)**

Figure 4.16: Front a) and backside b) images after opening up to the contact pads of the bottom electrodes. From the front in a), the electrode damage is clearly seen as a dark particle from where it looks like an explosion has spread in the radial direction. Inverting this, seen in b), looking through the backside of the glass a slightly lighter discoloration of the metal is observed. A minute disturbance of the edge is seen for the lower pad where the particle is located.

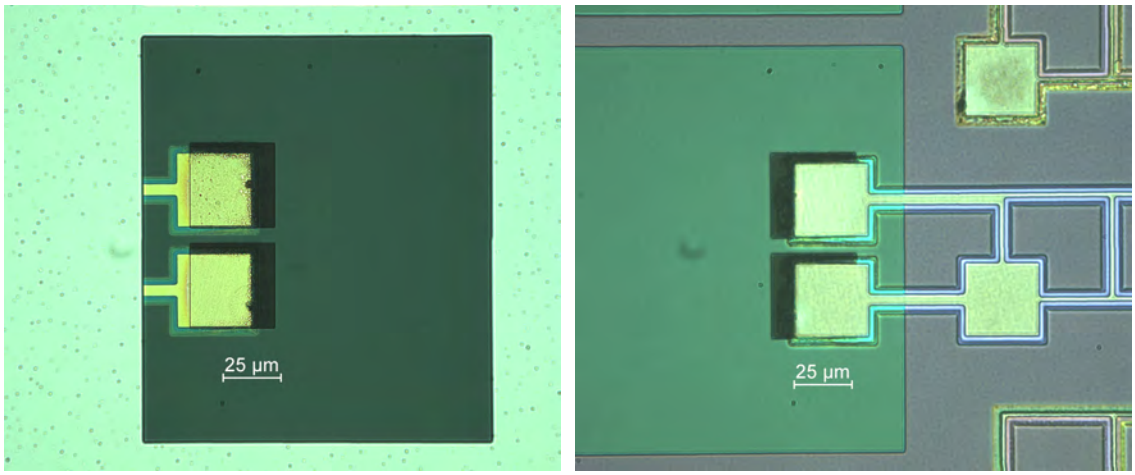
pads, why a comparison of the backside microscopy images was made so that inspection could be performed on the entire array. The electrode damages are extremely difficult to detect from the backside images as seen in Fig. 4.16 and Fig. 4.17. The tendency is a particle or spot that is incinerated in two patterns either what looks like the center-point of an explosion, see Fig. 4.16, or a complete scorching of the entire metal pad as seen in Fig. 4.17. From the backside, this is sometimes seen as a slightly lighter discoloration of the metal and distorted blurred metal or oxynitride, though not explicitly.

The dark spot is surrounded by a lighter aura seen in Fig. 4.16 b) and Fig. 4.17 b) from the backside images and was later in the characterization found to have a direct correlation with top and bottom electrode short circuits. This will be described in detail in section subsubsection 4.3.1.4. By sequentially documenting the individual fabrication steps with microscopy images, like in Fig. 4.15, it could be proven that the damages originated from anodic bonding prior to plasma exposure of the dry etch of the poly-Si top plate. As a consequence of this, combined with the time-consuming task of manually obtaining high-quality microscopy images of the contact pad opening, a high-quality stitching optical microscope was borrowed from NILT a company operating within the DTU Nanolab clean room. This enables backtracking and important reverse engineering of the fabrication process and ultimately pinpointing problems as they occur.

Furthermore, it was observed that the damages to the bottom electrodes predominantly developed at the contact pads, as seen in Fig. 4.18, where the oxynitride layer had been etched away before the alignment bonding.

This observation could indicate that the oxynitride-free area provides a more favorable situation for these damages to occur. However, the damages are also observed where there is oxynitride is present.

The electrode damages gave rise to a number of considerations: 1) reducing the voltage in the anodic bonding processes which were tested in subsubsection 4.3.1.5, 2) increasing the wire width, and 3) ensuring that the thickness, as well as the



(a) **(b)**

Figure 4.17: Front a) and backside b) image after opening up to the contact pads of the bottom electrodes. Here the electrode damage is more comprehensive enclosing scorching of the entire pad, still originating from a particle. From the backside in b), lighter discolorations of the metal, as well as a dark spot at the edge with a lighter aura, and blurred metal edges are observed.

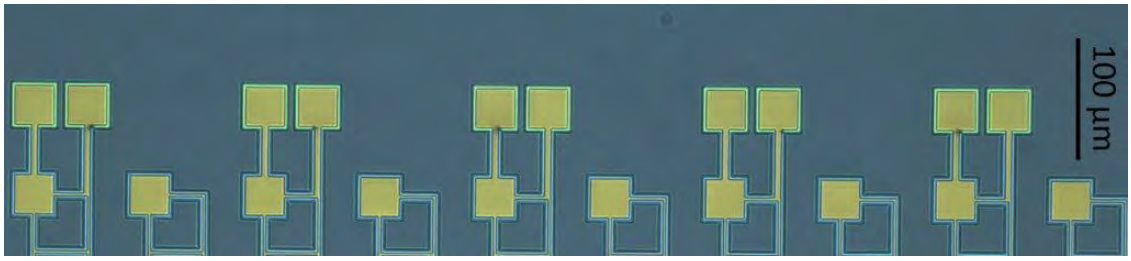


Figure 4.18: Backside microscope image after anodic bonding showing dark spots at all the contact pads at the intersection between the connecting wire and the contact pad where the oxynitride has been removed. This indicates a tendency and might suggest that the oxynitride-free area is more favorable for this defect to occur.

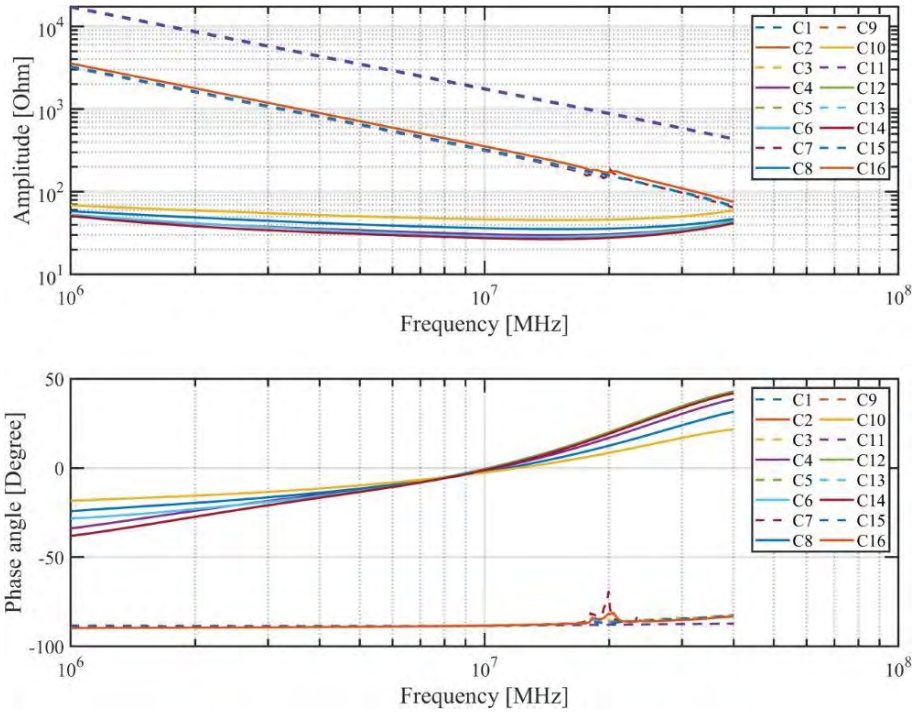
breakdown voltage of the insulation layers, meets the requirement of 160 V during CMUT operation. Consequently, the breakdown voltage of the nitride and the oxide were measured both the oxide and the nitride have a breakdown voltage of 0.9 V/nm indicating a high-quality insulation layer [85].

4.3.1.4 Short circuits between the top and bottom electrodes

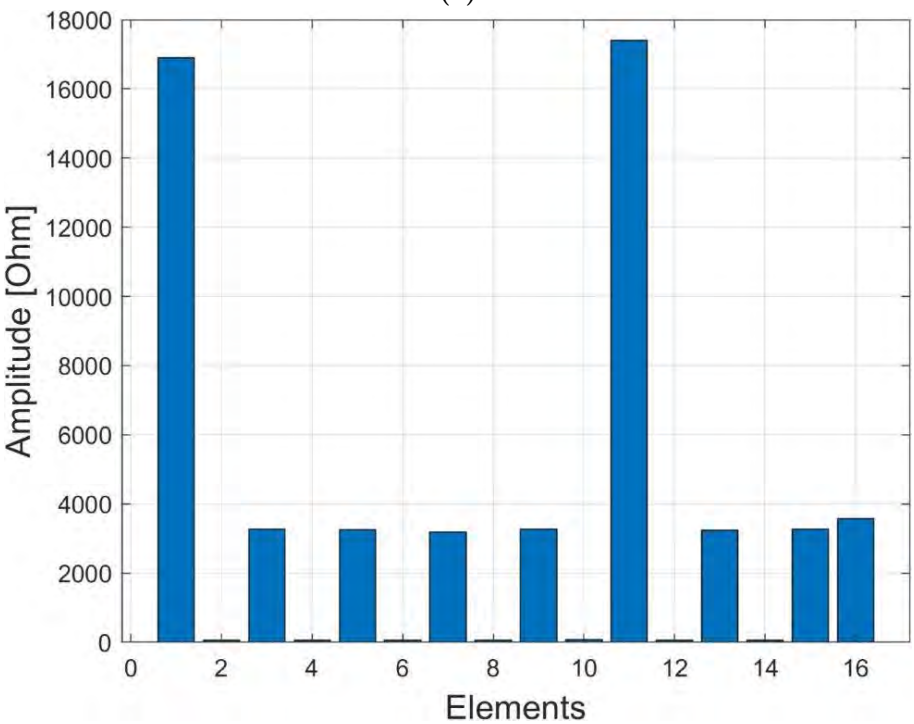
After wire bonding an RC16+16 chip from the TH1_20220322_01 wafer, top-to-bottom electrode impedance measurements were performed. This was performed by connecting all rows together and then measuring the impedance between each of the column elements and the rows. After this measurement, the same procedure was used to characterize each row element. Recently, it was discovered that these showed a direct correlation between a dark spot with a lighter discoloration of the metal seen from the backside to a short circuit between the top and bottom electrodes. The impedance measurement from all the columns can be seen in Fig. 4.19, where a) shows the impedance and phase angle vs frequency and b) a bar plot of the impedance amplitude. By coincidence, it is every other column element except number 16 that is short-circuited. The short-circuited elements exhibit a phase angle different from the ideal $-90°$ and a low impedance amplitude between 160 Ω to 330 Ω seen in b). To examine the nature of this Focused Ion Beam Scanning Electron Microscope (FIB-SEM) was utilized to open holes in the designated CMUT cell, see Fig. 4.20, where the dark spot was localized through backside microscope image coordinates gathered from L-Edit. The FIB-SEM investigation was performed by postdoc Rune S. Grass.

In Fig. 4.21, the cross-section of the CMUT cell is shown, outlined in red in Fig. 4.20 b). This cross-section reveals that the gold, somehow, has moved up through the vacuum gap, reaching the oxynitride layer and creating a direct pathway. In other places, the oxynitride has broken off and lies on the gold bottom electrode and the gold has moved up through the oxynitride into the conducting poly-Si plate connecting the gold bottom electrode to the top electrode consisting of the boron doped poly-Si and 1 µm aluminum. This is the cause of the short circuit. One hypothesis is that the oxynitride is weakened at some points during the anodic bonding enabling this phenomenon of gold bridging the vacuum gap into the poly-Si plate by presumably electrical breakdown of the oxynitride. Reduced voltage and temperature during bonding are possible solutions. Depositing a diffusion-inhibiting layer on top of the gold bottom electrode could also be a solution. An examination of the structural integrity of the insulation layers is to be considered as well.

Furthermore, SEM cross-sectional images of an RC190+190 wafer, from the same batch as the rest of the RC190+190 wafer presented in this thesis, which has not had aluminum deposited, revealed that the gold and poly-silicon react and form what resembles an Au-Si eutectic bond, seen as the porous structure in Fig. 4.22 and Fig. 4.23 between the gold bottom electrode and the oxynitride-poly-Si plate. Comparing the porous structure seen in Fig. 4.22 c) with SEM images from articles of Au-Si eutectic bonds [86–88] also showed in Fig. 4.22 a-b) combined with the FIB-SEM images in Fig. 4.21 it indicates that this is a eutectic bond between Au-Si or Au-Si_3N_4 detrimental to the CMUT. This is a metallurgic reaction, which is temperature driven, hence by reducing the temperature in the anodic bond process this should be remedied as the diffusivity of gold in silicon increases with temperature. The anodic bond is performed at 350 °C, whereas the eutectic point for Au-Si is at 363-370°C, reducing the temperature to 325 °C should be tried to see if successful bonding is



(a)



(b)

Figure 4.19: The impedance measurement for all columns in the RC16+16 array at 1 MHz with a 100 V DC bias. a) displays the impedance and phase angle as functions of frequency, while b) illustrates a bar plot of the impedance amplitude where it is easily observed that all even elements are short-circuited, except no. 16, due to the low impedance 160 Ω to 330 Ω. Equivalently in a), these column elements also have a phase angle that deviates from the expected −90°. All the short-circuited elements had a dark spot surrounded by an aura of discoloration of the bottom electrode.

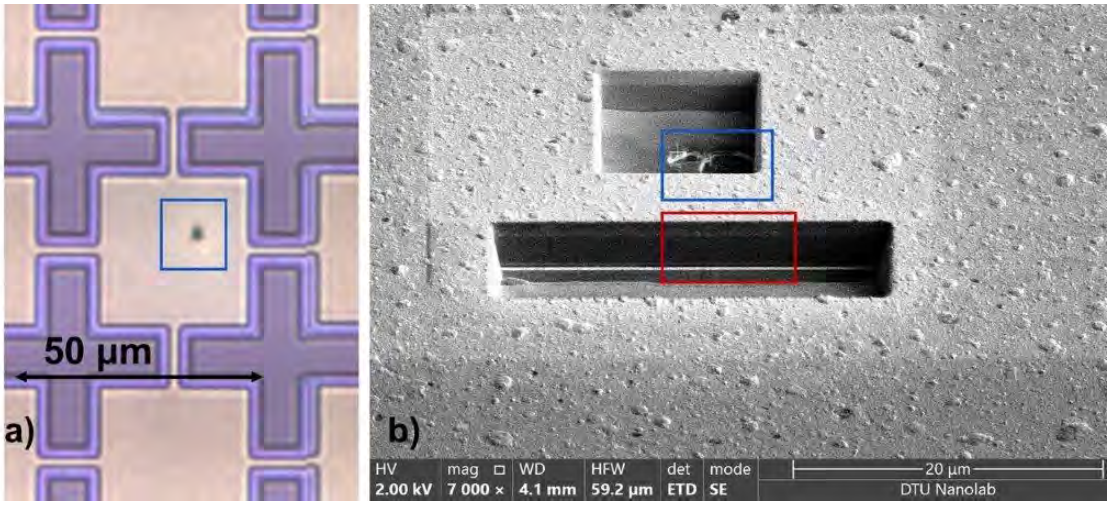


Figure 4.20: Backside microscope image a) showing a dark spot with a lighter aura (marked in the blue box) in the bottom electrode of a short-circuited element in the RC16+16 array. The coordinates of this defect's location were found through L-edit and used to localize the spot for FIB-SEM characterization. In b) a SEM image from the FIB-SEM investigation the corresponding blue box is the front side of the same location where FIB-SEM has been utilized to examine the defect from the top, seen by two unexpected holes in the top plate. Also, a cross-sectional cut was performed with the FIB-SEM to investigate the vacuum gap and the red box marks the section which is depicted in Fig. 4.21 further into the cell.

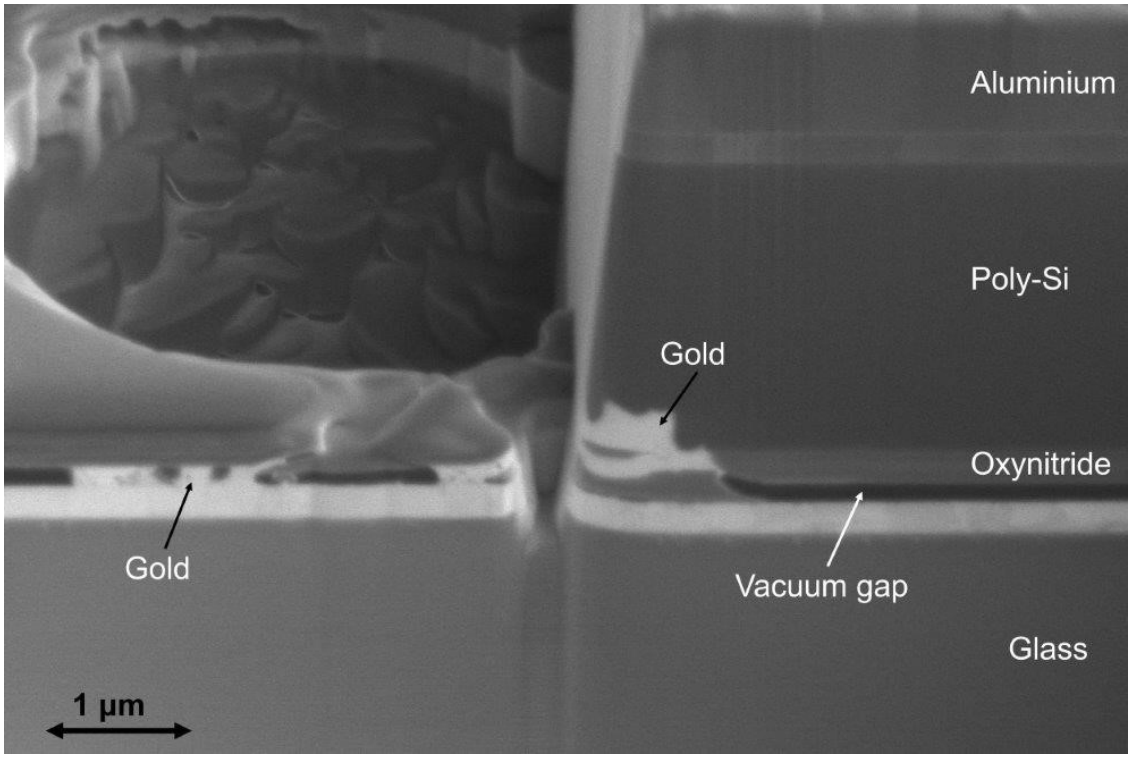


Figure 4.21: FIB-SEM cross-section, of the area marked in red in Fig. 4.20 b), of an anodically bonded RC CMUT cell. This shows that the gold bottom electrode has migrated up through the vacuum gap connecting to the oxynitride. To the right, the oxynitride has broken off and lies on top of the gold electrode and the gold has migrated all the way up to the poly-Si plate creating a direct short circuit between the top and bottom of the CMUT cell. This porous structure of the gold combined with the emergence into the poly-Si indicates Au-Si eutectic bonding.

possible.
This phenomenon is believed to be caused by the presence of gold particles within the vacuum gap, enabling the gold to penetrate the top plate thereby being the root source of the short circuits. To support this hypothesis, another SEM image of the same wafer as in Fig. 4.23 is captured with a focus on the vacuum gap where three protrusions on the gold electrode are seen in Fig. 4.24 seen below the white arrows and these are assumed to be gold particles from the evaporation and likely be precursors of the short circuit which were not large enough to form a short circuit. Connecting these observations with the ones in Section 4.2.2, it indicates that the remaining major challenge is these gold particles forming short circuits between the top and bottom that ultimately prevent the fabrication of a fully-functioning anodic bonded RC array. Whether or not it is possible to obtain a completely flat uniform metal surface for the bottom electrodes will be the determining factor if anodic bonding is the fabrication technique that can achieve a 15 MHz $\lambda/2$-pitch RC1024+1024 CMUT array.

4.3.1.5 Reduced voltage during anodic bonding

The standard recipe for anodic bonding has three increasing voltage steps of 150 V, 300 V and 600 V. As a result of the electrode damages after anodic bonding on the contact pads in subsubsection 4.3.1.3 and the wire burnout presented in subsubsection 4.3.1.2 a study with lower bonding voltages with three recipes of a maximum of 300 V, 400 V and 500 V was devised and prepared. The study was performed by MS.c student Sebastian Stangegaard on anodically bonded linear arrays and supervised by the author. The results are presented in Table 4.4.
It was observed that all the shorted elements had a dark spot on the bottom electrode during the electrical characterization of wafer 06, see Fig. 4.25. The remaining wafers still need to be finalized inside the cleanroom. The study showed that reducing the maximum voltage used in anodic bonding resulted in fewer dark spots. Specifically, reducing the voltage from 600 V to 400 V reduced the occurrence of dark spots from 1 in 10 elements to 1 in 25 elements. Moreover, extending the piranha clean time before bonding to 5 minutes, instead of the usual 10 seconds, further reduced the number of dark spots by half. With a 5-minute piranha clean and a voltage of 400 V, only 1 dark spot was observed in 55 elements. The remaining wafers need to be finalized and electrically characterized. However, the visual backside microscope inspection and electrical characterization, also based on Section 4.2.2 and subsubsection 4.3.1.4, strongly indicates that decreasing the anodic bonding voltage to 400 V and the piranha cleaning time of the bottom wafer to 5 min should decrease the dark spots responsible for the short circuits between the top and bottom electrodes. Potentially anodic bonding voltage as low as 300 V could be used, as the wafer bonded at 300 V was not piranha cleaned and resulted in large voids across the wafer.

4.3.2 Isotropic holes in KOH etch

The preceding RC190+190 batch (TH1_20211122) was damaged in the long KOH etch of the handle layer as the plate was ripped off before the etch time as calculated by the etch rate. Consequently, the 3-hour KOH etch of the current RC190+190 wafers was unceasingly observed by lifting the wafers every 5th minute as the bubbles forming during the etching process prevent direct visual inspection of the wafers. After 1 h, a peculiar pattern of isotropic super fast etching holes began to emerge.

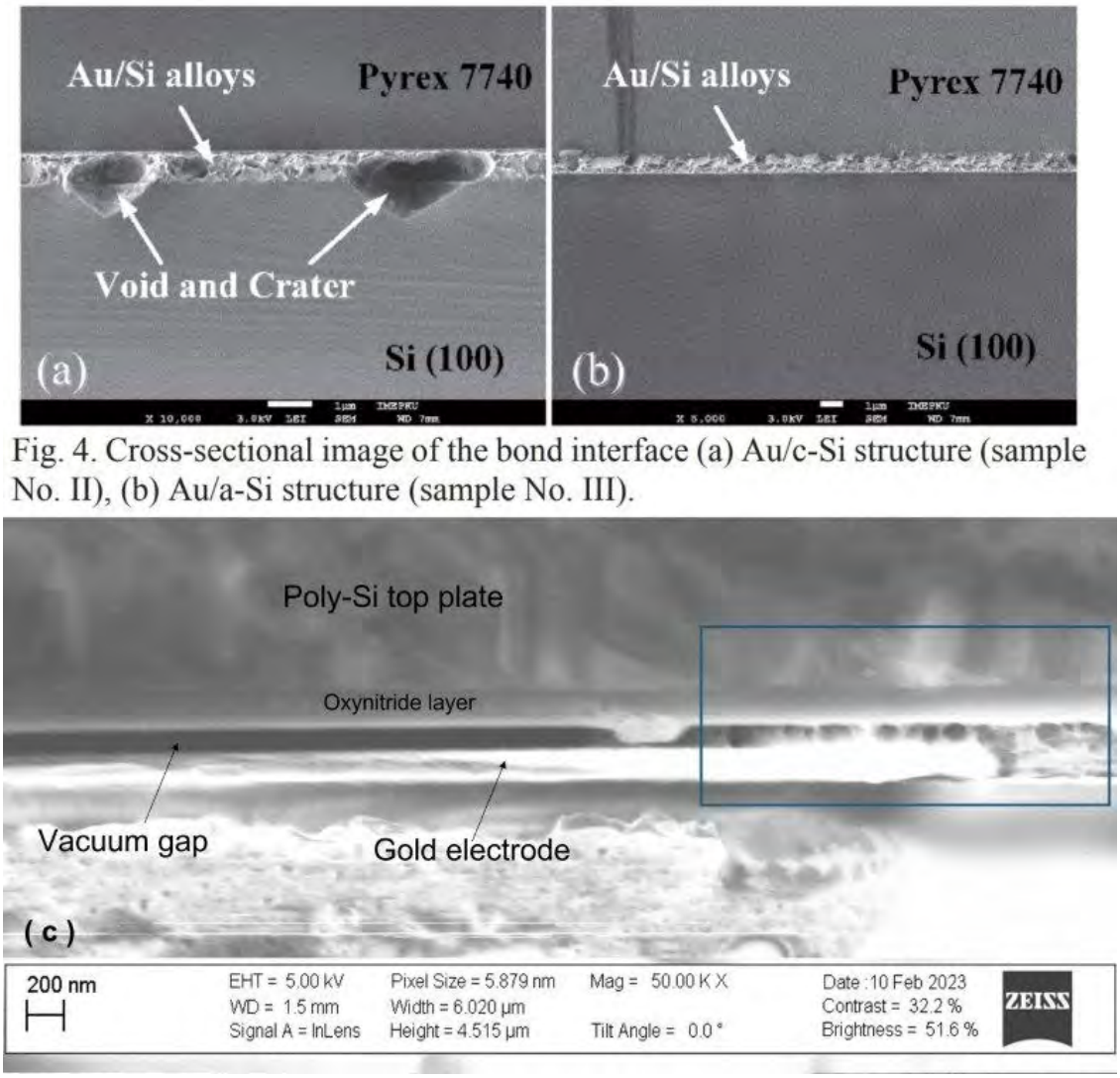


Figure 4.22: a) and b) are SEM images of eutectic bonding of Pyrex/gold/silicon from [86] inserted for comparison. In c) a SEM image of the cross-section of a CMUT cell where a porous structure formation marked in the blue box between the gold bottom electrode and the plate is observed. This structure resembles that of the eutectic bonding observed in a) and b). The SEM image was captured by MS.c student Peter Dalsgaard working as a student helper in the MEMS-group. The porous structure below the cell and bottom electrode is currently not understood and it was observed to be shrinking during SEM imaging.

Table 4.4: Results from lower maximum voltage during anodic bonding and piranha treatments correlation with dark spots per elements which were found to be short circuits between top and bottom electrodes. Only wafer 06 is finalized and electrical characterization of these anodically bonded linear 384 elements arrays showed that all short circuits had dark spots. These experiments were performed by MS.c student Sebastian Stangegaard and supervised by the author.

Wafer	Max. anodic bonding voltage	Piranha	Dark spots per elements
02	600 V	10 s	1/10
05	600 V		1/10
03	500 V		1/10
06	300 V, then re-bonded to 400 V		1/25
07	400 V	5 min	1/55

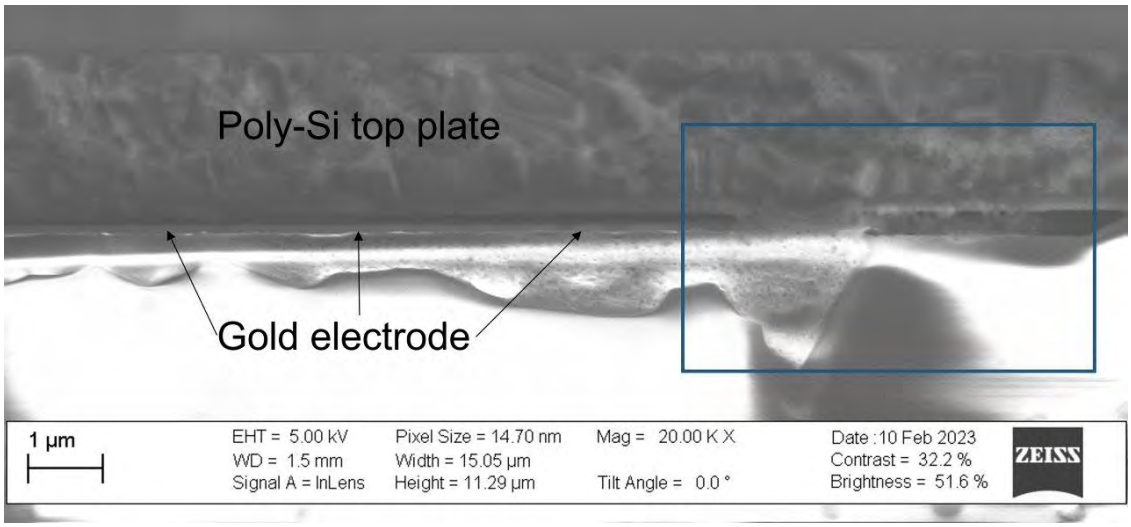


Figure 4.23: Cross-section of a CMUT cell taken with an SEM showing a porous structure formation between the gold bottom electrode and the plate is observed and is enclosed by the blue box. The porous structure is seen extending far into the poly-Si and explains the gold observed from the top view in Fig. 4.20 b) during FIB-SEM. This porous structure resembles that observed for eutectic bonding between gold and silicon seen in Fig. 4.22 a) and b) as well as in [88]. This SEM image was taken by MS.c student Peter Dalsgaard.

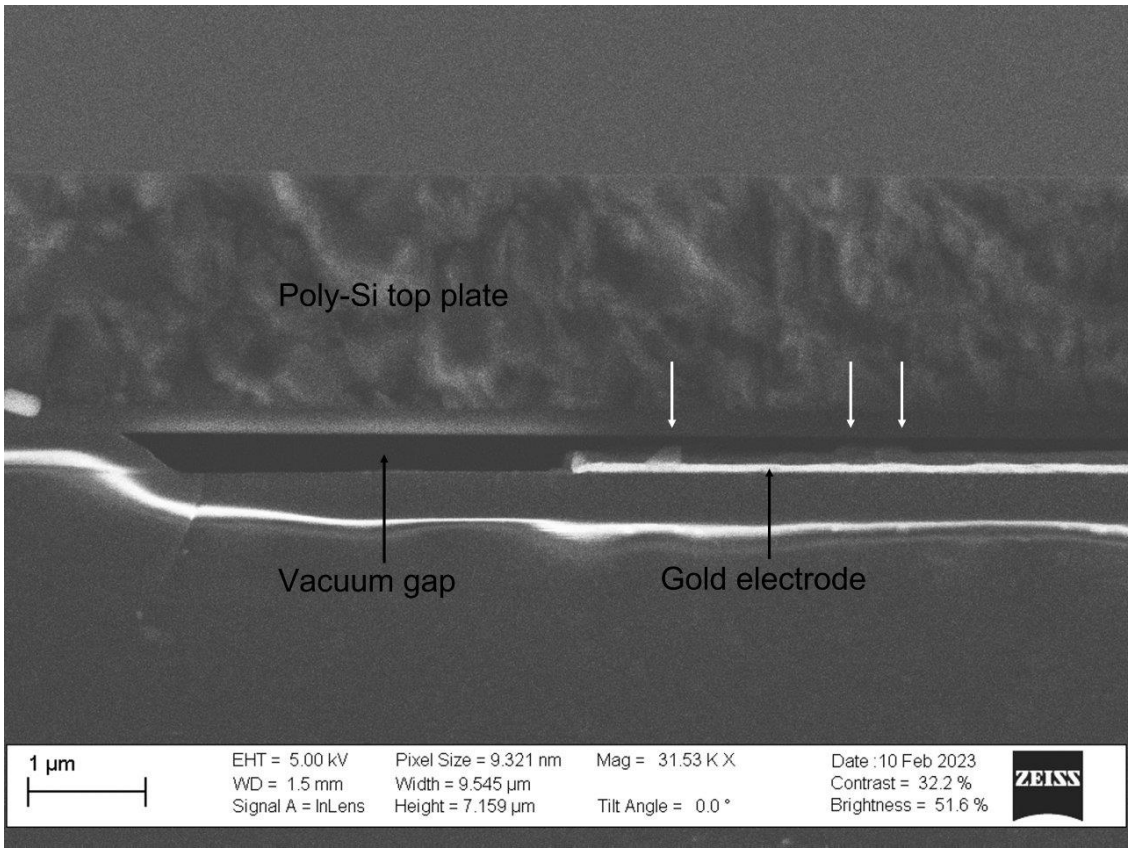


Figure 4.24: Cross section SEM image of the edge of a CMUT cell showing the vacuum gap and the vacuum cavity margin until the gold bottom electrode furthest to the right in the image. On top of the gold bottom electrode, there are three protrusions indicated by the white arrows. The protrusions are believed to be gold particles from the evaporation and precursors to the short circuits observed during FIB-SEM in Fig. 4.21. The SEM images were captured by MS.c student Peter Dalsgaard working as a student helper in the MEMS-group.

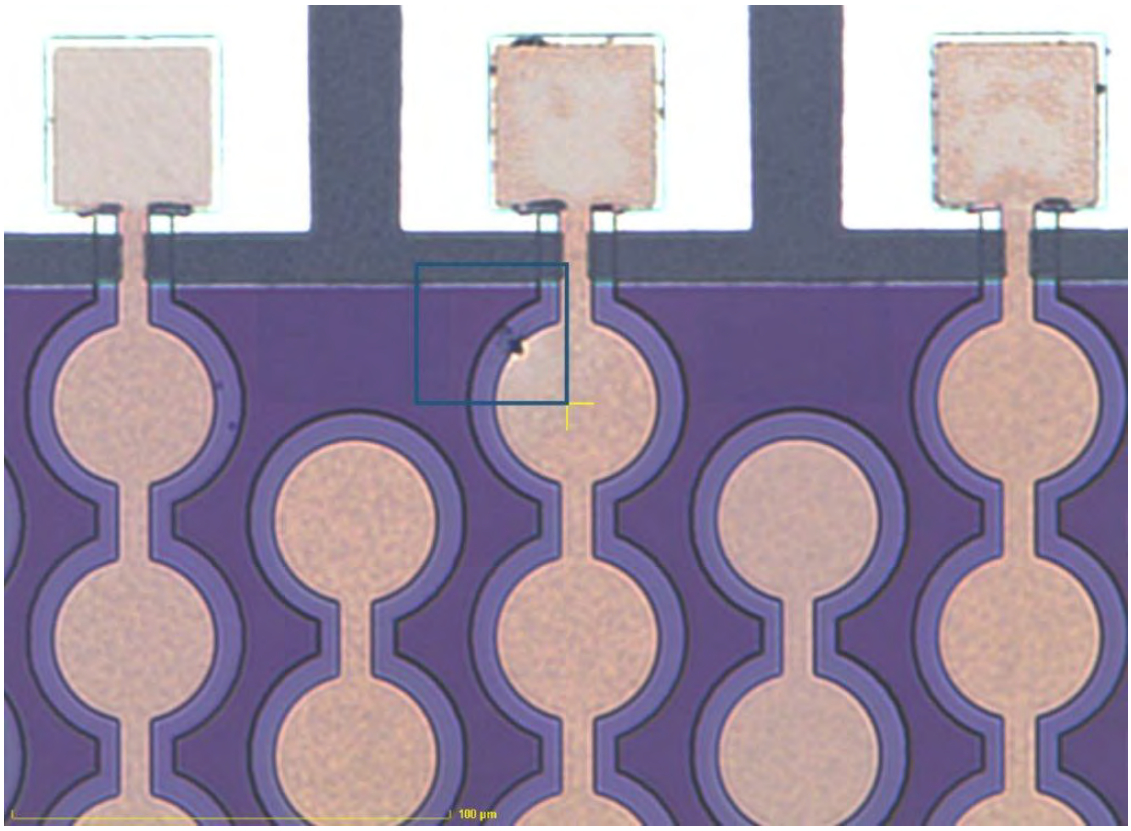


Figure 4.25: Back side image of a short-circuited linear element, no. 339 where a dark spot is surrounded by a discoloration. In this study, it was found that all short-circuited or low capacitance frequency response linear elements had this dark spot with a discoloration aura.

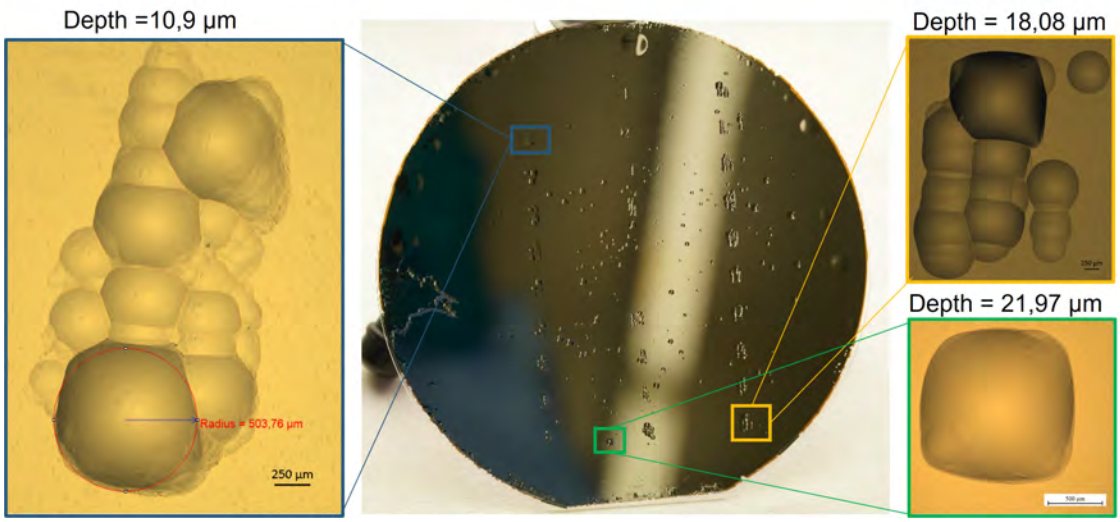


Figure 4.26: Camera picture of the RC190+190 wafer after 3 h KOH etch at 90 °C showing the pattern of isotropic holes. Three microscope images as well as the depth of the deepest part measured with a stylus profilometer are shown in the figure. The isotropic holes have a tendency to form shapes like caterpillars and are accumulated in a three-stripe vertical pattern. After 3 hours the holes are 10 µm to 22 µm deep suggesting an accelerated etch rate of 7%.

Since KOH is an anisotropic silicon etch, these isotropic holes are highly unexpected. In Fig. 4.26 a picture taken after 3 hours, i.e. almost completion of the handle layer etch, shows the isotropic holes pattern along with microscope images and measured depths. The holes were measured with a stylus profilometer and showed depths between 10 µm to 22 µm, which is why they are called super fast etching. For 22 µm in 3 h corresponds to an increased etch rate of 7 %. These super etching holes are what ruined the last batch, see Fig. 4.30 a), since the etch rate is much greater the KOH will reach the BOX layer long before the rest of the layer is etched and penetrate through the poly-Si plate and rip off the plate. Another wafer of the current RC190+190 batch can be seen in Fig. 4.27, where the same wafer is photographed in different lighting to emphasize the faster etch rate of these isotropic holes. The isotropic holes have reached the BOX layer seen as purple spots with a zoom-in from the stylus profilometer measurement showing that a considerable part of the thermal oxide has also been etched enough to see the array beneath. The BOX layer is a thermal oxide and is supposed to function as an etch stop due to the selectivity of oxide being above 1:200 in KOH. Thermal silicon dioxide, SiO_2 has an etch rate of 6 nm/min which for an approximately 500 nm BOX would require 500 nm/ 6 nm/min = 1 h 23 min before the KOH would perforate the entire layer. Yet this accelerated etch rate continues in the oxide as well and ultimately continues through the final poly-Si layer (the top plate) before the remaining BOX is etched as seen in Fig. 4.30 a) as the gold bottom being visible through the isotropic holes while most of the BOX layer remains intact and covers the wafer. This explains why the earlier wafer batches encountered issues where the plate was ripped off prematurely during the KOH process ruining the wafers. This discovery of faster etching isotropic holes was shared with process specialist Rune Kenneth Dybdal Christiansen and laboratory technician Nick Sørensen from DTU Nanolab and in collaboration. A larger study of this was performed and will be described below.

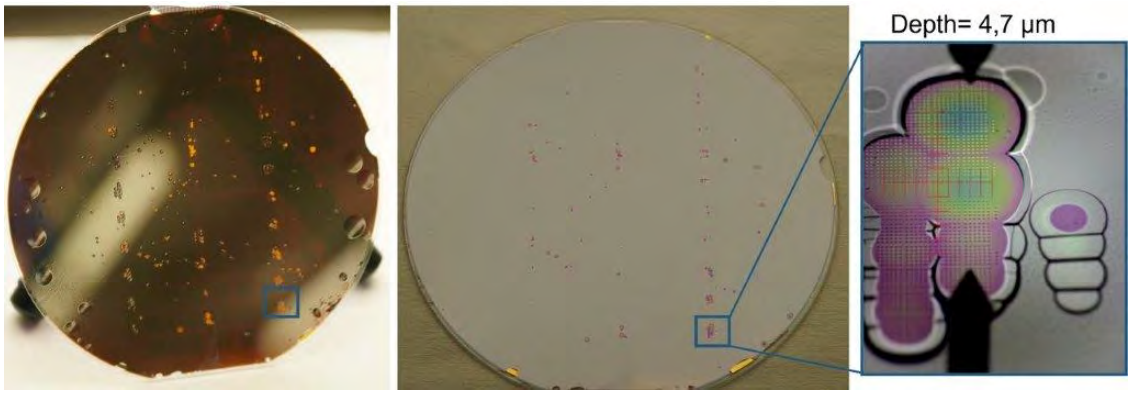


Figure 4.27: Picture of another of the RC190+190 wafers after 3 h KOH etch. The isotropic holes have reached the BOX layer seen as purple spots with a zoom-in showing the array beneath indicating that the etch rate in the oxide is also accelerated. The image furthest to the left is to locate the arrays and see where the hole pattern overlap.

4.3.2.1 Wafer type

From the literature, it was explained that accumulations of point defects in Si(100) caused the faster etching and resulted in filled indentations i.e. isotropic holes [89]. Therefore, several different wafer types from different manufacturers were KOH etched without a clear indication of more suitable or higher-quality wafers as all wafers had sporadically isotropic holes. And to exclude a bad batch, blank silicon wafers from the same batch as the one used for PSOI fabrication were also etched in KOH.

4.3.2.2 KOH mixture

The chemical mixture of the KOH was also tested by DTU Nanolab, there are 3 different wet benches with KOH available named KOH1, KOH2, and KOH3 of which all were tested. KOH3 is the wet etching bench used in the process flow in the thesis. 25 wafers were etched in KOH1 and no isotropic holes were found. 25 new, blank silicon wafers were etched in KOH2 and on 2 wafers there were found 2 isotropic holes on each wafer. Quality control wafers from the last two years were inspected and showed isotropic holes measured with a stylus profilometer to be between 2-5 µm in depth. The holes have a tendency to accumulate in shapes like a caterpillar.

4.3.2.3 Wafer bonder chuck

The peculiar phenomenon was that, contrary to the blank silicon wafers and the unstructured and unbonded PSOIs that were etched the isotropic holes were scattered sporadically across the wafer. Whereas, the wafer-bonded PSOI showed a pattern. Talking to PhD student Jesper Yue Pan about these fast etching holes in KOH after anodic bonding, he had experienced the same problem in 2018 due to the wafer chuck. The fast etching holes pattern is identical to the marks left on the wafer bonder chuck see Fig. 4.28.
To solve this problem a new wafer chuck was implemented and together with Rune Christiansen, and a blank silicon wafer was anodically bonded to a Pyrex wafer. The silicon wafer is the same kind utilized for the PSOI fabrication, SN611. The bonded wafer stack was subsequently KOH etched at 80 °C for 1 hour and showed an increased number of isotropic holes covering the entire silicon wafer surface, see

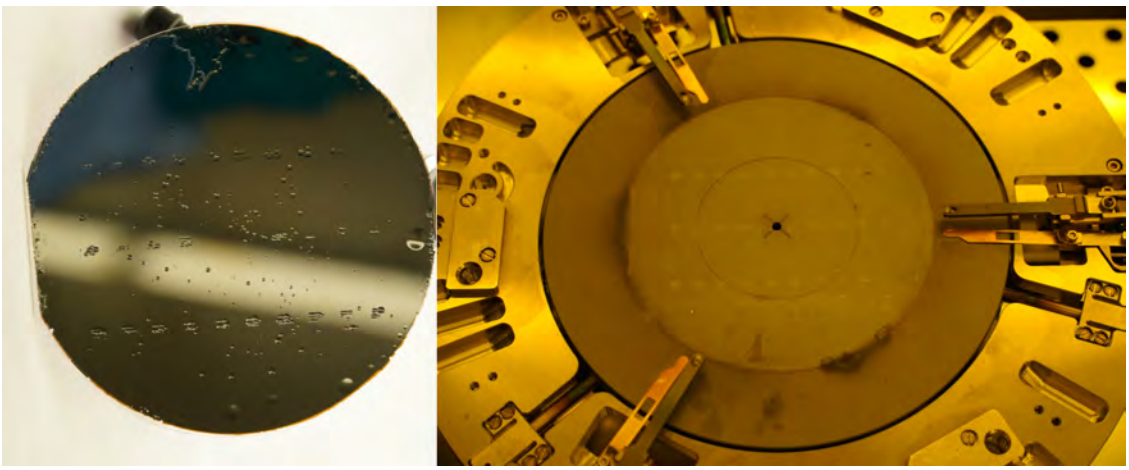


Figure 4.28: On the left the 1 hour KOH etched wafer bonded PSOI handle layer, TH1_20220322_04, with the pattern of isotropic holes. To the right, the wafer bonder chuck where the exact same pattern causing the fast etching isotropic holes in the wafer stack is seen on the chuck. The marks left on the chuck stem from a previous user that ran an 1800 V bond in 2018. The marks are translated from the chuck through the entire PSOI stack that is: 180 nm Oxynitride, 2.3 µm poly-Si, 500 nm BOX, 350 µm silicon handle layer, and 2nd BOX of 500 nm. These fast etching holes are detrimental to the fabrication process of our CMUTs.

Fig. 4.29 a-b). A control wafer stack was also bonded with the old fixture (chuck) and KOH etched, which also showed isotropic holes all over the surface plus in the pattern of the old wafer chuck, see Fig. 4.29 c-d). This experiment was repeated with wafers from a different manufacturer, Topsil GlobalWafers A/S, and showed identical results the old fixture resulted in isotropic holes in the pattern of the chuck, and the new fixture resulted in smaller but more isotropic holes scattered almost uniformly across the wafer as observed for the other silicon wafers. This indicates that the process of anodic bonding increases the number of isotropic holes observed after KOH etching of silicon.

A graphite sheet was tested by DTU Nanolab as a stopping layer for translating the indentations from the wafer bonder into the bonded wafer stack. This seemed like a plausible idea since the author backtracked the wafers anodically bonded throughout this thesis and it seemed not to be an issue prior to the introduction of alignment bonding. Before alignment bonding, regular anodic bonding was done with two dummy wafers used to shield the wafer stack during anodic bonding from the salts that had accumulated on the electrodes. Comparing the previous RC190+190 batch, TH1_2021122, to the current RC190+190 batch, TH1_20220322 seen in Fig. 4.30, it is clear to see the pattern from the wafer chuck through which the KOH reached the bottom electrodes and ruined the preceding batch (TH1_20211122). Anodic bonding using a graphite sheet between the silicon and the wafer chuck showed a decrease in isotropic holes after KOH etching. Alignment bonding with the graphite sheet was made possible by cutting a hole through the graphite sheet for the vacuum suction. Alignment bonding with a graphite sheet was introduced during the RC512+512 processing and resulted in 3-4 isotropic holes per wafer after KOH etching the handle layer. The exact process of how the anodic bonding results in faster etching isotropic holes in the PSOI and silicon wafers is currently not understood.

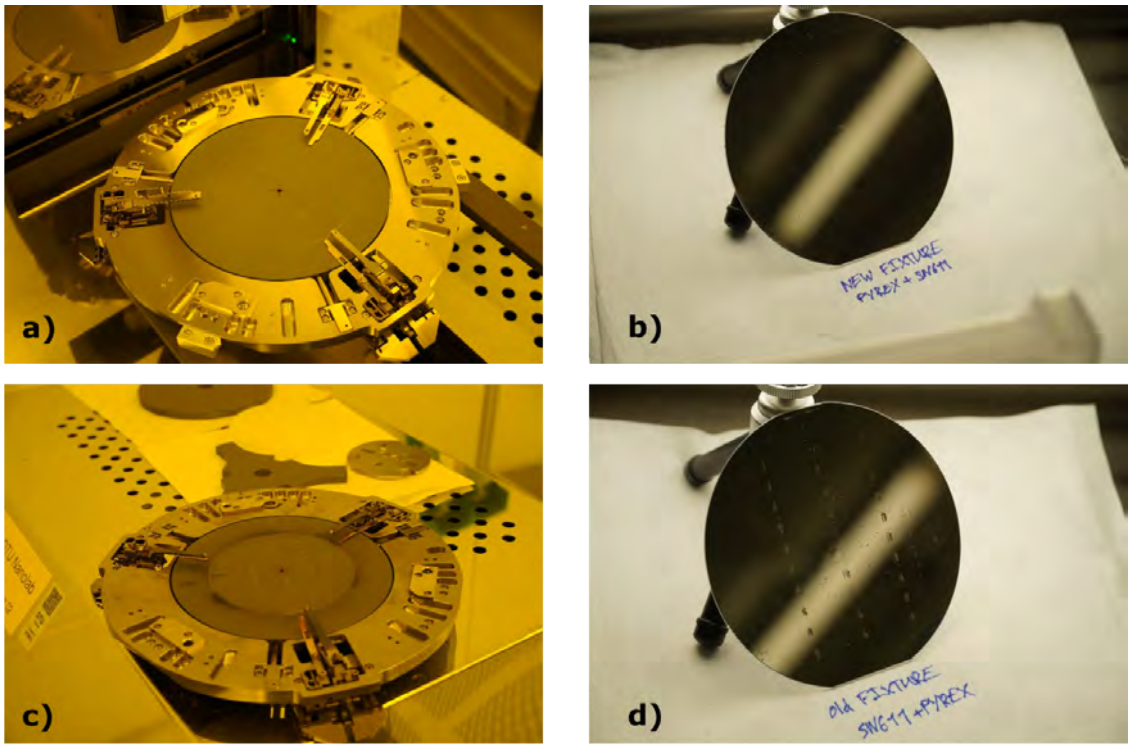
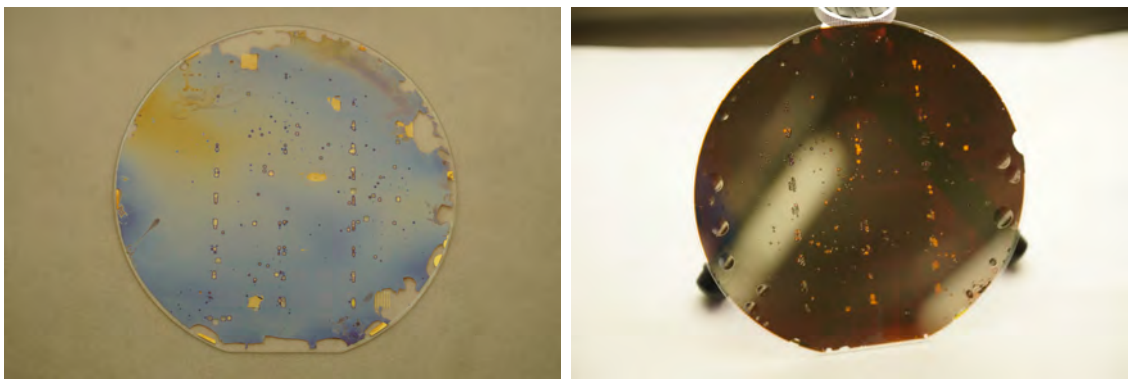


Figure 4.29: New fixture (chuck) for the wafer bonder seen in a) used for the first time to anodically bond a blank silicon SN611 wafer with a blank Pyrex wafer. After 1h of KOH at 80 °C resulted in b) isotropic holes spread uniformly across the surface. The old fixture (chuck) for the wafer bonder c) where the pattern originates from, used to anodically bond a control of a blank silicon wafer to a blank Pyrex wafer. This was also KOH etched at 80 °C for 1 hour and revealed the pattern translated from the chuck into isotropic holes in the silicon. The number of isotropic holes is increased for wafers bonded with the new chuck when comparing wafers bonded with the old chuck, which are of course accumulated in the pattern and slightly larger.



(a) **(b)**

Figure 4.30: Pictures after thinning down the silicon handle layer in KOH. To the left, a), is the preceding RC190+190 batch,(TH1_20211122), before the discovery of the isotropic holes pattern. To the right in b), the current RC190+190 batch, TH1_20220322, where the isotropic hole pattern was discovered to stem from the wafer bonder chuck, and explains the faster etch rate which had ruined the previous batch. In a) the accelerated etch rate continues in the BOX layer as the KOH etch has perforated the BOX + poly-Si layer and the bottom electrodes are seen in the isotropic holes while the majority of the BOX is still intact and covering the wafer, explaining the issues with the previous wafer batches having the plate ripped off in the KOH prematurely.

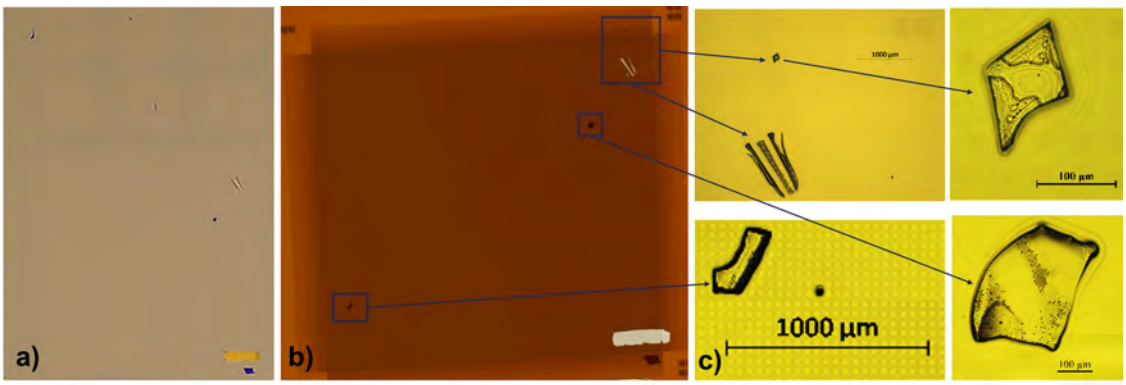


Figure 4.31: The figure displays an overview of an RC190+190 array, where a) is a picture of the top plate showing ruptured plate pieces with the blue-purple oxynitride of the upward-facing top plate, with the downward-facing boron-doped poly-Si creating a conducting path and causing a short circuit between the places it connects. In b), a backlit image of the RC190+190 array is shown, with blue boxes indicating the poly-Si flakes and holes, and a zoomed-in microscope image is displayed in c). The holes resulting from the rupturing top plate will render the elements dysfunctional in the final array, and the poly-Si flakes on top of the array will cause short circuits in the top elements. Keeping in mind that the pitch of the RC190+190 is 95 µm and the RC512+512 is only 51 µm, the same size poly-Si flakes will short circuit twice as many elements in the RC512+512 necessitating a solution to be found.

4.3.3 Voids causing top plate ruptures and flakes

A major challenge that occurs after having bonded the wafers and during the thinning of the PSOI wafer is that anywhere at the bonding interface where the bond strength is weakened due to voids or the structural integrity is compromised the plate is prone to rupturing. The dislodged plate pieces or poly-Si flakes from burst voids are seen in Fig. 4.31. In the figure an overview of a RC190+190 array is shown and Fig. 4.31 a) shows the blue-purple oxynitride of the top plate facing upwards i.e. the conducting boron doped poly-Si is facing downwards creating a conducting path creating a short circuit between top electrodes and in b) a backlit picture of the RC190+190 array with blue boxes marking out the poly-Si flakes and holes with a zoom-in microscope images shown in c). The holes after the rupturing plate will result in non-functional elements for the finalized array and the poly-Si flakes on top of the array will cause short-circuiting of the top electrodes and a solution therefore needs to be found.

At the point of having thinned down the PSOI by wet etching to the poly-Si top plate the alignment marks need to be etched open. The wafer is spin coated, exposed and developed, and an opening over the alignment marks is made by dry etching. During the pump-down process to create a vacuum in the dry etch system's load-lock, any large voids present on the wafer might rupture, resulting in the dispersion of conducting boron-doped poly-Si flakes. Void ruptures that occur when the plate is *not* covered with photoresist could potentially end up shorting neighboring top elements in the array. An attempt was made to remove the flakes that landed on the plate through ultrasonic agitation, to overcome the adhesion caused by Van der Waals forces. However, this was unsuccessful. Furthermore, a 10 min BHF etch was tried since the flakes that landed with the oxynitride facing down could potentially be under-etched and released from the surface as the first 60 nm of the 180 nm oxynitride is a thermal silicon dioxide with an etch rate of 75 nm/min in

BHF, however, only a few flakes were released. Manually mechanically removing the poly-Si flakes in a probe station resulted in the probe needle breaking through the plate. These conducting flakes ended up short-circuiting some elements of the RC190+190 arrays, see Fig. 5.12. Therefore, voids should be minimized and wet etched if possible. The solution that was implemented was to manually open up holes in the photoresist over the voids and etch them simultaneously during the dry etch opening of the alignment marks, which was done for the RC512+512 batch, see Fig. 3.24 a). This allows the rupturing silicon to land on top of the resist which was manually removed, with a combination of remover 1165, IPA and Acetone, to minimize the number of flakes over the large arrays. Furthermore, a study of the bonding strength and integrity is ongoing which is also one of the reasons for increasing the piranha process time according to Section 4.2.4, since if the bond is strong and void-free, the holes and poly-Si flakes will be a non-issue. A comparative picture of four different anodic bonded wafers after being etched down to the top plate is seen in Fig. 4.32. The wafers shown in the top are made by postdoc Rune S. Grass and in a) a regularly anodic bonded wafer, made before the alignment bonding was introduced, is seen with a near void-free bond compared to b) which is the TH1-A chip fabricated with alignment bonding and also a 10 min piranha, see Table 4.2, which have a lot of smaller voids and frayed edges. Then, in c) is the RC190+190 wafer made with a 10 s piranha and in d) the RC512+512 wafer with a 5 min piranha clean, see Table 4.2. Both display a multitude of small voids, however a decrease in d) the RC512+512 wafer due to an increased piranha clean and the intermediate graphite sheet during anodic bonding preventing the isotropic super etching hole pattern. These two solutions have brought the fabrication a long way and the perfectly bonded area of 7 cm $\times$ 7 cm could facilitate an RC1024+1024 element array the size of 5.3 cm $\times$ 5.3 cm.

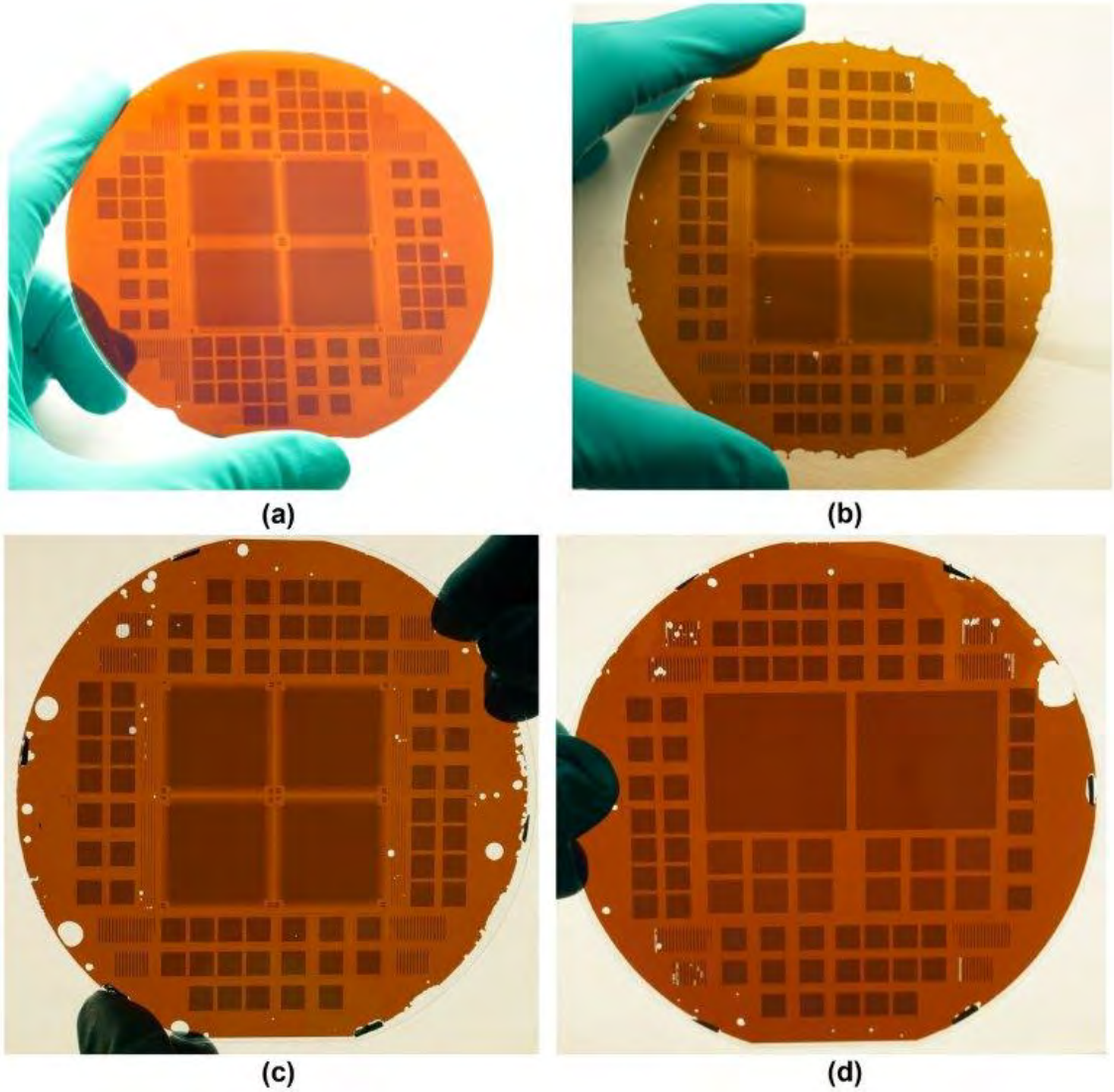


Figure 4.32: The wafers presented at the top were fabricated by postdoc Rune S. Grass. In a), a regularly anodic bonded wafer without alignment bonding is depicted, which exhibits a nearly void-free bond, in contrast to b), which shows the TH1-A chip fabricated with alignment bonding and a 10 min piranha cleaning process (as described in Table 4.2), resulting in numerous small voids and frayed edges. Subsequently, c) displays the RC190+190 wafer subjected to a 10 s piranha cleaning process, while d) shows the RC512+512 wafer that underwent a 5 min piranha cleaning process (as detailed in Table 4.2). Both c) and d) exhibit multiple small voids, although there is a decrease in the number of voids observed in d) due to an increased duration of piranha cleaning and the use of an intermediate graphite sheet during anodic bonding, which prevents the formation of the isotropic super etching hole pattern.

4.4 Chapter summary

This chapter focused on the process optimization of the challenges that arose while fabricating the RC190+190 wafers as well as the RC512+512 wafers and the characterization, tests and solutions performed to optimize the process. The most significant discoveries of this thesis were presented in this chapter. These discoveries included the identification of the isotropic hole pattern, which caused the formation of super etching channels in the wafer stack, which have previously destroyed wafer batches by penetrating the top plate prematurely. This issue was successfully addressed by implementing a protective graphite sheet during anodic bonding. Additionally, the investigation and correlation of gold particles found during bottom electrode metal evaporation form short circuits during anodic bonding between the top and bottom electrodes of the CMUT cell. This discovery was confirmed through FIB-SEM imaging and impedance measurements of the RC16+16 array from the RC190+190 wafers. Steps have been taken to mitigate the particle problem, such as investigating the different metal tools and implementing a particle scan prior to metal deposition to assess the number of generated particles. As a concluding mark, ongoing investigations are being carried out to gain further insights into this issue of the top and bottom electrode short circuits as this represents the final challenge that needs to be overcome. The subsequent chapter will present the electrical characterization of the RC190+190 wafers.

Chapter 5

Transducer characterization

5.1 Introduction

In this chapter, detailed electrical characterization is performed on the RC190+190 wafers. Firstly, the electrical characterization of all 120 linear elements and impedance measurements of linear elements are described and demonstrated. Followed by a complete characterization of all eight large RC190+190 arrays.

5.2 Electrical characterization

To assess the electrical performance of the CMUT impedance measurements are performed on the Cascade Summit 12K Probe Station through the B1500A Semiconductor Device Parameter Analyzer from Keysight. Three types of measurements are conducted to verify the characteristic CMUT behavior: Zf, IV, and CV. The impedance versus frequency, Zf, measurement should confirm a phase angle of $-90°$ and a linear negative gradient impedance. Additionally, the frequency at which the capacitance-voltage curve, CV, should be performed is determined by evaluating a stable capacitance in the frequency range. Ideally, the CMUT should have a low leakage current in the current-voltage, IV, measurement and a symmetric parabolic capacitance-voltage curve, CV. Therefore, working elements are determined by:

- **Zf**: -90 degree phase, straight declining impedance and stable capacitance
- **IV**: Current $> 100\,\mu A$ deemed shorted and current $< 100\,fA$ not connected
- **CV**: Parabolic coherent CV, without hysteresis.

These studies are conducted at low frequencies, ranging from 10 kHz to 1 MHz, and are significantly distant from the resonance of the CMUT. The CMUTs are designed to have a center frequency of 8 MHz and a pull-in voltage of 160 V with an operating voltage at 128 V. Only the RC190+190 wafers are electrically characterized, due to cleanroom equipment being out of use and preventing the finalization of the RC512+512 arrays for the last five months of this PhD.

5.3 Linear arrays

5.3.1 A single linear element

In this section measurements performed on the 15th linear element on TH1_20220322_01 in the southeast, SE, corner of the wafer are presented, an overview of the linear

Figure 5.1: A stitched microscope image overview of the 15 linear elements in the south-east corner of the wafer, *TH1_20220322_01_CLinSE*. The 15th element, *E15* furthest to the right, is characterized and described in detail in the section below.

array can be seen in Fig. 5.1 with the characterized element, *E15* furthest to the right.

The CMUT characteristics described in the prior section can be seen in the overview of Fig. 5.2 for the linear element. Inspecting Fig. 5.2 from top to bottom, from the IV measurement the isolation between the top and bottom electrode of the CMUT is verified with a low leakage current of a 100 pA. The frequency response of the impedance magnitude, Zf, in a double log plot, is a negative straight line confirming it is a capacitive device. Additionally, the capacitance frequency graph reveals that the capacitance remains stable across the entire frequency range and the phase is $-90°$ as expected. The measurement of capacitance up to $\pm$ 100 V exhibits a parabolic behavior characteristic of a CMUT.

A prolonged Zf measurement was executed and the impedance is stable up to 5 MHz observed in Fig. 5.3 with a phase angle value of almost $-90°$ characteristic of an ideal capacitor. The semi-log plot of the capacitance frequency response decreases slightly towards 1 MHz as normally observed when probing followed by an increase in capacitance towards 5 MHz becoming less capacitive due to the measurement setup. Higher frequencies will be tested and described in the Section 5.4.

A CV curve was measured with a resolution of 200 mV and the results are shown in Fig. 5.4. A parabola was fitted to the data and is shown as a dashed line, showing a perfect parabolic fit up to 100 V with an extracted offset voltage of 0.36 V indicating that there is nearly no fixed charge in the CMUT. The capacitance is stable and without any hysteresis, hence no mobile dielectric charging. The capacitance of a linear element is identical to that of an RC16+16 and is calculated from Eq. 2.17

$$C_{16} = \frac{\epsilon_0 A^2}{g_{\text{eff}}} = \left(\left(\frac{\epsilon_0 A^2}{g} \right)^{-1} + \left(\frac{\epsilon_0 \epsilon_{\text{OxyNi}} A^2}{t_{\text{OxyNi}}} \right)^{-1} \right)^{-1} = 36.87\,\text{pF}, \tag{5.1}$$

where the measured 37.44 pF zero bias capacitance deviates 1.5 % from the calculated capacitance. This increase in capacitance could be explained by fringing fields.

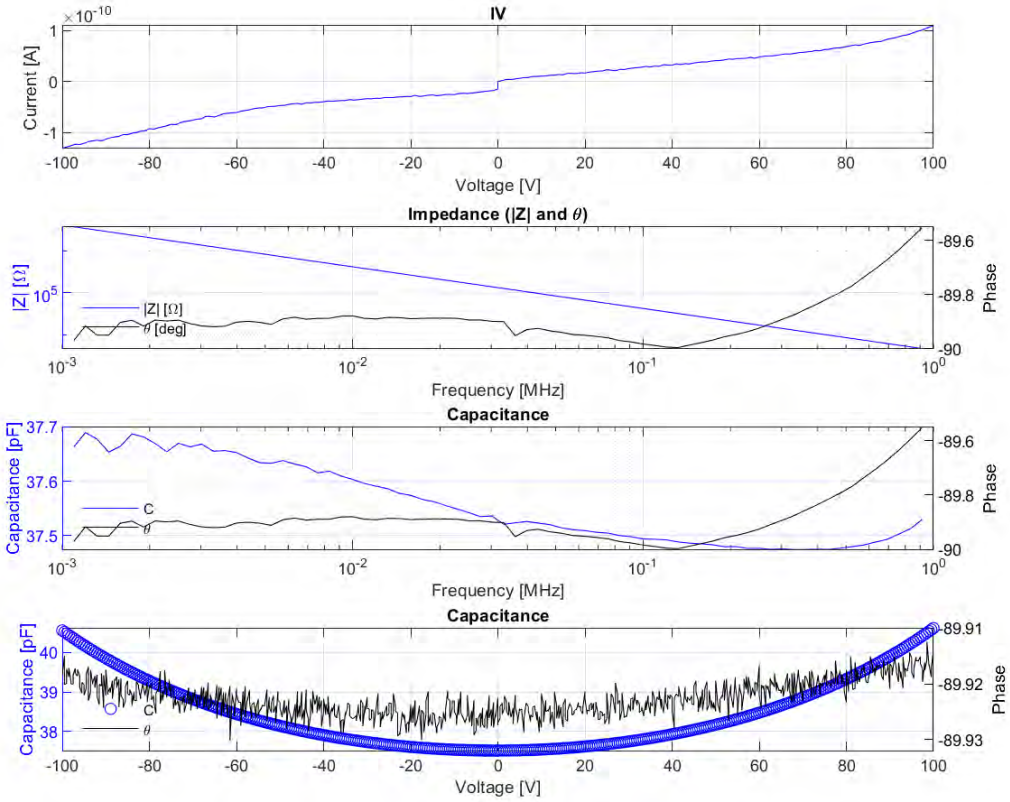
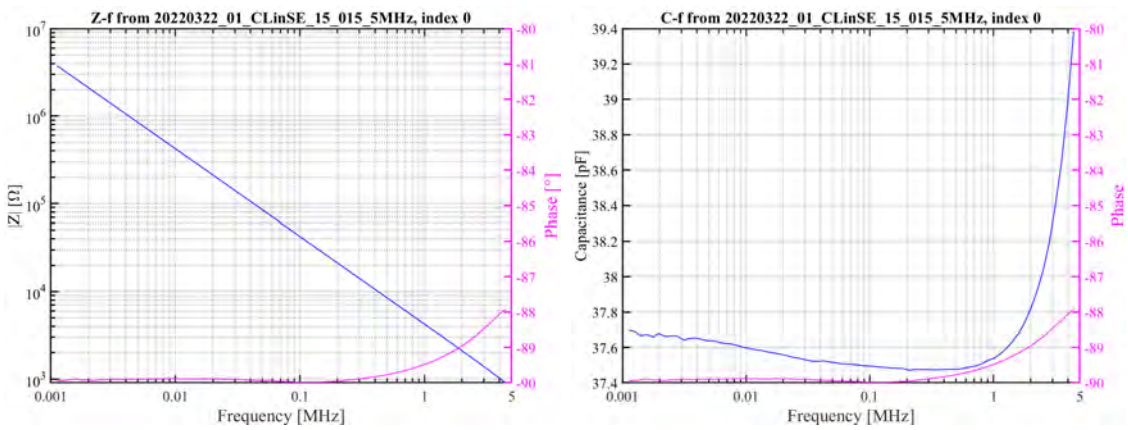


Figure 5.2: The classic characterization measurements IV, Zf, Cf and CV shown for *TH1_20220322_01_CLinSE_E15* and probed on all linear elements.



(a) **(b)**

Figure 5.3: Zf response on a double logarithmic scale with a straight line impedance and a negative phase value of $\approx -90°$ as of that of an ideal capacitor. C-f semi-log plotted shows a slight increase in capacitance above 1 MHz due to the use of regular DC probes, the observed response does not represent the true CMUT response.

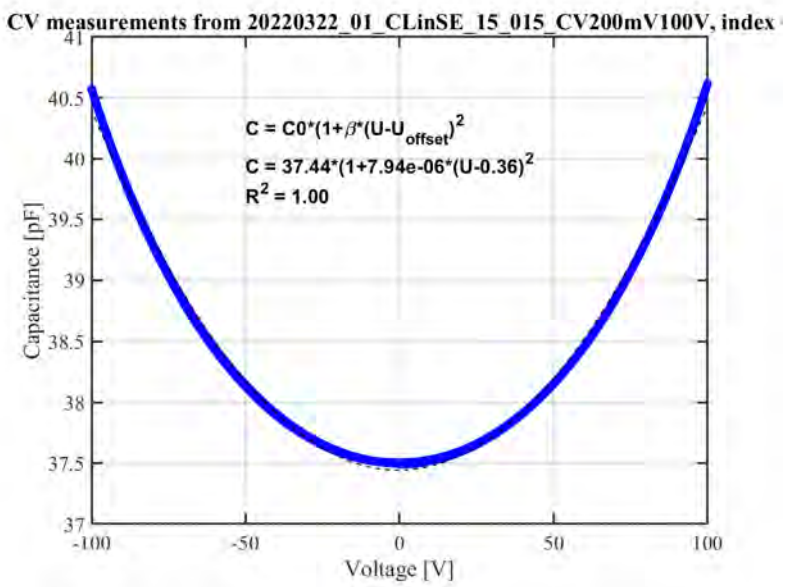


Figure 5.4: Capacitance measured for positive and negative increasing and sequentially decreasing bias. Showing a fully parabolic curve with a negligible offset voltage and no charging indicates a stable device.

5.3.2 All linear elements

All four sections (NE, NW, SE, SW) of linear elements were characterized on both wafers and the results are presented in Table 5.1. In total 120 linear elements were electrically characterized.

	TH1_20220322_01				TH1_20220322_04					
	NE	NW	SE	SW	NE	NW	SE	SW	Avg	Units
Total accepted	15	10	15	13	5	7	2	8	9,375	Elements
Short circuited	0	5	0	2	10	8	13	7	5,625	Elements
Not connected (NC)	0	0	0	0	0	0	0	0	0	Elements
Low C ($C_{\text{min}} < 5$ pF)	0	0	0	0	0	0	0	0	0	Elements
Bad elements ($R^2 < 0.90$)	0	0	0	0	0	0	0	0	0	Elements
Yield	100	66,67	100	86,67	33,33	46,67	13,33	53,33	62,5	%
C_0 mean	38,83	37,4	38,2	38,26	40,37	37,32	39,46	41,73	38,94	pF
C_0 std deviation	1,14	1,33	0,95	1	0,45	0,49	0,4	9,69	1,93	pF
C_0 median	39,02	37,18	37,84	38,27	40,57	37,38	39,46	38,7	38,55	pF
C_0 mean of range	36,82-40,51	35,76-39,29	36,88-40,09	36,98-40,55	39,59-40,72	36,50-37,96	39,18-39,74	35,00-65,31		pF
V_{offset} mean	-0,23	-0,04	-0,12	-0,15	-0,68	0	-0,53	3,39	0,20	V
V_{offset} std deviation	0,05	0,11	0,18	0,08	0,21	0,16	0,36	6,75	0,98	V
V_{offset} median	-0,22	0,04	-0,08	-0,15	-0,8	-0,05	-0,53	0,96	-0,10	V
IV_{max} mean	136,45	116,93	136,3	141,11	149,4	155,28	159,84	65358	8294	pA
IV_{max} std deviation	14,23	21,82	13,51	10,41	6,5	9,39	2,5	184414	23061	pA
IV_{max} median	142,54	117,14	137,96	144,33	148,45	153,38	159,84	165,38	146	pA
IV_{max} mean of range	105,58-149,54	88,94-144,49	111,38-156,07	120,96-154,15	142,48-160,11	144,41-168,87	158,07-161,61	115,63-521760		pA
Hysteresis	0	0	0	0	0	0	0	0		Elements
Hysteresis	0	0	0	0	0	0	0	0		Elements

Table 5.1: Overview table of all the linear arrays measured at the four sections on both wafers.

The top part of the table addresses the yield in which the wafer *TH1_20220322_01* is superior. The combined yield of the linear elements across the two wafers is 62.5 %, and the presence of short-circuited elements is the sole reason for the deviation from a 100 % yield. An average of 5.6 elements are short-circuited per 15 linear elements, this is quite high yet explainable.
An example of 1:1 visual explanation of the 5 short-circuited elements in NW on wafer TH1_202220322_01 is seen in Fig. 5.5. Through backside inspection with a high-resolution microscope, the shorts are explained by a ruptured top plate caused by voids from the bonding or isotropic holes from the KOH etch resulting in the short circuit of elements no. 1 and 11. The remaining three short-circuited elements 9, 10 and 12 are due to the dark spots with a lighter aura of metal as seen in the

bottom of Fig. 5.5. Similarly, for the linear elements located at SW, the two short-circuited elements no. 10 and 15 are caused by dark spots. Hereby explaining all short circuits for the measured linear elements on wafer TH1_202220322_01. Unlike voids, which are predominantly found along the wafer's edge due to particles introduced during handling, the dark spots with surrounding discoloration in the bottom electrodes are not location-dependent and pose a problem across the entire wafer. The absence of the top plate resulting from voids is due to the outer placement of the linear elements, along the periphery of the wafer as shown on the wafer map in Fig. 2.9, where particles from handling tend to cause void formation.

An interesting finding is that all non-shorted linear elements exhibit exemplary electrical CMUT behavior. None of the elements show any disconnection, i.e. zero in the *not connected (NC)* category. Furthermore, there is no capacitance measured below 5 pF across the elements that is the *Low C* category and finally none in the *Bad elements* category with a non-parabolic fit. This indicates a robust fabrication process and demonstrates the high-quality electrical performance of the CMUT devices, especially considering the placement along the periphery of the wafer. As mentioned, the low yields are all due to short-circuited elements, whereof many are explained by the placement at the edge of the wafer more exposed during fabrication.

The electrical key parameters are $C_{0,\,\mathrm{avg}} = 38{,}95 \pm 1{,}93$ pF, $V_{\mathrm{offset,avg}} = 0.21$ V and $IV_{\mathrm{max,median}} = 146\,\mathrm{pA}$ from which it can be concluded that the linear elements are stable and reliable without hysteresis or dielectric charging. Hysteresis in this context refers to a phenomenon where there is a difference in capacitance values during increasing and decreasing bias sweeps. Instead of observing identical values and a consistent parabolic CV curve, a discrepancy or gap between the two is observed. This hysteresis is attributed to dielectric charging [90, 91]. The formula for determining hysteresis is to measure the difference in capacitance between 0 V to ± 100 V, $C_{(0\mathrm{V}\rightarrow\pm100\mathrm{V})}$, and then the following ±100 V to 0 V, $C_{(\pm100\mathrm{V}\rightarrow0\mathrm{V})}$, described as

$$\frac{\Delta C_{\pm\mathrm{sweep}}}{C_0} = \frac{C_{(0\mathrm{V}\rightarrow\pm100\mathrm{V})} \cdot C_{(\pm100\mathrm{V}\rightarrow0\mathrm{V})}}{C_0} \tag{5.2}$$

$$\Delta C_{\pm\mathrm{hyst}} = \sum^{N} \frac{\Delta C_{\pm\mathrm{sweep}}}{C_0} / N \tag{5.3}$$

where $\Delta C_{\pm\mathrm{sweep}}/C_0$ is a vector containing the ΔC values for bias sweep divided by C_0 extracted from the CV-curve. The value of $\Delta C_{\pm\mathrm{hyst}}$, calculated as the mean of the vector, indicates the extent of hysteresis in the CV data. Additionally,$\Delta C_{\pm\mathrm{hyst}} \cdot N$, corresponds to the area or gap between the two capacitance curves for either the positive or negative side of the plots. Previously analyzed data from an anodic bonded RC190+190, the TH1-A chip, had established a threshold value of $\Delta C_{\pm\mathrm{hyst}} > 0.95 \times 10^{-3}$ as acceptable, and this criterion was employed again.
Linear elements are the simplest form of CMUT arrays. Linear arrays play a crucial role in assessing the electrical performance of the device and determining the success of the fabrication. They provide valuable insights into the device's functionality and assist in identifying areas that may require further process optimization.

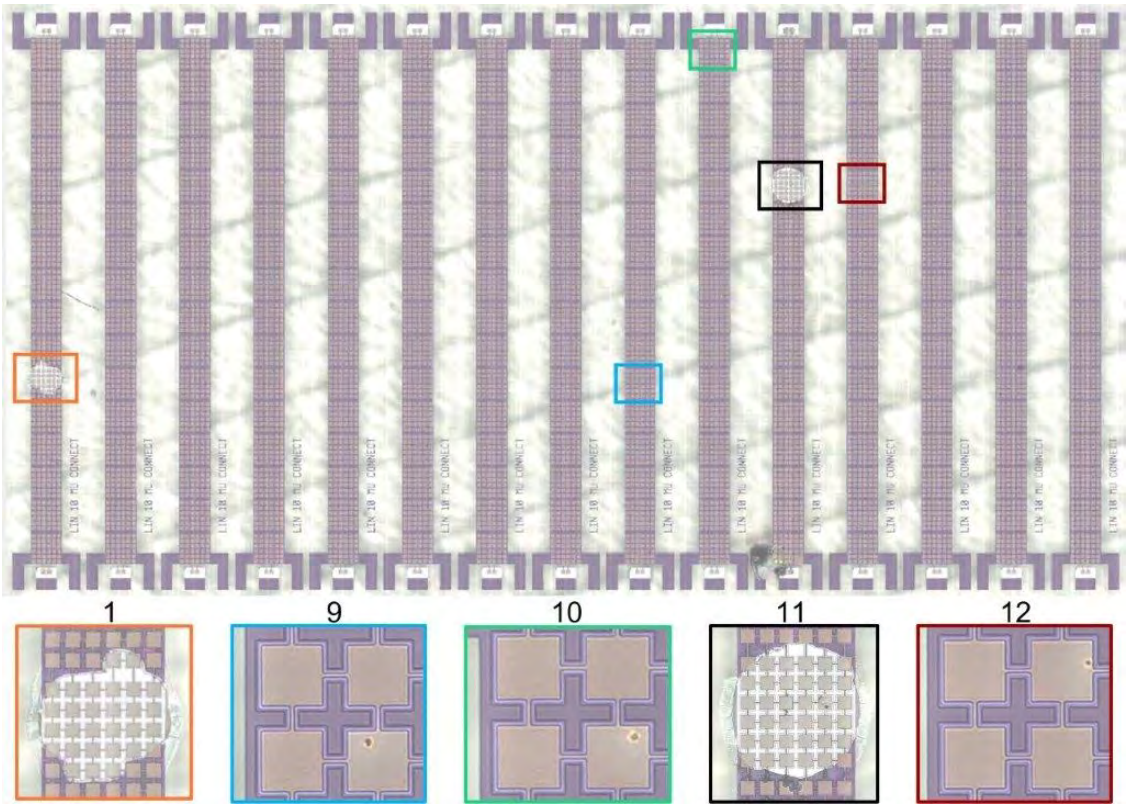


Figure 5.5: A stitched backside microscope image of the 15 linear elements located in the northwestern, NW, corner of wafer TH1_202220322_01. A color-coded correlation between the five shorted elements: 1, 9, 10, 11 and 12 is presented. Two types of damages are observed as a cause for the short circuit: Voids and dark spots in the bottom electrode. The voids are presumably from particles caught at the bond interface during the anodic bonding process resulting in air-filled voids that rupture during etch thinning of the top PSOI wafer. The dark spots in the bottom electrode surrounded by discoloration have been characterized with FIB-SEM and show that the gold bridge the vacuum gap and penetrates the top plate, hereby connecting the top and bottom of the CMUT. Dark spots are seen across the entire wafer, while voids are mainly observed along the wafer's edge, due to particles caught in the bond interface, where the linear elements are placed.

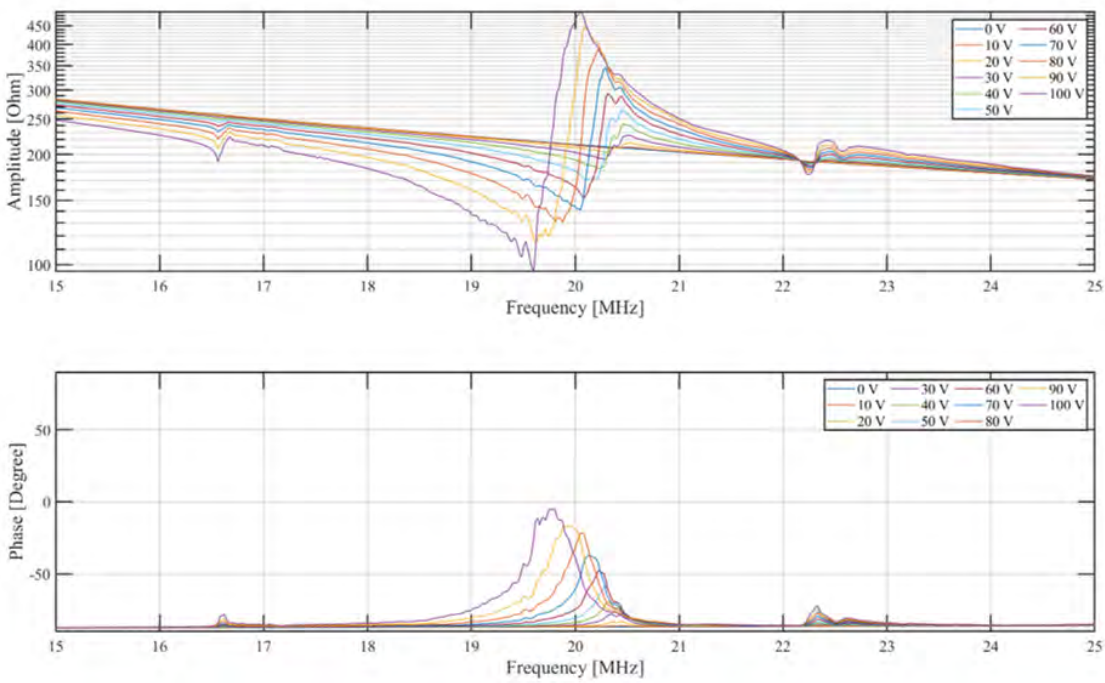


Figure 5.6: Impedance measurement from 0 V to 100 V for a linear element showing a downshift in frequency with increasing bias from 20.4 MHz to 19.6 MHz. The main peak is observed with an increasing phase and amplitude alongside two fixed peaks at 16.5 MHz and 22.3 MHz. At the present time, the origin of these additional peaks remains unknown.

5.4 Impedance measurements

In this section, the impedance measurements on linear elements are presented. Probing the linear element at a higher frequency to examine the frequency response near resonance was done on the Agilent E4990A impedance analyzer combined with the Keithley 2410 Sourcemeter operated by a GUI in MATLAB developed by former postdoc Martin Lind Ommen. In Fig. 5.6 the impedance can be observed for TH1_20220322_01_CLinSE_15_E15, at voltages from 0 V to 100 V. A downshift in frequency from 20.4 MHz to 19.6 MHz indicates spring softening for increasing voltages of the CMUT cells. There are two spurious peaks at 16.5 MHz and 22.3 MHz accompanying the main peak. The spurious peaks do not show spring softening with increased bias, suggesting that they are not CMUT cells, the source is still being examined.

Theoretically, the pull-in voltage is designed to be 160 V. However, as seen in Fig. 5.7 there is no large decrease in frequency at 160 V. Merely a gradual decrease as seen in Fig. 5.6 evidently the actual collapse point is yet to be reached. The peak phase angle is 16.2° and the slope capacitance, the capacitance calculated from the impedance at low frequency, of 45.2 pF at 160 V.

Subsequently, the bias was increased to 200 V, see Fig. 5.8, on an adjacent linear element in an effort to reach the pull-in voltage. A clear indication of pull-in did not occur. Furthermore, the evolution of the peak phase angle with increasing bias should be a steady increase whereas here it is exhibiting a weaving behavior that might suggest dielectric charging. Nearly, a complete phase shift with a peak at 71.3° and a sloped capacitance of 61.4 pF is measured at 200 V. The smaller peaks occurring at approximately 22 MHz, 27 MHz, 33 MHz and 37 MHz roughly after every increase of 5 MHz is currently not understood.

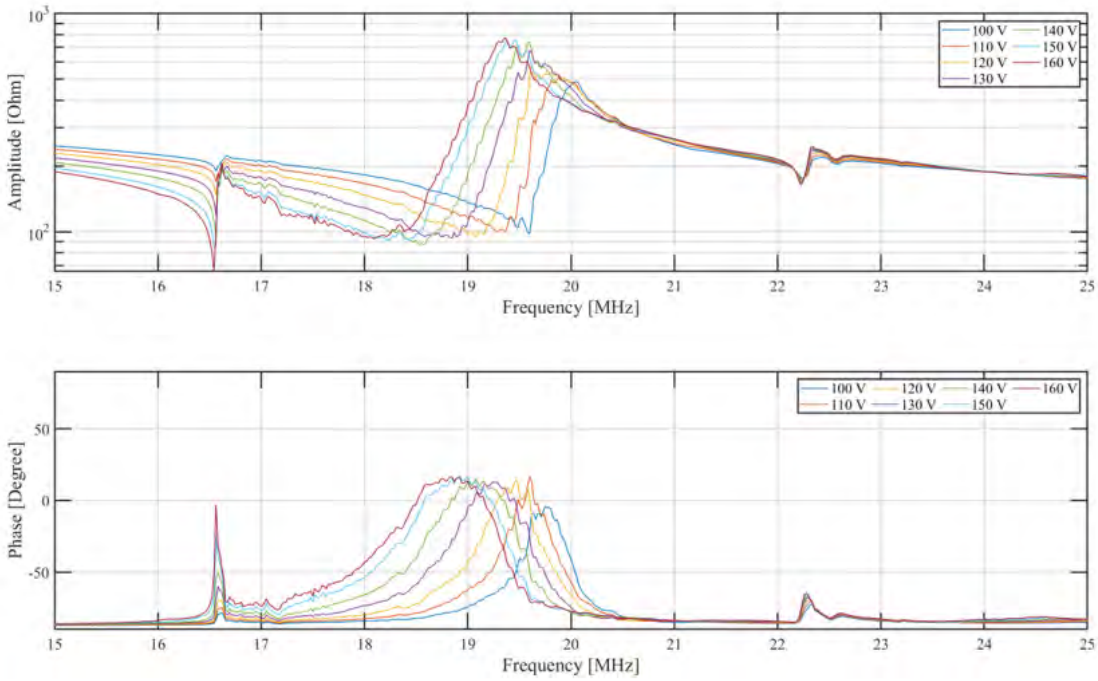
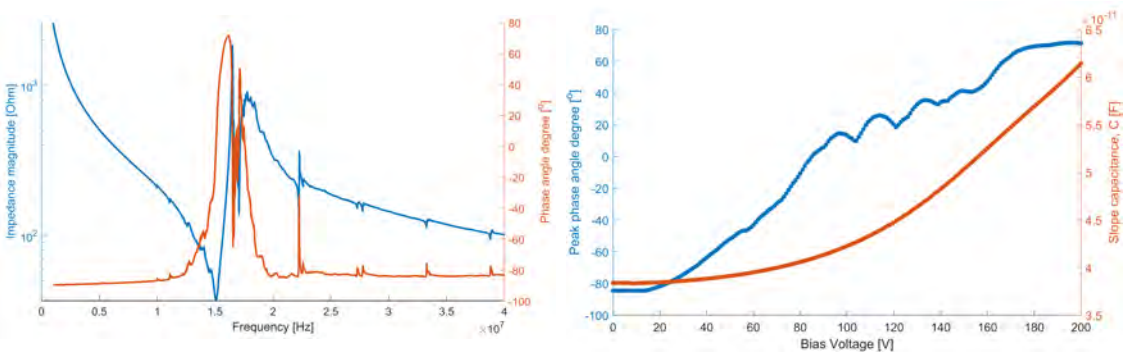
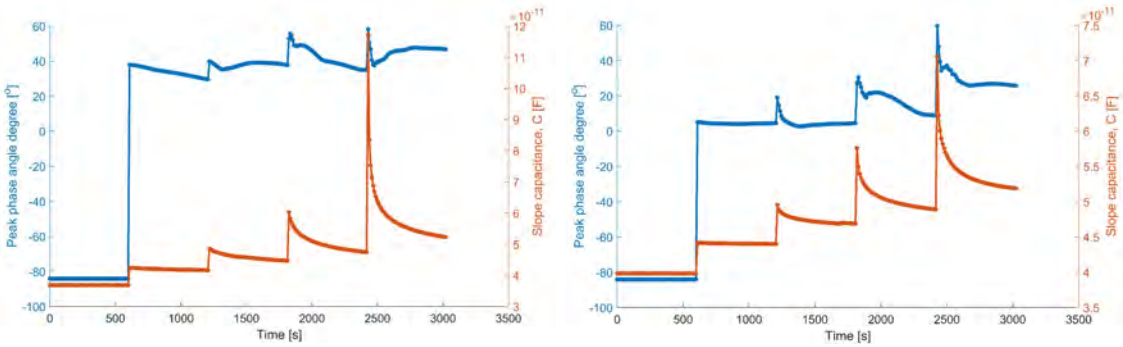


Figure 5.7: Impedance measurement from 0 V to 160 V a linear element showing a downshift in frequency with increasing bias displaying spring softening of the top plate of the CMUT. The main peak is accompanied by two stationary peaks at 16.5 MHz and 22.3 MHz, at the time of writing still unknown from where these originate.



(a) (b)

Figure 5.8: Impedance measurement from 0 V to 200 V a linear element showing the impedance magnitude and phase angle as a function of frequency in a). The phase angle and sloped capacitance of the impedance are plotted as a function of applied bias voltage in b).



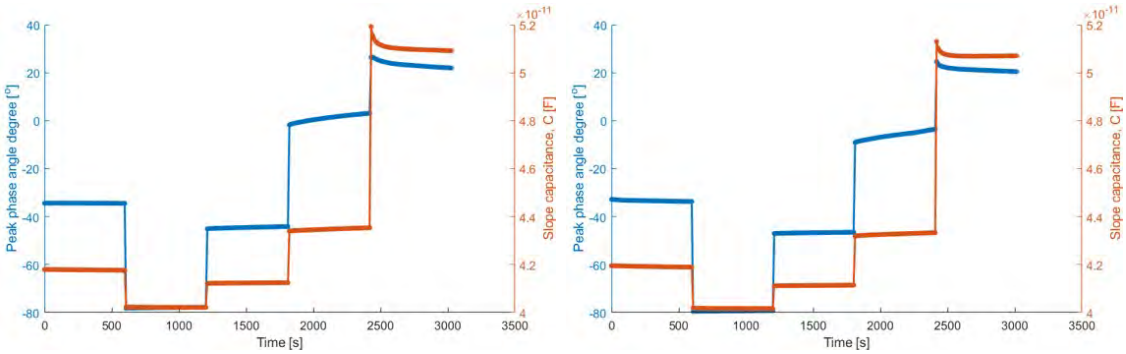
(a) (b)

Figure 5.9: First stability measurements of the linear element conducted for positive a) and negative DC ramps. The voltage steps are 0 V, 100 V, 130 V, 160 V and 200 V and held for 10 min. The CMUT is stable up to 100 V.

FEM simulation of the CMUT with a vacuum gap of 135 nm, an insulation layer of 180 nm a poly-Si top plate thickness of 2.3 µm yields a pull-in voltage of $V_{\mathrm{pi}} =$ 166 V and a biased center frequency at 80 % V_{pi} of 22.3 MHz. At 130 V the observed frequency is almost 2 MHz lower than anticipated in air.

5.4.1 Stability

In order for the CMUT chip to be approved for clinical use, it should be stable and able to take images for a prolonged time. Therefore stability measurements where specific voltages are held for a duration of 10 min are performed to ascertain the stability of the CMUT.
A bias staircase where each voltage is held for 10 min can be seen in Fig. 5.9 for a linear element for positive a) and negative b) biases. For 0 V and 100 V the CMUT is stable, at higher voltages, the capacitance drops rapidly which is caused by charging in the device. With a pull-in voltage of 160 V the operating voltage would preferably be 80 % of that i.e. 128 V. The CMUT could still be driven at 100 V and effectively be used in an ultrasound probe.
Investigating this charging phenomenon a 2nd and 3rd stability test was repeated on the same element with the same polarity see Fig. 5.10. Surprisingly, the 2nd and 3rd repetitions showed a stable capacitance and peak phase angle when the same polarity was applied. Leading to the idea, that the CMUT could be operated by a precondition of receiving a calculated charge and then performing stably. For the second measurement a peak phase of 22° and a capacitance of 51 pF was obtained at −200 V. Comparing the third measurement which had a peak phase of 20° and a capacitance of 51 pF also at −200 V, these are the same indicating a stable performance. The total time of the stability measurements is 50 min.



(a) **(b)**

Figure 5.10: 2nd and 3rd stability measurements performed on the same element for negative biases in steps of 0 V, 100 V, 130 V, 160 V and 200 V. Each voltage step has a duration of 10 min. The element has a more reliable and stable performance compared to the first stability test in Fig. 5.9, indicating that a precondition operation could be performed.

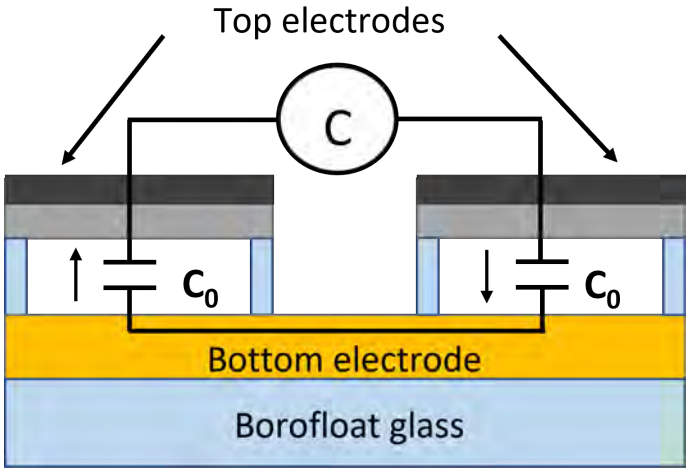


Figure 5.11: Simplified equivalent circuit of measuring between neighboring top electrodes for an RC CMUT array.

5.5 Row Column arrays

The Row-Column addressed array structure does not allow for individual element characterization using conventional micro-probe systems [54]. Therefore, a measuring technique of a row-column array between neighboring elements can be lumped into a *simplified* equivalent circuit see Fig. 5.11 was presented by Prof. Erik V. Thomsen and demonstrated [92] where the author contributed prior to this Ph.D. study. Measuring between two neighboring electrodes should result in two capacitors in series resulting in half of the single element capacitance, $C_0/2$ measured between the top and bottom electrode. The minimum element capacitance calculated from Eq. 2.17 at zero applied bias:

$$C_0 = 52\text{pF} \qquad C_0/2 = 26\text{pF}.$$

Due to the way the RC array is characterized by probing two neighboring elements, it is important to keep in mind when reading this section that all data, including IV and CV curves, are plotted for top-to-top and bottom-to-bottom elements and *not* top to bottom which is the case when the RC array is fully wire bonded and mounted in an ultrasound probe.

5.5.1 A single RC190+190 array

An RC190+190 array, named RC3, from wafer TH1_202220322_01, has been measured at low frequencies at medium integration time with yield, capacitance and voltage statistics seen in Table 5.2. The voltage is limited to a maximum of ± 50 V, which is equivalent to an effective voltage of 25 V on each element, taking into account voltage division. This approach enables a comprehensive mapping of the characteristics of the array elements, allowing for the identification and sorting of short-circuited, not-connected and low capacitance elements without the risk of causing damage to the elements due to prematurely pull-in occurring as the designed pull-in voltage is 160 V.
The yield determined for the bottom and top electrodes was 99.47 % and 96.30 %, respectively. The single short-circuited top element is found and visibly explained by wafer level optical inspection, caused by an interconnecting poly-silicon flake

Arrays statistics	**TH1_20220322_01_CRC3**		
	Bottom electrode	**Top electrode**	**Units**
Total accepted	188	182	Elements
Short circuited	1	1	Elements
Not connected (NC)	0	0	Elements
Low C beside shorts and NC	0	3	Elements
Bad elements, ($R^2 < 0.90$)	0	3	Elements
Yield	99.47	96.30	%
C_0 mean	52.04	33.87	pF
C_0 std deviation	27.78	12.78	pF
C_0 median	45.84	29.32	pF
C_0 mean of range	20.21-168.82	20.04-85.67	pF
V_{offset} mean	0.00	-0.03	V
V_{offset} std deviation	0.19	0.22	V
V_{offset} median	-0.01	-0.04	V
$\Delta\ C_{+\text{hyst}} > 0.95 \times 10^{-3}$	0	1	Elements
$\Delta\ C_{\text{-hyst}} > 0.95 \times 10^{-3}$	0	0	Elements

Table 5.2: Array statistics for RC190+190 array, RC3.

see Fig. 5.12. The current statistic for the top to top elements and the bottom to bottom elements can be seen in Fig. 5.13 where the working elements are marked blue and short-circuited elements are marked red. There is only a single shorted element in both graphs, where the shorted top to top element is explained by a burst top plate piece shown in Fig. 5.12. In characterization, there are three ways that elements can be short-circuited: Top to top element, bottom to bottom element and finally a top to bottom element short circuit. The latter will be measured after the array has been wire bonded. The first two, however, are already measured and stated. In the design process of this RC190+190 run several process optimization and design changes were implemented to achieve a higher yield. Among these a broadening of the kerf from 2.5 µm to 6 µm as a result of the top to top short circuit observed in the previous run of RC190+190 array, TH1-A. Examples of observed top to top shorts are: incomplete etching of the aluminum due to the small kerf when utilizing IBE, pieces of the ruptured top plate of conducting poly-silicon and particles that masked during the top electrode separation etch and short-circuiting the two neighboring electrodes. The RC190+190 array, TH1-A, has 46 shorted top to top elements, whereas this RC190+190 array, RC3, has 1 shorted top to top element. That is a 98 % reduction in the amount of top to top shorted elements while before it was 25 % of the top elements and with the improvements it is 0.5 % for the top to top measurements on this RC190+190 array. The bottom to bottom element shorts was previously observed through gold ribbons interconnecting them. In the previous TH1-A chip, there was 2 bottom to bottom short circuits and in this RC3-chip, there is only 1 bottom to bottom short circuit.

In Fig. 5.14 the minimum capacitances obtained from the CV tests are shown for both the bottom a) and top elements b). Likewise, the working elements are marked blue and the shorted elements are marked red. The median capacitance extracted from the CV measurements at zero bias, see Table 5.2, for the bottom elements is $C_{0,\ \text{median}} = 45.84\,\text{pF}$ and for the top elements it is $C_{0,\ \text{median}} = 29.32\,\text{pF}$, where the top elements are closest to the theoretical capacitance of 26 pF. Histograms for the

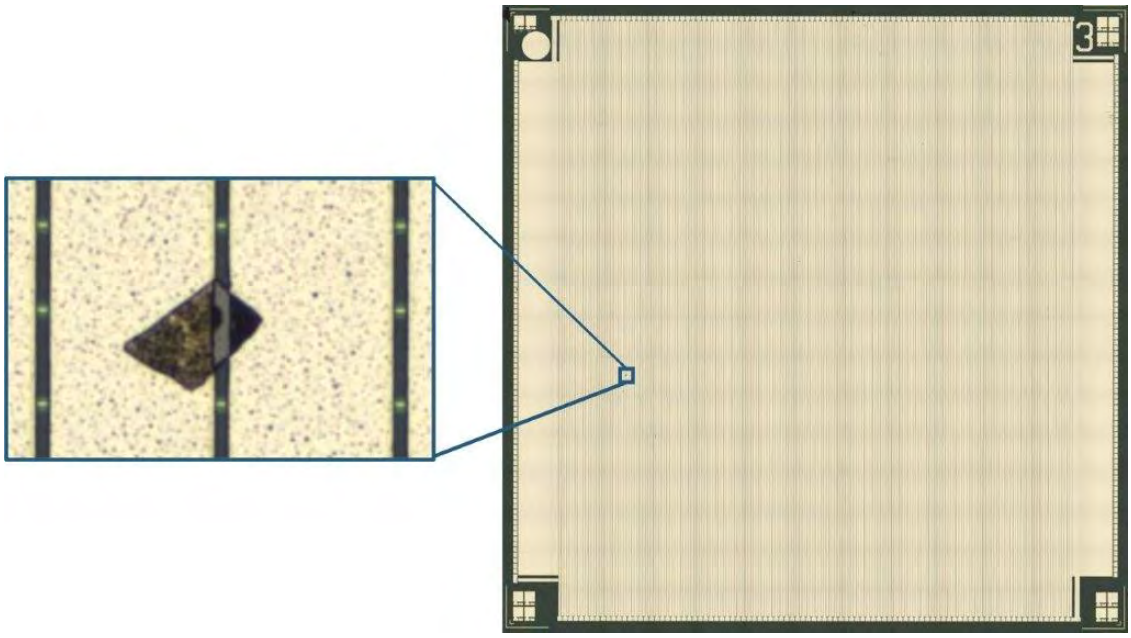
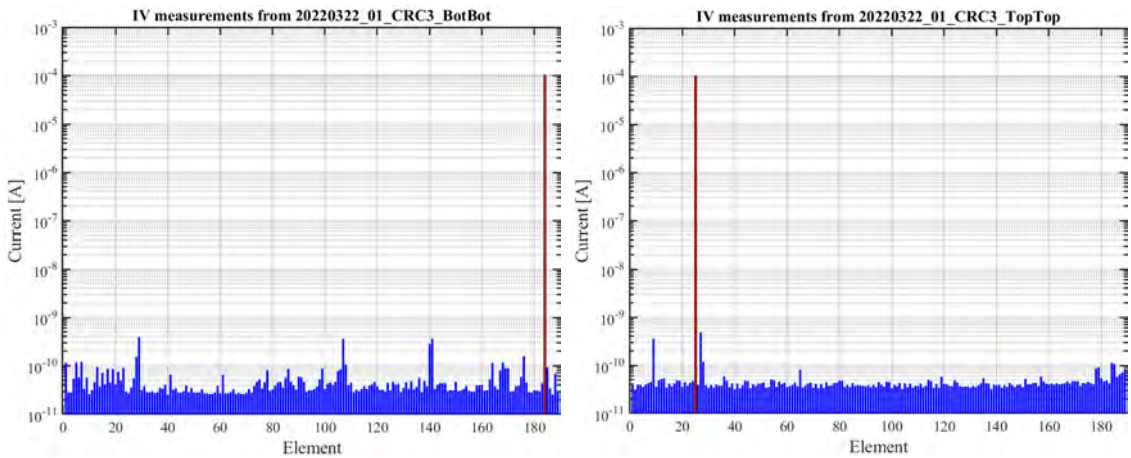


Figure 5.12: Stitched microscope image of the finalized RC190+190 array number 3, named RC3, with a zoom-in on the poly-silicon flake connecting top element no. 25 to its neighbor short-circuiting the two top electrodes.



(a) **(b)**

Figure 5.13: A bar plot is used to display the maximum currents along the y-axis measured in the IV tests for the element on the x-axis for the top elements in a) and the bottom elements in b). The working elements are shown in blue and exhibited a consistently low current below 1 nA. There is only one short-circuited bottom element, no. 184, and similarly, only one short-circuited top element, no. 25, exceeds the current limit of 100 µA and is marked red.

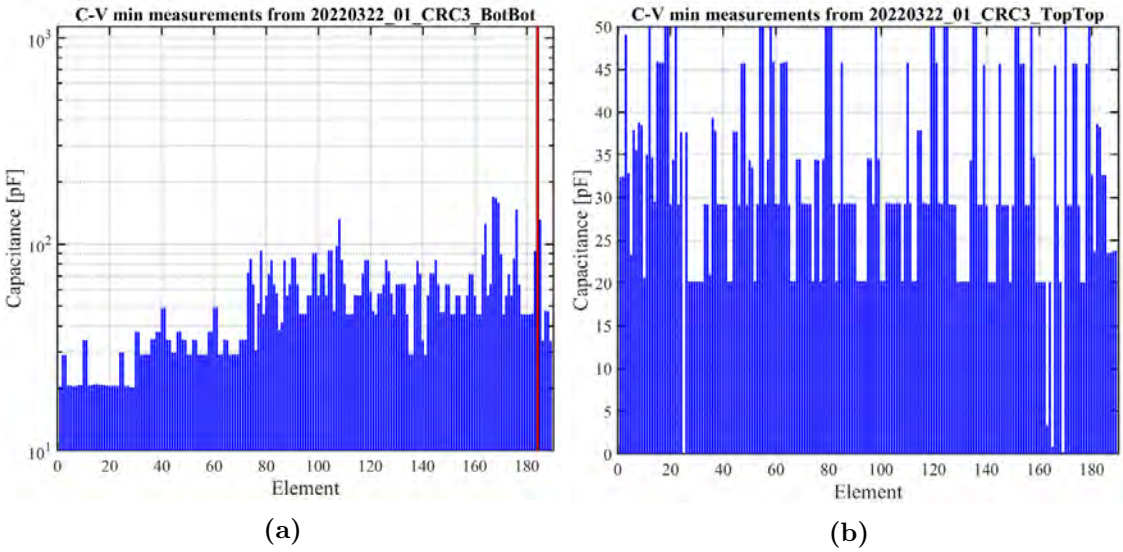


Figure 5.14: A bar plot of the minimum capacitance measured in CV tests along the y-axis, with each element represented on the x-axis for the bottom elements a) and the top elements b). The y-axis for the zero voltage capacitance is displayed on a logarithmic scale for better visualization of the bottom elements in a) and on a linear scale with a cut-off at 50 pF for the top electrodes in b). The mean capacitance for the bottom electrodes is $C_{\text{min}} = 52.04\,\text{pF} \pm 27.78\,\text{pF}$ and for the top electrodes $C_{\text{min}} = 33.87\,\text{pF} \pm 12.78\,\text{pF}$, also stated in Table 5.2. The capacitance can roughly be grouped into levels at 20 pF, 30 pF, 60 pF and > 60 pF, which will be elaborated in the text. In b) for the top elements, no. 25 is short-circuited and no. 163, 165 and 169 are categorized as bad elements with $C_0 < 5\,\text{pF}$ and a non-parabolic fit, see Table 5.2.

minimum capacitance, extracted from the CV measurements can be seen in Fig. 5.15 for neighboring top and bottom elements, respectively. A variation of capacitance is observed, though divided into distinct levels easily seen from the histograms of capacitance. This grouped division suggests a system, thus a cause and explanation to be examined.

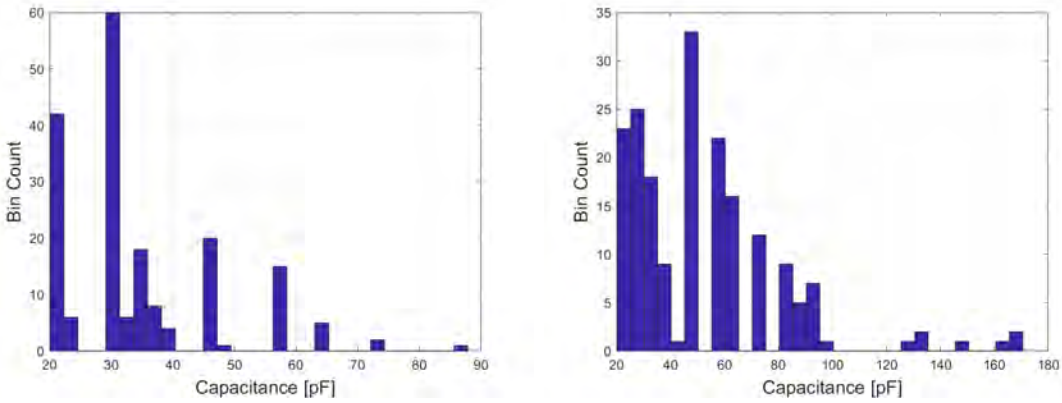
Inspecting Fig. 5.14 and Fig. 5.15, the levels are roughly 20 pF, 30 pF, 60 pF and > 60 pF. Process variation in the fabrication can explain the capacitances from 20-30 pF, as the vacuum gap, g, deviates 10 nm to 15 nm and the lateral reduction of the bottom electrodes area, A, is 1 µm to 2 µm for the connecting wires. The minimum and maximum capacitance due to fabrication deviation in vacuum gap height, g, as well as bottom electrode area, A, is

$$C_0 = 47\text{pF} \quad \text{and} \quad 52\text{pF}$$
$$C_0/2 = 22.5\text{pF} \quad \text{and} \quad 26\text{pF}.$$

Above 26 pF the cause can be multiple adjacent connected elements, as presented in [92] short-circuited neighboring elements can be calculated as

$$C = \frac{(m+1)(n+1)}{m+n+1} = \frac{1 \times 2}{1+2} = \frac{2}{3}C_0 \tag{5.4}$$

for one shorted neighbor, $m = 1$ to one side and none to the other, $n = 0$ yielding $2/3\ C_0$ from an element which has double the area, hence shorted with its neighbor (not probed). This type of interconnecting scheme can explain the capacitance level of 31 pF-35 pF. This reasoning would be applicable only if the capacitance values are measured on the adjacent elements to the short-circuited elements i.e. top elements no. 25 and 26 and bottom elements no. 184 and 185. All other elements



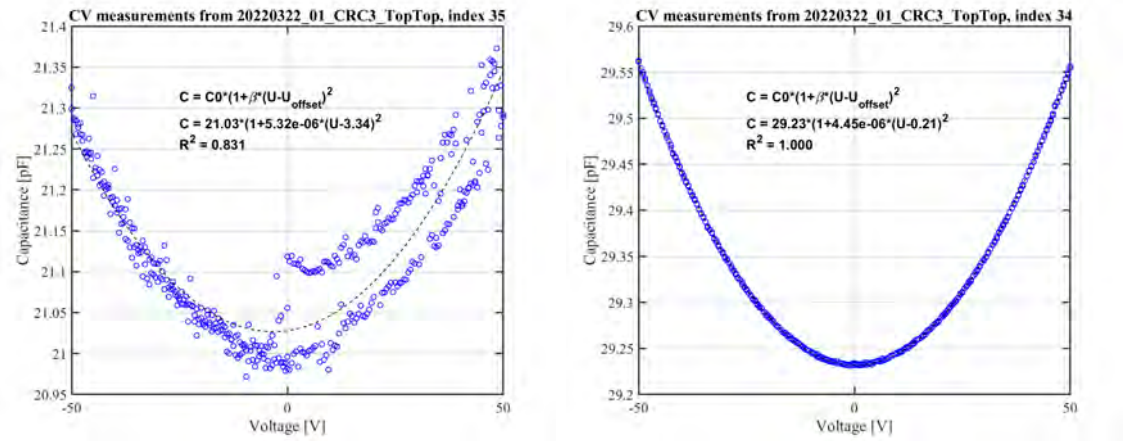
(a) (b)

Figure 5.15: Histograms for the minimum capacitance, extracted from the CV measurements for the top a) and bottom b) elements of RC3, respectively. The capacitance levels are categorized as 20 pF, 30 pF, 60 pF and > 60 pF. Process variation that occurred during fabrication may account for capacitance values between 20-30 pF, as there is a deviation of 10-15 nm in the gap height and a 1-2 µm lateral reduction in the area of the bottom electrodes.

exhibit higher capacitance values can not exclusively be explained by connection to neighboring shorted elements. These higher capacitance levels could be explained by orthogonally connected elements through top and bottom electrodes, enabling much more complex connecting schemes between several top and bottom elements. This peculiarity is investigated after wire bonding, where it is possible to do individual element probing and measure from the bottom to the top electrodes in the RC array.

Regarding the rest of the categorizations in Table 5.2, there are 3 bottom elements that are not connected and 3 bottom elements that do not exhibit a parabolic fit, bad elements, these are the same 3 elements no. 163, 165 and 169. All three were inspected with high-resolution microscopy from the front and backside, see Fig. 5.12 without clear visual indication for the failure. In the two bottom rows of Table 5.2, the sorting was based on the presence of hysteresis observed in the CV measurements. Hysteresis is characterized by a disparity in capacitance values between upward and downward bias sweeps, contrary to the expectation of identical values and a coherent parabolic curve. Hysteresis in the CV curve is attributed to dielectric charging, a well-known and highly unwanted phenomenon [90,91]. Fortunately, only one top element, no. 35, showed hysteresis during a positive DC bias sweep seen in Fig. 5.16 compared to an exemplary parabolic capacitance curve for the neighboring element no. 34 seen in b). In contrast to the mobile dielectric charge, there exists a trapped charge that leads to a shifted center point in the parabolic capacitance-voltage (CV) curve. This shift is referred to as the off-set voltage denoted V_{offset} and for the bottom and top electrodes, the values are $V_{\text{offset}} = 0\,\text{V} \pm 0.19\,\text{V}$ and $V_{\text{offset}} = -0.03\,\text{V} \pm 0.22\,\text{V}$, respectively.

Linear elements identical to that of the RC190+190 were made with openings to the bottom electrode at both ends so that resistance in the bottom electrode could be measured from one end to another. The resistance of the bottom electrode of an RC190+190 was measured to 412 Ω which is higher than the theoretically calculated value of 238 Ω (see Eq. 2.26). The CMUT is designed to transmit at 8 MHz and have an element capacitance of 52 pF, however, the capacitance measured after



(a) **(b)**

Figure 5.16: Capacitance voltage sweeps for first + 100 V decreasing to zero bias and then sweeping to - 100 V returning to zero bias. Hysteresis refers to the measured difference in capacitance between increasing and decreasing sweeps at the same bias, where it should be the same value and follow a coherent parabolic curve. The hysteresis is attributed to dielectric charging, a widely recognized and undesirable phenomenon [90,91]. Fortunately, only top element no. 35 seen in a) exhibited hysteresis during the positive DC bias sweep. An exemplary parabolic capacitance curve is observed for the neighboring top element no. 34 shown in b) and observed for all working elements as seen in Table 5.2.

wire bonding was 56 pF. The increased resistance and capacitance will increase the predicted ωRC-value from Eq. 2.26 and reduce the magnitude of the preserved signal at the end of an element. The ωRC-product and the absolute value of the transfer function which can be calculated as described in Section 1.6 for the finalized RC190+190 are

$$\omega RC = 2\pi 8\,\mathrm{MHz} \times 419\,\Omega \times 56\,\mathrm{pF} = 1.179 \tag{5.5}$$

$$|H(L,\omega)| = 90\,\%. \tag{5.6}$$

If the RC190+190 array is operated at a frequency of 8 MHz it should generate a uniform pressure according to 90 % of the signal being preserved at the end of the element and the image quality thus maintained. This is a viable result compared to previously manufactured row-column probes from this research group with around 80 % of the signal preserved at transmit.

Table 5.3: Overview of the in total eight large RC190+190 arrays from the two finalized wafers. An elaborate version is seen in Table 5.4.

Wafer	TH1_20220322_01								TH1_20220322_04									
RC	1		2		3		4		1		2		3		4		Average	Units
Electrode	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top		
Total accepted	185	168	186	182	188	182	137	184	181	176	142	175	166	169	187	117	170,3125	Elements
Short circuited	1	12	3	6	1	1	0	4	6	13	6	14	1	13	1	12	5,875	Elements
Not connected (NC)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Elements
Beside shorts and NC																		
Low $C(C_{\text{min}} < 5$ pF)	0	7	0	1	0	3	7	0	0	0	36	0	15	4	0	35	6,75	Elements
Bad elements ($R^2 < 0{,}90$)	3	2	0	0	0	3	45	1	2	0	5	0	4	3	0	22	5,625	Elements
Yield	97,88	88,89	98,41	96,3	99,47	96,3	72,49	97,35	95,77	93,12	75,13	92,59	89,42	89,42	99,47	63,49	90,34	%

5.5.2 All RC190+190 arrays

Table 5.4: Complete overview of the in total 8 large RC190+190 arrays from the two finalized wafers, elaborate version of Table 5.3.

Wafer	TH1_20220322_01								TH1_20220322_04									
RC	1		2		3		4		1		2		3		4		Average	Units
Electrode	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top	Bot	Top		
Total accepted	185	168	186	182	188	182	137	184	181	176	142	175	166	169	187	117	170,3125	Elements
Short circuited	1	12	3	6	1	1	0	4	6	13	6	14	1	13	1	12	5,875	Elements
Not connected (NC)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Elements
Low $C(C_{\text{min}} < 5$ pF)	0	7	0	1	0	3	7	0	0	0	36	0	15	4	0	35	6,75	Elements
Bad elements ($R^2 < 0.90$)	3	2	0	0	0	3	45	1	2	0	5	0	4	3	0	22	5,625	Elements
Yield	97,88	88,89	98,41	96,3	99,47	96,3	72,49	97,35	95,77	93,12	75,13	92,59	89,42	89,42	99,47	63,49	90,34375	%
C_0 mean	60,64	37,02	59,37	34,83	52,04	33,87	50,64	34,46	52,11	36,09	60,39	36,75	53,17	31,3	50,02	31,97	44,66688	pF
C_0 std deviation	38,52	15,4	35,05	14,27	27,78	12,78	33,65	14,6	45,94	18,54	35,5	21,39	37,07	14	33,8	13,57	25,74125	pF
C_0 median	49,18	30,21	56,12	29,22	45,84	29,32	44,57	29,24	39,45	29,22	54,52	28,66	45,24	28	43,23	27,82	38,115	pF
C_0 mean of range	20,08-327,77	20,49-83,89	19,69-177,22	19,97-82,27	20,21-168,82	20,04-85,67	17,73-233,88	20,08-115,84	19,42-523,06	19,42-114,56	19,14-253,88	15,76-192,03	19,20-262,68	19,18-79,57	18,72-299,99	18,94-79,38		pF
V_{offset} mean	0,04	0,57	0,08	0,13	0	-0,03	-0,06	-0,04	-0,03	-0,02	0,15	0,04	0,07	-0,09	0,02	-0,07	0,0475	V
V_{offset} std deviation	0,48	1,1	0,63	0,37	0,19	0,22	0,46	0,33	0,81	0,13	1,37	0,41	0,68	0,27	0,36	0,63	0,5275	V
V_{offset} median	0,07	0,53	0,1	0,12	-0,01	-0,04	-0,02	-0,07	-0,01	-0,02	0,03	0,05	0,01	-0,15	0,02	-0,05	0,035	V
Hysteresis ($\Delta C_{+\text{hyst}} > 0,95 \times 10^{-3}$)	4	1	5	2	0	1	3	2	3	0	2	0	1	0	1	0	1,5625	Elements
Hysteresis ($\Delta C_{-\text{hyst}} > 0,95 \times 10^{-3}$)	2	3	5	2	0	0	2	3	1	0	2	0	2	0	0	3	1,5625	Elements

An overview of all the 8 large RC190+190 arrays is outlined in Table 5.3 and the complete overview in Table 5.4.
Generally, a high yield is achieved for all eight RC190+190 arrays, with a total average across the wafers of 90 %. The majority of shorted elements can be visually found using optical microscope inspection and explained, especially of the top electrodes. On average only 5.87 shorted elements or just 3 % for both top and bottom electrodes. All of the in total 3040 elements that were measured with this neighboring scheme were connected i.e. 0 not connected elements and only an average of 6.75 elements had a capacitance below 5 pF this category has an outlier, namely TH1_20220322_04 RC2 which have 36 bottom elements < 5 pF. Subtracting this outlier the number decreases to 4.8 elements on average that exhibit low capacitance. Likewise, 5.625 elements are deviating from the symmetric parabolic capacitance characteristic. The outlier in this group is TH1_20220322_01 RC4 with 45 bottom elements showing hysteresis, subtracting this outlier brings the average down to three elements per 190 elements that exhibit hysteresis merely 1.5 %. The individual yield for wafer TH1_20220322_01 is 93 % and for wafer TH1_20220322_04 it is 87 %. In conclusion, a robust and stable device with a high yield.

5.6 Discussion: Vertical short circuits

For both linear and row-column elements dark spots with a surrounding lighter halo have been observed in the bottom electrode metal from backside microscope inspection. As shown on Fig. 5.5 for linear elements and Fig. 4.20 for row-column arrays these dark spots are observed primarily at the CMUT cells and not at the connecting wires.
A disadvantage of the row-column addressing scheme is that a vertical short affect both the row and the column element and any other elements that may be connected to either one, accelerating the complexity and consequence of these vertical shorts immensely.
The RC16+16 array, mentioned in subsubsection 4.3.1.4, has 7 short circuits caused by dark spots in 7 different cells verified with impedance measurements and backside microscope confirmation. The gold bottom electrode area is $16 \times 676\,644\,\mu m^2$. Calculating the density gives 7 particles/16 $\times 676\,644\,\mu m^2 = 65$ particles/cm^2. The RC16+16 array consists of 16×16 linear elements which have 36 cells per sub-element, which is a total of 36 cells $\times 16 \times 16 = 9216$ cells where 7 dark spots are found to cause short circuits. Converting this into a percentage of short-circuited CMUT cells yields 0.08 %. These 7 short circuits or 0.08 % shorted cells affect 7 columns and 6 rows which resulted in 40 % shorted elements in the RC16+16 array. A small overview is seen in Table 5.5. This proves how 7 defects in 9216 cells can render almost half of the elements unusable. Thereby, elucidating the immense challenge and complexity of scaling two orders of magnitude to reach the goal of a defect-free RC1024+1024 with one million cells.
Comparing this with the linear arrays where the same procedure of measuring short circuits from top to bottom elements has been proven to have a direct correlation with dark spots with a discoloration halo of the bottom electrode. The linear element has 36 cells and 16 sub-elements with 1 dark spot being the causality of the short circuit corresponding to 0.17 % of the cells.

To determine the root cause of these damages, demonstrated and discussed in subsubsection 4.3.1.3 and subsubsection 4.3.1.4, a range of experiments and studies are

Table 5.5: Summary of percentages and dark spots/particle density.

Description	Percentage
Shorted cells in RC16+16 array	0.08 %
Shorted cells in linear array	0.17 %
Particle density (particles/cm^2)	65

to be conducted. Plausible hypotheses include solid-state diffusion which occurs at lower temperatures or Si-Au eutectic bonding. The influence of the bonding voltage is yet to be determined. The experiments can be divided into individual studies to investigate the phenomenon causing the gold to bridge the vacuum gap and penetrate the oxidized silicon nitride layer entering the poly-silicon top plate.

1) First of all a variety of metals including gold, which should satisfy the ωRC-design criterion and exhibit smooth thin films, should be tested as bottom electrodes bonded and examined with backside microscopy to locate any defects to the metal. One such possible metal is Molybdenum, Mo, with a resistivity of 5.34 µΩcm on the order of gold and smooth films [93]. Molybdenum deposition is possible with both e-beam evaporation and sputter deposition and could be etched with ion beam etching. Considering the scaling prospects, molybdenum bottom electrodes of 250 nm can facilitate an RC512+512 CMUT with 86 % of the signal preserved at the end of the element. The eutectic bonding of Mo-Si is a binary system with several phases and the lowest eutectic temperature is approximately 1400 °C and the second transition temperature at 1900 °C [94, 95]. Another low-resistivity metal to be reconsidered is aluminum as aforementioned the implementation of a 30 nm titanium diffusion barrier layer showed promising results for further studies. A higher eutectic point of Al-Si is found at 577 °C [96] which should not interfere with anodic bonding at 350 °C, whereas the eutectic point for Au-Si is 363 °C. Finally, chromium could be a viable intermediate step before the long-term goal of an RC1024+1024 chip. Despite this higher resistivity a higher eutectic point of 1390 °C is advantageous [97]. The metal particles on the as-deposited metal are believed to be the precursor of the observed defects shown in Fig. 4.4 as they resemble the dark spots with discoloration recently correlated with the top-to-bottom short circuits in subsubsection 4.3.1.4.
2) Wafer bonding should be performed, that is anodic bonding without the applied bias while maintaining the temperature of 350 °C and tool pressure of 5×10^{-3} mbar to determine the effect of the applied bias.
3) The temperature should be decreased and tested in a range from 200 °C to 300 °C during bonding. Usually, anodic bonding is performed at elevated temperatures between 300 °C to 500 °C and polarized from 100 V to 1500 V [59].
4) Different bonding pressures should be tested.
5) Diffusion-inhibiting layers, preventing the gold from entering the poly-silicon top plate through the oxidized nitride layer, should be investigated. Two schemes are possible, either deposited on top of the bottom electrode or implemented in the top wafer stack. One possibility for the bottom electrode is titanium wolfram, TiW, which has proven efficient in preventing the formation of Au-Si eutectic bonding [98]. TiW has previously been explored as a bottom electrode material in this research group for anodic bonding and has proven compatible with the fabrication process and can be etched with the IBE tool, an advantage of a physical etching technique during process optimization is the flexibility. For the configuration utilizing an inhibiting layer as part of the top wafer, silicon dioxide has been shown to block Au-

Si eutectic. This is consistent with our own observations of these damages occurring at the openings of the contact pads i.e. where the oxynitride has been removed as seen in Fig. 4.18. However, this observation is not conclusive as the damages also emerge where the poly-silicon is covered with a 200 nm oxynitride layer.
6) All of the above should be performed as anodic bonding, where the applied bias should be varied in a range from 200 V to 600 V. The reason for trying to make it work with anodic bonding is to utilize the viscosity reflow of the glass that allows for the inclusion of particles to be immersed into the glass and obtain a hermetic seal despite particles at the bond interface. This is a distinct characteristic of the anodic bonding process where the electrostatic pressure combined with the reflow of the glass below the strain point of 515 °C facilitates the incorporation of sub-micron particles. This is an advantage, as the DTU Nanolab Cleanroom is ISO certified to be a class 100 cleanroom in the laboratory rooms containing the wafer bonder, and a class 10 cleanroom is recommended for ideal bonding conditions.

Au-Si eutectic bonding

The FIB-SEM characterization revealed holes or large voids in the top poly-Si plate where gold was present, see Fig. 4.20. In Au-Si eutectic bonding voids or craters are observed to form for Au/c-Si (crystalline silicon) and not Au/a-Si (amorphous silicon), as reported by [99], shown for Si (100) comprised of Si (111) planes. Chen et. al. explains that the voids occur due to a density mismatch between Si and Au(Si) liquid alloy of 2.33 g/cm^3 and 18.64 g/cm^3, respectively, as Si dissolves into Au forming the voids. The top plate in the CMUT is an LPCVD polycrystalline-silicon, which has (110)-textured columnar grains, hence it is not completely crystalline however this could explain the voids found in FIB-SEM seen in Fig. 4.21.

Au-Si diffusion bonding

The findings presented in the dissertation on "Eutectic and Solid State Wafer Bonding of Silicon with Gold" and article [98, 100], presented that already at room temperature as-deposited Au/a-Si show interdiffusion between the Au and a-Si layers for the Au/a-Si couple after two weeks of storage. Samples with as-deposited Au/a-Si were annealed at 250 °C, 300 °C and 350 °C for 10 min, 20 min and 30 min. SEM characterization proved that the inter-diffusion of Au/a-Si increases with increasing anneal duration and temperature. For our samples, the gold somehow gains access to the poly-silicon. The anodic bonding performed in this fabrication process is at 350 °C for approximately 50 min, considering the findings of [98] the interdiffusion is evident as the entire 2 µm amorphous silicon layer was consumed in half an hour annealing at this temperature and our top plate is 2.3 µm.

5.7 Chapter summary

A comprehensive electrical characterization of both linear and row-column arrays of the two RC190+190 wafers combined with illustrative depicting of the observed phenomena and CMUT characteristics was explained. This extensive assessment of the electrical performance especially of the RC190+190 allows evaluation of the array prior to probe assembly and to determine the best-performing array to be integrated into the prototype probe. The following chapter briefly explains the probe assembly procedure as well as impedance measurements and preliminary acoustic

measurements. Furthermore, the important discovery of vertical short circuits was discussed. This issue poses a huge challenge as the 0.08 % short-circuited cells can render almost half the elements non-functional and potentially determine whether or not row-column arrays are realizable if these are not eliminated.

Chapter 6

Probe assembly

This chapter describes the process of mounting, wire bonding and casting the RC190+190 chip into a prototype ultrasound probe which is a novel platform that allows the interchangeable nose pieces that facilitate rapid prototyping and characterization between the transducer chips. Impedance measurements are performed after wire bonding and preliminary acoustic measurements were performed after the probe assembly and are presented.

6.1 Introduction

The prototype probe, acoustic stack and assembly procedure, is a first of its kind and was designed and developed by Kasper F. Pedersen and to some extent described in [67]. To provide an understanding of the probe assembly, the results from this assembly are included in this work with permission from Kasper F. Pedersen. The mounting and casting process of the RC190+190 array is performed at the MEMS lab by postdoc Rune S. Grass and Kasper F. Pedersen. Gluing the RC190+190 array chip to the Chip Carrier Board (CCB) was done with a combination of two types of glue: Structalit 5604 (heat-curing) main adhesive and Dymax 630-T (UV and heat curable) for fixating and aligning to the center of the chip using a Scorpion / ARP-1200S rework station. When the glue has cured the RC190+190 chip is ready for wire bonding.

6.2 Wire bonding

Accordingly to the higher yield and performance of wafer TH1_20220322_01, see Table 5.4, the 4 RC190+190 arrays were diced out for wire bonding and subsequently mounted in the prototype probe. All wire bonding was performed in our MEMS research laboratory utilizing the TPT HB100 wire bonder by my colleagues, Ph.D. student Kasper F. Pedersen and postdoc Rune S. Grass. Prior to wire bonding any of the arrays, three RC16+16 arrays (TH1_20220322_01_CRC16N_r1c1, r1c2, r1c3, and r2c1) were initially mounted on different test PCBs (Lollipop v2.1). This was done to conduct initial electrical impedance measurements for pre- and post-PDMS casting comparison, as well as to determine suitable wire bonding parameters with a desired pull strength of approximately 5-10 grams. Wedge bonding was utilized for the bonding process, and overall, there were no significant issues encountered, except for the occasional formation of wire tails during the initial bond to the PCB gold pad. Any missing bonds were re-bonded when necessary.

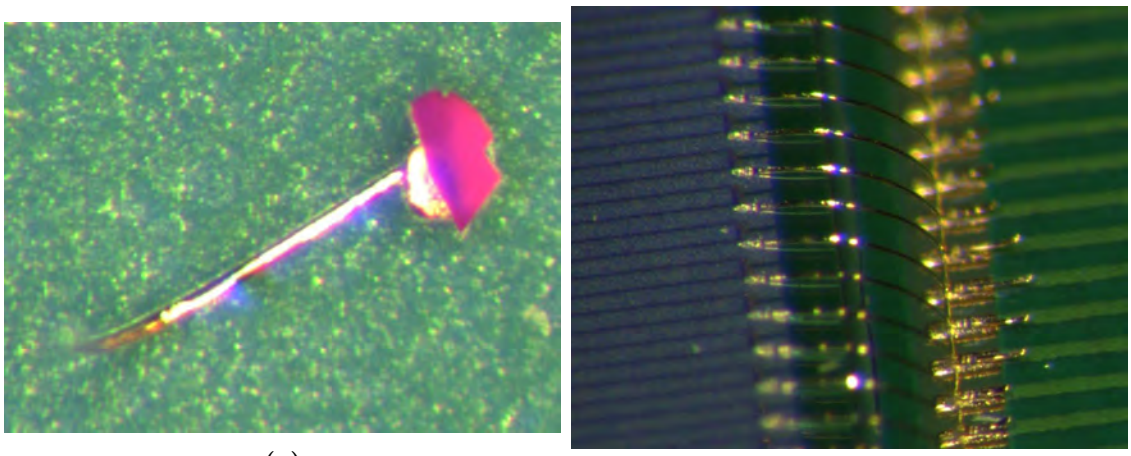
The initial array subjected to wire bonding was the RC4 chip, with electrical parameters seen in Table 5.4. At first, the same set of parameters utilized for the RC16+16 arrays was employed, including the ultrasonic power and tool force. Several bonds were tested on the top electrode pads, proving successful without any issues. The average pull strength was measured at 10.65 g for the even rows and 9.73 g for the odd rows, which is above the standard. However, the wedge bonds failed to adhere to the bottom electrode pads on the chip.

Attempts were made to address the adhesion problems by adjusting the ultrasonic power and force within the ranges of 70-100 and 170-210, respectively. However, these adjustments failed to resolve the issue. Bonds did not adhere at lower power levels, while higher levels caused damage to the pads, resulting in the tearing off of the metal and a section of the nitride beneath the electrode pad along with the failed wedge bond. It was speculated that this issue stemmed from a weak anodic bond between the oxynitride and the borosilicate glass wafer as seen in Fig. 6.2. The presence of the more rigid poly-Si layer on top of the nitride mitigated this effect on the top electrode pads. Due to the extensive damage to the bottom electrode pads and the unsuccessful annealing test in the furnace, this RC4 chip was abandoned.

The RC1 chip was selected for a second attempt at wire bonding. The bonding process for the top electrode pads proceeded without major problems with wedge bonding as on the previous RC4 chip, with only a few unsuccessful bonds that couldn't be repaired despite multiple re-bond attempts. However, the bottom electrode pads presented challenges again, and it was initially difficult to identify suitable parameters for wedge bonding. As an alternative approach, ball bonding and bump bonding, along with stand-off stitch (SOS) or wedge bonding, were experimented with after conducting tests on other RC16+16 arrays. This involved significant calibration of the ball bonding tool and the formation of the bonding balls.

Initially, an alternative approach was attempted by placing the bump on the chip pad before performing wedge bonding, in order to enhance the adhesion of the wire bond to the contact pad and dissipate the energy over a larger area and hopefully not tear the pads as observed previously. However, this method resulted in a high failure rate, with the wedge tool frequently lifting off the bump and causing tear and delamination of delicate pads due to the sideways motion involved in bump placement. On the other hand, ball bonding starting from the PCB pad showed a higher success rate, but occasional sliding off of the balls from the PCB pad (despite using a fine-pitch ball bonding tool) led to the destruction of the chip pad during the second bond. The most effective approach, although resulting in tall, uneven, and taut wires, involved starting the ball on the chip level and completing it on the PCB pad. This method minimized sideways motion and avoided placing excessive stress on the chip pad as the pull force is spread to a larger area during the formation of the wire bond in order to preserve the bottom contact pads. However, a drawback was observed as the wire tended to slide off the PCB pad or adhere poorly due to the design of the PCB, which featured raised contact pads without a soldering mask in between. The ball bonding method also resulted in torn contact pads, see Fig. 6.1 a).

In a final attempt, wedge bonding was revisited, this time starting from the PCB pad, and a different parameter space was explored. The temperature was increased from 110 °C to 115 °C, and the ultrasonic power and force were adjusted to 100 ultrasonic power and 200 Force unit specified by TPT for the second bond. Surprisingly, this adjustment enabled the successful bonding of the previously problematic



(a) (b)

Figure 6.1: A torn ball bonded bottom electrode contact pad a) showing the ball bond with the purple-colored oxynitride underneath the pad. The successful wedge wire bonding of the top electrodes is shown in the image seen in b).

bottom electrode pads, even those that were heavily damaged and torn as seen in Fig. 6.2. A broken off wire bond can be seen The tail mode of the bond was set to table tear to avoid stressing the bond on the chip. Some of the previously ball-bonded connections were replaced with wedge bonds. Through meticulous microscope inspections and multiple re-bonding attempts, nearly all the bottom electrode pads, except for 5, were successfully bonded.
To address short circuits between neighboring pads and between pads and apodization regions, attempts were made to sever the connections whenever feasible. Handheld needles and probe needles were utilized for this purpose. However, in cases where there was a risk of damaging the contact pad or element, the short circuits were left intact to avoid potential loss. An image of the successful wire bonding is shown in Fig. 6.1 b) for the top electrodes.

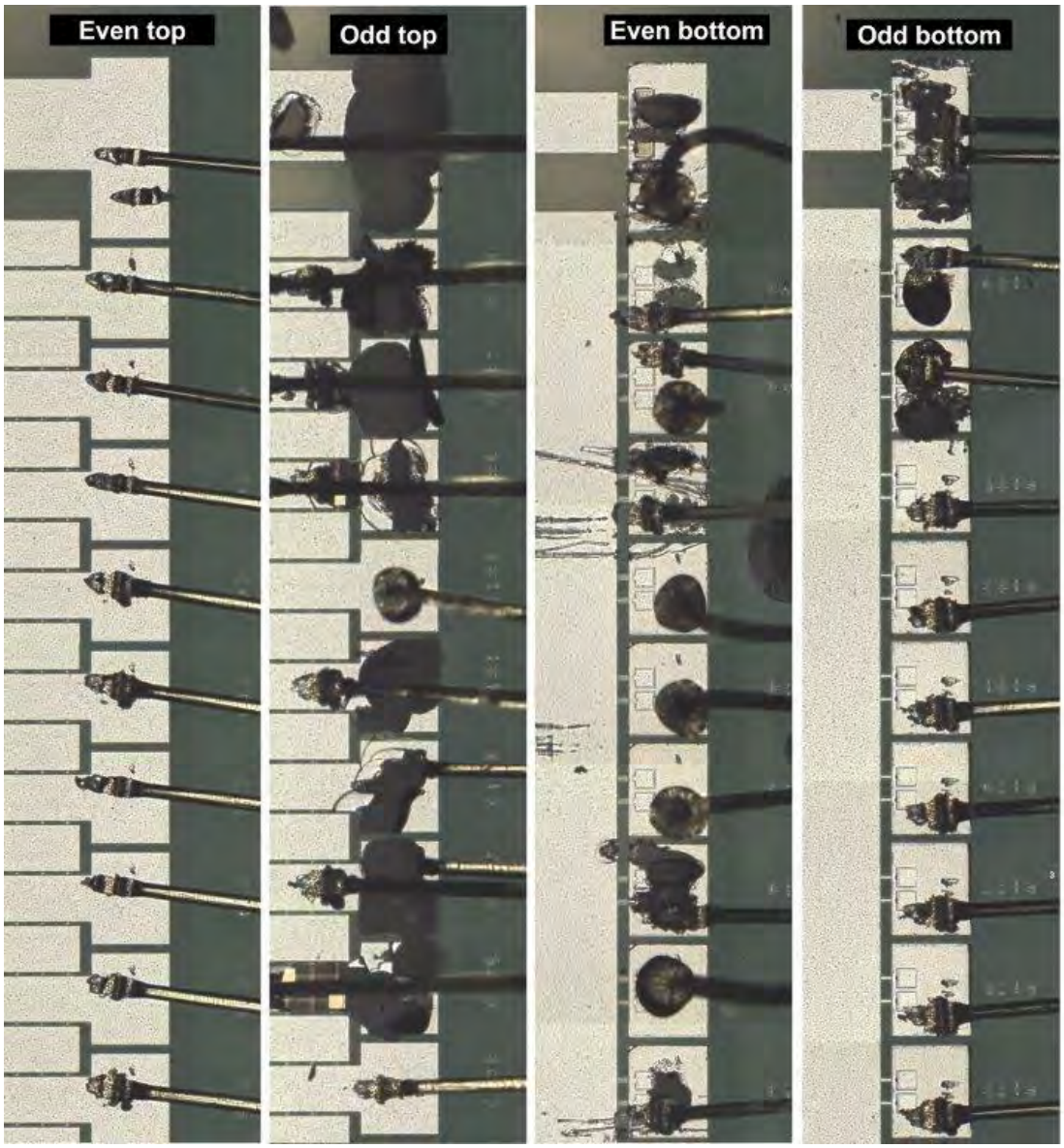


Figure 6.2: Microscope images after wire bonding all taken at the apodization contact for RC190+190 array, RC1 of wafer TH1_20220322_01. In the order from right to left: Even top electrodes, showed the best bonding pads all placed with wedge bonds and then odd top electrodes, displaying the difficulties in finding the best wire bonding parameter as both wedge bonds, ball bonds and wedge on ball bonds are demonstrated. In odd top electrodes, the oxynitride has broken off in several places where wire bonding has been tried, indicating a poor adhesion between the borofloat glass substrate and the dielectric oxynitride. Similarly, for the even and odd bottom electrodes, various different bonding techniques and parameters were tested. At the even bottom electrodes, a ball bond with a missing tail can be observed.

6.3 Packaging

The final wire bonded RC190+190 is seen in Fig. 6.3 a) and the probe assembly is commenced. The CCB is the electronic board along with the frame for the Electromagnetic interference (EMI) shield incorporated later. Anywhere where the primer or PDMS is unwanted is masked during the casting process. And if not specified curing is done at a raised humidity at 45 °C. The mounting and casting process can be divided into four main steps, which are briefly outlined in the lists below. Accompanying images are provided for illustrative purposes.

Step 1: First layer of PDMS casting

- Priming of the surface of the array and the inside of the frame with DowsilTM 1200 and curing for 1 h
- Mixing of the PDMS in a centrifuge to minimize bubbles
- Pouring a layer of PDMS into the inside square of the EMI frame
- Degassing of the PDMS inside a vacuum chamber ≈10 min
- Leveling of the PDMS to the frame using a flat PMMA sheet and clamps
- The pressure is kept for 20 h at an elevated temperature of 45 °C

The first layer of PDMS casting is completed and shown in Fig. 6.3 b).

Step 2: EMI shield

- Priming on top of the first PDMS layer and on the frame, see Fig. 6.3 c)
- Mixing of the PDMS in a centrifuge to minimize bubbles
- Aluminum film of 1 µm is placed on a PMMA carrier for support and is primed
- PDMS is poured on top of the first layer in a strip along the edge, see Fig. 6.3 d)
- The PMMA block with the aluminum film is carefully placed at that edge and then gently applying pressure forming a continuous wavefront of PDMS towards the other side of the array
- Again, pressure is applied for leveling by PMMA sheets and clamps, see Fig. 6.3 e) for 20 h

Step 3: Mounting in nose piece for prototype probe

- Any excess EMI film is cut off using a scalpel, along the outside edges of the area where the primer was applied
- Apply a layer of Loctite 3863 conductive glue along the edges of the EMI film, then cured for 30 min, see Fig. 6.3 f)
- For increased adhesion the PPSU nose piece is abraded along the inside ledge
- A glue Loctite 480 (cyanoacrylate) is applied to the ledge, it cures quickly
- Then the CCB is quickly placed inside the nose piece

- PMMA sheets and screws are used to fixate the CCB while the glue is curing
- After partially curing another thin layer of Loctite 480 glue is applied between the edges of the CCB and the nose piece, curing another 12 h, see Fig. 6.4 a)

Step 4: Last PDMS layer
This step is essentially the same as described in step 1, the first layer of PDMS where the differences are

- A dam of Kapton tape is formed to keep the PDMS from spilling onto the PPSU, see Fig. 6.4 b), then priming
- PDMS is poured and degassed (even more important)
- A thick non-flexible plate of PMMA is carefully placed at that edge at an angle of 40° and then gently applying pressure forming a continuous wavefront of PDMS towards the other side of the array
- To keep the pressure Kapton tape is tightly wrapped along both axes of the nose piece and furthermore fixed with clamps
- The last curing at 45 °C for 12 h
- Demoulding the PMMA plate and cleaning up the finalized nose piece, see Fig. 6.4 c-d)

The nose piece is finalized and can be mounted in the prototype handle, see Fig. 6.4 e-f). The prototype handle consists of a body with amplifier boards and two cables that can couple to the commercial BK medical scanner and the experimental research scanner, SARUS located at CFU.

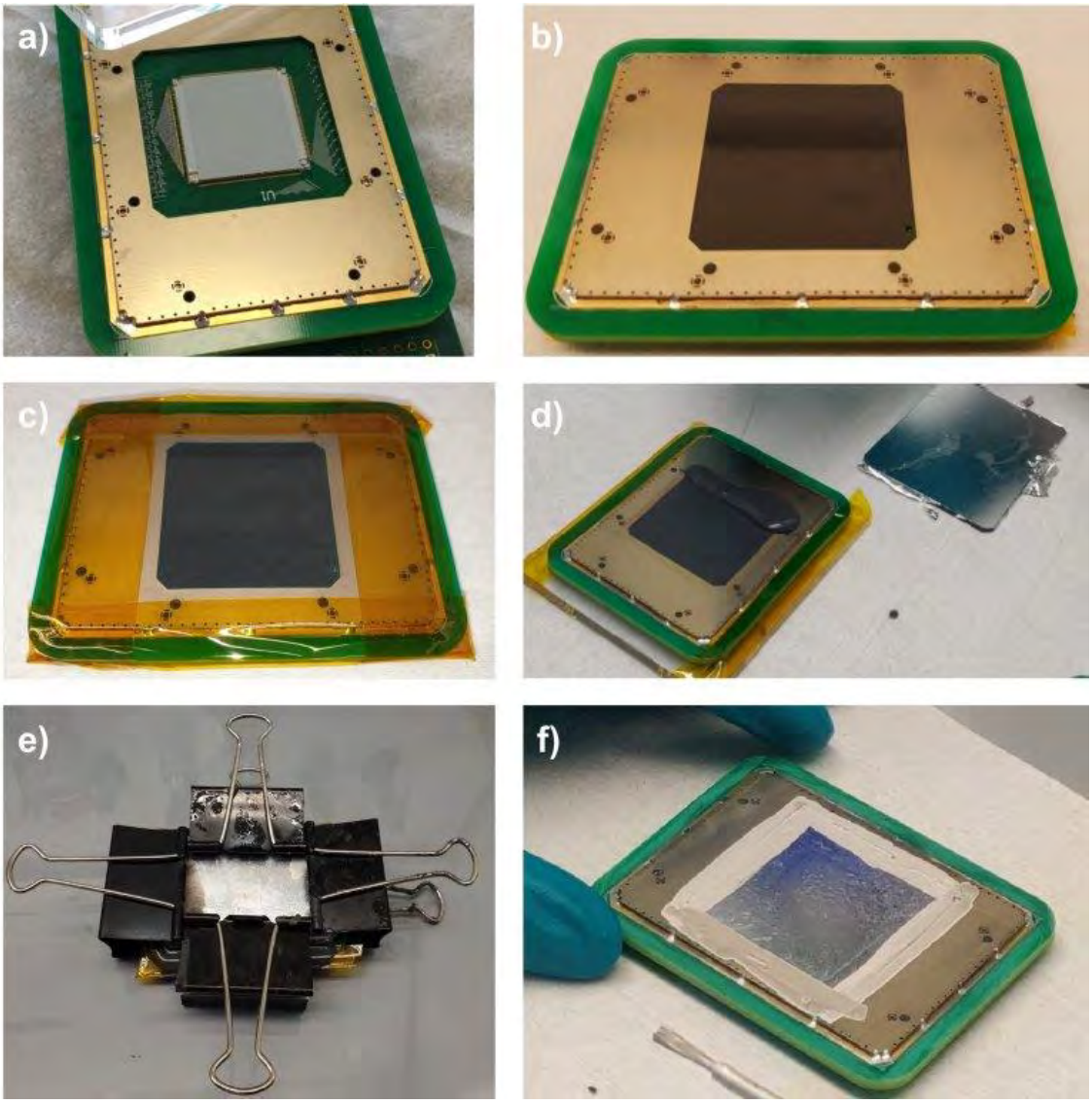


Figure 6.3: a) Wire bonded RC190+190 array to CCB and b) first layer of PDMS. In c) masked and priming of PDMS followed by c) where the first stripe of PDMS is poured and the aluminum shield is prepared. Clamps and PMMA plate in e) leveling while curing and f) attaching the shield with conductive glue to the frame.

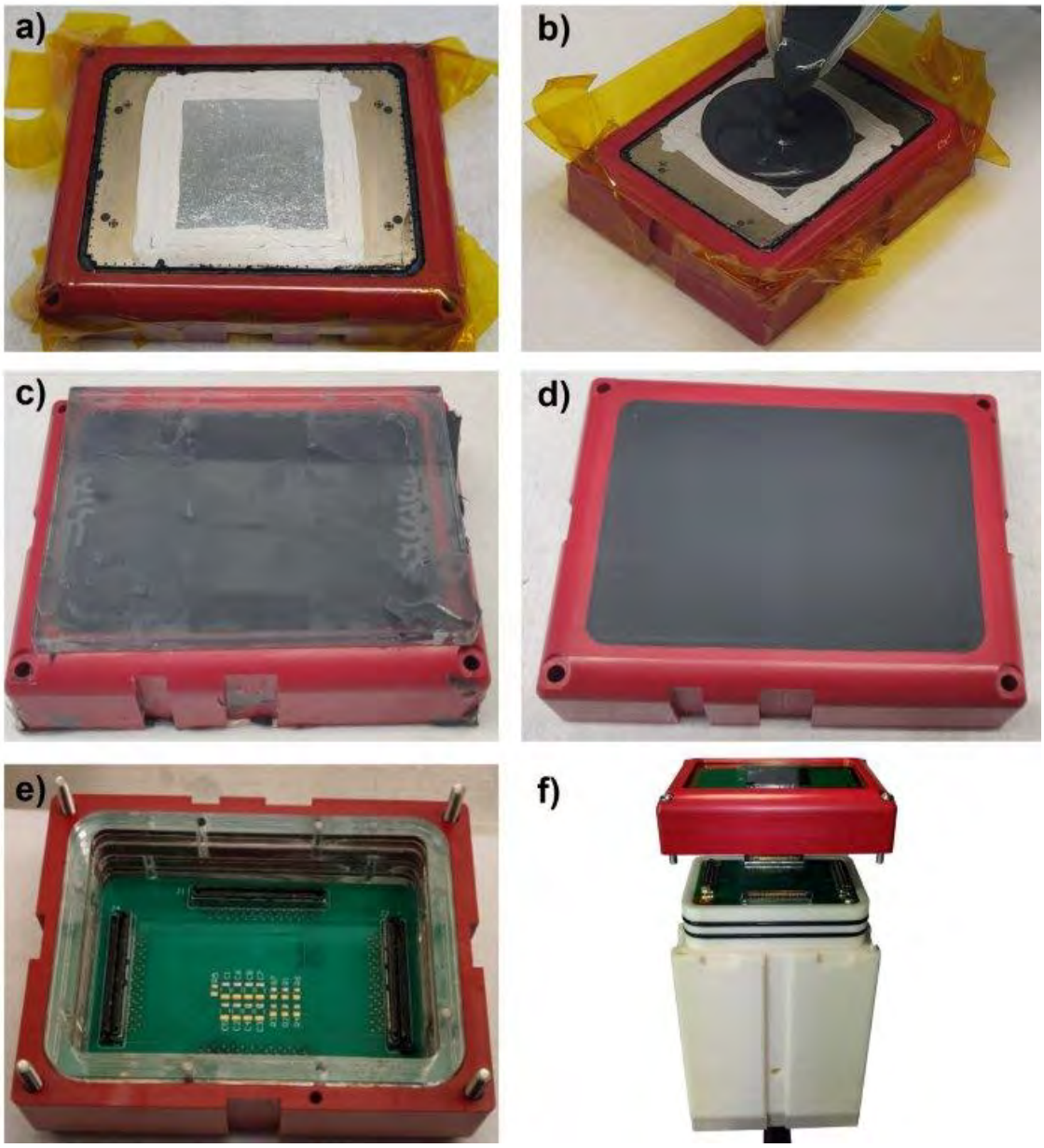


Figure 6.4: CCB is mounted in the nose pieces and secured and sealed with Loctite glue at the edge. The second layer of PDMS is poured b) and leveled and cured in c). The nose piece mounting and casting is finalized shown from the front in d) and backside with connectors in e) and can be attached to the prototype probe handle as shown in f).

6.4 Impedance measurements

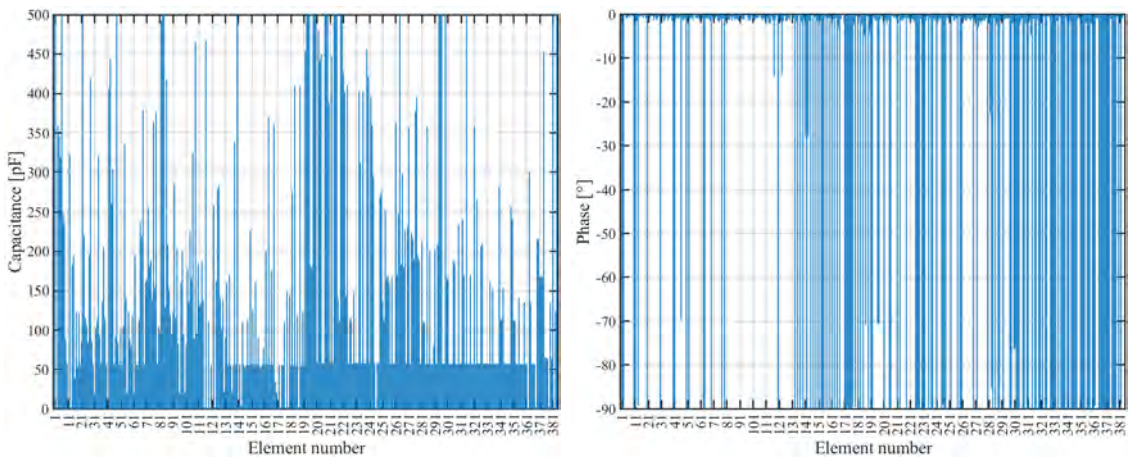
After wire bonding the RC190+190 array, RC1 and mounting to the CCB it was measured in the probe station. The CCB has four connectors on the backside complementary of the odd and even number of rows and columns. Through the EMI frame and connector pins, all the fx rows can be grounded via the chuck of the probe station while measuring with the other DC probe on the individual column elements. Impedance measurements were conducted from the top to the bottom electrodes. Initially, all rows were connected together, and the impedance between each column element and the rows was measured. Following this measurement, the same procedure was employed to characterize the impedance of each individual row element. From the impedance measurement, Z-f the capacitance, phase angle and resistance of each individual element is characterized and sorted by the criteria:

- Low $R_\mathrm{p} < 10\,\mathrm{k\Omega}$ and low $C < 5\,\mathrm{pF}$ = non-working element
- Low $C < 5\,\mathrm{pF}$ = floating element = not connected element
- High phase angle $> -80°$ = not a capacitor
- Working elements have none of the above
- Medium $R_\mathrm{p} > 10\,\mathrm{k\Omega}$ = might be a capacitor, working element
- High $C > 120\,\mathrm{pF}$ = neighboring short circuit or shorted to apodization = working element

Consequently, 38 columns (bottom elements) and 74 rows (top elements) were categorized as working elements. This is a considerable reduction compared to the sorting based on the IV, CV and Z-f measurements performed prior to wire bonding which found 186 columns and 168 rows were working (see Table 5.3), however, these were measured utilizing the neighbor-to-neighbor scheme as described in Section 5.5. The impedance measurements carried out after wire bonding are true top-to-bottom measurements. An overview of the categories can be seen in Table 6.1 and bar plots of the capacitance and phase angle are seen in Fig. 6.5. As expected the columns have a larger amount of short-circuited elements of 135 compared to the rows of 94. The capacitance level at 56 pF is observed for the working elements in Fig. 6.5 a) and higher capacitance values are attributed to orthogonal short circuits as explained by the amount of 0° phase angles in b). While some of the observed damages can be attributed to incidental collateral effects resulting from the challenging wire bonding procedure, it is evident that the remaining challenge lies in the top-to-bottom short circuits as described in subsubsection 4.3.1.4.

Table 6.1: Sorting based on impedance measurements on the wire bonded RC190+190 array RC1.

Condition	**Ok**	**Low Rp**	**Low Cp**	**N-N short**	**High C**
Rows	74	94	5	17	0
Columns	38	135	16	0	1



(a) (b)

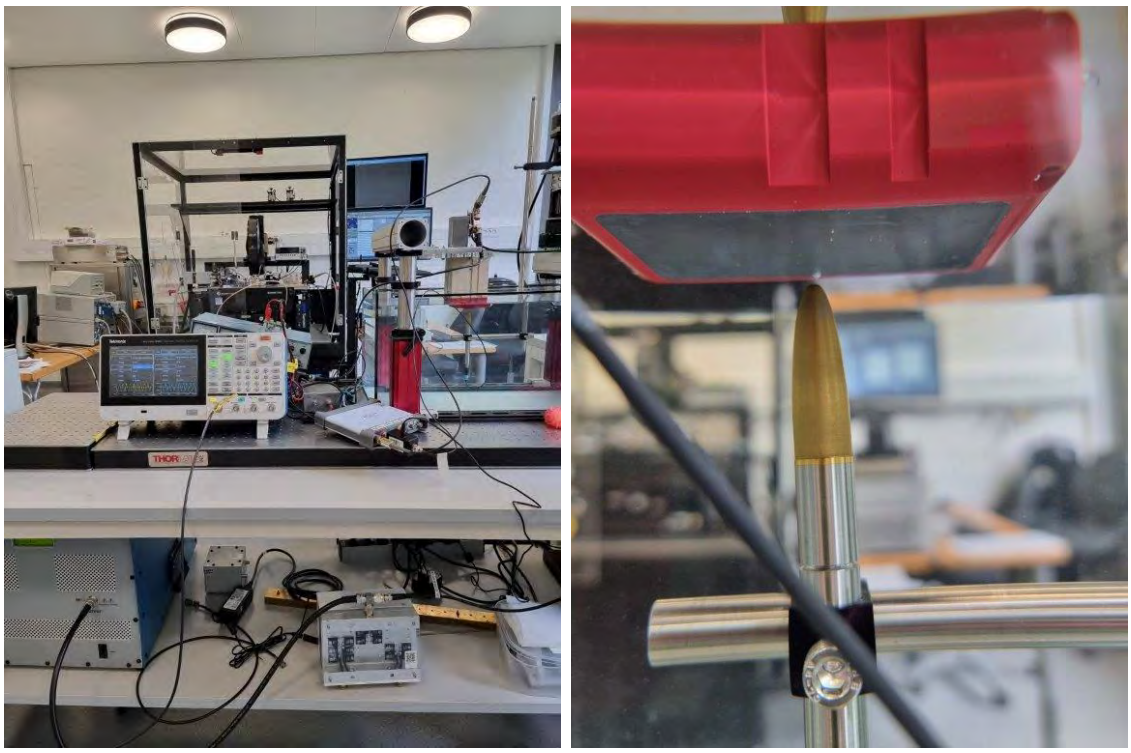
Figure 6.5: Bar plots from the impedance measurements on the RC190+190 array RC1 showing capacitance a) and phase angle in b). Element no. 1-192 are row and no. 193-184 are columns. For working elements the capacitance is 56 pF as observed in a) accompanied by a number of higher capacitances that are short-circuited elements explained by the large number of phase angles around 0° in b).

6.5 Acoustic measurements

Recently, the prototype probe was finalized and this section presents the initial results from the acoustic characterization. After wire bonding, mounting and casting of the acoustic stack into the nose piece implemented into the prototype probe acoustic measurements could be executed on the RC190+190 array, RC1.
To verify the acoustic performance one of the working elements initial measurements were performed in our new experimental setup seen in Fig. 6.6. The surface of the nose piece containing the RC1 chip was immersed in a water-filled tank with the Onda HGL-0400 hydrophone placed 1.5 cm beneath the probe, see Fig. 6.6 b). The prototype probe is currently not able to connect to the signal generator and oscilloscope used for data sampling in the MEMS lab. Therefore, the prototype probe is used without the amplifier boards and only the nose piece.
A 10-pulse sinusoidal excitation signal was generated with a 100 V DC and a peak-to-peak 60 V AC on the row element 95 and the transmitted signal from the RC CMUT element can be seen in Fig. 6.7. The amplitude of the impulse response is 5.9 mV.
For the same element, row 95, the frequency was varied from 2 MHz to 20 MHz with a constant bias of 100 V applied. This was maintained by varying the gain in the signal generator connected to a high-voltage amplifier to keep a constant voltage at during the frequency sweep. These measurements were used to plot the frequency spectrum of the single element seen in Fig. 6.8. The frequency response shows a peak frequency at approximately 12.5 MHz and a center frequency was calculated to 10 MHz. The fractional bandwidth was calculated using

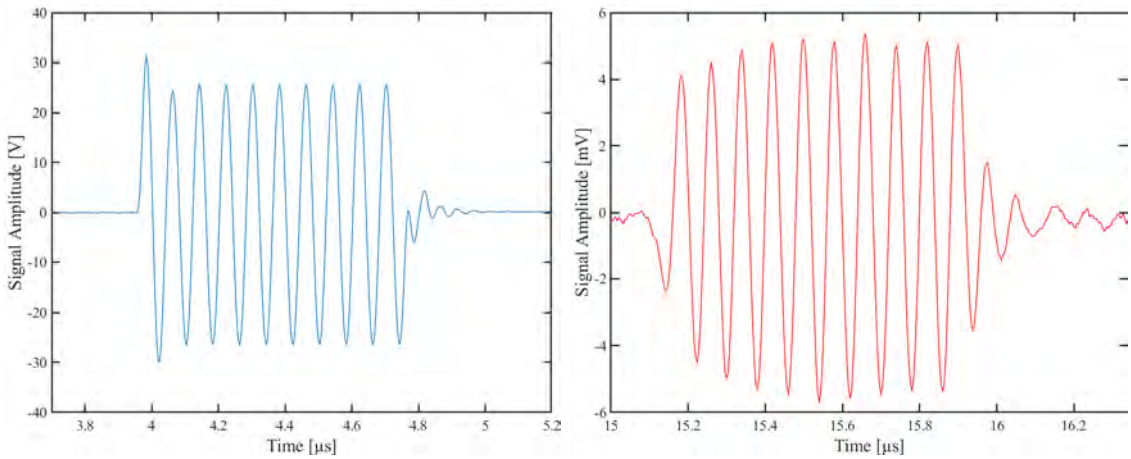
$$f_{\text{rel.BW}} = \frac{f_{\text{-3dB,1}} - f_{\text{-3dB,2}}}{f_{\text{c}}} \times 100\% \tag{6.1}$$

to $F_{\text{-3dB, peak}} = 30.8\%$ and $F_{\text{-6dB, peak}} = 79.8\%$, and $F_{\text{-3dB, center}} = 137.5\%$ and $F_{\text{-6dB, center}} = 145\%$ for a row element in transmit, see Table 6.2. These measurements are performed on our own experimental acoustical setup due to the poor signal-to-noise observed when trial measurements were performed on SARUS. Consequently, com-



(a) (b)

Figure 6.6: The experimental acoustic setup up in the MEMS laboratory a) with a close-up of the prototype probe nose pieces positioned such that the transducer surface is slightly submerged just below the water surface seen in b) with the Onda HGL-0400 hydrophone underneath.



(a) (b)

Figure 6.7: The excitation signal is seen in blue in a) and the transmitted signal recorded with the hydrophone from row element 95 is seen in red in b). The generated signal is a 100 V DC and a 60 V AC sinusoidal waveform spanning 10 periods. The observed CMUT signal exhibits an exemplary shape and stability.

Table 6.2: Results from acoustical measurements.

	Row 95	**Unit**
Peak frequency	12.5	MHz
Center frequency	10	MHz
Relative fractional bandwidth, peak −3 db	30.8	%
Relative fractional bandwidth, peak −6 db	79.8	%
Relative fractional bandwidth, center −3 db	137.5	%
Relative fractional bandwidth, center −6 db	145	%

paring to previously fabricated CMUT probes measured on SARUS is not a straightforward task and would preferably need to be remeasured on our setup. Despite this, the TH1-A chip, also mounted in the prototype probe, gave a −3 dB fractional bandwidth of 88.9 % for a row element when measured on SARUS [60].
To investigate the pressure distribution along an element the acoustical pressure was measured at a distance of 0.5 cm from the probe surface. Acquisitions were measured manually with a step size of 0.5 mm. The pressure is plotted as a function of step position along the element in Fig. 6.9. The largest at 3 mm is the pressure measured closest to the contact pad and as expected with the largest amplitude. The pressure gradient from the contact pad to the peak at 16 mm at the end of the element, noting the apodization region is not biased, drops from 4.12 MPa to 3.61 MPa. A coarse interpolation between these to peak from the contact pads to the end of the element gives a preserved signal strength of 88 %. All the dips are most likely caused by orthogonal short circuits to the bottom electrode (columns) as described previously.
For the top electrode, a preserved signal was calculated to 99 %, for 1 µm aluminum with a resistivity of 2.7 µΩcm at 8 MHz, the measured attenuation is higher. Nevertheless, this result is solely based on one element. Due to the amount of orthogonal poor-performing and short-circuited elements a uniform pressure distribution can not be obtained. The results are summarized in Table 6.2. Unfortunately, the newly assembled probe was accidentally damaged mechanically during measurement, therefore no further measurements have been performed.

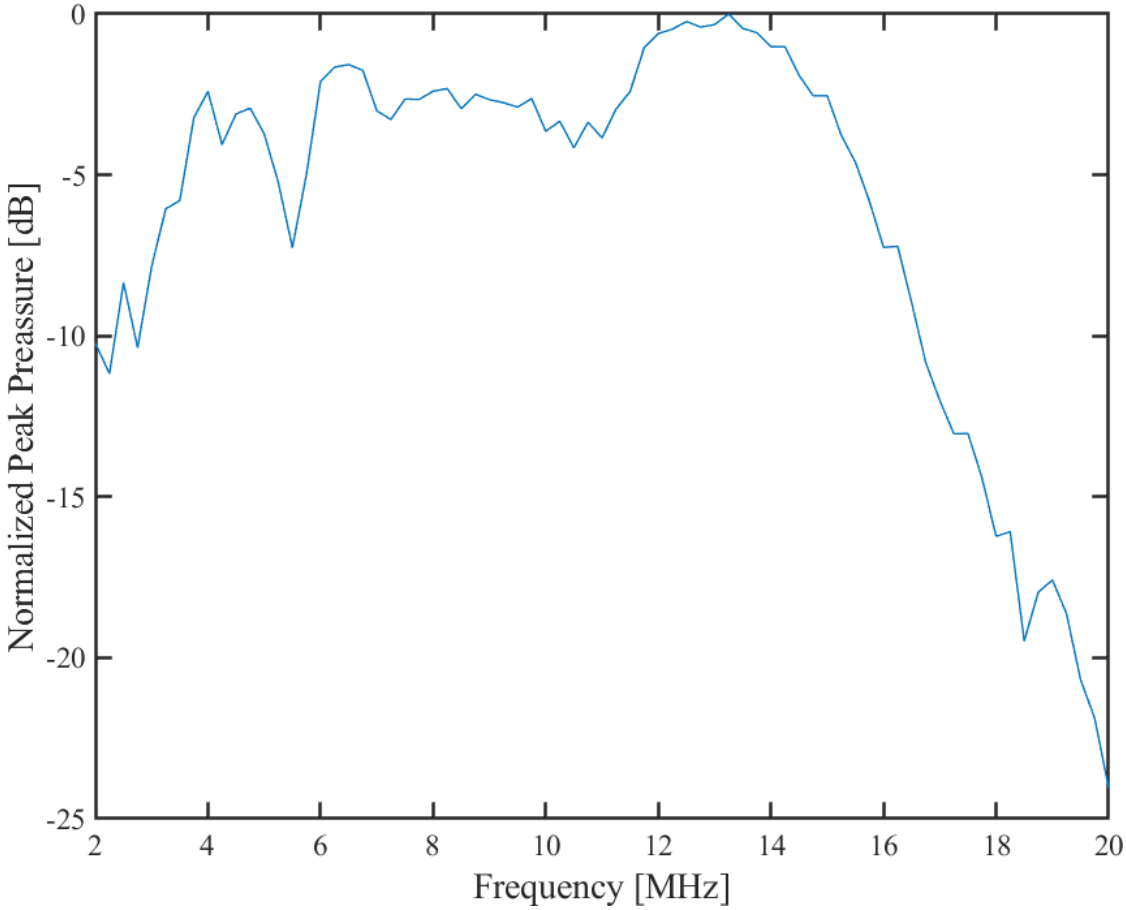


Figure 6.8: Frequency spectrum for the transmission impulse response of row 95 (top element) as captured by the Onda hydrophone. A peak frequency is seen at 12.5 MHz chosen as the peak frequency. The dip at 5.5 MHz corresponds to the substrate ringing of a 500 µm borosilicate wafer and is reoccurring at double frequency.

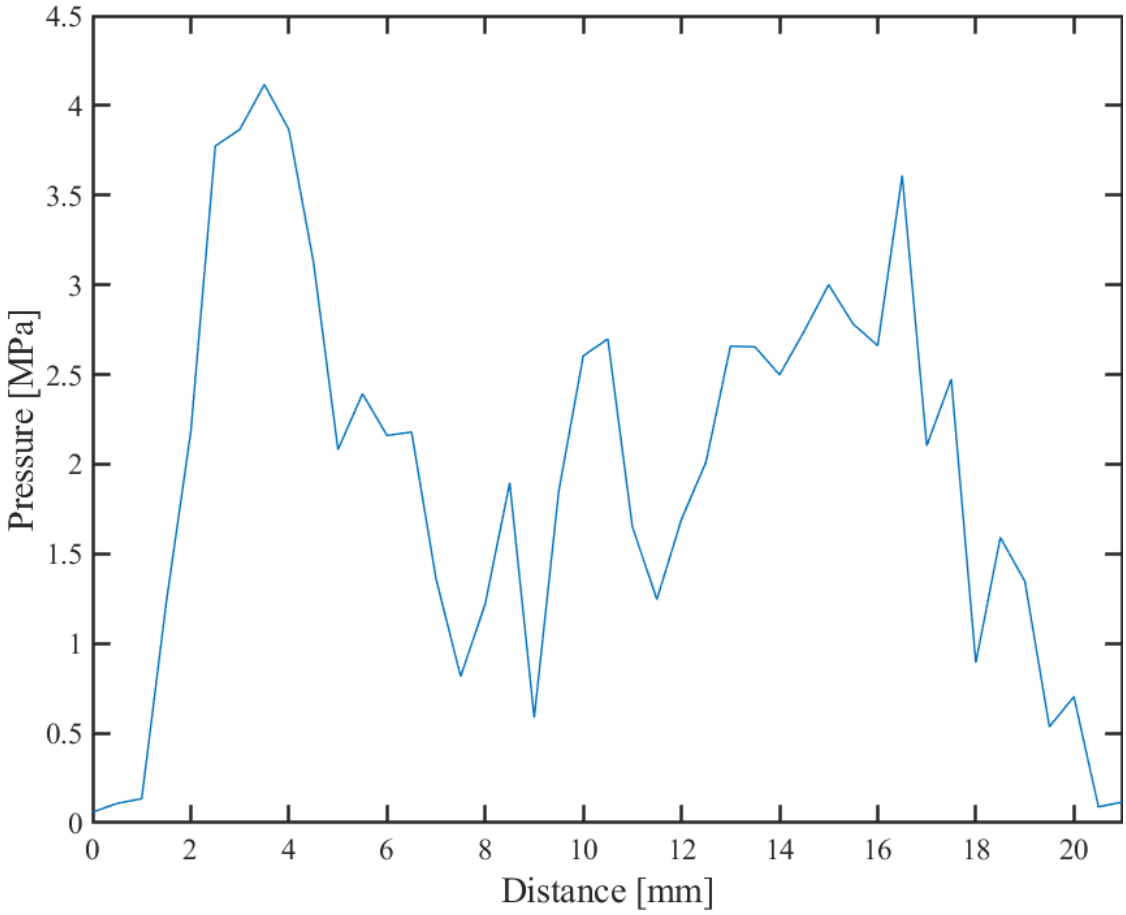


Figure 6.9: Pressure gradient along the row element no. 95 (top element). The contact pad of the element is placed at the distance 3 mm with the largest amplitude, the dips along the element correspond to orthogonal short circuits and the end of the element is at a distance of 16 mm. Disregarding the dips from the orthogonal shorts, the pressure amplitude is estimated to decrease 12 % from the contact pads to the end.

6.6 Chapter summary

The probe assembly, wire bonding, impedance measurements and initial acoustical characterization of the RC190+190 chip RC1 were presented in this chapter. The impedance measurements showed a considerable amount of orthogonally short-circuited elements, which were discussed. The preliminary acoustical measurements of a single row element showed a 10 MHz center frequency with a relative bandwidth of 145 % in transmit. Further acoustic characterization should be performed to investigate the success of optimizing the bottom electrodes according to the ωRC-design criterion. This chapter concludes the part on anodically bonded row-column CMUT arrays.

Chapter 7

3D printed phantoms

7.1 Introduction

This chapter presents the specialized 3D-printed phantoms used to validate the resolution and ascertain the performance of the high-resolution RC CMUT ultrasound probes and algorithms. The phantoms are not commercially available and imperative to reach the goal of the SURE project which is to achieve 3D super-resolution ultrasound in real time facilitated by large-scale RC CMUT probes and advanced imaging algorithms. The phantom fabrication technique is detailed and the two types of phantoms are explained and a novel micro flow phantom is presented.

7.2 Motivation

At the core of the human body lies the vascular system, comprising billions of vessels. The diameter of these vessels varies, ranging from a few centimeters in the aorta down to the smallest vessels, such as arterioles and venules, with dimensions below 100 µm, and capillaries with diameters of 5-9 µm [101]. Angiogenesis, the formation of new blood vessels from existing ones, is a vital and continuous process occurring during normal growth and in response to changing needs in the body. A properly functioning vascular system is essential for the overall well-being of the body. Conversely, disruptions in the microstructures of the vascular system have been directly associated with various disease processes, including cancer, diabetes, Alzheimer's, and Parkinson's disease [102, 103]. While angiogenesis is a completely normal process, it can also indicate underlying issues, particularly when cell proliferation becomes uncontrolled, as observed in cancer growth [104].

Understanding the relationship between cancer and the vascular system can be utilized in cancer treatment. By monitoring microvascular changes, it may be possible to detect the effectiveness of treatment methods sooner, enabling quicker intervention. Similarly, in diabetic kidney disease, diagnosing and treating microvascular changes at an early stage could lead to improved outcomes. Focusing on microvascular changes and their early detection holds the potential for more effective treatments and better outcomes in various medical conditions. This is exactly the goal of the SURE project which aims to develop 3D super-resolution ultrasound imagining of the erythrocytes by developing 2D Row-Column probes and advanced imaging algorithms. However, one of the major challenges in realizing these 3D super-resolution RC probes and algorithms lies in having suitable phantoms for testing and validating them.

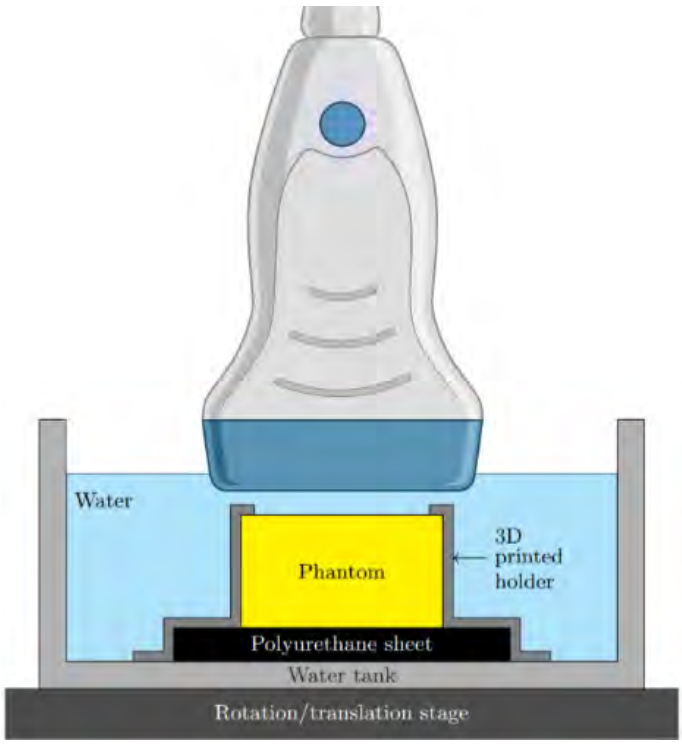


Figure 7.1: A sketch of the experimental setup for testing 3D printed ultrasound phantoms. Sketch partly reprinted from [105].

It is common practice to test ultrasound probes and algorithms on tissue-mimicking phantom structures to validate the resolution and performance before experimenting on animals and humans. The phantom test setup is sketched in Fig. 7.1. Tissue-mimicking phantoms can simulate cysts and blood vessels. The latter are called flow phantoms which emulate blood flow in different vascular structures. The SURE project needs a flow phantom system that allows for well-controlled measurements of super-resolution flow.Super-resolution validation necessitates phantoms where the dimensions are known to micrometer precision. Unfortunately, commercially available phantom systems do not meet these requirements, hence the development of these specialized phantom systems specifically tailored for this purpose was undertaken. It is an extremely complex technology that was developed by former postdoc Martin Lind Ommen during his PhD. A thorough description of the 3D-printed phantoms for super-resolution validation is given in his PhD [106]. During this PhD both flow and novel scatter phantoms were fabricated and a new type of flow phantom for 3D super-resolution ultrasound imaging was designed and realized and will be explained in the following section.

7.3 3D printed phantoms

In order to develop Super-Resolution Ultrasound techniques, stereolithography (SLA) 3D-printed specialized ultrasound phantoms with micrometer specifications were fabricated. The phantoms are printed by stereolithography (SLA), a 3D printing technique that utilizes a liquid resin solidified into the desired pattern through localized illumination. The printer setup can be seen in Fig. 7.2. This process occurs layer by layer to create the specified 3D model. The light source is a light-emitting diode (LED) at 365 nm which is reflected by a digital micromirror device (DMD) to

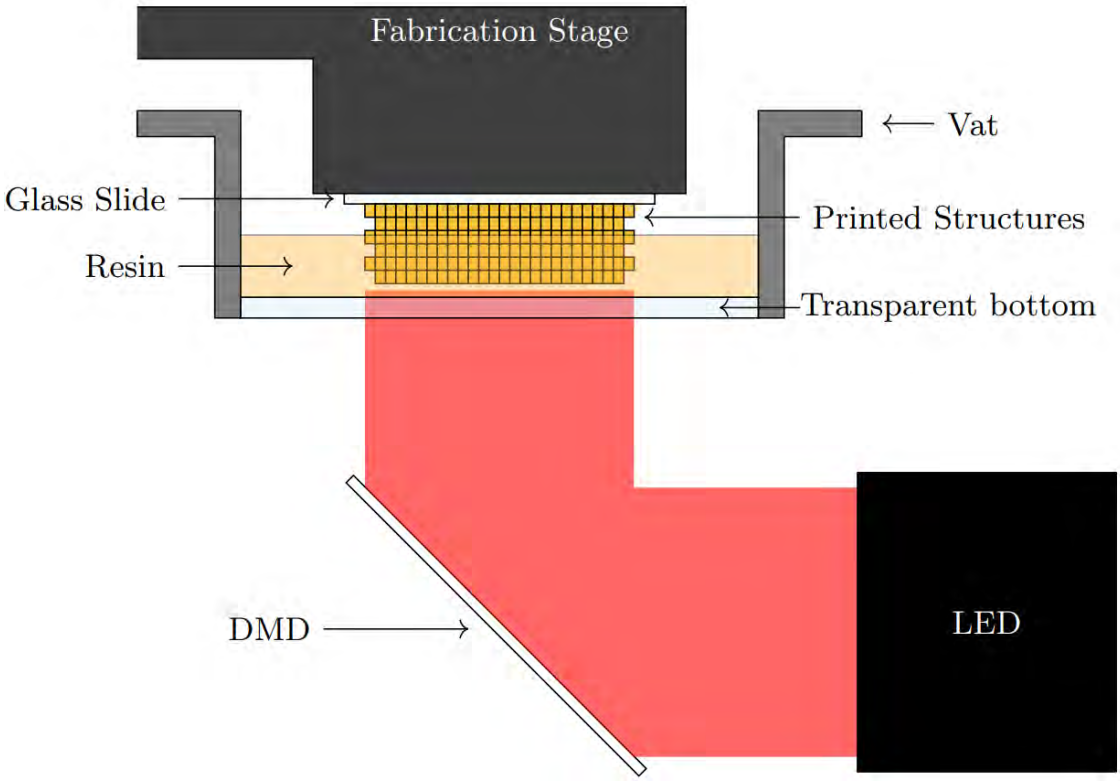


Figure 7.2: Sketch of the 3D printer stereolithography (SLA) setup. An LED emits light that illuminates a DMD. The DMD reflects the light, forming the desired pattern, which passes through the transparent bottom of the printer vat. As a result, the resin in the vat is exposed to light and initiates the cross-linking process of polymerization of the yellow hydrogel phantom. The first layer of the printed structures is cross-linked to the glass slide that is securely positioned on the movable fabrication stage. The process is repeated shown here for six layers. Sketch reprinted from [106].

form the desired pattern through the transparent bottom of a vat. The vat contains the resin, and the structures are printed on a glass slide mounted on the fabrication stage. The DMD has 1920 by 1080 mirrors and a pixel size of 10.8 µm. The glass slide is pretreated with trimethoxysilane to increase adhesion as the phantom is printed upside-down. Prior to printing the fabrication stage is gradually lowered into the liquid resin, leaving a short distance from the vat bottom that determines the thickness of the first printed layer. As the liquid resin is illuminated it undergoes cross-linking and starts to polymerize. Each layer is exposed like projection imaging so when the exposure is finalized the stage is moved upwards 20 µm to match the pixel size and the process is repeated forming multiple layers. The printed phantoms are hydrogels, which are polymer networks containing 75 % water. These are especially useful for ultrasound as most tissues have approximately the same water content [107]. The acoustic properties of the printed phantoms were characterized and determined to have an average speed of sound of 1577 m/s and an average density of 1.045 g/ml and a swelling factor of 2.6 % [106]. They are printed with a voxel size of 10.8 µm × 10.8 µm × 20 µm. The dimensions of the phantom's outer structure measure 21.26 mm x 11.97 mm x 11.97 mm. These dimensions are derived from the original designed size of 20.726 mm x 11.664 mm x 11.664 mm, accounting for a 1.026-factor adjustment due to swelling.
To print the phantom design, the MATLAB code used to control the 3D printer requires the 3D model to be sliced into separate layer (.png) files. To ensure that the printed structure aligns precisely with the slices, manual generation of the .png files and the build lists provides full control over individual slices. This level of control becomes increasingly important as structures become smaller and when aiming to achieve the smallest attainable features. Therefore, MATLAB scripts were developed to create the slice .png files and build lists manually. The SLA 3D printer is owned and developed by Prof. Niels Bent Larsen's research group and is optimized for creating organs-on-chips. The hydrogel is optimized accordingly to be diffusion open for cell cultures to receive nutrients to be transported through vascular-mimicking printed structures. The printing resin is comprised of three components: an aqueous pre-polymer solution, a photo-initiator, and a photo-absorber which are dissolved in DI water. The pre-polymer undergoes polymerization upon local initiation by the light-activated photo-initiator, resulting in the formation of a solid. The selection of the pre-polymer, photo-initiator, and photo-absorber, as well as concentrations are tailored to cell culture as aforementioned [108]. The resin mixture is:

- Pre-polymer, poly(ethylene glycol) diacrylate (PEGDA) 700 g/mol, 200 mg/ml
- Photoinitiator, which cross-links the PEGDA pre-polymers when illuminated at the right frequency - lithium phenyl-2,4,6-trimethylbenzoylphosphinate (LAP), 5 mg/ml
- Photo-absorber, which dictates the layer thickness of the prints - quinoline yellow (QY) 12 mg/ml.

These are all dissolved in Milli-Q water and matched for a layer exposure time of three seconds, which ensures adequate cross-linking of the pre-polymers to the previously printed layers. The photo-initiator LAP is selected based on its water solubility and absorption spectrum that matches the LED. Similarly, the photo-absorber QY is chosen for its water solubility and high extinction coefficient at the specific wavelength used. This choice ensures that the attenuation is appropriately

matched to achieve a slight overlap between the newly exposed layer and the previously exposed layer, resulting in optimal cross-linking. The printing solution is prepared shortly prior to the commencement of 3D printing. Once the phantom printing is completed, it is carefully cut from the cover glass and placed in Milli-Q water to avoid dehydration. Due to the hydrogel's open diffusion properties, the photo-absorber QY gradually diffuses out into the water, coloring it yellow. Furthermore, it is important to cut the phantom from the cover glass as the phantom swells 2.6 % and the first printed layer is fixated to the glass inhibiting the expansion. This may lead to undesirable stress and bending of the phantom, which may be irreversible if it is left on the cover glass for an extended period.

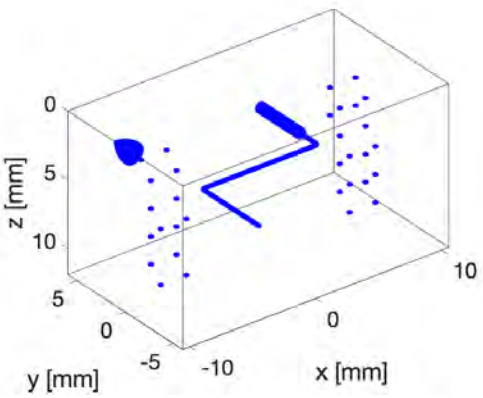
7.4 Flow phantom

Traditional phantom fabrication methods involve using tubes suspended in water and perfusing them with micro-bubble-containing liquids. However, these methods do not offer the level of feature control required for super-resolution ultrasound and have limitations in three-dimensional feature placement. The issue is that the repeatability is questionable as is the position accuracy. The micro flow phantoms developed aim to solve this issue where the exact position and diameter of the channel are known, see Fig. 7.3. A custom MATLAB script was developed to provide precise voxel-level control over all printed models [106]. This capability represents one of the key advantages of the 3D printing technique. This particular flow phantom in Fig. 7.3 has a 205 µm channel width and was used to prove a theoretical model to compensate for the underestimation of velocity in 2D super-resolution ultrasound [109]. In Super-resolution ultrasound imaging the vessel size is often small compared to the resolution in the elevation direction, and tracking algorithms tend to underestimate the true velocity. The study conducted by postdoc Iman Taghavi at our collaborators at CFU proposed a theoretical model that predicts a 33% underestimation of peak velocity in 2D imaging when the vessel size is smaller than the full width half maximum in the elevation direction, in this study the FWHM = 770 µm. Field II simulations and hydrogel 3D printed micro flow phantom measurements were conducted and the results confirmed an underestimation of peak velocity by 26% ± 5% (mean ± standard deviation) and 34% ± 8%, respectively. These findings align with the theoretical prediction of 33%. Therefore, the proposed theoretical model can be employed to compensate for velocity estimates in such cases.

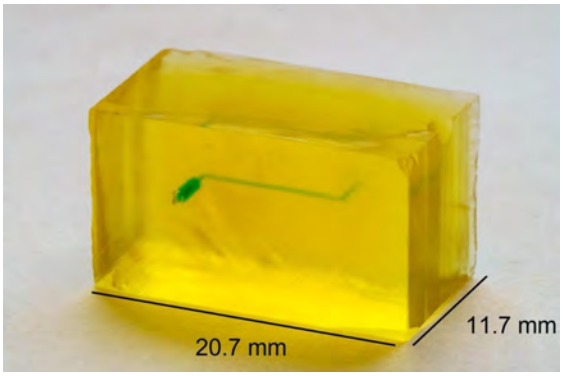
A new micro flow phantom was developed for 3D super-resolution imaging, see Fig. 7.4. Unlike the other phantoms, which were reprinting of existing designed phantoms, this phantom was sketched and subsequently designed by the author using the dedicated MATLAB script. Two tapered V channel separations allow for direct visualization of super-resolution capabilities in both the z-y plane and the x-y plane, without first having to tailor the phantom channel separations to the intended experimental frequency and probe.

7.5 Scatter phantom

A novel type of phantom was developed based on printed hollow cavities that exhibit sound reflection called 3D scatter phantoms. By ensuring the cavities are smaller than the imaging wavelength, they can serve as stable point targets for repeated

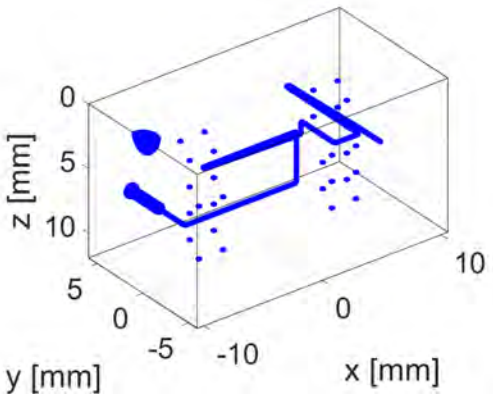


(a)

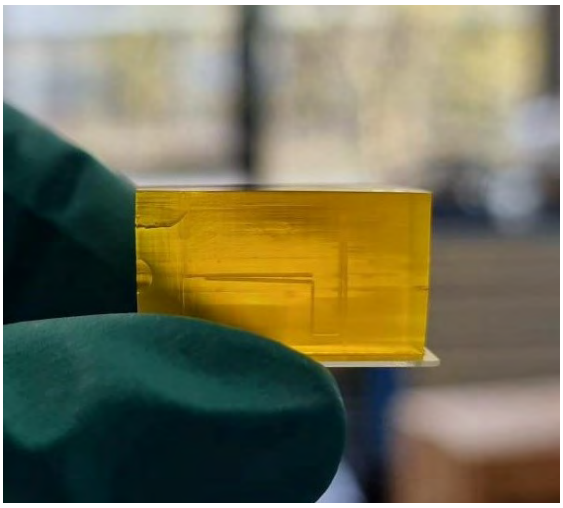


(b)

Figure 7.3: In a) the MATLAB design of the single channel phantom for 2D and 3D imaging with two sets of alignment marks called fiducial markers. b) shows a picture of the 3D printed hydrogel phantom which has been perfused with blue fruit dye highlighting the channel path.

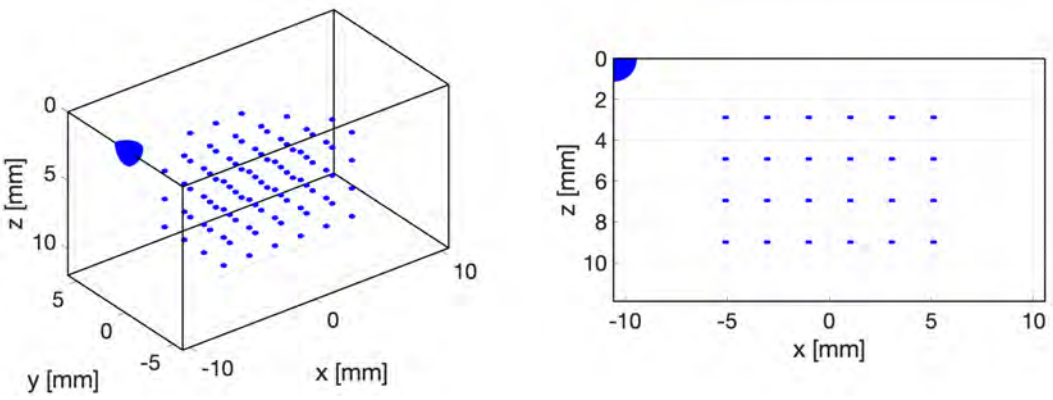


(a)



(b)

Figure 7.4: A 3D model of the phantom design is generated with the MATLAB script showing the two V channels along with the needle inlet and fiducial markers for alignment. The picture of the printed flow phantom in b) shows it from the y-x plane while the phantom is still attached to the cover glass.



(a) (b)

Figure 7.5: Design of the 3D scatter phantom a) shows an overview and b) the x-z plane.

imaging and provide an accurate structure. An alternative to the conventional flow channel phantoms for validating super-resolution ultrasound imaging is the use of these fixated sub-wavelength scatterers. Initially, these scatterers were introduced as fiducial markers in flow phantoms to facilitate precise alignment of the phantom with the ultrasound probe at the micrometer level. However, it was soon realized that they could also serve as the basis for a novel type of phantom [106].
The 3D printed point spread function (PSF) phantom with scattering voids is arranged in a grid pattern of 6 x 4 x 4 in (x, y, z), see Fig. 7.5. The phantom has a scatter spacing of 2.052 mm in all three directions prior to swelling. The scatterers have dimensions of 205 µm wide in both lateral axes and 80 µm along the vertical axis all accordingly to match the voxel grid.
The purpose of the phantom is to allow 3D super-resolution ultrasound imaging calibration. The phantom was used to compare the imaging performance of a row-column (RC) matrix probe with synthetic aperture (SA) imaging to a commercially available linear array probe. The resolution and contrast of the RC probe were compared to the optimized SA sequence of the linear array probe. B-mode images of the 3D printed PSF phantom were presented, showcasing the isotropic resolution of 1.05 λ, 1.10 λ, 0.62 λ = (x, y, z) obtained with the RC probe. On the other hand, the linear array probe had an elevation resolution determined by the fixed elevation focus of the array, resulting in the inability to differentiate the four rows of point scatterers in the elevation direction. This proves that row-column arrays produce superior volumetric images compared to translated linear array probes [33, 110].

7.6 Chapter summary

In this chapter design, 3D printing technique and setup of specialized super-resolution phantoms were demonstrated. The procedure for fabricating the hydrogel phantoms and the methodology for executing the design print was given. Two types of phantoms, namely the micro flow and 3D scatter phantoms, were introduced, highlighting their contributions to the research. Finally, a new micro flow phantom for 3D super-resolution was presented.

Chapter 8

Quartz Fusion silicide CMUTs

In this chapter, the quartz fusion CMUT process based on the polysilicon-on-quartz (POOQ) substrate is presented first with the idea and concept. Next, the characterization and development of the POOQ wafer is described. Then, a detailed process flow of the fabrication of a quartz fusion row-column CMUT is presented. Followed by the tests performed for fusion bonding, LOCOS and silicide formation. Finally, the chapter is concluded with an outlook on this novel process.

8.1 Introduction

CMUTs can be fabricated with versatile bonding techniques, and also sacrificial release, such as fusion bonding, anodic bonding and polymeric bonding of a top and bottom wafer. The bottom electrodes are made prior to bonding, hence they determine the thermal budget of the remaining processing and thereby the bonding technique. Utilizing doped silicon electrodes allows high-temperature processes such as LOCOS and fusion bonding see Fig. 8.1 a), whereas metal electrodes are used in anodic bonding b). Both methods are renowned for their advantages. CMUTs achieved through fusion bonding of silicon substrates allows for LOCOS, which is renowned for the nanometer gap control and high-quality oxides which are often empirically favorable considering dielectric charging. Unfortunately, the doped silicon electrodes are not viable with large-scale arrays as the ωRC-criterion becomes infeasible to meet fabrication-wise as mentioned in the introduction Section 1.6. Anodic bonding based on a borofloat substrate, insulating the electrodes and minimizing cross-talk is preferred for the implementation of highly conductive metal electrodes. However, the anodic bonding technique due to the use of metal electrodes limits the thermal budget. It is hypothesized in this research group, that the quality of the insulating dielectrics increases with temperature and that dielectric charging is correlated with the quality of the dielectric. As the focus of this thesis is to develop large-scale arrays, ensuring that the elements maintain a uniform pressure along the elements makes the metal electrodes an obvious choice. However, in the search for minimizing dielectric charging, a combination of these advantages is presented in this chapter. In this chapter a new CMUT process called the quartz fusion process is described. Initially, the process was suggested by Prof. Erik V. Thomsen and postdoc Andreas S. Havreland and tested by the author. The name quartz fusion comes from the idea of fusion bonding two specially made quartz substrates. The initial process flow is seen in Section A.2. This process is based on the so-called POOQ substrate for both the top and bottom wafers. The use of quartz as a substrate material allows for higher operating temperatures, thereby facilitating fusion bonding

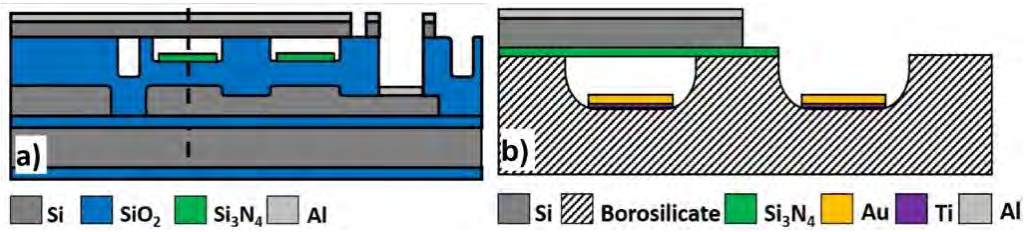


Figure 8.1: Sketch of a CMUT structure realized with a) fusion bonding of a silicon top wafer onto a LOCOS structured bottom wafer with doped silicon bottom electrodes and b) anodic bonding of a silicon top plate onto a borofloat substrate with metal bottom electrodes.

Table 8.1: Thermal expansion coefficient, α softening point and thermal stability for substrates as well as possible bottom electrode materials.

	$\alpha \times 10^6$/K	Softening Point °C	Thermal stability °C	Resistivity µΩcm
Borofloat	3.25	820		
Quartz	0.57	1585		
PolySi	2.7-4.5			
NiSi	12		700	14-20
$TiSi_2$	8-16		980	13-20

in combination with local oxidation of silicon (LOCOS) processing. Furthermore, POOQ wafer facilitates the implementation of silicides as bottom electrodes. If realized for a linear array, the elements would be located at the bottom and the ground at the top, which would make probe assembly considerably easier. Silicides have a lower resistivity than doped silicon see Table 8.1, making silicide formation a viable method for achieving low-resistance bottom electrodes with the well-known LOCOS process for CMUT presented by Park. et. al. [24]. Titanium disilicide enables RC512+512 array at a mere thickness of 250 nm and even RC1024+1024 at 1 µm both with a signal strength of 94 % predicting a uniform pressure distribution along the bottom elements. The novelty is that the silicide formation combined with LOCOS-processing is presented on an insulating substrate, POOQ, minimizing the cross-talk while simultaneously increasing the conductivity through silicide bottom electrodes.

8.2 Concept

Large row-column arrays require low electrode resistivity to ensure uniform pressure transmission and low substrate coupling to prevent cross-talk between elements. The anodic bonding process provides low resistivity through the implementation of metal electrodes and an insulating pyrex substrate, but limits the thermal budget and the equipment options due to pyrex's sodium content. LOCOS with doping of silicon for bottom electrodes achieves medium to low resistivity but increases the thermal budget and the cross-talk. Using an insulating substrate like the POOQ wafer allows for a broader range of processes and equipment to be used, including high-temperature techniques like fusion bonding and silicide formation for low-resistance bottom electrodes. The quartz fusion process combines the benefits of an insulating substrate with the favorable features of LOCOS and fusion bonding, while using lower resistance titanium disilicide electrodes instead of regular doped silicon electrodes. A

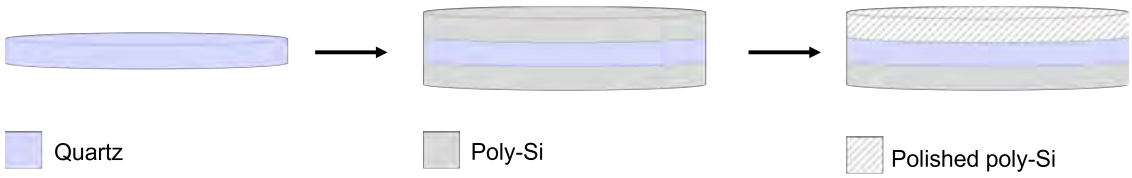


Figure 8.2: The process flow of a simple POOQ wafer. Starting with a quartz substrate where a LPCVD poly-Si is deposited and finally polished by CMP down to a an average roughness below 1 nm.

simplified outline of the quartz fusion process is presented in this list with the key points of the fabrication

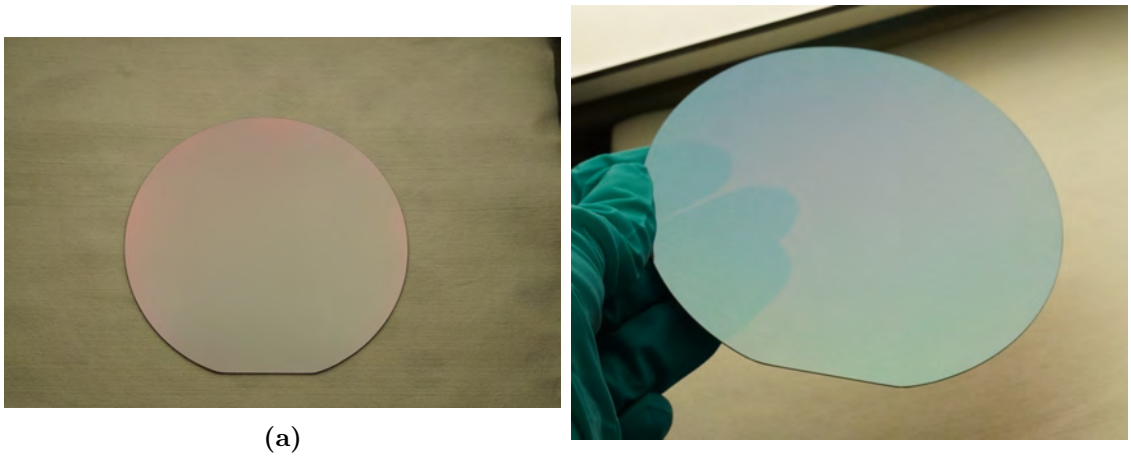
- Quartz substrate with poly-Si, POOQ wafer
- Bottom electrodes through titanium disilicide, $TiSi_2$ formation
- LOCOS to form the cavities
- Ecth separating the bottom electrodes
- Fusion bonding this wafer with another POOQ as top wafer
- Thinning down to the device layer, the top plate
- Open to contact pads
- Deposit aluminum for top electrodes and define these through etching.

In order to realize a fusion bonded CMUT on POOQ wafers, where the cavities have been made with LOCOS and the bottom electrodes from silicide formation. Four things have to be demonstrated: 1) That it is possible to fabricate POOQ, 2) that POOQ wafers support thermal oxidation for LOCOS processing below 980 °C. 3) That POOQ wafers facilitate fusion bonding i.e. surface roughness $\leq$ 1 nm and annealing $\leq$ 980 °C. 4) Lastly, that $TiSi_2$ formation is possible on a quartz substrate. Point 1-3 are described in Section 8.3 and point 4 in Section 8.9.

8.3 POOQ - polysilicon-on-quartz

In its simplest form a POOQ wafer is a quartz substrate on which a polysilicon (poly-Si) thin film is deposited and subsequently polished by CMP to sub-nanometer roughness, see Fig. 8.2. Generally, CMUT processing consists of a top and bottom wafer. The bottom wafer is defined with the bottom electrodes. For the top plate originally an industrial standard SOI wafer was used, where the buried oxide layers are etched back along with the handle layer. The specifications on produced SOI device layer, which is used for the top plate, have a standard deviation of up to 0.5-2 µm in plate thickness. This is a large deviation as most of the plates are between 1-5 µm and will influence the resonance frequency. Therefore, an alternative PSOI wafer was designed by former postdoc Andreas S. Havreland [65]. The PSOI the device layer which makes up the top plate can be tailored down to nanometer precision in thickness and uniformity. Also, insulating dielectrics can be deposited or grown to the specific application i.e. pull-in, destructive testing. A new addition to these substrate types was presented by the author at IUS 2021 [111]. Namely the POOQ

wafer. A quartz substrate on which a thickness tailored poly-Si is deposited and polished to a sub-nm surface roughness by CMP, see Fig. 8.3 and Fig. 8.4.
The quartz substrate is Corning HPFS 7980 fused silica. Contrary to the borofloat wafer that contains ions that are employed to perform the anodic bonding, the quartz is ion free high purity amorphous SiO_2. An LPCVD poly-Si is deposited at 620 °C where the dopant and thickness can be customized. To facilitate fusion bonding the poly-Si is polished from an average surface roughness of R_a=22.6 nm to R_a=0.16 nm with the Logitech CM62 Orbis CMP tool. The polishing slurry consists of silica grains, which makes CMP an inherently dirty process, which requires thorough cleaning before fusion bonding is achievable. A sequential 10 min piranha, 5 min BHF and another 10 min piranha clean effectively remove the particles verified by particle scan prior and post the cleaning procedure. An image of the POOQ wafer can be seen in Fig. 8.3.



(a) (b)

Figure 8.3: POOQ wafer with 2 µm LPCVD poly-Si to the left. Then further processed with oxidation at 950 °C, seen as the semi-transparent wafer to the right.

Currently, the POOQ wafer can be used for a top wafer. It can also be used as the bottom wafer with the transformation of the poly-Si into titanium disilicide. Continuous processing with LOCOS, without the implementation of the titanium disilicide, is shown to the left in the process flow sketch in Fig. 8.4. Thermal oxidation at 950 °C grew an oxide of 933 nm measured by ellipsometry (VASE J.A. Woollam). A picture of the semi-transparent oxidized POOQ is seen in Fig. 8.3 with a surface roughness of 1.75 nm, above the fusion bonding limit. The reason for this increase in surface roughness is that the poly-Si grains grow at the increased temperature of 950 °C. Hence, a direct oxidation post poly-Si deposition is performed yielding a surface roughness of R_a=23.4 nm. Conclusively, polishing of the silicon dioxide is necessary. The CMP polishes away the material and the removal rate depends on back pressure, time and the polished material. This was tested in a study and optimized for both the PSOI and POOQ process. Post CMP the oxide goes through the standardized cleaning procedure developed in this group. A prolonged BHF dip of 5 min increases the surface roughness of the oxide see Tab. XX to 1.86 nm. A compromise of etching the silica grains from the slurry and not increasing the oxide roughness was found to be 20 seconds. Thus, 10 min piranha, 20 seconds BHF followed by a 10 min piranha treatment of the polished oxide resulted in a satisfactory low roughness of $R_a = 0.67$ nm. Unfortunately, the necessary polishing of the oxide sacrifices the precise control obtained through LOCOS of the gap height.

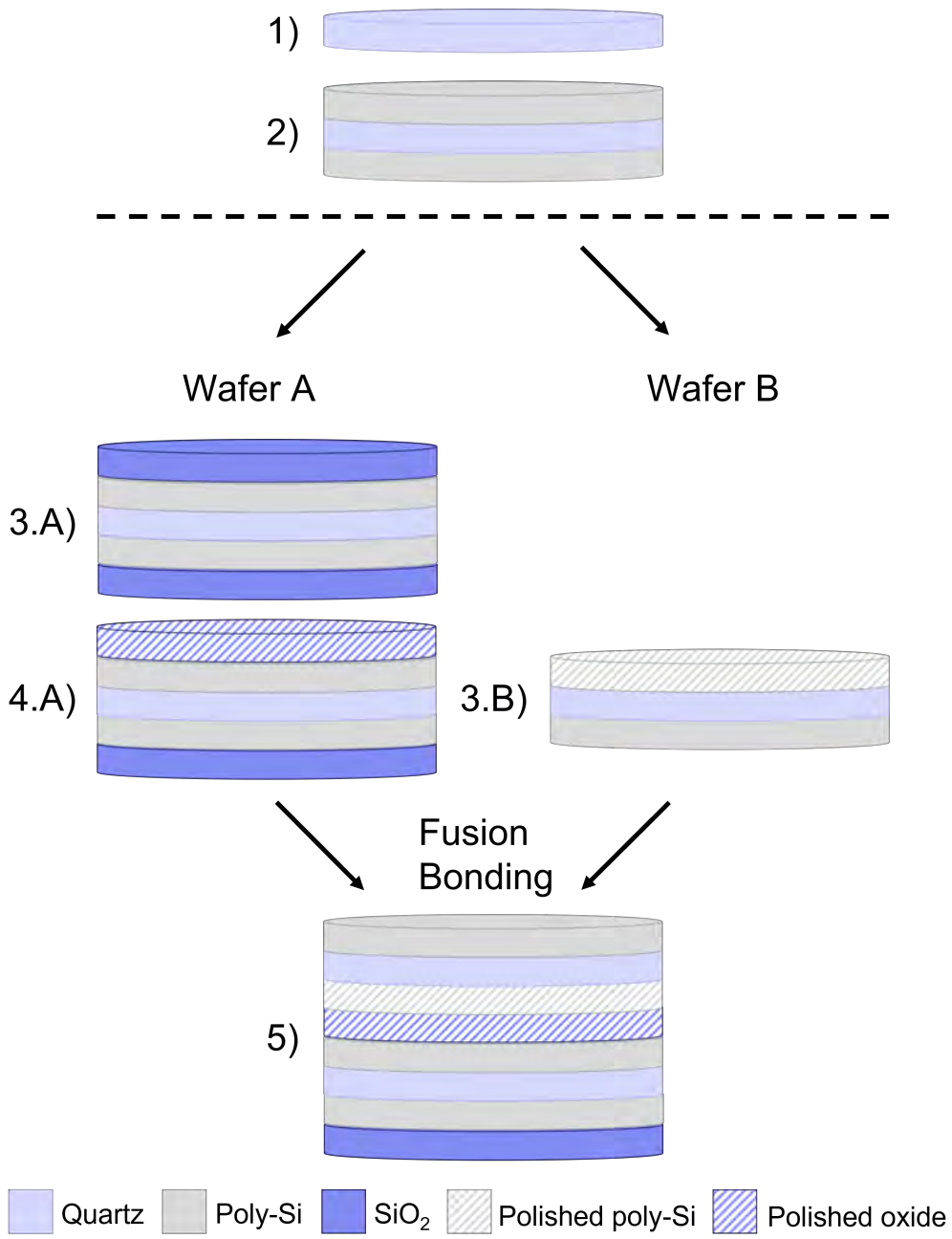


Figure 8.4: Sketch of process flow for POOQ fabrication, oxidation and fusion bonding. 1) The quartz substrate, 2) LPCVD of poly-Si. From beyond the dashed line the POOQ wafer can be processed to a bottom substrate, Wafer A, or a top plate, Wafer B. The fabrication of Wafer A is thermal oxidation 3.A) and polishing & cleaning 4.A). Wafer B, the poly-Si is polished & cleaned 3.B). Both wafers are cleaning in RCA1 and fusion bonded 5).

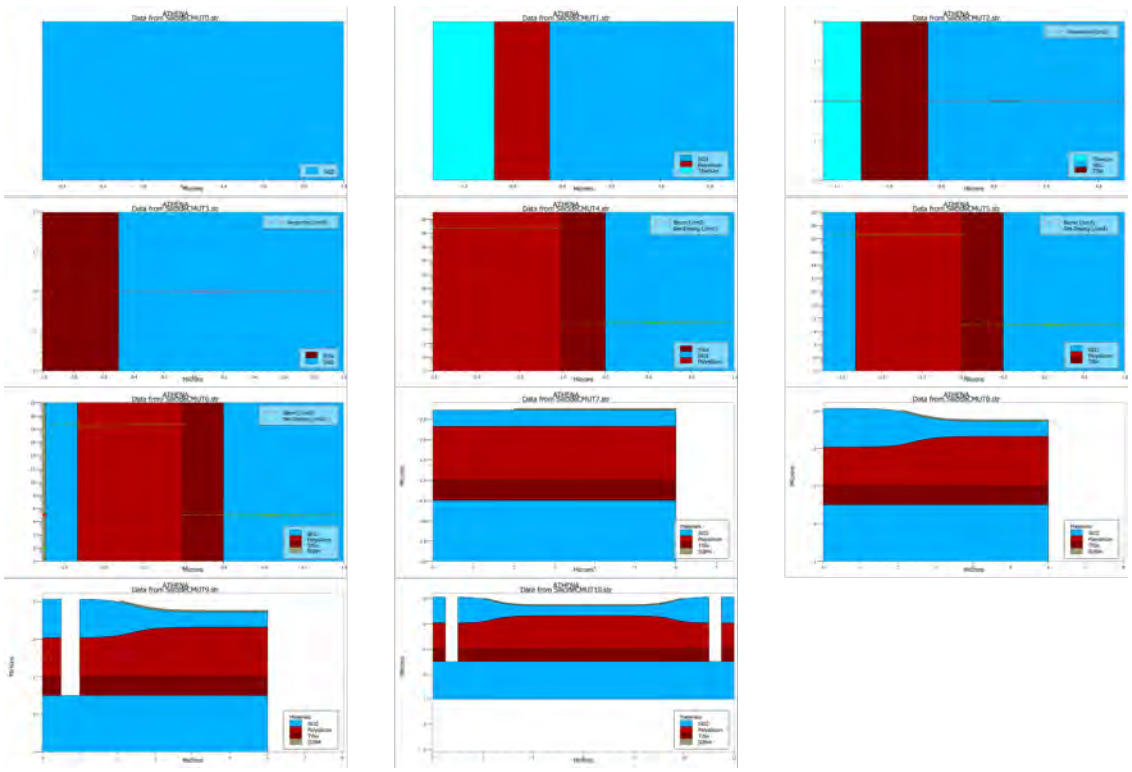


Figure 8.5: Athena simulation of a quartz fusion RC CMUT based on a POOQ with titanium disilicide, $TiSi_2$ as bottom electrodes. 0) Quartz substrate, 1) deposition of poly-Si and titanium, Ti and 2) annealing for silicide formation. 3) Unreacted Ti is removed and the 2nd annealing of $TiSi_2$ to form the low resistivity phase is performed followed by 4) a boron LPCVD poly-Si. 5) Insulation wet oxidation at 950 °C and 6) a nitride deposition, with a poly-Si mask (not shown). The poly-Si masks the nitride etch 6) which forms the pads. The nitride pads form the cavities through 7) LOCOS at 950 °C. 9) Consecutive dry etching of the oxide, poly-Si and the silicide separates and defines the bottom elements of a 10) RC silicide POOQ-based CMUT.

8.4 Quartz fusion fabrication

The fabrication of a quartz fusion CMUT for a Row-Column Array is stepwise simulated and verified in Fig. 8.5. by the microfabrication process simulation tool Athena, proving that a LOCOS quartz-based silicide CMUT is possible. A description of the process flow is given.

First, a quartz substrate with an LPCVD deposited poly-Si and then a titanium film is annealed at 600 °C to form the first phase of $TiSi_2$, C49. A piranha clean is used to remove unreacted excess titanium prior to the second annealing at 750 °C to transform the $TiSi_2$ to the second phase of $TiSi_2$, C54 the low resistivity silicide. Then, an RCA clean is performed before a boron-doped poly crystalline-silicon layer is deposited using a LPCVD at 620°C. The purpose of the poly-Si is to facilitate oxidation. To enable fusion bonding later in the process the poly-Si is polished using a Logitech CM62 Orbis CMP machine. The polishing slurry introduces particles and therefore a thorough clean of 10 min piranha is carried out, followed by a 20 s buffered HF dip and then another 10 min piranha clean is required to remove the polishing grains. To achieve a successful fusion bond, the surface roughness should be below 1 nm [74]. Hence, the CMP process is crucial for fusion bonding to be successful.

Table 8.2: Parameters for the poly-silicon recipes for the two LPCVD furnaces of 4" and 6" tube diameters.

	POLYBOR	**POLY620**	**AMORBOR**	**POLY**	**AMORPH**
Silicon crystallinity	Boron Poly	Poly	Boron Amorph	Poly	Amorph
Furnace	4"	4"	4"	6"	6"
SiH_4 gas flow [sccm]	80	80	80	70	70
BCl_3 gas flow [sccm]	0	0	0	0	0
B_2H_6 gas flow [sccm]	7	0	7	0	0
Pressure [mTorr]	200	200	250	200	200
Temperature [°C]	618-625	618-625	560	616 - 625	562-565

An insulating oxide of 350 nm is grown at 950 °C. LOCOS is typically performed above 1000 °C, but for the titanium disilicide to maintain its low resistivity the temperature should be kept under 980 °C [112]. Therefore, the wet thermal oxidation is performed at 950 °C to preserve the resistivity of the titanium disilicide. Then, an LPCVD process is used to deposit first a layer of nitride and then poly-Si with thicknesses of 60 nm and 100 nm, respectively. These are patterned by lithography to define the CMUT cavities and arrays through LOCOS. First, an etch of the poly-Si and plasma ashing of the resist. Followed by a nitride etch in 160 °C phosphoric acid, H_3PO_4 for 45 min and another poly-Si etch, stripping the poly-Si mask and leaving the nitride pads used for cavity definition. LOCOS is done by a 950 °C wet oxidation. A post oxide of 730 nm is grown to define a gap of approximately 200 nm. However, it is known that the roughness of poly-Si increases with temperature, thus this high-temperature oxidation will increase the surface roughness of the bonding interface which may implicate a polishing of the oxide, this will be tested.

For a Row-Column CMUT the individual bottom electrodes need to be etch-separated. This is achieved by dry etching first the oxide, then the poly-Si and lastly the $TiSi_2$ reaching the insulating quartz. The top wafer is also based on the POOQ wafer, where the poly-Si is highly doped with boron. Polished to a sub-nm roughness by CMP and cleaned in a sequential 10 min piranha, 5 min BHF dip and 10 min piranha treatment.

An RCA cleaning of both the top and bottom wafer is done and they are immediately hand bonded afterward under high-efficiency particulate air filter (HEPA). The combined wafers are pre-bonded in the wafer bonder followed by a 950 °C annealing step for 70 min to form the fusion bonds. Subsequently, the top poly-Si layer is removed by reactive ion etching (RIE) exposing the quartz handle for removal in 40% HF. Finally, the opening to the bottom electrodes contact pads is done with reactive ion etching (RIE). An aluminum layer of 400 nm is deposited by e-beam evaporation for the top electrodes and patterned by lithography and defined by ion beam etching.

8.5 Characterization of POOQ

To facilitate a platform for high-temperature LOCOS and fusion bonding three important features of the POOQ are to be characterized: Roughness, wafer bow and stress.

Table 8.3: Poly depositions throughout the quartz fusion process development batches. Showing roughness for the two LPCVD furnaces of 4" and 6" tube diameters.

Batch	Furnace	Material	Thickness [µm]	AFM roughness [nm]		
				Rq	Ra	Rmax
1 QF	4" LPCVD	POLYBOR	1.9	52.5	41.8	340
2 QF	6" LPCVD	POLY x 1	1.2	22.5	18.0	151
2 QF	6" LPCVD	POLY x 2	2.4	28.7	22.8	177
3 QF	4" LPCVD	POLYBOR	1.9	38.2	30.4	268
4 QF	4" LPCVD	AMORBOR	1	7.20	5.65	66.3
5 QF	4" LPCVD	POLYBOR	1	10.2	7.87	70.1
5 QF	4" LPCVD	POLYBOR	1.9	12.4	9.64	82.4
6 QF	4" LPCVD	POLYBOR	2	28.1	22.6	165

8.5.1 Roughness

Surface roughness is a determining factor in whether or not fusion bonding with the POOQ is possible. Parameters like deposition rate, roughness, quality and stress are furnace dependent and need to be optimized for the specific furnace. Two furnaces Tempress LPCVD polysilicon furnaces of 4" and 6" diameter tubes were used in these tests. The different furnaces recipes and their parameters can be seen in Table 8.2. Amorphous silicon is formed at deposition temperatures below 590 °C around 560-570 °C, whereas poly-crystalline silicon is usually formed between 615-625 °C. Amorphous silicon results in tensile stress while poly-silicon results in compressive stress in the thin film. High-temperature 1100 °C annealing will decrease the residual stress to near-zero [113]. It was found that increasing anneal temperature decreases the stress [114]. Temperatures from 570°C to 630°C, will result in (110)-textured columnar grains [115]. High-temperature annealing will result in a coarsening of the grains, increasing the surface roughness [115]. The deposition rate and roughness increase with deposition temperature for poly-Si deposition. An overview of the variation in roughness through the 6 batches of quartz fusion that were tested can be seen in Table 8.3. Boron-doped poly-Si from the 4" LPCVD furnace have an average roughness ranging from R_a= 9.64-41.8 nm for approximately 2 µm and as low as 7.87 nm for a 1 µm. This variation indicates that the condition of the furnace at the time of deposition determines the roughness since pressure, flow and temperature are kept constant, see Table 8.2. Undoped polysilicon gave a roughness of R_a= 18 nm and amorphous boron-doped silicon resulted in R_a= 5.65 nm. Judging purely on the numbers from Table 8.3, amorphous boron-doped silicon obtains the lowest roughness, but this is not the only parameter that the POOQ has to fulfill. The results of the various depositions, as well as combinations with CMP and oxidation will be elaborated below. The surface roughness is characterized with a Bruker AFM Dimension Icon-Pt over a minimum area of 1-2 µm at 1Hz.

For the test of 6" LPCVD furnace, undoped polycrystalline silicon a 1 µm poly-Si layer R_a= 18 nm and for 2 µm poly-Si it is R_a= 22.8 nm, hence double thickness increases the average roughness with approximately 5 nm, see Table 8.3 and Table 8.4. For the goal of doing LOCOS processing a wet thermal oxidation of the undoped poly-Si layer was performed and decreased the average roughness to 15.5 nm, which is a reduction of 2.5 nm. This decrease in roughness is attributed to annealing at a higher temperature of 950 °C grain structure of the poly-Si rearrange and the residual stress is reduced, assuming that the grain growth has saturated. The original

Table 8.4: 2nd QF

Wafer	Topmost material	Treatments/processes before AFM	AFM roughness [nm]			Bond to	Bonded
			Rq	Ra	Rmax		
08	Poly Si	1xPoly	22.5	18.0	151		
01	Poly Si	2xPoly	28.7	22.8	177		
05	SiO2	1xPoly+WET950	19.8	15.5	135		
08	Poly Si	1xPoly + CMP	0.190	0.147	1.82	07	No
01	Poly Si	2xPoly + CMP	0.188	0.138	1.76	No	
01	SiO2	2xPoly + CMP + WET950	2.18	1.75	14.9		
07	SiO2	1xPoly + WET950 + CMP	0.171	0.136	1.51	08	

Table 8.5: 3rd QF

Wafer	Topmost material	Treatments	AFM roughness [nm]		
			R_q	R_a	R_{max}
02	B-Poly Si	POLYBOR	38.2	30.4	268
03	SiO2	POLYBOR + WET950	33.1	26.3	242
06	SiO2	POLYBOR + WET950	31.1	25.1	198
06	SiO2/Si	POLYBOR + WET950 + CMP 5 min	0.138	0.131	7.69

idea for the process design was to polish the poly-Si and then perform oxidation for LOCOS, this was done with wet thermal oxidation at 950 °C resulting in R_a= 1.75 nm as seen in Table 8.4, which is above the fusion bonding limit, therefore, the oxide needs to be polished. All three samples were polished with CMP recipe (hm soi cmut) for 3 min and obtained comparable roughness of R_a= 0.136-0.147 nm.
In the 3rd batch, the 4" LPCVD furnace tube was changed and resulted in a lowered roughness of R_a= 30.4 nm of the poly-silicon compared to the first run of 41.8 nm. Again, the phenomenon of a decrease in roughness after oxidation to 25.1-26.3 nm was observed, see Table 8.5. To obtain a sub-nm smoothness the oxidized wafers were polished with CMP with the recipe (hm soi cmut) for 5 min to R_a= 0.13 nm. This is sufficient for fusion bonding, however at a cost of the precise thickness control inherent to the LOCOS oxidation.
Up until now, only polycrystalline silicon has been tested. Thus, to salvage the nanometer control of the LOCOS, amorphous boron-doped silicon was tested for polishing prior to oxidation in the hopes of having a surface roughness post oxidation of less than 1 nm in the 4th batch. Amorphous silicon was deposited and gave a roughness of R_a= 4.63 nm and then polished by CMP to an average roughness of R_a= 0.006-0.134 nm, depending on the polishing recipe see Table 8.6. All four test wafers were oxidized at 950 °C and resulted in an average roughness of R_a= 1.11-1.34 nm. Unfortunately still above the fusion bonding limit. It was hypothesized that the amorphous silicon would not coarsen like the poly-silicon without the grain growth at higher temperatures the roughness could be minimized. However, the result shows that the surface roughness will be approximately 1.3-1.7 nm after oxidation for both polished amorphous and poly-silicon, see Table 8.4 and Table 8.6.
A comparative table of different materials and substrates can be seen in Table 8.7. It is observed that oxidation of a silicon wafer with R_a= 0.07 nm prior to oxidation gives R_a= 0.09 nm post oxidation at 950 °C, essentially negligible. From this, it can be concluded that is indeed the amorphous or poly-Si film roughness that is translated through the growth of the oxide observed in the previous batches. Also, the numbers indicate that boron doping increases the roughness comparing boron-doped amorphous of R_a= 4.63-5.65 nm with amorphous of R_a= 0.456 nm. Contrary,

Table 8.6: 4th QF

Wafer	Topmost material	Treatments	AFM roughness [nm]		
			R_q	R_a	R_{max}
01	Amorph Si	Amorph Si LPCVD 1 µm	5.88	4.63	51.5
01	Amorph Si	Polished aSi CMP hm soi cmut 1min	0.08	0.07	0.76
02	Amorph Si	Polished aSi CMP hm soi cmut 1min	0.08	0.06	0.93
03	Amorph Si	Polished aSi CMP cmut kitste 1min	0.121	0.89	2.55
04	Amorph Si	Polished aSi CMP cmut kitste 1min	0.173	0.134	1.64
01	SiO2	Oxidized polished aSi CMP hm soi cmut 1min	1.54	1.20	12.5
02	SiO2	Oxidized polished aSi CMP hm soi cmut 1min	1.43	1.11	15.7
03	SiO2	Oxidized polished aSi CMP cmut kitste 1min	1.77	1.34	18.3
04	SiO2	Oxidized polished aSi CMP cmut kitste 1min	1.60	1.22	16.9

Table 8.7: Comparative table of substrates and layers throughout the quartz fusion process optimization.

	Material	Substrate	Furnace recipe	Temp	Thickness	AFM roughness [nm]		
						Rq	Ra	Rmax
	Silicon wafer					0.088	0.070	0.817
WAFR 20210426 FS 13	Quartz wafer	Quartz				0.274	0.217	2.28
	Silicon oxide	Silicon	WET950C	950	730 nm	0.112	0.089	0.933
POLYBOR 1900nm Sitest stlope 20212303	Poly-Si boron doped	Silicon	POLYBOR	620	1900 nm	28.4	22.8	178
WAFR 20210322 QF 02	Poly-Si boron doped	Quartz	POLYBOR	620		38.2	30.4	268
WAFR 20210426 FS 14	Poly-Si undoped	Quartz	POLY620	620	500 nm	9.42	7.37	74.2
WAFR_20210426_QF_01	Amorph Si boron doped	Quartz	AMORBOR	580	1050 nm	5.88	4.63	51.5
NILT 863nm aSi 6LPCVD FS 01	Amorph Si	Quartz	AMORPH	580	863 nm	0.572	0.456	4.84
WAFR 20210428 QF 04 AMORBOR	Amorph Si boron doped	Quartz	AMORBOR	580	1000 nm	7.20	5.65	66.3

the undoped poly-Si of R_a= 7.37-22.8 nm and boron-doped poly-Si range from R_a= 7.87-41.8 nm is inconclusive as to whether or not doping affects the roughness. For future work, the author would suggest undoped amorphous silicon for the bottom wafer for LOCOS oxidation, where the effect of the conductivity affect it would have on the future silicide bottom electrodes. For the top wafer, a boron-doped poly-Si polished to a mirror finish with CMP is recommended. At the current time, it was decided to polish the oxide surface as well as the boron-doped poly-silicon surface of the top wafer to achieve surface roughness below 1 nm.

8.5.2 Wafer bow

The wafer bow is the radius of curvature of the wafer. Thin film stress and thickness, annealing and etching of the different material layers will influence the bow. All measurements were done with a Dektak XTA stylus profilometer from Brüker on ball bearings.

The initial wafer bow of quartz is 1.6-10.3 µm, and depositing an LPCVD boron-doped poly-Si thin film in the 4" furnace of 1.9 µm gives a wafer bow of 5.3-12.2 µm. Mechanical polishing (CMP) with the recipe (hm soi cmut) for 3 min of the 1.9 µm poly gives a comparable wafer bow of 12.9 µm. Contradictory to expected, as to the removal of material from one side should influence the bow. Continuing with oxidizing this polished poly-Si at 950 °C gives a wafer bow of 14.3 µm, see Table 8.8. Polished oxide on top of polished poly-Si has a wafer bow of 3.5 µm. The wafer bow of polished oxide is between 5.1-10.1 µm. Out of the two CMP recipes, the gentle (cmut kitste) recipe gives less bow of 2.4 µm whereas the rougher (hm soi cmut) recipe gives a bow of 16.1 µm for polished silicon. All of these wafer bows were on quartz substrates. For comparison, two silicon substrates with 300 nm oxide were polished with the same recipes resulting in a similar wafer bow of 2.1 µm for (cmut kitste) and -2.1 µm for (hm soi cmut). However, on the wafer with -2.1 µm bow

Table 8.8: 5th QF

Wafer	Topmost material	Treatments/processes before AFM	AFM roughness [nm]			Wafer bow [µm]	Bond to	Bonded
			Ra	Rq	Rmax			
WAFR 20210604 QF 07	Poly Si	Polished poly-Si CMP hm soi cmut 3min	0.195	0.144	4.76	12.9	05	No
WAFR 20210604 QF 08	Poly Si	Polished poly-Si CMP hm soi cmut 3min	0.144	0.114	1.29			
WAFR 20210604 QF 05	SiO2	Oxidized polished poly-Si CMP hm soi cmut 3min	1.12	0.907	7.50	14.3	07	No
WAFR 20210604 QF 06	SiO2	Oxidized polished poly-Si CMP hm soi cmut 3min	1.56	1.24	10.1		08	No
WAFR 20210604 QF 08	Poly Si	RCA cleaned polished poly-Si	0.302	0.229	3.58		06	No

all of the oxide was polished away due to the high removal rate of (hm soi cmut) resulting in the concave profile. Fusion bonding of wafers with 10-15 µm wafer bow has been reported. All of the POOQs were convex, which is ideal for bonding as the wafers then initially contact at the center minimizing enclosures of air voids.

8.5.3 Stress

The thin film stress in the poly-Si and the silicon dioxide, SiO_2 of the POOQ was calculated using Stoney's equation:

$$\sigma = \frac{E}{(1-\nu)\frac{t_s^2}{6t_f}(R_f - K_i)}. \tag{8.1}$$

Where E and ν are Young's modulus and Poisson's ratio of the substrate, t_s is the substrate thickness, t_f is the film thickness, R_F is the final curvature (after etching the film from the backside), and K_i is the initial curvature both measured with a profilometer. An overview figure of the process can be seen in Fig. 8.6.

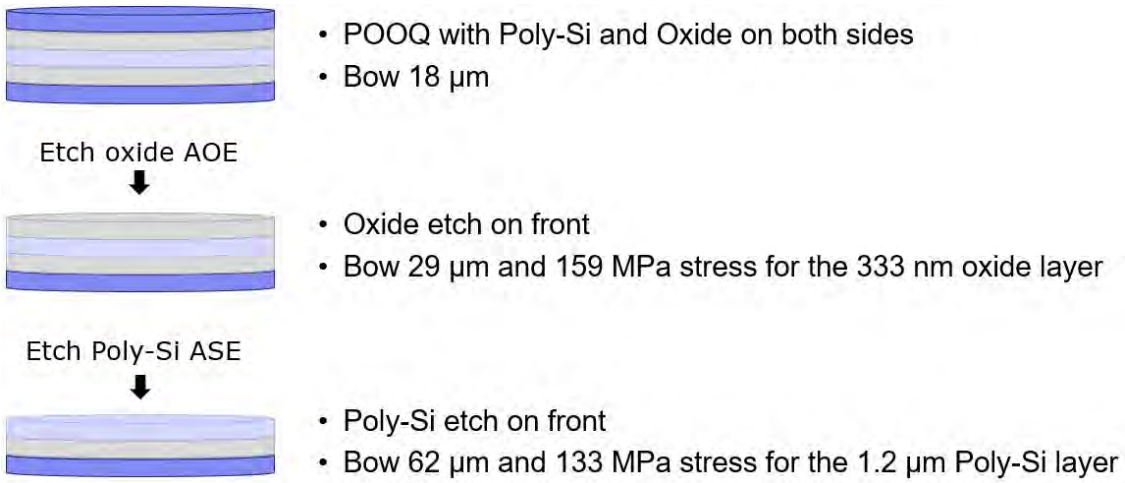


Figure 8.6: Summary of the thinning down test on WAFR_20210216_QFtest_07 showing stress and bow for the different etching steps.

A 29 µm bow for a glass wafer with 1.2 µm Poly-Si on both sides and 333 nm oxide on one side. The stress in the silicon oxide was calculated to be -159 MPa compressive stress. Compared with the literature wet thermally grown oxide at 950 °C on a silicon substrate results in -225-275 MPa compressive stress, this is reasonable given that the POOQ is based on a quartz substrate. The stress for the 1.2 µm LPCVD deposited Poly-Si was calculated to -133 MPa compressive stress since the deposition temperature was 620 °C the stress should be compressive and on the order of -255MPa [113] for an undoped poly-silicon deposited at 615 °C. The thin film stresses of the POOQs are acceptable.

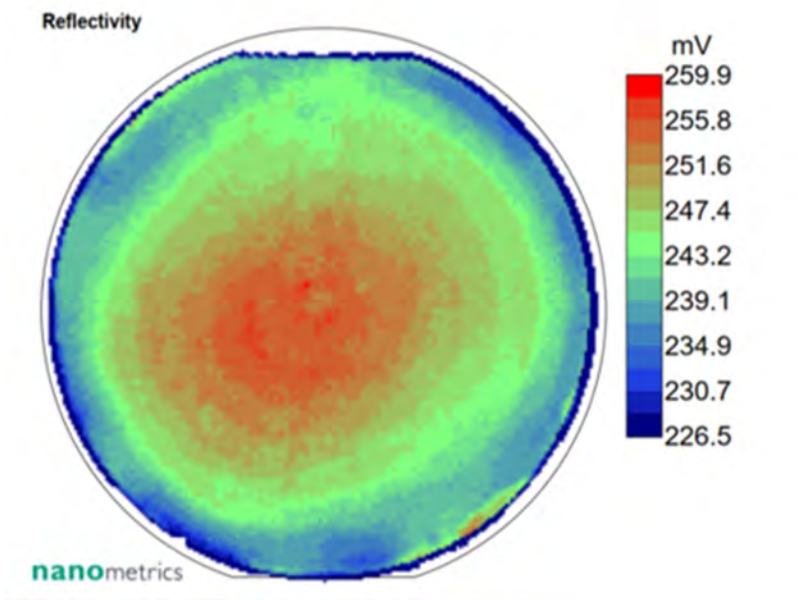


Figure 8.7: Reflectance map of the fusion bonded POOQ A and B wafers.

8.6 Fusion bonding

For successful fusion bonding three characteristics are imperative: 1) Roughness $\leq$ 1 nm, 2) wafer bow $\leq$ 5 µm, preferably convex and 3) clean particle-free surfaces. The last requirement would have been ideal to examine with a particle scanner, unfortunately, at the time of these experiments the particle scanner was sent to the USA for repair and was out of use for 11 months.
Several fusion bonding experiments were carried out during the process optimization of the POOQ.
As a proof of concept that POOQ facilitates LOCOS and fusion bonding, wafer A and B in Fig. 8.3 were fabricated and fusion bonded. Precondition cleaning of both wafers was done with an RCA1 of H_2O, NH_4OH and H_2O_2 in a (5:1:1) ratio. Followed by an immediate hand bond under a HEPA filter to minimize the particle exposure to the cleaned bonding surfaces. Pre-bonding was done at 50 °C in a Süss SB6 wafer bonder, then bond annealed in nitrogen for 70 min at 950 °C to preserve potential future silicide electrodes. The resistivity of $TiSi_2$ is preserved below 980 °C. After fusion bonding the bond quality was inspected with a reflectance mapping tool (RPM 2000, Nanometrics) shown in Fig. 8.7. The characterization of the reflectance map shows a uniform bonding interface with no voids. Hereby, proving that the POOQs can be thermally oxidized, polished and successfully fusion bonded together.

8.7 Plate thinning

After fusion bonding, it was tested if the quartz handle of the top wafer could be removed by wet etching in 40% HF. First, the silicon oxide and the poly-silicon layer were removed with reactive ion etching. Then, a two-step 40% HF etching of the top quartz wafer. Prior to etching, the wafer stack was submerged in water to allow for the diffusion of water into potential voids at the oxide bond interface. Should any HF diffuse into these voids it would be diluted and the rate at which the bond would be etched should be minimized. First, a 6 h HF etch was executed and then

left in water overnight or at a minimum of the etch time to diffuse any HF acid that might consume the wafer or harm the handler. The bond looked intact from the front see Fig. 8.8 a), although the back revealed islands of poly-Si left where a uniform layer was expected see Fig. 8.8 b-c). Nevertheless, the second step of 5 h HF etch was done to test the endurance of the bond and afterward left in water overnight. At the final inspection approximately 50% of the bond was intact, see Fig. 8.8 d). However, all the back-protecting poly-Si was removed due to pinholes in the poly-Si see Fig. 8.8 e-f) which shows beautiful intricate patterns etched into the glass. The quality of the poly-Si is the limiting factor for this method, even though LPCVD is usually known for its thin-film continuity and conformal coating.

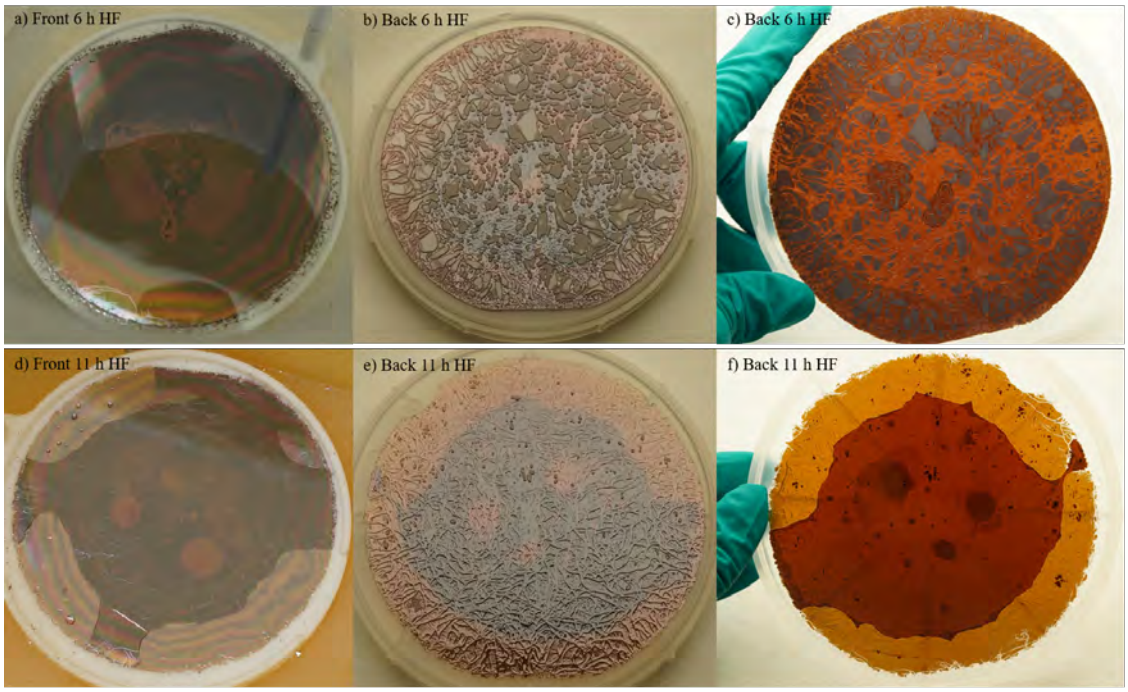


Figure 2. Images of the wafer stack after etching in 40% HF for 6 h and 11 h seen in a-c) and d-f), respectively. The frontside where the quartz wafer is etched is seen in a) and d). The backside is seen in b-c) and e-f). Approximately 50% of the bond interface is preserved after 11 h in HF.

Figure 8.8

Thinning down the 500 µm quartz wafer sets strict requirements of the quality of the poly-Si film on the back i.e., no pinholes or the entire device will be consumed if it is to be etched back by 40% HF. Another approach to etching the quartz could be RIE using a BOSCH process without the passivation layers to increase the etch rate. However, the selectivity is poor between the silicon and the silicon dioxide (quartz) therefore the final micrometers should be removed in HF. Alternatively, a third method, where the quartz could be removed by lapping and the final micrometers should be removed by wet etching as well.

8.8 LOCOS structure on POOQ

The formation of the cavities through LOCOS processing was performed on a POOQ wafer. First, a 1.9 µm boron-doped LPCVD poly-Si was deposited at 620 °C with a roughness of 30.4 nm. In the next step, an insulating 386 nm silicon oxide was grown at 950 °C, resulting in an R_a = 26.3 nm. LOCOS is typically performed above 1000 °C, but for the titanium disilicide to maintain its low resistivity the temperature was kept under 980 °C [112]. Subsequently, a 60 nm nitride and a

100 nm poly-Si layer were deposited by LPCVD to define the LOCOS structure. The layer was patterned by lithography to define the CMUT cells and arrays. The poly-Si layer was etched first for 4 min in an isotropic poly-Si etch with HNO_3, BHF and H_2O in a 20:1:20 ratio and the resist was stripped by plasma ashing, see Fig. 8.9. The nitride was defined by etching in 160 °C hot H_3PO_4 for 45 min and the poly-Si mask was stripped in the poly-Si etch, see Fig. 8.9 turning the cavity pads from yellow to green. The LOCOS was done by a 950 °C wet oxidation, see Fig. 8.10. This yielded a 730 nm silicon oxide growth defining a gap height of 200 nm measured by AFM. An AFM scan across a CMUT cell was performed and gave a roughness on the post oxide of 24.1 nm and 22.9 nm in the nitride cavity. The bonding interface should have a smoothness of < 1 nm, hence polishing is required. In conclusion, fusion bonding is not possible without sacrificing precise control of LOCOS-grown oxide.

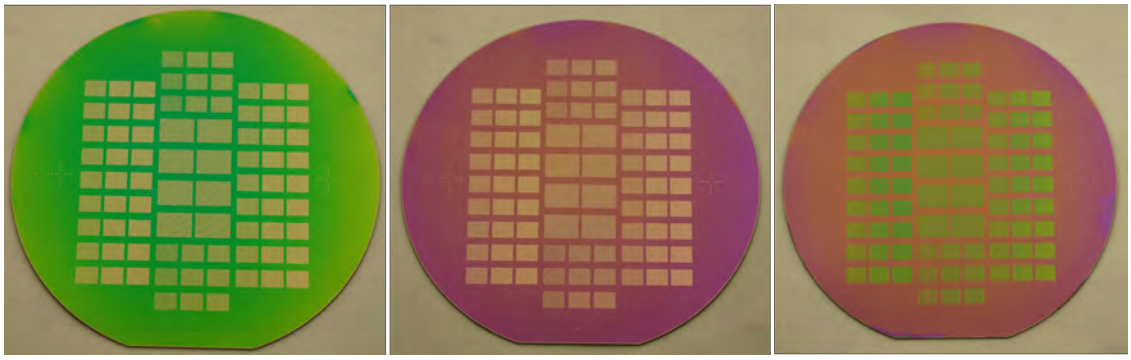


Figure 8.9: From left to right: 1st poly-Si etch defining cavities with the poly-pads, showing a uniform green nitride substrate, then the nitride etch showing a uniform magenta oxide and finally only a color change of the arrays to green nitride when stripping the poly-Si mask. The POOQ wafer is now ready for the LOCOS.

In an article on fabricating MOSFETs on quartz substrates through LOCOS, it was found that the thermal expansion mismatch between the quartz substrate and the LPCVD poly-Si causes extensive crazing during laser recrystallization, making it necessary to divide the poly-Si film into smaller regions with stress relief grooves. In another approach, field regions were transformed into silicon dioxide via LOCOS, while device islands were masked by nitride. This approach prevented crazing and stabilized the silicon islands during laser recrystallization.

8.9 $TiSi_2$ formation

For the bottom wafer, the advantage of the insulating glass substrate is utilized. In this case, a quartz wafer on which low-resistivity titanium disilicide bottom electrodes are to be formed.
Titanium disilicide, $TiSi_2$ is valued for its high thermal stability up to 980 °C and low resistivity down to 13 µΩ cm to 20 µΩ cm. The formation of $TiSi_2$ is performed by annealing either co-sputtered Ti and Si or by evaporating Ti onto silicon or poly-Si thin film and reacting the two. The latter approach was done on both silicon and quartz substrates by Andrea Maria Pierri Enevoldsen, Christian Broberg Christensen and Peter Dalsgaard Nicolaisen in their BSc. project [116] supervised by the author in which the process and challenges are explained in detail. A brief summarized overview of the results will be given below.

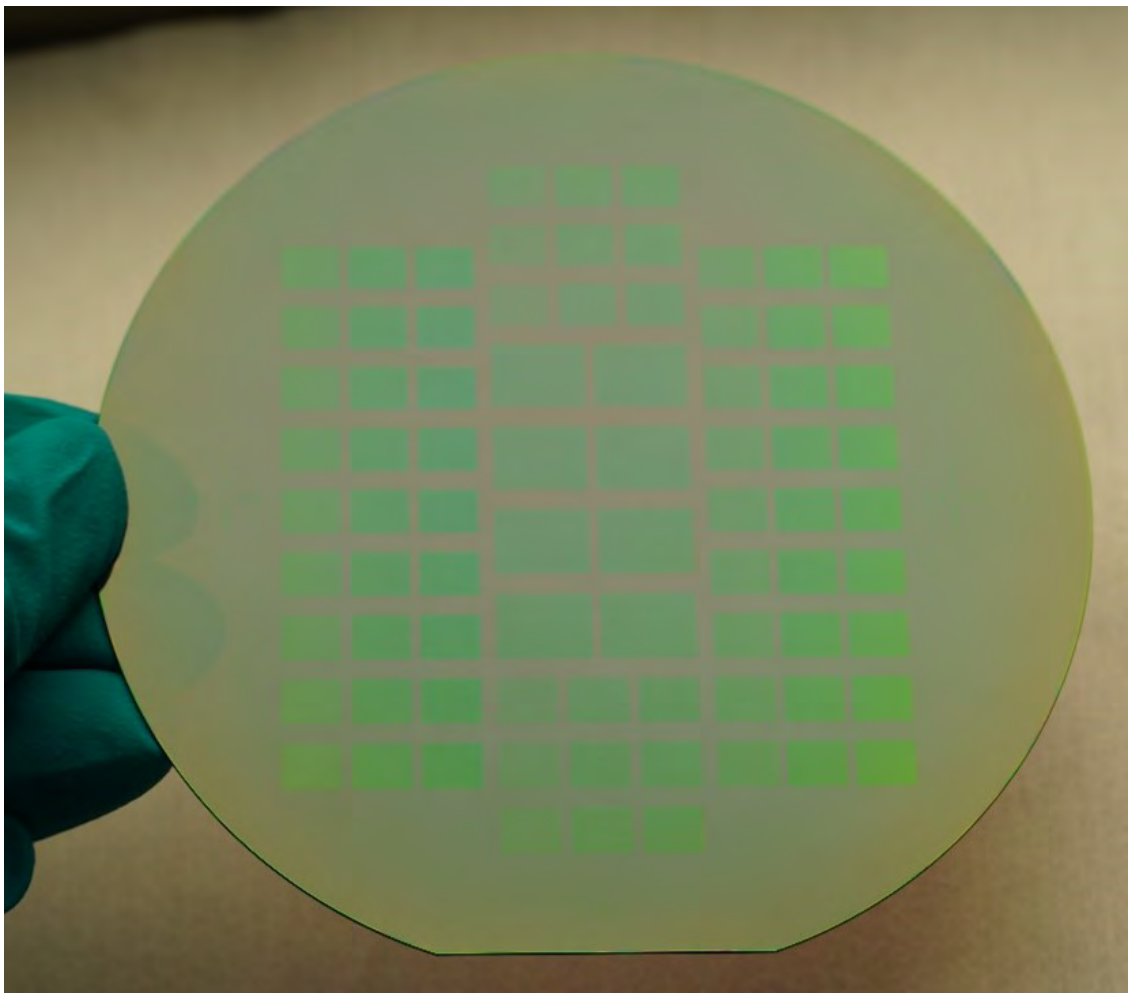
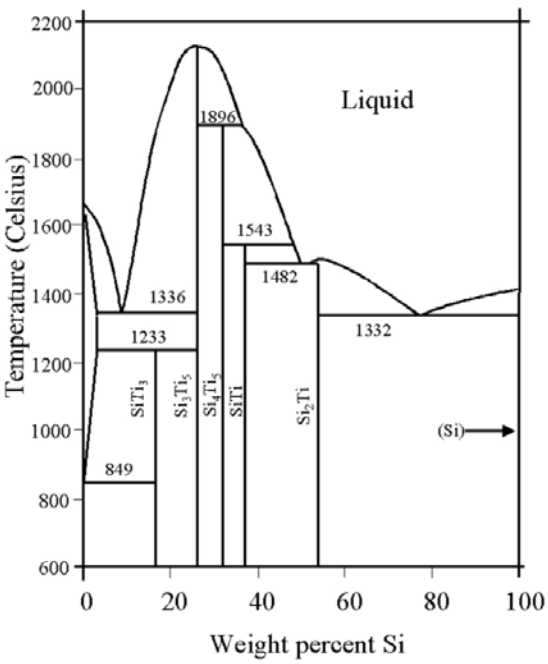
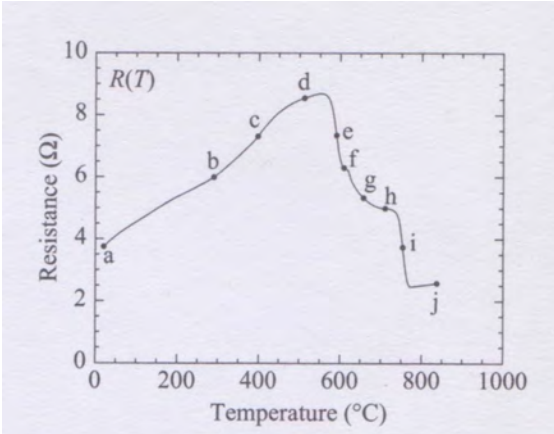


Figure 8.10: Image of W08 after LOCOS and microscopy image of the cavities, where the roughness is visibly transferred from the underlying poly-Si to the oxide and nitride.

A phase diagram for the titanium-silicon system is shown in Fig. 8.11. It illustrates the five equilibrium phases that can be formed between titanium and silicon. Additionally, Fig. 8.11 presents a resistance versus temperature plot for Ti-poly-Si (poly-Si refers to polycrystalline silicon) furnace annealing. The phases formed in the titanium-silicon system are influenced by various factors such as the annealing ambient, contamination, and interface treatment. The first crystalline phase to be formed is the metastable state C49 titanium disilicide at 550 °C upon solid-state diffusion of silicon into titanium, see Fig. 8.11. The C49 phase is base-centered orthorhombic with a higher resistivity of 80-100 µΩ cm corresponding to the point between d)-e) in the resistance curve with a sharp decline. This decrease in resistance is seen when the Ti-Si phase is transformed from the amorphous phase, α-TiSi to the C49-$TiSi_2$. Annealing to 750 °C a second sharp decrease in resistivity occurs between the point h)-i) where the equilibrium phase C54-$TiSi_2$ forms. The C54-$TiSi_2$ has a lower resistivity of 13-20 µΩ cm. The formation is polymorphic, meaning that the ratio of Ti:Si of 1:2 is still the same as in the C49 phase. However, the C54 phase is face-centered orthorhombic with double the number of atoms compared to the C49 phase [117]. Increasing the temperature above 900 °C will result in agglomeration increasing the resistance. The reaction forming titanium disilicide can be described as



(a)



(b)

Figure 8.11: Binary phase diagram of titanium and silicon to the left. Resistance curve with increasing anneal temperature for a Ti-poly-Si to the right, increased in steps of 10 °C/min with a four-point probe from [117].

$$Ti + Si \rightarrow \alpha - TiSi_x \rightarrow C49 - TiSi_2 \rightarrow C54 - TiSi_2, \tag{8.2}$$

noting that the amorphous phase, $\alpha - TiSi_x$ and the C49 phases are not part of the binary phase diagram, but are inherently formed before transitioning into the equilibrium phase.

A table with the combination overview of the results from the BSc. project is seen in Table 8.9. The findings of the BSc. project showed that holes in the $TiSi_2$ and the formation of TiN occurred when annealing in nitrogen on both substrates both decreasing the resistivity measured with XPS and XRD. While bubble-formation, which could be a composite revealed by EDX occurred when annealing silicon substrates in a vacuum. Unfortunately, cracks of a couple of microns deep were found extensively on all quartz substrates, whether annealed in nitrogen or vacuum, detrimental to the fabrication process. The formation of the cracks is presumably due to the difference in linear thermal expansion coefficients for $TiSi_2$ $11 \cdot 10^{-6}$ K^{-1} at 600 °C and for quartz, $0.54 \cdot 10^{-6}$ K^{-1} at 600 °C [116] [118]. The metastable C49 $TiSi_2$ has a thermal expansion coefficient $10.9 \cdot 10^{-6}$ K^{-1} [119]. For $TiSi_2$ over a range of 300-1600 K, the thermal expansion coefficient ranges from $8 - 17 \cdot 10^{-6}$ K^{-1} [120]. Furthermore, all substrates showed a wafer bow between 40-90 µm over an 8 cm range after the second annealing for the C54 formation. This large wafer bow counteracts the possibility of wafer bonding. Another observation was that the TiSi-phase formations occurred at lower temperatures than expected. The low resistivity C54-$TiSi_2$ phase was found as low as 650 °C. Controlling the oxygen level seems to be crucial when inspecting the XPS data and the formation of titanium oxide will increase the resistivity beyond usage. In the topmost layer, XPS showed a large amount of oxygen for vacuum-annealed samples this was only measured on quartz

Table 8.9: Overview of the BSc. projects findings of occurring defects in the formed $TiSi_2$ on the quartz and silicon wafers and in which annealing ambient: nitrogen, N_2 or vacuum.

	Quartz	**Silicon**
Cracks	N_2, Vacuum	
Holes	N_2	N_2
Bubble		Vacuum
TiN	N_2	N_2
TiO2	N_2, Vacuum	

which could indicate that the oxygen might stem from the substrate. Annealing in inert argon should be tested, however currently not available at DTU Nanolab. Crack formation is the most urgent challenge, which needs to be solved in order to realize titanium disilicide on quartz. However, the stress caused by thermal mismatch has been observed for tungsten polycide on quartz at temperatures of 1000 °C [121]. In conclusion, control of the annealing ambient as well as contaminates is at the essence of forming low resistivity $TiSi_2$.

8.10 Chapter summary and outlook

Out of the four requirements for a quartz fusion titanium disilicide CMUT three were successfully demonstrated, namely that POOQs can be fabricated and that they facilitate LOCOS and fusion bonding. The last requirement of titanium disilicide formation on quartz proved difficult. Previously, a former Ph.D. student from this research group has successfully fabricated titanium disilicide, though with tools that have been decommissioned [112]. The conditions of the cleanroom equipment are extremely important for silicide formation and the process optimization required to achieve this was out of the scope of this PhD. In the future, the author would suggest a combination of fusion- and anodic bonding as presented previously by this group in the TR2 probe [122]. Here the titanium disilicide would be fabricated on a silicon substrate, circumventing the large thermal mismatch between $TiSi_2$ and quartz. With this method, the bottom elements are trench etch separated 100 µm into the silicon substrate. Then through lapping the silicon substrate is thinned down until the trenches are met and a borosilicate glass wafer is anodically bonded onto the backside to form the substrate. Hereby, avoiding having to form titanium disilicide, $TiSi_2$ on quartz while maintaining the insulating glass substrate.

Chapter 9

Conclusion and outlook

This thesis presents the research conducted in the Ph.D. project titled "Micromachined 2D Transducers for 3-D Super Resolution Ultrasound Real-Time Imaging of Erythrocytes". The primary objective of this project was to develop large-scale 2D row-column-addressed capacitive micromachined ultrasonic transducer (CMUT) arrays for 3D super-resolution imaging. This objective was accomplished by designing, developing and fabricating two large-scale row-column-addressed (RC) arrays of RC190+190 elements and RC512+512 elements. The arrays are designed with a $\lambda/2$ element pitch and a center frequency at 8 MHz and 15 MHz, respectively. Both chips are fabricated utilizing the robust anodic bonding technique incorporating gold bottom electrodes that allow for scaling the RC190+190 array to RC512+512 to maintain the image quality as the chip area scales. The RC190+190 chip was electrically characterized and subsequently mounted, wire bonded and cast into an interchangeable nose piece incorporated into the prototype probe enabling high-resolution volumetric imaging in real-time for earlier detection of cancer and vascular-related diseases.

Conclusion

For the goal of achieving a large-scale 2D RC CMUT, with the anodic bonding process, different metals have been evaluated for the bottom electrodes. The chosen metal should have a low resistivity in order to minimize the delay line effect and satisfy the so-called ωRC criterion, ensuring a uniform pressure distribution throughout the entire element. This criterion helps in selecting the appropriate top and bottom electrode material and dimensions for large-scale arrays. Furthermore, the metal should be compatible with the fabrication process.
Chromium, aluminum, and gold, commonly used metals in the semiconductor industry with low resistivity, were selected for CMUT fabrication. Chromium, with a resistivity of $15 \times 10^{-6}\,\Omega$cm, proved to have a higher ωRC value, rendering it unsuitable for large-scale arrays. Furthermore, chromium showed incompatibility with plasma ashing and mild etching in piranha clean, with an etch rate of 16 nm/min. Consequently, chromium was excluded from consideration for the RC1024+1024 primarily due to not fulfilling the ωRC criterion. However, the use of chromium could be an intermediate step and utilized for a second generation of RC512+512. Aluminum has an even lower resistivity of $2.7 \times 10^{-6}\,\Omega$cm and was already utilized as the top electrode. Unfortunately, aluminum is not compatible with piranha cleaning with an etch rate above 5200 nm/min. Also, anodic bonding with aluminum in the

glass cavities resulted in dendritic and fractal formation in the metal. The fractals and dendritic structures became more prominent with increased applied bias during anodic bonding experiments performed by the author. The fractals were even observed at voltages as low as 200 V, making aluminum unsuitable as a bottom electrode material. The implementation of a 30 nm titanium diffusion barrier layer prevented the formation of these fractals and dendritic structures and seems promising for future studies. Gold has a low resistivity of $3.15 \times 10^{-6}\,\Omega$cm (measured) and, being a noble metal is not etched in piranha. Gold is compatible with the entire process flow. The gold bottom electrodes yield an ωRC value that facilitates scaling up to an RC1024+1024 CMUT, which is the ultimate goal of the SURE project. Yet, gold evaporation is prone to so-called spitting forming gold particles up to 2 µm in diameter correlated with short circuits in the CMUT, detrimental to the yield.

Consequently, gold bottom electrodes were chosen for the preferable low resistivity and compatibility with plasma ashing and piranha cleaning. The CMUT array was designed with a $\lambda/2$-element pitch and a cell side length of 37 µm. Optimization of a short wet gold etch was implemented to remove the gold ribbons which are commonly formed during ion beam etching. Large arrays can now be fabricated using the optimized fabrication process and allow a high structural chip yield, which has been a severe problem for the large silicon-based row column probes performed by this research group. The PSOI wafer technology, utilized for the top plate of the CMUT, has been optimized to achieve high-quality and void-free bonding up to an area of 7 cm × 7 cm enabling future RC1024+1024 chips to be realized and demonstrated by this work. One of the implemented process optimizations was an increase in the inter-element kerf from 2.5 µm to 6 µm to reduce the number of short circuits between the top-to-top elements. The number of short circuits between top-to-top elements was reduced from 46 to only 2 in the current RC190+190 array, compared to the previous generation RC190+190 array (TH1-A). In total eight 2D RC190+190 CMUT arrays were finalized and electrically characterized which gave an average element yield of 90 %. An RC190+190 array was mounted into a novel prototype probe and acoustically characterized. The preliminary acoustical measurement on a single row element showed a fractional bandwidth of 145 % and a center frequency of 10 MHz. The pressure uniformity was approximate 88 % measured at the end of the element.

The last remaining obstacle is the top-to-bottom short circuits which have been identified and characterized by FIB-SEM on the finalized RC190+190 wafer. FIB-SEM characterization has shown defects of the gold bottom electrode bridging the vacuum gap and entering the poly-silicon top plate, despite the 180 nm insulating oxynitride, short-circuiting the top and bottom electrodes of the CMUT. Backside high-resolution microscope images of the bottom electrodes reveal dark spots with a surrounding discoloration halo, which directly correlate with the short circuits between the top and bottom electrodes measured through impedance measurements. Comparing same-location microscope images after metallization and after anodic bonding indicate that particles from metal deposition might be precursors of these short circuits. Conclusively, there are 65 dark spots per cm^2 of the bottom electrode area that is 0.08 % of the cells that are short-circuited. For the RC16+16 array which was measured, this resulted in 40 % short-circuited elements, which severely limits the electrical yield.

The second part of this thesis presented the specialized stereolithography 3D-printed hydrogel phantoms. Both micro-flow and scatter phantoms have been fabricated with unrivaled micrometer precision of the channels and scatters. The 3D point-spread-function scatter phantom has enabled our collaborators at the CFU research group to prove that row-column probes have superior resolution compared to translated linear array probes in volumetric imaging. Moreover, the 205 µm wide single-channel micro-flow phantom was used to validate a theoretical model aimed at compensating for the underestimated velocity in 2D super-resolution ultrasound. Additionally, a novel micro flow phantom was designed with two tapered V channels, enabling direct visualization of super-resolution capabilities independent of frequency and probe for future studies.

The third part of this thesis presented the work on a novel quartz fusion titanium disilicide ($TiSi_2$) process flow for CMUT fabrication. The process relies on a so-called POOQ wafer utilized for both the top and bottom wafer of the CMUT. Three out of four requirements were proven by fabricating POOQ wafers, subsequently performing LOCOS and fusion bonding at a temperature below 1000 °C to preserve the low resistivity of $TiSi_2$. With the available tools in the DTU Nanolab clean room, it is currently not possible to fabricate high-quality, uniform and low resistivity titanium disilicide, even though, silicide formation has been proven previously. While the concept of a CMUT composed entirely of glass with a $TiSi_2$ bottom electrode with low resistivity is promising, it is not yet facilitated by the equipment. This quartz fusion titanium disilicide CMUT would theoretically allow the realization of an RC1024+1024 in accordance with the ωRC design criteria.

Outlook

In the short term, the RC512+512 wafer fabrication should be finalized and subsequently, electrical and acoustical characterization should be performed on this largest-of-its-kind array.
Furthermore, more of the fabricated RC190+190 arrays should be mounted in the prototype probe, despite the top-to-bottom short circuits, and full acoustic characterization should be performed. Acoustical pressure maps should be measured to obtain further insight into the success of the optimization regarding the bottom electrode design to maintain an even pressure distribution along the elements.
Future work should continue to investigate vertical short circuits between the top and bottom electrodes. This phenomenon, described in this thesis of gold penetrating into the top plate in spite of the vacuum gap and insulating oxynitride layer, necessitates a line of different metals to be tested. A study of the occurring reactions during anodic bonding should be examined. A range of experiments where cavities have been etched in the glass substrate and different metals defined as bottom electrodes should undergo anodic bonding at different temperatures and voltages. To analyze the effect, backside microscope inspection of the metal should be performed pre- and post-anodic bonding and determine if dark spots with surrounding discoloration occur. Once bonded FIB-SEM characterization should be performed. One metal that might be suitable is Molybdenum, Mo, with a low resistivity of $5.34 \times 10^{-6}\,\Omega$cm and is known to form smooth thin films. Molybdenum deposition is possible with both e-beam evaporation and sputter deposition and could be etched with ion beam etching. Considering the scaling prospects, molybdenum bottom electrodes of 250 nm can facilitate an RC512+512 CMUT with 86 % of the signal preserved at the end

of the element. Additionally, process-compatible metal diffusion inhibiting layers should be examined and possibly implemented on the bottom electrode or as a part of the dielectric insulation layers. In the pursuit of realizing these large-scale 2D RC CMUT arrays this challenge is the last known remaining obstacle.

Acronyms

BHF buffered hydrofluoric acid

BOX Buried Oxide layer

CCB Chip Carrier Board

CFU Center for Fast Ultrasound Imaging

CMP chemical mechanical polishing

CMUT capacitive micromachined ultrasonic transducer

EDX Energy-Dispersive X-ray spectroscopy

EMI Electromagnetic interference

FIB-SEM Focused Ion Beam Scanning Electron Microscope

HEPA high-efficiency particulate air filter

IBE ion beam etching

KU Københavns Universitet

L-Edit L-Edit layout designer (Tanner Tools), CAD software

LAP lithium phenyl-2,4,6-trimethylbenzoylphosphinate

LOCOS local oxidation of silicon

LPCVD low pressure chemical vapor deposition

MLA maskless aligner

NAVMI non-dimensionalized added virtual mass incremental factor

NESW North, East, South, West

PDMS Polydimethylsiloxane, polymer

PEGDA poly(ethylene glycol) diacrylate

PES Aluminium etchant Phosphoric Acid mixture, PES-77-19-4

poly-Si polysilicon

POOQ polysilicon-on-quartz

PSOI polysilicon-on-insulator

QY quinoline yellow

RIE reactive ion etching

RoHS Restriction of Hazardous Substances Directive

SEM Scanning Electron Microscope

snr Signal to Noise Ratio

SOI Silicon-on-Insulator

SURE Super Resolution Ultrasound Real Time Imaging of Erythrocytes in 3-D

TOBE Top-orthogonal-to-bottom-electrode

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Appendix A

Process flows

A.1 Anodic bonding Process Flow

Process flow title			Revision
Anodic bonded CMUT with insulating oxynitride			**V4**
	Contact email kitste@dtu.dk	Contact person Kitty Steenberg	Contact phone +4528892964
	Labmanager group	Batch name TH1 – Transducer Human 1	Date of creation	Date of revision 04-08-2022

Objective

Batch name: RCABCMUT

The purpose of the project is to fabricate Capacitive Ultrasonic Transducers using an anodic bonding process via a homemade SOI wafer, with addition of an oxynitride membrane. This process flow is for experienced user for RCABCMUT.

Substrates

Substrate	**Orient.**	**Size**	**Doping/type**	**Polish**	**thickness**	**Box**	**Purpose**	**#**	**Sample ID**
Silicon	<100>	4”	n (Phos.)	DSP	350±15µm		Top plate	25	SN611, SN595
Boron glass		4”	p (Boron.)	DSP	500±10µm		Bottom plate	25	SB 589

Comments:

Fabrication process for bottom plate:

Step	Heading	Equipment	Procedure	Comments
1	Preparation for Bottom electrode fabrication			All borofloat wafers
1.1	Wafer selection	Wafer box	Use the dedicated vacuum tweezer at the wafer locker	Note the wafer IDs and box: TH1_YYYYMMDD _XX All further handling of the wafers should be limited to only vacuum-tweezers unless otherwise unavoidable
2	Cr deposition as masking layer for cavity etch			All borofloat wafers
2.1	Cr deposition by E-beam evaporation	Temescal	**Recipe:** Cr **Deposition rate:** 10 Å/s **Final thickness:** 50 nm	All borofloat wafers.
3	Lithography process 1 – Cavities pattern			All borofloat wafers
3.1	Spin coating	Gamma UV	AZ MiR 701 positive resist 2 µm with HMDS **Recipe:** 1421 - DCH 100mm MiR 701 2um HMDs **Cleaning wafer:** 0400 100mm Coater Clean	Clean spinner nozzle and run the dummy wafers – inspect dummy wafer in white light Stop: Large comets & particles
3.2	Exposure	MLA-3 aligner	**Mask:** CAV **Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm	See PP Mask Polarity This is a positive mask used as is.
3.3	Develop	TMAH UV developer	**Recipe:** 3001 DCH 100mm PEB60s@110C SP60s	Looked fine with 1 min vs 2 min PEB
3.4	Inspection	Optical microscope	Check pattern	Stop: Delamination, defects in the center.
4	Cr mask etch			All borofloat wafers
4.1	Cr etch	Cr etch 18 in beaker	Cr etch 18 **Time:** 1:00 min	Easy to see when etch is finished as glass will be clear. Re-use Cr etch 18.
4.2	Inspection	Optical Microscope	Ensure no under etch	Stop: If it's not squares with connectors
5	Cavity etching			All borofloat wafers
5.1	Cavity etch	BHF plastic beaker	**Etch rate:** ≈24 nm/min **Etch time:** 16.5 min **Target depth:** 400 nm	Preferable to batch etch to keep cavity depths the same Variation observed
5.2	Inspection	Camera		Name: 00X_TH1XX_Process_XX, the 00X is sequentially numbered
6	Removal of masking layers			All borofloat wafers

6.1	Resist strip	Resist strip wet bench	**Time:** 10 min with ultrasonic agitation	
6.2	Cr removal	Cr etch 18 in beaker	**Etch time:** 1-2 minutes **Etch rate:** ~50-100 nm/min	Wafers need to be completely transparent when done
6.3	Inspection	Optical microscope		See if pattern is good, and see whether all Cr is gone Stop: If the cavities are not well-defined squares - see Kitty picture
6.4	Inspection	Dektak XT		Preferable measure on all wafers in the same spot. Contact pads in the wafer center – NESWC – Move up before piranha Less handling
6.5	Inspection	Camera		Name: 00X_TH1XX_Process_XX, the 00X is sequentially numbered
6.6	Cleaning-Piranha	Piranha in a beaker	Sulfuric acid H2SO4 (98%) and peroxide H2O2 (30%) in the ratio 4:1 Temp: 70-80C Time: 10 min	First add H2SO4 into a glass beaker then add H2O2. Ensure no organics/resist before bot electrode
7	**Bottom electrode metal**			
7.1	~~Dehydration~~	~~250°C Oven~~	~~**Time:** 2-5 h~~	~~Optional, recommended~~ Particle contamination~~?~~
7.2	Deposit Ti/Au	Temescal	**Recipe:** Ti/Au **Final thickness Ti/Au:** 220 nm **Ti deposition rate:** 5 Å/s **Au deposition rate:** 1 Å/s	In this step, the Au thickness can be adjusted to fit a specific gap height. Low deposition rate to minimize particles
7.3	Inspection	Optical microscope	Darkfield inspection look for metal particles	Stop: If you see many large Au particles all over the wafer
8	**Lithography process 2 – Bottom electrode**			
8.1	Spin coating	Gamma-UV	**Recipe:** 3411 - DCH 100mm 5214E 1,5um HDMS	Clean spinner nozzle and run 2-3 dummy wafers – inspect dummy wafer in white light Stop: Large comets & particles
8.2	Exposure	MLA-3 aligner	**Mask:** BOT **Exposure dose:** 80 mJ/cm^2 **Defocus:** -2 **Laser:** 405 nm **Mode**: Quality **Mode:** Fast – more serpentine	See PP Mask Polarity This is a positive mask used as image reversal. The polarity is reversed during bake and flood exposure to protect the metal in the cavities. Overexposure to avoid stitching
8.3	Develop	TMAH UV developer	**Recipe:** 2002 DCH PEB 110 C 120 s	Post exposure bake → not sensitive
8.4	Exposure	Aligner: MA6-2	**Exposure dose:** ≈198 mJ/cm^2 **Time:** 18 @ 11 mW/ cm^2	Flood exposure of wafer

8.5	Develop	TMAH UV developer	**Recipe:** 1002 DCH 100 mm SP 60 s	
8.6	Inspection	Optical microscope	Inspection look for metal particles	Check that resist pattern is well defined inside cavities. Use dark field to make edges more visible.
8.7	Inspection	Camera		Name: 00X_TH1XX_Process_XX, the 00X is sequentially numbered
9	Dry etching – Bottom electrode			
9.1	Etching Au	IBE/IBSD Ionfab 300	**Recipe:** Au acceptance –angle **Etch time:** 5:15 min for 10nm/210nm Ti/Au	Etch time will depend on the metal thickness. You don't want to much over etch. Time it with a dummy wafer. 10 nm Ti etched in 1 min. Ensure that the clamps are not brittle and that they press the wafer down to be cooled otherwise the wafer will burn!
9.2	Inspection	Optical microscope	Ensure that elements are isolated	Do not dismount from IBE chuck while inspecting
9.3	Inspection	Camera		Name: 00X_TH1XX_Process_XX, the 00X is sequentially numbered
9.4	**Etch ribbons**	Gold etch in beaker	Kalium Iodine gold etch: KI:I2:H2O - 200g:50g:1000ml **Etch time**: 2 s	**This step is to remove ribbons – redeposit from IBE** Gold etch is reused – dip into etch and pull out immediately and into QDR to avoid under etching
9.5	**Inspection**	Optical microscope	Note down connecting wire width	Check under etch
9.6	**Resist strip**	Plasma asher 1	**Pressure:** 0.8-1.0mbar. **Gas:** O2: 400 ml/min, N2: 70 ml/min **Power:** 500 W **Time:** 10-15 min	Remove top layer of resist damaged by IBE
9.7	**Inspection**	Optical microscope	Note down connecting wire width	
9.8	Resist strip	Resist strip wet bench	**Time:** 25 min with ultrasonic agitation This step might be necessary to repeat several times to remove resist (x3-5). Preferable keep the wafers submerged (and wet) as long as possible to avoid stiction and redeposition of particles.	Check wettability when pulled from bath to determine if resist residues are present

9.9 **Inspection**	Optical microscope	Note down connecting wire width Check that pattern is well defined inside cavities. Use dark field to make edges more visible. Check that there is no resist (residue) left.	Stop: If you see metal ribbon/filaments short-circuiting the bottom electrodes
9.10Inspection	Camera		Name: 00X_TH1XX_Process_XX, the 00X is sequentially numbered
9.11Inspection	Dektak XT	Measure final gap and metal height	All wafers at the same point on the wafer: the NE contact pad at RC1,2,3,4 Stop: Large particles within cavities

Fabrication process for anodic bonding of PSOI top plate:

Step Heading	Equipment	Procedure	Comments
10 Preparation			**All PSOI wafers**
10.1Wafer selection	Wafer box	Take the wafers from the storage and put them in a wafer box.	Note the wafer IDs and box: WAFR_YYYYMMDD_PSOI_XX
11 Deposition SOI			**All PSOI wafers**
11.1 RCA clean	RCA (4",6")	All wafers including test wafers should be RCA cleaned	Include a Si particle scan + furnace test wafers Flush both bath (x2) and cannisters with water and dump it immediately
11.2 SiO2 dry oxidation – BOX layer	Phosphor Drive-in (A3)	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. **Recipe:** DRY1100 **Time:**12 h 30 min **Target thickness:** 500 nm	Approximately 500 nm or approximately 12 hours and 30 minutes. The 500 nm is a thickness that previously has been sufficient for many fabrications. However, if the handle wafer is removed entirely by dry etching, it might be a good idea to use a thicker (wet) oxide on the order of 1 µm, to ensure acceptable etch stopping properties
11.3 Measure thickness	Filmtek and VASE	Measure thickness on the Filmtek and VASE and note the result with MSE/RSME and recipe used	Furnace test wafer Save this data so that it can be fitted for the model when measuring Poly-Si
11.4 Poly-Si deposition – Device layer	LPCVD Poly-Si (4") (B4)	Place a test wafer in the center of the boat and place device wafers and eg. test wafers equally distributed on each side of the test wafer. No spacing between wafers. Fill up with dummy wafers for boron doped poly.	Deposition of device layer. Remember, you are not allowed to deposit continuously for more than 3 hours (corresponding to

		Recipe: POLYBOR **Time:** 5 h 48 min **Target thickness:** 3 µm Always adjust the furnace time according to the deposition rate in the process log on labmanager Note down target and measured thickness Target thickness varies and should be +~100 nm to final thickness post CMP	approximately 2 µm). Hence, if you want 3 µm poly it is advantageous deposit 2×1.5 µm rather than first 2 µm and then add 1 µm on top. The reason being the thin film measuring equipment (FilmTek, Ellipsometer) becomes less precise for large film thicknesses on furnace test. We do SEM cross section thickness now on our own PSOI also.
11.5 Measure thickness	Filmtek and VASE	Measure thickness on the Filmtek and VASE and note the result with MSE/RSME and recipe used Filmtek recipe: PolySi(3my) on SiO2 thick PSD2 Vase recipe: PSOI_model	Furnace test wafer Use the SiO2 data to fit the BOX layer if you have carried on the wafer from the oxidation
11.6 Measure thickness	SEM	Cross-section – Pre CMP Measure: device layer & BOX thickness CNESW **Lens:** InLens **Magnification:** 25kX, **Bias:** 5kV	1 PSOI
12 Chemical Mechanical polishing (CMP)			**All PSOI wafers**
12.1 Storage during CMP	Plastic Beaker	Put wafers in a plastic beaker filled with water and use a holder that fits all wafers you want to polish in the subsequent step. Transport the beaker to the Polisher/CMP	Make a chemical note stating water
12.2 Polishing	CMP	**Recipe:** cmut_kitste **Time:** 1 min 30 s or 3 min – this is adjusted in step 2 which has a 13 s off set for the carrier to reach to plate. Therefore, 1 min and 30 s polishing is set to be 1 min 43 s in step 2	Insert shim's and napcon to approx. + 30 µm and measure CNESW note down and comment concave/convex in logbook Brush conditioning should be done right before polishing Take the wafers from the water filled beaker into the CMP, and afterwards put the now polished wafer back into the water filled beaker. Repeat this process for all the wafers in your holder. Be aware of different hydrophilic properties on the surface after the polishing, such variation can imply particle contamination. Hence, check the wetting

			properties after the clean, and verify these properties are uniform across the wafer surface.
12.3 Piranha	Beaker 1	Recipe: H2SO4:H2O2 in the ratio 4:1. Time: 30 min	First Sulfuric acid (H2SO4) and then hydrogen peroxide (H2O2) in the ratio 4:1. We have our own beaker for this on our shelf called Piranha 1.
12.4 Rinse	QDR	Recipe: 1	Use the rinse program with spray cycles. Do not dry the wafers, transport them to Oxide etch 2: BHF while they are wet
12.5 Oxide etch	BOE in beaker	Time: 10 min for Poly-Si	Use the beaker used for storage
12.6Rinse	QDR	Recipe: 1	Use the rinse program with spray cycles. Do not dry the wafers.
12.7Piranha	Beaker 2	Recipe: H2SO4:H2O2 in the ratio 3:1. Time: 30-60 min	First Sulfuric acid (H2SO4) and then hydrogen peroxide (H2O2) in the ratio 3:1. We have our own beaker for this on our shelf called Piranha 2.
12.8Rinse	QDR	Recipe: 1	Use the rinse program with spray cycles.
12.9Spin dry	Spin dryer		Leave in for 30 s when program is stopped to dry completely.
13 Characterization			**1 PSOI**
13.1Particle Scan	KLA Tencor SurfScan 6420	**Recipe**: 4IN_POLY_SI **Gain:** 4 (800nm-8.3µm), 5 (300nm-1.3µm), S-S Polarized Note down particle count at gain	Ensure that the PSOIs are clean
13.2 Measure roughness	AFM Icon-1	QNM tapping mode **Scan size:** 1-2 µm, 1 Hz Rq < 1 nm Rmax < 5-10 nm	Note down: material and CMP process along with Rq XX nm, Ra XX nm, Rmax XX nm Measure at least C and one edge point N/S/E/W Valleys are ok, peak no-go
13.3 Measure thickness	SEM	Cross-section – Pre CMP Measure: device layer & BOX thickness CNESW **Lens:** InLens **Magnification:** 25kX, **Bias:** 5kV	1 PSOI - The exact plate thickness, h of the CMUT after polishing
14 Oxy nitride			**All PSOI wafers**
14.1RCA clean	RCA (4",6")	All wafers including test wafers should be RCA cleaned	Include a Si particle scan + furnace test wafers Flush both bath (x2) and

			cannisters with water and dump it immediately
14.2Particle Scan	KLA Tencor SurfScan 6420	**Recipe:** 4IN_POLY_SI **Gain:** 4 (800nm-8.3µm), 5 (300nm-1.3µm), S-S Polarized Note down particle count at gain	Kitty will ask if this is okay to go into C1 furnace after particle scan
14.3SiO2 dry oxidation	Furnace (C1) - Anneal-oxide	Place a test wafer in the center of the boat and place device wafers and e.g. test wafers equally distributed on each side of the test wafer. No spacing between wafers. **Recipe:** DRY1000, **Ox time:** 15 min, anneal 20 min **Target thickness:** 20 nm	
14.4Nitride deposition	Furnace (B2) - LPCVD Nitride 4"	**Recipe**: NITRIDE4, **Time:** 60 min **Target thickness:** 200 nm	Maybe thicker according to electric field during anodic bonding
14.5SiO2 wet oxidation	Furnace (C1) - Anneal-oxide	Place a test wafer in the center of the boat and place device wafers and e.g. test wafers equally distributed on each side of the test wafer. No spacing between wafers. **Recipe:** WET1100, **Ox time:** 3 hours, anneal 20 min **Target thickness:** 920 nm (test wafer)	
14.6Measure thickness	SEM	Cross-section – Oxynitride Measure: BOX, device layer and oxynitride CNESW **Lens:** InLens **Magnification:** 25kX, **Bias:** 5kV	CNESW – The final plate and insulation thickness
15 Structuring the oxynitride			**All PSOI wafers**
15.1Spin coat	Gamma UV	1421 - DCH 100mm MiR 701 2um HMDS	
15.2Exposure	MLA3	**Mask:** **Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm	Open holes for contact pads in the oxynitride for alignment bonding
15.3Developer	TMAH UV-Lithography	3001 DCH 100mm PEB60s@110C SP60s	
15.4Dry etch Nitride	AOE	**Recipe:** SiO2_res **Time:** 3 min **Temp:** 0 C	Cool time 20-30 min
15.5Resist strip	Plasma asher 2	**Time:** 45 min **Gasses:** O_2 400 ml/min, N_2 70 ml/min **Power:** 1000 W	
15.6Measure roughness	AFM Icon-1	QNM tapping mode **Scan size:** 1-2 µm, **Frequency:** 1 Hz Rq < 1 nm Rmax < 5-10 nm	Note down: material and CMP process along with Rq XX nm, Ra XX nm, Rmax XX nm Measure at least C and N/S/E/W Valleys are ok, peak no-go

15.7Inspection	Camera		Name: 00X_TH1XX_Process_XX, the 00X is sequentially numbered

Fabrication process for anodic bonding of top and bottom plate:

Step Heading	Equipment	Procedure	Comments
16 Cleaning before wafer bonding			**All wafers**
16.1 Inspection - Roughness	AFM	QNM tapping mode **Scan size:** 1-2 µm, **Frequency:** 1 Hz Rq < 1 nm Rmax < 5-10 nm	Check sub-nm roughness prior to bonding – top and bottom
16.2RCA clean	RCA (4",6")	ONLY RCA1	**All top plates** Include a Si particle scan Flush both bath (x2) and cannisters with water and dump it immediately Only RCA1 due to particle concern and without HF dip, so oxynitride is not etched.
16.3Cleaning-Piranha	Piranha in a beaker	Sulfuric acid H2SO4 (98%) and peroxide H2O2 (30%) in the ratio 4:1 **Temp:** 70-80°C **Time:** 10 sec We are currently unsure if this step is needed at all. Under etch of bottom electrodes is a risk factor.	**All borofloat wafers**. First add H2SO4 into a glass beaker then add H2O2. Consider if this step is necessary as the piranha might etch the Ti adhesion layer. If used, the solution should be stirred properly either with a hotplate or by hand. Only a short clean is likely needed. Alternatively, acetone (maybe with US), IPA and water might be enough to remove residue.
17 Wafer bonding			**All wafers**
17.1Alignment bonding	Aligner: MA6-2 & Wafer bonder 02	MA6-2 is converted to alignment pre-bonder and the procedure in the manual is followed. Check that all O-rings are in place. **Load:** 1) PSOI silicon top wafer is loaded first with bonding interface down, 2) then the bottom glass substrate. **Alignment distance:** ≈ 100-150 µm Include graphite sheet to avoid isotropic holes	Put on a new pair of gloves on top of your others. If possible, pre-orientate wafer flats of both top and bottom in boxes. Take wafers out under HEPA filters to avoid particles. Smallest

		during etching in KOH according to test by rkch and kitste	alignment distance depends on wafer bow and particles. Bottom and top plate directly from the cleaning process.
17.2Anodic bonding	Wafer bonder 2	**Recipe:** CMUT/anodic bond 4-inch 600V align **Voltage steps:** -150V -300V, -600V, at 350°C Note down total charge	Check that the center pin touches the wafers Maybe lower voltage?
17.3 Inspection	Optical microscope	Inspecting for voids and electrode damages	Look for defects, also near edges Stop: Major voids on all large arrays + edge possibly tear off the plate in KOH
17.4 Inspection	Camera		Name: 00X_TH1XX_Process_XX
18 Handle and box layer etching			**All bonded wafers**
18.1Crystal bond	Hotplate: 90-110°C	Dummy wafer is put facing up on tissue paper on hotplate. Crystal bond is applied from the center and out in a circular motion. Bonded wafer is placed on top with glass-side facing down. Stack is removed from hotplate and cooled down. **Recipe:** Standby 90°C, Pins down	Spread crystal bond evenly and do not apply too much, so that it spills out. After cooling, check that wafer stack is bonded.
18.2Nitride etch	ASE	Etch oxynitride layer away from top **Recipe:** MEMS/KITOXYSI, **Gasses:** C4F8: 13 sccm, **Power:** Coil: 1300W, Plat: 200W, **Etchtime:** 3 min at 20°C, with 180 nm oxynitride	Visible color change is seen when etch is completed. Color should resemble Si. Almost 10x faster than maengsin
18.3Crystal de-bond	Hotplate: 90-110°C	Bonded stack is placed on hotplate and device wafer is slid off dummy wafer using a tweezer (or by pushing the edge with your finger). Both wafers are wiped with wet napkins and sprayed with a water gun to remove wax. **Recipe:** Standby 90°C, Pins down	
18.4 Inspection	Camera		Name: 00X_TH1XX_Process_XX
18.5 Poly-Si layer	Si KOH etch 3	Etch top (not useable) device layer away. **Process 4:** 90°C **Etch time:** 2-5 min for a thickness of 2-3 µm Adjust concentration of KOH bath every time before use. Very important that all of the Poly-Si is gone, better to over etch in this step.	Time depends on the thickness of the poly-Si on the PSOI wafer. Will stop bubbling. Remember 40 min heat-up time. Ensure that ALL of the poly-Si plate is removed otherwise it will translate down through the stack and possibly ruin chips as the leftover accumulates through the process

18.6 Inspection	Camera		Name: 00X_TH1XX_Process_XX
18.7 Oxide etch	BHF	Plastic beaker inside fume hood Etch of non-useable box layer. **Etch rate:** 75 nm/min. **Etch time:** 6-10 min for 400-500 nm SiO2	Time depends on the thickness of the oxide on the PSOI wafer. Surface is hydrophobic when etch is done Ensure that ALL the oxide is removed otherwise it will translate down through the stack and possibly ruin chips as the leftover accumulates through the process
18.8 Inspection	Camera		Name: 00X_TH1XX_Process_XX
18.9 Si etch	Si KOH etch 3	Etch handle layer away **Process 4:** 90°C **Etch rate:** 1.7µm/min **Etch time:** 3 hours 15 minutes for a thickness of 350 µm If concentration is adjusted at the start of the process the etch might take longer time and running at 90 °C for longer is preferred. OBS! Kitty observed isotropic holes during the last batch TH1_20220322 and through experiments with Nanolab it was discovered that these comes from the anodic bond, be extremely careful and check the wafers regularly as the holes are superfast etching and might rip off the plate and ruin the entire wafer	This is a critical step of the process flow. Recommended to check how the wafers look regularly during the step, also removing it from the bath to check. Keep an eye on the wafer in the last 30 min. Alternatively use process 3: 80°C after 2 h 30 min. The concentration might change during the long etch and increase etching time needed Stop: If plate defects occur. Assess whether the main arrays are salvageable.
18.10 Inspection	Camera		Name: 00X_TH1XX_Process_XX
18.11 Oxide etch	BHF	Plastic beaker inside fume hood Etch of not useable box layer. **Etch rate:** 75 nm/min. **Etch time:** 6-10 min or a thickness of 400 nm	Time depends on the thickness of the oxide on the PSOI wafer. Surface is hydrophobic when etch is done. Ensure all oxide is etched away.
18.12 Inspection	Camera		Name: 00X_TH1XX_Process_XX
18.13 Cleaning-Piranha	Piranha in a beaker	Sulfuric acid H_2SO_4 (98%) and peroxide H_2O_2 (30%) in the ratio 4:1. **Temp:** 70-80°C	First add H2SO4 into a glass beaker then add H2O2. To remove potassium ions and more.
19 Lithography – Alignment mark access			**All bonded wafers**

19.1Coat wafer	Gamma UV	**Resist:** AZ MiR 701 positive resist **Recipe:** 1411- DCH 100mm MiR 701 1.5 um HMDS	2 dummy wafers. Stop: Large comets & particles
19.2Exposure	MLA-3 aligner	**Mask:** Align **Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm	Contrast is not very good in this step. Squares or circles can be drawn in drawmode using the overhead camera in MLA.
19.3Develop	TMAH UV developer	**Recipe:** 3001 DCH 100mm PEB60s@110C+SP60s	
19.4Inspection	Optical microscope	Check pattern and alignment marks.	Ensure that resist covers electrodes uniformly
20 Etch - Alignment mark access			**All bonded wafers**
20.1Crystal bond	Hotplate: 90-110°C	Dummy wafer is bonded to glass-side of device wafer. **Recipe:** Standby, Pins down	After cooling, check that wafer stack is bonded. It might not be necessary at this step to do crystal bonding. The ASE might clamp the wafers fine.
20.2Device layer etch	ASE	Dry etching through Poly Si stopping on nitride. 4-5 cycles, **Recipe:** shallolr OBS! Pop voids before ASE	OBS! Pop voids before ASE 2 cycles might be enough for 2.2 µm plate
20.3Crystal de-bond	Hotplate: 90-110°C	Bonded stack separated on hotplate and cleaned with water on napkin. **Recipe:** Standby, Pins down	Remaining wax is likely removed in plasma asher 1
20.4Resist strip	Plasma asher 1	Photoresist stripping **Pressure:** 0.8-1.0mbar. **Gas:** Mixture of O2 and N2. **Power:** 1000watts. **Time:** 30-45 min	
20.5 Inspection	Camera		Name: 00X_TH1XX_Process_XX
21 Top electrode deposition 1			**All bonded wafers**
21.1Deposition Al	Temescal	**Recipe:** Al **Final thickness Al:** 200nm **Deposition rate Al:** 10 Å/s	
22 Lithography – Top electrode			**All bonded wafers**
22.1Coat wafer	Gamma UV	**Resist:** AZ MiR 701 positive resist **Recipe:** 1421 - DCH 100mm MiR 701 2um HMDS	Clean spinner nozzle and run 1-2 dummy wafers. Spin coat as soon as possible after metal deposition Stop: Large comets & particles
22.2Exposure	MLA-3 aligner	**Mask:** OPE-Poly **Exposure dose:** 320 mJ/cm^2 **Defocus:** 0 **Laser:** 405 nm	See PP Mask Polarity This is a positive mask used as is.

22.3Develop	TMAH UV developer	**Recipe:** 3008 DCH 100mm PEB120s@110C SP60s	
22.4 Inspection	Optical microscope	Check pattern and alignment marks.	Stop: If bottom electrode pad openings are not well-defined
22.5 Inspection	Camera		Name: 00X_TH1XX_Process_XX
23 Etch – Opening to bottom electrode			**All bonded wafers**
23.1Al wet etch	PES solution in beaker	Etch of pure aluminum. **Etch rate:** ≈ 45-60nm/min. **Etch time:** ≈ 6 min.	Mix the solution with the wafer holder when starting the etch, as it is quite viscous. Visual feedback when done etching
23.2Inspection	Optical microscope	Inspection of aluminum etch.	Stop: If metal is not etched. Check in microscope and continue etch is necessary. A bit of underetch is okay
23.3Resist strip	Plasma asher 1	Photoresist stripping **Pressure:** 0.8-1.0mbar. **Gas:** 400 O2 and 70 N2. **Power:** 1000 watts. **Time:** 45 min	
23.4 Inspection	Camera		Name: 00X_TH1XX_Process_XX
23.5Crystal bond	Hotplate: 90-110°C	Dummy wafer is bonded to glass-side of device wafer. **Recipe:** Standby, Pins down	After cooling, check that wafer stack is bonded.
23.6Device layer etch	ASE	Dry etching through Poly Si. **Time:** 5 cycles, **Recipe:** shallolr **Temp:** 20C	
23.7Crystal de-bond	Hotplate: 90-110°C	Bonded stack separated on hotplate and cleaned with wet tissue paper. **Recipe:** Standby, Pins down	Careful not to get water of the front-side. Remaining wax is removed in plasma asher 1
23.8 Inspection	Optical microscope	Ensure that contact pads are open	Name: 00X_TH1XX_Process_XX
23.9 Inspection	Camera		Name: 00X_TH1XX_Process_XX
24 Top electrode metal			**All bonded wafers**
24.1Deposit Al	Temescal	**Recipe:** Al **Final thickness Cr:** 800 nm **Al deposition rate:** 10 Å/s	The bottom electrode cavities are plugged with aluminum in this step. Clean the wafers with a nitrogen air gun before this step. Make IBE test wafers.

24.2Inspection	Optical microscope	Inspection of plugged cavities	
25 Lithography – Separation of top electrodes			**All bonded wafers**
25.1Coat wafer	Gamma UV	**Resist:** AZ MiR 701 positive resist **Recipe:** 1411- DCH 100mm MiR 701 2 um HMDS	Clean wafers with a nitrogen air gun before this step. Clean spinner nozzle and run 1-2 dummy wafers. Stop: Large comets & particles.
25.2Exposure	MLA-3 aligner	**Exposure dose:** 320 mJ/cm^2 **Laser:** 405 nm **Defocus:** 0 **Mask:** TOP	See PP Mask Polarity This mask needs to be reversed, so the metal can be exposed and etched to separate top from bottom electrodes.
25.3Develop	TMAH UV developer	**Recipe:** 3008 DCH 100mm PEB120s@110C SP60s	
25.4Inspection	Optical microscope	Check pattern and alignment marks for particles.	Stop: Large comets & particles.
25.5 Inspection	Camera		Name: 00X_TH1XX_Process_XX
26 Etch – Top electrode metal			**All bonded wafers**
26.1Etching Au	IBE/IBSD Ionfab 300	**Recipe:** Al etch with resist **Etch time:** ≈ 50 min for 1000 nm Al Split the etch up in 2-3 steps and let the wafer cool just a bit between etches.	You can time the etch with a dummy wafer. Bulk area might be etched fine after 40 min, but in-between electrodes still have metal requiring 10 min extra.
26.2 Inspection	Optical microscope	Inspect that the top electrodes are separated	Do not dismount from IBE chuck while inspecting
26.3 Inspection	Camera		Name: 00X_TH1XX_Process_XX
27 Etch – Separate top electrodes			**All bonded wafers**
27.1Crystal bond	Hotplate: 90-110°C	Dummy wafer is bonded to glass-side of device wafer. **Recipe:** Standby, Pins down	After cooling, check that wafer stack is bonded.
27.2Plate etch	ASE	Dry etching through Poly Si. **Time:** 5-6 cycles, **Recipe:** shallolr **Temp:** 20C	Stop on oxynitride, make sure not to over etch.
27.3 Inspection	Optical microscope	Inspect that the top electrodes are separated down to the underlying nitride layer/glass	
27.4Crystal de-bond	Hotplate: 90-110°C	Bonded stack separated on hotplate and cleaned with wet tissue paper and water gun. **Recipe:** Standby, Pins down	Careful not to too much water of the front-side. Remaining wax is removed in plasma asher 1

27.5 Inspection	Camera		Name: 00X_TH1XX_Process_XX
27.6Resist strip	Plasma asher 1	Photoresist stripping **Pressure:** 0.8-1.0mbar. **Gas:** 400 O2 and 70 N2. **Power:** 1000watts. **Time:** 30-45 min	
27.7Inspection	Optical microscope	Final inspection (particles and short-circuits) before taking wafers out of cleanroom	
27.8Inspection	Camera		Name: 00X_TH1XX_Process_XX

A.2 Quartz Fusion Process Flow

Step	Equipment	Recipe	Comments
Silicide creation			
1	Silicide process	Silicide process	Silicide process.
Clean			
2.0	RCA Bench	Full RCA clean	-
Poly-silicon deposition			
2.1	LPCVD Poly-Si (4") (B4)	POLYBOR	2 µm or a thicker layer.
Polishing			
3.0	Polisher/CMP	IHM_SOI_CMUT	See PSOI fabrication process to see all process details regarding clean after CMP.
Clean			
3.1	Piranha	-	10 minutes. First Sulfuric acid (H_2SO_4) and then hydrogen peroxide (H_2O_2) in the ratio 4:1. We have our own beaker for this on our shelf called Piranha 1.
3.2	Oxide etch 2: BHF (clean w. wetting agent)	-	5 minutes.
3.3	Piranha	-	10 minutes. First Sulfuric acid (H_2SO_4) and then hydrogen peroxide (H_2O_2) in the ratio 3:1. We have our own beaker for this on our shelf called Piranha 2.
Clean			
4.0	RCA Bench	Full RCA clean	-
Thin film			
4.1	Furnace: Anneal-oxide (C1)	DRY980 or WET980	400 nm. This layer will later be the insulation oxide. Remember oxidation rate will most likely differ from crystalline silicon. The resistivity of the silicide degrade if the temperatures rises above roughly 980 C°. A wet oxide might be necessary for this step.
4.2	Furnace: LPCVD Nitride (4") (B2)	nitride4	14 minute deposition yielding a thickness of approximately 55 nm.

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Table A.1 – continued from previous page

Step	Equipment	Recipe	Comments
4.3	LPCVD Poly-Si (4") (B4)	POLY620	11 minute deposition resulting in a thickness of approximately 100 nm.
Lithography			
5	Spin Coater: Gamma UV	2421 DCH 100mm nLOF 2020 2um HDMS	-
6	Aligner: Maskless 02 (MLA2) or Aligner: MA6 - 2	-	**Cavity mask.** Aligner: Maskless 02 (MLA2) dose 400 or Aligner: MA6 - 2 10.2 sec exposure with an intensity of 11 mW/cm^2
7	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	-
8.0	Developer: TMAH UV-lithography	2001-DCH PEB 110C 60s	Bake step prior to the wet poly etch.
Etch			
8.1	Poly Si etch	-	Etch until pattern is fully developed and the poly on the backside is removed as well. Etch rate depends heavily on when the BHF was added to the solution, so check that on Labmanager before etching.
9	Plasma Asher 2	Manual	45 minutes. O_2 flow 400 ml/min and N_2 flow 70 ml/min.
10	Nitride etch: H3PO4	-	Approximately 45 minutes at 160°. Etch rate $\approx$ 2.6 nm/min.
Clean			
11	Piranha	-	10 min (wafer cleaner can also be used).
Lithography			
12	Spin Coater: Gamma UV	1411 - DCH 100mm MiR 701 1.5um HMDS	-

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Table A.1 – continued from previous page

Step	Equipment	Recipe	Comments
13	Aligner: Maskless 03 (MLA3) or Aligner: MA6 - 2	-	**Bottom electrode.** Aligner: Maskless 03 (MLA3) dose 320 or Aligner: MA6 - 2 15.5 sec exposure with an intensity of 11 mW/cm^2
14	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	-
Etch - Bottom electrode			
15	ASE	1shalolr	Etch through poly silicon and the silicide layers, and stop on the quartz substrate. Etch rate in silicon/poly-silicon is approximately 600 nm per bosch cycle.
Clean			
16.0	RCA Bench	Full RCA clean	-
LOCOS oxidation			
16.1	Furnace: Anneal-oxide (C1)	WET980	The LOCOS post oxide thickness is determined by the design. Use the Furnace MatLab script for accurate and precise calculations of the resulting thickness. Remember oxidation rate will most likely differ from crystalline silicon. The resistivity of the silicide degrade if the temperatures rises above roughly 980 C°. A wet oxide might be necessary for this step.
Pre bond clean			

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Table A.1 – continued from previous page

Step	Equipment	Recipe	Comments
17.0	RCA Bench	Only RCA1[1]	Remember to clean a POly On Quartz (POOQ) wafer in this step as well. It is a good idea to position the wafers in bonding pairs, meaning the bond interfaces face towards each other. A pre bonding can then be performed under the RCA HEPA filter using a vacuum tweezer, to obtain to smallest possible particle contamination.
Fusion bonding			
17.1	Wafer Bonder 02	CMUT fusion bonding standard	To protect the surface from undesired particles and contamination (from the top piston in the wafer bonder) use a dummy silicon wafer on top of the bonded stack. Remember to have the unpolished side towards to the bonded stack.
17.3	Furnace: Anneal-bond (C3)	ANN980	70 minutes.
Lapping - Handle removal			
18	Polisher/Lapper	-	Remove/lap until the the handle (Quartz) wafer is approximately 20 µm.
Clean			
19	Piranha	-	10 min. Clean necessary since the wafer is coming from the Polisher/Lapper.
20	Beaker	-	7-10 min in 40% HF to etch the remaining quartz. It might be possible to remove the entire handle wafer in 40% HF, but, it requires the films on the backside are sufficient to protect the substrate wafer.
Post KOH clean			

Continued on next page

Table A.1 – continued from previous page

Step	Equipment	Recipe	Comments
Lithography			
14	Spin Coater: Gamma UV	1411 - DCH 100mm MiR 701 1.5um HMDS	-
15	Aligner: Maskless 03 (MLA3) or Aligner: MA6 - 2	-	**Access to bottom electrode mask.** Aligner: Maskless 03 (MLA3) dose 320 or Aligner: MA6 - 2 15.5 sec exposure with an intensity of 11 mW/cm^2
16	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	-
Etch - opening to bottom electrode			
17	ASE	1shalolr	Etch through device layer. Etch rate in silicon/poly-silicon is approximately 600 nm per bosch cycle.
18	AOE	SiO2_res	Etch through post oxide layer. Etch rate is approximately 200 nm/min.
Metal deposition			
19	E-Beam Evaporator (Temescal)	Al	400 nm.
Lithography			
20	Spin Coater: Gamma UV	1411 - DCH 100mm MiR 701 1.5um HMDS	-
21	Aligner: Maskless 03 (MLA3) or Aligner: MA6 - 2	-	**Top electrode mask.** Aligner: Maskless 03 (MLA3) dose 320 or Aligner: MA6 - 2 15.5 sec exposure with an intensity of 11 mW/cm^2. Notice the design has (typically) to be inveted when MLA3 is used, remember then to extend the boarders to ensure exposure over the entire wafer.
22	Developer: TMAH UV-lithography	3001 DCH 100mm PEB60s@110C SP60s	-

Continued on next page

Table A.1 – continued from previous page

Step	Equipment	Recipe	Comments
23.0	Developer: TMAH UV-lithography	2001-DCH PEB 110C 60s	Bake step prior to the wet Al etch.
Etch - top electrode definition			
23.1	PES Al etch[2]	-	Remember inspection of the elements in a microscope after the etch, and make sure the aluminium is completely etched between the elements. ICP metal etch could also be used to etch the metal.
24	ASE	1shalolr	Etch through device layer. Etch rate in silicon/poly-silicon is approximately 600 nm per bosch cycle.
25	Plasma Asher 1	Manual	45 minutes. O_2 flow 400 ml/min and N_2 flow 70 ml/min.

Appendix B

Process optimization

B.1 Anodic bonding lecture note

Anodic Bonding

Advanced methods in micro- and nanofabrication

By Rune Sixten Grass and Kitty Steenberg

DTU Health Technology

This document will briefly cover the topic of anodic bonding and explain some of the mechanisms involved in the bonding process, as well as how to improve bond quality.

Most of the information can be found in the book "Bonding in Microsystems Technology" by J. A. Dziuban.

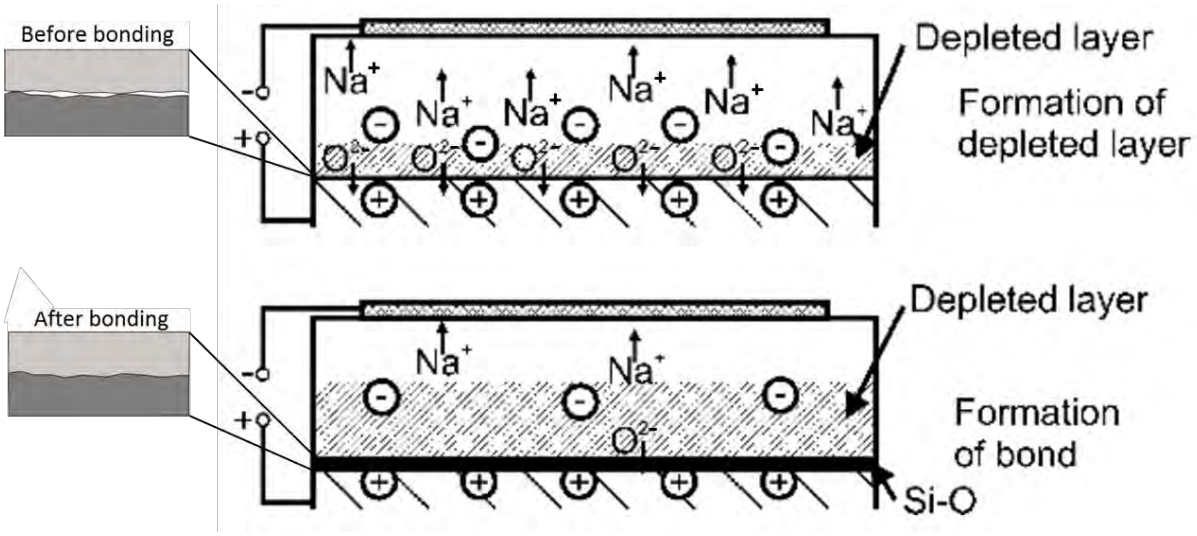
Contents

Methods – How it works

Anodic bonding is generally the bonding of a glass wafer to a silicon wafer, by means of elevated temperature, which allows the applied bias to drive a current and set up an electrostatic force pulling the two wafers intimately in contact.

First the two wafers are put together and Newton's rings with interferential colours will start to appear at the interface. The wafer stack is now placed on the bottom electrode, the anode, with the

silicon wafer facing down and the glass wafer facing up. The wafer stack is then heated up to a bonding temperature usually between 300-500° C, decreasing the glass resistivity and increasing the mobility of the ions inherent in the glass. A bias is applied accordingly, see the figure below, which will make the Na^+ ions drift towards the cathode leaving behind a negatively charged area near the bonding interface. This depletion layer sets up an electrostatic force pulling the two opposite charged wafers close together, this intimate contact is what facilitates the bond formation.



Bonding Mechanisms

Chemical bond formation

There is no overall agreement on how the bonds are created in anodic bonding, however two models are quite popular. One is where the oxidants are inherent in the glass wafer, where O^{2-} and OH^- oxidize Silicon at the interface through this reaction

$$Si\ (s) + O_2\ (g) \rightarrow SiO_2\ (s)$$

creating strong siloxane bonds. The other model is the water-pump model, where molecular water is trap between the glass and the silicon wafer and is decomposed and the hydroxide reacts with the silicon through a local oxidation process

$$Si\ (s) + 2H_2O\ (g) \rightarrow SiO_2\ (s) + 2H_2\ (g)$$

$$Si\ (s) + 2OH^-\ (g) \rightarrow SiO_2\ (s) + 2H^+\ (g) + 2e.$$

The excess hydrogen ions will flow towards the cathode together with the sodium ions and the excess electrons will drift towards the anode, this is what is detected as ionic currents during the bonding process.

Electrostatic pulling force

When a polarization voltage is applied to the wafer stack during bonding a capacitor is set up. The electrodes are made up of the bottom silicon wafer (anode) and the metal cathode on top of the glass wafer. Due to the higher conductivity (compared to the glass) of silicon, the bottom wafer is assumed to have the same potential as the anode. The flat capacitor can be expressed by

$$C = \frac{\varepsilon_0 \varepsilon_r}{d} \cdot S$$

ε_0 and ε_r being the vacuum- and relative permittivity, S the surface area of the wafers and d the distance between the electrodes (here initially being the thickness of the glass wafer). The electrostatic force pressing/pulling the wafers together is given by

$$F = -\frac{1}{2}U^2\frac{C}{d}$$

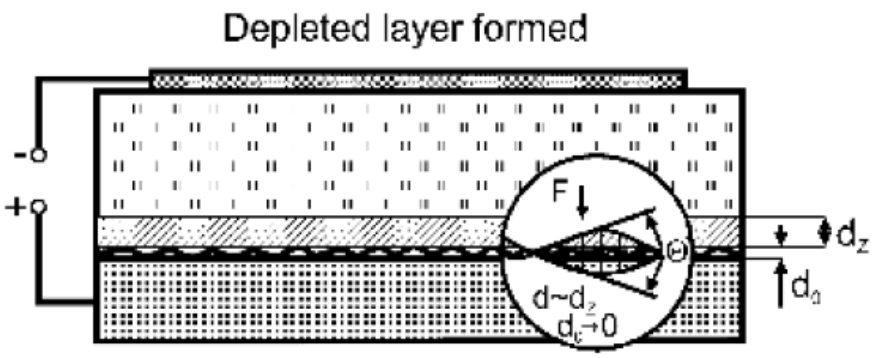
and the electrostatic pressure is given as

$$P = -\frac{F}{S}$$

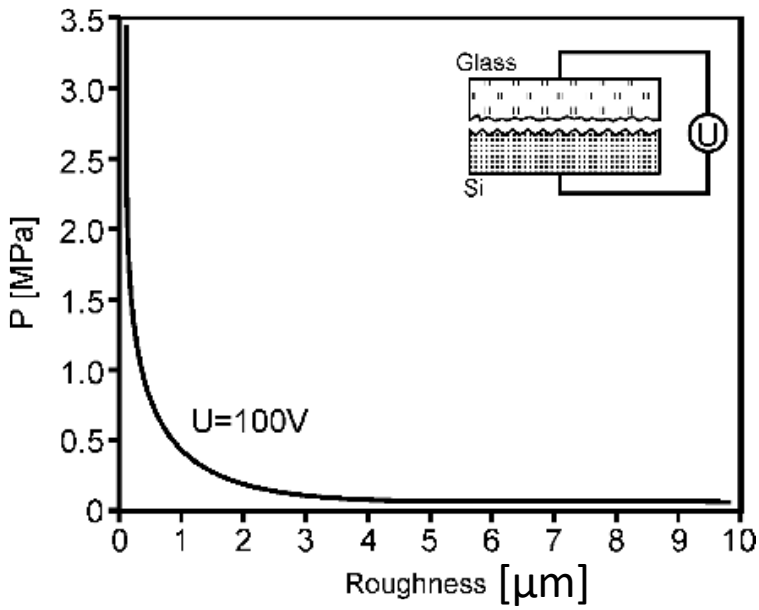
which when inserting the force gives the pressure as function of the electric field intensity

$$P = -\frac{1}{2}\frac{\varepsilon_0\varepsilon_r}{d^2}\cdot U^2$$

$$P = -\frac{1}{2}\varepsilon\cdot E_p^2$$



When the depletion layer is formed the voltage drop mainly occurs in the air gap between the wafers (<0.5 µm), due to the unevenness or surface roughness, seen in the above figure. This increase in force and surface contact facilitates the formation of bonds. As the gap closes the voltage



drop primarily occurs over the depletion layer and the force increases dramatically, as seen in the figure below

Due to the high pulling force, small dust particles trapped at the interface or waviness/unevenness of the silicon surface can be more easily be tolerated compared to e.g. fusion bonding. Because of the viscous properties of the glass wafer, it will flow slightly and conform to the silicon wafer surface when the stack is heated during bonding. The glass also undergoes elastic deformation during the bond and the polarisation voltage, U, needed for complete wafer contact can be described by the following equation

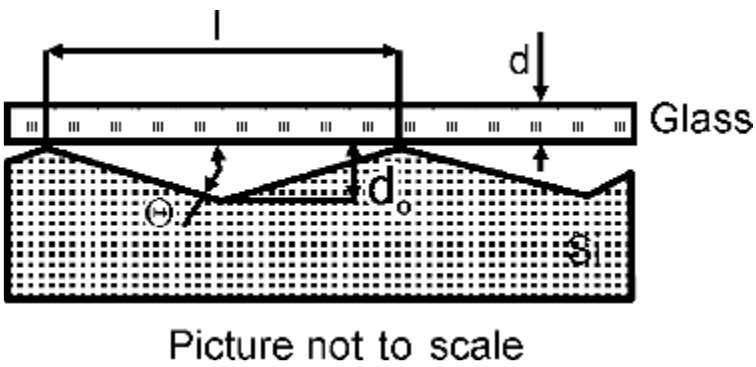
$$U \geq \sqrt{\frac{h\nu d^3}{80E \cdot l^4}}$$

h being the height of waviness, ν being Poisson's ratio, *l* the length of waviness, E Young's modulus and d the thickness of the glass plate, see figure below.

Because of the glass viscosity and equation for the bond time needed to absorb particles, τ_N , on the wafer surface at the interface can be given as

$$\tau_N = \frac{3\eta H^2 P \pi l^2}{E\ U^2}$$

Where η is the viscosity at bonding temperature, P is the dust particle surface density, H the is particle diameter.



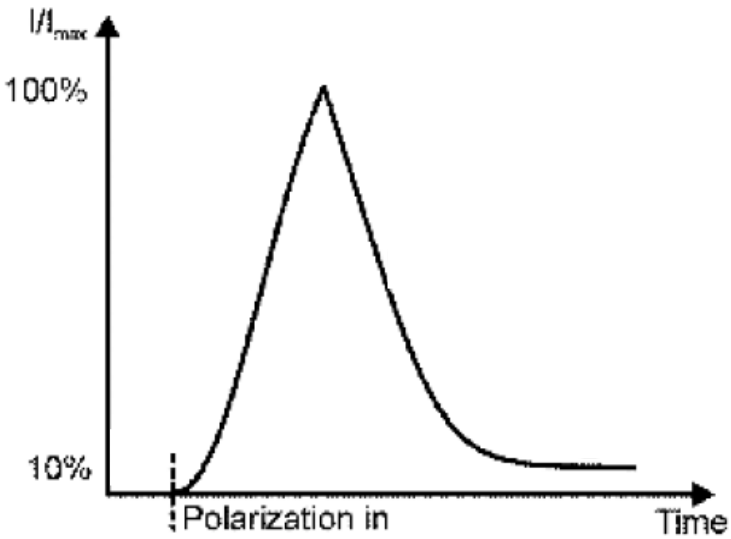
Successful bonds – Adjustable parameters

Current/Voltage characteristics

Good bonds are defined by having a fast, almost immediate maximum current peak followed by a rapid drop down to approximately 10% of the max current, see figure below. The max current is often limited by the equipment as an example the wafer bonder 02 inside the DTU Nanolab cleanroom has a max of 13 mA. Having a high amount of accumulated charge commonly indicates a good bond.

Ionic currents

During bonding the currents in the wafer stack and in the glass wafer will on factors such as the glass composition, the temperature, polarization voltage and cathode shape. As previously mentioned there will be a flow of sodium ion and hydroxide ions and other components from the glass wafer. The sodium will flow to the cathode and neutralize, forming Na_2O or NaOH precipitated as salt at the



interface by reacting with oxygen or water molecules taken from the surface or the cathode material.

If the cathode used is a so-called tip cathode (stainless steel rod with a diameter of 2-3 mm to 1 cm), all the ionic currents will be concentrated at a single point on the glass surface. The electrical field can become so high that breakdown of the glass or decomposition can occur, increasing the sodium current and thereby the precipitation of salt. This will render the glass surface at that point unusable and corrode the cathode, depending on its material. As this surface will likely be the wafer backside, it might not matter for certain applications. The breakdown might however damage sensitive devices.

If a flat cathode fully in contact with the glass is used instead the field will be uniform. However due to micro roughness on the cathode surface the field will be slightly disturbed and the local ionic current can increase. This can further degrade the cathode and increase local current spikes and breakdown of the glass wafer. It is therefore important to use a uniform cathode for protecting the glass backside and the cathode itself.

We recommend that a low resistivity (high-doped) silicon wafer is used as an intermediate dummy wafer between the glass wafer and the cathode. Due to the low surface roughness of the wafer, the field will be uniform, allowing for higher polarization voltages to be used without breakdown of the glass wafer. Unwanted precipitated salt will likely also mainly form on the wafer and not the cathode itself.

Choosing the right materials – how to avoid thermal strain

Heating up and bonding two materials together, they will expand corresponding to their thermal expansion coefficient, if the two material's expansion coefficients do not align within a certain degree it will cause thermal strain in the wafer stack.

This thermal expansion mismatch could lead to wafer bow or even breaking of the wafers, hence bonding materials should have similar thermal expansion coefficients. Figure 2.3 shows the thermal expansion coefficient for Silicon and Pyrex 7740 (glass) vs temperature, by choosing a bonding temperature, here 275° C, so that the shaded areas are equal in size there won't be induced thermal strain in the wafer stack, hence no stress after cooling. [1]

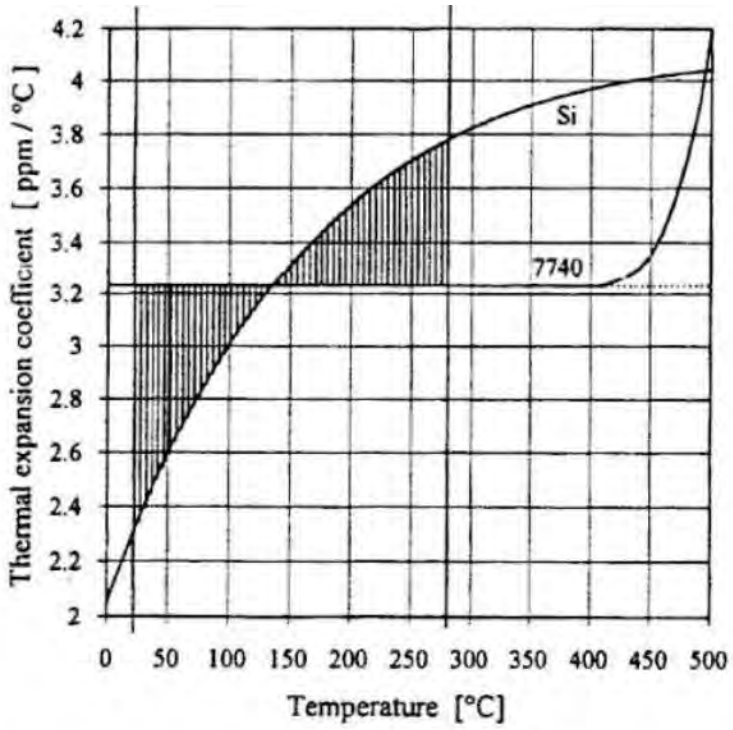


Figure 2.3: Thermal expansion coefficient of Silicon and Pyrex across a temperature from 0-600°C

Prebonding - how to get a good base for a successful

Generally, an RMS surface roughness below 50 nm is required for successful anodic bonding.

Cleaning

In the article by Joyce et. Al. [1] comparing piranha and RCA cleaning on both Si and SiO_2, they found that the RCA clean gave lower surface roughness, a higher bonding current and with a shorter time for the current to half in value, indicating that silicon wafers should be RCA cleaned prior to bonding. This agrees with the observations we have made ourselves regarding particle contamination which will be elaborated in the next section. Glass wafers are not allowed in the RCA clean, therefore they have to be piranha cleaned and possibly go through a HF dip to remove particles.

Pre-treatment

Besides RCA cleaning the wafers, it might also improve the bonding quality if the wafers are pre-treated before bonding. One such example of bonding silicon wafers with a nitride layer to a glass wafer is presented by Weichel et al. [2]. They present that treating the silicon nitride surface with either an oxygen plasma or oxidising the surface, will activate the wafer surface and likely lower the activation barrier for bond formation and thereby improving the bond strength.

They saw a significant increase in yield and bonding strength using different types of surface treatment.

Three different methods were

- Oxygen plasma treatment in RIE
- Plasma ashing with an oxygen plasma
- Wet oxidisation in a furnace at 1000°C

Similar surface activation methods might in general improve bonding quality, depending on the intermediate layers used and wafer stack material.

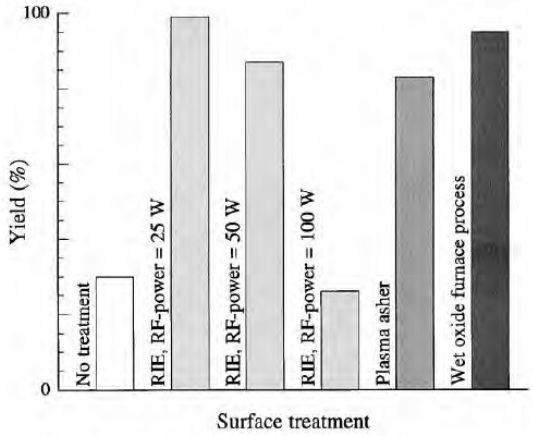


Fig. 1. Yield for thin-film anodic bonding using various surface treatments of the silicon nitride coating.

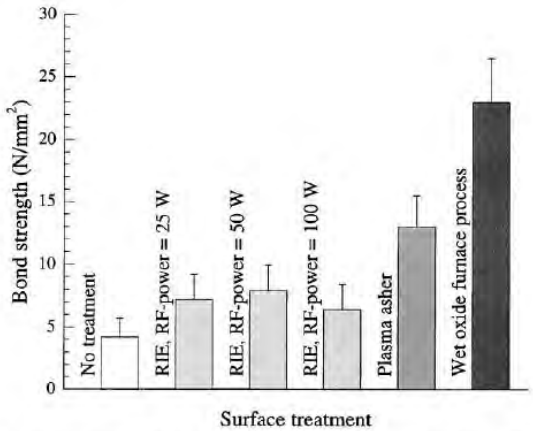


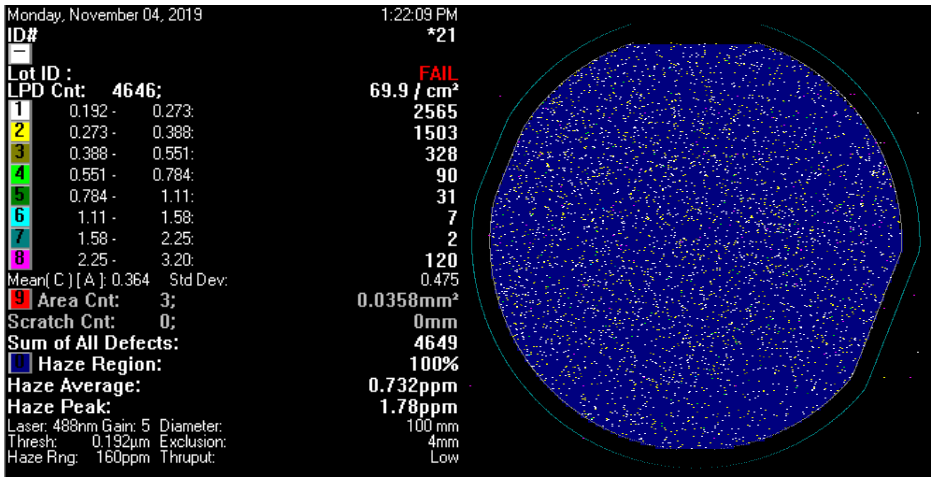
Fig. 2. Bond strength for thin-film anodic bonding using various surface treatments of the silicon nitride coating.

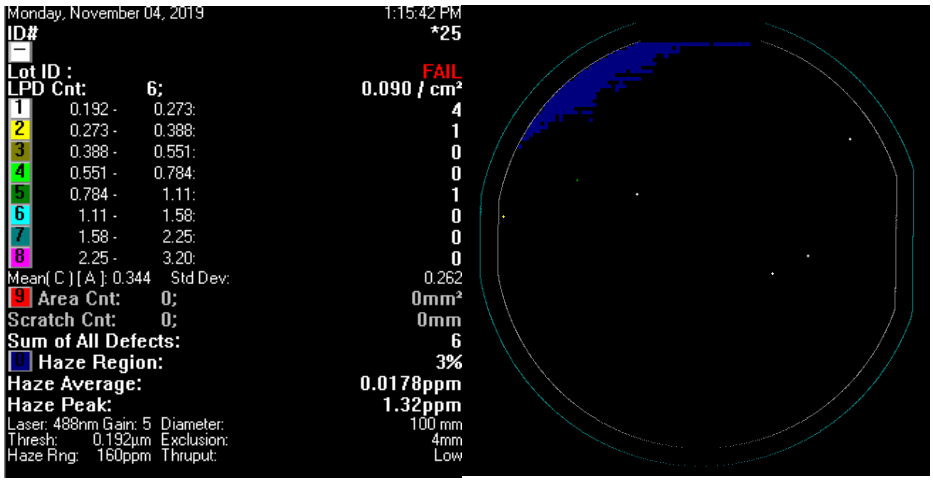
Particle measurements

During bonding, particles of various sizes can get trapped in the interface of the two bonding wafers, even if these are cleaned beforehand. As mentioned earlier it is possible to bond over and absorb particles depending on their size and amount. It is however always preferable to clean wafers with RCA or a piranha solution, to remove as many particles as possible.

A high particle count of small and large particles may render the wafer stack un-bondable. They simple will not stick during either pre-bonding, where the Newton's rings form upon initial contact, or they might come apart after the bonding process. If the bonding is successful, air pockets or voids can form in the bonding interface with particles at their centre.

There are different methods for measuring particles on a wafer surface, some of these being an AFM to measure particle size and density over a small area, an optical microscope in darkfield mode or a dedicated particle counter. An example of two scans from a particle counter is seen in the two figures below, where the distribution of particles across the wafer and their sizes are listed (e.g. 2565 particles of size 0.192 to 0.273 µm). The first figure is a measurement of an uncleaned silicon wafer and the second is from an RCA cleaned silicon wafer.





Depending on the design placement on the wafer surface, the wafer depicted in first figure could result in a successful bond. This will depend on whether voids will form and how sensitive the design is.

In general, it is good practice to have bondable areas that are not smaller than a few micrometres wide. Designs should also not be placed too close to the handling edge of the wafer (approximately 0.5 to 1.0 cm).

Comparison to other bonding techniques

Here a very brief overview of some other types of bonding techniques is presented and the advantages of anodic bonding is summed up compared to fusion bonding.

Beside the presented method of anodic bonding other types of bonding techniques can be used depending on the application.

Eutectic bonding, where silicon wafers are bonding together with an intermediate metal layer forming a eutectic interface at relatively low temperatures. This can result in good hermetically sealed bonds with low stress, showing high bonding strength and high yield.

Adhesive bonding involves bonding a polymer layer to silicon through a low temperature process. The polymers often used are benzocyclobutene (BCB) or SU-8 and can e.g. serve as membranes or cavity lids. Using a photosensitive polymer is advantageous as cavities as structures are directly formed with standard lithography processes. These however often have low breakdown voltages.

Fusion bonding (FB) or direct bonding is a common bonding technique where clean, flat, and smooth silicon wafer surfaces are first bonded together at room temperature by weak surface forces. The process is often assisted by a pressing force. The process tolerates only very little surface roughness and few particles. As with anodic bonding, cleaning and chemically activating the surfaces beforehand can improve bonding. The wafer stack is then annealed at higher temperatures to form permanent strong bonds. Intermediate oxide layers can be used in the silicon to silicon bonding stack, often serving as structural patterns forming cavities or trenches. An example is the LOCOS process used to form oxide cavities.

Compared to fusion bonding the anodic bonding (AB) process can tolerate a higher surface roughness (< 50 nm compared to < 1 nm for fusion bonding) and is less sensitive to particles. Anodic bonding is also a faster process, with usually around 30-40 min per wafer depending on voltage ramps, whereas for fusion bonding annealing often takes 6-11 hours. Annealing however can be done in batches. AB is also advantageous due to it being a low temperature process where metals and sensitive materials can be used. Bonding energy and tensile strength achieved during AB is often higher than for FB due to the high field applied during bonding.

The limitations of using AB as explained previously is often that glass substrates are necessary for the process. This can lead to thermal mismatch. Borofloat glass is also restricted for use due to cross-contamination in some cleanroom equipment. Since it has a very low conductivity compared to silicon it also has difficulties clamping in etching equipment.

Alternative materials used with anodic bonding

Anodic bonding is not limited to only glass and silicon although these are the key components in the stack. Different intermediate layer such as thin-film dielectrics, metals, and metal oxides can also be used. We will not go into details with the possibilities but just list a few example materials below

- Bonding of silicon substrates to borosilicate glass through thin intermediate layers:
    - SiO_2, SiO_x – thin layers of oxide on the silicon substrate
    - SiO_2/Si, SiO_2/SiC layers – double layers of oxide and silicon grown on silicon
    - Al or Al_xO_y layers – aluminium or aluminium oxides
    - Ti, Ta – titanium or tantalum intermediate metal layers
    - Si_3N_4 layer – insulating silicon nitride or silicon oxynitride layers (improved bond)
    - Silicon to silicon bonding through thin glass layers
- Glass–FeNiCo alloy – For creating vacuum seals by bonding of glass to Kovar alloy which has a similar expansion coefficient as glass

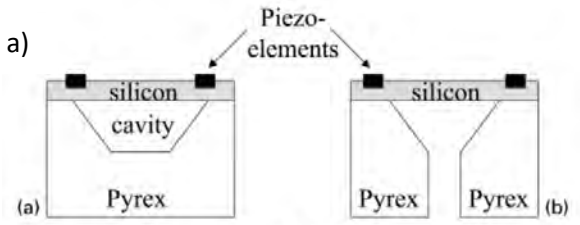
Applications

The applications using anodic bonding has been increasing over the years and many technologies already present make use of the technique.

In the field of sensors and actuators it is used for micromachined capacitive accelerometers, positioning sensing, infrared vibrometry sensing and various microphones and pressure sensors. In these examples a cavity with either ventilation holes in the glass or a vacuum chamber is created from the bonded glass wafers. Such a pressure sensor and microphone can be seen in a) and b) respectively in the figure below.

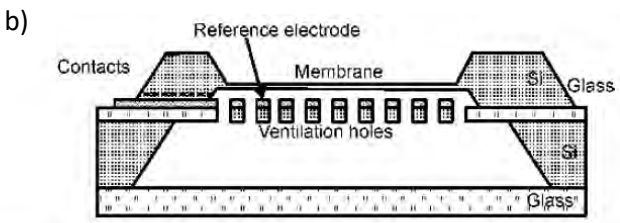
Microfluidic channels also see the use of anodically bonded structures. Channels are formed by either etching trenches in silicon or glass and subsequently bonding of the two wafers. In- and outlets can be made and combined with actuactors for micropumps and valves. A benefit of the see-through glass wafer is also the possiblity of measuring particles or studying the fluid in microscopes. A microfluidic channel device is shown in c) in the figure below.

Anodic bonding also has a use in packaging where e.g. mems devices or small dies need encapsulation and a vacuum sealed environment.

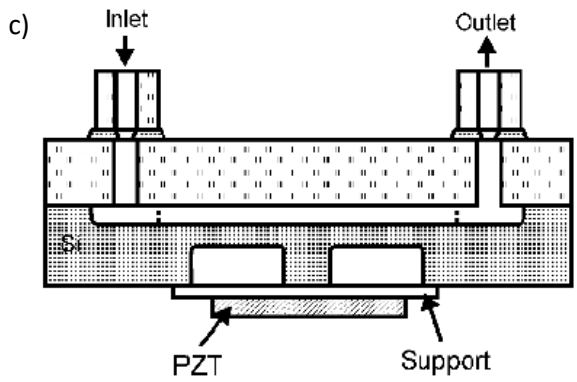


a absolute pressure sensor; *b* gauge pressure sensor

2 Schematic picture of silicon–Pyrex pressure sensors



Silicon-glass microphone.



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[2] Joyce, Robin, et al. "Effective cleaning process and its influence on surface roughness in anodic bonding for semiconductor device packaging." *Materials Science in Semiconductor Processing* 31 (2015): 84-93.

[3] Weichel, Steen, et al. "Low-temperature anodic bonding to silicon nitride." *Sensors and Actuators A: Physical* 82.1-3 (2000): 249-253.

Dziuban, Jan A. *Bonding in microsystem technology*. Vol. 24. Springer Science & Business Media, 2007.

Fractal testing on Al and Ti + Al

Wafer	Name	Anodic bonding	Fractals
Glass wafer with Ti 10 nm + Al 280 nm	WAFR_20210105_02	Heating to 350C for 30 min	No fractals
Glass wafer with cavities with Al 290 nm	TR2_20200302_08	Heating to 350C for 30 min	No fractals
Si + Ti 10 nm + Al 280 nm on glass	WAFR_20210105_01	Heating to 350C for 30 min → Inspection → CMUT/anodic bond 4 inch 250-600V 350C no center pin	Holes/seed formation beginning of fractal, despite titanium diffusion layer
Si + Glass wafer with cavities with 290 nm Al	TR2_20200302_07	CMUT/anodic bond 4 inch 250-600V 350C no center pin	Holes/seed formation beginning of fractal → field assisted In agreement with my own tests
Si + Glass wafer with cavities with 30 nm Ti + 250 nm Al	TH1_20210107_01	CMUT/anodic bond 4 inch 250-600V 350C no center pin	Major void over 2 of RC 190, **no fractals** Resist strip, no TMAH
Si + Glass wafer with cavities with 30 nm Ti + 250 nm Al	TH1_20210107_02	CMUT/anodic bond 4 inch 250-600V 350C no center pin	Accidentally bonded wrong side
Si + Glass wafer with cavities with 30 nm Ti + 250 nm Al	TH1_20210107_03	CMUT/anodic bond 4 inch 250-600V 350C no center pin → with wafer	Voids , **no fractals** but ribbon formation from IBE, pattern shifted during bonding Plasma asher + TMAH
Si + Glass wafer with cavities with 290 nm Al	TR2_20200302_06	CMUT/anodic bond 4 inch 250-600V 350C no center pin → with wafer	Holes/seed formation beginning of fractal Plasma asher + TMAH
Si + Glass wafer with cavities with 30 nm Ti + 250 nm Al	TH1_20210107_04	CMUT/anodic bond 4 inch 600V 375C_with_wafer	**No fractals** but ribbon formation from IBE, pattern shifted during bonding Plasma asher + TMAH

Figure B.1

B.2 Fractal test supplementary material

Color coding: Ok Test No-go

Glass substrate – bottom substrate

Metal bottom electrode Thick layer Adhesion layer	Bottom electrode lithography definition (MLA)	Bottom electrode definition	Cleaning method (prebonding)	Bondable (Ok or need test)	Plasma Asher cleaning	ASE Tolerable
Cr	Negative resist	Cr etch 18	Piranha	Test (higher temp)	Etched (Leave resist on)	Ok
Cr/Au (200nm/15nm)	Negative resist	Cr etch 18 / Au etch diluted	Piranha	Ok	Test – low power	Ok
Cr/Au (15nm/200nm)	Negative resist	Au etch/Cr etch 18 Test diluted	Piranha	Ok – do test at 375C	Test – low power	Ok
Al	Negative resist	Alu wet etch, PES	Plasma+TMAH or Resist strip	Fractals	Ok	Ok
Cr/Au (15nm/200nm)	Negative resist	IBE	Piranha	Ok	Test – low power	OK
Cr	Negative resist	IBE	Piranha	Ok	Etched (Leave resist on)	Ok

For pure Cr leave resist on for protection

Figure B.2

B.3 Metals, etching techniques and process compatibility

Appendix C

Paper A - Anatomic and Functional Imaging using Row-Column Arrays

Anatomic and Functional Imaging Using Row–Column Arrays

Jørgen Arendt Jensen, *Fellow, IEEE*, Mikkel Schou, Lasse Thurmann Jørgensen, Borislav G. Tomov, Matthias Bo Stuart, Marie Sand Traberg, *Member, IEEE*, Iman Taghavi, *Member, IEEE*, Sigrid Huesebø Øygaard, Martin Lind Ommen, Kitty Steenberg, Erik Vilain Thomsen, *Member, IEEE*, Nathalie Sarup Panduro, Michael Bachmann Nielsen, and Charlotte Mehlin Sørensen

***Abstract*— Row–column (RC) arrays have the potential to yield full 3-D ultrasound imaging with a greatly reduced number of elements compared to fully populated arrays. They, however, have several challenges due to their special geometry. This review article summarizes the current literature for RC imaging and demonstrates that full anatomic and functional imaging can attain a high quality using synthetic aperture (SA) sequences and modified delay-and-sum beamforming. Resolution can approach the diffraction limit with an isotropic resolution of half a wavelength with low sidelobe levels, and the field of view can be expanded by using convex or lensed RC probes. GPU beamforming allows for three orthogonal planes to be beamformed at 30 Hz, providing near real-time imaging ideal for positioning the probe and improving the operator's workflow. Functional imaging is also attainable using transverse oscillation and dedicated SA sequence for tensor velocity imaging for revealing the full 3-D velocity vector as a function of spatial position and time for both blood velocity and tissue motion estimation. Using RC arrays with commercial contrast agents can reveal super-resolution imaging (SRI) with isotropic resolution below 20 μm. RC arrays can, thus, yield full 3-D imaging at high resolution, contrast, and volumetric rates for both anatomic and functional imaging with the same number of receive channels as current commercial 1-D arrays.**

***Index Terms*— Beam forming, row-column (RC) arrays, super resolution, ultrasound, velocity measurement.**

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This work involved animals in its research. Approval of all ethical and experimental procedures and protocols was granted by the Danish Animal Experiments Inspectorate under the Ministry of Environment and Food under Application No. 2020-15-0201-00547.

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I. Introduction

CURRENTLY, 2-D ultrasound imaging is mostly conducted using 1-D array transducers with 192–256 elements, which are employed to dynamically focus on the image. Digital beamformers are used, where the signal from each transducer element is sampled at 4–8 times the center frequency for sampling rates between 12 and 60 MHz. A fully populated 15-MHz array with 256 channels will, thus, give data rates up to 30.7 GB/s, which are beamformed in real time. Currently, most arrays have a fixed geometric focus in the elevation plane (orthogonal to the imaging plane), and the focusing is often poor in this direction, underlining the necessity for 3-D focusing and imaging.

Attaining 3-D ultrasound images requires electronic steering in both the azimuth and elevation directions to allow dynamic focusing along all three directions (axial, azimuth, and elevation). Matrix arrays were early conceived as they allow full control in both directions in both transmit and receive. However, it creates another practical problem as the number of channels increased quadratically with the side length of the array assuming a square array aperture. A straightforward translation to 3-D would give arrays with $192 \times 192 = 36\,864$ elements or $256 \times 256 = 65\,536$ elements yielding data rates of 2560 GB/s, which is clearly not possible to process in real time. This has been solved by making sparse matrix probes, where only part of the elements are connected resulting in higher sidelobe levels [1]–[6]. A second approach is to make micro-beamforming in the handle to reduce the amount of data. Philips has introduced the fully sampled matrix phased array x-matrix probe shown in Fig. 1 with 9212 elements, which potentially could have 96×96 elements. Such a probe can be steered in both directions, and this necessitates an element size of half a wavelength λ given by

$$\lambda = c/f_0 \tag{1}$$

where c is the speed of sound (1540 m/s in tissue) and f_0 is the transducer center frequency. In this case for a 3-MHz probe, the element size is 250 μm and the side length of the probe is $48\lambda = 24$ mm. Much of the beamforming is performed in the transducer handle to reduce the amount of data coming out of

Fig. 1. Fully populated matrix array from Philips with beamforming in the handle. The probe has 9, 212 active elements, but note that the plug can only handle 256 simultaneous connections.

the probe to probably 256 channels, making this an extremely complex and expensive probe to develop and manufacture.

The focusing ability of ultrasound probes is related to their size and imaging depth. The full-width at half-maximum (FWHM) of the point spread function (PSF) is

$$\mathrm{FWHM} = \lambda F\# = \lambda \frac{D}{W} \tag{2}$$

where D is the imaging depth, W is the aperture width, and $F\#$ is the F-number, in which its lowest theoretical value is 1/2 (the diffraction limit). The best possible attainable lateral resolution is, thus, $\lambda/2$. For the Philips probe, this can only be attained down to 12 mm, and after 48 mm, the resolution goes beyond 2λ, which is considered as the resolution limit for an acceptable ultrasound image. In cardiology, a lower resolution has to be accepted due to the narrow space between the ribs, which prevents the use of larger probes when scanning the heart. In other applications with a wider acoustic window, such resolution is not acceptable.

In other clinical specialties, the matrix probe should be larger, further increasing the amount of elements and the complexity of the probes. In general, the lateral resolution in the two planes scales with the side length of the probe, and increasing the resolution by two will quadruple the number of probe elements. Matrix probes are, thus, not an optimal approach for attaining a high image quality, and conventional 1-D array probes have a poor out-of-plane resolution limiting their ability to visualize small objects when they are not at the elevation focus. Other solutions for optimal imaging are therefore needed.

A. History of RC Imaging

A possible solution to these problems is to employ row–column (RC) array probes [7]–[25]. Here, the matrix elements are addressed as either rows or columns, as shown in Fig. 2. The amount of connections to an $N \times N$ elements array is $2N$, reducing the amount of connections by $N/2$, which for a 256 × 256 elements arrays is a factor of 128. Often, only rows or columns are used in transmit and the orthogonal elements in receive, and suitable multiplexing can therefore reduce the scanner connection to N, a further reduction by 2.

It is, thus, possible to have very large RC arrays without the amount of connections to the array getting prohibitively large. The consequence of this is a theoretical focusing capability, which is much better than for a fully populated array, as the

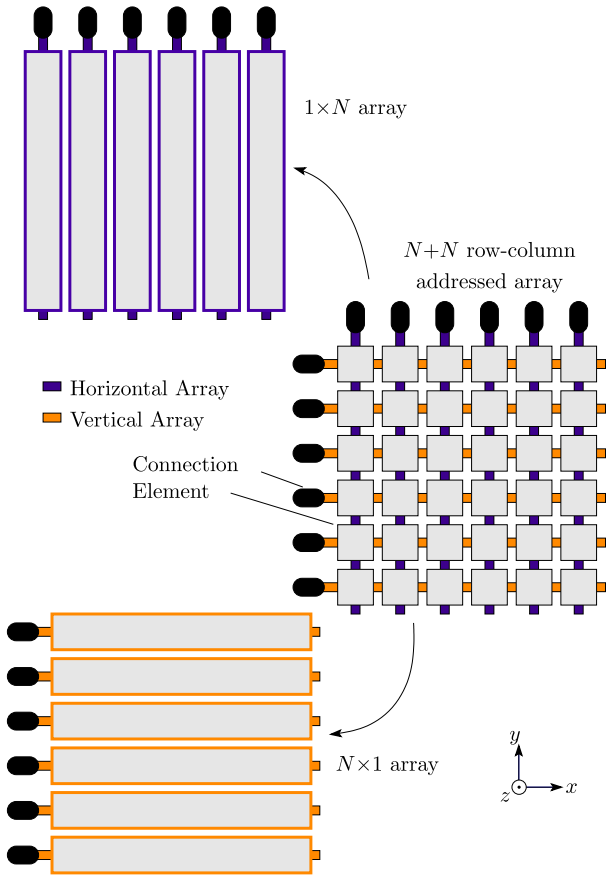

Fig. 2. Row–column-addressed 2-D transducer array can be interpreted as two orthogonal 1-D arrays. A 2-D transducer array is shown in the right, where each transducer element is addressed by its row or column index, effectively creating the two arrays shown to the left (from [24]).

width of the array is larger, and the FWHM is correspondingly smaller.

The area of the array scales quadratically with the side length or element count, which is beneficial for the transmitted pressure and the received energy. RC probes can therefore have an increased penetration depth compared to other probes as demonstrated in [26].

The initial idea of RC arrays was presented by Morton and Lockwood [7] at Queen's University, Kingston, ON, Canada, with simulations of a convex array for revealing the imaging area and PSF. Further simulations were given in [17]. Fabrication of such an array and data from its use was given in [27].

The group by Daher and Yen [9] at the University of Southern California, Los Angeles, CA, USA, has also fabricated a number of arrays and extensively investigated their performance. Initial simulations of a 256 × 256 RC array were presented in [8] with more extensive simulations in [9]. Results from a 64 × 64 PZT array operating at 5.6 MHz were shown in [10] and later for an impressive 256 × 256 PZT array operating at 6.4 MHz with a size of 40 mm × 40 mm [12]. More results from a cyst phantom were presented in [13] and a full overview of the results are given in [16]. A spatial compounding method for RC arrays used on the 256 × 256

PZT array is described in [14]. Examples of a 32×32 elements capacitive micromachined ultrasonic transducer (CMUT) array with a center frequency of 5.45 MHz along with another 32×32 elements array operating at center frequency of 12 MHz were presented in [15] and [18], showing that high-frequency and high-bandwidth RC arrays can be fabricated in the CMUT technology.

A novel approach similar to RC arrays for 3-D imaging was presented by the group at Roma Tre University, Rome, Italy, using the concept of a criss-cross array [11], where a CMUT array with two spatially superimposed linear orthogonal arrays was investigated. This yields $2N$ connections and an imaging example using two emissions to reduce grating lobes was presented. A fabricated CMUT prototype with overlapping arrays was presented in [28] with $120 + 120$ elements, and imaging was conducted using the ULA-OP scanner [29]. Focusing in the orthogonal plane was attained by approximating a Fresnel lens using a varying bias voltage across elements.

Zemp *et al.* [30] at the University of Alberta, Edmonton, AB, Canada, have also developed a series of RC probes often under the name TOBE: top-orthogonal-to-bottom electrode. The feasibility and fabrication of such an array was presented in [30] for a 64×64 elements array fabricated in the CMUT technology with more details in [23]. Its use for photoacoustic imaging was demonstrated in [31] using a laser for excitation and synthetic aperture (SA) imaging for creating the image. Chee and Zemp [32] described an advanced modulation scheme, where a combination of individual elements could be acquired simultaneously for the CMUT TOBE array. Other combinations of this scheme were presented in [33] and [34], and results with sidelobes below 45 dB were attained. Recent results for a 10-MHz 64×64 elements electrostrictive array using the Hadamard encoding in transmit for an increased signal-to-noise ratio and SA focusing were presented in [35] and for 30 MHz in [36], demonstrating the good image quality of these arrays and imaging schemes.

Flesch *et al.* [37] at the Institut Langevin, Paris, France, have also worked extensively with RC arrays, especially for flow estimation and super-resolution imaging (SRI). A plane wave compounding scheme was described and used for power Doppler imaging (detecting the presence of flow). Using that scheme for flow imaging has unfortunately revealed fairly high grating lobes [38]. The approach has also been used for imaging a rat brain in [39] and [40] using a 15-MHz 128×128 PZT array.

Our group in Denmark has worked extensively with RC arrays for the last ten years within anatomic and functional imaging primarily based on SA sequences. We have also fabricated a range of RC probes, including PZT- and CMUT-based devices [41], and developed fabrication schemes for diverging lenses and probes with integrated lenses [42], [43]. The various results and possibilities will be presented in the following. The challenges of using the RC array are detailed in Section II, the possibilities for making anatomic images are shown in Section III, and the blood velocity estimation is presented in Section V. A method for SRI is presented in Section VI, and a discussion of the benefits, challenges, and future potential is presented in Section VII.

II. Challenges for RC Imaging

RC arrays have a number of challenges, which have to be addressed before high-quality imaging, can be performed. As for all ultrasound imaging schemes, data can be acquired in principally two different ways: focused emissions or broad insonation of the region of interest. The first option will, for 3-D imaging, give an unacceptably low volume rate, unless multiple lines are beamformed in receive as in the early approaches to volumetric imaging [44], [45]. The second approach broadly insonates the volume of interest using cylindrical or plane waves, which decouples the frame rate and the number of image lines. Examples of such imaging will be given in Section III.

A second challenge is the large elements. In ordinary imaging, the elements can be considered point sources and delay-and-sum beamforming is employed based on the geometric distance from emissions through the imaging point to the receiving element. For an RC array, the elements are large, and this changes the emitted field and the calculation of delays. The long elements will give rise to an emitted field, which can be considered a plane wave along the length of the element and a circular wave across the element or essentially a cylindrical-shaped wave. This should be taken into consideration when predicting the wavefront's position in focusing on the image, as is done in the beamformers described in [24]. The focusing calculation in the two orthogonal planes is shown in Fig. 3 for the time-of-flight (ToF) calculation. A precise mathematical description of this can be found in [24].

The large-size elements only make it possible to image in the rectangular region below the probe, and the beam cannot be steered outside this region for pulse-echo imaging. How to solve this problem is described in Section IV-B on lensed and convex RC arrays.

A third challenge from the long elements is the edge waves generated at the ends of the element. The long elements will delay these edge waves significantly compared to the main wave, and this leads to ghost echos after the main PSF, as shown in Fig. 4. The top image shows the PSF for a 62×62 elements array, where edge echoes are seen after the main response. This can be avoided by introducing a roll-off apodization at the edge of the elements to taper off their end response and reduce edge artifacts. This has been employed on the bottom figure, where the ghost echoes disappear.

The major benefit of the RC arrays is of course their size, which benefits their focusing ability and penetration depth. This is shown in Fig. 5, where they are compared to both fully populated arrays and sparse Mills cross arrays [46]. The area, corresponding to penetration depth, is always larger for RC arrays and the side length is the same as for the most sparse 2-D array, yielding a comparable FWHM resolution. The RC arrays, thus, attain both a good penetration depth and a narrow focus.

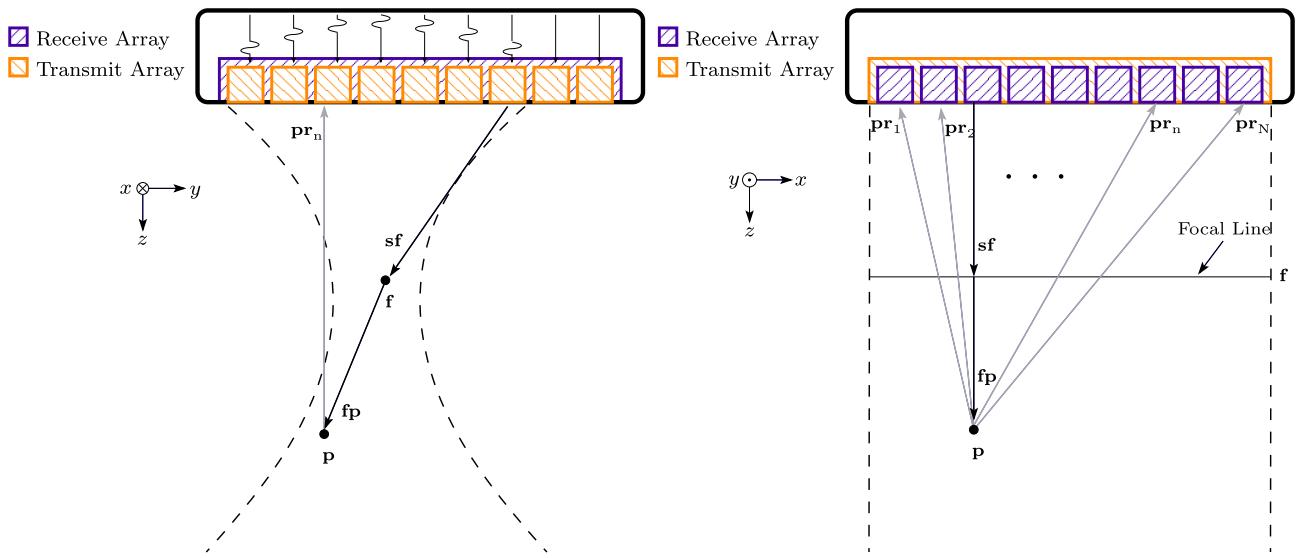

Fig. 3. ToF illustration of a focused emission. The vector **sf** connects the first source line element that is excited with the focal line **f**. **fp** is the vector from the nearest point on the focal line to the point being beamformed (**p**), and $\mathbf{pr}_n$ is the vector from **p** to the nearest point on the receive line element $\mathbf{r}_i$. On the left, the setup is sliced orthogonal to the transmitting line elements and parallel with the receiving line elements. On the right, the setup is sliced parallel with the transmitting line elements and orthogonal to the receiving line elements. The focal zone **f** on the left looks like a focal point, but on the right, it is seen to be a focal line (text and figure from [24]).

RC arrays, however, have several issues to address to attain high-quality imaging, including that the contrast of the images is often slightly lower than for current 2-D scanners. These issues are described in the following, starting with the general principles of SA imaging, which is needed to attain an optimal image quality and a high volume imaging rate.

III. Anatomic Imaging

RC arrays can be used in two fundamentally different ways: using focused emissions or using SA imaging with circular or plane emissions. The first necessitates that the image lines are acquired one at a time, and for a volume with 100×100 lines, this often takes more than a second. The preferred method is therefore to use SA imaging, where dynamic transmit focusing is attained by emitting with a number of broadly insonifying beams and by receiving with the orthogonal array elements for dynamic receive focusing. Emitting with waves that are plane in both directions and tilted along the steerable direction, also called ultrafast imaging, has been studied in [37], [38], and [47], which, however, seems to give fairly high sidelobe and grating lobes.

The second wave type is circular waves, which are plane along the long direction of the transmit element and circular in the orthogonal direction. These virtual sources can have a negative F-number for a diverging wave, or they can be focused on increasing the transmitted pressure. Both focus placements seek to acquire data suitable for creating a synthetic transmit aperture. Synthetic transmit aperture imaging can be used for improving the image quality by having dynamic focusing in both transmit and receive [48]. The imaging is performed by circular transmission with a single or a collection of elements. The origo of the wave is therefore known precisely and can be used in the beamformation. The scattered signal is then received by all elements of the orthogonal transducer elements. The path from transmission to reception can, thus, be precisely calculated. A full volumetric image of the object is focused for each emission as the whole image volume is insonified. This is a low-resolution volume, as it is only focused in transmit. Repeating the process for a number of virtual sources and summing all the low-resolution volumes will yield a high-resolution volume, which is dynamically focused on both transmit and receive.

The spread of the virtual sources and the corresponding largest distance span will determine the FWHM attainable in the transmit direction and correspondingly, the spread of the receive elements will determine the FWHM in the orthogonal direction. The contrast for the resulting PSF is determined by the number of transmit sources and the number of receiving elements. Currently, the best image quality is attained by emitting with a virtual source in one direction and then receiving with the orthogonal elements. SA focusing will then yield the optimal PSF if the beamformer described in Section IV-A is employed. Often a group of elements is used as emitters to increase the emitted energy [49], [50], and the effective width of the aperture is then reduced by the number of elements in the virtual source.

The focusing ability is also dependent on how many receiving element that can contribute to the receive focusing, which is determined by the acceptance angle given by [51]

$$\alpha = 2 \arctan \frac{1}{2F\#}.$$

A wide element will restrict the acceptance angle and increase the possible F-number. The minimum attainable F-number of 0.5 is obtained when the element has a size of half a wavelength. This also applies for the transmitting elements, and the ideal pitch of the RC array is, thus, $\lambda/2$.

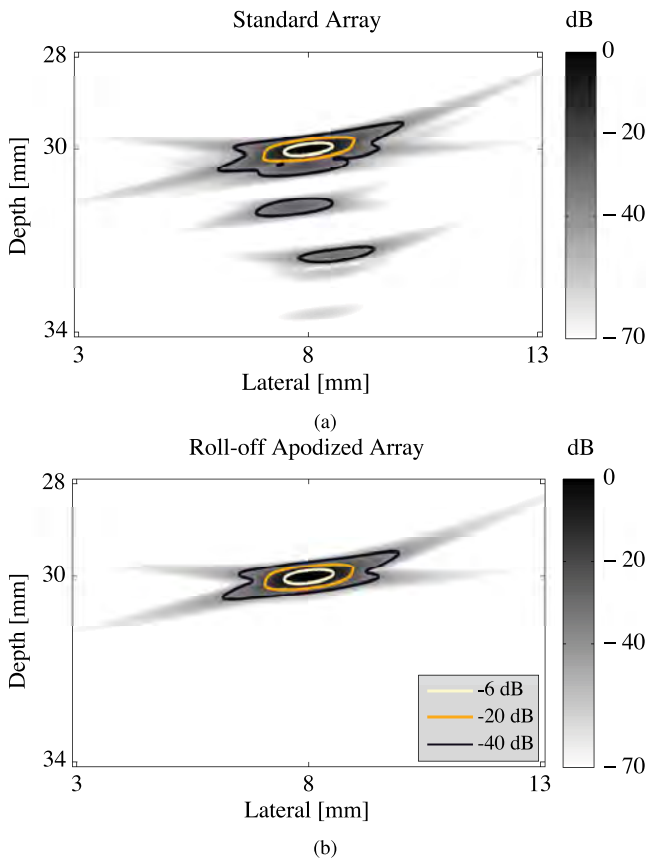

Fig. 4. PSF for two 64 × 64 simulated RC arrays at $(x, y, z) = (8, 3, 30)$ mm. (a) PSF of a standard nonapodized transducer array. (b) PSF of a transducer array with integrated roll-off apodization. The main response of the PSFs is practically identical, but the ghost echoes of the roll-off apodized array are greatly suppressed compared to the nonapodized standard array (from [24]).

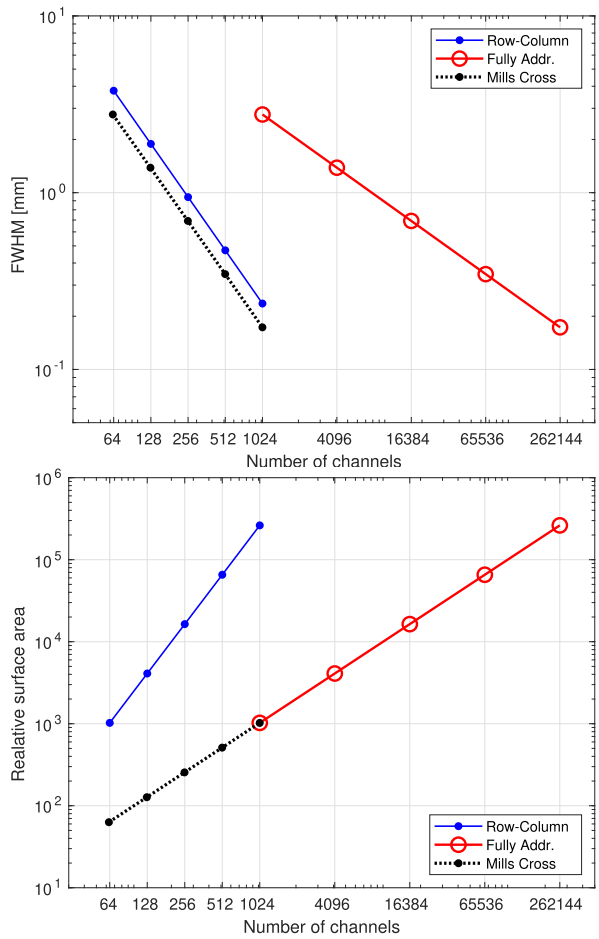

Fig. 5. Comparison of resolution (top) and array size (bottom) between an RC, a fully populated, and the Mills cross array (from [26]).

A. B-Mode Performance of RC Arrays

An example of the PSF and image quality obtainable from a 6-MHz Vermon 128 × 128 elements RC array is shown in Fig. 6. An SA sequence with 96 row emissions followed by 96 column emissions were made using an F-number of −0.7 with 32 elements and Hanning apodization in transmit. The scattered signals were received on all 128 orthogonal elements. This was beamformed with an F-number of 0.7 and a Hanning apodization for both transmit and receive. Imaging was conducted on a 3-D printed PSF phantom [52] with scattering cavities in a 6×4×4 grid with a 2.05-mm spacing in all three directions. The scatterers are 205 μm wide along the x- and y-axes, but only 80 μm in the z-direction. A Verasonics Vantage 256 scanner was used for the measurements shown on the top row in Fig. 6, and Field II [53], [54] was used for the corresponding simulation shown in the second row.

An isotropic resolution of $(1.05\lambda, 1.10\lambda, 0.62\lambda) = (x, y, z)$ is attained for the measured data, and a similar performance is seen for the simulated data. The data are also compared to a simulated 6-MHz linear array translated over the aperture in steps of 0.2 mm obtaining 100 images. A 12 emissions' SA sequence was used, and the images from this volumetric scanning are seen in the third row. The linear array probe has an elevation resolution determined by the geometric elevation focus at 22 mm with an F-number of 4.4, and the four rows of point scatterers can therefore not be differentiated due to the fixed elevation focus. The acquisition of the linear array dataset necessitated 12 × 100 = 1200 emissions and mechanical translation, whereas the RC dataset used 192 emissions corresponding to a normal focused linear array image. A volume rate of 52 Hz can therefore be attained down to a depth of 7 cm.

Finally, the bottom row in Fig. 6 shows the *in vivo* images of a Sprague-Dawley rat kidney. The dynamic range is 60 dB and an isotropic speckle pattern is seen in all three imaging planes due to SA imaging, a constant F-number throughout the image, and the large size of the RC array.

Resolution as a function of depth is visualized on the two left columns in Fig. 7, where points are seen in the xz planes and the wires in the yz-direction. The array has also been used for scanning a tissue-mimicking cyst phantom with an attenuation of 0.5 dB/[MHz·cm], as shown in the two right most columns in Fig. 7. The cyst size diameters are 2.0, 4.0, and 8.0 mm. The 2-mm cysts can clearly be seen down to 50 mm, and the 4- and 8-mm cysts are visible down to the penetration depth of 110 mm.

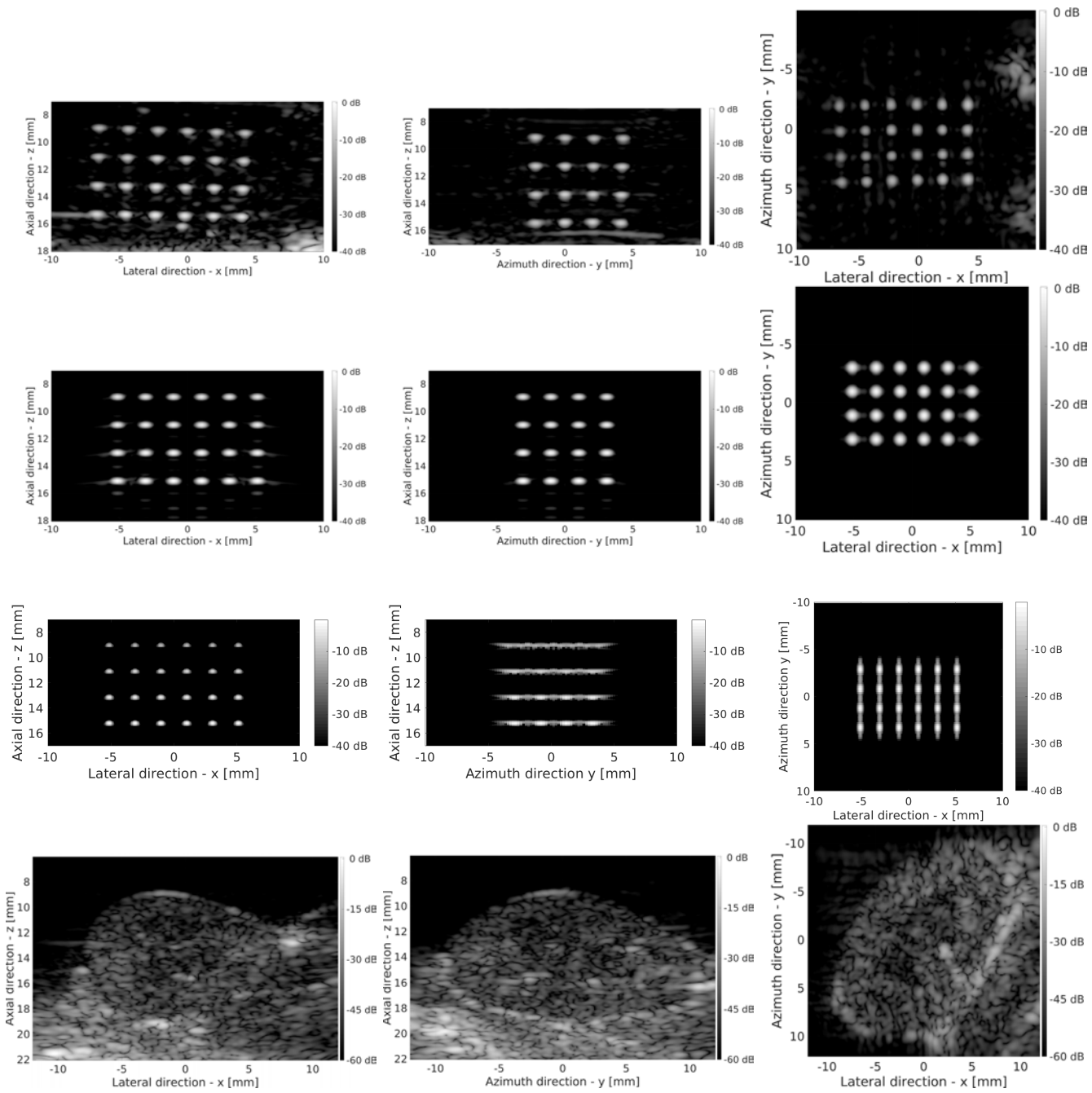

Fig. 6. PSFs obtained from a 3-D printed phantom with isolated point targets using a 6-MHz Vermon 128 × 128 elements RC array with λ pitch. The top row shows the measured images in the *xz*, *yz*, and *yx* planes (left to right). The corresponding simulated data from the phantoms are shown in the next row. Simulated data for a linear array probe translated across the phantom are shown in the next row for a GE 6-MHz linear array using an SA sequence. The bottom row shows the images of a rat kidney in all three planes.

The array used here is far from optimal for SA imaging. No edge apodization is included in the array and the probe pitch is λ, which limits the acceptance angle in both transmit and receive. An optimal array with both these properties does currently not exist and can therefore only be simulated. The optimal resolution possible using SA imaging for a 192 × 192 elements RC array has been simulated for two types of arrays in [55]. Both have $\lambda/2$ pitch for optimal imaging with geometries shown in Fig. 8, where the first is a traditional rectangular grid array and the other is an interwoven array for increasing the active area of the array. The second array is only possible to manufacture with silicon CMUT fabrication processes, whereas the first array can be made using the traditional PZT technology. The long elements are edge apodized to avoid the ghost artifacts after the PSFs. Imaging is conducted by emitting with one element at a time and receiving with the orthogonal elements, so a full volume uses 192 emissions, which is the same as for normal

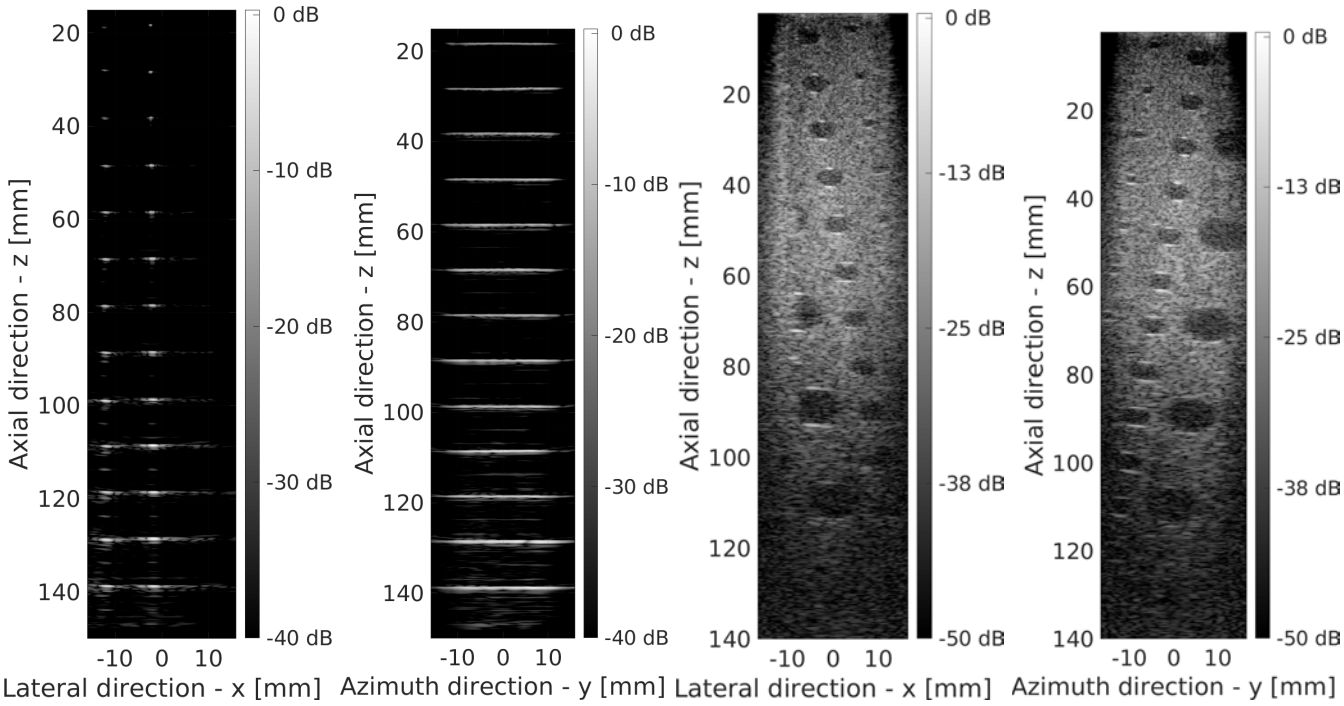

Fig. 7. Two left columns: orthogonal wire phantom images for the Vermon RC probe for a matrix wire phantom with two rows of wires stretch out along the *y*-direction. Two right columns: orthogonal cyst phantom images for the Vermon RC probe for a tissue-mimicking phantom with an acoustical attenuation of 0.5 dB/[MHz·cm].

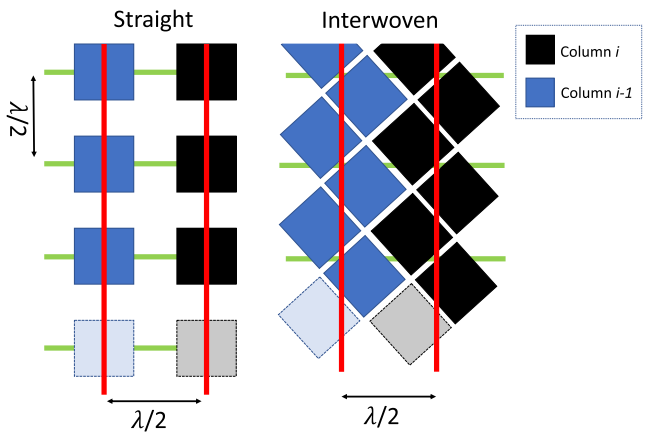

Fig. 8. Simulation setup. To the left, the straight element RC array is visualized. The cells have $\lambda/2$ spacing, which matches the interelement spacing. The interwoven structure is visualized to the right. The red lines symbolize the assumed acoustic center of the column elements, the green likewise for the rows (from [55]).

TABLE I
ESTIMATED METRICS FOR THE SIMULATED PSFS FOR THE TWO 192 × 192 ELEMENTS RCAS (FROM [55])

FWHM	Azimuth-Range	Elevation - Range	C-plane
Straight	0.62 λ	0.60 λ	0.60 λ
Interwoven	0.61 λ	0.62 λ	0.62 λ
CR20dB	Azimuth-Range	Elevation-Range	C-plane
Straight	1.42 λ	1.42 λ	1.43 λ
Interwoven	1.34 λ	1.34 λ	1.30 λ

linear array imaging, but here, the full volume is acquired and perfectly focused in all three directions.

The PSFs for the arrays were simulated in Field II and the quantitative numbers for FWHM and contrast are shown in Table I. It can be seen that the resolution is very close to an ideal obtainable resolution of $\lambda/2$ for SA focusing and a good contrast is also obtained. Full apodization in transmit and receive has not been employed, and this is why the PSFs are not round and have edge effect artifact, which can be avoided with proper apodization. The contrast is slightly lower than for normal SA imaging 1-D arrays, due to the switching between rows and columns in transmit and receive.

IV. IMAGING PENETRATION FOR RC ARRAYS

The large active area of the RC probe is advantageous for attaining a large penetration depth, defined as the imaging depth, where the signal-to-noise ratio attains a value of 0 dB. This is shown in Fig. 9, where the 128 × 128 elements Vermon RC array was used for imaging a cyst phantom with an attenuation of 0.5 dB/[MHz·cm]. The 6-MHz PZT array attains a penetration down to 11 cm or 428λ when using only 32 elements in transmit using an F-number of -1. Similar results have been attained in [26] for two 62 × 62 elements RC arrays, one fabricated using CMUT technology, and one traditional PZT array. The 3-MHz PZT array attained a penetration down to 14 cm when using only a single element in transmit, whereas using an F-number of 1 or -1 gave predicted penetration depths of 25–30 cm, considerably more than the conventional array's penetration of 300λ–400λ (15–20 cm). Here, it should also be kept in mind that these are first version

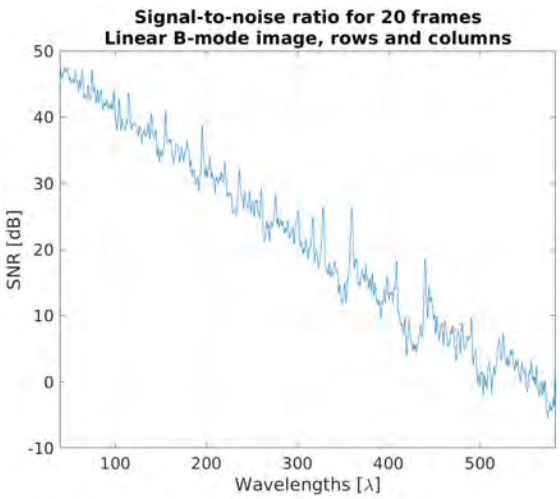

Fig. 9. SNR of the Vermon RC probe for a tissue-mimicking phantom with an acoustical attenuation of 0.5 dB/[MHz·cm] for the images shown in Fig. 7. The wavelength λ for soft tissue is 0.257 mm for the 6-MHz probe, and 400λ corresponds to 102.7 mm. The penetration depth when the SNR is 0 dB is roughly 550λ corresponding to 141 mm.

prototype arrays, the experimental scanner SARUS [56] was used, and the arrays were fairly small (62 × 62 elements, $\lambda/2$ pitch). A more realistic array with 256 × 256 elements would have a 16 times larger surface area, and using a better prototype and scanner would also significantly increase the penetration depth. This can be translated to imaging with a higher center frequency if the large penetration depth is not needed, which would increase resolution in all three directions proportionally to the wavelength. For the 62×62 elements PZT probe using an F-number of −1, the measured mechanical index (MI) was 0.67 and the derated spatial-peak-temporal average intensity I_{spta} was 0.53 mW/cm. The allowable limits for MI is 1.9 and 720 mW/cm for I_{spta} for peripheral vessels [57]. It is, thus, possible also to increase the transmitted pressure by a factor of 3, and the limit on I_{spta} can essentially not be reached, showing the further potential for increasing the signal-to-noise ratio.

A. Beamforming Implementations

Beamforming of RC data must consider the long and narrow elements, where the emitted field is a plane wave along the long side and a circular wave in the orthogonal direction, as shown in Fig. 3. The left figure illustrates a focused emission at **sf** in the yz plane and the emission of the plane wave in the xz plane, so the emitted field is described as a focal line and not as a focal point. The ToF calculation has to take this into account, where the transmit time is from the transducer surface to the focal line and from the focal line to the field point **fp**. The time to reception is then from **fp** to the center of the receiving elements. The projection of the distances to the long elements is shown in Fig. 10. A more detailed explanation and the exact equations can be found in [24].

The importance of replacing the delay calculation with the specifics for the RC array rather than the traditional

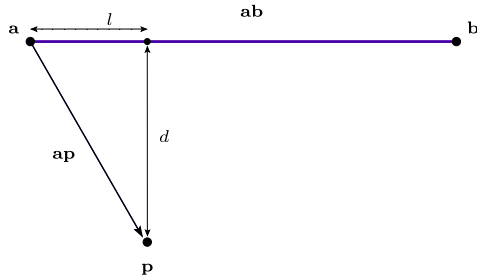

Fig. 10. Projection of the point **p** onto the line segment **ab**. *l* is the distance from **a** to the projected point and *d* is the shortest distance from **p** to **ab** (from [24]).

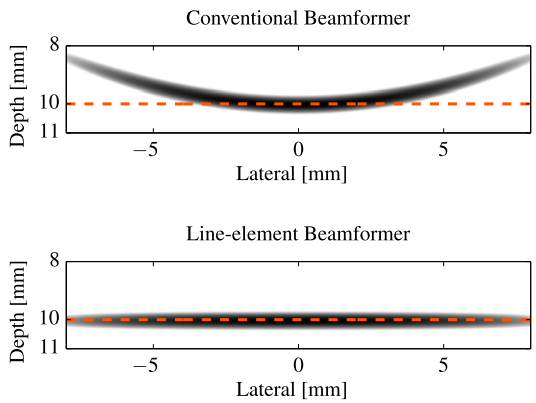

Fig. 11. B-mode images of a wire phantom beamformed with a conventional beamformer (top) and with the proposed line element beamformer (bottom). The dashed lines indicate the location of the wire phantom. The B-mode images are shown with a dynamic range of 40 dB. When using a conventional beamformer, the B-mode is seen to be geometrically distorted (from [24]).

spherical delay calculation is shown in Fig. 11, where the received signal quickly attains the wrong geometric position, if the new calculation method is not employed. This can both lead to the geometric distortion shown but also leads to a diminished resolution and contrast, if not implemented properly.

Efficient implementations of this type of beamforming have been developed for a GPU in [58] and [59]. The software is written under the CUDA environment and takes in radio frequency (RF) data from the RC channels and then yields a focused line, image, or volume. The beamformer is parametric and can be used for very large volumes only limited by the RAM of the GPU card. An example of performance for a state-of-the-art Titan V Nvidia card is shown in Fig. 12. This roughly corresponds to the newer Nvidia GTX 3090 card. This GPU can attain a beamforming performance of around 40 Gsamples/s. Two intersecting B-mode images with 96 lines containing 512 samples for a 192×192 elements RC array can, thus, be beamformed with a frame rate around 30 Hz when 64 emissions are used for creating the volume. A full volume with 96 × 96 lines can be beamformed in 1.45 s. It is, thus, possible to make real-time scanning and plane visualization with a state-of-the-art GPU card, and the full volume can be beamformed in a reasonable time for off-line visualization and inspection.

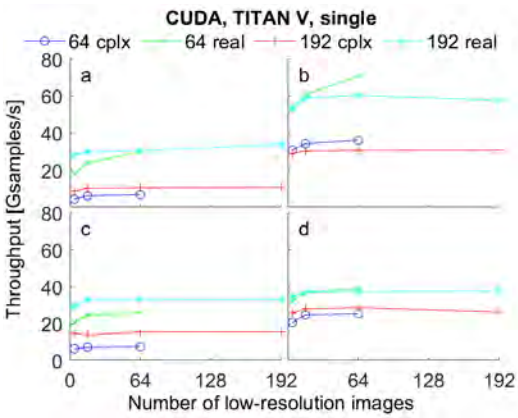

Fig. 12. Throughput as a function of number of low-resolution images for the CUDA beamformer on the TITAN V GPU with single-precision calculations. (a) and (b) Throughputs for the shallow phantom and (c) and (d) deep phantom. (a) and (c) Cross planes and (b) and (d) full volumes. The colored lines show performance for 64 or 192 receiving elements and for real or complex (cplx) sample values (from [58]).

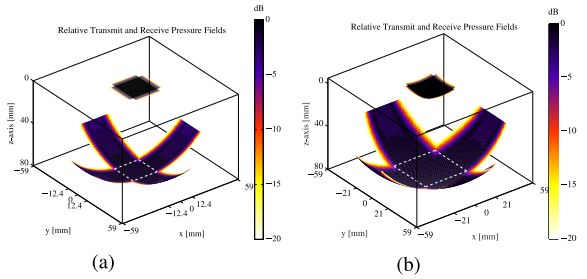

Fig. 13. Relative transmit and receive pressure fields at a radial distance of 80 mm for azimuth and elevation steering angles from $-45°$ to $45°$. The imaging area is the intersection of these two fields, which is the rectilinear forward-looking box and the curvilinear forward-looking region in front of the transducer using a lens with $f_{\#} = -1$ (from [60]). (a) Flat RC array. (b) Curved RC array.

B. Lensed RC Imaging

Currently, flat RC probes can only image in the rectilinear region below the active transducer surface. This is acceptable for small parts imaging near the probe surface, but for abdominal or cardiac imaging, the field of view is too limited and has to be expanded. This can be attained using either a lens in front of the probe or by fabricating a convex probe. The imaging region is shown in Fig. 13 for both a flat and a lensed array, which expands the usable field of view. The flat array is restricted by the large elements, which limits the field along the element length, and the combination of transmitting with, e.g., the rows and receiving with the orthogonal elements gives a field of view, which is the intersection of the two limited regions. This is expanded by the diverging lens, as shown in the right figure.

Lensed RC probes are in the early stage of development, and very few results have so far been published [60], [61]. The results are based on concave lenses attached to the 62×62 element probe described before [24], [25], and it is needed to modify the beamforming geometry to include this in the delay calculations. Fig. 14 shows how the diverging lens changes the ToF, which has to be accounted for in the beamformer as described in [60].

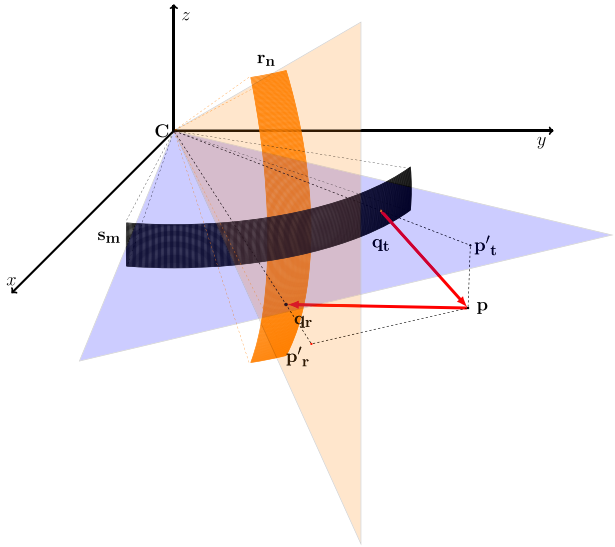

Fig. 14. ToF of a wavefront is given by the shortest distance from the source $\mathbf{s}_m$ to the point being focused $\mathbf{p}$ and back to the receiving element $\mathbf{r}_n$, divided by the speed of sound (from [60]).

The diverging lens beamformer has been simulated for both point and cyst phantoms with good results demonstrating the larger field of view. The same general trend is seen for the cyst phantom simulations, where a larger field of view is attained along with a good contrast in the image [60]. Lenses for the 62×62 elements RC array have been fabricated and tested on the arrays. Results for wire and cyst phantoms have been measured and processed and are shown in Figs. 15 and 16. They both show similar results as for the simulations that an increased field of view is attained along with good focusing abilities and an acceptable contrast. More results and details can be found in [61].

The current equations in the lensed beamformer give reasonable results, but it has been shown that ray-tracing theory can further enhance the quality of the results and increase the field of view [62]. This should be further investigated and incorporated in the beamformers.

C. Convex RC Imaging

An obvious method to avoid making a lens would be to shape the RC probe in a double curved, convex shape as suggested in [17]. The SA sequence developed for flat RC arrays would be nearly directly applicable to a convex array, where the beamforming then would take the geometry into account. Such arrays would have many benefits for abdominal ultrasound imaging. Their footprint could be made quite large, which ensures a low F-number even for large depths. The large size would also ensure a large penetration depth, as the emitted energy is distributed over a large area keeping MI low but still acquiring the returned energy from a large surface. Démoré *et al.* [17] demonstrated that a 128×128 RC convex array could cover at $60° \times 60°$ sector with a good image quality using their imaging scheme.

V. Flow Imaging

Current commercial scanners can all display the velocity of blood in the human circulation. The blood motion is detected

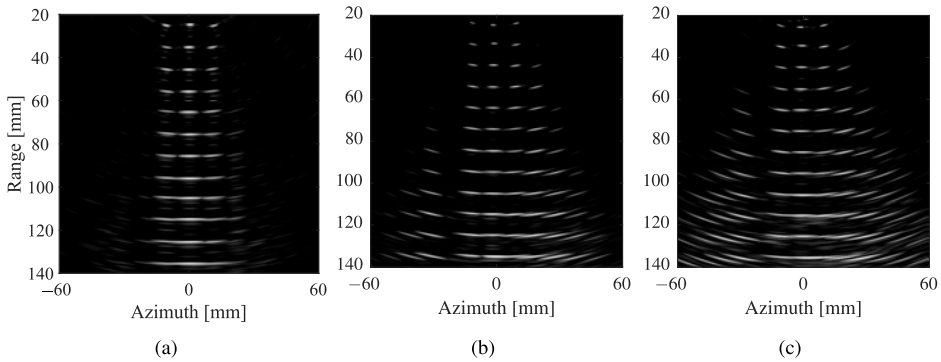

Fig. 15. Examples of a wire grid phantom imaged without and with different lenses are shown using a 30 dB dynamic range, (a) without lens, (b) for the 25.4 mm radius lens, and (c) for the 12.7 mm radius lens (modified from [61]).

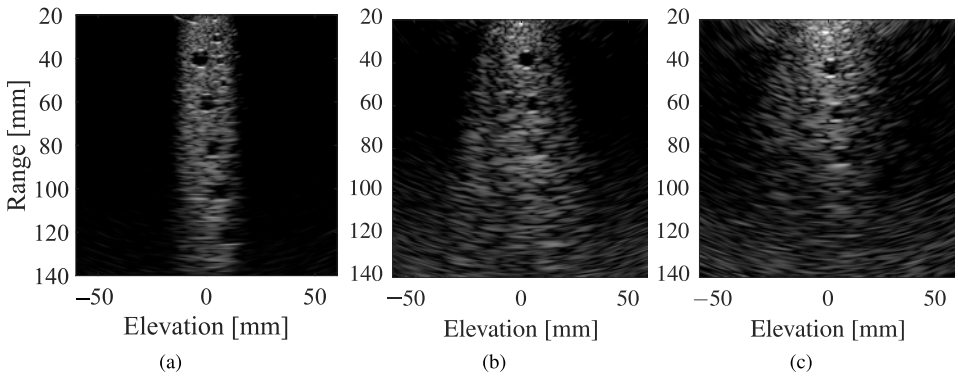

Fig. 16. Hollow cyst phantom images with both lenses are shown using a 40 dB dynamic range, (a) without lens, (b) for the 25.4 mm radius lens, and (c) for the 12.7 mm radius lens (modified from [61]).

by estimating the positional shift between two emissions using correlation-based estimators finding either the phase or the time shift [63]. These methods are well established and widely used in the clinical for quantifying vascular diseases. They, however, have several drawbacks. The detected shift is only in direction of the ultrasound beam, and most vessels run parallel to the skin surface, so the least important velocity component is detected. This is often remedied by titling the ultrasound beam and introducing angle compensation methods. These are unreliable for angles close to 90°, and for complicated vessel geometries, the angle will vary as a function of space and time precluding a single angle correction factor. This has been remedied by introducing vector flow imaging (VFI) in a number of methods [64], [65]. One VFI method uses the transverse oscillation approach where an oscillation perpendicular to the ultrasound beam is introduced during receive beamforming, and the shift in the lateral direction can then be estimated yielding the full 2-D velocity vector [66], [67]. This has been shown in a number of clinical studies to give improved flow estimates, which are more consistent and easier to use for medical doctors [68].

A. Tensor Velocity Imaging

The VFI approach gives consistent results for flow in the 2-D plane but neglects the out-of-plane component. The approach has therefore been translated to RC arrays for both traditionally focused emissions [69], [70] and for a fast SA-based approach [71], [72] using interleaved SA imaging [73], [74]. Here, the full 3-D blood velocity is estimated in the volume for each time instance for full tensor velocity imaging (TVI). The probe can be placed to just cover the vessel, and the full velocity vector is estimated for any position in the volume with hundreds of estimates per second.

An example of TVI is shown in Fig. 17 for measured pulsating flow in a carotid artery phantom, where the arrows indicate the direction and the colors indicate the velocity magnitude. The velocities over time for different positions in the vessel are shown in Fig. 17, showing that the velocity components in all directions can be estimated as a function of time everywhere in the volume. The full 3-D vector velocity field can therefore be acquired for a couple of heartbeats, and the velocity for any place and time can be determined retrospectively after the acquisition has been made, thus increasing the clinical relevance.

Further validation of the TVI method was performed using finite element method (FEM) simulations of pulsating flow in an *in silico* carotid artery phantom [75], where the ground truth is known. Motion correction was employed to improve the estimates [72], and the result is shown in Fig. 18 for both an autocorrelation estimator (left column) and cross correlation

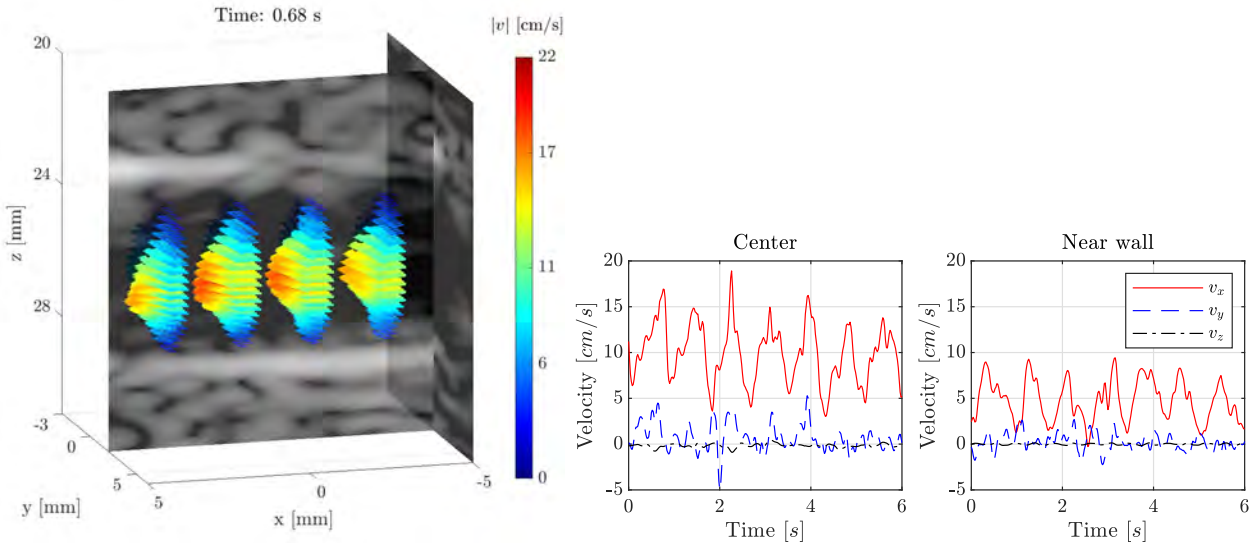

Fig. 17. Pulsating flow in a tissue-mimicking phantom is shown on the left. The flow is visualized using arrows, where color shows velocity magnitude and the arrows depict velocity direction and magnitude. The middle graph shows all three velocity components v_x, v_y, v_z (red, blue, black) for a point in the vessel center. The right graph shows the components at a point placed near the vessel wall (modified from [71]).

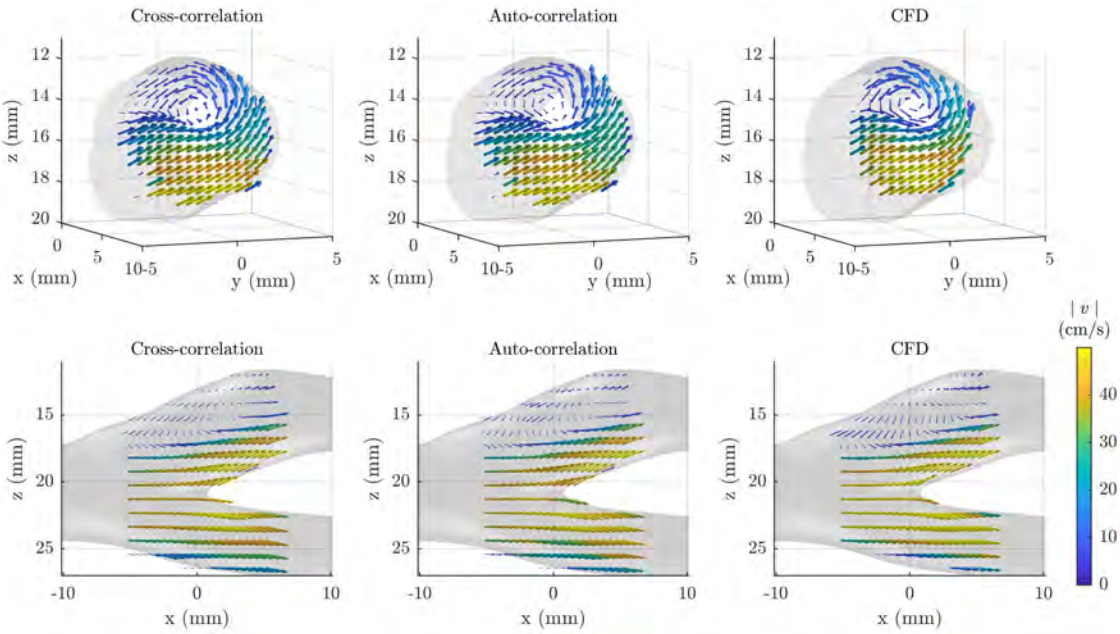

Fig. 18. TVI using a 62 × 62 elements RC array from simulated data in the carotid artery for two different estimators compared to the ground-truth finite element data on the right. Arrows indicate direction and magnitude, which is also indicated by the color. A vortex in the upper vessel branch is seen in the top row, and reverse flow is also present in the bottom row (from [75]).

estimator (middle column) and for the ground-truth FEM data. The estimates were found using an f_{prf} of 20 kHz and only 62 receive channels. In general, the relative standard deviation and bias were below 5% in most cases, yielding fully quantitative results independent of the relative position between the vessel and the probe.

VI. Super-Resolution Imaging

The latest addition to medical ultrasound is SRI, where the microvasculature can be visualized down to vessel sizes of 20–50 μm. This is attained by injecting a standard contrast agent (SonoVue) intravenously and then image the motion of the gas filled bubbles. A sparse distribution of bubbles makes it possible to track individual bubbles and establish their position with micrometer precision [76]–[82]. The data are acquired over minutes and motion correction of the acquired data must be performed to maintain resolution [83]–[89], but as most of the current methods are in two dimensions, they cannot compensate for large motions and out-of-plane motion.

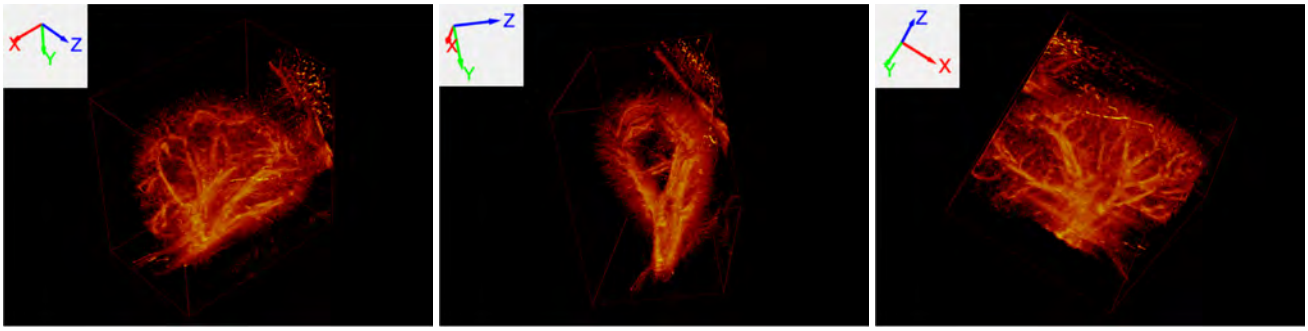

Fig. 19. Super-resolution images of the vasculature in a Sprague-Dawley rat kidney acquired *in vivo* using the 6 MHz 128 × 128 RC array. SonoVue was injected intravenously and the data acquired over 135 seconds. The images show the large segmental arteries and veins, the smaller arcuate vessels, and the small cortical radial vessels extending toward the surface of the kidney. The B-mode images are shown in Fig. 6.

It has been demonstrated that RC probes can also be used for SRI [90]. A 3-MHz 62 × 62 elements RC array with a half-wavelength pitch was used with an SA pulse inversion sequence with 32 positive and 32 negative row emissions for acquiring volumetric data using the SARUS research ultrasound scanner. Data received on the 62 columns were beamformed on a GPU for a maximum volume rate of 156 Hz when the pulse repetition frequency was 10 kHz. Investigations were performed on 3-D printed point and flow micro-phantoms, where the flow micro-phantom contained a 100-μm radius tube injected with the contrast agent SonoVue. The 3-D processing pipeline uses the volumetric envelope data to find the bubble's positions from their interpolated maximum signal and yielded a high resolution in all three coordinates. The localization precision for tracking a 3-D printed point phantom was (20.7, 19.8, 9.1) μm in the x-, y-, and z-coordinates. The flow micro-phantom had an estimated radial precision of 16.5 μm in the yz plane and 23 μm in the xz plane [90].

This approach has been translated to the Vermon 128 × 128 array for measurements on a Sprague-Dawley rat kidney. An amplitude modulation sequence with three emissions for the same virtual source and 48 virtual sources spread out over the row elements was employed at a pulse repetition frequency of 20 kHz between the three emissions and 1.3 kHz between the virtual sources for a volume rate of 24 Hz. A 1:5 dilution of SonoVue at an intravenous infusion rate of 55 μl/min was employed over the 135-s acquisition. The data were then processed with an SRI pipeline as described above, and the final 3-D images are shown in Fig. 19 for three different views. The volume rate was fairly low, to keep the data rate low to enable acquisition over a long period of time. For this shallow scanning down to 3 cm, f_{prf} could be maintained at 25 kHz for a volume rate of 250 Hz or recursive imaging [91] could be used to raise the volume rate to 8.3 kHz.

This technique makes it possible to visualize the flow in vessels with sizes down to 20 μm, which can be used in the diagnosis of vascular diseases found along with, e.g., cancer and diabetes. The images can both reveal the anatomy of the vasculature to reveal vascular rarefaction, neonvascularization, increased tortuosity, and so on and give quantitative data for the flow to identify changes caused by disease [92], [93].

VII. Discussion and Conclusion

It has been shown that RC arrays essentially can be used for any kind of ultrasound imaging for visualizing the anatomy, blood flow, and tissue motion and performing SRI allowing visualization of the microvasculature and measurement of flow velocities in the microcirculation. The active number of array elements is of the same order as for conventional 1-D arrays, and the number of transmitters and receivers is therefore as for conventional 2-D imaging. Demands on the transmit stage receive data rates, and storage sizes are also the same as for 2-D imaging. The number of beamforming operations depends on what should be visualized in terms on planes and volumes, but high-end GPU cards are capable of attaining real-time visualization of orthogonal planes, and 3-D solid volumes can be calculated in seconds [58], [59].

A good B-mode image quality can be attained by using SA sequences with 2 × 96 emissions on a 128 × 128 elements RC array, yielding an isotropic PSF in the region where a constant F-number can be maintained. FWHM can be close to the diffraction limit if the array is optimized for high-quality imaging with edge apodization and a pitch of $\lambda/2$. Even the first version substandard arrays with λ pitch and no edge apodization can yield high-quality *in vivo* images as shown on a rat kidney scan. Comparing these results to traditional 2-D imaging, it should be kept in mind that the yz and xy planes are never shown. These planes for traditional linear arrays with a fixed geometric focusing have very poor resolution, which at the optimal geometric focusing often is 3–5λ and away from this focus can be 10λ–20λ instead of 0.6λ attained here. With the RC arrays, it is, thus, possible to attain an isotropic resolution, and much better imaging with a uniform speckle pattern is possible, where any slice and orientation can be attained retrospectively after the data have been stored.

The large size of the arrays, and the use of the full aperture during reception and synthetic transmission, makes the signal-to-noise ratio high. The penetration depth is above 550λ even for low-intensity and low MI transmission and can be increased to be above 800λ for higher pressure transmission surpassing that of conventional 1-D arrays. This is also surpassing 2-D matrix arrays, as their elements are small and

often sparse arrays have to be used to keep the element count manageable.

TVI can also be obtained using an RC array with only 62–128 receiving elements and a transverse oscillation approach. The full velocity vector in any direction and at any place in the volume can be shown as a function of time. Using SA imaging and recursive imaging makes it possible to retrospectively probe any location in the volume and see the time evolution of the flow. Vortices and complex flow are easily visualized for any slice, making quantification easier. The method is complex with interleaved emissions, transverse oscillation, motion correction, and dedicated beamformers and estimators resulting in a high computational load. The demands are a factor 62–128 times lower than for a fully populated array, and modern GPUs offer thousands of processing units to make real-time beamforming and estimation possible.

Volumetric SRI can also be attained by RC arrays with a resolution down to 15 μm. A long observation over minutes is essential to ensure imaging of the smallest vessels, and the data rate from the arrays should therefore be low. This is very difficult to attain for fully populated or sparse matrix arrays due to the many elements, and they are also difficult to manufacture due to the small $\lambda/2$ pitch elements when the frequency is high. RC arrays, therefore, have distinct advantages for SRI as the data rate corresponds to normal linear arrays, and high-frequency arrays are easier to manufacturer and attain the needed signal-to-noise ratio for the low MI emissions demanded for contrast agents. Here, SA is also beneficial as the emitted MI is low, and a good SNR is attained when all emissions are combined.

RC arrays currently also have a number of drawbacks. The imaging is now performed by switching between the transmitting and receiving aperture, and this necessitates more emissions for SA 3-D imaging than what is currently used for 2-D SA imaging. Often only 8–12 emissions are needed for very high-quality 2-D SA images, whereas 48–96 times two emissions are needed for an optimal volumetric image quality. New methods for improving this are currently being investigated [47]. It should also be possible to develop combined sequences, where data are acquired for both anatomic and functional imaging with an optimal image quality at fast volume rates and where both high and low velocities can be reliably estimated from the same data. This is an area of active research.

The contrast in 3-D imaging is also poorer than for 2-D imaging, and this should be further optimized. This problem is also related to the lack of proper arrays. Rasmussen *et al.* [24] showed that edge apodization of the elements is vital for avoiding ghost echoes, and the imaging also benefits from having $\lambda/2$ pitch elements, which very few RC arrays have. Having better arrays with the correct geometry will obviously improve both image quality and frame rate to mature RC technology. The imaging region of current flat arrays is also limited to the rectangular region of the transducer footprint. This can possibly be solved by employing lensed RC arrays or convex RC arrays, but again, proper arrays are lacking and should be developed.

Overall, it can, however, be stated that RC arrays can fulfill all the demands for fast, high-quality volumetric ultrasound imaging. Anatomic, flow, functional, and SRI have all been demonstrated for simulations and phantom measurements and a few *in vivo* examples. It is our hope that the great potential of general RC imaging will be demonstrated in future clinical trials using optimized arrays. The combination of having a large array capable of having a good focusing, contrast, and penetration depth can, especially for abdominal imaging, lead to high-quality 3-D anatomic and functional images.

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Appendix D

Paper B - Compensation for Velocity Underestimation in 2D Super-Resolution Ultrasound

Compensation for Velocity Underestimation in 2D Super-Resolution Ultrasound

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***Abstract*—Super-resolution ultrasound imaging (SRI) has shown the potential for visualization of the vasculature with sub-wavelength resolution. Microbubble (MB) tracking in SRI can improve image quality and enable velocity estimation. However, it is usually neglected that the size of the vessel might be relatively small compared to the full width half maximum resolution in the elevation direction (FWHM$_y$) and the velocity estimated by tracking algorithms is usually lower than the true velocity. Considering the small size of desired vessels in SRI, it is hypothesized that the velocity is underestimated in SRI when the MB contributions are averaged in the elevation direction. In this work, a theoretical model is introduced, which shows peak velocity of a 3D parabolic velocity profile underestimated by 33% in 2D imaging when the size of vessel is smaller than the FWHM$_y$. The hypothesis was verified using Field II simulations and hydrogel 3D printed micro flow phantom measurement. A GE L8-18i-D linear array transducer with FWHM$_y$ of approximately 770 μm at the target imaging depth and a Verasonics Vantage 256™ scanner were used. Simulation and measurement results were compared to the theory. Simulations with various parabolic velocity profiles showed that the peak velocity was underestimated by 26% ± 5% (mean ± standard deviation), and in the measurement the underestimation was 34% ± 8%. The results were in correspondence to the theoretical value of 33%. Therefore, in this case the theoretical model can be used for compensation of velocity estimates.**

***Index Terms*—Super Resolution Imaging, Ultrasound Imaging, Velocity Underestimation, 2D Super Resolution Ultrasound**

I. Introduction

Super-resolution ultrasound imaging (SRI) has shown the potential for visualization of the vasculature with sub-wavelength resolution [1], [2]. Microbubble (MB) tracking enables estimation of clinically meaningful parameters such as velocity. Tracking also improves the quality of super-resolution images by filling the gaps between the detections and removing potential false detections. So far, several tracking algorithms have been used in SRI with an initial focus on making velocity maps and better MB assignment [3]–[11]. Typical tracking algorithms tend to ignore the out-of-plane velocity as focus in elevation is static and controlled by an acoustic lens and it is usually neglected that the size of the vessel might be relatively small compared to the beam width in the elevation direction. This however, leads to small vessels being entirely inside the elevation beam resulting in an image that is effectively an integration of vessels along the elevation direction. Although this is a good thing when visualizing structures it might introduce higher uncertainty and bias in the velocity estimates. Considering the small size of desired vessels in SRI, it is hypothesized that the velocity is underestimated in SRI, when the MB contributions are averaged in the elevation direction.

In this work, a theoretical model is introduced in Section II, which shows the underestimation in peak velocity. To evaluate the hypothesis, the velocity was estimated from tracking of scatterers both in simulations and in a micro-flow phantom, described in Section III. Then, in Section IV, the estimated velocity from simulations and phantom measurement were compared to the theoretical model and the ground-truth velocity profile. Finally the paper is concluded in Section V.

II. Theory

Theoretically, averaging a 3D parabolic velocity profile along the radial direction of a vessel results in a 2D parabolic velocity profile can be modeled as

$$v(x) = \frac{1}{2R}\int_{-R}^{R} V_{peak}\big(1-\frac{x^2+y^2}{R^2}\big)dy = V_{peak}\big(0.67-\frac{x^2}{R^2}\big), \quad (1)$$

where V_{peak} is the peak velocity and $R <$ FWHM$_y$/2 is the vessel radius. The term $R <$ FWHM$_y$/2, indicating that vessel is smaller than the thickness of ultrasound beam, is also an assumption for (1), therefore the integration is over the entire radius of the vessel. According to (1), the averaged velocity profile is still a parabolic profile but the peak velocity is underestimated by 33%. The key question is then whether this theoretical model is realistic enough to be used for compensation of velocity estimates in SRI?

III. Methods

To evaluate the theoretical model, a 168 elements λ pitch linear array probe (GE L8-18i-D) with a center frequency of 10 MHz (λ = 154 μm) was used. The height of the aperture was 4 mm, and the elevation focus was at 20 mm. Therefore the F-number (depth divided by active aperture width) is 5 leading to a beam with minimum thickness of 770 μm in the elevational direction ($\approx$ FWHM$_y$), which is wider than the size of the microvessels. A simple example of such a geometry is shown in Fig. 1. A synthetic aperture amplitude modulation sequence consisting 12 virtual sources each with three emissions of full-half-half amplitudes were used for contrast enhancement.

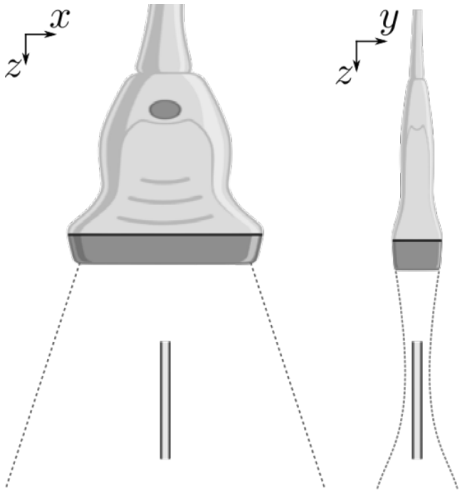

Fig. 1: Geometry of the probe, the ultrasound beam in the elevation direction, and a small vessel. A simple example of a case in which the vessel is completely within the elevation range of the ultrasound beam.

A. Simulation study:

The moving scatterers with a sparse density of 0.1 λ^{-3} inside a tube with a diameter of 250 μm was simulated using Field II [12], [13]. The simulated probe uses the actual properties of the GE L8-18i-D transducer, its measured impulse response, and the emission sequence. The simulation was repeated for peak velocities of 2, 5, 15, and 30 mm/s and each scatterer assumed as a MB. The scatterers were tracked using the nearest-neighbor algorithm. Then tracks for the instantaneous velocities were inserted into a high resolution image [11], forming super-resolution velocity maps. Finally, the mean velocity profile was calculated over several cross-sections of the tube. Then, the standard deviation of the mean profiles with normalized peak velocity was calculated for various peak velocities.

B. Phantom measurement:

In the measurement, a 3D printed hydrogel micro-flow phantom with a micro channel, shown in Fig. 2, was scanned using a Vantage 256™ scanner (Verasonics, United States). The phantom was precisely printed with a channel diameter of 205 μm [14]. A dilution of SonoVue (Bracco Imaging, Milan, Italy) with 0.9% saline (1:5) was infused with flow rate of 0.1 μL/s through the phantom inlet. The schematic for this measurement setup is shown in Fig. 3. The velocity maps were created using MB tracking [11]. The mean and standard deviation of velocity profiles were calculated over 10 cross sections of the channel.

IV. Results and Discussion

The mean and standard deviation of the profiles from the different velocity scenarios are shown in Fig. 4. According to the theoretical model, described in (1), the projected 2D profile has a 33% lower peak velocity. In the simulations, the peak velocity was underestimated 26% $\pm$ 5% (mean $\pm$ standard deviation), and in the measurement the underestimation was 34% $\pm$ 8%. Localization and tracking of highly

Fig. 2: 3D printed hydro-gel phantom with a 205 μm size channel after the perfusion testing with green dye (from [15]).

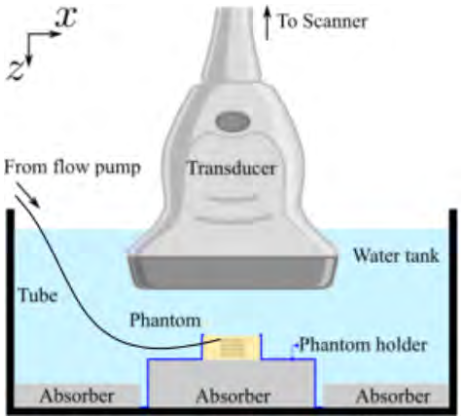

Fig. 3: Measurement setup used for the 3D micro-flow phantom experiment with SonoVue infusion.

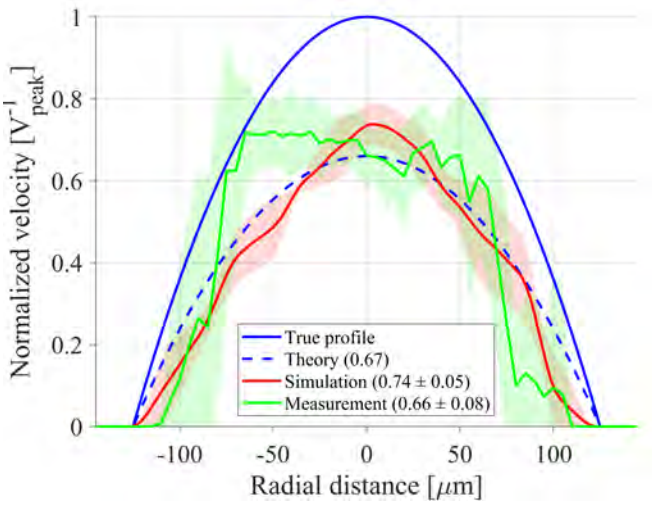

Fig. 4: Comparison of normalized velocity profiles for the simulations (red), phantom experiment (green), theoretical projection of 3D profile in 2D (dashed blue line), and central slice of 3D profile (blue solid line). The shaded area shows the standard deviation for the different profiles.

dense scatterers is recently used for a contrast-agent free SRI, called SUper Resolution ultrasound imaging with Erythrocyte (SURE) [16], [17]. The velocity underestimation of velocity profiles was also demonstrated SRI with the highly dense scatterers in a simulated phantom [18]. The results show that the theoretical model predicts experimental findings very well and uncovers the potential cause of underestimation. This allows for better estimation of the flow in 2D, as it can be compensated for by using the proposed model. The assumption of having the vessels with the smaller size compared with elevational thickness of the ultrasound beam is usually valid for super-resolution ultrasound. For example, in this study, the FWHM_y of the probe was approximately 770 μm at focus, while the microvasculature have a size much smaller than 200 μm. It is worth mentioning that in real case scenarios, the orientation of the vessel also contribute to the amount of averaging over the 3D velocity profile, which is not considered in this paper. One way to avoid the effect of poor elevation resolution on the estimated morphology and dynamic for the vasculature is 3D SRI using matrix probes [19], [20], sparse arrays [21], or row-column addressed arrays [22]–[24].

V. Conclusion

Theoretically, the velocity in the vessels with a small size compared to the elevational thickness of the ultrasound beam is underestimated 33% in 2D imaging. This theoretical model was derived and evaluated using simulations and phantom measurement. The simulation results showed that the peak velocity was underestimated 26% $\pm$ 5% (mean $\pm$ standard deviation). The amount of underestimation in the phantom measurement was 34% $\pm$ 8%. Both results were according to the predicted theoretical value.

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Appendix E

Paper C - Synthetic Aperture High Quality B-mode Imaging with a Row-Column Array Compared to Linear Array Imaging

Synthetic Aperture High Quality B-mode Imaging with a Row-Column Array Compared to Linear Array Imaging

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Abstract*—Row-column (RC) matrix probes can yield 3-D volumetric imaging using a number of receiving elements similar to traditional linear arrays for commercial scanners. Some doubts have, however, been raised on the B-mode image quality of RC probes. It is hypothesized that synthetic aperture (SA) RC imaging can yield a better volumetric resolution than commercial spatially translated linear arrays, and at the same time attain volume rates similar to frame rates for single slice linear array scanning. A Vermon 6 MHz 128×128 elements RC array with λ pitch was used on a Verasonics Vantage 256 scanner. A SA sequence with 2×96 emissions on the rows and columns and reception on all 128 orthogonal elements were employed giving a 62.5 Hz volume rate for a pulse repetition frequency of 12 kHz. The resolution and contrast were compared to an optimized SA sequence for a 256-elements GE L3-12D 6 MHz linear array probe, where the volume was acquired using a linear probe translation in the elevation direction. Imaging was conducted on a 3-D printed point spread function (PSF) phantom with scattering voids in a $6 \times 4 \times 4$ grid with a 2.05 mm spacing in all three directions. The exposed kidney of a Sprague-Dawley rat was also scanned in vivo with the RC probe. B-mode images of the 3-D printed PSF phantom were shown with a 40 dB dynamic range along with the linear array scans. An isotropic resolution of $(1.05\lambda, 1.10\lambda, 0.62\lambda) = (x, y, z)$ was obtained for the row-column probe. The linear array probe had an elevation resolution determined by the geometric elevation focus of the array, and therefore the four rows of point scatterers could not be differentiated in the elevation direction due to the fixed elevation focus. The data rates were identical for the two arrays, but the RC array yielded an isotropic PSF with an improved contrast, and a 62.5 Hz volume rate comparable to normal linear array imaging. In vivo kidney images for the three orthogonal planes were shown with a 60 dB dynamic range demonstrating the isotropic speckle pattern in all three directions for all depths. The SA imaging RC sequence thus yielded a PSF independent of orientation and depth. Any slice plane in the volume therefore had a uniform speckle pattern, contrast, and resolution, demonstrating that RC arrays can yield higher quality B-mode images than linear arrays. The penetration depth of the probe and sequence was also measured to be 550λ corresponding to 141 mm.

I. Introduction

Three-dimensional ultrasound imaging has been devised and investigated since the pioneering work by von Ramm et al. [1, 2] from 1991. Matrix arrays have been employed, where the number of elements on each side is N for a total number of elements of N^2. The number N should be determined from the focusing demands on the array, where Full-Width-Half-Maximum resolution is FWHM $= \lambda F\# = \lambda D/W = \lambda D/(Np_e)$, where $F\#$ is F-number, λ wavelength, D imaging depth, W transducer width, and p_e probe element pitch. The point spread function (PSF) width is, thus, inversely proportional to the number of elements, which makes fabricating good resolution matrix arrays difficult due to the many elements. Further, a doubling of resolution necessitates quadrupling the total number of elements. Many approaches for making sparse arrays have been suggested [3–7], but they suffer from reduced contrast and reduced penetration depth due to the reduction in active transducer surface area.

A remedy for breaking the N^2 dependence on resolution is to employ row-column (RC) arrays, where only the rows or the column are accessed at a time [8–20]. Doubling resolution for these arrays also doubles the number of elements, but quadruples the probe surface. Therefore very large arrays can be made, which can maintain a low F-number for large depths and further yield an excellent penetration depth [21]. The remaining question is then whether a sufficient contrast can be attained for the arrays. The hypothesis of this paper is that row-column arrays can yield better volumetric images than translated linear array probes.

A commercial 128×128 RC array from Vermon, (Tours, France) is compared to a state-of-the-art GE linear array probe through Field II simulations, and results similar to the simulation are shown for the RC array. In-vivo data from scanning a rat kidney is also presented. The synthetic aperture imaging scheme and the setup is presented in the next Section and the results in Section III. A discussion of the results and method along with conclusions are presented in the last Section.

II. Data acquisition and beamforming

A commercial 6 MHz 128×128 elements RC probe from Vermon with a λ pitch is used for the imaging with a Verasonics Vantage 256 system. Synthetic aperture (SA) imaging

is used for acquiring the volumetric data. A number of virtual sources are evenly spread out over the aperture to ensure the minimum possible F-number, and both rows and columns are used alternatively in transmit to ensure the best possible contrast. Signals are received on all elements orthogonal to the transmit elements, so rows are used in receive when transmitting on columns. The virtual sources employ 32 elements in transmit and 96 + 96 transmissions (rows + columns) are made for a complete data set. Edge effects are avoided by having the virtual source aperture start at the edge of the probe - hence 128-32=96 transmissions.

The SA sequence was made using an F-number of -0.7 with a Hanning apodization in transmit. Beamforming was conducted with an F-number of 0.7 in receive, and a Hanning apodization for both transmit and receive using the GPU beamformer presented in [22].

Imaging was conducted on a 3-D printed point spread function (PSF) phantom [23] with scattering cavities in a $6 \times 4 \times 4$ grid with a 2.05 mm spacing in all three directions. The scatterers are 205 μm wide along the $x-y$ axes, but only 80 μm in the z direction.

The RC volumetric images were compared to Field II [24, 25] simulated images obtained from a 256-elements GE L3-12D 6 MHz linear array probe with a geometric elevation focus at 22 mm giving an F-number of 4.4. A 12 emissions SA sequence was used with 32 active elements and an F-number of -0.7. The probe was translated in the elevation direction over the phantom in steps of 0.2 mm obtaining 100 images for the volume.

Finally, the exposed kidney of an anesthetized Sprague-Dawley rat was also scanned in vivo with the RC probe.

III. Results

An example of the PSF and image quality obtainable from a 6 MHz Vermon 128×128 elements RC array is shown in Fig. 1. Top row displays images from measurements on the phantom, and the corresponding Field II simulation is shown in the second row. An isotropic resolution of $(1.05\lambda, 1.10\lambda, 0.62\lambda) = (x, y, z)$ is attained for the measured data, and a similar performance is seen for the simulated data. The data are also compared to the linear array volume scan in the third row. The linear array probe has an elevation resolution determined by the geometric elevation focus F-number of 4.4, and the four rows of point scatterers can therefore not be differentiated due to the fixed elevation focus. The acquisition of the linear array data set necessitated $12 \times 100 = 1200$ emissions and mechanical translation, whereas the RC data set used 192 emissions corresponding to a normal focused linear array image. A volume rate of 62.5 Hz can therefore be attained down to a depth of 6 cm (pulse repetition frequency $f_{prf} = 12$ kHz).

Finally the bottom row in Fig. 1 shows in vivo images of a Sprague-Dawley rat kidney. The dynamic range is 60 dB and an isotropic speckle pattern is seen in all three imaging planes due to SA imaging, a constant F-number throughout the image, and the large size of the RC array.

Fig. 2 shows the attained penetration depth for the probe and sequence when measured on a tissue mimicking phantom with an attenuation of 0.5 dB/[MHz cm]. Twenty different images have been measured and the mean of these subtracted to yield the noise. The penetration depth is defined as the depth when the Signal-to-Noise Ratio (SNR) reaches zero, which is at 550λ at 6 MHz corresponding to 141 mm.

IV. Discussion and Conclusion

Three-dimensional ultrasound is important for capturing all information in a scan. It offers the possibility of acquiring a full volume and then retrospectively inspect the volume as is normally done in radiology for CT, MR, and PET images. Such an imaging system could be devised for the abdomen for scanning the full liver or kidneys. The current resolution offered by matrix arrays is limited due to the small size of the probes because of restrictions in the number of elements. Resolution essentially scales with the squared number of elements, and trying to restrict the large number of elements by employing sparse arrays leads to a limited penetration depth and reduced contrast. A possible solution is to use a translating aperture for 3-D imaging, but it has been shown here that the elevation resolution is quite poor due to the fixed lens of the array yielding a non-isotropic point spread function. Dual stage focusing could be employed in the elevation direction, but this demands a very accurate registration of the probe position down to $\lambda/100$ to get a good resolution and contrast, which is difficult in vivo.

A viable alternative is to use RC arrays, where resolution scales linearly with the number of elements and the penetration depth is quite large. The large probe size makes is possible to maintain a constant F-number over a large range, as was demonstrated for the rat kidney example shown in Fig. 1. The speckle pattern has a constant size in all three orthogonal planes and for all depths, and any slice in the volume will therefore have the same speckle appearance. A matrix array with the same number of active elements would only have 16×16 elements, and the resolution would be 9.7λ at 20 mm for an elements pitch of $\lambda/2$, or 9 times worse than the RC array. Such a small size array would also have a very low penetration depth, whereas the RC array can penetrate down to 550λ, when using spherical emissions with 32 elements for a very low MI and I_{spta}.

Currently, the SA sequence employed for the RC arrays contains 96 + 96 emissions for a high quality result in terms of resolution and contrast. The sequence length should be the subject of further optimization to increase the volume rate from 62 Hz to higher levels. A second challenge is the availability of RC arrays. Only a few arrays exist, and the pitch of the arrays is λ, which is not optimal for SA imaging as it restricts the acceptance angle for the transmitted and received signals. A third limitation is that RC cannot be steered outside the rectangular region below the active aperture. This restricts the available volume, and convex or lensed RC arrays should be developed [26].

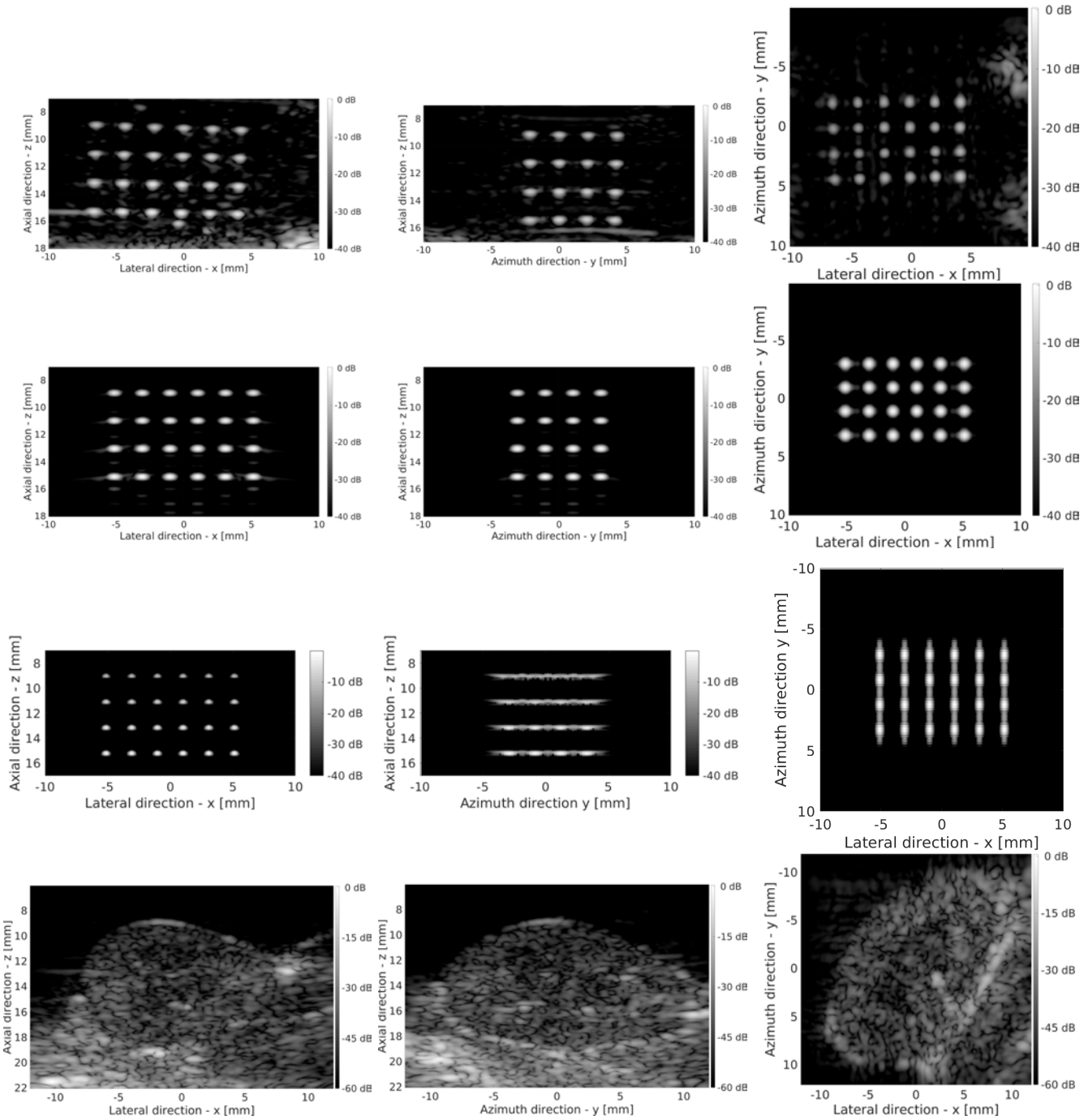

Fig. 1. Point spread functions obtained from a 3-D printed phantom with isolated point targets using a 6 MHz Vermon 128×128 elements row-column array with λ pitch. The top row shows the measured images in the $x-z$, $y-z$ and $y-x$ planes (left to right). The corresponding simulated data from the phantoms is shown in the next row. Simulated data for a linear array probe translated across the phantom is shown in the next row for a GE 6 MHz linear array using a SA sequence. The bottom row shows images of a rat kidney in all three planes obtained using the RC array.

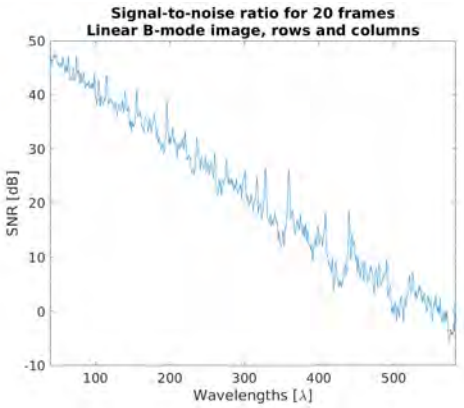

Fig. 2. Penetration depth when the SNR is 0 dB for the Vermon RC probe for a tissue mimicking phantom with an attenuation of 0.5 dB/[MHz cm]. It is 550λ corresponding to 141 mm.

A complete imaging system would also necessitate the estimation of blood velocity, tissue motion and should be applicable for non-linear and super resolution imaging. This has lately been demonstrated in [27], which showed examples of 3-D super resolution volumetric images [28] and full tensor velocity imaging in a volume [29]. RC arrays can, thus, acquire high quality data for both anatomic and functional imaging, and the volumetric data can be studied retrospectively in full 3-D.

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Appendix F

Paper D - Polysilicon on Quartz Substrate for Silicide Based Row-Column CMUTs

Polysilicon on Quartz Substrate for Silicide Based Row-Column CMUTs

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***Abstract*—This paper presents a new type of insulating substrate, polysilicon-on-quartz (POOQ), that can be used for wafer bonded capacitive micromachined ultrasonic transducers (CMUTs). The substrate is based on a quartz handle wafer on which a device layer of polysilicon is deposited. The polysilicon is polished to an average surface roughness below 0.2 nm which allows for wafer bonding. Fusion bonding of such wafers is successfully performed at 950 °C which opens up for new CMUT device designs including the use of silicides for low resistance large scale row-column addressed (RCA) ultrasound transducers.**

I. Introduction

Capacitive micromachined ultrasonic transducers (CMUTs) have been fabricated using several wafer bonding techniques including fusion bonding [1]–[3], anodic bonding [4], [5] and polymeric bonding [6], [7]. Common for all of these techniques is the use of one wafer to define the plate of the CMUT and another where the cavities and the bottom electrodes are defined. These electrodes are normally formed before the bonding step. The wafer defining the plate typically has one thin layer corresponding to the thickness of the plate and a layer that acts as an etch stop when the handle layer is removed. Several wafer structures have been used for this purpose including wafers with a built-in boron doped etch stop layer [8], silicon on insulator (SOI) substrates [1], [2], and more recently a polysilicon-on-insulator (PSOI) wafer [9]. The PSOI structure has a layer of polished polysilicon which is used to form the plate of the CMUT and a layer of thermal oxide that functions as the etch stop during handle wafer removal.

In this article, we present a new member of this wafer family namely the polysilicon-on-quartz (POOQ) substrate. Figure 1 shows an image of a POOQ wafer. As the name implies, this structure is made on a quartz substrate on top of which a layer of polysilicon is deposited and polished. In this case, the polysilicon layer forms both the plate of the CMUT and acts as an etch stop when the quartz handle wafer is removed.

Pushing the limits for higher resolution in ultrasound imaging, transducer arrays are generally becoming increasingly larger, because resolution scales with the number of elements [10], and the the elements are becoming smaller, to meet a $\lambda/2$ pitch requirement to avoid grating lobes [11], as the driving frequency increases. These requirements can provide a challenge for CMUT devices as the use of long elements combined with small pitch increases the resistance of the elements. This can lead to a detrimental effect where the resistance and capacitance of the CMUT elements form a delay line which can lead to uneven pressure emission and phase delays [12]. This effect is especially a problem for long elements such as those used in large scale row-column arrays [12]. To ensure a signal loss of less than 1% along an element, the dimensionless product ωRC should be less than 0.35 [12], where ω is the angular frequency, R is the element resistance, and C the element capacitance. Decreasing the resistance of the elements is clearly advantageous and can be obtained by selecting materials with a low resistivity such as those shown in Table I. Therefore, large row-column addressed (RCA) arrays require low electrode resistivity to transmit a uniform pressure [12] and at the same time a low substrate coupling to avoid element crosstalk [13]. This can be achieved by using anodic bonding [4] where metal electrodes provide low resistivity and the pyrex substrate limits the crosstalk due to the insulating properties. However, the use of pyrex for anodic bonding limits the thermal budget and due to the sodium content in pyrex, many cleanrooms have cross-contamination restrictions that limits the range of processing equipment that can be used during fabrication. Local oxidation of silicon (LOCOS) has also been used for CMUT fabrication [2] and is typically combined with fusion bonding and utilize doping of silicon for the bottom electrodes to achieve a medium to low resistivity, see Table I. This increases the thermal budget and removes the cross-contamination issue, however, the use of a silicon substrate can lead to increased crosstalk between the bottom electrodes [12]. Thus, the use on an insulating substrate is very attractive, and one such substrate is the POOQ wafer. Another advantage is that the alkali-free quartz substrate is less restricted than the pyrex wafer used in anodic bonding in terms of cross-contamination. Hence, a broader range of processes and equipment is accessible with this substrate.

As quartz wafers can be used for higher temperature processing, the POOQ wafer allows the use of techniques such as fusion bonding and silicide formation which could be a way to obtain low resistance bottom electrodes due to the low resistivity of silicides as shown in Table I. The objective of this work is therefore to demonstrate fabrication and fusion

Table I
RESISTIVITY FOR POSSIBLE BOTTOM ELECTRODES: DOPED SI, $TiSi_2$ & AU.

Material	Resistivity [Ωcm]
Highly doped silicon [14]	$\approx 10^{-4}$
Titanium silicide, C49 - $TiSi_2$ [15]	80-100 $\times 10^{-6}$
Titanium silicide, C54 - $TiSi_2$ [15]	13-20 $\times 10^{-6}$
Gold [16]	2.2 $\times 10^{-6}$

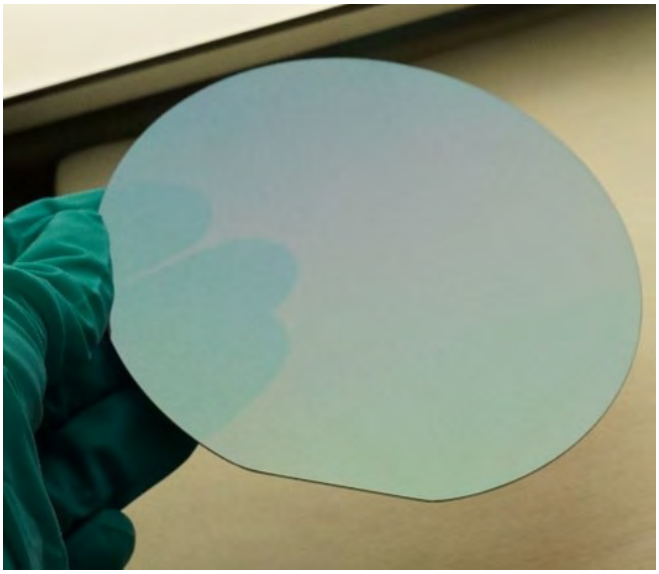

Figure 1. Picture of an oxidized POOQ wafer. Notice that the wafer is semi-transparent.

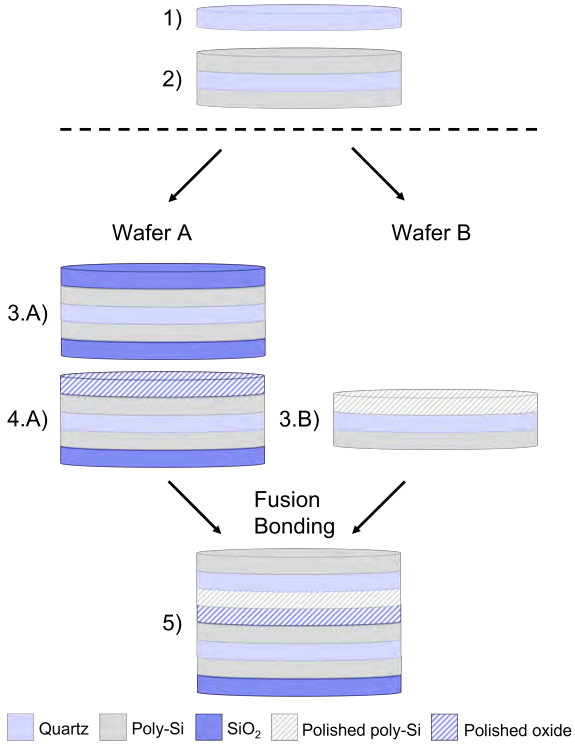

Figure 2. Process flow for fabrication and fusion bonding of POOQ wafers. 1) The quartz wafer, 2) LPCVD of polysilicon. The process is separated into the fabrication of the bottom substrate, Wafer A, and the top plate, Wafer B. The process steps performed on Wafer A are 3.A) thermal oxidation and 4.A) polishing & cleaning of the oxide. For Wafer B, 3.B) shows polishing & cleaning of the polysilicon. Then, 5) Wafer A and B are fusion bonded.

bonding of POOQ wafers to allow for future silicide based RCA arrays.

This paper is organized as follows: The fabrication and fusion bonding of POOQ wafers is described in Section II. Then, future applications of POOQ wafers for CMUT fabrication is discussed in Section III. Finally, Section IV concludes the paper.

II. FABRICATION

This section describes the fabrication and fusion bonding of POOQ wafers. During the fusion bonding step two POOQ wafers, A and B, are bonded together as illustrated in Figure 2. For a CMUT device, Wafer A corresponds to the substrate where the bottom electrodes are formed whereas Wafer B will be used to form the plate and top electrode. During the process, the surface roughness was measured using a Bruker Dimension Icon-Pt atomic force microscope (AFM), and the results are shown in Table II and presented in the text as the average surface roughness, R_a.

A. Wafer A: Oxidized POOQ - Polysilicon-on-quartz wafers

For Wafer A, the process proceeds as follows:

1) The quartz wafer is a Corning HPFS 7980 fused silica substrate, having a surface roughness of less than 1 nm and a wafer bow below 10 µm.

2) Boron doped polysilicon (p^+ Si) was deposited at 620 °C using a Tempress low pressure chemical vapor deposition (LP-CVD) polysilicon horizontal furnace. The polysilicon layer is 2 µm thick and the resulting surface roughness is R_a=22.6 nm.

3.A) A wet thermal oxidation was performed at 950 °C. The thickness of the grown oxide layer was measured by ellipsometry (VASE J.A. Woollam) to be 933 nm. After deposition of polysilicon and oxidation the POOQ wafer is transparent, as seen in Figure 1, and the surface roughness is 23.4 nm.

4.A) To enable fusion bonding, the surface roughness should be below 1 nm [17]. Therefore, the oxide was polished using a Logitech CM62 Orbis chemical mechanical polishing (CMP) machine. The polishing slurry introduces particles and a thorough clean is needed at this point. Wafer A was therefore cleaned for 10 minutes in piranha, then a 20 s buffered hydrofluoric acid (BHF) dip was performed followed by another 10 minutes of piranha clean to remove residual polishing grains. A prolonged BHF dip of 5 min will increase the surface roughness to 1.86 nm, thus the BHF dip is limited to 20 s. After polishing and cleaning the average surface roughness of the oxide is 0.67 nm. The wafer bow was measured with a Dektak XTA stylus profiler to be 5.1 µm, hence a convex wafer bow.

Table II
SURFACE ROUGHNESS AND WAFER BOW DURING POOQ FABRICATION.

Step	Material and process	Surface roughness, R_a [nm]	Wafer bow [µm]
1	Quartz wafer	0.27	< 10
2	Polysilicon	22.6	-
3. A	Oxide	23.4	-
4. A	Polished oxide, 20 s BHF	0.67	5.1
3. B	Polished poly-Si, 5 min BHF	0.16	2.4
-	Oxidized polished polysilicon	1.75	-
-	Polished oxide after 5 min BHF	1.86	-

Polishing of the oxide changes its thickness. In order to preserve the precise thickness control of the thermal oxidation, polishing of the polysilicon prior to oxidation in step 2) was investigated. After polishing and cleaning the surface roughness of the polysilicon was 0.16 nm. Oxidation of the polished polysilicon increased the surface roughness to 1.75 nm, slightly above the conventional rule of thumb for a good fusion bond. Thus, polishing after oxidation is necessary and the oxide thickness has to be increased to compensate for the loss of thickness during polishing.

B. Wafer B: POOQ - Polysilicon-on-quartz wafer

The processflow for Wafer B is identical to Wafer A up until step 3). The polysilicon is polished to a sub-nanometer smoothness of R_a = 0.16 nm in step 3.B). The post CMP cleaning of the polysilicon surface consists of a 10 min piranha treatment, a 5 min BHF dip followed by another 10 min piranha treatment. At this point in the process a convex wafer bow of 2.4 µm was obtained.

C. Fusion bonding

Prior to fusion bonding, step 5), both Wafer A and B were cleaned in an RCA1 solution consisting of H_2O, NH_4OH and H_2O_2 in a (5:1:1) ratio. Afterwards, they were immediately hand bonded under a high-efficiency particulate air (HEPA) filter. The combined wafer stack was then pre-bonded in a Süss SB6 wafer bonder at 50 °C followed by a 950 °C bond anneal in nitrogen for 70 min. Characterization of the bond quality was performed using a reflectance mapping tool (RPM 2000, Nanometrics) and the measured reflectance map is shown in Figure 3. The reflectance map shows a uniform bonding interface without voids, indicating a successful bond.

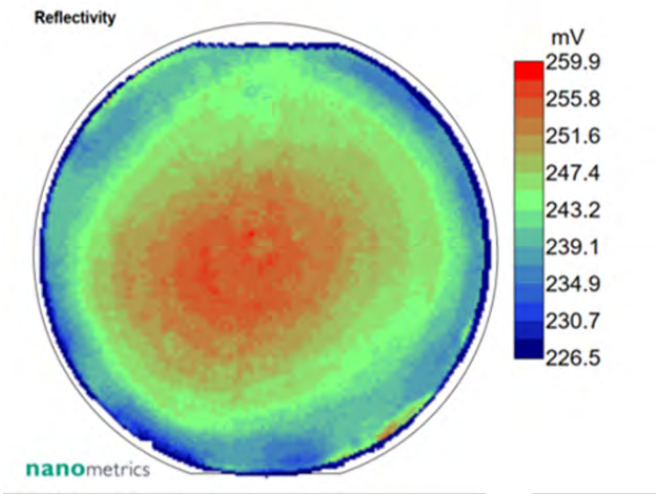

Figure 3. Reflectance map of the fusion bonded POOQ A and B wafers.

III. DISCUSSION

As demonstrated above, POOQ wafers can be thermally oxidized and fusion bonded at temperatures below 1000 °C. This opens up for a range of new CMUT device designs where substrate coupling can be reduced due to the use of an insulating substrate and low resistivity electrodes can be formed using silicides.

In the most simple case, cavities for the CMUT device could be formed in the polished oxide, step 4.A in Figure 2, and the doped polysilicon layer could be used to form the electrodes. As usual, aluminum top electrodes could be formed after the handle layer of Wafer B is removed and the plates of the CMUT cells are exposed. Likewise, contacts to the bottom electrodes could be made using etching to open up contact holes and an aluminum deposition combined with a masked etching step to form the contacts. This process could be used for CMUTs where the dimensions do not violate the ωRC criterion taking the medium resistivity of the doped silicon into account, as discussed in Section I. In a more advanced version of this process, a LOCOS step could be introduced similar to the process described by Park et al. [2]. However, this would require careful process control as the oxide formed during the LOCOS step will need polishing sacrificing the precise gap control, which is one of the key advantages of LOCOS processing.

As the POOQ wafers can be fusion bonded at a temperature of 950 °C, titanium silicide, $TiSi_2$, can be used for the bottom electrodes as this material keeps its low resistivity for process temperatures below 980 °C [15]. The process can be used for both linear and row-column addressed arrays and is illustrated in Figure 4. The process uses two POOQ wafers, WP1 and WP2, that are fusion bonded together. The structures on wafer WP1 are formed using a POOQ wafer where the polysilicon layer is converted into a silicide by depositing a metal layer that is annealed for silicide formation. On top of the silicide, a new layer of highly doped polysilicon is deposited and thermally oxidized. Alternatively, a layer of silicon dioxide based on tetraethoxysilane (TEOS) could be deposited. Then, the oxide layer is polished and cavities are formed in the oxide by etching. The bottom electrodes can then by separated by etching through the different layers until the quartz substrate is reached.

Wafer WP2 is used to define the plate of the CMUTs and is fabricated in the same way as Wafer B as described in Section II. The two wafers are then fusion bonded as shown in Figure 4a). The next step in the process forms the structure shown in Figure 4b). The handle wafer can be thinned down by reactive ion etching (RIE) or wet etching using hydrofluoric

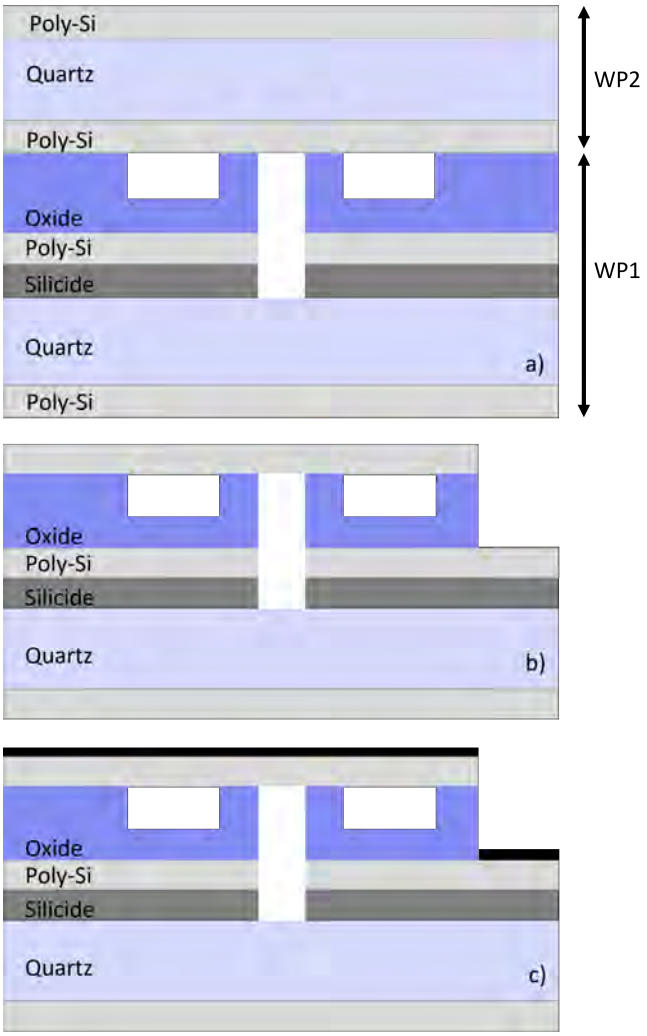

Figure 4. Process flow for future silicide based linear or RCA CMUT arrays enabled by the use of POOQ wafers in combination with fusion bonding. a) Two wafers, WP1 and WP2, are fusion bonded. b) Openings for bottom electrodes are formed. c) Top and bottom electrodes are contacted by a layer of aluminum.

acid (HF) until the polysilicon layer is reached. Dry etching can then be used to access the bottom electrodes. Finally, Figure 4c), the top electrodes and contact pads to the bottom electrodes are defined by depositing aluminum followed by lithography and etching.

IV. Conclusion

In conclusion, we have introduced a new type of insulating substrate, POOQ, that can be used for formation of CMUTs. The substrate is based on a quartz wafer where a deposited and polished layer of polysilicon is used as a device layer with a surface roughness of 0.16 nm. The device layer can be oxidized and polished to obtain a surface roughness of 0.67 nm and has successfully been used for fusion bonding performed at a temperature of 950 °C. This opens for a range of new CMUT device designs where silicides can be used as electrodes.

Acknowledgment

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Appendix G

Paper E - Large Scale High Voltage 192+192 Row-Column Addressed CMUTs Made with Anodic Bonding

Large Scale High Voltage 192+192 Row-Column Addressed CMUTs Made with Anodic Bonding

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***Abstract*—This work presents the fabrication process of anodically bonded 192+192 2D row-column addressed (RCA) capacitive micromachined ultrasonic transducer (CMUT) arrays.**
Four large 2.1 by 2.1 cm^2 arrays with a resonance frequency of 7.5 MHz in water and $\lambda/2$ element pitch at $95\,\mu\mathrm{m}$ are shown successfully fabricated. The arrays exhibit a $100\,\%$ bond yield by anodically bonding an SOI wafer to a borosilicate glass wafer structured with CMUT cavities. A silicon nitride layer has been used at the wafer bonding interface to insulate the top and bottom electrodes for high voltage operation to at least $\pm 200\mathrm{V}$ DC bias. Electrical measurements have been performed on 192+192 RCA arrays and smaller 16+16 RCA arrays. These showed a resonance frequency of approximately $18\,\mathrm{MHz}$ in air at a bias of $-200\,\mathrm{V}$, corresponding to $80\,\%$ of the pull-in voltage and 50 mV AC, with a coupling coefficient of $26.8\,\%$.

I. Introduction

The image quality of medical ultrasound images improves as the number of elements is increased. Unfortunately, having a large number of elements poses a challenge for 3D ultrasound imaging, where the scaling properties of the number of interconnections depend highly on the addressing scheme. By employing a row-column addressing (RCA) scheme [1], the number of interconnections, N, scales as $2N$ compared to N^2 for conventional fully populated matrix (FPM) arrays [2]. The capacitive micromachined ultrasonic transducer (CMUT) technology is in this work used to realize 2D row-column addressed (RCA) arrays, since the technology enables a convenient design flexibility. In addition, the RCA arrays also offer broad bandwidth [3], high coupling coefficient [4], and reduced self-heating [5]. 2D CMUT arrays have already been demonstrated in the literature both for FPM [6] and row-column [7] arrays.

The large area needed for RCA arrays with a high channel count sets strict requirements for the yield and robustness of the fabrication process, which is the focus of this work. Especially the ability to bond the top plate to the bottom substrate without voids or complications due to particles is a critical step.

A large RCA array area does also produce a high transmit pressure, which is needed for deep tissue penetration. The stored electrostatic energy in the CMUT scales with the applied bias voltage squared, hence, more energy can be converted into the mechanical domain as the bias is increased.

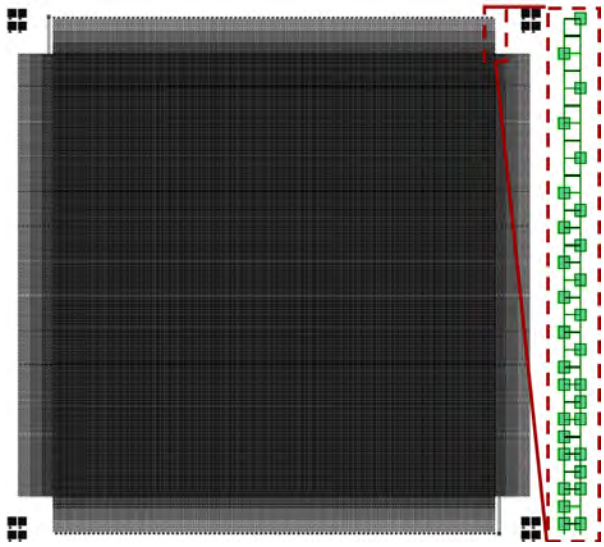

Figure 1. Design overview of the 192+192 row-column CMUT array. The integrated apodization scheme for one element is seen in the inset.

This work presents the development of a high voltage 192+192 element RCA transducer array based on CMUT technology using anodic bonding. This has earlier been demonstrated for a linear array in [8] and later for a 32+32 RCA array [9]. Both of these CMUT arrays were characterized at bias voltage lower than $75\,\mathrm{V}$, whereas the aim of this work is to operate the CMUT at bias voltages up to $200\,\mathrm{V}$. Other techniques have been presented for RCA CMUT fabrication such as sacrificial release cavity formation and polymer based devices [10], [11].

The anodic bonding technique involves the bonding of a silicon-on-insulator (SOI) top plate wafer to a borosilicate glass (Borofloat 33) substrate and gives several advantages during fabrication and for device performance.

The insulating glass lowers substrate coupling between the bottom electrodes (column elements), which gives the same receive sensitivity on rows and columns [12]. Utilizing glass as a substrate makes it possible to define cavities directly by etching instead of using e.g. sacrificial release methods [13] or performing local oxidation of silicon (LOCOS) [14]. The anodic bonding process is less sensitive to particle contamination

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and easily gives strong bonds, which allows us to make large arrays with high yield.

Furthermore, low resistivity metal electrodes are advantageous for large RCA arrays, since the electrode resistance can result in significant attenuation along the elements [15]. A low attenuation along the bottom electrodes and thereby uniform transmit pressure is achieved by lowering the dimensionless product ωRC, where, ω, is angular frequency, R, is the resistance, and C, is the capacitance of an element.

II. Design & Fabrication

A. Design

Fig. 1 shows the design of the CMUT array.

The RCA CMUT arrays presented are designed with 192+192 row and column elements having a $7.5\,\mathrm{MHz}$ center frequency in immersion. The CMUT cells have a square geometry with a side length of $37\,\mu\mathrm{m}$, a $\lambda/2$ element pitch at $95\,\mu\mathrm{m}$ and a plate thickness of $3\,\mu\mathrm{m}$. The design includes an integrated apodization scheme [16] at the edge of the array extended over 15 sub cells to reduce edge wave effects. The whole wafer design, seen in Fig. 2, features four large 192+192 RCAs measuring $2.1 \times 2.1\,\mathrm{cm}^2$ and 76 smaller 16+16 RCA test arrays. The 16+16 arrays feature structures with either shorted top or bottom electrodes for ease of characterization.

To realize the high voltage aspect of the design mentioned above, a silicon nitride layer is incorporated as an intermediate dielectric layer between the plate and glass substrate in two different designs shown on Fig. 3. The first design Fig. 3 a) and b), utilized the nitride membrane as pull-in isolation inside the cells. This gave rise to short circuits in the 400 nm gap between the aluminium top electrode and the chromium leading from the cell to the contact pad due to electrical breakdown in air. This breakdown occurs already below $10\,\mathrm{V}$ bias.

The second design, seen in Fig. 3 c) and d), uses another lithography mask when opening to the bottom electrode. In this design the silicon nitride membrane is instead extended to the bottom electrode contact pad. The silicon nitride membrane covering the Borofloat trench insulates the top and bottom electrodes and allows for high voltage operation up to at least $\pm 200\,\mathrm{V}$ DC bias.

B. Fabrication

The process flow is shown in Fig. 4. The material used as substrate is a borosilicate glass wafer with a thickness of $525\,\mu\mathrm{m}$ (Borofloat 33). First a $50\,\mathrm{nm}$ chromium metal layer is deposited and structured using a photolithographic process and wet etching, thereby forming a mask for etching the cell cavities. A buffered hydrofloric acid (BHF) is used to isotropically etch the CMUT cavities to a depth of $410\,\mathrm{nm}$ and the chromium mask is removed. In the next step a new $230\,\mathrm{nm}$ chromium layer is deposited and wet etched through a photoresist mask to structure the bottom electrode in the cell cavities and interconnecting leads. These steps are illustrated in Fig. 4, steps a) through d), where the cross-section corresponds to the cut-line shown in Fig. 3.

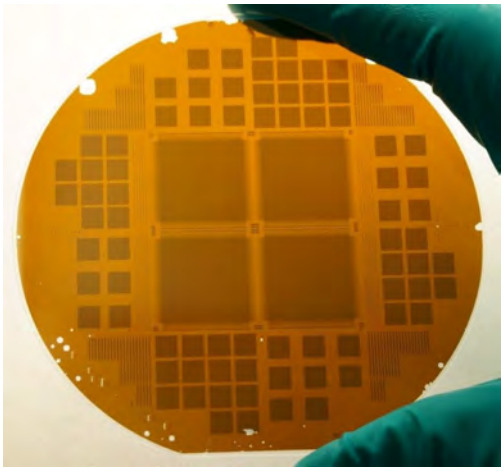

Figure 2. Photograph of the borosilicate glass wafer from step 6 in the fabrication process. The four 192+192 RCAs, the smaller 16+16 RCAs and the linear test elements are shown.

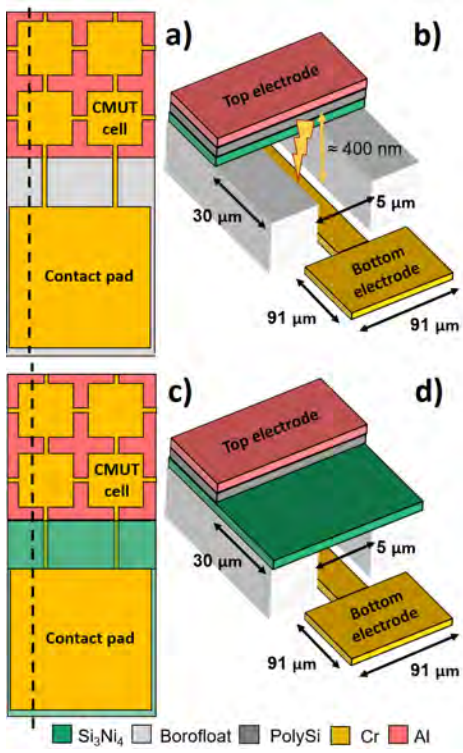

Figure 3. High voltage design overview. First and second design are a) – b) and c) – d), respectively. a) Top down view through the top electrode of the CMUT cells, contact pad and interconnecting leads. The borofloat substrate trench leading to the contact pad is uncovered. b) The same structure near the bottom electrode pad shown in 3D. The 400 nm distance between top and bottom electrodes right at the edge of the top plate leads to an electrical breakdown in air. c) Top down view through the top electrode. The borofloat substrate trench with the chromium leads is here covered by a silicon nitride bridge design. d) The $30\,\mu\mathrm{m}$ long borofloat trench is seen covered by an insulting nitride membrane. The dotted cut-line corresponds to the cross-section presented in the process flow in Fig. 4

A poly-silicon-on-insulator (PSOI) wafer is used [17], as an alternative to the conventional SOI wafer. The thickness of the poly silicon device layer is $3\,\mu\mathrm{m}$. A $200\,\mathrm{nm}$ stoichiometric silicon nitride layer is deposited on the PSOI wafer to obtain protective electrical insulation. The nitride covered PSOI wafer is then subsequently thermally oxidized for three hours at $1100\,^{\circ}\mathrm{C}$ in an H_2O environment to improve the anodic bonding conditions [18].

The PSOI and the glass substrate are then cleaned in an RCA-1 cleaning solution (H_2O, NH_4OH and H_2O_2 (5:1:1)) and a piranha solution (4:1) respectively. They are then anodically bonded in vacuum at an elevated temperature of $375\,^{\circ}\mathrm{C}$ through a four step voltage ramp (200 V/ 400 V/ 600 V/ 800 V) achieving an accumulated charge of approximately 3000 mC, step e).

Due to the transparency of the glass substrate the bond can be inspected for voids before the process is continued, without the need for infrared wafer mapping.

The silicon nitride, poly-silicon, BOX and handle layers are then removed from the backside of the PSOI wafer using dry and wet etching, leaving the $200\,\mathrm{nm}$ silicon nitride and $3\,\mu\mathrm{m}$ poly-silicon plate covering the cavities (step 6). Using a microscope for inspection, this critical etching process step shows a $100\,\%$ bond yield for the four large centre arrays and $98.8\,\%$ yield for the 16+16 arrays, seen in Fig. 2.

A $400\,\mathrm{nm}$ aluminium metal layer is then deposited and patterned by wet etching to create the top electrode contacts. This layer is subsequently used as a dry etching mask for separating the poly-silicon row elements using reactive ion etching (RIE). Finally, a new photoresist mask is made for opening the nitride covering the bottom electrode contact pads using a RIE process. These steps are illustrated in Fig. 4, steps g) through i).

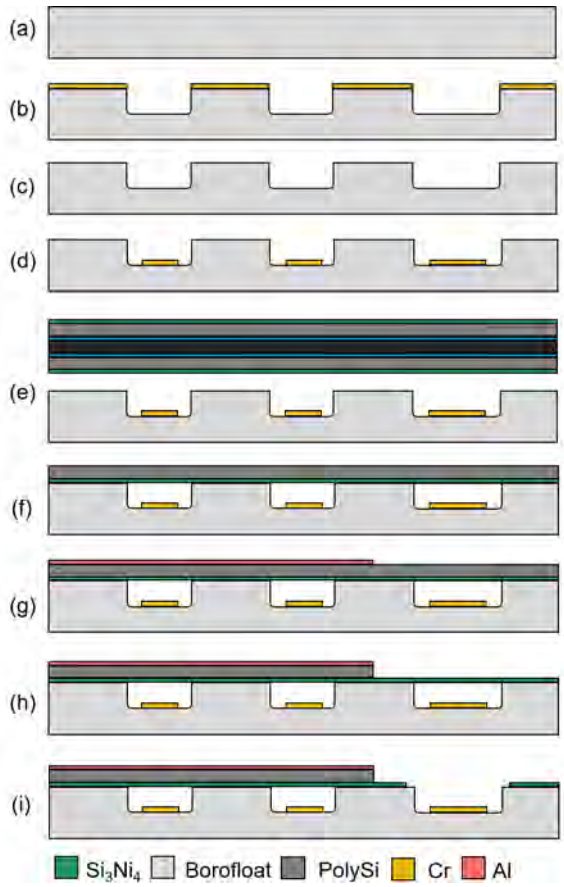

Figure 4. Fabrication process flow for the glass-based row-column CMUT array. The cross-section corresponds to the cut-line in Fig. 3

III. Characterization

A. Electrical

The electrical behavior of the 192+192 CMUT arrays has been characterized in air by performing current-voltage (IV), capacitance-voltage (CV) and impedance (Z-f) measurements pair wise between adjacent rows (top electrodes) of the 192+192 arrays. The 16+16 arrays were also characterized and measured between top and bottom electrodes by shorting either all top or bottom elements [19]. The measurements were made with an automated wafer prober (Cascade Summit 12K probe station), a parameter analyzer (Keysight B1500A Semiconductor Parameter Analyzer), and a dedicated impedance analyzer (Agilent 4294A Precision Impedance Analyzer) with a varying DC voltage and an AC voltage of $50\,\mathrm{mV}$ connected through a bias tee.

The capacitance vs. voltage characteristic, seen in Fig. 5, is shown for a voltage sweep from $-100\,\mathrm{V}$ to $100\,\mathrm{V}$ on a 16+16 array element. The minimum capacitance is measured to be $2.84\,\mathrm{pF}$ at $0\,\mathrm{V}$, and the CV curve exhibits the expected parabolic CMUT behaviour and no noticeable dielectric charging is seen. The impedance magnitude and corresponding -90° phase of a test element has been measured, Fig. 6, for frequencies up to $25\,\mathrm{MHz}$ with an applied DC bias voltage of $-200\,\mathrm{V}$ and $50\,\mathrm{mV}$ AC corresponding to $80\,\%$ of the designed pull-in voltage of $250\,\mathrm{V}$.

Resonance and anti-resonance peaks, f_{res} and f_{ares}, are seen at the frequencies $16.6\,\mathrm{MHz}$ and $19.4\,\mathrm{MHz}$, respectively. The electromechanical coupling coefficient has been estimated using

$$k^2 = (1 - (f_{res}/f_{ares})^2) \times 100\,\% \tag{1}$$

to be $26.8\,\%$.

All elements measured could support a DC bias of at least $\pm 200\,\mathrm{V}$ if the designed silicon nitride bridge was intact after etching. Elements which had their nitride bridge partially fractured in the final fabrication steps still experienced breakdown at lower voltages, i.e. around $150\,\mathrm{V}$ to $180\,\mathrm{V}$ DC.

IV. Conclusion

In this paper the fabrication process and initial electrical characterization of a row-column CMUT array based on a anodically bonded borosilicate glass substrate has been presented. Incorporation of a silicon nitride membrane between the top and bottom electrode has eliminated previously observed breakdown in air near the electrode pads and allowed for high voltage

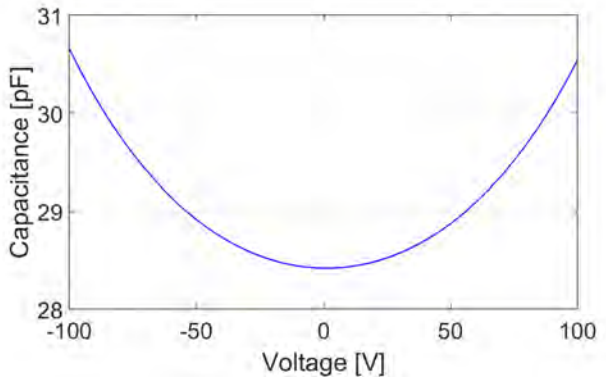

Figure 5. Capacitance vs. voltage (CV) measurement between top and bottom electrode on a an element from a 16+16 row-column CMUT array.

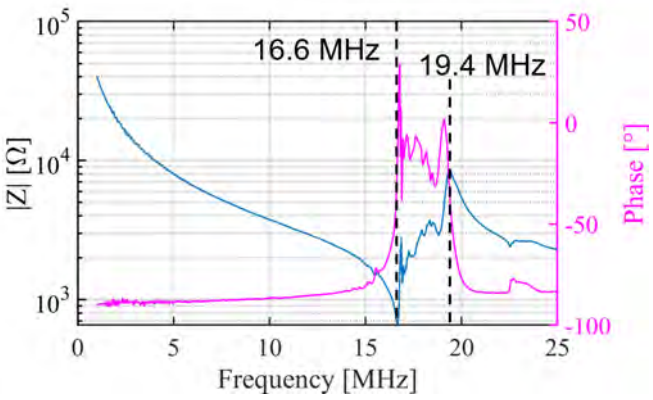

Figure 6. Impedance measurement of a CMUT test element at $-200\,\mathrm{V}$ DC bias and $50\,\mathrm{mV}$ AC. The resonance and anti-resonance peaks are seen at 16.6 MHz and 19.4 MHz, respectively.

operation at a bias of $\pm 200\,\mathrm{V}$. Electrical characterization of the CMUTs has shown the expected parabolic CV behaviour and a resonance frequency at $17\,\mathrm{MHz}$ in air. The fabrication process presented a $100\,\%$ and $98.8\,\%$ bond yield for the 192+192 and 16+16 arrays respectively. This demonstrated that anodic bonding is a viable fabrication platform for the fabrication of large defect free 2D RCA arrays.

The next step will be improving the quality of the silicon nitride etching process and performing a full electrical and acoustical characterization of transmit and receive properties of the RCA arrays.

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