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Heterogeneous integration of single InAs/InP quantum dots with the SOI chip using direct bonding

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Abstract: Quantum information processing with photons in small-footprint and highly integrated silicon-based photonic chips requires incorporating non-classical light sources. In this respect, self-assembled III-V semiconductor quantum dots (QDs) are an attractive solution, however, they must be combined with the silicon platform. Here, by utilizing the large-area direct bonding technique, we demonstrate the hybridization of InP and SOI chips, which allows for coupling single photons to the SOI chip interior, offering cost-effective scalability in setting up a multi-source environment for quantum photonic chips. We fabricate devices consisting of self-assembled InAs QDs embedded in the tapered InP waveguide (WG) positioned over the SOI-defined Si WG. Focusing on devices generating light in the telecom C-band compatible with the low-loss optical fiber networks, we demonstrate the light coupling between InP and SOI platforms by observing photons outcoupled at the InP-made circular Bragg grating outcoupler fabricated at the end of an 80 µm-long Si WG, and at the cleaved edge of the Si WG. Finally, for a device with suppressed multi-photon generation events exhibiting 80 % single photon generation purity, we measure the photon number outcoupled at the cleaved facet of the Si WG. We estimate the directional on-chip photon coupling between the source and the Si WG to 5.1 %.

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1. Introduction

Information processing at the quantum level, based on single photons or electrons, is a fundamental challenge to enable advanced quantum computation. Integrated quantum photonic circuits (IQPCs) offer scalability while operating on multiple flying qubits, simultaneously providing small-footprint devices with unprecedented performance. It can be achieved with complementary metal-oxide-semiconductor (CMOS) technology on large-size silicon-on-insulators (SOI) wafers. Although the SOI platform has already demonstrated scalability and flexibility in integrating and configuring a variety of active and passive photonic devices, including couplers, splitters, combiners, outcouplers, phase shifters and modulators [1,2], its main drawback is the lack of material-compatible light sources emitting non-classical photon. The main reason is silicon's indirect bandgap, preventing efficient light generation, and the significant lattice constant and the thermal expansion coefficient mismatch between Si and III–V materials, which are major

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challenges for monolithic integration [3]. The solution is hybridising the SOI platform with other material system with high-performance non-classical light sources.

Such a hybrid approach is not new, and it is often proposed for the heterogeneous integration of III-V lasers to silicon and realized typically by wafer bonding or transfer printing methods [4–7]. In the context of IQPCs, a remarkable effort is paid to including an isolated quantum emitter acting as a source of triggered single photons [8–10], or to control electron spins in crystal adatoms acting as quantum memories [11–13], which are the main components for the realization of fast and efficient quantum algorithms. For efficient photon guiding through Si waveguides, one should consider the issue of the Si absorption. It limits the usable photons' wavelength of above 1.2 µm. Among various single-photon sources emitting >1.2 µm, one can consider erbium ions [14], defects in 2D $MoTe_2$ [15], carbon nanotubes [16], or semiconductor quantum dots (QDs) [17].

Among others, the self-assembled semiconductor QDs are near-ideal sources of single photon states characterized by the high purity of emission [18–20], and nearly perfect photon indistinguishability [21–23]. Furthermore, QDs benefit from the broad wavelength tunability due to bandgap variation and size effect, as well as the capability of generation maximally entangled photon pairs with high fidelity using the biexciton–exciton radiative cascade [24–27]. Such photon pairs have the ideal two-photon quantum state for advanced schemes of quantum information processing [28–32]. Moreover, unlike highly attenuated lasers [33,34], parametric down-conversion [35] or four-wave mixing in nonlinear medium [36] widely used for quantum information processing, QDs can generate non-classical states deterministically [17].

The application potential of III-V QDs for on-chip photonics was revealed by several recent demonstrations also on its hybrid integration with silicon nitride (Si_3N_4) platform, which includes highly efficient optical interface between heterogeneously integrated Si_3N_4 waveguides (WGs) and GaAs-based QDs [37,38]. Another interesting example is a single QD in a nanowire transferred by a nanomanipulator and integrated with the Si_3N_4-based photonic circuit [39]. Next, epitaxially grown InP-based QDs emitting in the O-band telecom window (1.3 µm wavelength) were positioned deterministically on a silicon photonic chip with nanoscale precision by a pick-and-place approach [40], as well as an InAsP QD emitting around 0.9 µm was integrated in a CMOS compatible SiN photonic circuit with reconfigurable on-chip single-photon filtering and wavelength division multiplexing [41]. However, demonstrations with the heterogeneous integration of III-V QD-based single photon source with the SOI platform are very limited [42].

In this work, we present the fabrication and characterization of an optically-triggered on chip single-photon source made of an InAs/InP QD embedded in the InP nanobeam WG heterogeneously integrated with the Si WG on an SOI chip. The Si WG ends with an outcoupler based on half of the circular Bragg grating (CBG), allowing the outcoupling of photons to an off-chip environment. Therefore, the device comprises three essential elements of a IQPC: the SPS, the low-loss photons guiding medium, and the outcoupler. To hybridize the InP nanobeam with the SOI chip, we successfully developed the technological process involving QDs growth, photo- and electron-beam-lithography, dry and wet etching, and InP to SOI direct wafer bonding. Importantly, we utilise the advantage of InAs/InP QDs naturally emitting photons at a technologically-important telecom C-band, providing extremely low losses in Si WGs as well as in silica fibers. We characterize the device optically to demonstrate the effective transfer of photons generated by the biexciton-exciton cascade in the QD to the Si WG. We measure the single photon purity of the source, by outcoupling photons off the chip, and the photon coupling efficiency between the source and the Si WG. The latter is compared to the results of calculations based on the finite-difference time-domain (FDTD) simulations. Our results pave the way for a new generation of quantum devices combining optically active heterogeneously integrated InP/Si waveguides containing a single InAs/InP QD and a passive circuit realized on the Si platform with additional elements like ring resonators, directional couplers for efficient on-chip routing of

light quanta, single photon detectors [43] or grating-based outcouplers for interconnection with external fiber network.

2. Device structure

The investigated device contains three important elements of a IQPC embedded in the SOI platform: (i) the SPS, (ii) the low-loss photon guiding medium, and (ii) the photons outcoupler off the chip. Figure 1 presents the conceptual scheme of an exemplary IQPC designed to deliver processed signals off the chip to free space or to silica fibres network operating in the telecom C-band. Within the scheme, the SPS must be positioned accurately over the Si WG to enable efficient coupling of emitted photons into on-chip photonic circuits. Subsequently, photons are guided by the low-loss Si WGs and redistributed over various on-chip passive and active elements, allowing for signal processing on a single photon level. Finally, the processed states are transfered off the chip by light scattering on the outcoupler, read out by off-chip photon detectors, or transmitted through the silica fibres over the quantum network.

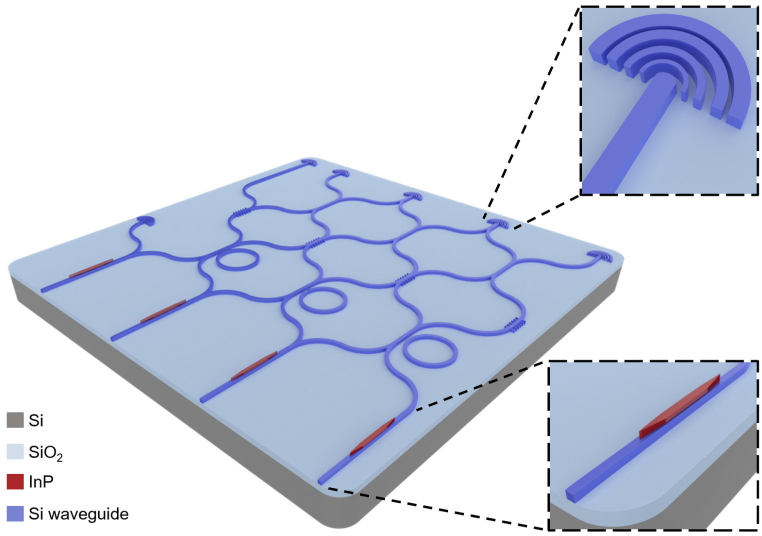

Fig. 1. Conceptual illustration of the integrated quantum photonic circuit (IQPC) with heterogeneously integrated QD emitter. The bottom layer (gray) is silicon substrate, the center layer (light blue) is silica, and the top layer consists of patterned silicon waveguides (blue) and InP (red) with InAs QDs. Enlarged images demonstrate a single photon source and outcoupler regions, while in between a circuit based on silicon waveguides presents a possible realization of information processing based on phase shifters, ring resonators and directional couplers.

The essential step of the proposed device fabrication technology is wafer bonding of the InP and SOI platforms. The technology facilitates the light transfer from the InP to the Si waveguide and is a reliable solution for the cost-effective fabrication of IQPCs on a large scale. We have outlined the technological steps in Fig. 2. The process starts with the growth of low-density Stranski-Krastanov InAs/InP QDs using metal-organic vapour phase epitaxy (MOVPE) [44] (Fig. 2(a)). The randomly distributed QDs are placed in the middle of a 580-nm-thick InP slab, which serves as a platform for defining InP WGs. In this case there is no control of QD position in the plane with respect to the WG axis. An InGaAs etch stop layer separates the slab from the InP substrate. Concurrently, Si WGs and alignment marks (AMs) are patterned using ultra-violet (UV) optical lithography in a positive-tone photoresist on top of the 220-nm-thick Si layer of a

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standard SOI chip (Fig. 2(b)). The Si WGs are defined by two 10 µm-wide openings which also act as efficient vertical out-gassing channels to facilitate high area bonding [45]. The pattern is transferred using inductively coupled plasma advanced oxide etch (ICP - AOE) to the Si layer (Fig. 2(c)). Then, an oxygen plasma treatment of the flipped InP chip and Si surfaces is used to increase the density of hydroxyl groups, which are responsible for establishing bonds at the interface [46,47]. Direct contact between surfaces is established immediately after the low-power plasma ashing by high force (∼ 2 kN) and temperature (250 °C) in vacuum conditions in the bonder. This effectively creates stable contact between InP and Si without any intermediate layer (Fig. 2(d)), as evidenced by a typically high bonding yield of more than 70 %, evaluated for a quarter of a 2-inch InP wafer.

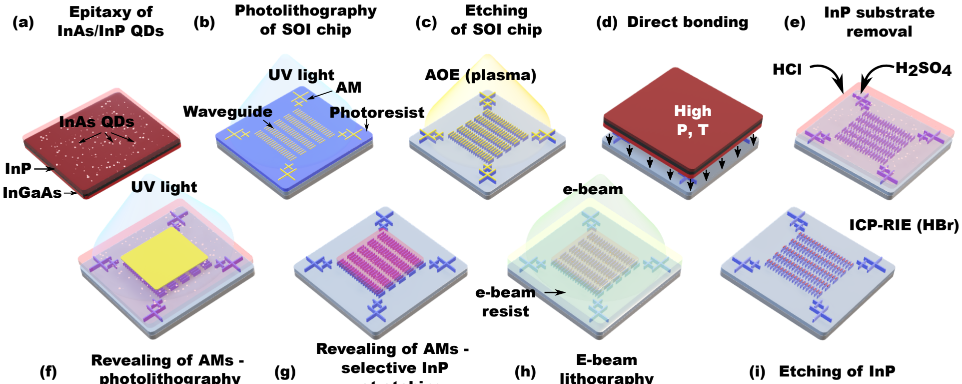

Fig. 2. Fabrication workflow of the hybrid InP/Si waveguides based on the scalable molecular wafer bonding technique. (a) Epitaxy of low-density InAs/InP QDs. (b) Patterning of Si waveguides and alignment marks (AM) in UV lithography. (c) Pattern transfer to Si. (d) Direct bonding of the SOI and InP wafers. (e) Substrate removal in wet etching. (f-g) Additional UV lithography and wet etching steps to reveal AMs in SOI, (h) E-beam lithography of the InP tapers (i) pattern transfer to InP using ICP-RIE dry etching and subsequent cleaving of the wafer perpendicularly through the Si waveguides.

The InP substrate and etch stop layers are removed using HCl and H_2SO_4 :H_2O_2, respectively (Fig. 2(e)). In order to achieve high-accuracy positioning of InP nanobeam WGs on top of the Si WGs during an e-beam lithography step, additional processing steps are introduced. First, the AMs defined in SOI are revealed. Openings in InP are defined using UV lithography (Fig. 2(f)) and then transferred by HCl etching (Fig. 2(g)). E-beam lithography using hydrogen silsesquioxane (HSQ) negative tone resist with high accuracy alignment (approx. 40 nm) [48] is used to define the InP nanobeam WGs and outcouplers positioned on top of the Si waveguides (Fig. 2(h)). This pattern is transferred to InP using HBr plasma in ICP-reactive ion etching (RIE) and the HSQ mask is removed in buffered hydrogen fluoride (BHF) (Fig. 2(i)). To see the progress of the fabrication documented with photos see Supplement 1 Section 2.

Within this approach, we realized a series of hybrid InP/Si WG structures with different geometrical parameters based on the optimized heterogeneously integrated InP-Si on-chip system [49], enabling broadband on-chip directional light coupling from the QD to the Si WG of approx. 33 % efficiency in the spectral range of 1.5-1.6 µm. The assumed geometry of crucial elements in the IQPC design is a 0.58 µm-high InP WG on top of a 0.22 µm-high Si WG. The InP(Si) WG width is set to 1.5(2.0) µm, 1.5(3.0) µm, 2.0(3.0) µm, 1.5(4.0) µm, 1.5(5.0) µm, and 3.0(5.0) µm. The straight hybrid WG section is 100 µm long, and we restrict the geometry of the InP WG taper to 25 µm length and finite tip width down to 0.25 µm. The outcoupler is realized with half of the CBG consisting of InP rings on top of a planar Si section (alternatively, a similar system could

be realized directly in Si, requiring additional e-beam lithography step). The grating geometry contains 5 periods in which the ring width is 0.7 µm, and the grating period is 1.2 µm.

The fabricated hybrid WG geometry is verified by scanning electron microscopy (SEM) analyses. Exemplary micrographs for the on-chip microstructures are demonstrated in Fig. 3. In Fig. 3(a), we present a single device which contains the hybrid WG section, the Si WG section and half of the CBG outcoupler on the right-hand side. On the left-hand side, the structure ends with a cleaved facet. The CBG outcoupler and the InP WG taper structure are depicted in more detail in Fig. 3(b), c and d, respectively. The images show high quality of the realized device and high accuracy of the integrated InP WG on Si WG with an estimated positioning error of less than 100 nm. However, we observed that the final geometry of the device differs slightly from the design, namely, the InP WG width is smaller by approx. 50 nm, while the Si WG width is smaller by approx. 150 nm (difference due to distinct dry etchings), both evaluated by a median value.

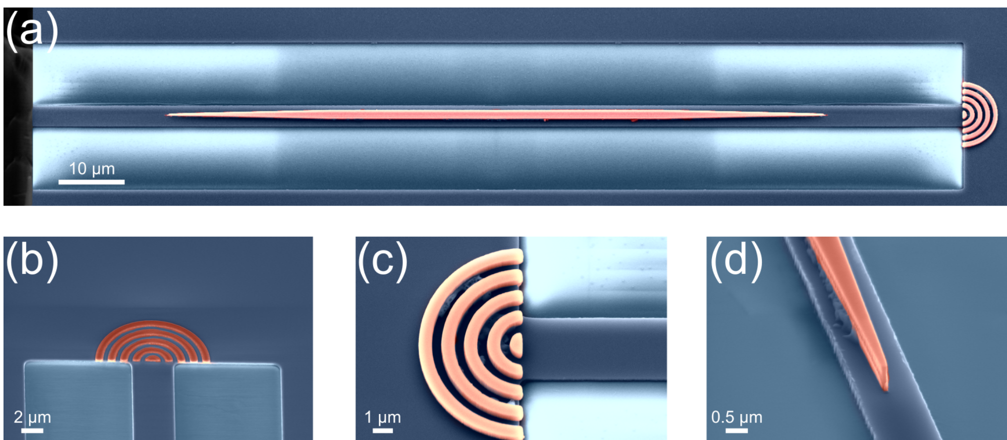

Fig. 3. (a) Scanning electron micrographs of the hybrid InP/Si waveguide structure containing a self-assembled InAs/InP QD emitter, (b) and (c) circular Bragg grating (CBG)-based outcoupler, (d) linear taper of the InP WG atop of the Si WG.

3. FDTD simulations

The fabricated series of structures described in the previous section were realized for the geometries according to our prior numerical studies, which were performed via a FDTD solver [49]. We found that the multimode operation of a hybrid waveguide is inevitable due to refractive indices contrast ($n_{Si} > n_{InP}$) in the target spectral range. It leads to a more efficient dipole coupling with the propagating modes on the order of 30 % with the minimum width of the InP WG of 1.2 µm. We also found that a taper length in the range of 15-25 µm provides optimum transfer efficiency from an InP/Si WG to a Si WG, and a taper tip must be of finite width, e.g. 0.25 µm.

The 3D FDTD calculations were based on the exact geometry of the device presented in Fig. 3. We use the same numerical procedure as in Ref. [49]. The model structure consists of a straight hybrid WG system defined by its cross-section with InP WG height of 0.58 µm, Si WG height of 0.22 µm and for all structures, InP(Si) WG widths are now corrected according to the analysis performed on SEM micrographs which reads 1.45(1.85) µm, 1.45(2.85) µm, 1.95(2.85) µm, 1.45(3.85) µm, 1.45(4.85) µm, 2.95(4.85) µm.

In the first part, we focus on modelling the dipole emission coupling into the hybrid InP/Si WG. The dipole is placed in the middle of the InP WG, in-plane linearly polarized perpendicular to the WG axis, and mimics the InAs QD embedded in InP. The linear polarization selected in this way allows to assess the coupling efficiency for any of the excitonic states when examined with

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no polarization filtering, as the excitonic states consists of two orthogonally polarized states, i.e. horizontal/vertical for neutral case or left/right circular for charged case, so the projection of both components onto the TE-like modes adds to the overall coupling which gives the same result regardless of the orientation of the QD with respect to the WG axis. The coupling coefficient (η) is calculated as an overlap between the propagating transverse electric (TE) modes and dipole emission over a distance of 30 µm along the WG to ensure convergence, see Supplement 1 for details – Sec. 3. The directional dipole coupling coefficient $\left(\frac{\eta}{2}\right)$ is around 30-40%, as shown in Fig. S1.

Next, we study the same geometries with a taper structure along a InP WG to evaluate the QD emission transfer efficiency between InP/Si WG and Si WG. Here, a straight waveguide region is 4 µm-long and follows a 25 µm-long taper ending with a 0.25 µm-wide tip (see Fig. 4(a)). First, in Fig. 4(b) - panel (i), we demonstrate the cross-sectional $|E|^2$ field distribution of the dipole emission, which indicates an efficient transfer from the hybrid InP/Si WG to Si WG via the taper structure, which allows for the evaluation of the on-chip directional coupling to the Si WG $\left(\beta = \frac{\eta}{2} \times \chi\right)$, where $\chi \sim$ 60-80% is taper transmission [49]. Second, in Fig. 4(b) - panel (ii), we show $|E|^2$ for the Si WG approaching the cleaved facet, where we used the Si WG structure only to simulate multimode light propagation towards the cleaved facet. Last, in Fig. 4(b) - panel (iii), we demonstrate the evaluation of a far-field distribution of light scattered on the sample edge, which gives insight into the angular distribution of the outcoupled field that might be collected by the microscope objective focused on the waveguide end (it corresponds to the results collected in our experimental configuration, in which we excite from top of the structure and detect from its sidewall). We found that by limiting the collection angle to 45 degrees (provided in the experiment by the 0.65 numerical aperture microscope objective), the evaluated far-field collection efficiency of 89 % can be reached. However, our simulations show (Fig. 4(c) - black data points) that the edge outcoupling (ϕ) is on the level of 55-60% while the losses are related to the $\sim$ 30% reflection of the guided light beam on the interface. The demonstrated evaluation shows that our device allows for the in-plane collection efficiency ($\kappa = \beta \times \phi$) of the directional emission (including losses) on the level of 10-15% (Fig. 4(c) - red data points), depending on the geometry. Notably, this value could be compared to the experimental count rate and used to evaluate the efficiency of the on-chip coupling of the QD emission for the fabricated structures.

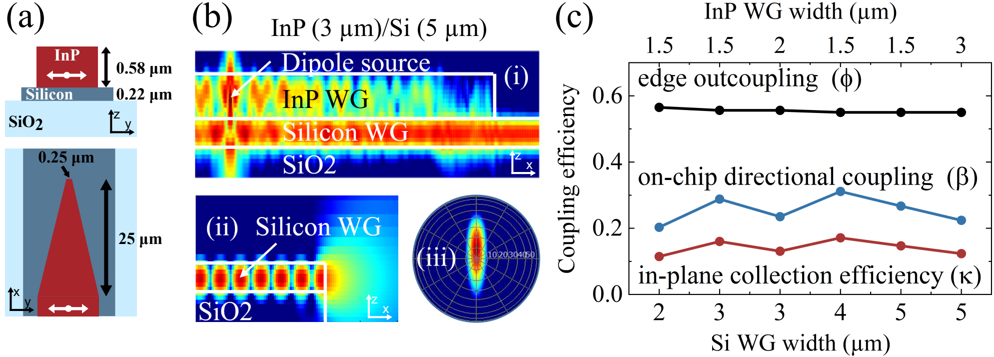

Fig. 4. a) Schematic model of the hybrid InP/Si waveguide structure on SiO_2 used in FDTD simulations, b) Electric field intensity distribution in a selected InP/Si WG structure used for evaluation of (i) on-chip dipole coupling, (ii) edge outcoupling to the far-field used in micro-photoluminescence (µPL) experiment. c) Edge outcoupling - ϕ, on-chip directional dipole coupling - β and the in-plane collection efficiency - κ for all fabricated geometries (with lines as a guide to the eye).

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4. Optical experiments

The optical experiments allow us to validate proposed technological processes and prove the coupling between the QD-based single photon emitter and the SOI platform in our device. Since the QDs density is low, the averaged dot-to-dot separation is 0.42 µm, translated on the low-fabrication fidelity defined by the number of devices with a QD. The fabrication fidelity can be increased by using the deterministic fabrication of an InP WG over a localized QD emitter. However, this issue is not addressed in the article. To determine fabrication fidelity, we performed a high-spatially resolved photoluminescence (µPL) experiment in which we tested roughly 50 neighbouring devices to find spectral features related to the presence of a QD in the InP/Si WG. Moreover, we focused on the QDs emitting in the telecom C-band near 1550 nm to hold compatibility with the low-loss silica fiber transmission window. We found that 4 % of the devices fulfil these requirements. Subsequently, we focused on a single device to examine a QD emission pattern and the QD single photon emission purity and demonstrate the coupling of photons from the InP/Si WG to the Si WG in the SOI platform.

Figure 5(a) shows the low-temperature ($T = 5$ K) µPL spectrum from a selected device consisting of a hybrid InP/Si WG system of InP(Si) WG widths of 2.95(4.85) µm. The spectrum is registered at different excitation power densities (P) at the straight section of the hybrid WG and unveils inhomogeneously broadened emission lines within the 1528-1553 nm spectral range. The linewidth of 1537 nm line is (197 ± 40) µeV which is less than 340 µeV as measured from similar QDs of unprocessed sample [50]. The improvement of the linewidth might be attributed to reduced charge fluctuations in the vicinity of the QD influencing spectral diffusion, as the less excitation power density is used in case of the structured system. Also we did not observed any QD blinking. Based on the previous studies on InAs/InP QDs [51–53] and analysis of the intensity dependence between the lines, the spectral features are attributed to recombination of the neutral exciton (X), biexciton (XX) and negatively-charged exciton (X^-) complexes confined to a single InAs QD placed in the InP WG. In this case, the µPL experiment configuration utilises the same excitation and detection path parallel to the WG surface (normal direction). Importantly, except for the previously mentioned case, the µPL response did not reveal any additional spectral lines in the C-band upon scanning the excitation spot along the WG. This indicates no other optically active QDs emitting in the required spectral range within the device.

To demonstrate the coupling of photons from the QD to the SOI platform, we compared the QD spectra obtained under the already introduced normal µPL excitation-detection scheme with the spectra recorded with two new experimental configurations, where the excitation path is spatially separated from the detection one. In both new schemes, the excitation is realized normal to the InP WG, however, the detection is either provided through the outcoupler or the cleaved facet of the chip, as presented in Fig. 5(c). This is feasible by applying another microscope objective in the detection path, gathering photons from the outcoupler in the normal direction and the cleaved facet of the Si WG in the in-plane direction of the chip.

Figure 5(b) displays the results of the µPL experiment for different detection paths. It shows the same qualitative picture of the X and XX emission lines from the InAs QD in the selected device. The X and XX photons registered at the cleaved facet of the chip may have a component directly related to the anisotropic QD emission collected by a microscope objective oriented in-plain of the structure, which makes the coupling between a QD and the Si WG questionable. However, observing out-scattered photons from the Si WG on the grating outcoupler provides solid proof for the coupling. In this case, the QD-emitted photons must travel roughly 80 µm distance separating InP WG and the CBG to be scattered and collected in the normal direction.

Analysis of the emission line intensity presented in Fig. 5(b) can shed light on the coupling efficiency and be qualitatively compared with the FDTD model predictions. The model shows that, for a dipole source placed in the InP WG, photon extraction efficiency towards the normal direction and within the 0.4 numerical aperture (NA) amounts to 7 %. It is nearly twice less than

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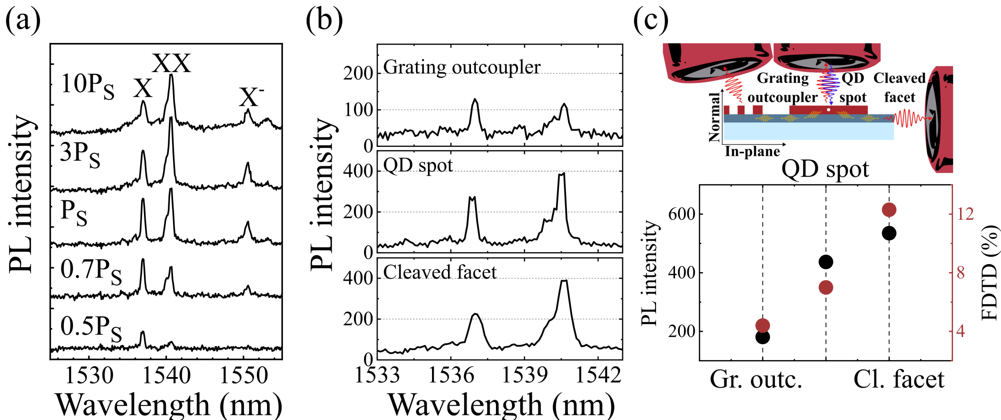

Fig. 5. (a) μPL spectra at $T = 5$ K collected under continuous wave excitation versus excitation power on a single quantum dot (QD) integrated into a hybrid InP/Si waveguide structure. The neutral exciton (X), biexciton (XX), and negatively charged exciton (X^-) lines are observed at $P_S = 7$ μW. (b) QD emission is collected in three different setup configurations, showing qualitatively the same response with clear separation of the excitation and detection path using either the CBG-based outcoupler or cleaved facet of the chip. c) Qualitative comparison of PL intensity collected from the grating outcoupler, right at the QD position and cleaved facet (in-plane direction) with evaluated efficiencies via the FDTD method.

for the in-plane of the chip. In this case, the photon extraction efficiency is the highest, reaching 12.3 %, and results from the multiplication of the evaluated edge outcoupling ϕ =55 % (Fig. 4(c)) and the on-chip directional coupling β = 22.4 % [49]. The lowest expected photon extraction efficiency is delivered by the grating outcoupler and reaches 4.4 %. The value results again from the on-chip directional coupling β = 22.4 % from the dipole source to the hybrid WG, multiplied with the outcoupling efficiency along sample normal direction within the 0.4 numerical aperture of approx. 20 % [49] .

The numerically evaluated extraction efficiencies for each detection channel are summarized in Fig. 5(c), in which we additionally plot the integrated intensities of μPL lines from Fig. 5(b). Both data sets follow the same trends, demonstrating good qualitative agreement, thus confirming extraction efficiency gradation for different detection schemes.

To estimate coupling efficiency quantitatively, a standard continuous-wave μPL is complemented with the pulse excitation experiment, allowing for accurate counting of emitted photons with a single-photon detector (see Supplement 1). Experimentally, the in-plane collection efficiency can be found using the following expression $\kappa = \left(N_{phot}\right)/\left(L_{rep} \times \gamma\right)$, where N_{phot} is the number of collected photons per second (detector counts), L_{rep} is the laser pulse repetition frequency, which equals to 76 MHz, and γ is the the photon collection efficiency of the setup. Here, the counted photons were outcoupled from the cleaved facet of the chip after being transmitted through the Si WG and collected by the microscope objective with NA = 0.65. The evaluated γ parameter amounts to 0.115 %, as shown in the Supp. Inf (see section 5). For that experiment, another QD-containing device is selected, characterized by the μPL spectrum settled in the telecom C-band as displayed in Fig. 6(a). The spectrum consists of three inhomogeneously broadened lines assigned to neutral exciton (X), positively-charged exciton (X^+) and biexciton emission from the same QD. The assignment is suggested by the expected charged-exciton and biexciton binding energy for InAs/InP QD [50,52,53] and the power-dependent μPL experiment with results presented in Fig. 6(b). From Fig. 6(b), one can see that X and X^+ emission follow

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a linear dependence of the line intensity (I) with the excitation power (P): $I \propto P^1$, whereas for the XX emission, this tendency is close to superlinear: $I \propto P^2$, as expected for the XX-X cascade emission process in a QD [50,52,54]. Figure 6(c) shows the μPL spectrum for the investigated device recorded for the pulsed excitation condition. It allows to establish the count rates above the background level for the X and X^+ emission lines, which are N_{phot}=1.0 kHz and 1.4 kHz, respectively. Subsequently, it provides the κ = 2.8 %. We note here that there can be several factors which lead to underestimating outcoupling efficiency theoretically assessed to 12.3 % (Fig. 4(c)). Among these factors there are technological ones: (i) misalignment of the QD with respect to the InP WG axis [49], as the fabrication was not realized in a deterministic manner, which may result in less QD emission coupling to propagating modes in the WG; (ii) misalignment between the InP WG and the Si WG, which leads to inefficient on-chip coupling, i.e. transfer of emitted photons from the InP/Si hybrid section to Si WG; (iii) irregularities along both InP and Si WGs sections, inaccurate taper sharpening in the vicinity of the taper tip or roughness at the sample edge due to cleaving; (iv) lower than expected photon collection efficiency from the cleaved facet (FDTD gives 89 %); and (v) possible non-radiative recombination in the QD which implies reduced internal quantum efficiency [55–57].

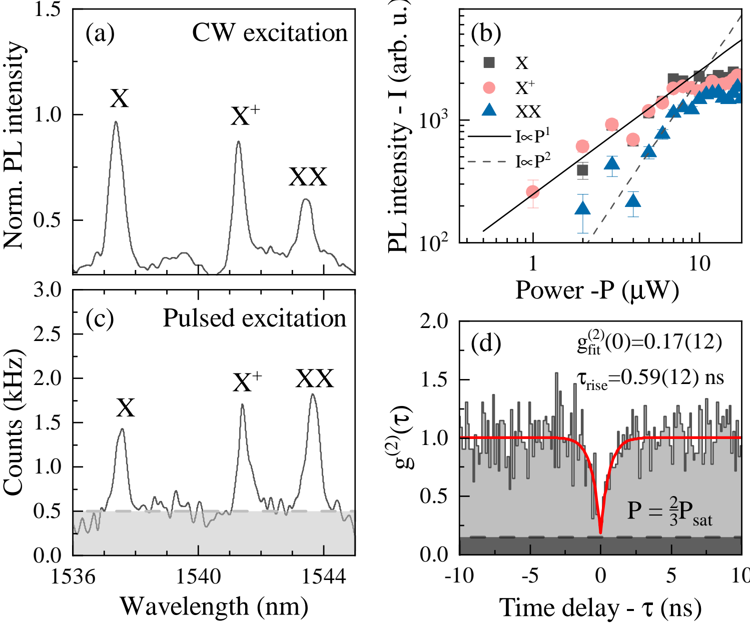

Fig. 6. (a) μPL spectrum of QD emission collected from a cleaved facet of a device at T = 5 K using continuous wave (CW) excitation, revealing neutral exciton (X), positively-charged exciton (X^+), and biexciton (XX) lines. (b) CW excitation power-dependent intensity evolution for the QD emission lines. The solid (dashed) black line shows the linear (superlinear) trend expected for X and X^+ (XX) emission from a QD. (c) QD emission under pulsed excitation with the count rate for each QD line. The dashed gray line indicates the dark counts' background at 0.5 kHz. (d) Auto-correlation histogram of the QD natural exciton emission measured under CW excitation and from the cleaved edge of the device. P_{sat} = 7 μW. The solid red line is a fit to experimental data. The dashed line represents the contribution level of the background emission with energy equal to that of the observed transition.

In this situation, we can estimate the on-chip directional coupling that reaches up to 5.1 % ($\beta = \kappa / \phi$). However, if the examined QD-WG system is far from optimized, especially considering

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losses related to before-mentioned factors, i.e. (i) in-plane misalignment of the QD and (ii) misalignement of the InP WG on the Si WG, which could reduce β by roughly 20 % [49], we could state that further optimization is possible and can lead to more efficient transfer to the Si WG. Noteworthy, since we observe the QD emission from the CBG-based outcoupler, the estimated coupling is only half of the bidirectional emission (η) coupled to the Si WG. Therefore, we should note that using an appropriately designed reflector (e.g. the Bragg grating) on one side of the WG, providing reflectivity close to 99 % [58,59], one can assure directional on-chip coupling β to a Si WG of approximately 10 %. Last, in the experiment we do not select any polarization. As the excitonic states consists of two orthogonally polarized states (X, XX - linear horizontal/vertical, CX - circular left/right) and typically have negligible polarization anisotropy for non-resonant optical excitation, the evaluation of β comprises half of the QD emission. In other words, since X consists of two linearly polarized states, e.g. along and perpendicular to the WG axis, only one of them is effectively coupled to the TE modes. For arbitrary dipole orientation both states projected to TE polarization couple and still 50% of total X emission is coupled. Therefore, if one could excite just one X state via quasi-resonant or strict resonant excitation with polarization matching to TE modes, the β could be doubled.

Finally, we investigate the quantum nature of the on-chip coupled QD emission in a selected device by performing second-order auto-correlation measurements in the Hanbury-Brown and Twiss (HBT) configuration. The QD emission is collected from the cleaved facet of the device, while the CW laser excitation is provided from the top at the QD position. We focus on the neutral exciton emission, presented in Fig. 6(a).

The measurement conditions maximize the signal-to-background ratio and allow for registering the histogram counts, exhibiting a clear antibunching behaviour presented in Fig. 6(d). The fitting procedure results in the second-order correlation function at zero time delay of $g^{(2)}_{fit}(0) = (0.17 \pm 12)$, proving a single photon emission of the source. The non-zero value of antibunching dip should in general be take into account in the evaluation of the on-chip coupling. Then the corrected β value would be 4.2%. However, The histogram shows the normalized measured values without background subtraction. Multiphoton events present at τ=0 are predominantly related to background contribution (see the analysis in Supplement 1 Section 3B) and a corrected antibunching dip reveals the purity of emission of the level of 98%. Similarly, the background counts (marked with a dashed line in Fig. 6(c)) are also excluded for the evaluation of exctraction efficiency. In this sense, we could state that the correction due to non-zero antibunching dip observed in the evaluation of on-chip directional coupling is not required. The observed value of $\tau_{rise} = (0.59 \pm 12)$ ns reflects relatively high effective pump rate (laser excitation power) [60] and is in accordance with previous results for these QDs [50]. In addition, we observe no bunching for the time delays close to ±1 ns, which indicates a low probability of re-excitation of the QD due to carrier recapturing processes in the QD occurring right after the excitonic recombination of carriers trapped by the surrounding traps [61,62].

5. Summary and conclusions

The InAs/InP quantum dots are perceived as quantum emitters, able to deliver single photons in the telecom C-band spectral range for quantum information processing. In this work, we show the method for successful heterogeneous integration of these single photon emitters with the SOI platform - one of the most interesting for the highly integrated quantum photonic chips. The proposed integration scheme utilizes a wafer-scale direct bonding of III-V optically active materials with a pre-patterned SOI platform, followed by the fabrication of nanobeam waveguides supporting light transfer from an InAs/InP QD to the Si waveguide. This technology is not limited only to SOI and can be applied with e.g. SiN-SOI, which allows for fast and reliable engineering of quantum photonic chips, providing a step to scalable technology comprising

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multiple non-classical light sources based on InAs/InP QDs and various passive and active elements fabricated on the SOI or other platforms.

The performed 3D FDTD numerical calculations allowed setting up a single device geometry comprised of a single InAs QD embedded in the InP tapered waveguide on top of the Si waveguide. The geometry provided on-chip directional coupling efficiency between a QD and the Si waveguide at 20-30%. This value is reasonable concerning unfavourable refractive index contrast between InP and Si materials. Additionally, with simulations, we pinpointed sources of photon losses providing further device optimization paths, whereas smaller waveguides should achieve better performance.

Finally, we tested selected devices to provide qualitative and quantitative information regarding the on-chip coupling efficiency and outcoupling off the chip to free space. We primarily use the InP-made half of the circular Bragg grating (CBG) attached to the end of the Si WG. The CBG allows the outcoupling of QD-delivered photons travelling through the SOI chip interior. Moreover, for a selected device with a QD showing 80 % single photon emission purity in the telecom C-band, we could estimate the on-chip coupling efficiency by counting the Si WG travelling photons outcoupled at the cleaved edge of the chip. In this case, the on-chip directional coupling efficiency was estimated to 5.1 %. This number is less than theoretically provided, however, it is influenced by many technological factors. Expanding the proposed hybridization scheme with the method allowing for accurately positioning a QD inside the InP WG can significantly increase the on-chip coupling efficiency.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See Supplement 1 for supporting content.

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