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Analysis of Converter Valve-Side Single-Phase-to-Ground Faults in Symmetrical Monopolar MMCs

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***Abstract*—Converter valve-side single-phase-to-ground (SPG) faults are among the most critical issues affecting the secure operation of modular multilevel converters (MMCs). However, the fault characteristics of these faults in symmetrical monopolar MMCs have not been thoroughly explored. This paper aims to fill this gay by theoretically investigating SPG faults in such systems. The analysis considers various influencing factors, including MMC grounding schemes and dc line types. The findings demonstrate that valve-side SPG faults cause dc voltage oscillations and therefore, large discharging currents from the distributed capacitors of dc lines. These scenarios are examined through mathematical analyses and verified through simulations of a generic MMC-HVDC system using PSCAD/EMTDC. The results accurately reveal the fault behaviors under different system conditions, providing valuable insights for the design of protection systems and insulation coordination for internal ac grounding faults in MMC stations.**

Keywords—DC systems, MMC, single-phase-to-ground fault, converter protection, fault.

I. Introduction

With the rapid development of high power electronic devices, modular multilevel converters (MMCs) have advanced significantly and are now used in both high-voltage (HV) and medium-voltage (MV) dc systems [1]-[2]. However, ensuring their fault-tolerant operation remains a challenge.

To address this challenge, a fault-tolerant operation framework for MMCs has been proposed in [3] to maintain functionality during submodule (SM) open-circuit faults. Ref. [4] outlines potential fault scenarios in an MMC-HVDC link and provides a detailed analysis of dc faults. Studies on dc fault handling methods for MMC-based HVDC systems are presented in [5]-[6], and the modeling and control of MMCs under ac grid-side unbalanced faults are discussed in [7]. However, more attention should be focused on internal AC grounding faults at MMC station wall bushings.

In MMC stations, the interface transformers are located outside the converter valve hall, with the converter wall bushings acting as interfaces between the converter ac buses and the transformers [8]. These wall bushings are within the overlapping protection zones of the converter and transformer (see Fig.1). Flashover and insulation failure at these bushings can lead to single-phase-to-ground (SPG) faults at the valve side of the MMC, which are usually permanent. Although the probability of such station internal SPG faults is low, their analysis and the development of protective solutions should not be overlooked.

Valve-side SPG faults in asymmetrical and bipolar MMCs can lead to severe issues, such as grid-side non-zero-crossing fault currents and overvoltage in upper-arm SM capacitors [9]-[10]. To address these issues, various solutions have been proposed. For example, a dc side *RL* grounding circuit has been proposed in [8] to dampen dc offset currents and create current zero-crossings for the grid-side ac circuit breaker

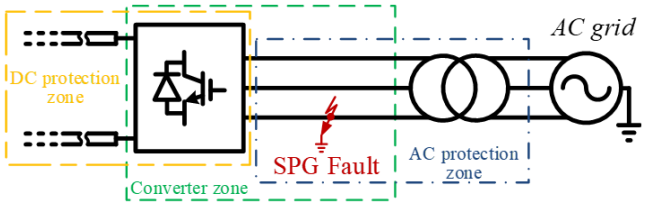


Fig. 1. MMC station internal SPG fault and protection zones.

(ACCB). Additionally, a protection scheme involving thyristor-pairs and damping resistors has been proposed to bypass the diodes and mitigate dc offset currents in [11]. In the ANGLE-DC MVDC project, a dc-link thyristor branch has been proposed to prevent capacitor overvoltage caused by the valve-side SPG fault in the bipolar configuration [12]. However, due to differences in converter station configurations, these solutions are not directly applicable to symmetrical monopolar MMCs.

Valve-side SPG faults in symmetrical monopolar MMCs have been studied in [13]-[14]. However, a theoretical analysis of the large dc pole voltage oscillations has not been provided, nor have the effects of dc lines during the fault been considered. Previous studies on valve-side SPG faults in two-level voltage source converters in [15]-[16] are not entirely applicable to MMCs due to fundamental differences in converter topologies. Therefore, additional research is needed to address valve-side SPG faults in symmetrical monopolar MMCs.

This paper aims to fill these research gaps by: 1) conducting a theoretical analysis to reveal the fault characteristics of valve-side SPG faults in symmetrical monopolar MMCs; 2) investigating factors influencing the fault characteristics, such as the converter grounding and types of dc lines used in point-to-point MMC-HVDC links. The theoretical analysis is supported by simulations performed in PSCAD/EMTDC, with results showing good agreement with the theoretical analysis. These studies will aid in the design of protection systems for internal ac grounding faults in MMC stations.

II. Analysis of MMC Valve-Side SPG Faults

A. Fault Characteristics under SPG Faults

Fig. 2(a) illustrates the configuration of a symmetrical monopolar half-bridge (HB) MMC. Fig. 2(b) presents its single-phase equivalent circuit, where the MMC operates according to:

$$u_x = -\frac{1}{2}L\frac{di_x}{dt} - \frac{1}{2}Ri_x + \frac{u_{xN} - u_{xP}}{2} \quad (x = a,b,c) \tag{1}$$

$$L\frac{di_{xcirc}}{dt} + Ri_{xcirc} = \frac{1}{2}V_{dc} - \frac{u_{xN} + u_{xP}}{2} \quad (x = a,b,c) \tag{2}$$

where Eq.(1) represents the dynamics between the MMC and the ac system. Eq.(2) describes the internal dynamics of the MMC.

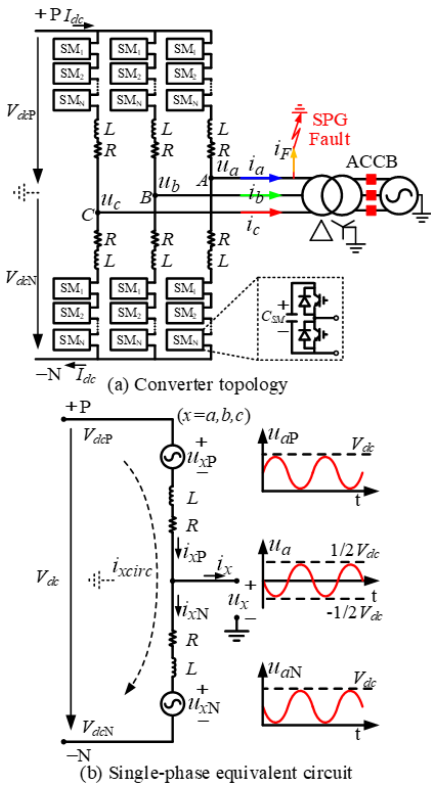


Fig. 2. Symmetrical monopolar HB-MMC.

By neglecting the voltage drops on arm inductors and resistors, as well as the internal circulating currents, the positive and negative dc terminal voltages according to Fig. 2(b) are given in:

$$\begin{cases} V_{dc\mathrm{P}} = u_x + (u_{x\mathrm{P}} + L\dfrac{di_{x\mathrm{P}}}{dt} + Ri_{x\mathrm{P}}) \approx u_x + u_{x\mathrm{P}} \\ V_{dc\mathrm{N}} = u_x - (u_{x\mathrm{N}} + L\dfrac{di_{x\mathrm{N}}}{dt} + Ri_{x\mathrm{N}}) \approx u_x - u_{x\mathrm{N}} \end{cases} \tag{3}$$

where $u_{x\mathrm{P}}$ and $u_{x\mathrm{N}}$ represent the total voltages of the upper and lower amrs, respectively, and are described in:

$$\begin{cases} u_{x\mathrm{P}} = 1/2V_{dc}[\sin(2\pi ft + \theta_x) + 1] \\ u_{x\mathrm{N}} = 1/2V_{dc}[1 - \sin(2\pi ft + \theta_x)] \end{cases} \tag{4}$$

where θ_x is the phase angle of the total arm voltage, f is the ac system frequency. Based on Eq.(3), the voltages follow:

$$\begin{cases} u_{ab} \approx u_{b\mathrm{P}} - u_{a\mathrm{P}}, u_{ca} \approx u_{a\mathrm{P}} - u_{c\mathrm{P}} \\ u_{ab} \approx u_{a\mathrm{N}} - u_{b\mathrm{N}}, u_{ca} \approx u_{c\mathrm{N}} - u_{a\mathrm{N}} \end{cases} \tag{5}$$

where u_{ab} and u_{ca} are the line-to-line voltages at the valve side.

Fig. 3(a) illustrates the pre-fault converter valve-side voltages. Due to the delta grounding of the interface transformer, it forms a virtual neutral point with a zero voltage potential. However, an SPG fault (at phase A) establishes a real zero voltage grounding point, as illustrated in Fig. 3(b).

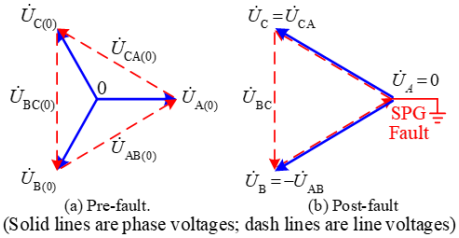


Fig. 3. Changes of MMC valve-side voltages.

In this case, the voltage of the faulted phase becomes zero, but the line-to-line voltages remain unchanged. Consequently, the three phase-to-ground voltages become

$$\dot{U}_{\mathrm{A}} = 0,\ \dot{U}_{\mathrm{B}} = -\dot{U}_{\mathrm{AB}},\ \dot{U}_{\mathrm{C}} = \dot{U}_{\mathrm{CA}}. \tag{6}$$

If the MMC is not blocked by the converter protection system, substituting Eq.(6) into Eqs.(3) and (5) gives:

$$\begin{cases} V_{dc\mathrm{P}} \approx u_{a\mathrm{P}} = 1/2V_{dc}[\sin(2\pi ft + \theta_a) + 1] \\ V_{dc\mathrm{N}} \approx -u_{a\mathrm{N}} = -1/2V_{dc}[1 - \sin(2\pi ft + \theta_a)] \end{cases} \tag{7}$$

According to Eq.(7), after the SPG fault, $V_{dc\mathrm{P}}$ and $V_{dc\mathrm{N}}$ start to oscillate, mirroring the behaviors of the upper and lower arm voltages in the faulted phase. Both voltages contain a dc offset and oscillate at the ac grid frequency. The maximum values of $V_{dc\mathrm{P}}$ and $V_{dc\mathrm{N}}$ reach the pole-to-pole voltage V_{dc}, which is 2 p.u. of the normal dc pole-to-ground voltage. Moreover, it can be observed that $V_{dc\mathrm{P}} - V_{dc\mathrm{N}} \approx u_{a\mathrm{P}} - (-u_{a\mathrm{N}}) = V_{dc}$, which means the dc terminal voltage remains constant.

B. Impact of MMC Grounding Schemes

Grounding of MMCs can be implemented on either the ac side or dc side, each with its own merits and demerits that require detailed analysis. Commonly used grounding schemes for MMCs are summarized in Table I.

TABLE I
COMMONLY USED GROUNDING SCHEMES FOR SYMMETRICAL MONOPOLAR MMCS

	Converter transformer	Converter dc side
Ungrounded	(a) (b)	
Delta/Star and Star-point reactor	(c) (d)	DC side high resistor (g)
AC side high resistor	(e) (f)	

Fig. 4 Illustrates the occurrence of a valve-side SPG fault under different converter grounding schemes. In all cases, grounding point ① represents the pre-fault zero voltage potential reference of the converter, while grounding point ② is the new zero potential voltage reference caused by the SPG fault.

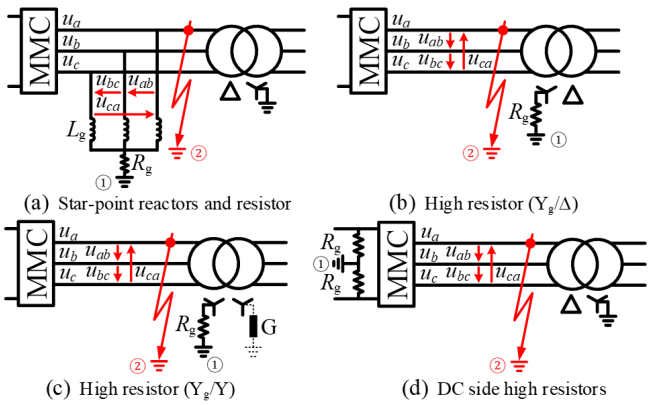


Fig. 4. Valve-side SPG faults under different MMC grounding schemes.

The analysis in the last section confirms that the line-to-line voltages at the valve-side remain unchanged during an SPG fault. Then, as depicted in Fig. 4(a), the line-to-line voltages at the star-point reactors are also unaffected. Due to the large grounding impedance, the fault currents flowing through the star-point reactor and resistor are limited to very small values.

As demonstrated in Figs. 4(b) and (c), the fault currents remain minimal due to the high grounding resistance, validating the previous analysis for these schemes.

In the scenario depicted in Fig. 4(d), the dc side features two resistors with a real grounding point. Consequently, the oscillating 2 p.u. dc side voltages will generate fault currents in the two resistors. However, if very large resistors are selected to handle the 2 p.u. maximum voltage, the fault currents will still be very small.

Based on the above analysis, it can be concluded that the fault characteristics are unaffected by different MMC grounding schemes. Additionally, the circuits indicate that there is no fault current path under the valve-side SPG fault. As a result, the converter's local overcurrent protection will not activate to block the converter.

C. Impact of DC Transmission Lines

In the above analysis, the impact of the distributed capacitors in dc lines, particularly in long HVDC cables, has been ignored. Consequently, although the dc pole voltage exhibits large oscillations, no discharging fault currents arise from the dc transmission line itself. However, the energy stored in the dc transmission lines will discharge through their distributed capacitors, resulting in significant discharging currents that contribute to the SPG fault point through the MMC, as illustrated in Fig. 5.

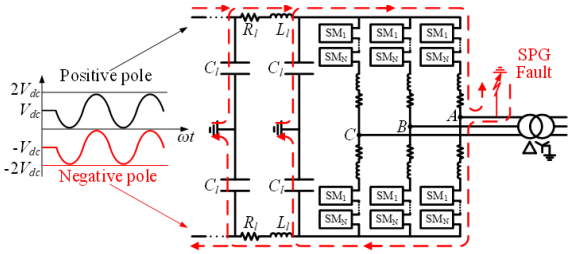


Fig. 5. Impact of the dc line distributed capacitors.

R_l, L_l and C_l represent the distributed resistor, reactor and capacitor of the dc transmission line, respectively. Once an SPG fault occurs, the dc pole voltages begin to oscillate as illustrated in Fig. 5. Subsequently, the energy stored in the dc line discharges through the illustrated current paths. The length and voltage level of the dc line affect this discharging effect.

D. Overvoltage of SM Capacitors

Once the converter's local protection system detects a valve-side SPG fault, the MMC will be blocked, rendering it an uncontrollable diode bridge as depicted in Fig. 6(a). As shown in Fig. 6(b), the SM capacitors in the upper and lower arms can be charged through the series diodes if the following conditions are met:

$$V_{dcP} - u_x > u_{xP(0^-)} \tag{7}$$

$$u_x - V_{dcN} > u_{xN(0^-)} \tag{8}$$

where $u_{xP(0^-)}$ and $u_{xN(0^-)}$ represent the total capacitor voltages of each arm immediately before the converter is blocked.

As shown in Fig. 6(a), during the SPG fault, u_a will drop to 0 (u_a =0). When the converter is blocked, the dc pole voltages will cease oscillating and therefore, will be lower than V_{dc}. In this case, Eqs. (7) and (8) will not be met, which means that the capacitors in both the upper and lower arms of the faulted phase will not charge, and their voltages will remain unchanged once the converter is blocked.

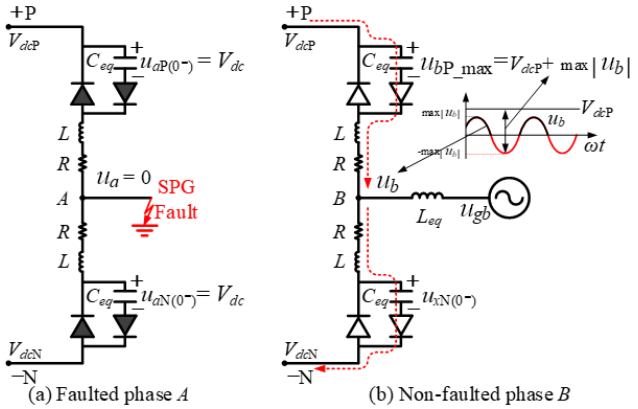


Fig. 6. Equivalent circuits after being blocked.

In the non-faulted phases, such as phase B shown in Fig. 6, the upper-arm capacitors will be charged during each negative half-cycle of u_b and the lower-arm capacitors will be charged during each positive half-cycle of u_b. The charging will stop until the overvoltage reaches the maximum magnitudes of the post-fault valve-side voltage, as illustrated in Fig. 6(b). Therefore, the converter should be isolated as quickly as possible to minimize the capacitor overvoltage.

It is important to note that this phenomenon differs from bipolar MMCs, where only the upper-arm capacitors experience overvoltage, while the lower-arm capacitors remain unaffected.

III. Simulations and Analysis

A. Test Sytem

A symmetrical monopole MMC-HVDC system is modelled in PSCAD/EMTDC, as shown in Fig. 7. The parameters are based on the France-Spain link [17] and are detailed in Table II. In this study, the widely used grounding Scheme (c) in Table I is considered. The SPG fault is set at phase A of the power receiving MMC2 at t = 2 s, with a fault resistor of 0.1 Ω. In the base case, the XLPE cable model with R= 0.0192 Ω/km and L=0.24 mH/km is used.

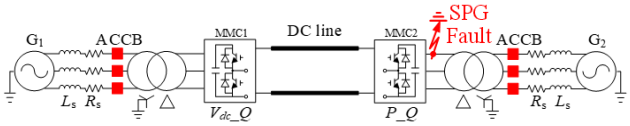


Fig. 7. Schematic diagram of an MMC-HVDC transmission system.

TABLE II
Parameters of the MMC HVDC Link

Parameters	Values
Capacity (MVA)	1050
Rated DC voltage (kV)	± 320
AC grid frequency (Hz)	50
Rated AC voltage (kV)	400
Transformer ratio (kV/kV)	333/400
Transformer leakage reactance (p.u.)	0.18
Number of SMs in each arm	10
SM capacitance (mF)	8
Arm inductance L (H)	0.05
Arm resistance R (Ω)	0.1
AC system equivalent resistance R_S (Ω)	1.51625
AC system equivalent reactor L_S (H)	0.04826

Simulations are first conducted under the base case (shown in Fig. 2), followed by the application of different factors to assess their impact on the SPG fault characteristics.

It is important to note that, during the SPG fault, the converter remains unblocked in the tests. As shown in Fig. 8(a), the SPG fault leads to u_a =0. At the same time, the two non-faulted phases become the line-to-line voltages. The valve-side ac currents are unaffected, as shown in Fig. 8(b). Fig. 8(c) demonstrates that positive and negative dc pole

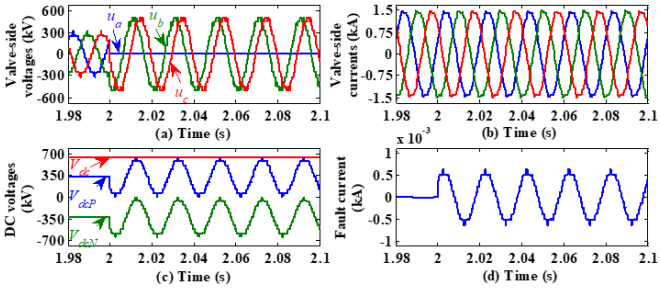


Fig. 8. The base case subject to the valve-side SPG fault.

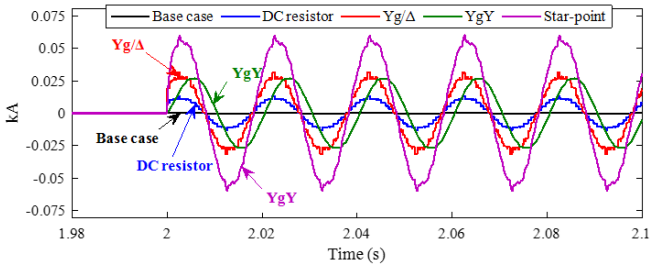


Fig. 9. Fault currents under different grounding schemes.

voltages begin to oscillate sinusoidally at the ac fundamental frequency. However, it can be seen that the dc terminal voltage V_{dc} remains unchanged. Fig. 8(d) indicates that the current flowing into the fault point [i_F shown in Fig. 2(a)] is very small, less than 0.6 A, making it negligible. The results are consistent with the theoretical analysis presented in Section II.

B. Impact of MMC Grounding Schemes

To assess the impact MMC grounding schemes on SPG fault characteristics, Schemes (c) through (g) are applied to the above base case model. The grounding impedances are listed in Table III. Simulations indicate that the valve-side ac voltages, currents and dc voltages under Schemes (d) to (g) are very similar to the results in Fig. 8. Therefore, those results are not repeated in this section.

TABLE III
PARAMETERS OF THE GROUNDINGS

Parameters	Values
Scheme (d)	5 H and 5 kΩ
Schemes (e) and (f)	10 kΩ
Scheme (g)	50 kΩ

The fault current [i_F shown in Fig. 2(a)] under various groundings is presented in Fig. 9. In the base case, i_F remains at 0, indicating that the fault does not estabilish a closed fault current path. When the dc-side grounding Scheme (g) is used, the fault current is very small (max. 0.013 kA), due to the oscillating dc pole voltages discharging the dc line. For Schemes (e) and (f), the fault currents are induced by the valve-side zero-sequence voltage during the SPG fault. These currents are under 0.03 kA and can be further reduced by increasing the grounding resistor. The 30˚ phase angle difference between the two currents is due to the transformer windings. For Scheme (d), the fault current is higher, at less than 0.06 kA, because of the lower grounding impedance compared to the other schemes.

The simulation results align closely with the analysis, indicating that different grounding schemes do not significantly impact the fault currents.

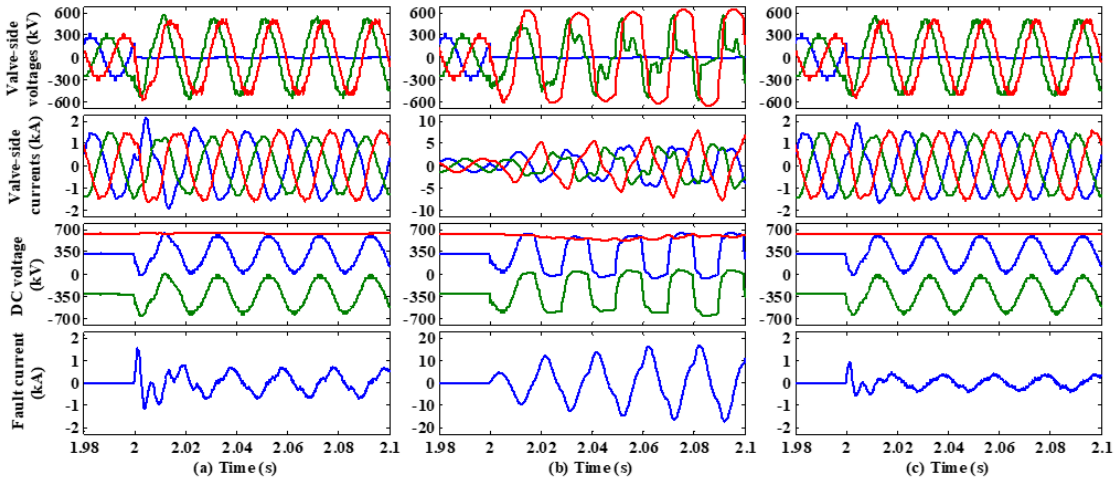
C. Impact of DC Transmission Lines

The above analysis does not test the impact of the dc transmission lines, such as cable and overhead line (OHL). This section investigates their impact on the valve-side SPG fault behaviors by applying Frequency Dependent (FD) HVDC cable and OHL models to the base model. The parameters for the cable and OHL are from [18] and [19] and are presented in Fig. 12 in the Appendix.

In the case shown in Fig. 10(a), a 20 km FD cable model is used. Compared to Fig. 8, there are noticeable distortions in all voltages and currents following the SPG fault. The fault current i_F appears with a maximum of 0.7 kA. The reason behind this phenomenon is that the energy stored in the cable discharged through its distributed capacitors, driven by the oscillating dc pole voltages.

The situation worsens significantly in the results shown in Fig. 10(b), where the FD cable is increased ten times to 200 km. In this case, the energy stored in the cable is much greater than the previous case, resulting in much larger discharging currents feeding into the fault point. This causes a substantial fault current i_F and severe distortions in all voltages and currents, with i_F exceeding 16 kA, posing a significant risk of damaging the devices.

In the case shown in Fig. 10(c), a 200 km FD OHL model is employed. The fault consequences are less severe compared to the results in Fig. 10(b) because the distributed capacitors of OHLs is smaller than that of cable-based systems. Although



(a) 20 km frequency dependent cable model. (b) 200 km frequency dependent cable model. (c) 200 km frequency dependent OHL model

Fig. 10. The impact of HVDC cable and OHL.

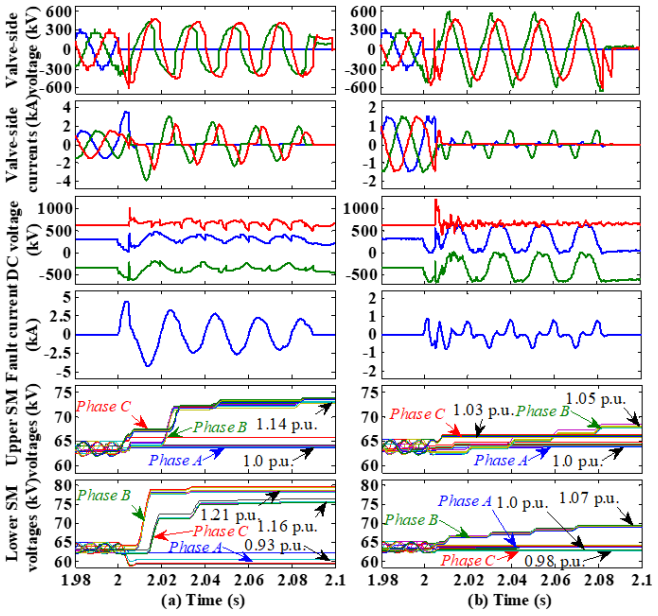


Fig. 11. Fault behaviors under 200 km FD cable and OHL models.

the fault current i_F is not excessively large and the valve-side voltages and currents are not severely impacted, the dc pole voltages still exhibit significant oscillations.

The simulations show good agreement with the theoretical analysis.

D. Overvoltage of SM Capacitors

The typical protection strategy using the grid-side ACCB [8] to isolate the faulted converter is assessed for both the 200 km FD cable and OHL models. The converter will be blocked if the IGBT currents exceed 2 kA, with an assumed ACCB operating time delay of 80 ms.

Fig. 11(a) illustrates the fault behaviors using the FD cable model. When the converter is blocked due to the overcurrent protection, the valve-side currents, dc pole voltages and fault current i_F are all relieved compared to the results in Fig. 10(b), where the converter is not blocked. Distortions in dc voltages are due to the diode bridge after the converter is blocked. Notably, capacitor voltages in the faulted phase remain unchanged after blocking, while those in the non-faulted phases are overcharged.

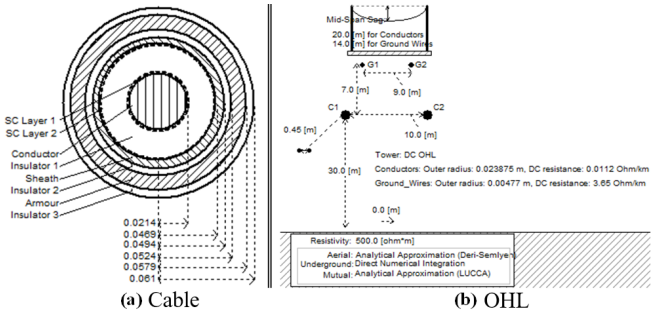
Fig. 11(b) shows the case using the FD OHL model. In this case, the valve-side fault currents are significantly reduced after blocking. The fault current i_F is smaller due to the reduced discharging effect from the OHL. Additionally, capacitor overvoltage is relieved compared to the cable-based model. This is because the OHL has a lower discharging effect, resulting in less charging of the SM capacitors. Consequently, the overvoltage capability requirements for SM capacitors in OHL-based systems can be less stringent than those in cable-based systems.

IV. Conclusion

This paper presents a theoretical analysis to understand the fault behaviors of symmetrical monopolar MMCs under valve-side SPG faults, considering various influencing factors. The analysis is verified using simulations in PSCAD/EMTDC. The findings reveal that a valve-side SPG fault in symmetrical monopolar MMCs results in: *i*) overvoltage ($\sqrt{3}$ times) at the valve side in the non-faulted phases; *ii*) serious oscillations of the positive and negative dc pole voltages, whose behaviors follow the upper and lower arm voltages in the faulted phase; *iii*) substantial fault currents discharged from the distributed capacitors of the dc line, particularly in cable-based systems; *iv*) overvoltage in SM capacitors of both the upper and lower arms when the converter is blocked.

Additionally, the studies reveal that different MMC grounding schemes have a negligible impact on fault behaviors, while longer dc transmission lines exacerbate fault consequences. Implementing a grid-side ACCB as a protection strategy can protect the MMC from the severe valve-side SPG fault consequences.

Appendix



(a) Cable (b) OHL

Fig. 12. Parameters of the dc transmission lines.

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