Method for fabricating sic-on-insulator material stacks

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(54) Title: METHOD FOR FABRICATING SIC-ON-INSULATOR MATERIAL STACKS

(57) Abstract: The invention regards a method for nanofabricating a SiC-on-insulator material stack, comprising the steps of providing a SiC layer comprising a first proximal surface and a first distal surface, providing a Si substrate comprising a SiOx layer on a second proximal surface, depositing a first adhesive layer and a second adhesive layer of an adhesive material on the first and the second proximal surfaces, respectively, contacting the first adhesive layer and the second adhesive layer with each other, and curing the first and the second adhesive layers for forming a SiC on-insulator material stack.

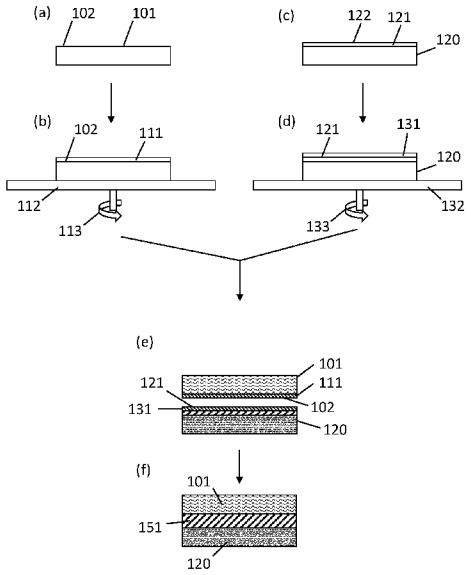

FIG. 1

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Method for fabricating SiC-on-insulator material stacks

Field of disclosure

The invention relates to a method for fabricating up to wafer size SiC-on-insulator material by using an adhesive, for application in nanophotonic experiments.

Background

The research in the field of the semiconductor SiC has gained increased attention. In the past, this material has been studied extensively due to its well-known high temperature, high frequency and high performance electronic properties. Nowadays, the uses of the optical properties of SiC are raising the importance in this material in state of the art nanophotonic experiments. Properties such as the wide band gap, the high thermal conductivity and the large second and third order non-linearity are key to develop applications within quantum transport experiments and nonlinear photonics.

In particular, special interest is on the hexagonal close-packed 4H-SiC. The recent ability to industrially manufacture ultra high purity 4H-SiC has opened the door to a massive implementation of SiC in nowadays electronic and photonic systems. Specially, the properties of this material such as the band gap of 3.2 eV, the low absorption loss at telecommunication wavelength and the fabrication of high quality wafers are the key properties for the fabrication of next generation photonic systems and circuits. Previous experiments have demonstrated the outstanding properties of 4H-SiC in form of high Q-factor microring resonators or single photon sources, thereby showing the possibilities for future application in photonic integrated circuits, electronics, quantum electronics or quantum photonic integrated circuits.

Nevertheless, the refractive index of 4H-SiC (n = 2.646) requires a thin adjacent silicon oxide layer as an optical insulator to be able to effectively use it in photonic circuits. This stack of materials is defined as 4H-SiC-on-insulator stack and holds promising properties in the use in of nanophotonics field.

Due to the complexity of fabricating 4H-SiC in epitaxial processes, the fabrication method typically used to create a 4H-SiC-on-insulator stack is to bond a 4H-SiC wafer on top of an oxidized silicon substrate. In order to achieve this, several approaches

have been tested in the past, such as plasma activated bonding, anodic bonding and direct bonding.

Prior fabrication of SiC-on-insulator material stacks typically rely in the direct bonding method, which requires extremely smooth surfaces both in the Si oxide layer and the SiC prior the bonding step. This requisite strongly affects the size of the generated samples, due to imperfections appearing by the native roughness of both surfaces. In addition, no known industrial large scale fabrication machines or apparatus exist for the fabrication of SiC-on-insulator material stacks. Relaxing any of the strong requirements needed during the bonding method is an active field of research. Hence, any advancement in the industrial fabrication of 4H-SiC-on-insulator would help to develop better quality and cheaper nanophotonic devices for scientific research and commercial use.

Summary

Considering the prior art described above, it is an object of the present invention to relax the roughness requirement needed in the SiC and the Si oxide surfaces while fabricating 4H-SiC-on-insulator material stack. At the same time, it is an object of the present invention to increase surface size of a generated material stack.

The object can be achieved by means of a nanofabricating method of SiC-on-insulator material stack, comprising the steps of providing a SiC layer or SiC substrate comprising a first proximal surface and a first distal surface, and providing a first substrate comprising a second proximal surface.

The first substrate can be a low refractive index substrate, such as sapphire, and/or the first substrate can be provided with a SiOx layer on the second proximal surface.

A first adhesive layer of an adhesive material, which is preferably flowable, is deposited on the proximal surface of the SiC layer. A second adhesive layer of the adhesive material is deposited on the second proximal surface. Different adhesives on the SiC layer and on the Si oxide layer can also be contemplated within concept of the present disclosure. The first adhesive layer and the second adhesive layer are placed in contact with each other and a curing step can be performed to the stack, changing the

chemical composition of the adhesive layer and forming a final SiC on-insulator material stack.

Thus, this method allows to industrially fabricate wafer size material stacks of SiC on-insulator without the prior art limitations or smoothness of the initial materials.

Preferably, the adhesive material is comprised of hydrogen silsesquioxane. The physical and chemical properties of hydrogen silsesquioxane allows to perform the spin coating technique while precisely controlling the thickness of the deposited layer. A particularly relevant chemical property of the hydrogen silsesquioxane is the change in chemical composition of the compound under a curing process by applying thermal energy. Such property requires standard nanofabrication techniques and allows to generate high quality SiC on-insulator stacks in full size commercial semiconductor wafers.

Description of the drawings

The invention will in the following be described in greater detail with reference to the accompanying drawings:

Fig. 1 a schematic view of a method for fabricating stacks of SiC-on-insulator materials via the use of an adhesive.

Fig. 2 a graph describing the thickness of the applied HSQ layer as a function of the rotation speed used during the spin resist fabrication step.

Detailed description

Fig. 1 shows a schematic view of the method for fabricating wafer size SiC on-insulator substrates herein disclosed. Fig. 1a shows a first step, where a layer or substrate of 4H-SiC 101 is provided with a first proximal surface 102. Said SiC layer 101 may comprise a 4 inch, 8 inch or even 12 inch wafer, which are common wafer sizes used in the semiconductor and integrated photonic circuit fields. The surface comprising a 12 inch diameter substrate is in the order of 700 cm^2. Fig. 1b shows a second step, where droplets like e.g. few droplets of a flowable hydrogen silsesquioxane adhesive can be deposited on the first proximal surface 102 of the SiC layer forming a first adhesive layer 111. The SiC layer may be placed in a spin coating apparatus 112, wherein the layer spins at high velocity as indicated by a first arrow 113. Due to the centrifugal force

experienced by the hydrogen silsesquioxane, the first adhesive layer is stretched out for covering most or all of the first proximal surface; at the same time the thickness of the first adhesive layer will be reduced and the first adhesive layer will be even and uniform.

Other type of flowable adhesive materials may be used, such as for example benzocyclobutene, poly(methyl methacrylate), or other kind of ultra violet, deep ultra violet, thermal or electron beam resists.

Fig. 1c shows a third step, where a first substrate 120 of sapphire or a semiconductor is provided having a second proximal surface 121. Said semiconductor may be comprised for example by a II-VI semiconductor, III-V semiconductor or a IV type semiconductor. A layer of a low refractive index insulator 122 can be deposited on or generated in the second proximal surface of the first substrate 120. Said insulator may be comprised for example by Si oxide (SiOx layer), sapphire or quartz. The Si oxide layer will be preferable if the first substrate is made of a III-V semiconductor or Si. The III-V semiconductor can e.g. be GaAs, InAs, GaSb, InSb, InP, GaP or AlAs. The II-VI semiconductor can e.g. be ZnO, MgO, MgTe, ZnSe, CdTe or CdS. The Si oxide layer is optional if the first substrate is made of sapphire. Additionally, a low refractive index layer on one side or both sides of the SiC layer or substrate is optional.

The Si oxide layer 122 of the second proximal surface 121 of the first substrate 120 might be provided from an industrial manufacturer or developed via any of the nanofabrication techniques available for such purpose, such as thermal oxidation of the Si first hundreds of nm. The thickness of the Si oxide layer can be controlled during thermal oxidation step. A typical thickness for the Si oxide may be in the range of few hundreds of nm, although ultra-thin films in the order of several nm and thick films in the order of several μm might be of interest for the realization of 4H-SiC-on-insulator material stacks.

Similarly to the second step as shown in Fig. 1b, Fig. 1d shows a fourth step, where droplets like few droplets of hydrogen silsesquioxane adhesive are deposited on the second proximal surface 121 of the first substrate 120 for forming a second adhesive layer 131. The first step may be provided on or placed on a spin resist 132 for performing spin resist step as indicated by a first arrow 133 to reduce the thickness of

the hydrogen silsesquioxane and for forming an even second adhesive layer 131, and for covering most or all of the second proximal surface 121.

The third step can be performed before, after or at the same as the first step and/or the second step. The fourth step can be performed before, after or at the same as the first step and/or the second step.

A baking step involving the application of heat may be performed on the SiC layer and the first substrate for baking the first and second adhesives. This step may be performed or skipped depending on the desired chemical arrangement of the hydrogen silsesquioxane prior the next steps. Other adhesives might require different number of baking steps and conditions, depending on the particular chemical properties of the compounds.

Fig. 1e shows a fifth step, where the first proximal surface 102 and the second proximal surface 121 are approached until contact. The first adhesive layer 111 of the SiC layer 101 and the second 131 adhesive layer of the first substrate 120 are contacted. A force can be applied on the SiC layer 101 and the first substrate 120 to enhance the distribution of first and second adhesive layers. The applied force might be spread homogeneously along the wafer or at selected points spread homogeneously or inhomogeneously at selected points of the substrates. Said required force and a required temperature might be applied by a wafer bonding apparatus. A wafer bonding allows to precisely control the bonding conditions between a plurality of wafers. It also allows to apply a certain pressure and temperature profile along the wafers during the bonding process, depending on the physical and chemical properties of the substrates and adhesive being used.

The thickness redistribution of the hydrogen silsesquioxane layer while applying the opposing force on the substrates smooths any roughness originally located on any distal surface of the substrates. The smoothening of the interface between substrates due to the hydrogen silsesquioxane redistribution relaxes the requirement of ultra smooth surfaces needed in prior art fabrication of SiC on-insulator material stacks.

Fig. 1f shows a sixth step, wherein a curing step can be performed on the combined SiC layer 101 and first substrate 120. The curing may imply the application of thermal

energy to increase the temperature of the hydrogen silsesquioxane up to hundreds of °C during a time of up to some or several hours. A curing process may comprise the heating of the combined SiC layer and first substrate to 450 °C for 5 hours. Alternative curing processes may comprise the heating of the combined SiC layer and first substrate to 250 °C for 2 hours, or 650 °C for 5 hours, or 850 °C for 2 hours. During this process, the chemical composition of hydrogen silsesquioxane changes to pure Si oxide, converting the material stack in a 4H SiC – Si oxide – Si material stack comprising the and first substrate 120, a Si oxide layer 151, and the Sic layer 101 as shown in Fig. 1f. Other adhesives might require different number of curing steps and conditions, depending on the particular chemical properties of the compounds.

In an embodiment, the SiC on-insulator material stack can be configured, such that the optical loss is less than 0.1 dB/cm. It can be advantageous for a material stack to have low optical losses, as that would mean that it can be used for photonic applications. The reason why the present disclosure can achieve such low optical is due to the reduction of the SiC thickness caused by mechanical means such as polishing or saw milling, or by chemical means, such as by performing wet etching. After such a process, the SiC layer can have higher thickness uniformity, surface smoothness and less surface states due to the surface passivation. The reduction of surface states is caused by radical hydrogen ions, which are capable of terminating the dangling bonds that may be present in the material stack, effectively passivating the surface.

The surface passivation can be beneficial, as it prevents dangling bonds from causing surface states in the interface of the material. As described in the previous paragraph, the surface passivation can lead to lower optical losses less than 0.1 dB/cm, and the surface passivation can be performed by either wet or dry methods. For example, dry methods can be performed by depositing a thin layer of oxide such as AlO_x, SiO_2 or HfO_x using atomic layer deposition. Another way of achieving surface passivation via a dry method can be annealing the SiC on-insulator material stack in a furnace up to or at 400 °C. The annealing process can also be performed at higher temperatures, depending on the specifications of the SiC on-insulator material stack. In an embodiment, the surface passivation can be performed by wet methods, such as submerging the SiC on-insulator material stack in a chemical that treats the surface. For example, such a chemical can be Poly(ethylene glycol) (PEG), hyperbranched polyethylenimine (PEI) or poly(propionyl ethyleneimine-co-ethyleneimine) (PPEI-EI).

The mentioned nanofabrication techniques in the present disclosure may be applied to full size semiconductor wafers of typically 4", allowing the fabrication of high surface substrates in a scalable manner.

The method can be configured, such that the SiC layer is a crystalline polytype, such as wurtzite, 15R, 6H or preferably 4H. Differences among the various crystalline polytypes lie on the type of cubic and hexagonal bonds of the SiC layer.

Fig. 2 shows a plot 200 describing the ability for controlling on the thickness of hydrogen silsesquioxane during the spin resist step. The y axis 201 shows the final thickness of the hydrogen silsesquioxane and the x axis 202 shows the revolutions per minute applied to the substrates during the spin process. The square data points 203 correspond to experimental measurements of the final thickness of the hydrogen silsesquioxane deposited on different first substrates, for a given rotation speed. All data points were measured for spin resist experiments of 60 seconds. The black curve 204 corresponds to the fitted data of the spinning experiments of the hydrogen silsesquioxane, performed on a 2x2 cm first substrate of Si. A saturation is observed in the hydrogen silsesquioxane of 750 nm at higher rotation speeds. The grey curve 205 corresponds to the fitted data of the spinning experiments of the hydrogen silsesquioxane, performed on a 4" first substrate of Si. In this case, the thickness tends to decrease when increasing the rotation speed, so that the thickness of the hydrogen silsesquioxane can be controlled by controlling the rotation speed.

The measured data presented in Fig. 2 allows to fine tune the desired thickness of the hydrogen silsesquioxane adhesive between the SiC layer and the first substrate of Si. This allows reducing the effect of possible smoothness variations between the first and second proximal surfaces due to the redistribution of adhesive, making a high quality and continuous interface.

A final step may be performed after the curing of the hydrogen silsesquioxane. A thickness reduction of the SiC layer from the original thickness to a thin film thickness of some or several μm or even hundreds of nm may be desired for certain nanophotonic implementations. Said thickness reduction may be performed by

mechanical means such as polishing or saw milling, or by chemical means, such as by performing wet etching.

Certain nanophotonic integrated circuit implementations may require the use of a sapphire or III-V semiconductor substrate as a substitute to the Si substrate. Said semiconductors are expected to behave similarly while applying the disclosed fabrication method and it is understood that a person skilled in the art may reach similar final material stacks by interchanging the Si substrate by another semiconductor substrate. In the particular case of performing the disclosed method on a sapphire substrate, a thin layer of Si oxide on the proximal surface of the first substrate would not be needed due to the intrinsic optical properties of the sapphire.

An industrial scale apparatus for fabricating SiC on-insulator material stacks to a large scale may be defined as follows. The apparatus may comprise a first spin coater configured for holding and spinning a SiC substrate having a first adhesive layer on its proximal surface. A second spin coater is configured for holding and spinning a substrate having a second adhesive layer on its surface. The spin coater is configured for positioning the SiC layer on the first substrate so that the first proximal surface and the second proximal surface face each other, or viceversa. The apparatus may further comprise a wafer bonder for applying a pressure on the SiC layer and the substrate, for pressing the first proximal surface and the second proximal surface against each other and achieving a homogeneous adhesion. The apparatus may further comprise a heating element for curing the first and the second adhesive layers for forming a SiC on-insulator material stack. The fabricated substrates may be of any standard size used in the semiconductor industry, such as for example 4 inch, 8 inch or 12 inch wafers.

Claims

1. A method for nanofabricating a SiC-on-insulator material stack for photonics, comprising the steps of:
   - providing a SiC layer comprising a first proximal surface and a first distal surface,
   - providing a first substrate comprising a second proximal surface,
   - depositing a first adhesive layer and a second adhesive layer of an adhesive material on the first and the second proximal surfaces, respectively,
   - contacting the first adhesive layer and the second adhesive layer with each other, and
   - curing the first and the second adhesive layers for forming a SiC on-insulator material stack.

2. The method according to claim 1, wherein the method comprises the step of baking the first adhesive layer and the second adhesive layer, preferably before contacting the first adhesive layer and the second adhesive layer with each other.

3. The method according to any of the preceding claims, wherein the first substrate is a low refractive index substrate, such as sapphire or quartz, and/or a II-VI, IV or III-V semiconductor, and/or a Si substrate.

4. The method according to any of the preceding claims, wherein the first substrate is provided with a SiOx layer or a quartz layer on the second proximal surface.

5. The method according to any of the preceding claims, wherein the method comprises the step of reducing the thickness of the SiC layer, preferably after curing the first and the second adhesive layers.

6. The method according to any of the preceding claims, wherein the SiC layer is a crystalline polytype, such as wurtzite, 15R, 6H or preferably 4H.

7. The method according to any of the preceding claims, wherein the SiOx layer is generated by nanofabrication processes, such as by thermal oxidation of Si, or by chemical vapour deposition.

8. The method according to any of the preceding claims, wherein the adhesive material is hydrogen silsesquioxane.

9. The method according to any of the preceding claims, wherein the adhesive material is deposited and/or distributed, preferably homogeneously, on the first and the second proximal surfaces by spin coating.

10. The method according to any of the preceding claims 2-9, wherein the step of baking the first adhesive layer and the second adhesive layer comprises a series of several baking steps, wherein at least a first of the baking steps comprises a first baking temperature different than a second baking temperature of a second baking step, optionally wherein the first of the baking steps has a first baking duration different that a second baking duration of the second baking step.

11. The method according to claim 10, wherein each baking step comprises different baking temperatures and optionally different baking durations.

12. The method according to any of the preceding claims, wherein the annealing step comprises a series of several annealing steps, wherein at least a first of the annealing steps comprises a first annealing temperature different than a second annealing temperature of a second annealing step, optionally wherein the first of the annealing steps has a first annealing duration different that a second annealing duration of the second annealing step.

13. The method according to claim 12, wherein each step comprising different annealing temperatures and optionally different annealing durations.

14. The method according to any of the preceding claims, wherein the thickness reduction of the SiC layer is performed by polishing techniques, such as mechanical milling, wet etching or dry etching.

15. The method according to any of the preceding claims, wherein the step of curing the first and the second adhesive layers comprises a step of heating the

first and the second adhesive layers to no more than 450°C, preferably less than 300°C, more preferably less than 200°C.

16. A SiC on-insulator material stack comprising a SiC layer on top of a SiOx layer on top of a first substrate, wherein the SiC on-insulator material stack has a surface area of more than 10 cm^2, preferably more than 50 cm^2, even preferably more than 100 cm^2, and most preferably more than 700 cm^2.

17. The SiC on-insulator material stack according to claim 16, wherein the first substrate is made of an element selected from the group III-V or IV, preferably Si.

18. The SiC on-insulator material stack according to claim 16 or 17, wherein the SiC on-insulator material stack has an optical loss of less than 0.1 dB/cm.

19. The SiC on-insulator material stack according to claim 18, wherein the SiC on-insulator material has been surface passivated.

20. The SiC on-insulator material stack according to any of the claims 16-19, wherein the SiC on-insulator material stack is nanofabricated according to the method of any of the claims 1-14.

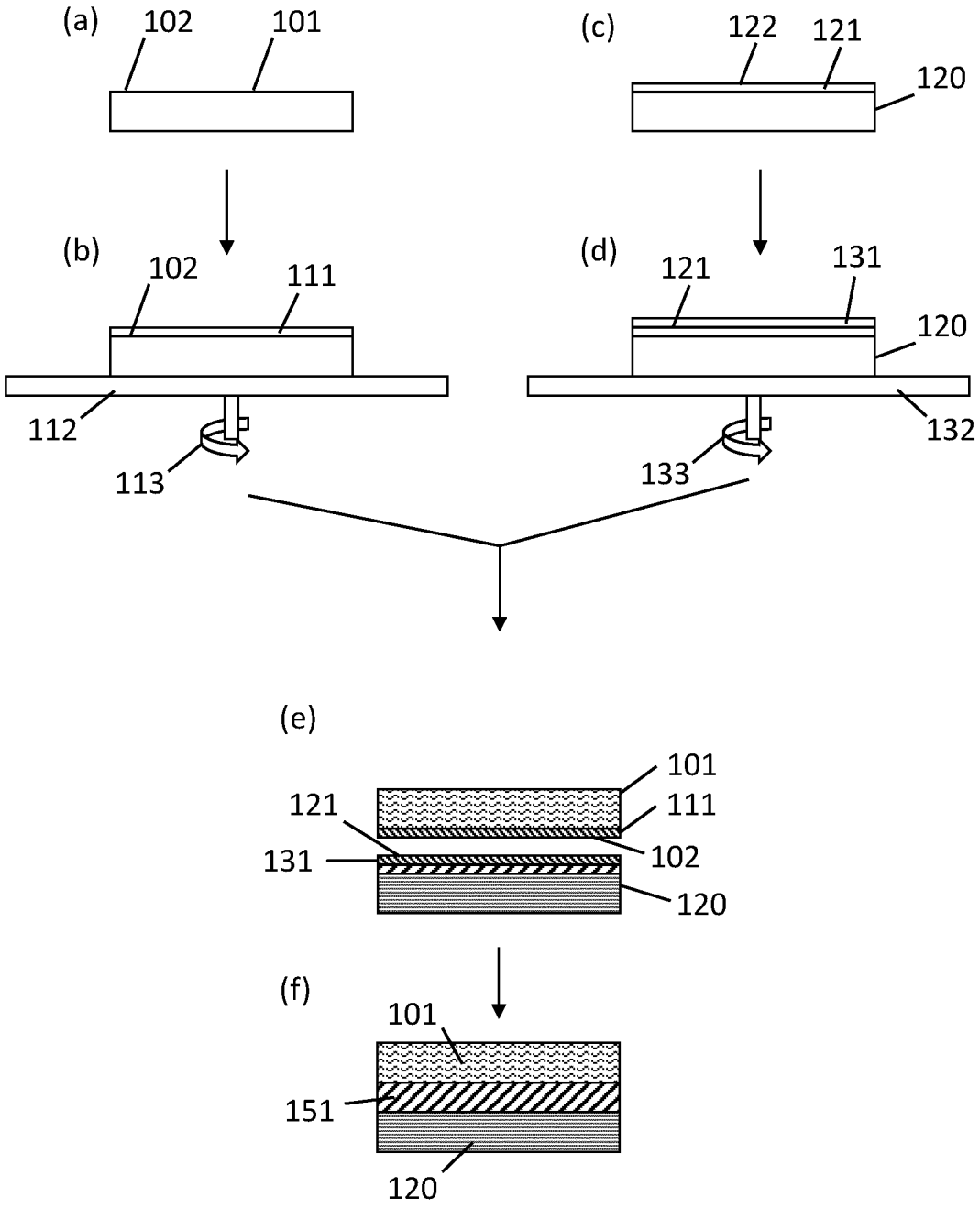
21. An apparatus for fabricating a SiC on-insulator material stack for photonics according to any of the claims 16-20, wherein the apparatus comprises
    - a first spin coater configured for holding and spinning a SiC layer having a first adhesive layer on a first proximal surface, and
    - a second spin coater configured for holding and spinning a first substrate having a second adhesive layer on a second proximal surface,

    wherein the first spin coater is configured for positioning the SiC layer on the first substrate so that the first proximal surface and the second proximal surface face each other, and/or the second spin coater is configured for positioning the first substrate in the SiC layer so that the first proximal surface and the second proximal surface face each other, wherein the apparatus comprises
    - a wafer bonder for applying a pressure on the SiC layer and/or the first substrate for pressing the first proximal surface and the second proximal surface against each other, and

- a first heating element for curing the first and the second adhesive layers

for forming a SiC on-insulator material stack.

22. The apparatus according to claim 21, wherein the apparatus has a second heating element for baking the first adhesive layer and the second adhesive layer, optionally the first heating element and the second heating element are the same.


(a)
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(c)
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(d)
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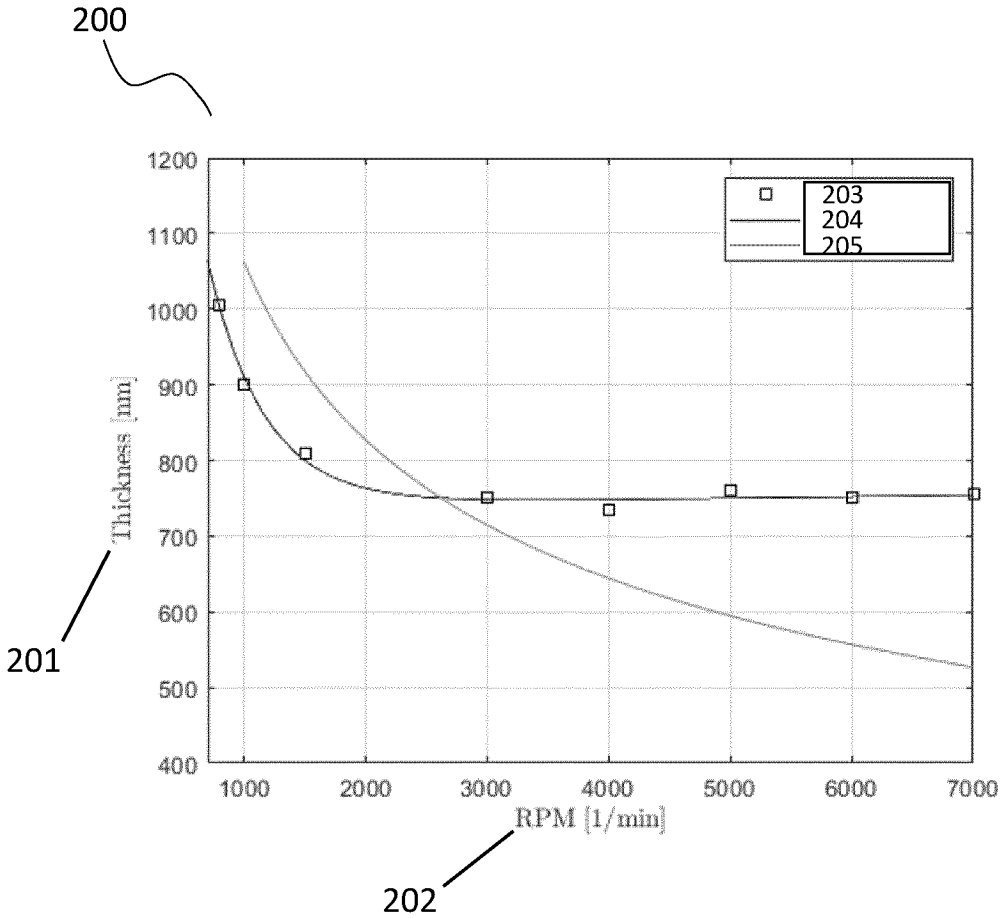
FIG. 1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Thickness [nm]
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1000
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5000
6000
7000
RPM [1/min]
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204
205

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2023/074776

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/20 H01L21/02 H01L21/762
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/284589 A1 (LEE JAE HYUNG [US] ET AL) 29 September 2016 (2016-09-29) paragraphs [0111] - [0119]; figures 2A-2F,6	1-22
A	JINWOOK W CHUNG ET AL: "N-Face GaN/AlGaN HEMTs Fabricated Through Layer Transfer Technology", IEEE ELECTRON DEVICE LETTERS, IEEE, USA, vol. 30, no. 2, 1 February 2009 (2009-02-01), pages 113-116, XP011240903, ISSN: 0741-3106, DOI: 10.1109/LED.2008.2010415 figure 1	14

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Date of the actual completion of the international search	Date of mailing of the international search report
6 November 2023	16/11/2023

Name and mailing address of the ISA/	Authorized officer
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1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2023/074776

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016284589 A1	29-09-2016	KR 20160094416 A	09-08-2016
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