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Published in:

Proceedings of 2024 IEEE Energy Conversion Congress and Exposition (ECCE)

Link to article, DOI:

[10.1109/ECCE55643.2024.10861181](https://doi.org/10.1109/ECCE55643.2024.10861181)

Publication date:

2025

Document Version

Peer reviewed version

[Link back to DTU Orbit](#)

Citation (APA):

dos Santos Serra, A. W., Ribeiro, L. A. S., & Savaghebi, M. (2025). An Improved Control for Grid-Following Inverter with Active Damping and Capacitor Voltage Decoupling. In *Proceedings of 2024 IEEE Energy Conversion Congress and Exposition (ECCE)* IEEE. <https://doi.org/10.1109/ECCE55643.2024.10861181>

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An Improved Control for Grid-Following Inverter with Active Damping and Capacitor Voltage Decoupling

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Abstract— In this paper a current control strategy is proposed for grid-following inverters that are connected to the grid through *LCL* filters. A lead compensation is utilized in series with the proportional gain of the current controller so that high bandwidth is achieved. Furthermore, capacitor current feedback active damping is used to mitigate the effect of the *LCL* filter resonance frequency. In addition to the improvements mentioned before, capacitor voltage decoupling is also used to enhance the disturbance rejection capability of the inverter. The proposed strategy is validated through theoretical analysis and experimental results obtained in a testbench.

Keywords—grid-following inverter, *LCL* filter, current controller, active damping

I. INTRODUCTION

The energy matrix has suffered a meaningful change in the last years with the increasing penetration of renewable energy sources (RESs), mainly photovoltaic and wind power plants, alongside with energy storage systems (ESSs). The use of RESs brings many advantages to the electrical grid, including distributed energy generation where its application may improve reliability and stability of the local electrical grid, as well as providing benefits to suppliers by reducing system losses over long transmission lines and reducing the total investments required to create a new transmission line due to increased energy consumption [1]. A type of converter widely used to make the connection between RESs and the electrical grid is the grid-following (GFL) inverter, where its control strategy is normally set to operate at rated output power and to inject it in an energized grid. The current references of the current loop (which can use a Proportional+Integral (PI) controller in synchronous reference frame or Proportional+Resonant (PR) controller in stationary reference frame) are usually generated by two power control loops, being one for active power (P) and another one for reactive power (Q) [2].

One of the most common events when it comes to GFL inverters operating connected to the grid, is the presence of voltage harmonics at the point of common coupling (PCC) and the variation in the grid impedance, however it is known that

these two events can deteriorate the GFL's inverter desired operation [3]. In the GFL inverters, a filter is needed to attenuate the switching harmonics generated from pulse-width modulation (PWM), with the *LCL* filter being one of the most used due to its better harmonic attenuation with reduced inductance when compared to the *L* filter [4]. Nevertheless, the *LCL* filter introduces an inherent resonance at the resonance frequency (f_r) with a high resonance peak and a sharp phase step down of -180° , which can lead to unstable operation of the GFL's inverter current loop [5]. Due to this undesirable effect, many control techniques have been proposed aiming to damping the resonance at f_r , with active damping (AD) being one of the most used solutions.

Assuming the time delay equal to 1.5 times the sampling period (T_s), it is known that the critical frequency is one-sixth of the sampling frequency (f_s) below the Nyquist frequency ($f_s/2$). For digital control systems, a stable grid-side current control can be achieved for the *LCL* filter whether f_r is between one-sixth and half of f_s and below $f_s/6$ for converter-side current control [6]. Nevertheless, if the grid impedance changes, f_r will also change, and the stable operation of the GFL inverter can no longer be guaranteed.

Therefore, control strategies must be used at the GFL inverter current loop to avoid the unwanted effect of the resonance (which can change with variation in line impedance), as well as improving the injected current quality under adverse grid conditions.

Several works have been developed aiming to provide positive damping for the resonance problem in *LCL* filters. In [7], the authors propose a second-order lead filter in cascade with a bandpass filter as an AD controller for inverter-current feedback AD. It is shown that this second-order filter with the bandpass filter preserves the *LCL* filter's low-frequency gain and inductive nature resulting in improved dynamic response. In [8], the authors propose a strategy based on passivity to design a capacitor-current feedback AD to achieve passive output admittance. It is shown that introducing a small delay into the

capacitor-current feedback AD, the passivity of the output admittance around $f_s/6$ is enhanced.

In this context, this paper presents a control strategy for GFL inverter based on capacitor current feedback AD to mitigate the resonance, and capacitor voltage decoupling (CVD) to improve disturbance rejection capability. The main advantages of the proposed technique are as follows:

- A current controller with high bandwidth.
- A simple approach based on a first-order function to extend the critical frequency up to the Nyquist frequency.
- Improvement of the disturbance rejection capability of the GFL inverter based on CVD, whose analysis to the best of the authors knowledge has not been found in previous papers.

The rest of the paper is organized as follows. Section II presents the description of the system and the problem definition. Section III is dedicated to the development of the proposed control strategy. The experimental results are presented in Section IV. Finally, Section V concludes this paper.

II. SYSTEM DESCRIPTION AND PROBLEM DEFINITION

The topology of a GFL inverter with LCL filter and current loop is shown in Fig. 1, where v_{dc} is the dc-link voltage, v_g is the grid voltage, v_c is the capacitor voltage, i_g is the grid-side current, i_c is the capacitor current, v_{pcc} is the voltage at the PCC, L_1 is the converter-side inductance, C is the filter capacitance, L_2 is the grid-side inductance, and R_1 and R_2 are the equivalent series resistance (ESR) of L_1 and L_2 , respectively. The grid inductance is represented by L_g . The i_g is controlled by a PR controller $G_i(s)$ and uses AD and CVD. A Phase-locked loop (PLL) is used to obtain the phase angle (θ) of the voltage at the PCC and to keep i_g at a specific phase with respect to v_{pcc} . The current reference is given by I^* . The i_c is fed back through the active damping function $G_{ad}(s)$ and v_c is decoupled through a function of $G_{cva}(s)$ to improve the disturbance rejection capability of the GFL inverter. The system parameters shown in Fig. 1 are listed in TABLE I.

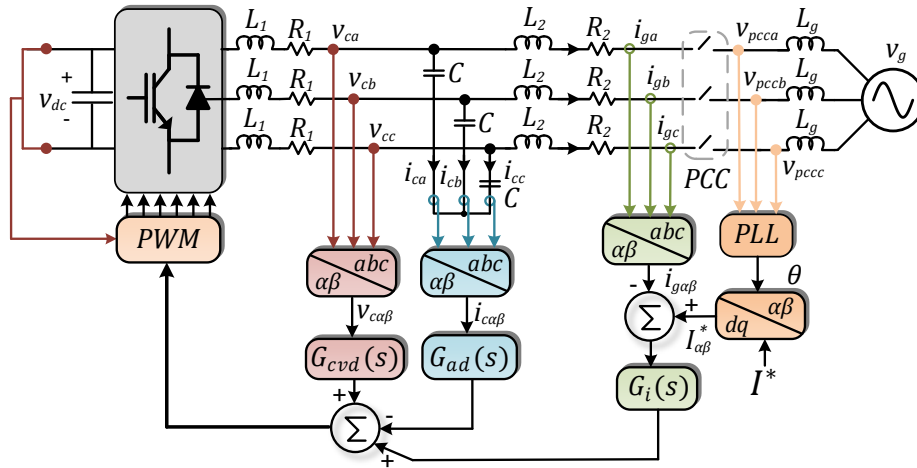


Fig. 1 Three-phase GFL inverter.

The closed-loop control block diagram of the system depicted in Fig. 1 is shown in Fig. 2. Being the computational and PWM time delay represented as $G_d(s)$ in Fig. 2 and it is given by (1) [9].

TABLE I SYSTEM PARAMETERS

Parameter	Value
DC-link voltage (v_{dc})	300 V
Grid line voltage (RMS) (v_g)	110 V
Grid frequency (f_g)	60 Hz
Inductor (L_1)	1 mH
Inductor (L_2)	300 μ H
ESR (R_1)	0.6 Ω
ESR (R_2)	0.35 Ω
Capacitor (C)	15 μ F
Sampling frequency (f_s)	10 kHz
Switching frequency (f_{sw})	10 kHz

$$G_d(s) = e^{-1.5T_s s} \quad (1)$$

The value of f_r can be obtained from (2) and it was designed to be between $f_s/6$ and $f_s/2$, based on the values shown in TABLE I.

$$f_r = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \quad (2)$$

When AD is used in digital control systems, it can be considered as a virtual impedance (Z_v) in parallel with C [10]. This impedance Z_v is composed of an equivalent resistor R_{eq} and an equivalent reactance X_{eq} . The equivalent circuit containing R_{eq} and X_{eq} is shown in Fig. 3.

The expression of Z_v is given by (3) [11].

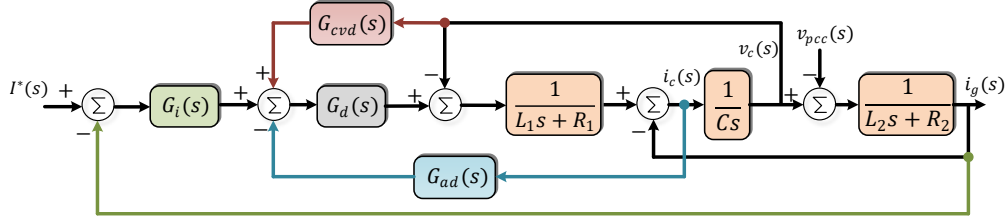


Fig. 2 Closed-loop system control block diagram.

$$Z_v = \frac{L_1}{CK_d} e^{1.5sT_s} \quad (3)$$

Being K_d the proportional gain of AD, in other words, $G_{ad}(s) = K_d$ in this specific case.

Assuming $s = j\omega$ into (3), yields to (4).

$$Z_v(j\omega) = \frac{L_1}{CK_d} \cos(1.5\omega T_s) + j \frac{L_1}{CK_d} \sin(1.5\omega T_s) \quad (4)$$

From (4), the expressions of $R_{eq}(\omega)$ and $X_{eq}(\omega)$ are deduced as (5) and (6), respectively.

$$R_{eq}(\omega) = \frac{L_1}{CK_d \cos(1.5\omega T_s)} \quad (5)$$

$$X_{eq}(\omega) = \frac{L_1}{CK_d \sin(1.5\omega T_s)} \quad (6)$$

Fig. 4 shows the frequency response curves of R_{eq} and X_{eq} , and it is noticed that there is a region between $f_s/6 < f < f_s/2$ where the value of R_{eq} is negative. It can also be noticed that X_{eq} is inductive in the range $f < f_s/3$ and capacitive in the range $f_s/3 < f < f_s/2$. This negative resistance is undesirable, as it leads to the insertion of open-loop unstable poles at the current loop [12].

Once the problem has been defined, it is necessary to extend the positive damping region to avoid instability, and consequently the unwanted operation of the converter. The next section will present the control strategy proposed in this paper to solve the aforementioned problem, as well as a way to increase the bandwidth of the current controller and the disturbance rejection capability of the GFL inverter.

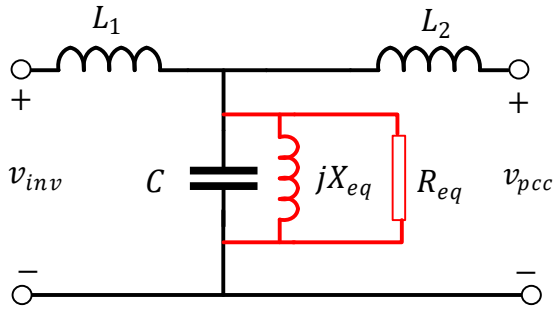


Fig. 3 Equivalent circuit of Z_v .

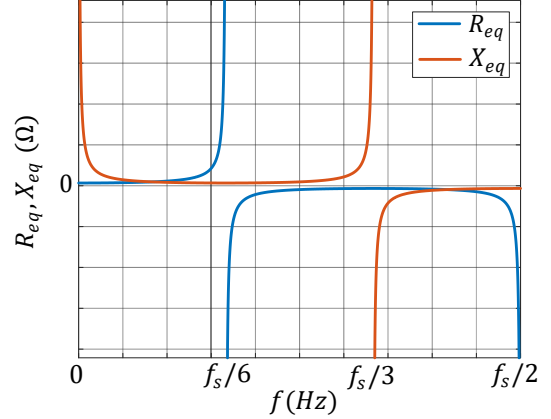


Fig. 4 Frequency response of R_{eq} and X_{eq} .

III. PROPOSED CONTROL STRATEGY

A. Current Controller Design

It is used a PR controller to control the injected current i_g , and its function is given by (7).

$$G_i(s) = R_a G_L(s) + \frac{K_{ri}s}{s^2 + \omega_o^2} \quad (7)$$

Being R_a the proportional gain, K_{ri} the resonant gain and ω_o is the grid nominal frequency in rad/s.

The function $G_L(s)$ is the lead compensator to diminish the effects of the computational delay and has the form of (8).

$$G_L(s) = \frac{k_1s + k_2}{k_3s + k_4} \quad (8)$$

As the system is controlled in the discrete-time domain, the lead compensator proposed in [13], $G_L(z)$, will be used. Its function is given by (9) and K_L is the lead gain.

$$G_L(z) = \frac{1}{1 + K_L z^{-1}} \quad (9)$$

To facilitate the tuning of R_a , the LCL filter was approximated by a L filter, being the total inductance value corresponding to the sum of L_1 and L_2 , and the total ESR value corresponding to the sum of R_1 and R_2 . Fig. 5 shows the closed-loop block diagram to control i_g . The plant parameters, a and b , are given by (10) and (11), respectively:

$$a = e^{-(R_1+R_2/L_1+L_2)T_s} \quad (10)$$

$$b = (1 - a)/(R_1 + R_2) \quad (11)$$

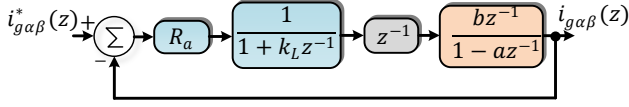


Fig. 5 Closed-loop block diagram for the current loop.

The closed-loop transfer function referring to Fig. 5 is shown in (12) and the poles of this function must satisfy the relation in (13):

$$G_L(z) = \frac{R_a b}{(z + K_L)(z - a) + R_a b} \quad (12)$$

$$\begin{aligned} (z - p_1)(z - p_2) &= (z + K_L)(z - a) + R_a b \\ &\rightarrow z^2 - (p_1 + p_2)z + p_1 p_2 \\ &= z^2 + (K_L - a)z - K_L a + R_a b \end{aligned} \quad (13)$$

Being p_1 and p_2 the closed-loop dominant poles. Equating the two sides of the equation, it is possible to obtain the parameters K_L and R_a according to (14) and (15), respectively:

$$K_L = a - (p_1 + p_2) \quad (14)$$

$$R_a = (p_1 p_2 + k_L a)/b \quad (15)$$

The desired location of $p_{1,2}$ is given by (16) and the damped natural frequency ω_d is given by (17). The damping factor and the natural frequency are represented by ξ and ω_n , respectively.

$$p_{1,2} = e^{-\xi \omega_n T_s} [\cos(\omega_d T_s) \pm j \sin(\omega_d T_s)] \quad (16)$$

$$\omega_d = \omega_n \sqrt{1 - \xi^2} \quad (17)$$

The bandwidth of the current controller was chosen to be equal to 2 kHz, so that $\xi = 0.9$ and $\omega_n = 2\pi 1650$ rad/s. In TABLE II are presented the gains of the current controller. The resonant part of the current controller is discretized with the Impulse Invariant method to obtain the discrete-time implementation, since this method is the most optimal and its zero distribution causes less phase lag for high frequencies [14]. The gains $k_1 = 1.285$, $k_2 = 2.57 \cdot 10^4$, $k_3 = 1$, $k_4 = 3.14 \cdot 10^4$ were obtained with the MATLAB and they will be considered in the analysis to be shown later.

TABLE II CURRENT CONTROLLER GAINS

Gain	Value
Proportional gain (R_a)	4.86
Resonant gain (K_{ri})	1000
Lead gain (K_L)	0.22

B. AD Design – Capacitor current feedback

One of the ways to avoid the resonance effect is to increase the positive damping region and, in this way, guarantee the stability of the GFL inverter even under grid impedance variation. The proposed alternative was to feed back the filter capacitor current and pass it through a first-order lead

compensation, being this function has been tuned around the LCL filter f_r . The transfer function of $G_{ad}(s)$ is shown in (18), where τ_z and τ_p are the gains and the first one must be bigger than the second.

$$G_{ad}(s) = \frac{1 + \tau_z s}{1 + \tau_p s} \quad (18)$$

Fig. 6 shows the frequency response of $G_{ad}(s)$, being the gains τ_z and τ_p tuned to provide phase lead around the f_r of the LCL filter, and the calculated values are $\tau_z = 1.73 \cdot 10^{-4}$ and $\tau_p = 1.73 \cdot 10^{-5}$. These gains were designed to provide the largest phase lead around f_r based on the parameters shown in TABLE I, and even if there is a grid impedance variation, $G_{ad}(s)$ will still provide enough phase lead around the frequency range of interest.

The function $G_{ad}(s)$ was discretized utilizing the Tustin method to obtain the discrete-time implementation, since it was with this method that the best approximation between the continuous and discrete time domain was obtained.

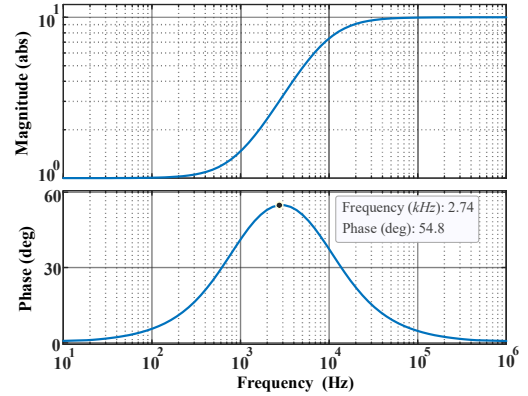


Fig. 6 Frequency response of $G_{ad}(s)$.

C. CVD Design

To make it possible to analyze the disturbance rejection capability of the GFL inverter, initially, it is necessary to obtain an expression that represents the converter output impedance $Z_o(s)$, and we can get it after making several simplifications in the block diagram shown in Fig. 2. Fig. 7 shows the simplified block diagram.

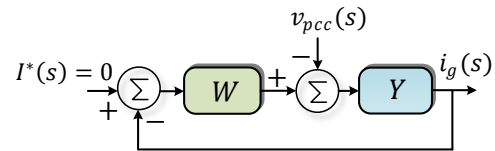


Fig. 7 Simplified block diagram to obtain $Z_o(s)$ expression.

The functions W and Y are given by (19) and (20), respectively.

$$W = \frac{a_0}{a_1 s^2 + a_2 s + a_3} \quad (19)$$

$$Y = \frac{a_1 s^2 + a_2 s + a_3}{b_1 s^3 + b_2 s^2 + b_3 s + b_4} \quad (20)$$

The coefficients are as follows: $a_0 = G_i(s)G_d(s)$, $a_1 = L_1C$, $a_2 = C(R_1 + G_{ad}(s)G_d(s))$, $a_3 = 1 - G_{cvd}(s)G_d(s)$, $b_1 = L_1L_2C$, $b_2 = C(L_2R_1 + L_2G_{ad}(s)G_d(s) + L_1R_2)$, $b_3 = L_1 + L_2 - L_2G_{cvd}(s)G_d(s)$ and $b_4 = R_1 + R_2 - G_{cvd}(s)G_d(s)R_2$.

With (19) and (20), $Z_o(s)$ can be expressed as (21).

$$Z_o(s) = \frac{b_1s^3 + b_2s^2 + b_3s + b_4 + a_0}{a_1s^2 + a_2s + a_3} \quad (21)$$

To decouple the effect of v_c , it is proposed to use the function $G_{cvd}(s)$ which consists of a first-order low-pass Butterworth filter in series with a lead compensation, where the latter has the same form as shown in (18), thus, resulting in a lead-lag-compensation.

The gains were tuned to compensate for the delay at the fundamental frequency (60 Hz). The cutoff frequency of the low-pass filter was set equal to 1500 Hz, and this value was chosen as a trade-off between stability and improved disturbance rejection capability. The parameter values are $\tau_z = 1.8041 \cdot 10^{-4}$ and $\tau_p = 3.4354 \cdot 10^{-5}$.

The frequency response of $Z_o(s)$ is shown in Fig. 8 for two cases, 1 - without $G_{cvd}(s)$, i.e. no decoupling of v_c and 2 - the proposed strategy, with $G_{cvd}(s)$ being a lead-lag compensation. It is observed that the disturbance rejection capability of the GFL inverter using the lead-lag compensation is improved when compared to the case that does not decouple the effect of v_c , and analyzing the phase diagram, it is also noted that the system is stable in the whole frequency range according to the passivity theory [15], which it is not valid for the first case.

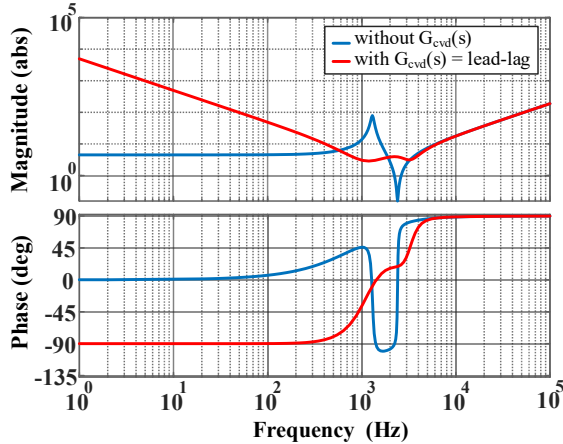


Fig. 8 Frequency response of $Z_o(s)$ without and with $G_{cvd}(s)$.

Fig. 9 shows the frequency response which relates $i_g(s)/v_{inv}(s)$, being $v_{inv}(s)$ the PWM voltages at the terminal of the GFL inverter. It is possible to notice that the system with more damping around f_r is the one that uses the proposed strategy.

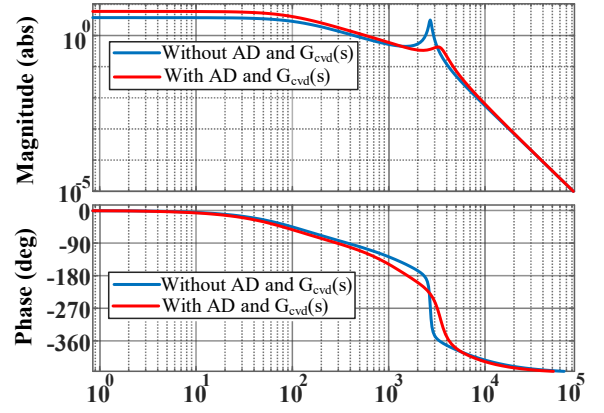


Fig. 9 Frequency response of $i_g(s)/v_{inv}(s)$ for both strategies.

IV. EXPERIMENTAL RESULTS

In order to validate the theoretical development, experimental results were performed in a testbench. Fig. 10 shows the photo of the experimental setup. The grid-simulator Chroma 61830 was used to emulate the electrical grid and it was connected to the GFL inverter through inductors which represented the line impedance. The GFL inverter was controlled by PE-Expert 4 digital control platform using PSIM for coding.

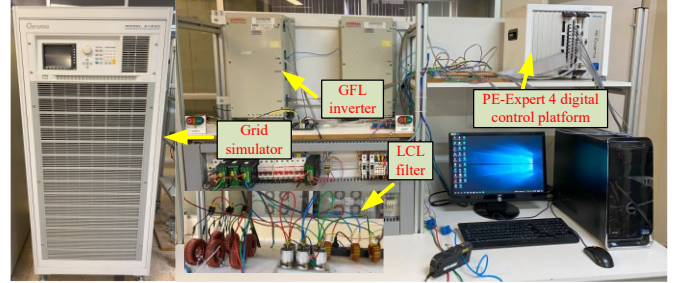


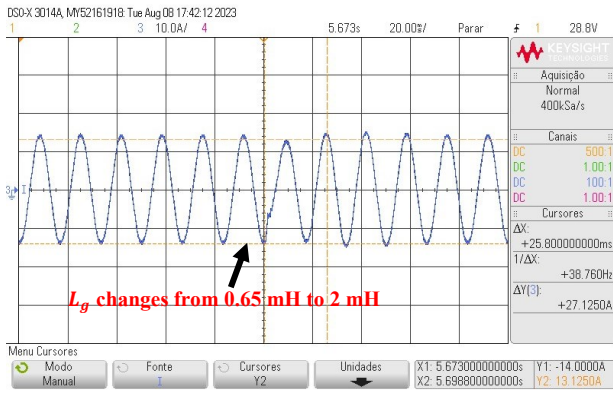
Fig. 10 Experimental setup.

The parameters of the test system were the same as listed in TABLE I. In the following subsections, the GFL inverter operation will be evaluated under two conditions, 1 - grid impedance variation and 2 - disturbance rejection capability. For the first case, it was utilized a circuit breaker to control the insertion or removal of the inductors.

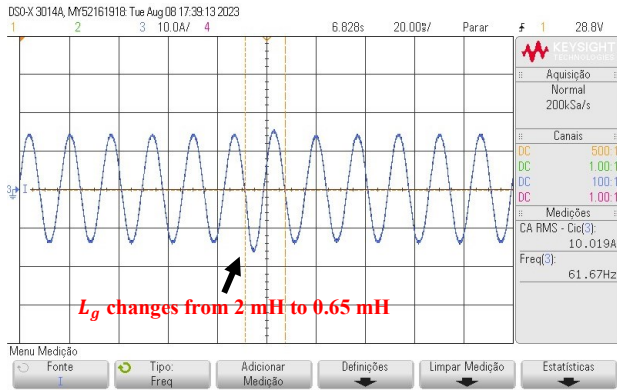
A. Grid impedance variation

Firstly, the current reference value was set to 14 A peak, and a change in L_g was imposed from 0.65 mH to 2 mH, as shown in Fig. 11 (a), and from 2 mH to 0.65 mH, as shown in Fig. 11 (b). These values of L_g were considered since f_r is either greater or less than $f_s/6$ depending on the value of L_g . As can be seen, the GFL inverter control could mitigate the resonance effect, is robust against line impedance variation and remained stable.

In order to see the effectiveness of the AD, it was disabled during the normal operation of the system, and it is noticed in Fig. 12 that the overcurrent protection trips the converter and consequently interrupts its operation.



(a)



(b)

Fig. 11 Grid injected current – phase ‘b’ (a) L_g varies from 0.65 mH to 2 mH; (b) L_g varies from 2 mH to 0.65 mH.

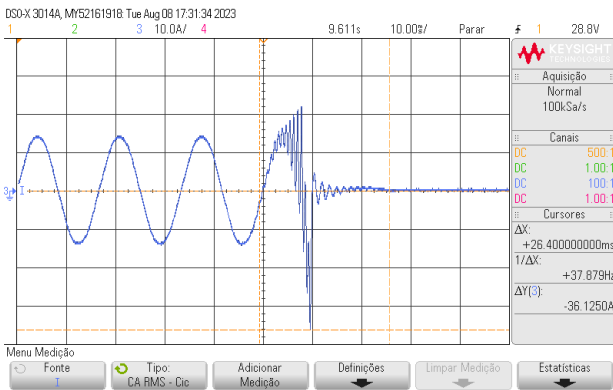


Fig. 12 Overcurrent protection actuation when AD is disabled.

B. Disturbance rejection capability assessment

The next test was performed to assess the effect of G_{cvd} and consequently the disturbance rejection capability of the GFL inverter. For this, it was used the grid simulator to generate distorted voltages with the presence of the 5th and 7th harmonics, and with a magnitude value equal to 2 % each. Fig. 13 shows one of the line voltages generated by the grid simulator.

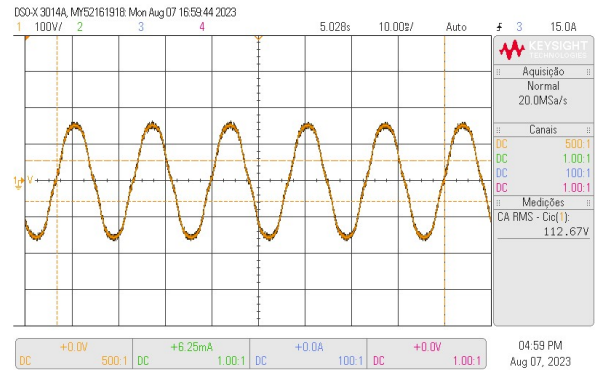
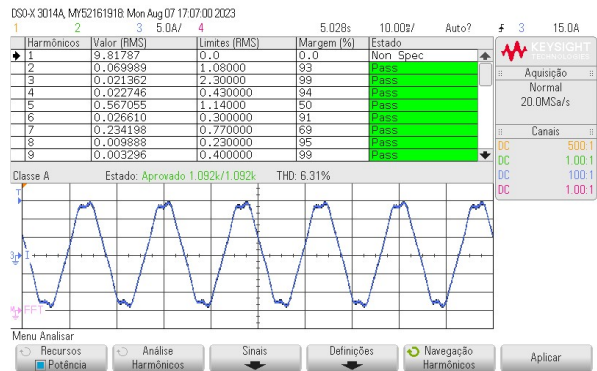
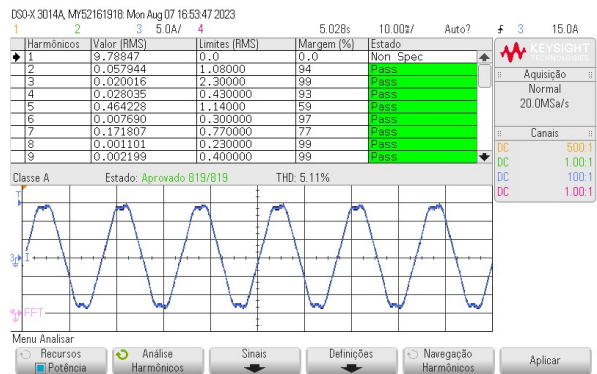


Fig. 13 Grid line voltage with 5th and 7th harmonics.

Fig. 14 (a) - (b) shows i_g in one of the phases, without G_{cvd} and with G_{cvd} being a lead-lag compensator, respectively.



(a)



(b)

Fig. 14 Grid injected current – phase ‘b’ (a) without G_{cvd} ; (b) with G_{cvd} = lead-lag.

According to Fig. 14, the lowest current total harmonic distortion (THD) was obtained with the proposed strategy, i.e., with the use of G_{cvd} as a lead-lag compensator, proving the improvement in the disturbance rejection capability of the GFL inverter in the face of distorted grid voltages.

V. CONCLUSIONS

This paper presented a control strategy for grid-following inverters based on active damping using capacitor current feedback. With this strategy, it was possible to mitigate the effect of the resonance, inherent in *LCL* filters and to increase the disturbance rejection capability of the inverter due to the presence of harmonics in the grid voltage using a lead-lag compensator to perform capacitor voltage decoupling, which proved to be superior to the case when no type of decoupling is performed.

ACKNOWLEDGMENT

The authors would like to thank the Brazil's Higher Education Personnel Improvement Coordination (CAPES – Coordenação de Aperfeiçoamento de Pessoal de Nível Superior-Brasil), Federal University of Maranhão (UFMA), Equatorial Energia S.A and Technical University of Denmark (DTU) for the support to the development of this work.

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