Current Controller for LCL-Type Grid-Following Inverter with Active Damping and Capacitor Voltage Decoupling

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Current Controller for *LCL*-Type Grid-Following Inverter with Active Damping and Capacitor Voltage Decoupling

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***Abstract*—This paper proposes a current control strategy for grid-following inverters interfaced into the grid through *LCL* filters. It is proposed to utilize a proportional+resonant controller with a lead compensation in series with the proportional gain which allows the inverter to achieve high bandwidth. Furthermore, an active damping scheme with capacitor current feedback is applied to mitigate the adverse effect of the *LCL* filter resonance frequency. Moreover, the concept of capacitor voltage decoupling is utilized to enhance the disturbance rejection capability of the grid-following inverter. Theoretical analysis and experimental results validate the proposed strategy.**

Keywords—grid-following inverter, LCL filter, active damping, disturbance rejection

I. INTRODUCTION

The increasing penetration of renewable energy sources (RESs), mainly photovoltaic and wind power plants, alongside with energy storage systems (ESSs) is reshaping the traditional power systems into one with an increasing presence of electronic power converters (EPCs) (which aims to make the interface between the RESs and the electrical grid). It poses major operational challenges to utility system operators [1]. Usually, the integration of these RES with EPCs results in converters operating as grid-following (GFL) inverters, where their control strategy is generally set to operate at rated output power and to inject it in an energized grid. Normally, a power loop is used to control active and reactive power (P and Q) and to generate the current references for the current control loop, which can use Proportional+Integral (PI) controller in synchronous reference frame or Proportional+Resonant (PR) controller in stationary reference frame. The GFL inverter must be properly synchronized with the ac voltage at the connection point, also known as the point of common coupling (PCC), to regulate the active and reactive power injected into the grid [2].

The electrical grid has voltage harmonics which can jeopardize the proper operation of the GFL inverter, as well as the grid impedance variation that can lead the converter to instability in more extreme situations [3]. In the GFL inverters, a filter is needed to attenuate the switching harmonics generated from pulse-width modulation (PWM). Commonly, either the *L* filter or the *LCL* filter is used [4], with the latter being widely utilized since it can provide better harmonic attenuation with reduced inductance compared to the former [5]. But the LCL filter has the disadvantage of introducing an inherent resonance at the resonance frequency (f_r) with a high resonance peak and a sharp phase step down of -180°, which can lead to unstable operation of the GFL current loop [6]. So, several techniques have been proposed aiming to damping the resonance at f_r, with active damping (AD) being one of the most used solutions.

Considering the time delay equal to 1.5 times the sampling period (T_s), it is known from the literature that the critical frequency is one-sixth of the sampling frequency (f_s) below the Nyquist frequency ($f_s/2$). For digital control systems, a stable grid-side current control can be achieved for the *LCL* filter whether f_r is between one-sixth and half of f_s and below $f_s/6$ for converter-side current control [7]. However, if the grid impedance changes, f_r will also change, and the stable operation of the GFL inverter can not longer be guaranteed.

Several works have been developed aiming to provide positive damping for the resonance problem in *LCL* filters. In [8], the authors propose an admittance shaping scheme based on capacitor voltage feedforward to increase passivity of the output admittance and to suppress grid-current harmonics. In [9], the authors propose a strategy for differential feedback grid-side inductor voltage to realize AD. To do that, a band-pass filter is used in series with lead compensation to feed grid-side inductor voltage. It is also shown that this strategy has better suppression of harmonics compared to traditional methods that implementing differential of state variable.

In this context, this paper presents a control strategy for GFL inverter based on capacitor current feedback AD to mitigate the resonance and provide capacitor voltage decoupling (CVD) to improve disturbance rejection capability. The main advantages of the proposed technique are as follows:

- A current controller with high bandwidth.
- A simple approach based on a first-order function to extend the critical frequency up to the Nyquist frequency.
- Improvement of the disturbance rejection capability of the GFL inverter based on CVD using a lead-lag compensator, when compared to other strategies (without CVD and with CVD as being a constant value), whose analysis to the best of the authors knowledge has not been reported in the literature.

The rest of the paper is organized as follows. Section II presents the description of the system and the problem definition. Section III is dedicated to the development of the proposed control strategy. The experimental results are

presented in Section IV. Finally, Section V concludes the paper.

II. System Description and Problem Definition

A GFL inverter with *LCL* filter and current loop is shown in Fig. 1, where v_{dc} is the dc-link voltage, v_g is the grid voltage, v_c is the capacitor voltage, i_g is the grid-side current, i_c is the capacitor current, v_{pcc} is the voltage at the PCC, L_1 is the converter-side inductance, C is the filter capacitance, L_2 is the grid-side inductance, and R_1 and R_2 are the equivalent series resistance (ESR) of L_1 and L_2, respectively. The grid inductance is represented by L_g. The i_g is controlled by a PR controller $G_i(s)$ and uses AD and CVD. A Phase-locked loop (PLL) is used to obtain the phase angle (θ) of the voltage at the PCC and to keep i_g at a specific phase with respect to v_{pcc}. The current reference is given by I^*. The i_c is fed back through the active damping function $G_{ad}(s)$ and v_c is decoupled through a function of $G_{cvd}(s)$ to improve the disturbance rejection capability of the GFL inverter. The system parameters shown in Fig. 1 are listed in TABLE I.

TABLE I System Parameters

Parameter	Value
DC-link voltage (v_{dc})	300 V
Grid line voltage (RMS) (v_g)	110 V
Grid frequency (f_g)	60 Hz
Inductor (L_1)	1 mH
Inductor (L_2)	300 µH
ESR (R_1)	0.6 Ω
ESR (R_2)	0.35 Ω
Capacitor (C)	15 µF
Sampling frequency (f_s)	10 kHz
Switching frequency (f_{sw})	10 kHz

The closed-loop system control block diagram of the GFL inverter with *LCL* filter, AD and CVD is shown in Fig. 2.

The computational and PWM time delay are represented in Fig. 2 as $G_d(s)$ and it is given by (1) [10].

$$G_d(s) = e^{-1.5T_s s} \tag{1}$$

The f_r is given by (2) and it was designed to be between $f_s/6$ and $f_s/2$, based on the values shown in TABLE I.

$$f_r = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{2}$$

The AD, when implemented in digital control systems, can be considered as a virtual impedance (Z_v) in parallel with C [4]. This impedance Z_v is composed of an equivalent resistor R_{eq} and an equivalent reactance X_{eq}. Fig. 3 shows the equivalent circuit with R_{eq} and X_{eq}.

The expression of Z_v is given by (3) [11].

$$Z_v = \frac{L_1}{CK_d} e^{1.5sT_s} \tag{3}$$

Being K_d the proportional gain of AD, in other words, $G_{ad}(s) = K_d$ for this case.

Making $s = j\omega$ into (3), yields to (4).

$$Z_v(j\omega) = \frac{L_1}{CK_d}\cos(1.5\omega T_s) + j\frac{L_1}{CK_d}\sin(1.5\omega T_s) \tag{4}$$

From (4), (5) and (6) are obtained.

$$R_{eq}(\omega) = \frac{L_1}{CK_d\cos(1.5\omega T_s)} \tag{5}$$

$$X_{eq}(\omega) = \frac{L_1}{CK_d\sin(1.5\omega T_s)} \tag{6}$$

The curves of the frequency response of R_{eq} and X_{eq} are shown in Fig. 4, and it can be seen that there is a region between $f_s/6 < f < f_s/2$ where the value of R_{eq} is negative. It is also noted that X_{eq} is inductive in the range $f < f_s/3$ and capacitive in the range $f_s/3 < f < f_s/2$. This negative resistance leads to the insertion of open-loop unstable poles at the current loop [12]. Therefore, it is necessary to extend the positive damping region to avoid instability. The next section will present the strategy proposed in this paper.

III. Proposed Strategy for the GFL Inverter

A. Current Controller Design

The injected current i_g is controlled by a PR controller and its function is given by (7).

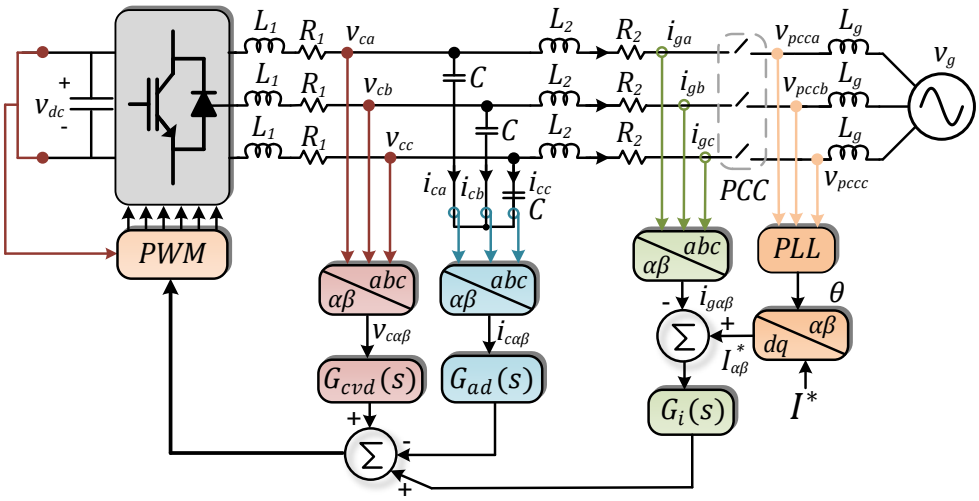


Fig. 1. Three-phase GFL inverter with *LCL* filter.

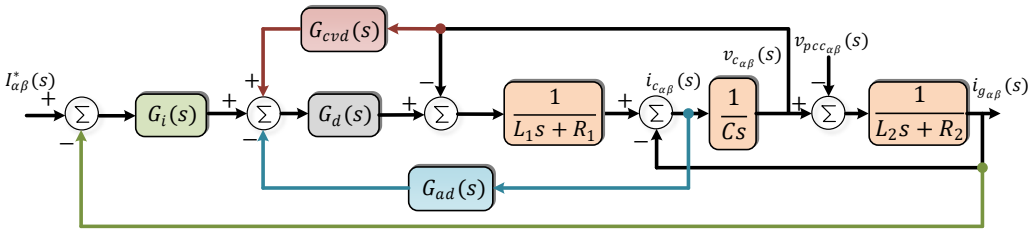


Fig. 2. Closed-loop system control block diagram of the GFL inverter.

$$G_i(s) = R_a G_L(s) + \frac{K_{ri} s}{s^2 + \omega_o^2} \tag{7}$$

Being R_a the proportional gain, K_{ri} represents the resonant gain and ω_o is the grid nominal frequency in rad/s.

The function $G_L(s)$ is the lead compensator to diminish the effects of the computational delay and has the form of (8).

$$G_L(s) = \frac{k_1 s + k_2}{k_3 s + k_4} \tag{8}$$

The system is controlled in the discrete-time domain, therefore the lead compensator proposed in [13], $G_L(z)$, will be used. Its function is given by (9) and K_L is the lead gain.

$$G_L(z) = \frac{1}{1 + K_L z^{-1}} \tag{9}$$

To facilitate the tuning of R_a, the *LCL* filter was approximated by a *L* filter. In Fig. 5, the closed-loop block diagram to control i_g is illustrated. The plant parameters, *a* and *b*, are given by (10) and (11):

$$a = e^{-(R_1+R_2/L_1+L_2)T_s} \tag{10}$$

$$b = (1 - a)/(R_1 + R_2) \tag{11}$$

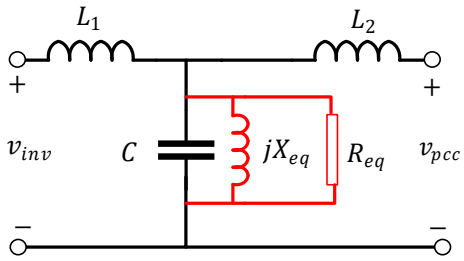


Fig. 3. Equivalent circuit of Z_v.

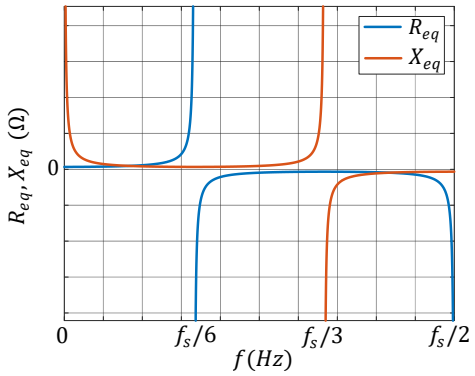


Fig. 4. Frequency response of R_{eq} and X_{eq}.

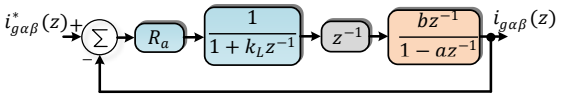


Fig. 5. Closed-loop block diagram for the current loop.

The closed-loop transfer function referring to Fig. 5 is shown in (12) and the poles of this function must satisfy the relation in (13):

$$G_L(z) = \frac{R_a b}{(z + K_L)(z - a) + R_a b} \tag{12}$$

$$\begin{aligned}(z - p_1)(z - p_2) &= (z + K_L)(z - a) + R_a b \\ &\rightarrow z^2 - (p_1 + p_2)z + p_1 p_2 \\ &= z^2 + (K_L - a)z - K_L a + R_a b\end{aligned} \tag{13}$$

Being p_1 and p_2 the closed-loop dominant poles. Equating the two sides of the equation, we can obtain the parameters K_L and R_a in (14) and (15), respectively:

$$K_L = a - (p_1 + p_2) \tag{14}$$

$$R_a = (p_1 p_2 + k_L a)/b \tag{15}$$

The desired location of $p_{1,2}$ is given by (16) and the damped natural frequency ω_d is given by (17). The damping factor and the natural frequency are represented by ξ and ω_n, respectively.

$$p_{1,2} = e^{-\xi \omega_n T_s}[\cos(\omega_d T_s) \pm j \sin(\omega_d T_s)] \tag{16}$$

$$\omega_d = \omega_n \sqrt{1 - \xi^2} \tag{17}$$

The current controller bandwidth was chosen to be equal to 2 *kHz*, so that $\xi = 0.9$ and $\omega_n = 2\pi * 1650$ rad/s. The gains of the current controller are presented in TABLE II. The resonant part of the current controller is discretized with the Impulse Invariant method to obtain the discrete-time implementation, since this method is the most optimal and its zero distribution causes less phase leg for high frequencies [14]. The gains $k_1 = 1.285, k_2 = 2.57 \cdot 10^4, k_3 = 1, k_4 = 3.14 \cdot 10^4$ were obtained with the MATLAB and they will be considered in the analysis to be shown later.

TABLE II CURRENT CONTROLLER GAINS

Gain	Value
Proportional gain (R_a)	4.86
Resonant gain (K_{ri})	1000
Lead gain (K_L)	0.22

B. *Active Damping Design*

As it was presented before, it is necessary to increase the positive damping region and, in this way, guarantee the stability of the GFL inverter even under grid impedance variation. The alternative was to use a first-order lead compensation in the AD implementation, tuned around the *LCL* filter f_r. The transfer function of $G_{ad}(s)$ is shown in (18), where τ_z and τ_p are the gains and the first one must be bigger than the second. Even if there is a grid impedance variation, $G_{ad}(s)$ will still provide enough phase lead around the frequency range of interest.

$$G_{ad}(s) = \frac{1 + \tau_z s}{1 + \tau_p s} \tag{18}$$

Fig. 6 shows the frequency response of $G_{ad}(s)$, being the gains τ_z and τ_p designed to provide phase lead around the f_r of the LCL filter, and the calculated values are $\tau_z = 1.73 * 10^{-4}$ and $\tau_p = 1.73 * 10^{-5}$. These gains were designed to provide the largest phase lead in f_r based on the parameters in TABLE I.

The function $G_{ad}(s)$ was discretized utilizing the Tustin method to obtain the discrete-time implementation, since it was with this method that the best approximation between the continuous and discrete time domain was obtained.

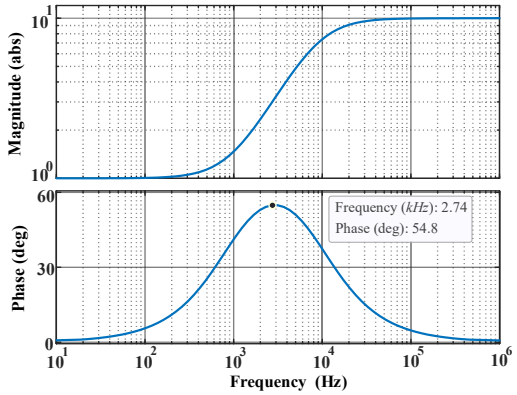


Fig. 6. Frequency response of $G_{ad}(s)$.

C. CVD Design

Making several simplifications in the block diagram shown in Fig. 2, it is possible to obtain an expression that represents the GFL inverter output impedance $Z_o(s)$, which through this it is possible to analyse the disturbance rejection. The simplified block diagram is shown Fig. 7.

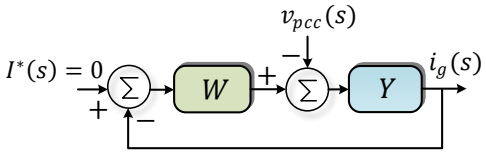


Fig. 7. Simplified block diagram.

Being W and Y given by (19) and (20), respectively.

$$W = \frac{a_0}{a_1 s^2 + a_2 s + a_3} \tag{19}$$

$$Y = \frac{a_1 s^2 + a_2 s + a_3}{b_1 s^3 + b_2 s^2 + b_3 s + b_4} \tag{20}$$

The coefficients are as follows: $a_0 = G_i(s)G_d(s)$, $a_1 = L_1 C$, $a_2 = C(R_1 + G_{ad}(s)G_d(s))$, $a_3 = 1 - G_{ff}(s)G_d(s)$, $b_1 = L_1 L_2 C$, $b_2 = C(L_2 R_1 + L_2 G_{ad}(s)G_d(s) + L_1 R_2)$, $b_3 = L_1 + L_2 - L_2 G_{cvd}(s)G_d(s)$ and $b_4 = R_1 + R_2 - G_{cvd}(s)G_d(s)R_2$.

With (19) and (20), $Z_o(s)$ can be expressed as (21).

$$Z_o(s) = \frac{b_1 s^3 + b_2 s^2 + b_3 s + b_4 + a_0}{a_1 s^2 + a_2 s + a_3} \tag{21}$$

It is proposed to use a lead-lag compensation, $G_{cvd}(s)$, consisting of a first-order low-pass Butterworth filter in series with a lead compensation as shown in (18). The gains are tuned to compensate for the delay at the fundamental frequency (60 Hz). The cutoff frequency of the low-pass filter was set equal to 1500 Hz, and this value was chosen as a trade-off between stability and improved disturbance rejection capability. The parameter values are $\tau_z = 1.8041 \cdot 10^{-4}$ and $\tau_p = 3.4354 \cdot 10^{-5}$. Fig. 8 shows the frequency response of $Z_o(s)$ for three cases, (1) without $G_{cvd}(s)$, i.e. no decoupling of v_c, (2) with $G_{cvd}(s)$ being a constant value equal to 0.9, and (3) with the proposed strategy, with $G_{cvd}(s)$ being a lead-lag compensation. It is observed that the disturbance rejection capability of the GFL inverter using the lead-lag compensation is improved when compared to the other cases, and analyzing the phase diagram, it is also noted that the system is stable in the whole frequency range according to the passivity theory [15], which it is not valid when the decoupling of v_c is not carried out.

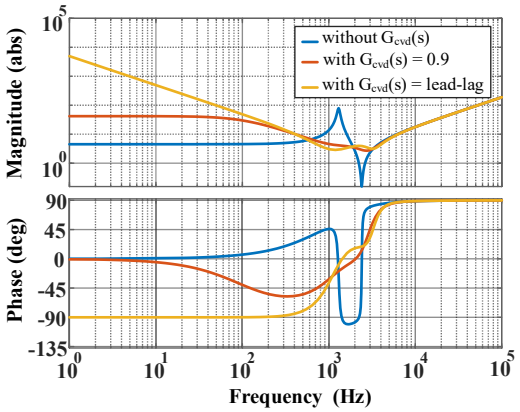


Fig. 8. Frequency response of $Z_o(s)$ considering different strategies.

The lead-lag compensator is discretized utilizing the Tustin method to obtain the discrete-time implementation for the same reason presented in the AD design.

IV. Experimental Results

To validate the theoretical development, experimental results were performed in a lab-test setup. Fig. 9 shows the photo of the experimental setup. The grid-simulator Chroma 61830 was connected to the GFL inverter through grid inductors. The GFL inverter was controlled by PE-Expert 4 digital control platform using PSIM for coding.

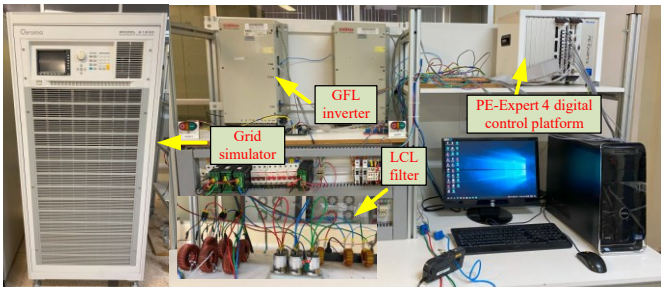


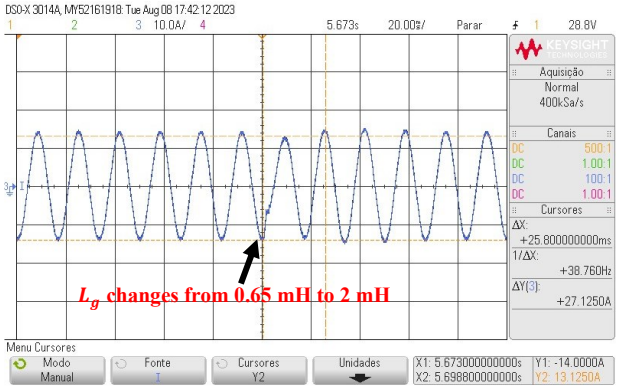
Fig. 9. Experimental setup.

The parameters of the test system were the same as listed in TABLE I. In the following subsections, the GFL inverter operation will be evaluated under two conditions, (1) grid impedance variation and (2) disturbance rejection capability.

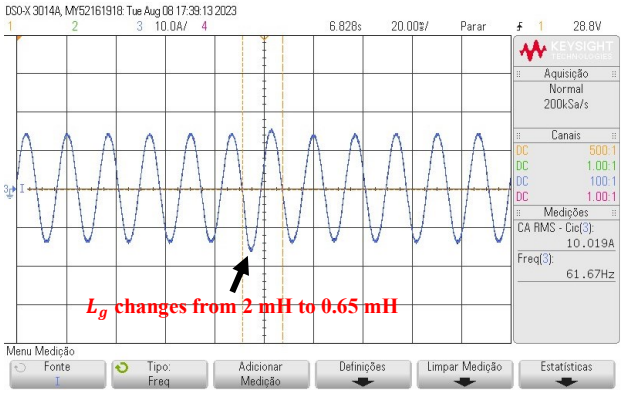
A. Grid impedance variation

The current reference value was set to 14 A peak, and a change in L_g was imposed from 0.65 mH to 2 mH, shown in Fig. 10 (a), and from 2 mH to 0.65 mH shown in Fig. 10 (b). These values of L_g were considered since f_r is either greater

or less than $f_s/6$ depending on the value of L_g. As can be seen, the GFL inverter control could mitigate the resonance effect, is robust against line impedance variation and remained stable.



(a)



(b)

Fig. 10. Grid injected current – phase 'b' (a) L_g varies from 0.65 mH to 2 mH; (b) L_g varies from 2 mH to 0.65 mH.

In order to see the effectiveness of the AD, it was disabled during the normal operation of the GFL inverter, and it can be seen in Fig. 11 that the overcurrent protection trips the inverter and consequently disables its operation.

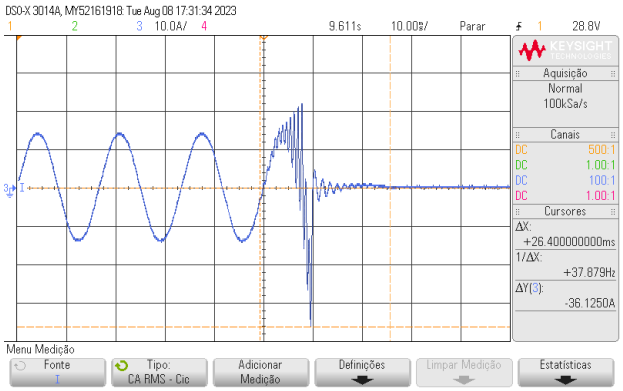


Fig. 11. Overcurrent protection actuation when AD is disabled.

B. *Disturbance rejection capability*

The next test was performed to evaluate the effect of G_{cvd} and consequently the disturbance rejection capability of the GFL inverter. For this, it was used the grid simulator to distort the grid voltage with the presence of the 5th and 7th harmonics, and with a magnitude value equal to 2 % each. Fig. 12 shows one of the line voltages generated by the grid simulator.

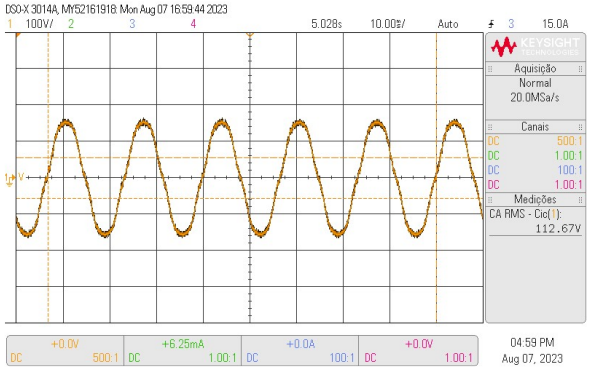
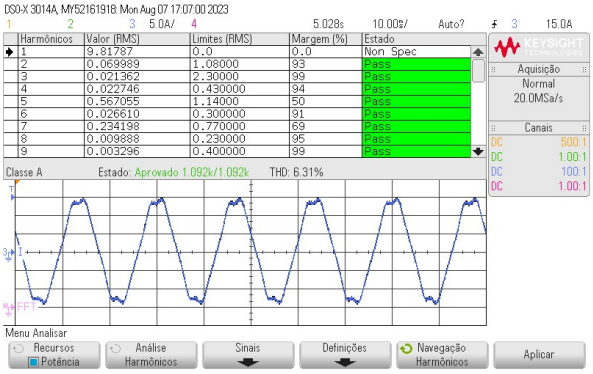
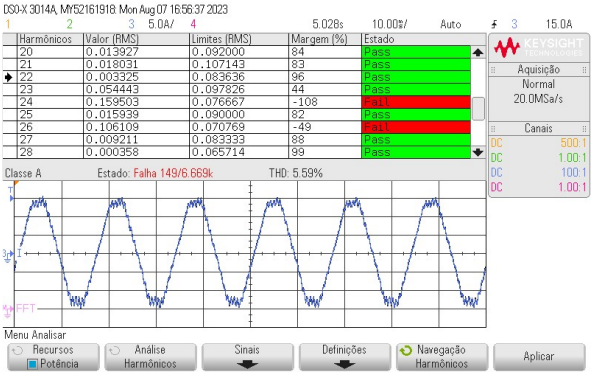


Fig. 12. Grid line voltage with 5th and 7th harmonics.

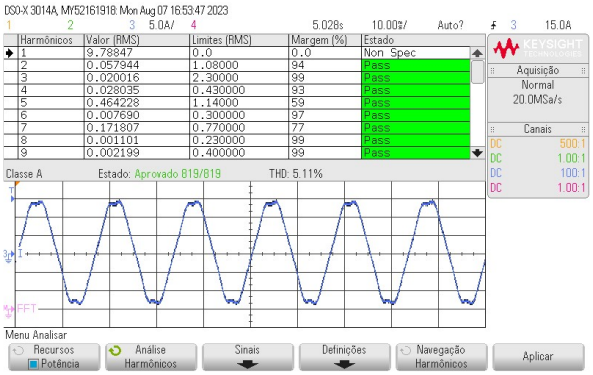
Fig. 13 (a) - (c) shows i_g in one of the phases, without G_{cvd}, with $G_{cvd} = 0.9$ and with G_{cvd} being a lead-lag compensator, respectively.



(a)



(b)



(c)

Fig. 13. Grid injected current – phase 'b' (a) without G_{cvd}; (b) with $G_{cvd} = 0.9$; (c) with G_{cvd} = lead-lag.

As can be seen in Fig. 13 (c), the lowest current total harmonic distortion (THD) was obtained with the proposed strategy (5.11 %), while the THD value was 5.59 % when CVD was used as a constant value (Fig. 13 (b)) and 6.31 % when CVD was not used. In other words, the use of G_{cvd} as a lead-lag compensator improved the disturbance rejection capability of the GFL inverter. It is also noteworthy that when using $G_{dec} = 0.9$, the harmonics of order 24^{th} and 26^{th} did not meet the standards required by the standard IEC 61000-3-2 class-A.

V. Conclusions

This paper presented a control strategy for grid-following inverters based on active damping using capacitor current feedback. With this strategy, it was possible to mitigate the effect of the resonance, inherent in *LCL* filters and to increase the disturbance rejection capability of the inverter due to the presence of harmonics in the grid voltage using a lead-lag compensator to perform capacitor voltage decoupling, which proved to be superior to strategies that decouple this voltage using a constant function or when no type of decoupling is performed.

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