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Nielsen, Ivan Riis

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A Novel SFG Structure for C-T High-Pass Filters

Ivan Riis Nielsen

Abstract—The design of higher order continuous-time filters is often based on the simulation of a corresponding passive prototype filter. Preferably this simulation should use integrators as the basic building block, since integrators generally have very good high-frequency and stability properties. Using the leapfrog signal flow graph (SFG) for the simulation of high-pass filters leads to a differentiator-based structure, so an alternative integrator-based SFG would be convenient. The direct SFG simulation method leads to an integrator-based SFG, but unfortunately its noise properties are relatively poor. This paper presents a new integrator-based SFG structure, which combines good high-frequency properties with good noise properties. A 3.0-kHz sixth-order elliptic high-pass MOSFET-C filter based on the new SFG was fabricated, and measurements that support the theoretical results are presented here.

I. INTRODUCTION

FILTER designs based on the simulation of a passive *LCR* prototype are desirable, since they can be expected to inherit the low-sensitivity properties of their *LCR* prototype. Generally the *LCR* prototype is characterized by some set of state variables X_i (currents and voltages in the *LCR* prototype) that are linked together through so-called state equations of the form

$$X_i(s) = \sum_{k=1}^{n_i} h_{ik}(s) X_{j_{i,k}}(s), \quad i \in [1 \cdots N]. \quad (1)$$

N is the number of state variables, n_i is the number of terms in the i th state equation, and $j_{i,k}$ indicate either a state variable or an input variable X_0 . This combination of variables and transfer functions constitutes a signal flow graph (SFG). If all $h_{ik}(\omega)$ are either constant or integrating, the SFG can be simulated using the integrator of Fig. 1(a), or if all $h_{ik}(\omega)$ are either constant or differentiating, the differentiator of Fig. 1(b). The filters discussed in this paper use the MOSFET-C equivalents [3] of Fig. 1.

The design of low-pass and bandpass filters is often based on the leapfrog method [1] which, in these cases, yields integrator-based structures. If the leapfrog method is used for the design of high-pass filters, then differentiators are required. Differentiators are, however, very difficult to implement with a large frequency range while maintaining stability, so integrator-based structures for implementing high-pass filters are preferred, since integrators generally have very good high frequency and stability properties.

The direct SFG simulation method presented in [2] provides such an integrator-based high-pass filter structure, but unfortu-

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The author is with the Center for Integrated Electronics, Institute of Computer Science, Technical University of Denmark, DK-2800 Lyngby, Denmark.

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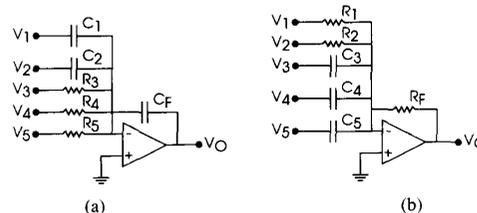


Fig. 1. Basic op-amp-based filter building blocks: (a) integrator and (b) differentiator.

nately it becomes very complex with higher order filters. This paper suggests an alternative integrator-based high-pass filter structure, which will be termed the incremental integration structure. With this new structure, the better properties of the leapfrog method (simplicity and regularity) and the direct SFG simulation method (integrator based) are combined into a new powerful high-pass filter structure.

II. BASIC BUILDING BLOCKS

We will now take a look at the properties of the basic op-amp-based building blocks of Fig. 1, assuming op-amp dc gain A_{DC} , gain-bandwidth product ω_T , and input-referred noise power density $S_{NA}(\omega)$.

The integrator in Fig. 1(a) has two nonintegrating inputs V_1 and V_2 and three integrating inputs V_3 , V_4 , and V_5 . In the general case with n nonintegrating and m integrating inputs, second-order transfer functions can be found (using KCL and a single-pole approximation to the op-amp gain). Assuming two widely spread real poles p_1 and p_2 ($|p_1| \ll |p_2|$), these can be identified from the denominator $D(s) = s^2 - (p_1 + p_2)s + p_1p_2 \approx s^2 - p_2s + p_1p_2$ and we find

$$p_1 \approx \frac{-\sum_{j=n+1}^{n+m} \frac{1}{R_j C_F}}{A_{DC}} = \frac{-\omega_0}{A_{DC}}$$

$$p_2 \approx \frac{-\omega_T}{1 + \sum_{j=1}^n \frac{C_j}{C_F}} = \frac{-\omega_T}{1 + a_0} \quad (2)$$

where ω_0 is the sum of unity-gain frequencies of the integrating inputs and a_0 is the sum of gains of the nonintegrating inputs. Assuming an infinite op-amp gain, the output noise density contributions (resistor and op-amp noise) add up to

$$S_{NO}(\omega) = \frac{4kT\omega_0}{\omega^2 C_F} + \left[\left(\frac{\omega_0}{\omega} \right)^2 + (1 + a_0)^2 \right] S_{NA}(\omega). \quad (3)$$

For integrators, more integrating inputs (larger ω_0) increases the lower band-limit $-p_1$ and increases low-frequency noise,

while more nonintegrating inputs (larger a_0) reduces the upper band-limit $-p_2$ and increases high-frequency noise.

The differentiator in Fig. 1(b) has two nondifferentiating inputs V_1 and V_2 and three differentiating inputs V_3, V_4 , and V_5 . In the general case with n nondifferentiating inputs and m differentiating inputs, second-order transfer functions can be found. Assuming a high- Q complex pole pair $-\sigma_p \pm j\omega_p$, it can be identified from the denominator $D(s) = s^2 + 2\sigma_p s + (\sigma_p^2 + \omega_p^2) \approx s^2 + 2\sigma_p s + \omega_p^2$ and we find

$$\begin{aligned} \omega_p &\approx \sqrt{\frac{\omega_T}{\sum_{j=n+1}^{n+m} R_F C_j}} = \sqrt{\omega_T \omega_0} \\ \sigma &= \frac{1}{2} \left(\frac{\omega_T}{A_{DC}} + \frac{1 + \sum_{j=1}^n \frac{R_F}{R_j}}{\sum_{j=n+1}^{n+m} R_F C_j} \right) \\ &= \frac{1}{2} \left(\frac{\omega_T}{A_{DC}} + (1 + a_0)\omega_0 \right) \end{aligned} \quad (4)$$

where ω_0 is the inverse of the sum of differentiator time constants, and a_0 is the sum of gains of the nondifferentiating inputs. Assuming an infinite op-amp gain, the output noise density is

$$S_{NO}(\omega) = 4kTR_F(1+a_0) + \left[\left(\frac{\omega}{\omega_0} \right)^2 + (1+a_0)^2 \right] S_{NA}(\omega). \quad (5)$$

For differentiators, more differentiating inputs (smaller ω_0) reduces the parasitic pole frequency ω_p and increases high-frequency noise, while more nondifferentiating inputs (larger a_0) increases low-frequency noise.

III. EXISTING HIGH-PASS FILTER SFG'S

The leapfrog filter structure [1] uses the voltages of shunt elements and the currents of series elements as state variables, and the basic state equations for high-pass filters are illustrated in Fig. 2(a). The current $I_{C_{k+1}}$ through C_{k+1} is obtained simply by multiplying the voltage ($V_k - V_{k+2}$) with the admittance (sC_{k+1}). Things are a bit more complicated with the node voltage V_k , that is if the zero producing inductors (L_{k-1} and L_{k+1}) exist; the inductor network is replaced by its Thevenin equivalent, giving constant transfers from the neighboring voltages and a contribution from the current ($I_{C_{k-1}} - I_{C_{k+1}}$) which is multiplied by the Thevenin impedance (sL'_k). Fig. 3(a) shows a full sixth-order elliptic high-pass leapfrog SFG.

The direct SFG simulation method [2] is a general method that will simulate any LCR prototype using integrators and in some cases (including high-pass filters) summing amplifiers. Inductor currents and capacitor voltages are chosen for state variables, and the state equations are illustrated on Fig. 2(b). Inductor currents are obtained by expressing the voltage as

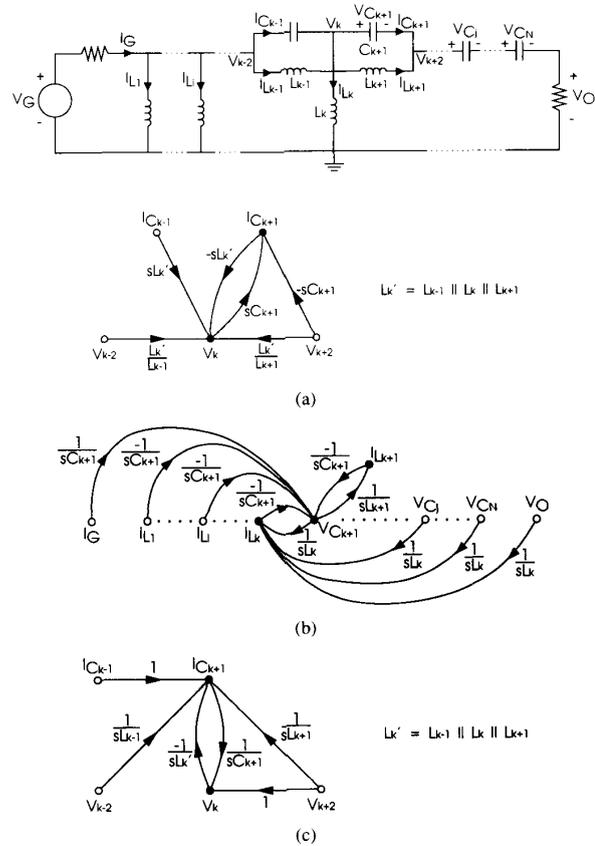


Fig. 2. Basic high-pass SFG sections: (a) leapfrog, (b) direct SFG simulation, and (c) incremental integration.

a linear combination of voltage state variables, and then multiplying by the admittance ($1/sL$). Similarly capacitor voltages are obtained by expressing the current as a linear combination of current state variables, and then multiplying by the impedance ($1/sC$). As we can see, solving a single section in the middle of the ladder requires knowledge of the entire ladder, from generator to load. A full sixth-order elliptic high-pass SFG using the direct SFG simulation method is shown in Fig. 3(b).

IV. THE INCREMENTAL INTEGRATION HIGH-PASS FILTER SFG

The development of a new high-pass filter SFG is motivated by the imperfections of the above-mentioned high-pass filter SFG's. The leapfrog method leads to a differentiator-based structure and this can be expected to cause some stability problems, problems which may be solvable, but no doubt require special actions to be taken. The direct SFG simulation method leads to a relatively complex structure with multi-input integrators and several redundant state variables. This gives an increased circuit complexity and (as will be shown later) increased noise.

The method proposed here attempts to combine the simplicity and regularity of the leapfrog SFG with the application of

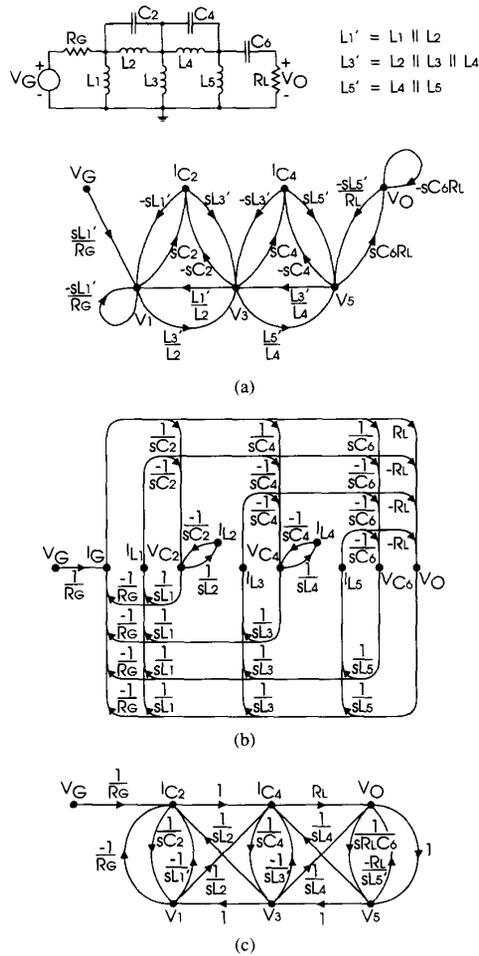


Fig. 3. Sixth-order elliptic high-pass LC prototype and SFG's: (a) leapfrog, (b) direct SFG simulation, and (c) incremental integration.

integrators. The basic element equations to be utilized are

$$V_{Ci} = \frac{I_{Ci}}{sC_i} \quad I_{Li} = \frac{V_{Li}}{sL_i}. \quad (6)$$

The direct SFG simulation method uses the left-hand sides of (6) (V_{Ci} and I_{Li}) as state variables and substitutes I_{Ci} and V_{Li} for linear combinations of state variables. Unfortunately this results in relatively complex equations. Alternatively we can select I_{Ci} and V_{Li} for state variables. What is left is to observe that in the case of high-pass filters, the difference between two consecutive capacitor currents can be expressed as a sum of inductor currents I_{Li} 's, and V_{Ci} equals the difference between two node voltages. The proposed state equations for a single section of a high-pass ladder is illustrated on Fig. 2(c). A capacitor current $I_{C_{k+1}}$ is obtained by subtracting the various inductor currents (V_k/sL_k , etc.) flowing from node k from the previous current $I_{C_{k-1}}$, and a node voltage V_k is obtained by adding a capacitor voltage ($I_{C_{k+1}}/sC_{k+1}$) to node voltage V_{k+2} . With appropriate modifications at the ends of the ladder, this produces the SFG shown on Fig. 3(c). This new approach has been termed the incremental integration method due to the gradual buildup of currents and voltages.

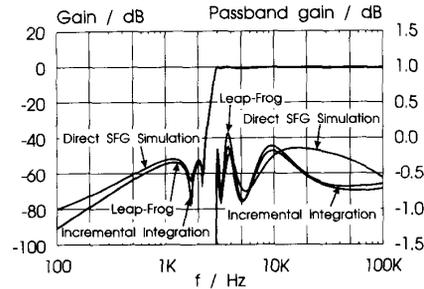


Fig. 4. Simulated gain responses.

V. COMPARISON OF HIGH-PASS FILTER SFG'S

The three different high-pass filter structures on Fig. 3 have been designed with a passband frequency of 3.0 kHz, a passband ripple of less than 1.0 dB, and a stopband attenuation of more than 50 dB. MOSFET-C filters [3] based on these high-pass filter SFG's have been designed and simulated. The filter designs used:

1. Scaled versions of the SFG's; all $X_i(\omega)$ were scaled to have the same maximum.
2. A total capacitance of 500 pF, distributed equally among the integrators/differentiators.
3. Op amps with a dc gain of 74 dB, a unity-gain frequency of 5 MHz, an output impedance of 1.0 k Ω , and input-referred noise level of 20 nV \cdot Hz $^{-1/2}$, and a noise corner of 200 kHz.
4. Resistors with a parasitic capacitance C_p of 0.6 pF/M Ω of resistance R .

The simulated gain responses are shown on Fig. 4. We see that all three circuits meet the required passband ripple and stopband attenuation. In all three cases the original gain responses were seriously distorted by the parasitic capacitances of the resistors. In the leapfrog and direct SFG simulation circuits this problem could be fixed by numerically optimizing selected component values to cancel this distortion. The response of the incremental integration filter was not fixed merely by optimization; voltage scaling was introduced at the integrator inputs having the most significant parasitics.

The incremental integration structure gives a significant spread between the gains of the integrating inputs of each integrator, in the actual case up to a ratio of 12. This means that some of the input resistors should be very large, giving large parasitic time constants. The principle of voltage scaling is illustrated in Fig. 5; a large input resistor R_2 is reduced by preceding it with a low-resistance voltage divider, and with down-scaling factor $n = 3$ the corresponding parasitic time constant is reduced by a factor of $n^2 = 9$. Note that unless n is so large that R_2/n significantly affects the total conductance seen from the summing node, neither resistor noise (3) nor the parasitic poles (2) are significantly affected.

The simulated high-frequency magnitude and phase responses are shown in Fig. 6. These curves show that the leapfrog filter is in fact unstable; the phase is increasing at the two upper parasitic pole frequencies (the peaks on the

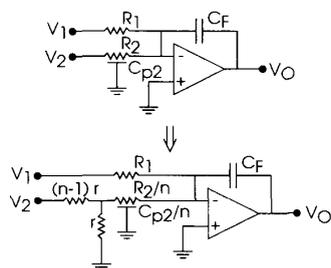


Fig. 5. Reducing resistor parasitics by voltage scaling.

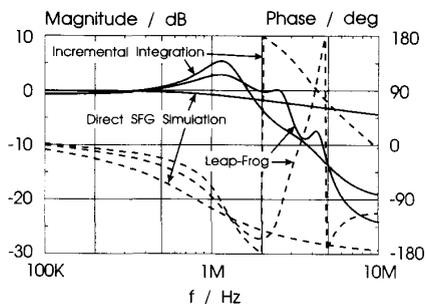


Fig. 6. High-frequency behavior.

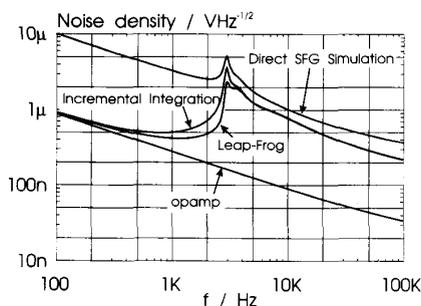


Fig. 7. Simulated noise densities.

magnitude response), so they must be right-half-plane poles. This observation was confirmed by transient analysis.

The simulated output noise densities of the three filters are shown in Fig. 7 together with the input-referred noise density of the op amp. The op-amp flicker noise clearly dominates in the stopband; the noise densities of the leapfrog and incremental integration filters approximate the op-amp noise, while that of the direct SFG simulation filter is approximately 20 dB larger. In the passband the leapfrog and incremental integration filters behave almost identically while the direct SFG simulation filter shows a few more decibels of noise.

The main results of the comparison are summarized in Table I.

VI. CHIP DESIGN

A sixth-order elliptic high-pass filter chip having a passband frequency of 3.0 kHz, a passband ripple of less than

	L-F	D-SFG-S	I-I
Stable	no	yes	yes
Noise 100-100kHz	low 151μV	high 300μV	low 163μV
Opamps	6	10	6

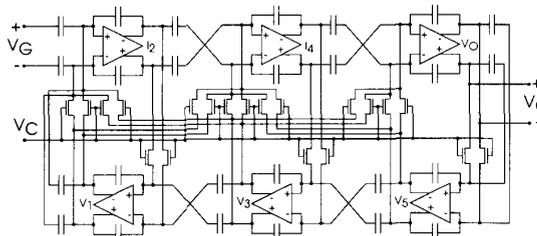


Fig. 8. Incremental integration high-pass filter.

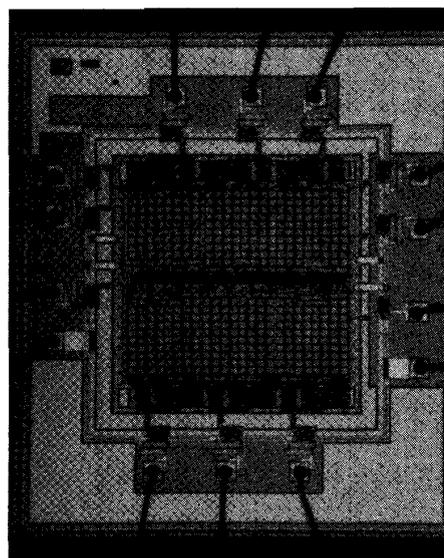


Fig. 9. High-pass filter chip.

1.0 dB, and a stopband attenuation of more than 50 dB was manufactured. The chip contained only the filter, that is no autotuning circuitry was included, and the op amps were Miller-compensated two-stage balanced op amps [4]. A simplified filter schematic without voltage scaling is shown in Fig. 8. The target process was a 2.4-μm analog CMOS process, and the chip core measures 2.9 mm² of which approximately 60% is capacitors. The chip is shown in Fig. 9.

The frequency response of the high-pass filter chip was measured and is shown in Fig. 10, and clearly we have an almost ideal elliptic high-pass response.

The measured noise response is shown in Fig. 11 together with the simulated noise response. As we can see there is a

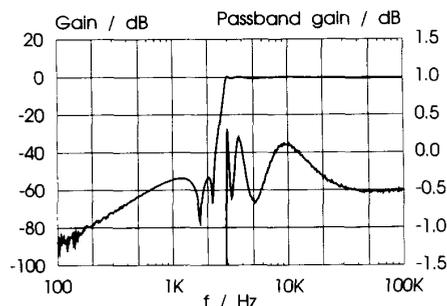


Fig. 10. Measured amplitude response.

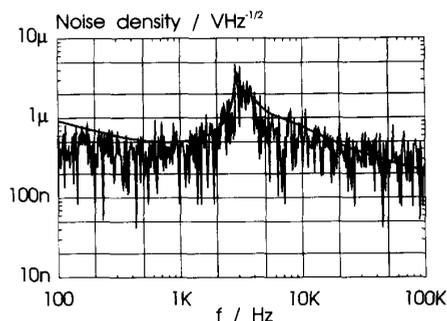


Fig. 11. Measured and simulated noise response.

good correspondence between the two curves, and integrating the measured noise from 100 Hz to 100 kHz gives a total noise voltage of $158 \mu\text{V}$, which should be compared to the simulated $163 \mu\text{V}$.

VII. CONCLUSIONS

A new SFG structure for simulating passive high-pass ladder filters, the incremental integration structure, has been proposed. The structure requires the use of integrators with nonintegrating inputs and an implementation based on the MOSFET-C technique is discussed. The incremental integration structure has been compared to the leapfrog and direct SFG simulation structures. Leapfrog high-pass filters are relatively simple and show good noise properties, but they are based on differentiators and thus stability problems exist. The direct SFG simulation method is based on integrators and has good stability properties, but it leads to a relatively high circuit complexity and a high noise level. However, the incremental integration structure combines the better properties of these two high-pass filter structures; it inherits the low-noise properties of the leapfrog structure and the good stability of the direct SFG simulation method. A sixth-order elliptic high-pass filter chip with a passband frequency of 3.0 kHz has been manufactured and measurements support the conclusions made here.

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