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Hybrid Control Method for a Single Phase PFC using a Low Cost Microcontroller

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***Abstract*- This paper presents a hybrid control method for single phase boost PFCs. The high bandwidth current loop is analog while the voltage loop is implemented in an 8-bit microcontroller. The design focuses on minimizing the number of calculations done in the microcontroller. A 1 kW prototype has been designed and tested.**

I. INTRODUCTION

The use of digital control for power electronics converters is a fast growing field of research. The use of powerful DSPs or FPGAs are common but the added system costs is generally so high that the improvements gained by using digital controls mostly can not justify the added system cost.

The idea of controlling a PFC digitally has been discussed in several papers. The most recent designs are based on a high speed DSP [1, 2] or a FPGA [3] and feature different techniques to eliminate the problem of input current distortion due to the propagation of the output voltage ripple through the feedback circuitry. A different approach to implementing digital control of a PFC is to let the inner control loop which controls the input current be analog while the outer control loop is digital [4]. The design presented in [4] uses an UC3854 for the current loop together with a multiplying DAC to generate the input current reference. The outer loop is implemented in a 80C196 microcontroller.

In this paper a simple hybrid control scheme for a 1 kW PFC based on a boost converter is presented. The design is based on an 8-bit PIC microcontroller and the analog control circuitry is build using cheap standard components. The digital control scheme implemented in the microcontroller utilizes as little as 4.8 % of the microcontrollers computing power.

II. THE HYBRID CONTROL SCHEME

The control scheme proposed in this paper is illustrated in Fig. 1. The control scheme is similar to the control scheme implemented in the analog controller UC3854 with an inner control loop controlling the input current and an outer control loop controlling the output voltage. The input current must be proportional to the input voltage to obtain a power factor close to 1. The voltage loop controls the input power of the PFC by adjusting the amplitude of the input current. To ensure a low distortion of the input current the control signal from the voltage loop must be constant for at least half a period of the input voltage during steady state operation.

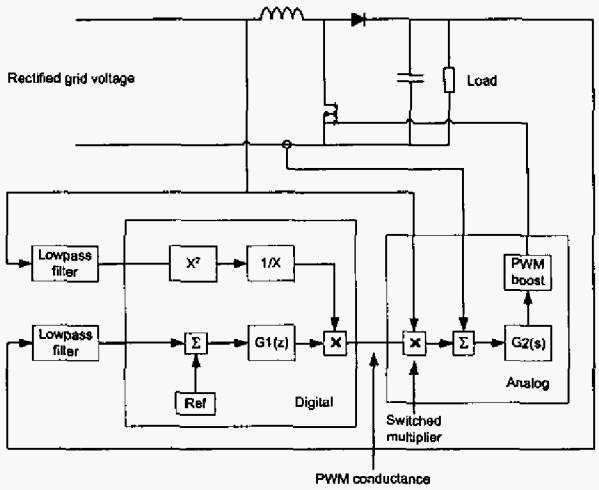

Figure 1 Proposed control scheme for a hybrid control of a PFC

The goal of this design is to use a digital microcontroller in the outer voltage loop. The reason for implementing the voltage loop controller in a microcontroller is to avoid the variations in the gain of the analog hardware multiplier that generates the input current reference signal in devices such as the UC3854 from Texas Instruments.

The implementation in the microcontroller must be optimized for a short execution time and low sampling frequency to minimize the load on the microcontroller. The idea is that the same microcontroller must be able to control a second converter connected to the PFCs output in a purely digital form with a high closed loop bandwidth. The current control circuit is analog because of the high bandwidth (typically 20 kHz) of the current control loop. If the current control is implemented in the microcontroller a sampling frequency of at least 200 kHz is necessary. The input current is controlled using average current mode control.

III. THE CURRENT CONTROL LOOP

The inductor current in the boost converter is controlled using average current mode control. The current is sensed with

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a resistor and compared to the current reference signal. The reference signal for the input current is generated in a switched multiplier (see Fig. 2). The switched multiplier is controlled by the PWM signal 'PWM conductance' generated by the microcontroller.

The gain of the switched multiplier is adjusted by changing the dutycycle, D, of the PWM signal. The low frequency gain of the switched multiplier is

$$G_{sw,mult.} = \frac{v_{ref}(t)}{v_{in}(t)} = \frac{(1-D)\cdot R2}{R1+(1-D)\cdot R2} \qquad (1)$$

The expression for the low frequency gain has been found using circuit averaging over one period of the PWM signal. The lowpass filter on the output of the switched multiplier consisting of R3 and C2 reduces the switching ripple on the input current reference signal. The transfer function of the switched multiplier has two poles both of which are placed at 2.5 kHz. If the poles are placed too low the reference signal will be distorted compared to the rectified grid voltage resulting in increased input current distortion.

The PWM oscillator circuit for the boost converter is synchronized with the 'PWM conductance' signal controlling the switched multiplier to avoid subharmonic oscillations in the current control loop.

IV. THE VOLTAGE LOOP

The design of the voltage loop is based on the model in Fig. 3. Two types of compensators were considered for the voltage loop. The P compensator has the advantage of a faster stepresponse at loadsteps than the PI compensator but has the disadvantage that the output voltage decreases when the load power increases. The higher the proportional gain is the smaller the voltage drop on the output voltage will be with increasing load.

The output capacitor adds - 90° to the phase of the open-loop transfer function of the voltage loop. If a PI compensator is used the total phase is -180° at frequencies below the compensators zero. The system will be unstable if the open-loop gain is larger than 1 and the phase is equal to -180°.

The P compensator was chosen because it is simpler to implement in the microcontroller and thereby utilizes less of the microcontroller's computing power than the PI compensator. Another reason is to avoid the instability of the voltage loop at low frequencies with a PI compensator.

To reduce the distortion of the input current a lowpass filter is added in the feedback of the output voltage. The filter can be either an analog filter on the input of the A/D converter sampling the output voltage or a digital filter implemented in the microcontroller. The advantage of using an analog filter is a low utilization of the microcontroller because the microcontroller doesn't have to complete a filtering algorithm. The advantage of the digital filter is that the filters transfer function doesn't change with the temperature or over time.

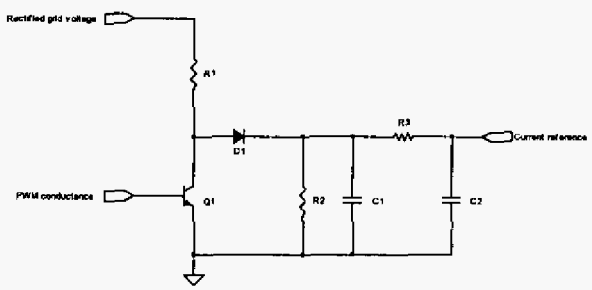

Figure 2 Switched multiplier

An analog first order filter and a digital first order IIR filter were considered in the design of the voltage loop. A description of both kinds of filters is given in the following paragraphs.

A. Analog first order filter

The analog first order filter is easily realised by adding a capacitor in parallel with the bottom resistor in the voltage divider which reduces the output voltage to a level that the microcontrollers A/D converter can measure. A schematic of the analog first order filter is shown in Fig. 4.

The cutoff frequency of the analog filter is placed at 15 Hz leading to a phase margin of 27° and an open loop crossover frequency of 30 Hz for the voltage loop.

B. Digital first order IIR filter

The proposed IIR filter has the transfer function

$$H_{IIR}(z) = \frac{1-a}{1-a\cdot z^{-1}} \qquad (2)$$

The pole/zero plot for the digital filter is shown in Fig. 5. The filter has a zero at the origin and a pole determined by the constant a. The closer a is to 1 the lower the filter's cutoff frequency is.

A simple implementation of the digital filter in the program code for the microcontroller is of great importance to ensure a low utilization of the microcontrollers computing power. The digital IIR filter can realized as shown in Fig. 6.

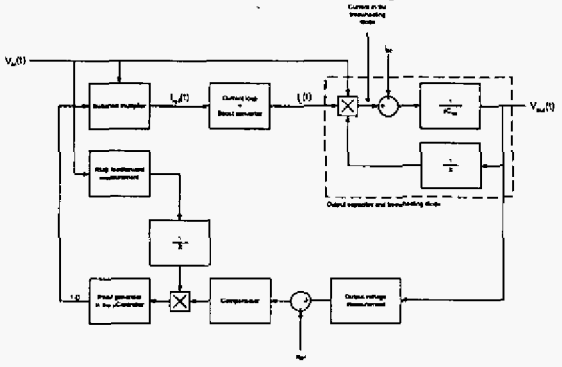

Figure 3 Model of the voltage loop

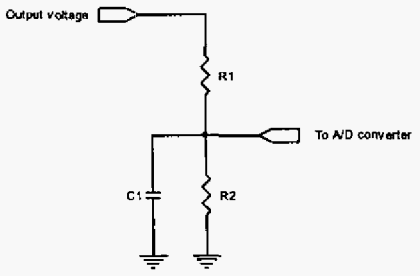

Figure 4 Analog first order lowpass filter

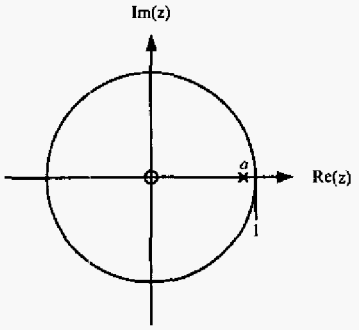

Figure 5: Pole/zero plot for the first order IIR filter

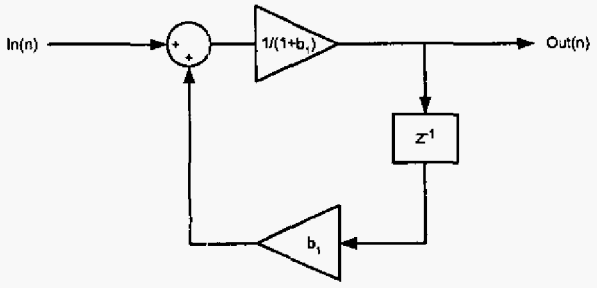

Figure 6 Realization of the digital IIR filter

The factor b_1 in the implementation of the IIR filter is selected as a power of 2 to enable the microcontroller to do the multiplication by shifting routines. The other multiplication is implemented as a division. The placement of the pole of the filter is limited by this implementation but it greatly simplifies the program code for the microcontroller and thereby reduces the utilization of the microcontroller's computing power.

In the final implementation of the voltage loop using the digital filter the pole of the IIR filter has been placed at $a = 8/9$ which results in a phase margin of 24° and a crossover frequency of 24 Hz.

C. Feedforward of the RMS value of the grid voltage

To ensure a constant gain in the voltage loop the control signal on the output of the compensator is divided by the square of the input voltage RMS value. Several methods for calculating the RMS value digitally were considered including methods involving sampling of the input voltage with high or low sampling frequencies. The method chosen is to use an analog second order lowpass filter with two real poles at 15 Hz on the input of the A/D converter measuring the input voltage. The method is chosen because of its simplicity. The filter reduces the rectified grid voltage to a DC voltage proportional to the input voltage RMS value assuming the grid voltage to be a pure sinewave.

V. A/D CONVERTER AND PWM GENERATOR RESOLUTION

The A/D converter and the PWM generator resolution is important in relation to the input current distortion. If the resolution of the dutycycle on the PWM signal controlling the switched multiplier is low the distortion of the input current will be large at low output power. A low resolution results in a large change in the switched multipliers gain if the least significant bit of the dutycycle-register in the PWM generator changes value. The result is a large change in the input power drawn from the grid and as a consequence of this the output voltage may rise or fall more than the deviation from the reference value was before the controller changed the dutycycle on the control signal.

A low resolution in the A/D converter measuring the output voltage will similarly result in quantisation error.

In the implementation of the hybrid control of the PFC in a PIC16F877A microcontroller the resolution of the PWM generator is 9 bits at a switching frequency of 39.1 kHz. The clock-frequency of the microcontroller is 20 MHz. The A/D-converter in the PIC16F877A has a resolution of 10 bits. The actual resolution has been increased by reducing the measuring range to 1/5 of the full input range of the A/D converter.

The resolution of the input voltage RMS value measurement is 8 bits.

VI. DIGITAL HARDWARE AND SOFTWARE IMPLEMENTATION

The following description of the software implementation describes the case where the analog filter is used to filter the feedback signal of the output voltage.

Referring to equation (1) it can be seen that the amplitude of the input current drawn from the utility grid is proportional to $1 - D$ where D is the dutycycle of the PWM signal controlling the switched multiplier. It follows from this that the compensator must calculate $1 - D$. To set the dutycycle in the microcontroller however it is necessary to calculate D. The equation describing the dutycycle of the control signal for the switched multiplier is given in (3).

$$D(n) = D_{\max} - \frac{\left(Ref - v_{out}(n)\right)}{v_{in,RMS}^2(n)} \cdot K_p \qquad (3)$$

where D_{max} is the maximum dutycycle of the PWM signal. The maximum dutycycle is as close to 1 as possible to enable the microcontroller to shut down the PFC. If the dutycycle is equal to 1 the gain of the switched multiplier is zero and the current reference signal will be zero as stated in (1).

The order in which the calculations in equation (3) are done is important for the accuracy of the result. The correct order of calculations is shown in Fig. 7.

The proportionl gain K_p for the prototype designed must be 8500 to obtain a voltage drop of no more than 20V at full load compared to the nominal output voltage of 385V. The gain K_p is a 14 bit number and the resolution of the output voltage measurement is 10 bit. The microcontroller has to do a 16×16 bit multiplication and the result can be limited to a 24 bit number. The execution time of a 16×16 bit multiplication followed by a 24×16 bit division would be quite high for the 8 bit microcontroller PIC16F877A.

Instead of doing the calculations realtime in the microcontroller the resulting dutycycle for every combination of input and output voltage can be stored in a lookup table and read by the microcontroller very fast. Since this solution will be much faster than doing the calculations realtime it has been used in the hardware implementation of the hybrid controlled PFC.

The resulting values of the dutycycle has been calculated and programmed in a 512 kb EPROM that is connected to the PIC16F877A. A flowchart for the interrupt service routine in the PIC16F877A is shown in Fig. 8.

The lookup table has been adapted to the input voltage range of the PFC. If the input voltage is out of range the microcontroller sets the dutycycle to D_{max} to shut down the PFC.

If the voltage loop is realized using the digital IIR filter instead of the analog first order filter an extra block is added to the flowchart in Fig. 8. The filter block is inserted in the flowchart after the measurement of the output voltage and the input voltage.

VII. Test Results

The PFC has been tested with a grid voltage of 230 V_{RMS} and a grid frequency of 50 Hz. The input voltage is an ideal sinewave supplied by an electronic source.

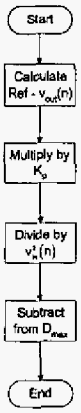

Figure 7 Order of calculations in software

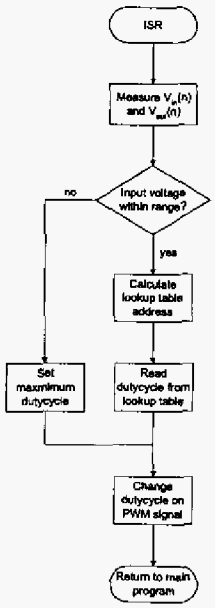

Figure 8 Flowchart for the microcontroller software

Measurements have been performed for both types of filter in the feedback loop of the output voltage.

A plot of the input current at load powers of 100 W and 1 kW respectively can be seen Fig. 10 and Fig. 11 using an analog filter in the output voltage feedback loop. The harmonic content of the input current at 1 kW load power is shown in Fig. 12. The measurement of the harmonic content of the input current shows that the PFC complies with the demands of EN61000-3-2 class A. The rapid changes occurring close to the peak of the input current occurs because the microcontroller samples the input and output voltage and changes the control signal. The input current has a large degree of distortion which is mainly due to quantization errors in the digital implementation of the voltage loop but in a smaller degree to limitations in the analog current loop.

The distortion of the input current is of a different nature than in an analog system because of the hybrid control system. The input current will in theory be proportional to the grid voltage in between samples but will change suddenly directly after an update of the control signal. If the sampling frequency is equal to the grid frequency multiplied by an integer the harmonic spectrum of the input current will only contain odd harmonics of the grid frequency. If the sampling frequency is not equal to the grid frequency multiplied by an integer the spectrum of the input current will have inter-harmonic distortion. The problem of inter-harmonic distortion won't occur at 50 Hz because the sampling frequency has been selected at 500 Hz. If the PFC should operate at 60 Hz it would be advantageous to select a sampling frequency of 600 Hz to avoid inter-harmonic distortion.

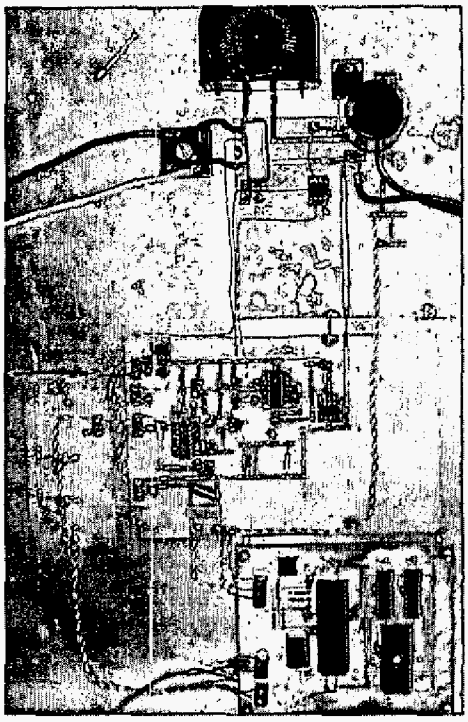

Figure 9 The experimental setup

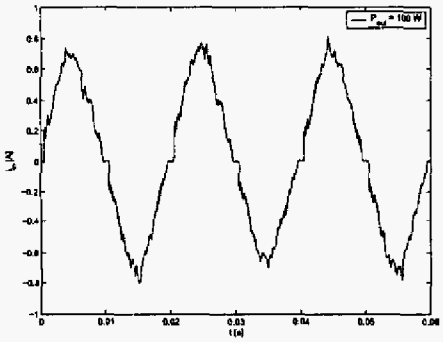

Figure 10 Input current for V_{in} = 230 V_{RMS} and P_{out} = 100 W with the analog filter in the voltage loop

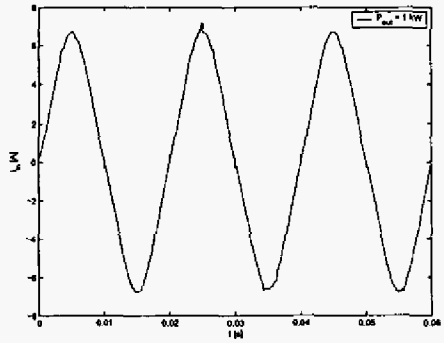

Figure 11 Input current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the analog filter in the voltage loop

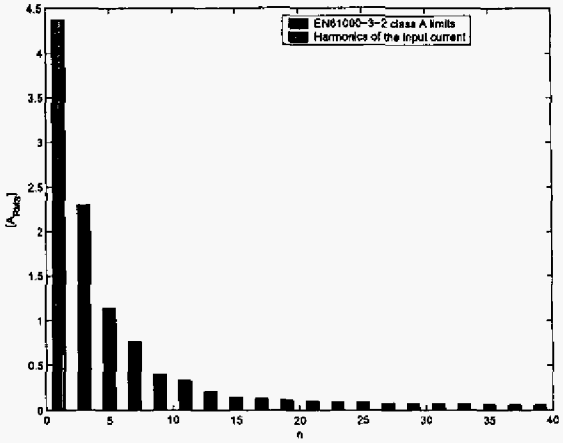

Figure 12 Harmonic content of input current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the analog filter in the voltage loop

Similar measurements of the input current have been performed on the PFC with the digital IIR filter in the voltage loop. The results are shown in Fig. 13 to Fig. 15. The measurements show that the input current is less distorted using the digital IIR filter compared with the analog filter especially at low levels of the output power. The total harmonic distortion at 1 kW is practically the same using the two different filters although the amount of third harmonic distortion is lower using the digital IIR filter.

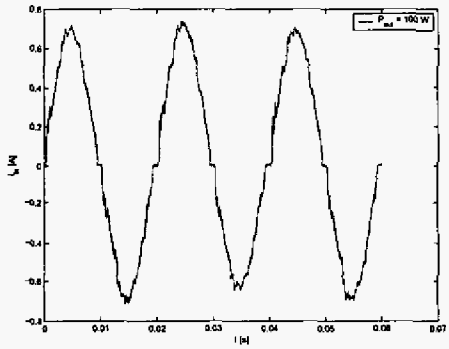

Figure 13 Input current for V_{in} = 230 V_{RMS} and P_{out} = 100 W with the digital IIR filter in the voltage loop

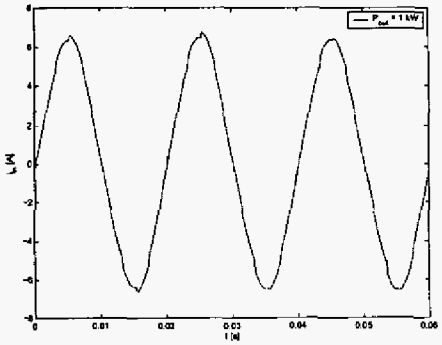

Figure 14 current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the digital IIR filter in the voltage loop

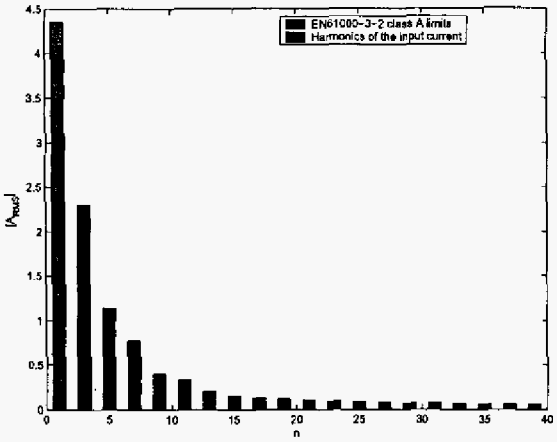

Figure 15 Harmonic content of input current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the digital IIR filter in the voltage loop

The dynamic response of the PFC at a loadstep has been measured with an electronic load (see Fig. 16 and Fig. 17). The electronic load draws a constant current which explains the ripple on the plot of the output power. The steady state output voltage at 100 W was 389 V and at 1.0 kW it was 367 V with both the analog and the digital IIR filter in the voltage loop.

The overshoot and undershoot of the output voltage is smaller with the analog filter than with the digital IIR filter which is due to fact that the phase margin of the voltage loop is higher with the analog filter. The settling time after a step is similarly shorter with the analog filter which can also be explained by the higher phase margin.

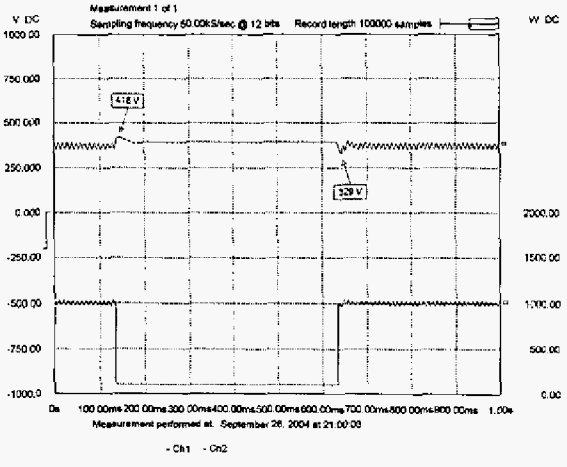

Figure 16 Stepresponse between 100 W to 1.0 kW output power with the analog filter in the voltage loop

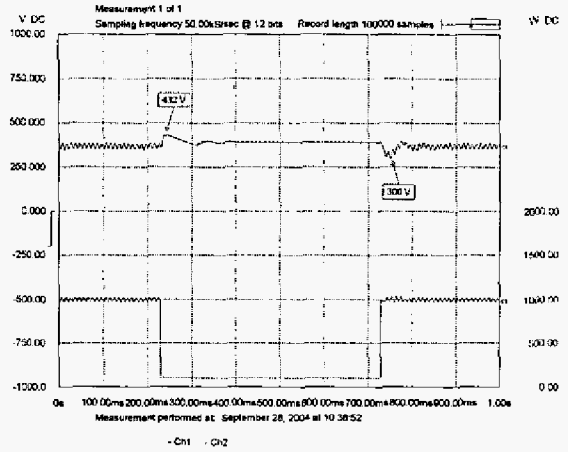

Figure 17 Stepresponse between 100 W to 1.0 kW output power with the digital IIR filter in the voltage loop

VIII. CONCLUSIONS

The proposed hybrid control scheme has been shown to give satisfactory test results. The harmonic distortion is low and the dynamic response of the designed PFC is equal to similar analog controlled PFCs. The utilization of the microcontroller is very low. The disadvantages of the design are a large EPROM used as a lookup table and the issue of inter-harmonic distortion if the sampling frequency doesn't equal the grid frequency multiplied by an integer.

A cheaper implementation of the proposed hybrid control scheme could be realized by leaving out the lookup table and using a microcontroller with a lower pincount e.g. a PIC12F683 microcontroller from Microchip.

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