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A 4 Gb/s 2-Level to 2 Gsymbol/s 4-Level Converter GaAs IC for Semiconductor Optical Amplifier QPSK Modulators

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Abstract—The design of a 50 Ω impedance matched two-to-four level converter GaAs IC for two-electrode semiconductor optical amplifier (SOA) modulators is presented. The designed IC exhibits eye diagrams with eye openings of better than 0.30 V and a spacing between adjacent output signal levels of 0.33 V for output symbol rates of up to 2 Gsymbol/s corresponding to input bit rates of up to 4 Gb/s. A novel differential super buffer output driver is applied, for which output reflection coefficients [S21] of less than -12 dB for frequencies up to 10 GHz are obtained. A 1 Gb/s optical QPSK microwave link transmission experiment using a packaged sample of the designed IC and a two-electrode semiconductor optical amplifier phase modulator has been conducted.

I. INTRODUCTION

New types of microwave systems that require long distance (>20 km) cable-based transmission or extensive signal distribution are now emerging. Examples of such systems are distributed microwave systems for cellular phone networks, feeding of remote antennas and phase array antennas.

A digital optical microwave link is typically based on an analog optical sub-carrier link, where the digitally modulated microwave signal is applied either directly to the laser or an external optical amplitude modulator [1]. However, in systems where long transmission distances, high carrier frequencies, extensive signal distribution or signal processing are required, it may prove advantageous to employ coherent techniques instead [2].

In the coherent optical microwave link presented in this paper the microwave signal is generated from the beat between two-phase locked semiconductor lasers [3]. The Tx laser signal is digitally modulated with the information baseband signal using an external optical phase modulator, which is realized by a two-electrode SOA (see Fig. 1). In addition to a high modulation efficiency, the SOA also provides optical gain [4]. The signal from the CCO laser is transmitted along the fiber link together with the Tx laser signal. The resulting beat signal on an optical front-end will thus generate a conventional phase or amplitude modulated 9-GHz microwave signal. The external optical modulator must accordingly be modulated with a four-level signal, so that an optical phase state is generated for each of the four levels of the driver signal. Further, in order to avoid the unwanted amplitude modulation that is usually associated with SOA phase modulators, it is necessary to use a differentially driven two-electrode SOA [5]. Encoding of binary NRZ input signals into differential four-level signals is therefore an essential part of such an optical QPSK microwave link transmitter.

At gigabit per second bit rates the above described type of driving scheme is not easily implemented using discrete electronics. Thus, in this paper we present a full-custom designed two-to-four level converter GaAs IC, that converts a binary NRZ bit stream to QPSK is performed by the two-to-four level converter GaAs IC in conjunction with the SOA.

II. PRINCIPLE OF OPERATION

The designed two-to-four level convert IC transforms a two-level NRZ bit stream at bit rate B to a corresponding four-level signal at symbol rate B/2 [6]. This two-to-four level converter has been used as driver in the above described optical QPSK microwave link, where generation and transmission of QPSK modulated 3–18 GHz carriers with modulation rates of up to 1 Gb/s are obtained.

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Fig. 2. Block diagram of two-to-four level converter IC.

them simultaneously in parallel form at bit rate B/2 to the
inputs of the two-to-four level encoder. The encoder will then
produce a serial output signal (D4L) at symbol rate B/2
having four different output voltage levels corresponding to
the four possible bit combinations of D1 and D2. All signals
shown in Fig. 2 are assumed to be differential.

The encoder is realized by letting D1 and D2 control a
pair of cross-coupled switches, which share the same resistive
loads but steer currents differing a factor of two in magnitude
as shown in Fig. 3(a). From Fig. 3(a), it is seen that theour possible combinations of switch settings will give four
different sets of voltage drops across the two resistive loads as
shown in Fig. 3(b). The desired encoder function of generating
differential four-level output signals from D1 and D2 is thus
obtained. The 2-b demultiplexer is designed using standard
techniques which can be found elsewhere in literature and will
not be discussed any further here.

III. CIRCUIT DESIGN

The two-to-four level encoder and the output driver are
implemented as being integral parts of each other as shown in
Fig. 4. It is seen that the ideal switches and associated
ideal current sources of the ideal encoder shown in Fig. 3(a)
are replaced by differential amplifiers. Thus, the two-to-four
level encoding is realized using two cross-coupled differential
amplifiers, which differ a factor of two in size but share the
same loads. In this manner, well-defined differential four-level
signals are obtained at the gate of T1 and T2. As mentioned
above, the two-to-four level encoder is implemented as an
integral part of the output driver. This is done in order to
minimize the number of stages succeeding the encoder, and
therefore preserving the well-defined logic levels. The
converter is intended to drive a two-electrode SOA via an
ac-coupled 50-Ω amplifier. However, although the applied
amplifier is impedance matched, the converter outputs should
still be impedance matched in order to reduce reflections
in the final modulator set-up. Therefore the output driver is
implemented as the differential super buffer shown in Fig. 4,
which can be designed to provide 50-Ω output matching while
driving an ac-coupled 50-Ω load [7]. By proper design the
currents through T1 and T2 will stay nearly constant (10 mA)
for the full range of output voltages (2 V ≤ VD4L ≤ 3 V), and
to a first order approximation the output impedance’s will then
be constant and given by the inverse of the transconductances
of T1 and T2.

The current sources supplying the current for T1 and T2
must sink a total current of 20 mA in order to fulfil a goal
of 1 V swing in 50 Ω, and the voltage drop across RL
in the encoder is, of course, proportional to the current through
RL. Thus, in order to obtain the desired output voltage swing
over process and temperature variations the current sources are
controlled via a control voltage CC generated by an on-chip
control circuit (VTO-generator). This control signal CC is also
used in the SCFL gates applied in the 2-bit de-multiplexer
preceding the encoder.

However, since the current through T1 and T2 are made
constant through the control voltage CC, the absolute output
voltage levels will still change with process and temperature
variations due to the change in gate-to-source voltage of T1 and
T2 with process and temperature. It is vital to keep both T1, T2
and the switching FET’s in saturation for the whole output
voltage swing in order to maintain a constant output impedance
during transitions between different output levels. From the
point of view of constant output impedance during switching,
the present design does not allow for any substantial variation
away from nominal output levels. Therefore the control circuit
shown in Fig. 5 has been implemented, which will stabilize the output common mode level against process and temperature variations. The control circuit is based on a downscaled half circuit equivalent to the output driver shown in Fig. 4. Thus $T_3$ and $R_D$ in Fig. 5 relate to $T_1$ and $R_L + R_C$ in Fig. 4. If, for example, the source potential of $T_3$ is higher than the expected nominal value, the current through $T_4$ will increase and thus lower the common mode voltage at the source of $T_1$. Please note in Fig. 5 that the series connection of $R_{C1}$ and $R_{C2}$ replaces $R_C$ in Fig. 4.

The quantitative analysis of the two above-mentioned control circuits is enabled by the manufacturer through a set of model parameters reflecting worst case process spreads. By then using the optimization feature of HSPICE resistor values and transistor widths, for example, the control circuit local to the output driver has been optimized as to minimize the spread in absolute output levels over the given variations in model parameters.

The output reflection coefficients $|S_{22}|$ for the highest and lowest output voltage level have been predicted by circuit simulations using HSPICE as shown in Fig. 6. As it can be seen, the output reflection coefficient is expected to stay below $-14.5$ dB and $-9$ dB for frequencies below 1 GHz and 10 GHz, respectively.

The performance of the developed differential super buffer output driver should be seen in view of the widely accepted open drain interfacing, which in its original form [8] cannot drive ac loads, due to the use of open drain outputs, nor does it employ impedance matching at the output, which necessitates good impedance matching at the receiving end. Creating output matching by placing a $50$-$\Omega$ resistor at the output of the transmitter will double the power dissipation of the output driver, double the size of the output transistors, and double the loading of the preceding stage. This is often not acceptable. As a compromise, designers have placed $100$-$\Omega$ resistors at the transmitting end and have thereby obtained some impedance matching at high frequencies [9], [10] but poor matching at low frequencies. Though the application of the output driver is very specific in our case, the authors believe that the developed differential super buffer output driver has a potential for high-speed impedance matched chip-to-chip interfacing at lower power dissipation than for existing configurations.

The logic gates employed in the 2-b de-multiplexer are designed using Source Coupled FET Logic (SCFL), which fits in naturally with the encoder sub-circuit topology. The final two-to-four level converter design has been processed in TriQuints 0.5-$\mu$m gate length ($F_I = 20$ GHz) DFET only HA process. A microphotograph of the designed two-to-four level converter IC is shown in Fig. 7.

**IV. MEASURED ELECTRICAL PERFORMANCE**

The chips were tested using wafer probing. By applying pseudo-random binary sequence (PRBS) data to the data input $(D_{2L})$ and monitoring the outputs on a sampling oscilloscope correct encoding is observed at input bit rates exceeding 4 Gb/s corresponding to 2 Gsymbol/s at the output (see Fig. 8). At input bit rates exceeding 4 Gb/s, eye diagrams with eye openings of better than 0.30 V are observed (see Fig. 9), but for input bit rates exceeding 4.5 Gbls the eyes are almost closed. The chip operates equally well with outputs dc-terminated to 50 $\Omega$ or ac-terminated to 50 $\Omega$. In both cases spacings between adjacent signal levels are 0.33 V, and the highest and lowest absolute output signal level are measured to be $V_{D4L,max} = 3$ V and $V_{D4L,min} = 2$ V, respectively, as expected from circuit simulations. The output
reflection coefficients \( |S_{22}| \) corresponding to the lowest and highest output signal levels have been measured. They are found to stay below \(-16\) dB and \(-12\) dB for frequencies below 1 GHz and 10 GHz, respectively, as shown in Fig. 10. During operation 300 mA is drawn from each of the \( V_{DD} = 5 \) V and \( V_{SS} = -5 \) V power supplies.

A few devices have been mounted in thin film carriers in order to be able to use them together with the SOA. No additional ringing was observed on the output signals for the mounted devices (Hybrid Integrated Circuits, HIC’s) as compared to the on-chip measurements. This we ascribe mainly to the application of impedance matching. The output reflection coefficients \( |S_{22}| \) for the two-to-four level converter hybrid integrated circuit (HIC) have been measured as shown in Fig. 11. As it can be seen, the output reflection coefficient for the two-to-four level converter hybrid stays below \(-10\) dB for frequencies below 10 GHz.

V. SYSTEM EXPERIMENT

An optical QPSK microwave transmission experiment, as shown in Fig. 1, has been conducted using the two-to-four level converter HIC and a two-electrode SOA phase modulator [11]. For the experiment, the beat between the two semiconductor lasers is phase locked to a 9-GHz microwave reference source, thereby providing a highly stable optically generated carrier at 9 GHz [3]. The QPSK modulation is obtained by modulating the two-electrode SOA with the differential four-level signal from the converter HIC. The bit rate of 1 Gb/s, which corresponds to an output symbol rate of 500 MsymboYs, is limited by the modulation bandwidth of the SOA used in the experiment.

The amplitudes of the real and complementary four-level output signals are adjusted individually as to cancel out the overall unwanted amplitude modulation from the SOA modulator. For the particular SOA applied in this experiment, the individual adjustment means that differential signals with 0.5 V and 1.5 V amplitude with 1 V offset is applied to the two SOA electrodes, respectively. As seen from Fig. 12, the differential modulation scheme results in a high degree of gain flatness of the SOA modulator (better than 1 dB peak-peak), which is an improvement of 3.8 dB when compared to single electrode SOA modulators driven by a single-ended four-level signal [11]. The obtained gain flatness allows for application in practical microwave links. The optically generated QPSK microwave signal has been synchronously demodulated, and the resulting In-phase and Quadrature signals are shown in Fig. 12 (upper traces). The correct encoding and successful demodulation after optical transmission clearly demonstrate the feasibility of differentially four-level driven SOA’s as QPSK modulators in optical microwave links.

VI. CONCLUSION

A two-to-four level converter GaAs integrated circuit for two-electrode semiconductor optical amplifier QPSK modulators has been designed. The designed IC exhibits eye diagrams with eye openings better than 0.3 V, equidistant voltage difference between adjacent output signal levels of 0.33 V and correct encoding is demonstrated at output symbol rates
of up to 2 Gsymbol/s corresponding to input bit rates of up to 4 Gb/s. Good output matching and output level definition have been obtained through a novel output driver design comprising both 2-to-4 level encoding and generation of high-speed 50-Ω matched differential outputs.

An optical QPSK microwave link transmission experiment has been conducted using a packaged sample of the designed IC as driver for a two-electrode SOA QPSK modulator. The differential outputs of the IC together with a differential modulation scheme of the SOA provide a high degree of gain flatness of the optically generated QPSK microwave signal. Demodulation of the optically generated QPSK microwave signal has also been conducted, which clearly demonstrates the feasibility of using the presented two-to-four level GaAs IC and a two-electrode SOA modulator in a coherent optical microwave link.

Though the presented converter IC is designed explicitly for applications in optical QPSK microwave links, the developed encoder circuit principle may also be utilized advantageously in future long distance high-speed optical fiber transmission systems limited by fiber dispersion.

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