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ABOVE 8GHz STATIC T-FLIP-FLOP OPERATION USING $F_T = 22.9$GHz GAAS MESFETS

J. Riishøj* and P. Danielsen*

ABSTRACT

Abstract: A static SCFL Toggle Flip-Flop GaAs IC having maximum operating frequency of $F_{\text{div}} = 8.25$GHz has been designed using a commercially available GaAs MESFET foundry service. The average $F_T$ for the present wafer is $F_T = 22.9$GHz giving a very high $F_{\text{div}}/F_T$-ratio of $F_{\text{div}}/F_T = 0.36$. In addition output voltage transition times of $T_t(20\%-80\%) = 35$ps are obtained by implementation of a novel output driver design.

MOTIVATION

Recently there has been a dramatic progress in the development of ultrahigh-speed frequency dividers, thus maximum frequencies of operation of above 20GHz have been reported. These high performance devices are based on very advanced transistors, such as very short gate SAINT MESFETs (1), HEMTs (2) or HBTs (3). There has hence been a rather intense publishing activity regarding high divider speed obtained through new or refinement of existing processes. We do not have access to such advanced transistors mentioned above but are restricted to use commercially available foundry services. Therefore our approach has been to get maximum performance from the given MESFET process through circuit design. In order to compare with elsewhere reported divider performance we use the $F_{\text{div}}/F_T$-ratio as a figure of merit of, how well a process is utilized. In Table 1 is shown a list of reported performance of static MESFET frequency dividers covering different authors (processes) over the past 14 years, and a grouping in the $F_{\text{div}}/F_T$-ratio of $0.30 < F_{\text{div}}/F_T < 0.33$ seems to be the case.

<table>
<thead>
<tr>
<th>$F_T$</th>
<th>$F_{\text{div}}$</th>
<th>$F_{\text{div}}/F_T$</th>
<th>Year</th>
<th>$L_g$</th>
<th>Author</th>
</tr>
</thead>
<tbody>
<tr>
<td>15GHz</td>
<td>4.5GHz</td>
<td>0.30</td>
<td>1977</td>
<td>1.00μm</td>
<td>HP</td>
</tr>
<tr>
<td>15GHz</td>
<td>5.0GHz</td>
<td>0.33</td>
<td>1982</td>
<td>1.00μm</td>
<td>HP</td>
</tr>
<tr>
<td>23GHz</td>
<td>7.5GHz</td>
<td>0.33</td>
<td>1985</td>
<td>0.55μm</td>
<td>NTT</td>
</tr>
<tr>
<td>60GHz</td>
<td>17.9GHz</td>
<td>0.30</td>
<td>1986</td>
<td>0.20μm</td>
<td>HRL</td>
</tr>
<tr>
<td>35GHz</td>
<td>11.0GHz</td>
<td>0.31</td>
<td>1986</td>
<td>0.50μm</td>
<td>NTT</td>
</tr>
<tr>
<td>32GHz</td>
<td>10.2GHz</td>
<td>0.32</td>
<td>1988</td>
<td>0.40μm</td>
<td>NTT</td>
</tr>
<tr>
<td>49GHz</td>
<td>16.0GHz</td>
<td>0.33</td>
<td>1989</td>
<td>0.50μm</td>
<td>OKI</td>
</tr>
<tr>
<td>74.3GHz</td>
<td>26.8GHz</td>
<td>0.36</td>
<td>1989</td>
<td>0.15μm</td>
<td>NTT</td>
</tr>
<tr>
<td>22.9GHz</td>
<td>8.25GHz</td>
<td>0.36</td>
<td>1991</td>
<td>0.50μm</td>
<td>CBT</td>
</tr>
</tbody>
</table>

Table 1: Reported performance of static dividers based on GaAs MESFETs.

DEVICE CHARACTERISTICS

We have used Anadigics GaAs foundry service. They offer a 0.5μm gate length MESFET process. According to the PCM data for our wafer the MESFETs have a pinch-off voltage of $V_p = -0.8$V, an ac transconductance of $G_m = 189$ms/mm, a saturation current of $I_{dss} = 140mA/mm$ and an average unity current gain frequency of $F_T = 22.9$GHz. $F_T$ is calculated as $F_T = G_m/2\pi C_{gs}$ at $V_{ds} = 2.5$V and $V_{gs} = 0$V.

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4-PHASE GENERATOR

Designers of e.g. high-speed multiplexers and demultiplexers may need 4 timing signals at half the clock rate shifted 0, 90, 180 and 270 degrees, respectively, instead of just a single signal at half the clock rate (4)(5). This lead to the divider configuration shown in Fig.1, where we use a Master-Slave D-Flip-Flop (MS D-FF) with the usual feed-back connections and take M, S and the corresponding complementary signals as output signals thus generating the desired 4 timing signals.

![Fig 1: 1/2 frequency divider configuration](image1)

SCFL 1/2 FREQUENCY DIVIDER

Both the master and the slave latch are realized using the well known SCFL two-level logic structure shown in Fig.2. Gate width scaling factors are chosen in such a manner, that all FETs are kept in good biasing conditions during the full logic swing, that is, switching FETs are operating near the peaking in the unity current gain frequency $F_T$ during switching, and the source follower input FETs are operating near the peaking in the transconductance $G_m$.

![Fig 2: SCFL latch configuration used for both master and slave.](image2)

NOVEL OUTPUT DRIVER DESIGN

In order to achieve short rise and fall times at the output ports we have applied open drain outputs, which is commonly seen for devices operating at or above 5Gbit/s (6)(7). In addition we suggest this differential output stage to be driven by the differential push-pull buffer/amplifier shown in Fig.3. By using this output stage we have achieved very short transition times.
Fig 3: Differential push-pull output driver. Q and M represent input and output signals, respectively.

MEASURED CIRCUIT PERFORMANCE

Circuit performance was measured using a Cascade Microtech probe station. The dual phase input clock signals were generated using an HP microwave generator, a power splitter and a variable delay line. Output signals were monitored on a HP 4 channel sampling oscilloscope and a spectrum analyzer. A maximum toggle frequency of 8.25GHz was obtained at a power dissipation of 740mW and an output voltage swing of 480mV. The corresponding response monitored by a spectrum analyzer is shown in Fig.4 At toggle frequencies above 7.5 GHz the output signal duty cycle drifts rapidly away from 50%, and the output voltage swing and input sensitivity are decreasing, Fig.5, thus adding the requirement for filtering and amplification at clock frequencies above 7.5GHz for most digital applications. However, at clock frequencies below 7.5GHz, e.g. at 5GHz as shown in Fig.6, square-wave like outputs are generated having near 50% duty cycle, app. 800mV amplitude (VOH=0V) and very short transition times, Table 2.

Fig 4: MS-TFF output measured by spectrum analyzer when operating at the maximum input frequency of 8.25GHz.
Fig 5: Input sensitivity (dashed line) and output voltage swing (solid line) as function of input clock frequency.

Fig 6: Measured output signals M,S,NM,NS and corresponding input clock wave-forms when operating on a 5GHz clock. Vertical: 1V/div and Horizontal: 20ps/div.

<table>
<thead>
<tr>
<th>10-90%</th>
<th>20-80%</th>
</tr>
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<tbody>
<tr>
<td>Tr</td>
<td>54ps</td>
</tr>
<tr>
<td>Tr</td>
<td>51ps</td>
</tr>
</tbody>
</table>

Table 2: Measured transition times at 5GHz clock frequency.
CONCLUSION

A 8.25GHz static 1/2 frequency divider IC has been designed using a commercially available 0.5µm gate length GaAs MESFET process with an average $F_t$ across the wafer of $F_t = 22.9$GHz. Thus a high $F_{div}/F_t$-ratio of $F_{div}/F_t = 0.36$ is obtained, which we ascribe to the utilization of the peaking in $F_t$ and $G_m$. Also very short transition times of $T_t(20\%-80\%) = 35$ps are obtained by applying a novel output-driver design, where we use a differential push-pull buffer/amplifier to drive an open drain differential output stage. Power dissipation is 740mW, and the output voltage swing is just above 800mV below toggle frequencies of 7.5GHz decreasing to 480mV at the maximum toggle frequency of 8.25GHz.

REFERENCES

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