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On-chip two-mode division multiplexing using tapered directional coupler-based mode multiplexer and demultiplexer

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Abstract: We demonstrate a novel on-chip two-mode division multiplexing circuit using a tapered directional coupler-based TE₀&TE₁ mode multiplexer and demultiplexer on the silicon-on-insulator platform. A low insertion loss (0.3 dB), low mode crosstalk (< -16 dB), wide bandwidth (~100 nm), and large fabrication tolerance (20 nm) are measured. An on-chip mode multiplexing experiment is carried out on the fabricated circuit with non return-to-zero (NRZ) on-off keying (OOK) signals at 40 Gbit/s. The experimental results show clear eye diagrams and moderate power penalty for both TE₀ and TE₁ modes.

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1. Introduction

On-chip optical interconnections based on silicon-on-insulator (SOI) nanowires are a promising technology for future massively-parallel chip multiprocessors [1]. Compared to traditional copper wire-based electrical interconnects, silicon-based on-chip optical interconnects offer broad bandwidth, allowing to reach very high capacities using the wavelength-division multiplexing (WDM) technology [2]. Mode-division multiplexing (MDM) offers a new dimension to increase the capacity of SOI optical links [3]. The key to realize on-chip MDM is an efficient mode (de)multiplexer. On-chip mode multiplexers based on weakly guiding asymmetrical Ψ - and Y- junctions have been suggested [4–7]. Multimode interferometers have also been proposed as mode multiplexers [8, 9]. Recently, mode multiplexers based on asymmetrical directional couplers (DCs) have also been proposed [10–14]. However, those structures are limited by their sensitivity to fabrication errors. Currently, an efficient mode multiplexer built on the SOI platform with low insertion loss, low crosstalk, and large fabrication tolerance is still unreported.

A tapered DC has been shown to be an efficient design in order to relax the fabrication tolerance of conventional asymmetrical normal DCs used as polarization splitters and rotators [15]. In this paper we demonstrate an on-chip two-mode division multiplexing circuit using a tapered DC-based TE_0 & TE_1 multiplexer and demultiplexer. The device can furthermore be fabricated by a simple process on the SOI platform. A minimum insertion loss of 0.3 dB and mode crosstalk lower than -16 dB over a wide bandwidth of 100 nm are demonstrated together with a large tolerance of more than 20 nm for the width deviation of the narrow silicon waveguide (compared to only a few nanometers for a normal DC) and with relaxed coupling length sensitivity. The chip is further employed in a system experiment where two non return-to-zero (NRZ) on-off keying (OOK) channels, each modulated at 40 Gbit/s, are mode-multiplexed and demultiplexed. The experimental results show clear eye-diagrams, and only 1.6 dB and 1.8 dB power penalty for the two demultiplexed channels. To the best of our knowledge, this is the first system demonstration of on-chip mode multiplexing on an SOI waveguide for interconnect applications.

2. Principle and design of the TE_0 & TE_1 mode multiplexer

The TE_0 & TE_1 mode multiplexer is based on a tapered DC, which parallel-couples a narrow silicon waveguide (waveguide width w_1) to a wide tapered waveguide (from w_{2a} to w_{2b} with center width of w_2) with a coupling length and gap of L and g , respectively, as shown in Fig. 1. The structure is degenerated to a conventional asymmetrical normal DC when $w_{2a} = w_{2b} = w_2$. For conventional DC-based TE_0 & TE_1 mode multiplexers, the TE_0 - TE_1 coupling relies on the phase matching between the waveguides, i.e. the effective refractive index of the TE_0 mode of the narrow waveguide should be equal to that of the TE_1 mode of the wide waveguide. In this case, if TE_0 light is injected into the narrow waveguide, a high coupling efficiency $r_{TE_0-TE_1}$ will be obtained at the output of the wide waveguide. On the other hand, because of the significant effective refractive index difference between the TE_0 modes in the two asymmetrical waveguides, a very low coupling efficiency $r_{TE_0-TE_0}$ (mode crosstalk) is obtained. However, in conventional asymmetrical DCs, the phase matching can be easily destroyed by fabrication errors of the narrow waveguide. A fabrication error-induced width deviation Δw will result in a larger effective refractive index deviation Δn_{eff} for the narrow waveguide than for the wide waveguide since the slope of the effective index of the TE_0 mode

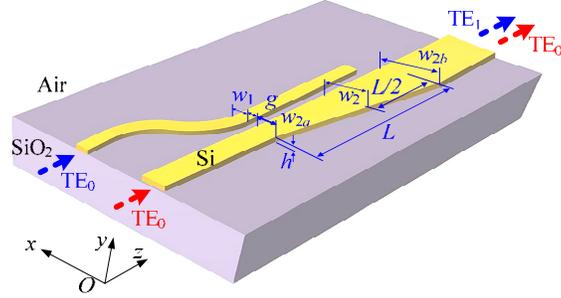


Fig. 1. Schematic structure of the proposed TE₀&TE₁ multiplexer.

versus waveguide width is larger than that of the TE₁ mode, as shown in Fig. 2(a). The larger the slope difference, the easier it is for the phase matching condition to be destroyed due to waveguide width errors. Moreover, the length of the DC should be properly designed to avoid the converted TE₁ light coupling back to the narrow waveguide. In order to relax these limitations, the wide waveguide is tapered from w_{2a} to w_{2b} in our proposed design. For the two widths w_{2a} and w_{2b} of the wide waveguide, the corresponding widths of the narrow waveguide enabling to satisfy the phase matching condition are w_{1a} and w_{1b} , respectively, as indicated in Fig. 2(a). Consequently, tapering the wide waveguide from w_{2a} to w_{2b} will result in a deviation tolerance between w_{1a} and w_{1b} for the narrow waveguide because a phase matching position can always be found along the taper. After the phase matching position, the conversion efficiency will be maintained and the fabrication error sensitivity of the coupling length will be relaxed. It should be noted that w_{2a} should not be too close to the width where the TE₁ and TM₀ modes are hybridized (700 nm in our case). A large tapering strength (width difference between w_{2a} and w_{2b}) provides a larger fabrication tolerance (from w_{1a} to w_{1b}) for the narrow waveguide. However, a larger tapering strength requires a longer tapering length L in order to achieve a sufficiently long effective coupling length around the phase matching position. Widths $w_1 = 390$ nm and $w_2 = 800$ nm were chosen as a starting point since these widths satisfy the phase matching condition, as shown in Fig. 2(a). Tapering from $w_{2a} = 750$ nm to $w_{2b} = 850$ nm with center width w_2 is selected for the wide waveguide. Figure 2(b) shows the TE₀-TE₁ coupling efficiency $r_{\text{TE}_0\text{-TE}_1}$ and mode crosstalk $r_{\text{TE}_0\text{-TE}_0}$ simulated as a function of wavelength using the eigenmode expansion (EME) method [16] with $L = 50$ μm and $g = 100$ nm. The residual TE₀-TM₀ coupling $r_{\text{TE}_0\text{-TM}_0}$ is also shown. One can find that a high $r_{\text{TE}_0\text{-TE}_1}$ with $r_{\text{TE}_0\text{-TE}_0}$ lower than -22 dB are obtained over a large wavelength range of 200 nm. In addition, a very small $r_{\text{TE}_0\text{-TM}_0}$ lower than -30 dB is also obtained thanks to the large refractive index difference between these two modes.

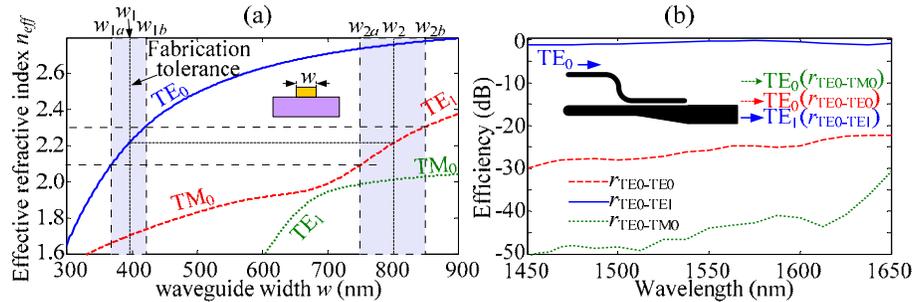


Fig. 2. (a) Effective indices of the TE₀, TE₁ and TM₀ modes of an air-clad SOI waveguide as a function of the waveguide width w for a waveguide height $h = 250$ nm. (b) Simulated TE₀-TE₁ coupling efficiency $r_{\text{TE}_0\text{-TE}_1}$, mode crosstalk $r_{\text{TE}_0\text{-TE}_0}$, and TE₀-TM₀ coupling efficiency $r_{\text{TE}_0\text{-TM}_0}$ as a function of wavelength. $w_1 = 390$ nm, $w_{2a} = 750$ nm, $w_{2b} = 850$ nm, $L = 50$ μm and $g = 100$ nm.

As mentioned previously, since the coupling efficiency $r_{\text{TE}_0\text{-TE}_1}$ is much more sensitive to the width of the narrow waveguide than to that of the wide waveguide, only the sensitivity to the width deviation of the narrow waveguide is investigated. The width of the narrow waveguide is changed between $w_1 \pm \Delta w$ to investigate the fabrication tolerance, where Δw is the width deviation due to fabrication error. A coupling gap $g = 100$ nm is selected. Figures 3(a) and 3(b) show the calculated coupling efficiency $r_{\text{TE}_0\text{-TE}_1}$ and mode crosstalk $r_{\text{TE}_0\text{-TE}_0}$ as a function of the width deviation Δw and coupling gap g , respectively, for both tapered and normal DCs. One can find that $r_{\text{TE}_0\text{-TE}_0}$ shows good tolerance to the width deviation Δw for both tapered and normal DCs since the phase mismatch of TE₀-TE₀ coupling is large in both cases. In case of a tapered DC, a high $r_{\text{TE}_0\text{-TE}_1}$ with $r_{\text{TE}_0\text{-TE}_0}$ lower than -25 dB is obtained within a width deviation range of about 40 nm for L varying from 30 μm to 50 μm . Since a high $r_{\text{TE}_0\text{-TE}_1}$ is maintained as L further increases, the width deviation tolerance is also expected for L longer than 50 μm . In addition, the tapered DC-based scheme also exhibits a good tolerance to the coupling gap, and a better gap tolerance is obtained for longer L . However, in the case of a normal DC, the width deviation tolerance is only a few nanometers, and the gap tolerance is even worse than for a tapered DC. Moreover, $r_{\text{TE}_0\text{-TE}_1}$, the width deviation tolerance, and the gap tolerance are much more sensitive to L than in the case of tapered DC.

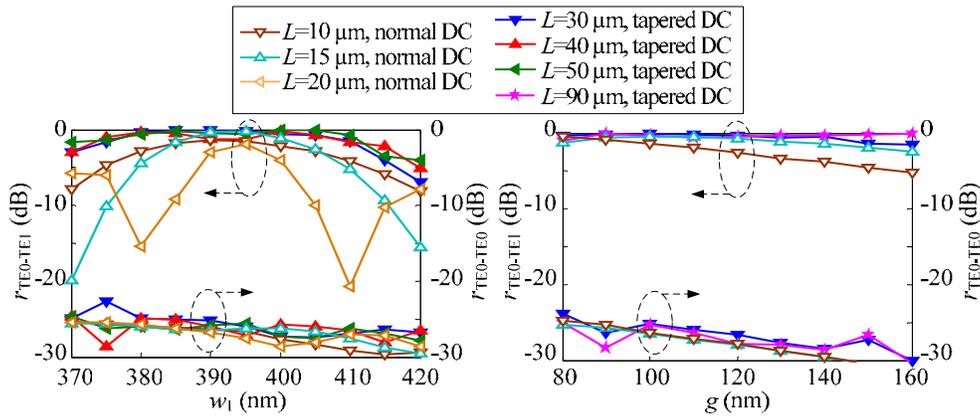


Fig. 3. Simulated coupling efficiency $r_{\text{TE}_0\text{-TE}_1}$ and mode crosstalk $r_{\text{TE}_0\text{-TE}_0}$ as a function of (a) width deviation Δw and (b) coupling gap g for different lengths L for both tapered and normal DCs. The operation wavelength is 1550 nm.

3. Device fabrication and characterization

Based on the proposed TE₀&TE₁ mode multiplexer design, a two-mode division multiplexing circuit was fabricated on a SOI wafer with 250 nm top silicon layer and 3 μm buried silicon dioxide by a single step of E-beam lithography (JEOL JBX-9500FS) and inductively coupled plasma reactive ion etching (STS Advanced Silicon Etcher). Polymer (SU8-2005) waveguides of dimensions 3.5 $\mu\text{m} \times 3.5 \mu\text{m}$ covering silicon inverse tapers were fabricated afterwards in order to reduce the coupling loss to tapered fibers. Figure 4(a) shows the fabricated device, which consists of a multiplexer (detailed in Fig. 4(b)) at the input side, a multimode data bus (750 nm wide), and a demultiplexer (identical to the multiplexer) at the output side. The width of the narrow waveguide is 355 nm, the wide waveguide is tapered from 748 nm to 848 nm, and the coupling gap is 100 nm, as shown in Figs. 4(c) and 4(d). Figure 5(a) shows the measured transmissions (normalized to a straight waveguide) from inputs CH₁ and CH₂ to the demultiplexed outputs CH₁ and CH₂, respectively, on the TE₀ mode, and the corresponding mode crosstalk (from inputs CH₁ and CH₂ to the demultiplexed outputs CH₂ and CH₁ on the TE₀ mode, respectively) for different widths w_1 of the narrow

waveguide and taper lengths L . High transmission from CH_1 and CH_2 to the corresponding demultiplexed CH_1 and CH_2 with lowest insertion loss of 0.3 dB and crosstalk lower than -16 dB are obtained over a large bandwidth of 100 nm for narrow waveguide widths of 360 nm and 380 nm, and taper length of 30 μm and 50 μm .

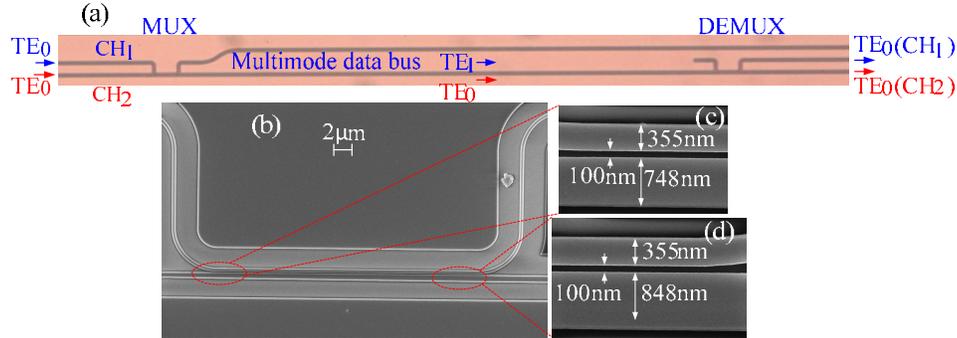


Fig. 4. (a) Fabricated TE_0 & TE_1 mode multiplexing circuit. (b) Scanning electron microscope (SEM) pictures of a fabricated TE_0 & TE_1 mode (de)multiplexer and details of its beginning (c) and end (d) sides.

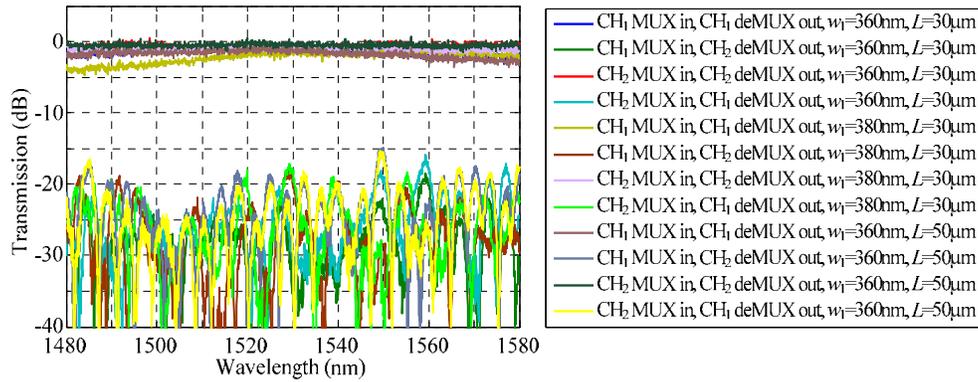


Fig. 5. Measured transmissions from inputs CH_1 and CH_2 to the demultiplexed outputs CH_1 and CH_2 on the TE_0 mode, and the corresponding crosstalk for different widths w_1 of the narrow waveguide and taper lengths L .

4. System demonstration

The fabricated chip was further employed for two-mode division multiplexing application with NRZ-OOK signals at 40 Gbit/s. Figure 6 shows the experimental setup. Continuous wave (CW) light at 1553.06 nm is modulated at 40 Gbit/s in the NRZ-OOK format in a Mach-Zehnder modulator with a pseudo-random binary pattern length of $2^{31}-1$, and then amplified by an erbium-doped fiber amplifier (EDFA). The amplified signal is split into two tributaries by a 3 dB coupler afterward. Before being injected into the silicon chip, the two tributaries are decorrelated using a length of 1 km standard single mode fiber. Polarization controllers (PCs) are used in order to set the state of polarization of each tributary so that it excites the TE mode of the silicon chip. The two channels, labeled CH_1 and CH_2 , are then simultaneously injected into the chip using a lensed fiber array for on-chip two-mode division multiplexing. The demultiplexed output signals from the chip are finally detected in a preamplified receiver.

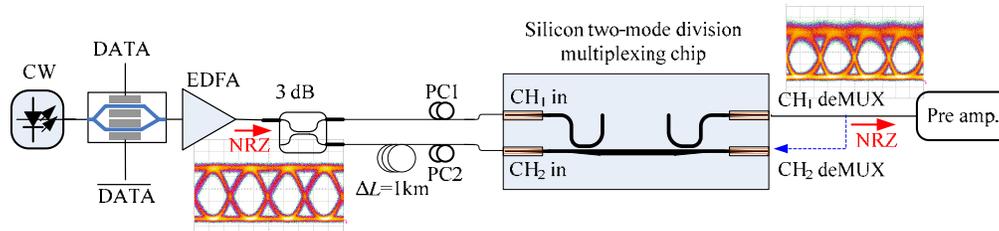


Fig. 6. Experimental setup for on-chip two-mode division multiplexing. The insets show the measured eye-diagrams of the NRZ signals after the transmitter and at one of the outputs of the demultiplexer, respectively.

Figure 7(a) shows the spectra of the signals recorded at the CH₁ and CH₂ demultiplexing ports when only either the CH₁ or CH₂ signal are injected into the waveguide, respectively. They correspond to either TE₁ mode or TE₀ mode propagation in the silicon multimode data bus, respectively. Crosstalk spectra (measured at CH₂ output with CH₁ excitation and at CH₁ output with CH₂ excitation) are also represented. Since the signal wavelength is tuned to the dip wavelength of the crosstalk spectrum (detailed in Fig. 5), a low crosstalk level below -20 dB is obtained for both channels. The corresponding demultiplexed signals exhibit clear eye diagrams, as shown in Figs. 7(c) and 7(d) when only the TE₁ or the TE₀ mode is propagating in the waveguide. When both TE₁ and TE₀ modes are multiplexed, clear eye diagrams are also obtained for the two demultiplexed signals thanks to the low mode crosstalk, as shown in Figs. 7(e) and 7(f). Figure 8 shows the results of bit-error-ratio (BER) measurements performed for the signals from the CH₁ and CH₂ demultiplexing ports with and without crosstalk. Low power penalties of 1.6 dB and 1.8 dB are obtained for CH₁ and CH₂ demultiplexing with crosstalk, respectively.

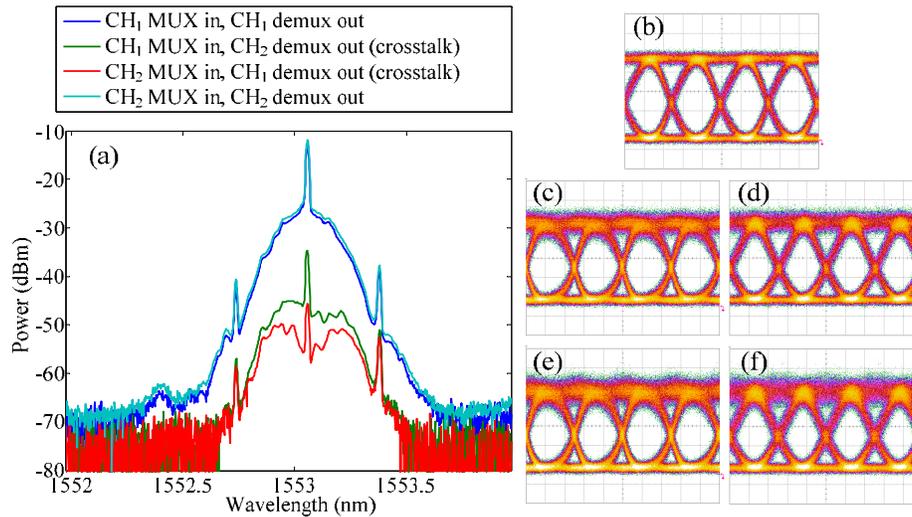


Fig. 7. (a) Measured spectra of the two demultiplexed NRZ-OOK signals at output ports CH₁ and CH₂, as well as the corresponding crosstalk for each demultiplexing channel. (b) Measured eye diagrams of the NRZ-OOK signal at the transmitter output. Measured eye-diagrams of the demultiplexed signal at the CH₁ output port without (c) and with (e) crosstalk. Measured eye-diagrams of the demultiplexed signal at the CH₂ output port without (d) and with (f) crosstalk.

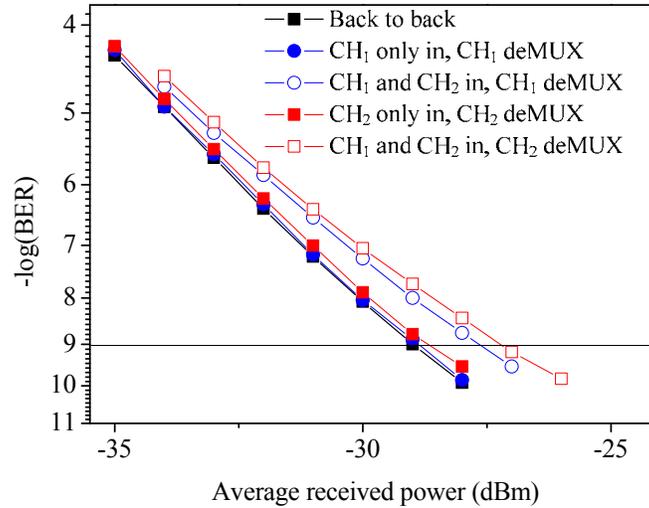


Fig. 8. BER measurements for the two demultiplexed channels with and without crosstalk.

5. Conclusion

In conclusion, we have demonstrated an on-chip two-mode multiplexing circuit using a novel TE_0 & TE_1 mode multiplexer built on the SOI platform. The circuit exhibits a lowest insertion loss of 0.3 dB, with mode crosstalk smaller than -16 dB over a wide bandwidth of 100 nm. A large fabrication tolerance of 20 nm and relaxed coupling length sensitivity are experimentally demonstrated. System experiments have been carried out for on-chip two-mode multiplexing application at 40 Gbit/s, showing clear eye diagrams for both demultiplexed channels and 1.6 dB and 1.8 dB power penalties with crosstalk for the two channels, respectively.