Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications

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Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications

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Keywords

Isolated Full Bridge Boost Converter (IFBBC), Loss Analysis, Fuel and Electrolyzer Cell, Power Semiconductors, Energy Storage.

Abstract

Energy production from renewable energy sources is continuously varying, for this reason energy storage is becoming more and more important as the percentage of green energy increases. Newly developed fuel cells can operate in reverse mode as electrolyzer cells; therefore, they are becoming an attractive technology for energy storage grid-tie applications. In this application dc-dc converter optimization is very challenging due to the large voltage range that the converter is expected to operate. Moreover, the fuel-electrolyzer cell side of the converter is characterized by low voltage and high current. Dc-dc converter efficiency plays a fundamental role in the overall system efficiency since processed energy is always flowing through the converter; for this reason, loss analysis and optimization are a key component of the converter design.
The paper presents an isolated full bridge boost dc-dc converter (IFBBC) designed for this new application focusing on losses analysis. The system topology is briefly discussed and the major concerns related to the system, cells stacks and converter operating points are analyzed. The dc-dc converter losses are modeled and presented in detail; the analysis is validated on adc-dc converter prototype rated at 6 kW 30-80 V 0-80 A on the low voltage side and 700-800 V on the high voltage side (for a grid-tie application). The prototype is based on fully planar magnetic, Si MOSFETs, Si IGBTs and SiC diodes; efficiencies up to ~96.5% and ~97.8% were demonstrated depending on the converter operating point.

Introduction

The energy production from renewable energy sources, such as wind, solar and tidal energy, is strongly fluctuating daily and seasonally, this is due to the nature of these energy sources. During high energy demand peaks or during low energy production from renewable energy sources it is necessary to relay on other more predictable energy sources. Vice versa, when the energy demand is low or there is an energy surplus from renewable sources it is desirable to store this energy. For this reason, smart grids and energy storage started to play an important role in today's energy market and energy policies.
Fuel cell technology was initially discovered in the late 19th century, and still nowadays is considered one of the most promising sources for distributed energy. Fuel cells are an attractive solution for distributed high-power density clean energy generation however, in order to have a bidirectional system they are often combined with electrolyzer cells [1]. In fact, conventional fuel cells cannot operate in reverse mode (with reversed current direction [2]) without incurring in low-efficiency and complex system design. Recent developments in fuel cell /electrolyzer cell technology, especially in Solid Oxide Fuel Cells (SOFC) and Solid Oxide Electrolyzer Cells (SOEC), have enabled these cells to operate in both modes with high efficiency. These cells could represent an attractive solution for the

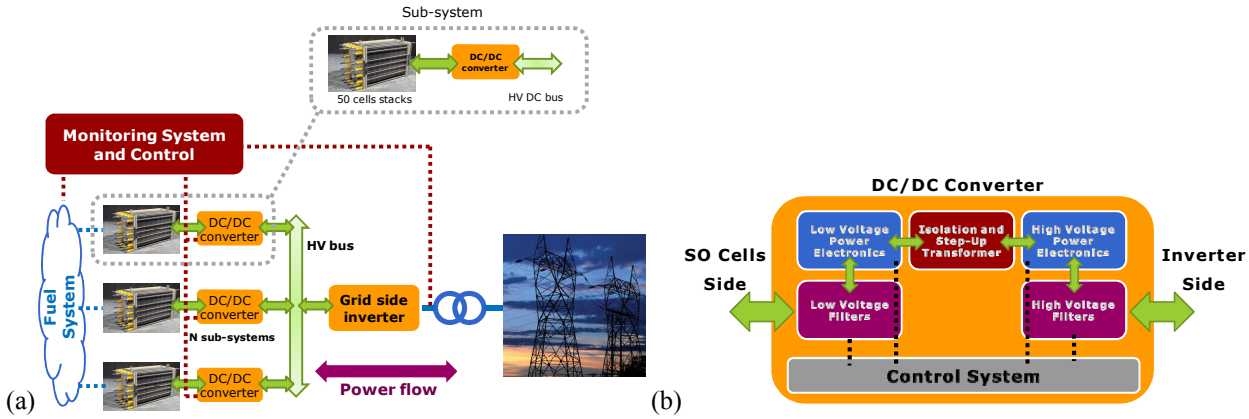


Fig. 1. System overview for fuel cell/electrolyzercell operation (a) and DC-DC converter structure (b).

next generation of smart grids since they can be used both as energy source and as energy storage depending on the market demands.
Realizing high power stacks of SOFC/SOEC represents a big challenge in terms of fuel /gas-pressure equalization within the cells, reliability and long term degradation. Therefore, in most cases fuel or electrolyzer cells are stacked in a limited number, which result in low voltages and high currents. For this reason a power conditioning system is required to adapt the voltage and current levels of the cells stack to a grid interface. DC-DC converters are used for power conditioning in several applications such as solar inverters, uninterruptible power supplies (UPS) and battery systems [3]; they represent the ideal interface for matching the SOFC/SOEC V-I characteristic to the grid interface.
This paper presents a complete loss analysis of an isolated boost DC-DC converter (IFBBC), suitable for bidirectional operation of SO cells. The analysis is verified on a 6 kW prototype with peak efficiency up to ~96.5 % and 97.8% depending on the converter operating mode. Results are discussed and analyzed in relation to the specified application.

System Specification and Converter Topology

The system topology strongly depends on the technology level reached by the SO cells; this defines the number of cells that can be stacked and, therefore, the low voltage interface of the DC-DC converter. As the number of stacked cells increases, cells reliability decreases and degradation increases due to different cell characteristics and unbalances in the fuel system. After a close discussion with SO-cells manufacturer and based on the state of the art a cells stack of 50 cells was considered as the most suitable for this application. With these specifications it was possible to define the DC-DC converter specifications as presented in Table I. The system can be scaled to various power levels by paralleling different SO cells stack and DC-DC converters as presented in Fig. 1a. Each DC-DC converter, Fig. 1b, allows operating each stack at its optimal point independently from the other stacks.
A simple bidirectional non-isolated boost converter could be sufficient however, for high step-up ratios its design becomes challenging making difficult to achieve high converter efficiency for wide operating voltage and power range. Moreover, another drawback of this topology is the lack of galvanic isolation: electric isolation from the fuel cell to the other part of the system is often desired in order to protect the cells stack especially when high voltages are present in the system. For this reason, isolated boost full bridge dc-dc converter represents a good candidate for this application (Fig. 2). It is capable of providing electric isolation with a small high frequency transformer moreover, the transformer provides voltage scaling allowing achieving high efficiency also with large step-up ratios. This topology when properly optimized can achieve very high efficiency and it proved to have the top-efficiency performance for these applications [4]. Most of the boost derived topologies suffer of start-up problems [5], this occurs whenever the output voltage is lower than the input voltage. In this application, the start-up is not critical since the DC-link voltage range is guaranteed by the grid-tie inverter and SO cells have a slow ramp-up time compared to the converter time constants which allow a soft start of the converter.

TABLE I
SOFC AND SOEC SPECIFICATIONS FOR DC-DC CONVERTER DESIGN

	SOFC	SOEC	
Low Voltage (LV) side	30-50	50-80	[V]
Current (LV) side	40-0	0-80	[A]
High Voltage (HV) side	700-800	700-800	[V]
Power Rating	~1500	~6000	[W]

Isolated Full Bridge Boost DC-DC Converter Design and Loss Analysis

The design and optimization of the converter should consider the different operating modes of the system. One of the main concerns related to energy storage is the profitability of the system; this has to be taken into account as weighting factors in the converter design and optimization. Supposing an electric energy conversion efficiency of 90% for both power flow directions, an electricity price of 35 €/MWh during periods of large availability from renewable energies and 50 €/MWh during high electricity demand [6]; with these values is possible to calculate the economic loss due to the convert efficiency:

- SOFC mode (energy production) ➔loss 5 €/MWh
- SOEC mode (energy storage) ➔loss 3.5 €/MWh

In both operation modes the energy conversion efficiency would cause a significant economic loss however, in SOFC mode low converter efficiency would cause more economical losses than in SOEC mode. For this reason it is preferable to have higher efficiency in SOFC mode than SOEC mode. Converter losses can be minimized for one operating point however, the converter has still to be capable of operating in the entire voltage range (30-80 V).
In the following sub-section an analysis of the converter losses when the converter is operating. This analysis is performed on a 6 kWdc-dc converter prototype designed for a maximum input current of ~80 A and capable of operating in the whole 30-80 V range. The converter high voltage side is rated at 700-800 V and it is suitable for a 400 $V_{AC,rms}$grid-tie inverter.

DC-DC Converter Loss Categorization

In order to perform a suitable converter design where the losses are minimized; it is essential to identify all the major loss sources, create models and verify the achieved results. When the major sources of losses are identified it is possible to tune the converter design in order to achieve high efficiency and minimize the losses. In order to obtain accurate models design-measurement loop iterations are required. These are time and cost demanding therefore, it is often desired to minimize these iterations. In this paper, the approach that has been used tried to gather as many information as possible from datasheet and minimize the number of measurements. In a second step the losses are evaluated for different converter operating points and the calculated converter efficiency is compared with the measured one.

Transformer Losses

The transformer is a key component to achieve high efficiency in an IFBBC. The low voltage side of the converter is characterized by high current therefore, particular care should be taken to minimize the winding losses. Moreover, the transformer leakage inductance acts as common source inductance in the selected topology limiting the current commutation time at MOSFET's turn-off and also the

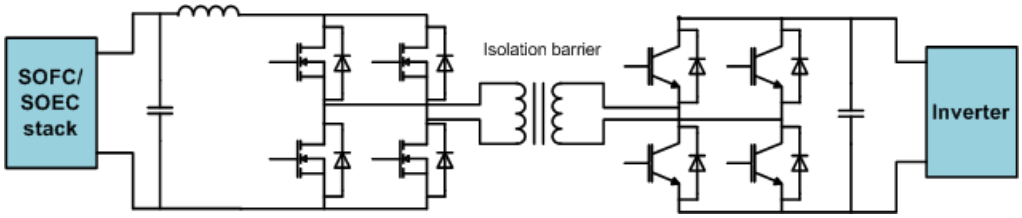


Fig. 2: Bidirectional isolated boost DC-DC converter.

converter efficiency. An interleaved winding structure for minimizing both winding losses (ac-resistance) and leakage inductance was selected for the transformer; the selected interleaved structure is P-S-P-S-P. The main drawbacks of introducing an interleaved structure are that the transformer P-S stray capacitance increases that the manufacturing process of the transformer is more complex. Large transformer stray capacitance is usually unwanted since it increases the common mode noise. However, for the intended application EMC requirements are not included and the EMC filter is not part of the study.
The transformer is designed based on planar cores (E64), two cores are stacked "in series" on in order to increase the overall core cross section and minimize the number of transformer primary turns (low voltage high current winding). The overall transformer design is performed for a switching frequency of 40 kHz minimizing the losses (1) around this switching frequency. Core losses are computed with the generalized Steinmetz equation (2)[7] and the winding losses are calculated based on Dowel's equation that takes into account skin and proximity effects (3)[8][9]. The transformer characteristics are summarized in Table II.

TABLE II
TRANSFORMER CHARACTERISTICS

Turns ratio	8
Primary	3 turns
Core	2*E64 pairs
Core material	Magnetics R
Structure	P-S-P-S-P
Primary winding (P)	PCB 2*400 µm
Secondary winding (S)	30*0.2 mm litz wire
Insulation P-S	2*0.1 mm Kapton

For the 6 kW prototype the design procedure resulted in 3 primary turns and 24 secondary turns on a two series E64 R-material planar transformer cores (for a frequency range around 40 kHz, K=0.074, α=1.43 and β=2.85, with B in kG and f in kHz, result in mW/cm^3). The primary transformer turns are realized with two parallel layers of 400 µm copper (custom thick copper PCB) insulated from each other by 500 µm layer of FR4. The 24 secondary turns are created with litz wires (30 strands of 200 µm diameter) interleaved with the primary winding in a P-S-P-S-P structure. Insulation between primary and secondary is created with two layers of Kapton tape (100 µm each layer). Very thick copper PCB windings (primary) were selected in order to achieve high filling factor in the transformer (in this case ~32%) which is normally not achievable with conventional PCBs. For modeling the transformer losses, the transformer windings resistance was reflected to the primary. A transformer short circuit measurement identified $R_{ac,pri\,eq.} = 5.6\ m\Omega$ and $L_{leak,pri\,eq.} = 82\ nH$ at the switching frequency.

$$P_{tr.} = P_{core} + P_{wind.} \quad (1)$$
$$P_{core} = K \cdot f^{\alpha} \cdot B^{\beta} \quad (2)$$
$$P_{wind.} = R_{ac,pri\,eq.} \cdot I_{pri,rms}^2 \quad (3)$$

Low Voltage Side: Conduction and Switching Losses

The maximum stress over the power semiconductors of the low voltage side of the converter is defined by the converter high voltage side (700-800 V) reflected to the low voltage side (87.5-100 V). At this voltage levels MOSFETs are the most suitable devices. The MOSFETs rating should be just above the maximum voltage stress plus a margin factor. MOSFETs are available rated at 120 V and 150 V, however, due to the low voltage high current the 120 V (lower $R_{DS,on}$) were preferred over the 150 V. Another advantage of the low $R_{DS,on}$1 120 V MOSFETs is that they are available in TO-220 package which has a lower stray inductance than the TO-247 package (used for low $R_{DS,on}$ 150 V devices). In order to decrease the conduction losses two MOSFETs are paralleled, each MOSFET has its independent gate resistor (2.5 Ω) and they are driven by a common driver with a 9 A capability. The selected MOSFETs are Infineon 120 V 4.1 mΩ TO-220. Since they converter does not have an active clamp, the devices may observe avalanche during switching; the selected power semiconductors have avalanche capability of 900 mJ for a single pulse and for repetitive pulses is thermally limited.

The primary low-voltage power semiconductor losses (4) are classified into: conduction ($P_{cond.}$), turn-on ($P_{turn-on}$) and turn-off ($P_{turn-off}$) losses. Conduction losses are simply calculated based on the MOSFETs RMS current($I_{pri\ SW,rms}(D)$) dependent on the duty cycle(5). Turn-on losses are limited to the discharge of the MOSFET's output capacitance ($C_{oss,V_{DS}}$)(6) since the current commutation is delayed by the common source inductance [10][11]. The MOSFET's turn-off losses are due to the limited current commutation speed due to the common source stray inductance which also includes the transformer leakage inductance (in series during in the commutation path). The MOSFETs body diode (10) conducts only when the converter power flow is from the high voltage to the low voltage side. In this case we have both conduction losses (11) and reverse recovery losses (12); dead time is applied to both rise and fall edges (factor two in (11)) and the current flowing through the device is the dc-current plus the ac-current component (first dead time interval) and the dc-current minus the ac-current (second dead time interval). The equivalent conduction losses of the body diode can be approximated with the average dc-current (11).

$$P_{MOS\ LV} = P_{cond.} + P_{turn-on} + P_{turn-off} \quad (4)$$

$$P_{cond.} = R_{DS,on}(T) \cdot I^2_{pri\ SW,rms}(D) \quad (5)$$

$$P_{turn-on} = \frac{1}{2} \cdot C_{oss,V_{DS}} \cdot \left(\frac{V_{HV}}{n_{tr}}\right)^2 \cdot f_{sw} \quad (6)$$

$$dt_{L\ leak} = (L_{leak\ tr.} + L_{leak\ LV\ switch}) \cdot (I_{DC,LV} + I_{AC,peak\ LV}) \cdot \frac{n_{tr}}{V_{HV}} \quad (7)$$

$$P_{turn-off} = \frac{1}{2} \cdot \frac{V_{HV}}{n_{tr}} \cdot \frac{I_{DC,LV} + I_{AC,LV\ peak}}{2} \cdot dt_{L\ leakage} \cdot f_{sw} \quad (8)$$

$$= \left(\frac{I_{DC,LV} + I_{AC,LV\ peak}}{2}\right)^2 \cdot (L_{leak\ tr.} + L_{leak\ TO-220}) \cdot f_{sw} \quad (9)$$

$$P_{bd.MOS} = P_{cond.bd.MOS} + P_{rev.rec.} \quad (10)$$

$$P_{cond.bd.MOS} = V_{fwd.bd.MOS} \cdot I_{DC} \cdot 2 \cdot t_{dead\ time} \cdot f_{sw} \quad (11)$$

$$P_{rev.rec.} = \frac{1}{2} \cdot Q_{rr} \cdot \frac{V_{HV}}{n_{tr}} \cdot \frac{I_{DC}}{I_{rr,ref}} \cdot f_{sw} \quad (12)$$

High Voltage Side: Conduction and Switching Losses

The converter high voltage side uses 1200 V 3rd generation Trench IGBTs from Infineon (IGW15N120H3) and SiC Schottky diodes (Cree C4D15120A) in antiparallel to the IGBTs. The IGBTs conduction and switching losses are introduced in the model based on datasheet values. The IGBTs conduction losses ($P_{fwd,IGBT}$) are calculated based on the IGBTs forward characteristic (datasheet); linearized to a threshold voltage (V_{ce}) and an on state resistance ($R_{on,IGBT}$) as shown in (14). The IGBTs switching losses are initially extracted from datasheet and then corrected based on a reference measurement in order to have higher accuracy in the calculation. From datasheet it is possible to scale the IGBTs losses for different temperatures, different gate resistors and different device switching voltage. This type of scaling is often linear and commonly used for simple loss modeling [12].In this case, the IGBT datasheet values also included the reverse recovery losses of the antiparallel diode which for the designed converter is a SiC diode. For this reason, the IGBT switching losses were scaled based on a reference measurement at 15 A 700 V [13]with a linear coefficient $K_{SW\ on,ref}$aand $K_{SW\ off,ref}$ (15).
In SOFC mode the current flows through the full bridge created with SiC Schottky diodes (IGBTs they do not have free-wheeling diodes and in this mode they do not contribute to the losses). The diodes losses (16) due to the forward voltage drop and due to the diodes resistance are included in $P_{fwd,diodes\ HV}$ (17). SiC Schottky diode are often claimed to have zero-recovery charge ($Q_{rr,HV\ diode}$) compared to conventional silicon diodes however, they also give a small contribute to the high voltage side losses due to the energy stored in their stray capacitance ($P_{HVdiod.rev.rec.}$) (18).

$$P_{IGBT} = P_{fwd,IGBT} + P_{sw,IGBT} \quad (13)$$

$$P_{fwd,IGBT} = V_{ce} \cdot I_{avg} + R_{on,IGBT} \cdot I^2_{HV\ SW,rms} \quad (14)$$

$$P_{sw,IGBT} = E_{on,IGBT}\left(I_{IGBT,turn-on}\right) \cdot K_{SW\ on,ref} \cdot f_{sw} + E_{off,IGBT}\left(I_{IGBT,turn-off}\right) \cdot K_{SW\ off,ref} \cdot f_{sw} \quad (15)$$

$$P_{diodes\ HV} = P_{fwd,diodes\ HV} + P_{HVdiod.rev.rec.} \quad (16)$$

$$P_{fwd,diodes\ HV} = V_{fwd}(T) \cdot I_{avg} + R_{on,IGBT} \cdot I^2_{diode\ HV\ SW,rms} \quad (17)$$

$$P_{HVdiod.rev.rec.} = \frac{1}{2} \cdot Q_{rr,HV\ diode} \cdot V_{HV} \cdot f_{sw} \quad (18)$$

Boost Inductor Losses

The boost inductor has to carry all the input current for this reason it is important to analyze and try to minimize the losses in this component. The losses in the boost inductor (19) are due to dc-resistance ($P_{DC,wind.}$), ac-resistance [9]($P_{AC,wind.}$) and core losses(P_{core}). The inductor winding losses are computed based on the dc-resistance ($R_{DC,ind}$) and the dc inductor current ($I_{LV,DC}$) (20). The resistance is easily calculated based on the copper cross section and the total length of the inductor windings. The ac-current ripple ($I_{LV,AC\ rms}$) strongly influences the converter efficiency especially at low power levels therefore, it has to be taken into account (21).According to Dowels [8], in a conventional inductor with concentric windings the ac-resistance rapidly increases due to proximity effect. In this design planar (PCB) windings are used, windings are not concentric anymore and the ac-winding resistance can be approximated based on the conductor thickness (h_{Cu}) times the dc-resistance (22). Inductor core losses strongly depend on the core material: high frequency materials such as gapped 3F3 cores provide low core losses however, they significantly increase the winding losses due to fringing flux in proximity of the gap. In this case the inductor was designed based on planar Kool Mu cores. This material has a distributed gap and it does not generate losses in the windings due to fringing flux. The main drawback of this material is its higher hysteresis core losses. The designed inductor has three planar Kool Mu E6030 cores pairs, two pairs in 90µ material and one pair with 26µ material. The cores are arranged in "series" in order to increase the overall core cross section. The winding structure is based on thick copper PCB windings (400 µm copper thickness); the inductor has five turns and each of them is realized by two parallel layers of 400 µm copper track. Core losses have been calculated from Steinmetz equation based on the coefficients for Kool Mu material (Kool Mu 26µ K=120, α=1.46, β=2.09 and Kool Mu 90µ K=193, α=1.26, β=2.01 with f_{sw} in kHz and flux density in T) according to (2).

$$P_{boost\ ind.} = P_{DC,wind.} + P_{AC,wind.} + P_{core} \quad (19)$$

$$P_{DC,wind.} = R_{DC,ind} \cdot I^2_{LV,DC} \quad (20)$$

$$P_{AC,wind.} = R_{AC,ind} \cdot I^2_{LV,AC\ rms} \quad (21)$$

$$R_{AC,ind} = \frac{h_{Cu}}{\delta} \cdot R_{DC,ind} \quad (22)$$

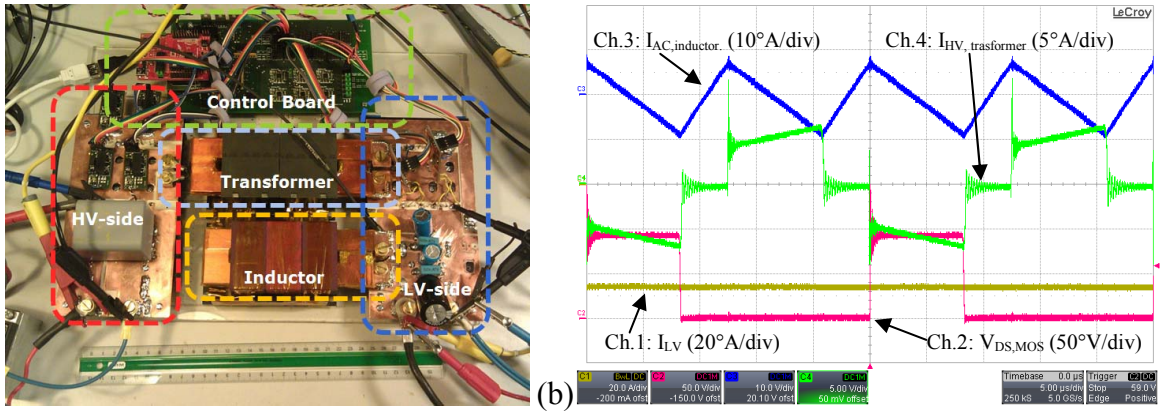
Control and Driver Losses

Control and driver losses have to be included in the loss analysis (23). Gate driver losses are easily calculated from the input capacitance (both for MOSFETs and IGBTs gate drivers (24)). This approximation simply considers the power required for driving the devices and not the overall power required by the gate driver (other circuitry on the gate driver). Moreover, the overall control power (P_{ctrl}) is difficult to calculate since it also depends on the power used by the DSP board with depends on the control loop and DSP features that are used (P_{DSP}) (25). In addition, cooling fans are used on the converter heatsinks (on the bottom of Fig. 3a), these fans have a power consumption of 3.8 W (P_{fans}). At low power level they have a strong impact on the converter efficiency, and therefore, to increase the overall efficiency, temperature control is desired.

$$P_{ctrl} = P_{gate-drivers} + P_{DSP-control-card} \quad (23)$$

$$P_{gate-drivers} = (Q_{g,tot,MOS} \cdot V_{g,MOS} + Q_{g,tot,IGBT} \cdot V_{g,IGBT}) \cdot f_{sw} \quad (24)$$

$$P_{DSP-control-card} = P_{DSP} + P_{fans} \quad (25)$$



(a) (b)

Fig. 3: 6 kW prototype of isolated boost converter (a) and switching waveforms at 60 V 40 A. Ch.1(yellow): I_{LV} (20 A/div), Ch.2(red): $V_{DS,MOS}$ (50 V/div), Ch.3(blue): $I_{AC,inductor}$ (10 A/div) and Ch.4(green): $I_{HV,\ transformer}$ (5 A/div).

Overall Converter Losses

The converter efficiency depends on the power flow direction; in fact in one operating mode the converter is operating as a boost converter (power flow from the low voltage to the high voltage side, SOFC mode), while with the opposite power flow the converter acts as a buck (SOEC mode). In SOFC mode the body diode of the low voltage side MOSFETs will never conduct and therefore, it will not have a contribution to the converter losses. In this operating mode, the current in the high voltage side bridge will flow uniquely through the SiC Schottky diodes and IGBTs will not contribute to the losses since they are bipolar devices and they cannot be used for active rectification. Similarly, in SOEC mode the diodes in the high voltage bridge are not used and, therefore, only the diode capacitance will contribute to the losses (no conduction losses). Moreover, the MOSFETs will have very low switching losses since during turn-off the MOSFETs body diode will start carrying the current and will maintain a low-voltage across the MOSFET (close to soft switching).
The other components of the losses remain unchanged and they do not depend on the converter operating mode. This results that the total converter losses for the two operating modes are given by:

$$P_{SOFC} = P_{tr} + P_{MOS\ LV} + P_{diodes\ HV} + P_{boost\ ind.} + P_{ctrl} \quad (25)$$

$$P_{SOEC} = P_{tr} + P_{bd.MOS} + P_{cond.MOS} + P_{IGBT\ HV} + P_{HVdiod.rev.rec} + P_{boost\ ind.} + P_{ctrl} \quad (26)$$

Experimental Results and Analysis

Experimental results are based on a developed 6 kW prototype (Fig. 3a and Fig. 3b). The goal of the prototype was to verify the expected performance of the converter and identify the main source for losses with experimental verification.
The converter was operated in SOFC and SOEC mode and its efficiency measured with a precision power analyzer (N4L PPA5530) using 1 mOhm 100 A current shunts for the entire 30-80 V range at different power levels. Measured efficiencies are presented on Fig. 4a and Fig. 4b for both power flow direction (SOFC = boost mode, SOEC = buck mode). At low voltage levels the power on the developed prototype is limited by its maximum current (80 A_{RMS}). Efficiency measurements were exported and interpolated with MATLAB to obtain a smoother plot. The darkened area on Fig. 4a and Fig. 4b indicates a prohibited operating point for the converter (current overload). In this darkened area(current overload)the efficiency was extracted based on a fit of the measured values in the normal converter operating range (30-80 V and 0-80 A).At the lowest input voltage (30 V) efficiency is limited by the high current flowing in the converter that give significant contribute in the conduction and switching losses. In this case the efficiency is limited to 95.9% in SOFC and 93.3% in SOEC mode. At the highest input voltage (80 V) the converter efficiency reaches a peak of 97.8% in SOFC and 96.5% in SOEC. It is observed that the efficiency is SOEC is always lower than in SOFC. In SOFC the MOSFETs are hard switching and the IGBTs do not give contribution to the losses, while in SOEC the IGBTs are giving large contribute to the losses (both switching and conduction losses) and the MOSFETs are used for active rectification (close soft switching).

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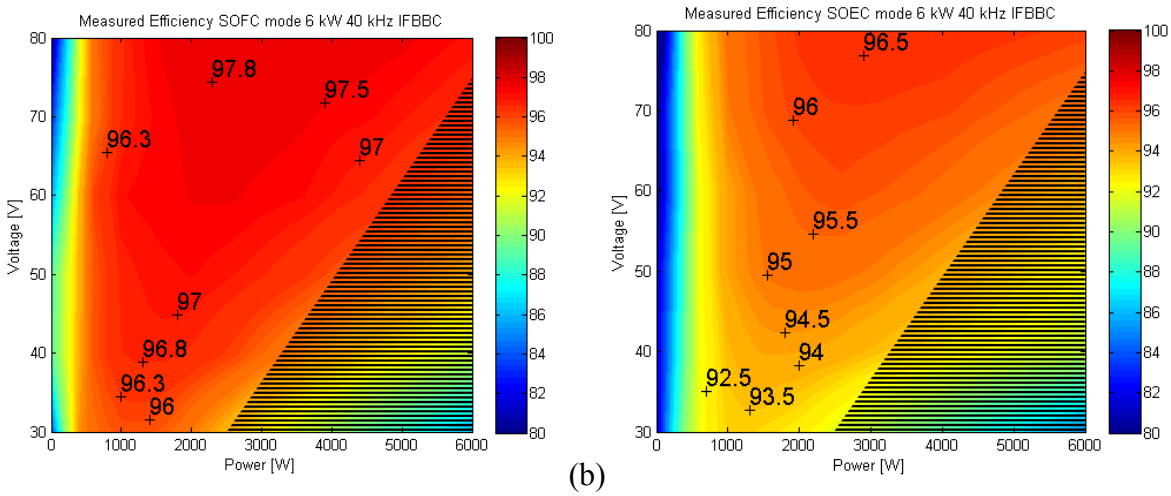


(a) (b)

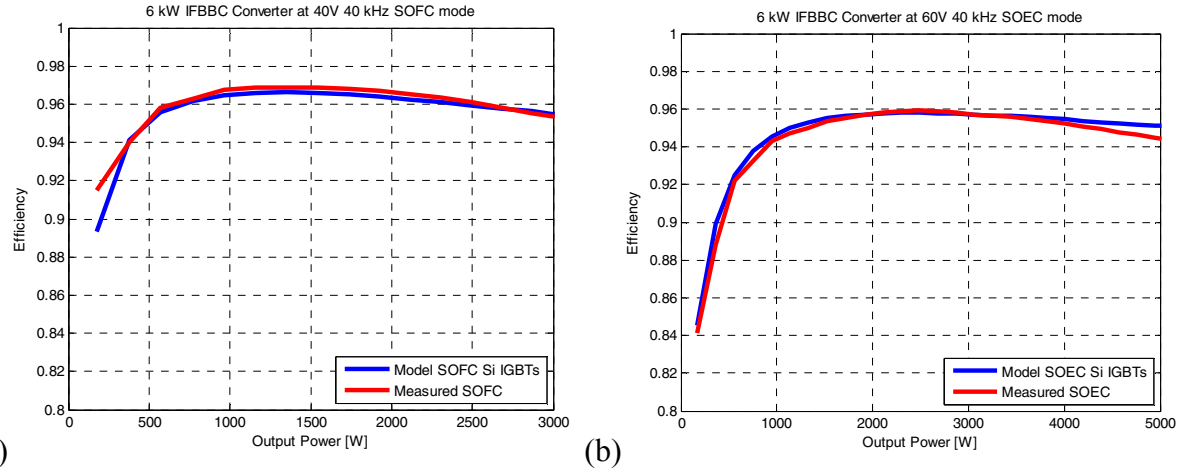
Fig. 4: Measured efficiency of the 6 kW IFBBC prototype at different voltage and different power levels, SOFC mode (a) and SOEC mode (b). Darkened area indicates that the converter is not allowed to operate in these conditions due to over current on the low voltage side (80 A current limitation).

Measured vs. Modeled Efficiency

The operating point of the dc-dc converter is defined by the SOFC /SOEC cells stack. In SOFC mode the voltage of the cells stack decreases as the power increases, vice versa in SOEC mode. The modeled converter efficiency is compared with the measured one. Two characteristic curves are presented: one at 40 V for SOFC mode (Fig. 5a) and one at 60 V for SOEC mode (Fig. 5b).Based on the presented loss model of the IFBBC a small difference is observed. It should be considered that the presented model assumed constant device temperature for power semiconductors, magnetic components and for copper. This assumption introduces an error since the converter component temperatures will vary continuously depending on the voltage and power flow through the converter. It is interesting to observe that the peak efficiency at 40 V and SOFC mode is ~96.8% at 1-1.5 kW(Fig. 5a); at 60 V in SOEC the peak efficiency is observed at 2-3 kW and it is ~95.9% (Fig. 5b).

Components of the Converter Losses

In proximity of the peak efficiency at 40 V in SOFC and 60 VSOEC, the different sources of losses in the converter are presented based on the modeled values (Fig. 6). It is observed that in SOFC mode at 1 kW and 40 V (Fig. 6a) the main source of losses is the boost inductor. At this power level the main



(a) (b)

Fig. 5: Comparison of measured versus calculated efficiency of the 6 kW IFBBC based on the presented models. Efficiency comparison at 40 V (a) SOFC mode (power flow from the low voltage side to the high voltage side) and 60 V (b) SOEC mode (power flow from the high voltage side to the low voltage side). 80 A current limitation.

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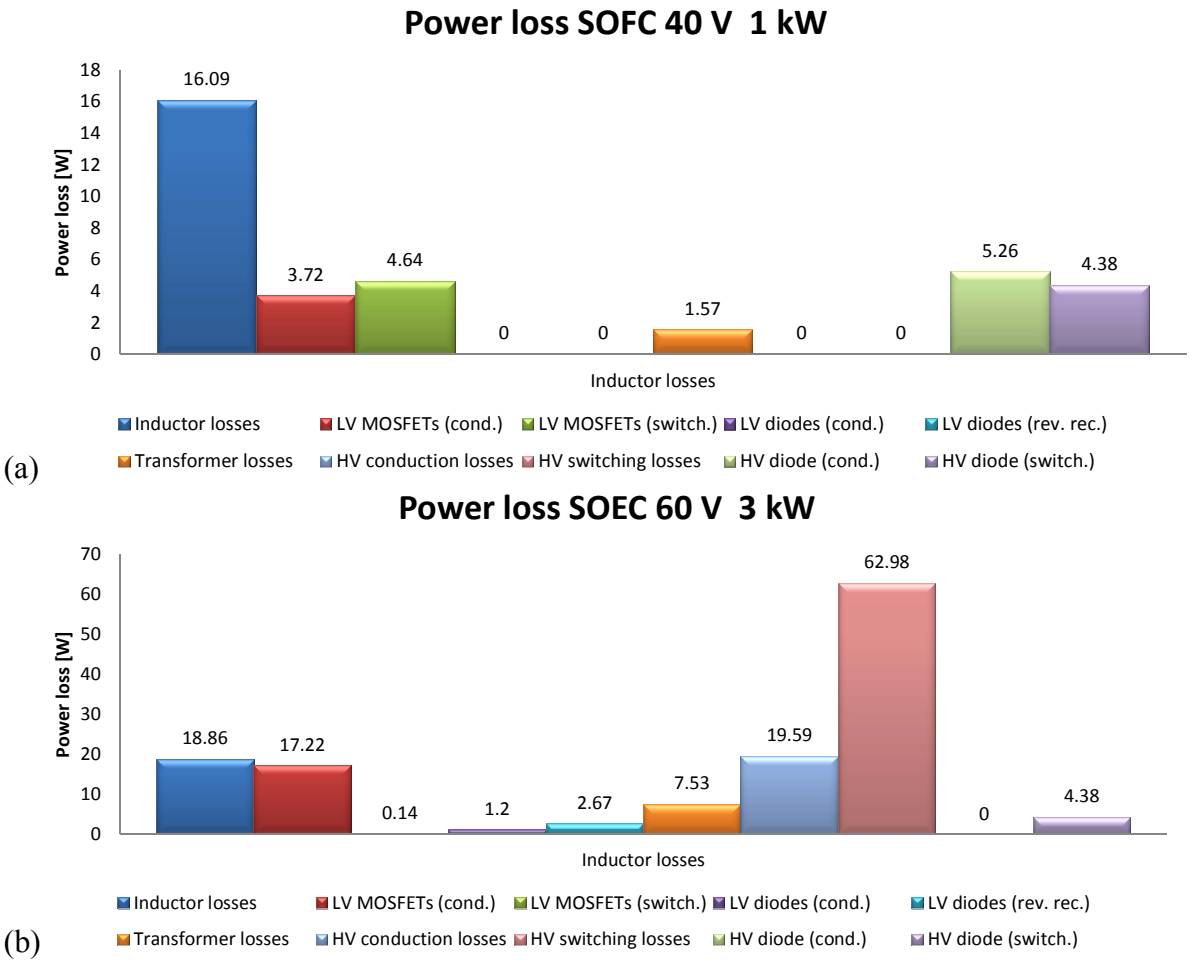

Fig. 6: Calculated loss components of the 6 kW IFBBC prototype at 40 V 1 kW in SOFC mode (a) and at 60 V 3 kW in SOEC mode (b). Based on the developed loss model.

inductor losses are due to the core losses; in fact even though the ripple current is limited, ac inductor flux produces significant losses (Kool Mu material has larger losses than traditional ferrites). As the power increase (e.g. 1.5 kW 40 V) the inductors losses have a minimal increase mostly due to winding losses. However, the losses in the other components significantly increase especially the ones in the power semiconductors. MOSFET's turn-off commutation time increases due to the large current to be commuted. Then above 1.5-2 kW (Fig. 5a) the efficiency starts decreasing due to the significant increase of the conduction losses at large current.

The loss components at 60 V 3 kW (Fig. 6b) in SOEC mode significantly change. The MOSFET's main loss contribution is given by the conduction losses (active rectification). The MOSFET's body diode conducts only for a short time (dead time) and their total contribution (conduction and reverse recovery) is minimal compared to other losses. The main sources of loss are the high voltage power semiconductors (IGBTs in hard switching condition); dominant are the switching losses which account up to ~45% of the total losses at this operating point, Fig. 6b.

On overall, it is observed that even with a limited variation of the voltage on the converter low voltage side (from 40 V up to 60 V) compared to the overall operating voltage range the distribution of the converter losses varies significantly. It is observed that the lowest efficiency in SOEC operating mode is due to the large losses generated by the IGBTs on the converter high voltage side. This operation mode would significantly benefit by the introduction of SiC devices which would increase the converter efficiency. Vice versa, in SOFC mode there is a significant component of the losses that is given by the boost inductor (mostly core losses). The inductor could be designed based on a gapped ferrite core which would significantly reduce the core losses but, would increase the inductor winding losses due to fringing flux in the core air gap.

Conclusions

The paper presented a new challenging application for bidirectional isolated boost DC-DC converters boost with wide low-voltage input and high-current. The developed converter is based on fully planar magnetic and has peak efficiency of 97.8% and 96% depending on the converter operating mode. The design procedure has taken into account the operating mode (SOFC/SOEC) of the cells stacks and a loss analysis for the converter prototype was presented. The presented loss models were evaluated based on a 6 kW converter prototype; measured and modeled efficiency had a good match validating the models. The converter losses were analyzed for two different operating points (40 V 1 kW and 60 V 3 kW) which are determined by the SOFC/SOEC stack characteristics.
The design highlighted how the two different converter operating modes (SOFC and SOEC) have significant variation in the distribution of the losses in the converter. Latest Trench IGBTs proved to be suitable for designing high efficiency converters achieving peak efficiency up to 96 %.However, it was observed the IGBT losses were still a large loss component and they are the main cause of the lower efficiency in SOEC mode compared to the SOFC mode. The introduction of new power semiconductors based on SiC (e.g. SiC JFETs or SiC MOSFETs) is required in order to further increase the converter efficiency especially in SOEC operating mode.

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