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VHF Series-Input Parallel-Output Interleaved Self-Oscillating Resonant SEPIC Converter

Milovan Kovacevic, Arnold Knott, Michael A. E. Andersen

Department of Electrical Engineering

Technical University of Denmark

Kgs. Lyngby, Denmark

Email: {mikov, akn, ma}@elektro.dtu.dk

Abstract—If the switches of two resonant SEPIC converters are capacitively coupled, it is possible to obtain a self-oscillating converter in which the two power stages operate in interleaved mode. This paper describes a topology where the inputs of two SEPIC converters are connected in series, thereby sharing the input voltage. For the same output power and switching frequency, the voltage stress of the switches is reduced by a factor of two while the voltage transformation ratio is doubled. This modification is possible with addition of only two capacitors in the power stage and a biasing circuit. Design considerations and challenges are investigated. To verify the proposed design, a 70 V input, 37 MHz prototype was built using low-cost switching and passive components, and experimental results are presented. Peak observed efficiency was 82%.

I. INTRODUCTION

Reducing the physical size of electronic equipment in power applications is desired in order to add more features into existing products, integrate power converters in places normally unfit for such equipment, and reduce system cost. Increasing the operating frequency of the converter is a direct way of reducing the size of energy storage elements such as bulky capacitors and inductors, which usually dominate the overall converter volume.

However, the challenges that arise when the converter operating frequency is increased into the Very High Frequency (VHF) band ranging from 30 MHz to 300 MHz are numerous. Conventional converter topologies become impractical due to high switching and gating losses [1]. Furthermore, it becomes increasingly difficult to implement high-side drivers, imposing additional limitations on converter topology selection. In recent publications, zero-voltage-switching (ZVS) converters with ground-referenced switches were almost exclusively used [2]–[8]; the only exceptions are low-voltage applications and converters-on-chip [9].

Switching losses in power semiconductor devices (discharge of the transistor parasitic output capacitance through the transistor on-resistance in a hard-switched design as well as current-voltage overlap during rise and fall times of the switching device) increase rapidly with frequency, thereby significantly reducing overall efficiency. Furthermore, parasitic reactive components cannot be ignored, since their sizes are comparable with the low capacitances and inductances resulting from the high frequency design. Commercial gate drivers for operation at VHF are rare; the fastest solution

was introduced by IXYS for operation up to 45 MHz [10]. However, this driver is relying on hard-switching of the MOSFET gate, introducing significant gating loss. Therefore, no efficient readily available gate driver IC solution exists. To obtain gate-driving signals, VHF converters today are either oscillator-driven [3], [11] or self-oscillating [12], [13].

With the exception of the Φ_2 inverter [14] and the resonant boost converter from [5], ZVS topologies typically used today are derived from or related to class E amplifier. As a consequence, the switches are exposed to high voltage stress, typically 3.6 to 4 times the input voltage at 50% duty cycle [15]. This limits the selection of the switching devices to those with high voltage rating, which implies either higher parasitic capacitances or higher on-resistance compared to a low-voltage components. In either case, worse performance and higher losses are expected. Converters based on Φ_2 inverter require additional passive components in the resonant tank, which increases the converter size and complexity and increase the conduction losses. The resonant VHF boost converter is more space/component-efficient, and the voltage stress is the same as in the conventional boost, but it is only able to step-up the input voltage; therefore is not suitable for applications where step-down voltage conversion is required.

Recently, a method for achieving self-oscillating operation of two interleaved converters has been developed [7], [16], which addresses the gate signal generation with low component count, but the voltage stress was still 3 times the input voltage. This paper presents a modification of the interleaved self-oscillating resonant SEPIC converter [16] where the converter inputs are connected in series. Compared to the parallel-input parallel output converter, the voltage stress is reduced by a factor of two, while the voltage transformation ratio is increased by the same factor for the same output power and switching frequency. This allows a wider selection of switching devices for a given input voltage, since the breakdown voltage handling capability requirement is reduced. Furthermore, it is possible to obtain galvanic isolation between the input and the output of the converter. Only a few additional passive components in the circuit are required. Section II introduces the circuit topology and operation principle. Section III presents experimental results from a designed prototype. Section IV discusses the design considerations and challenges. Finally, section V concludes the paper.

II. CIRCUIT OPERATION

Fig. 1 shows the topology of the proposed converter. Two resonant SEPIC converters [2] are capacitively coupled together, so the drain voltage of one MOSFET is used to drive the gate of the other MOSFET. Therefore, the converters operate with a phase-shift of 180° (interleaved operation). The oscillations are started automatically when the bias voltage is increased above threshold voltage (self-oscillating operation) [7], [16]. If the power stages are identical, the input voltage is shared equally between the inverter stages. The inverters are capacitively coupled to the rectifier stages via $C_{IF} - C_{IR}$ capacitor pairs. C_{IR1} and C_{IR2} are bulk capacitors, providing DC blocking and low AC impedance between the primary (input) grounds and secondary (output) ground. Therefore, the ground of the rectifiers is "floating" in respect to the ground voltage on the input side. Isolation strength is determined by the voltage rating of $C_{IF} - C_{IR}$ capacitor pairs.

As described in [16] for the parallel-input ISOR SEPIC (shown in Fig. 2), the switching frequency may be approximately determined as

$$f_S = \frac{1}{2\pi\sqrt{L_I C_{DS,tot}}} \quad (1)$$

where $C_{DS,tot}$ is the total drain capacitance seen by a switch when the rectifier is shorted:

$$C_{DS,tot} = C_{DS} + C_{GD} + C_I + \frac{C_1 (C_{GS} + C_2)}{C_1 + C_{GS} + C_2} \quad (2)$$

In Fig. 3, typical waveforms of the proposed converter are presented. Gate voltages v_{GS1} and v_{GS2} are scaled versions of v_{GS2} and v_{GS1} voltage, respectively, by a factor defined by the capacitive voltage divider; DC values of v_{GS1} and v_{GS2}

Fig. 1: Schematic of the interleaved self-oscillating resonant (ISOR) SEPIC converter with series input and parallel output (SIPO), and galvanic isolation between the inverter and the rectifier stages. "High-side" and "low-side" inverters share the input voltage. The stages are coupled via the same capacitive network as in a standard ISOR SEPIC converter.

Fig. 2: Schematic of the (parallel-input parallel-output) ISOR SEPIC converter, which does not have galvanic isolation between the input and the output.

Fig. 3: Simulated waveforms of the drain, rectifier, and gate voltages of the SIPO ISOR SEPIC converter with respect to ground at the input. $V_{IN} = 70$ V and $V_{OUT} = 12$ V. Time scale is normalized to the switching period T_S .

set by V_{B1} and V_{B2} , respectively:

$$v_{GSi}(t) = V_{Bi} + v_{DSj,ac}(t) \frac{C_1}{C_1 + C_2 + C_{GS} + C_{GD}} \quad (3)$$

$$i, j = \{1, 2\}$$

Initial input voltage distribution between the converters may be set by a pair of balancing resistors or evening out the current consumption in the biasing circuits.

III. EXPERIMENTAL RESULTS

To verify the proposed design, a proof-of-concept prototype was experimentally evaluated. The converter operation parameters are shown in Table I. Components used in the prototype are standard, low-cost semiconductor devices and passives. Capacitors in the resonant tank are 5% tolerance C0G ceramics. A complete component list is provided in Table II. Values for parasitic capacitances of the MOSFET are taken from the datasheet: $C_{GS} = 100$ pF, $C_{DS} = 21$ pF, and $C_{GD} = 7$ pF. Due to nonlinear nature of C_{DS} and C_{GD} and their dependence on v_{DS} , representative values of these capacitances are taken at the average value of v_{DS} , which is V_{IN} . With the listed components, from (1) the switching frequency is calculated as

$$f_S = \frac{1}{2\pi\sqrt{150 \text{ nH} (22 \text{ pF} + 7 \text{ pF} + 66 \text{ pF} + 21 \text{ pF})}} \quad (4)$$

$$= 38.15 \text{ MHz}$$

The achieved converter switching frequency was 37.2 MHz, which is a 2.6% error from the value predicted by (1). Efficiency of 82% was obtained for a 12 W output power; the power loss is mainly contributed by the conduction loss in the input inductor and the switch due to low Q-factor at the operating frequency, and the high on-resistance of the MOSFET.

Measured waveforms of the important voltages in the converter are shown in Fig. 5. All measurements were obtained with the oscilloscope probe connected in series with a small capacitance; therefore, the presented waveforms are scaled-down versions of the real voltages, with removed DC value. The reason for doing so is to reduce the influence of the probe on the converter operation due to impedance imbalance between d_1 and d_2 . A 2.2 pF capacitance was used in for drain and rectifier voltages, and 10 pF for the gate voltage measurements. This introduces scaling factors of 0.18 and 0.51 in the respective waveforms for a 9.5 pF passive oscilloscope probe.

High-frequency ringing is observed on top of the shown voltage waveforms, caused by the parasitic inductances of the components and the layout; especially the rectifier and the gate voltages are affected. Simulations in Spice suggest that the ringing in the rectifier while the diode is ON is due to the diode parasitic inductance, which resonates with C_I when the switch is ON, and C_I in series with equivalent drain-source capacitance C_{DS} . Similar effect holds for the stray inductance in the MOSFETs with C_I and C_R . The the gate signal ringing is caused by a superposition of two effects: gate parasitic

Fig. 4: Photograph of the experimental prototype.

TABLE I: Converter operation parameters.

input voltage V_{IN}	70 V
output voltage V_{OUT}	12 V
output power P_{OUT}	12 W
switching frequency f_S	37.20 MHz

TABLE II: List of the converter components.

Component	Value
L_{I1}, L_{I2}	Coilcraft 150 nH
L_{R1}, L_{R2}	Coilcraft 150 nH
C_{I1}, C_{I2}	66 pF (C0G)
C_{IR1}, C_{IR2}	780 pF (C0G)
C_1	27 pF (C0G)
C_2	—
C_{IN}	9.4 uF (X7R)
C_{OUT}	9.4 uF (X7R)
S_1, S_2	IR IRF5802
D_1, D_2	NXP PMEG6010

inductance ringing with the gate capacitance, and the insertion of the ringing from the power stage through C_1 and C_{GD} .

Due to imperfect matching between the components, the mid-point voltage between the converters was 33.5 V instead of intended 35 V when V_{B1} and V_{B2} are generated with biasing resistors. The reason is that the power stage with lower input voltage will have a lower bias voltage as a consequence, which further results in lower output power. Still, the converter shows a reasonably good self-balancing with no external intervention. When the biasing circuit is implemented with voltage references (VRs) in series with resistors, as shown in Fig. 6, the mid-point voltage increases to 35.5 V, thereby reducing the input voltage difference below 1.5%. The resistors in series to VRs are used to reduce the

(a) v_{DS1} : 5 V/div, 10 ns/div, scaling factor 0.18

(d) v_{DS2} : 5 V/div, 10 ns/div, scaling factor 0.18

(b) v_{R1} : 5 V/div, 10 ns/div, scaling factor 0.18

(e) v_{R2} : 5 V/div, 10 ns/div, scaling factor 0.18

(c) v_{GS1} : 2 V/div, 10 ns/div, scaling factor 0.51

(f) v_{GS2} : 2 V/div, 10 ns/div, scaling factor 0.51

Fig. 5: Experimental waveforms of the 35.3 MHz, 70 V input converter. The measurements were performed with small capacitances in series with the measurement probe to reduce the influence of the probe capacitance on the circuit operation.

power consumption of the references and to postpone the turn-on of the converter until the input voltage reaches 70 V.

IV. DISCUSSION

If the converters are ideally matched, the input voltage is shared equally between the converters. In practical implementation, the matching is never ideal and imbalance will appear in a certain degree. There are three main contributors to the imbalance in the proposed converter: asymmetry in the circuit layout, component variations, and difference in the gate bias voltages.

In order to suppress the imbalance, the converter layout has to be carefully designed. In the implementation described in this work, the layout is axially symmetrical (see Fig. 7), dictated by the pin placement of the switches. The components need to be chosen with tight tolerances. To improve capacitance matching, two or three capacitors may be used instead of one in order to reduce the equivalent series inductance and average the deviation from the desired value. This is particularly important for the gate-driving interconnection network as it influences amplitude of v_{GS1} and v_{GS2} . Use of COG/NP0 capacitors is recommended in order to suppress the voltage and

Fig. 6: Biasing circuits: passive with resistors (left) and with voltage references (right).

temperature dependence on the circuit capacitances, as well as for their high-frequency performance [17]. To further reduce variations in the converter components, as well as to increase power density of the converter, inductors may be implemented in the PCB [18].

The output power does not vary significantly with the gate

Fig. 7: Axial symmetry of the layout and component placement on the PCB.

bias voltage. However, a difference will appear if $V_{B1} \neq V_{B2}$. The most simple way to obtain V_{B1} and V_{B2} is by two pairs of biasing resistors. However, it does not guarantee equal input voltage sharing between the converters. Therefore, 5 V linear regulators are used to provide the bias voltages for the MOSFET gates, which has reduced the voltage imbalance between the converter inputs below 1.5%.

VHF converters are typically regulated using burst-mode [2]–[4] and bias voltage modulation control [5]. The interleaved converter does not show significant variation at the output with modulation of the bias voltage, therefore the converter output regulation may be obtained by implementing the burst-mode control scheme for wide load range. A mechanism for turning the “high-side” and “low-side” MOSFETs on and off needs to be provided. It is however significantly easier compared to topologies which utilize true high-side switches. The implementation of the control scheme is a subject of ongoing research.

Stacking of the inverter stages in series is not limited to 2. Each inverter may be used to drive additional inverters. The practical limitation is that the equivalent drain-source capacitance increases with each inverter stage. As a result, C_{IF} needs to be increased to maintain ZVS operation [16]. Moreover, from (1) it may be concluded that f_S will also be reduced. To maintain f_S , input inductance needs to be reduced in value, which as a consequence results in more power per converter stage. The complexity of the control circuitry also increases, as more outputs are required in the gate driver.

V. CONCLUSION AND FUTURE WORK

In this paper, the series-input parallel-output configuration of the interleaved self-oscillating resonant SEPIC topology was introduced. This topology allows a reduction of the switch voltage stress and increases the voltage transformation ratio by a factor of two compared to the parallel-input parallel-output ISOR SEPIC converter. This is achieved using a very small number of standard, low-cost components. Upsides and downsides of the presented converter are discussed, and guidelines for circumventing them are proposed. Due to non-ideal matching between the converters, additional effort is required to obtain ideal voltage balance between the converters. Proposed solution resulted in less than 1.5% in voltage difference

between the input stages. Measured waveforms of a 70 V input, 35 MHz converter were provided, reaching efficiency of 82%. As a part of the ongoing research, output regulation scheme is to be implemented. Inductors may be printed on the PCB to further increase power density and performance repeatability of the circuit.

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