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**Yan, Lei; Krozer, Viktor; Michaelsen, Rasmus Schandorph; Djurhuus, Torsten; Johansen, Tom Keinicke**

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# Physical based Schottky barrier diode modeling For THz applications

L. Yan[1], V. Krozer[2], R. Michaelsen[1], T. Djurhuus[2], T.K. Johansen[1]

[1]Department of Electrical Engineering, Technical University of Denmark, Kgs. lyngby, 2800, Denmark
[2]Goethe University of Frankfurt am Main, Frankfurt an Main, 60349, Germany
Email: krozer@physik.uni-frankfurt.de

***Abstract* — In this work, a physical Schottky barrier diode model is presented. The model is based on physical parameters such as anode area, Ohmic contact area, doping profile from epitaxial (EPI) and substrate (SUB) layers, layer thicknesses, barrier height, specific contact resistance, and device temperature. The effects of barrier height lowering, nonlinear resistance from the EPI layer, and hot electron noise are all included for accurate characterization of the Schottky diode. To verify the diode model, measured I-V and C-V characteristics are compared with the simulation results. Due to the lack of measurement data for noise behaviors, simulated noise temperature is compared with the experimental data found from the open literature.**

***Index Terms* — Schottky barrier diode, physical based model, barrier height lowering, hot-electron noise.**

## I. INTRODUCTION

Recent advances in monolithic integrated membrane technology are making Schottky diode based mixer and multiplier circuits ever more attractive [1]. Competitive mixers use Superconductor-Insulator-Superconductor tunnel junctions operating up to 1 THz and Hot Electron Bolometers operating from 1 to 7 THz. However, both types of mixers must operate at temperature below 4 K if sensitivity is stressed [2]. For commercial applications where cryogenic operation is not possible due to elevated sizes and costs, Schottky diode based technology operating at room temperature is a good candidate.

This work is a part of an effort to establish an accurate circuit model of a Schottky diode based on its physical parameters. The advantage of using a physical diode model is that the non-ideal features such as electron velocity saturation due to high electric field, barrier height lowering due to image force, and excessive noise due to hot-electrons can be included. Furthermore, with a physical device model, circuit designers can see the influence on the circuit performance due to the different fabrication parameters for example anode area, doping profile, and layer thickness. Those parameters are often used to optimize the Schottky diode characteristics for some specific applications such as mixers or multipliers [3].

## II. FEATURES OF THE MODEL

Fig. 1 shows a cross-sectional view of a planar Schottky-barrier diode. The metal-semiconductor contact is formed on top of a lightly doped EPI layer. A highly doped SUB layer with low resistance is used to form the Ohmic contact. Modulation on depletion region plays a key role for mixer and multiplier operations. Corresponding to its vertical structure, Fig. 1 also shows an equivalent circuit model of the diode. It includes two parts: 1) a junction which is represented by a parallel network with nonlinear conductance and capacitance 2) series impedance which represents the contributions from the un-depleted EPI layer, SUB layer, and Ohmic contact.

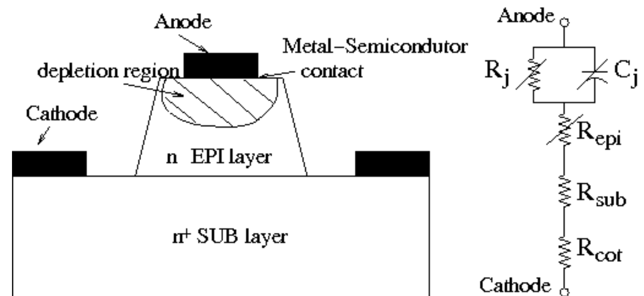


Fig. 1. The vertical structure of a Schottky barrier diode and the corresponding circuit model.

The current transport mechanism of the physical based model includes the contribution from field emission and thermionic field emission [4]. The series impedance of the diode due to the un-depleted region of the EPI layer, SUB layer, and Ohmic contact are calculated based on the anode and Ohmic contact area, depletion width, thickness and the associated conductivity of both EPI and SUB layers. For the SUB layer, the impedance due to current spreading and skin effect are considered [5]. The influence of displacement current and charge carrier inertia effects [6] within the SUB layer are represented by using a frequency dependent conductivity. The electron mobility is also a function of doping level, device temperature, and electrical field [7]. In this work, the calculation of

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depletion layer, barrier height lowering, and hot-electrons noise implementation are emphasized.

*A. Depletion width*

The variation of the depletion width is crucial for circuit analysis, because the most important model properties such as nonlinear conductance, capacitance, and resistance are all dependent on the depletion width. With the knowledge of doping levels and bias voltage, an approximation of the depletion width can be calculated by

$$w_{epi} = \sqrt{\frac{2\varepsilon}{qN_{epi}}(V_{bi} - V_j - V_T)} \quad (1)$$

where $N_{epi}$ is doping level of the EPI layer, $V_j$ is the applied voltage on the diode junction, $V_T$ is the thermal voltage, and ε is the permittivity of GaAs material. $V_{bi}$ represents the built-in potential of the junction and is derived from the barrier height $\Phi_B$ and the potential difference between Fermi level and bottom of the conduction band. Eq. 1 indicates that the depletion layer approaching zero when $V_j = V_{bi} - V_T$, but there is always a physical thin layer remaining and can be characterized by the Debye length

$$L_D = \sqrt{\frac{\varepsilon k_B T}{N_{epi} q^2}} \quad (2)$$

where $k_B$ is Boltzmann's constant. When the diode is reversely biased, Eq. 1 remains valid until the punch through voltage $V_p$ is reached where the EPI layer is completely depleted. With the condition of $w_{epi}$ equal to the total thickness of the EPI layer $T_{epi}$, the punch through voltage can be solved from Eq. 1 to be

$$V_p = V_{bi} - V_T - \frac{qN_{epi}}{2\varepsilon} T_{epi}^2 \quad (3)$$

When the applied reverse voltage is further increased, a very thin SUB layer will also be depleted. This depletion width can be calculated as

$$w_{sub} = \begin{cases} 0, & V_j \geq V_p \\ \sqrt{\frac{2\varepsilon}{qN_{sub}}(V_p - V_j)}, & V_j < V_p \end{cases} \quad (4)$$

The total depletion width of a Schottky diode is expressed as $w_{tot}=w_{epi}+w_{sub}$. Depending on the applied junction voltage, $w_{tot}$ can be formulated as:

$$w_{tot} = \begin{cases} T_{epi} + w_{sub} & for \quad V_p \geq V_j \\ w_{epi} & for \quad V_0 \geq V_j > V_p \\ P(V_j) & for \quad V_m \geq V_j > V_0 \\ L_D & for \quad V_j > V_m \end{cases} \quad (5)$$

where $P(V_j)$ is a higher order polynomial function which makes a smooth transition between $w_{epi}$ and $L_D$ for a large forward bias. $V_0=V_{bi}-3V_T$ and $V_m=V_{bi}-V_T$ is the lower and upper boundary of the transition region, respectively. With the knowledge of total depletion width and doping density of the EPI and SUB layers, the junction capacitance for each layer can be derived from Eq. 6 and Eq. 7, respectively:

$$C_{epi} = \left|\frac{dQ_{SC,epi}}{dV_j}\right| = A\frac{qN_{epi}d(w_{epi})}{dV_j} = \frac{\varepsilon}{w_{epi}}A \quad (6)$$

$$C_{sub} = \left|\frac{dQ_{SC,sub}}{dV_j}\right| = A\frac{qN_{sub}d(w_{sub})}{dV_j} = \frac{\varepsilon}{w_{sub}}A \quad (7)$$

where A is the anode area and $Q_{SC}$ is the space charge within the EPI and SUB layers. When the applied junction voltage $V_j$ is smaller than $V_p$, the capacitances of $C_{epi}$ and $C_{sub}$ are connected in series. Fig. 2 shows a typical depletion width transition when the forward bias is approaching flat band. The higher order polynomial avoids singularity of the capacitance function and results in a better convergence for the circuit simulator.

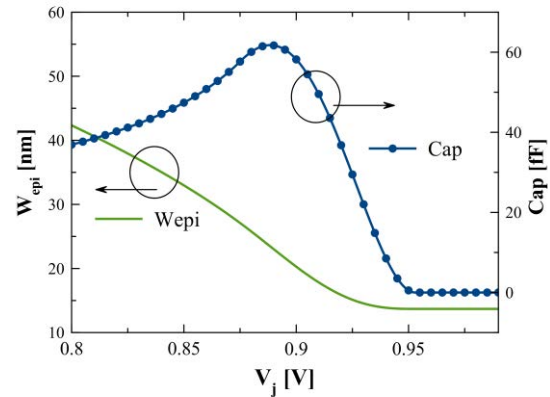


Fig. 2 Calculated junction capacitance and depletion width from Eq. 5. The numerical results are based on the assumed values of T=300 [K], $V_T$=25 [mV], $N_{epi}$=1e+23 [$m^{-3}$], $N_{sub}$=4e+24 [$m^{-3}$], $T_{epi}$=80 [nm], $T_{sub}$=5 [μm], and radius of anode contact a=2.1 [μm].

*B. Barrier height lowering*

Free electrons close to the barrier experience an image force, which lowers the Schottky barrier height for a Schottky contact. This barrier lowering has an impact on current flow across the barrier. At a distance of $x_m$ the

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barrier height lowering due to the image force is approximately

$$\Delta\phi = 2E_{\max}x_m = \sqrt{\frac{qE_{\max}}{4\pi\varepsilon}} = \sqrt{\frac{q}{4\pi\varepsilon}}\sqrt{\frac{qN_{epi}}{\varepsilon}w_{epi}} \qquad (8)$$
$$= \sqrt[\frac{1}{4}]{\frac{q^3N_{epi}}{8\pi^2\varepsilon^3}(V_{bi}-V_j-V_T)}$$

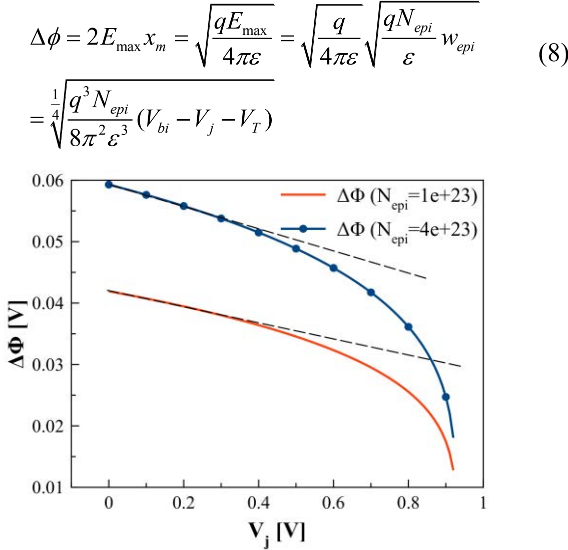


Fig. 3. Calculated barrier height lowering due to the image force from Eq. 8. The numerical results are based on the assumed values of T=300 [K], $V_T$=25 [mV], $V_{bi}$=0.95 [V], ε=1.16e-10 [F/m].

Fig. 3 shows effect of barrier height lowering due to different doping profiles. The variation of the built-in potential $V_{bi}$ is assumed to be small for both doping levels. It indicates that the higher the doping, the more the barrier height is reduced.

*C. Hot-electron noise*

The noise sources within the Schottky diode are usually divided into three parts: 1) thermal noise from series resistance from the un-depleted EPI layer, SUB layer, and Ohmic contact; 2) shot noise from conduction current through the junction; 3) excessive noise from hot-electrons. The derivation of hot-electron noise arises from electron energy and momentum balance equations [8]. The steady state solution of the equivalent noise temperature is expressed as

$$T_e = T_0 + \left[(2q^2\tau_s\tau_d E^2)/3k_B m^*\right] \qquad (9)$$

where $m^*$ is the effective electron mass and E is the electrical field. $\tau_s$ and $\tau_d$ is the mean scattering and energy relaxation time for GaAs material, which are defined by

$$\tau_s = m^*\mu_{epi}/q$$
$$\tau_d = \varepsilon/(qN_{epi}\mu_{epi}) \qquad (10)$$

By inserting the electrical field calculated from the diode current, doping level, and low field electron mobility, $T_e$ can be re-formulated as

$$T_e = T_0 + K_h I^2 \qquad (11)$$

where $$K_h = \frac{2\tau_d}{3qk_B\mu_{epi}N_{epi}^2A^2}$$

It can be seen that the excessive noise arises from the term of $K_hI^2$, which has a ～$I^2$ relationship with the junction current. An effective value of 0.5～1 [ps] is considered for $\tau_d$ in [8], but the direct calculation based on Eq. 10 shows a much smaller value. The comparison of noise temperature based on assumed and calculated $\tau_d$ is shown in Fig. 4. The results in Fig. 4 indicate that the theoretical formulation has to be adjusted by an empirical parameter, which represents the impact of the technological process and its maturity.

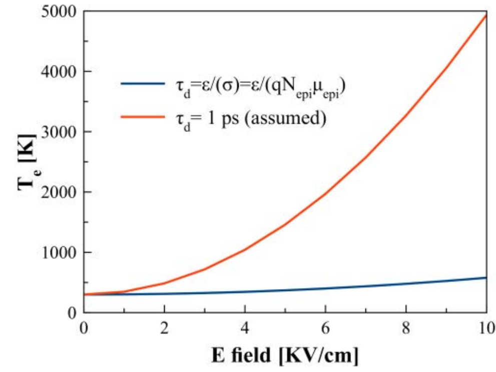


Fig. 4. Calculated equivalent noise temperature from Eq. 9. Different $\tau_d$ are considered for the noise characterization. The numerical results are based on the assumed values of T=300 K, $V_T$=25 [mV], $N_{epi}$=2e+22 [$m^{-3}$], $\tau_s$= 0.23 [ps], ε=1.16e-10 [F/m], $m^*$=0.068$m_0$, $m_0$= 9.1e-31 [kg].

## III. Model Verification

To verify the physical based diode model, the measured I-V and C-V characteristics from the fabricated Schottky diode at Chalmers and noise experimental data from the open literature are used. With the detailed knowledge of the Chalmers Schottky technology, the relevant diode parameters are set to be: T=300 [K], radius of anode contact a=0.5 [μm], effective radius of Ohmic contact b=23.9 [μm], barrier height $\Phi_b$ =1.02 [V], $N_{epi}$=5e+23[$m^{-3}$], $N_{sub}$= 5e+24 [$m^{-3}$], $T_{epi}$=48 [nm], $N_{sub}$ =2 [μm], and specific contact resistance ρ=5e-9 [$\Omega m^2$].

The comparison of I-V characteristics for an anti-parallel diode pair is shown in Fig. 5. The surface leakage for low forward bias region(< 0.4 [V]) is modeled by a parallel resistor with a value of 330 [MΩ]. As shown, there is a good agreement between the measurement and simulation result. Fig. 6 shows the junction capacitance versus voltage for the diode with an anode radius of 0.5 [μm]. The extracted capacitance data is not valid for larger bias points due to the short-circuited junction, and for reverse bias region the diode model predicts a 30% lower

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capacitance than the measurement, which might be due to a parasitic capacitance or originate from the extraction procedure where the pad to pad capacitance is de-embedded. Therefore, an extra overlapping capacitance of 0.7 [fF] is added to the result from the physical based model in Fig. 6.

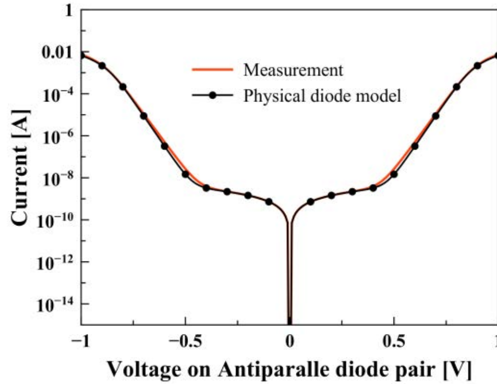


Fig. 5. The comparison of measured and simulated current-voltage characteristics for an antiparallel diode pair with an anode radius of 0.5 [μm].

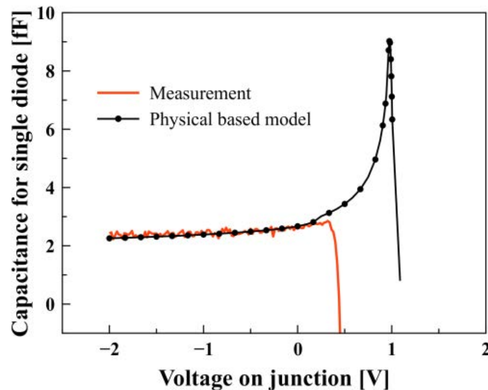


Fig. 6. The comparison of measured junction capacitance and simulation results for a Schottky diode with an anode radius of 0.5 μm.

The simulated noise temperature at 1.5 GHz is compared with measurement results from the open literature [12]. $\tau_d$ used in the calculation of hot-electron noise from Eq. 11 is increased by a factor of 20. In Fig. 7, a Schottky diode with parameters of a=1.5 [μm], $N_{epi}$ =2e+22 [$m^{-3}$], and barrier height of 0.99 [V] is used for comparison. It shows that the simulated noise temperature agrees well with the measurement.

## V. Conculsion

In this work, a physical based Schottky diode model is presented. It includes features of barrier height lowering, nonlinear resistance from the EPI layer, and hot electron noise. The I-V and C-V measurements of from fabricated Schottky diodes agree well with simulation results from the physical diode model. The predicted capacitance from

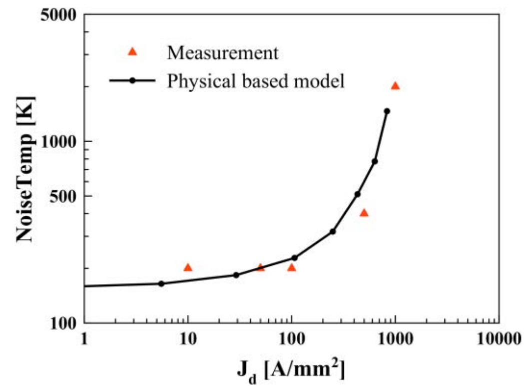


Fig. 7. The comparison of measured and simulated noise temperature at 1.5 GHz on (a) a Schottky diode with $N_{epi}$ =2e+22 [$m^{-3}$], anode radius of 1.5 [μm], and $\Phi_b$ =0.99 [V] (from [12]).

the physical model is lower than the measurements due to absence of a parasitic capacitance in the model. The noise behavior of the diode model is verified by the experimental data from the open literature. The good agreement verifies the noise sources implemented in the model.

## Acknowledgement


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