A 24 GHz integrated SiGe BiCMOS vital signs detection radar front-end

Jensen, Brian Sveistrup; Johansen, Tom K.; Zhurbenko, Vitaliy

Published in:
2013 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC)

Link to article, DOI:
10.1109/IMOC.2013.6646478

Publication date:
2013

A 24 GHz Integrated SiGe BiCMOS Vital Signs Detection Radar Front-end

Brian Sveistrup Jensen[†*], Tom K. Johansen[*], and Vitaliy Zhurbenko[*]
[*]Department of Electrical Engineering
Technical University of Denmark, 2800 Kgs. Lyngby, Denmark
Email:tkj@elektro.dtu.dk
[†]Cobham SATCOM
2800 Kgs. Lyngby, Denmark

***Abstract*—In this paper a 24 GHz integrated front-end transceiver for vital signs detection (VSD) radars is described. The heterodyne radar transceiver integrates LO buffering and quadrature splitting circuits, up- and down-conversion SSB mixers and two cascaded receiver LNA's. The chip has been manufactured in a 0.25 μm SiGe:C BiCMOS technology and its size is 1390 $\times$ 2690 μm^2. The transmitter demonstrates a maximum output power at 24 GHz of approximately -30 dBm with an externally applied LO power of 3 dBm. The receiver demonstrates a peak gain of 13.3 dB at 22.15 GHz with >10 dB return loss. The power consumption of the entire transceiver is approximately 164 mW.**

I. Introduction

Wireless sensors for the remote detection and monitoring of human vital signs has been of great interest since the first sensors were demonstrated in the early 1970's [1]. The sensitivity of wireless sensors based on microwave Doppler radars is limited due to several factors: 1) the large difference between the operation wavelength at microwave frequencies (1m to 1 cm) and the much smaller physiological movements due to heart and respiration activity, 2) reflections from stationary objects close to the human subject, and 3) interference from random body movements. Furthermore, the received low-frequency baseband signal ranging from 0.1 to 3.3 Hz may be buried in 1/f-noise coming from the electronic components, in particular the amplifiers and mixers in the receiver chain.

For reliable and robust reconstruction of the vital signs a network of sensors operating at high frequency can be explored. This requires the development of a compact low-cost radar front-end with dedicated single-chip solution. To overcome some of the limitation experienced with present VSD radars, which are mainly based on the direct conversion (homodyne) architecture [2], the low-IF heterodyne architecture with single-sideband (SSB) transmission was recently proposed by the authors [3]. Although the hardware is slightly more complex, the low-IF heterodyne architecture reduces or completely eliminates the problems with 1/f-noise, DC offset errors, and I/Q channel mismatches. To the best of the author's knowledge the transceiver front-end presented in this paper represents the first integrated vital signs detection radar chip built to demonstrate this concept.

The paper is organized as follows. At first, section II gives an overview of the integrated transceiver front-end. Section III explains the sub-circuit designs in details. The experimental results of the chip is presented in section IV. Finally, section V concludes the paper.

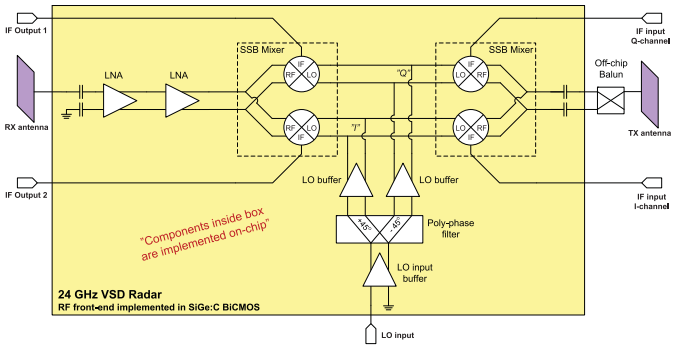

Fig. 1. Schematic of the implemented VSD radar front-end IC.

II. Chip Overview

The full VSD radar front-end has been designed and manufactured as an integrated circuit (IC) in the 0.25 μm SG25H3 SiGe:C BiCMOS technology from the German institute "Innovations for High Performance Microelectronics GmbH", abbreviated IHP. The technology features five metal layers from which the two topmost layers are thicker for improved implementation of inductors and microwave structures. The high frequency npn heterojunction bipolar transistor (HBT) available in this technology features $f_t/f_{max} = 110/180$ GHz while having breakdown voltages of 2.3 V.

Fig. 1 shows the schematic overview of the implemented IC. It consists of a transmitter chain (Tx) and a receiver chain (Rx) both of which utilize I/Q mixer topologies for SSB operation. The LO signal is split in $\pm 45^o$ branches through a second-order poly-phase filter network and buffers help maintain LO signal strength all the way to the mixers. An additional input buffer has been implemented on the LO port to lower the LO input power requirements even further. In order to ease testing of the IC, the LO generator is not implemented on-chip. The IF input (I and Q) are fed from an external source to provide a mean for optimizing image rejection (IR) performance through external adjustment of phase- and amplitude balance. At the Tx output, an external balun is needed to transform the differential output signal into a single-ended signal for the Tx antenna. The Tx output is taken directly following the SSB mixer without further amplification. This leads to a low transmitted power

978-1-4799-1397-8/13/$31.00 ©2013 IEEE

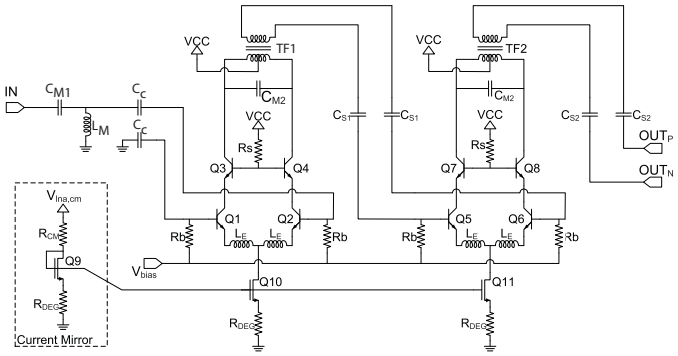

Fig. 2. Schematic of transformer-loaded LNA.

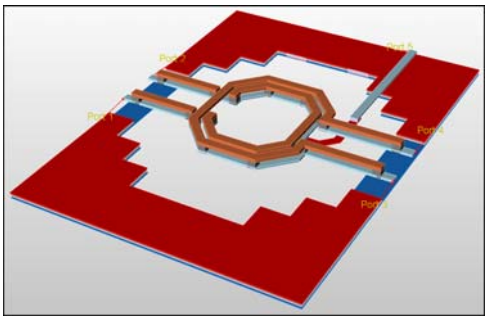

Fig. 3. 3D rendering of the transformer simulation setup in Agilent ADS 2011.

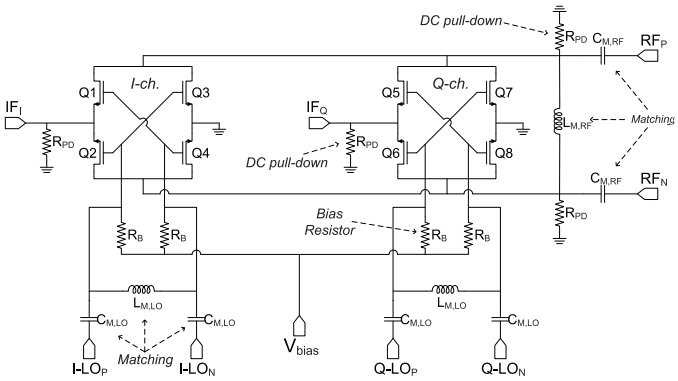

Fig. 4. Schematic of the single-sideband mixer core.

around -30 dBm. This level, however, was found sufficient due to the expected short distance to the human subject (typically 1-2 m). The Rx chain consists of two cascaded LNA's designed to provide approximately 27 dB of gain before entering the down-conversion mixer. The mixer conversion loss has been designed to be approximately 14 dB, indicating an expected total receiver gain of approximately 13 dB. Although only one IF output is needed, both branches of the I/Q mixer is taken out of the chip. When retrieving only one IF output, the expected receiver gain thus drops to approximately 10 dB (i.e. 3 dB lower).

As indicated in the schematic, the entire chip has been implemented using differential designs. This ensures that common-noise rejection and DC offsets are lowered considerably; two factors which can be rather high when implementing circuits on lossy substrates such as Silicon. The only exception is the IF input and output branches, which are implemented single-ended. However, as shown in the next section, the mixer cores are still operating in a differential fashion.

III. Sub-Circuit designs

In this section the design of the sub-circuits in the VSD radar transceiver chip is described.

A. Transformer-loaded LNA

Fig. 2 shows a circuit schematic of the two cascaded LNA's. The core of each amplifier is based on a cascode bipolar differential pair. The input signal is provided single-ended through the coupling capacitors C_c while C_{M1} and L_M provide input matching. Biasing of the bipolar pairs Q_1/Q_2 and Q_5/Q_6 is provided externally through bias resistors R_B. The emitter inductors, L_e, which are rather small are provided for a trade-off between gain and bandwidth performance. The cascode transistors Q_3/Q_4 and Q_7/Q_8 are biased directly to VCC through resistors R_s. The bias current for each stage is provided through a bipolar current mirror which is degenerated through R_{DEG}.

Each amplifier is loaded by a transformer with a center tap in one coil for DC biasing. As presented in [4], [5], the use of transformers have several advantages, as compared to a more traditional topology using inductors for loading of a single amplifier. First of all it provides direct AC coupling between the output and the input of the next stage. Furthermore, as the base input of the HBT (or gate of a MOS) is inherently capacitive, the secondary coil of the transformer acts as a direct matching component between the output and the input of the next stage. For precise tuning of the load transformer, the capacitors C_{M2} and C_{s1}/C_{s2} are included in the LNA design as shown in Fig. 2.

The transformer was optimized separately using electromagnetic simulations in Agilent ADS 2011. A 3D rendering of the transformer simulation setup with center tap on one coil for DC biasing is shown in Fig. 3. The stacking of multiple metal layers was investigated to lower series resistance in the coils but was actually found to reduce the quality factor Q due to increased capacitive coupling to the substrate. It was also found, that capacitive coupling eliminated the benefit of a patterned ground shield often included to minimize the induction of eddy currents in the substrate. A surrounding ground ring structure was included in the periphery of the transformer design. This ground ring allows a better control of the surroundings and a well-defined path for the return current during simulations. The performance of an integrated transformer can be assessed in terms of its so-called Transformer Characteristic Impedance (TCR) which is proportional to the available output power from the LNA [4]. An TCR higher than 800 Ω was obtained at the design frequency of 24 GHz for the optimized structure. This compares well with the 900 Ω reported for the optimized transformer structure in [5] at a similar frequency.

B. Doubled-balanced single-sideband mixers

Fig. 4 shows the core of the single-sideband mixer. It consists of two identical double-balanced FET resistive ring mixers. Double-balancing is important for isolation between

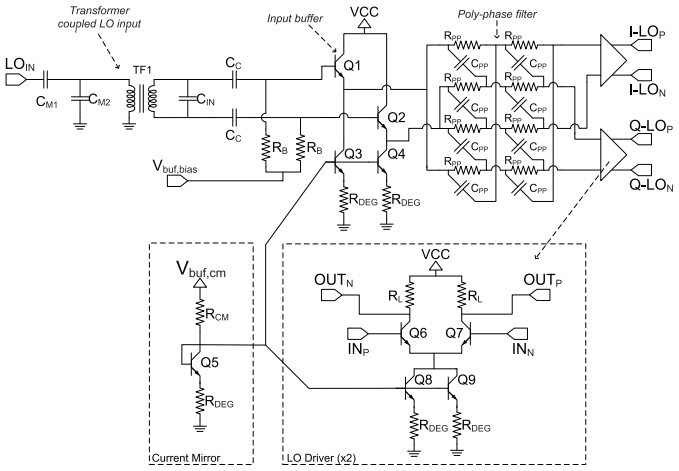

Fig. 5. Schematic of the LO input buffer, poly-phase filter for 90 degree split and LO driver for mixer inputs.

different inputs and outputs of the mixer, and ensures that leakage should be kept at a minimum. The passive FET mixer is incapable of conversion gain but it can be used for both the up- and down-conversion process. This means that the same mixer structure can be used for the transmit and receive path. Using a passive FET resistive topology also reduces 1/f-noise compared to topologies with a DC biasing current [6]. The 1/f-noise in the receiver mixers remains problematic even in the low-IF heterodyne architecture.

As shown in Fig. 4, the RF signal is split between each mixer. A combined matching is provided through the differentially operated inductor $L_{M,RF}$ and the series capacitors $C_{M,RF}$. Each of the LO input ports (I and Q) are fed through a similar matching network and combined with a DC bias voltage through a set of large resistors, R_B. This biasing lowers the requirements to the LO power needed to switch the MOS devices. The DC current, caused by the biasing will be kept low through a set of large DC pull-down resistors, R_{PD}, those purpose is to ensure a close-to-zero DC voltage on all drains and sources of the devices. The IF signal from each mixer is taken single-ended with the unused output connected to ground.

C. LO input buffer with poly-phase filter

The quadrature LO inputs required for the single-sideband mixers are generated by a second-order poly-phase filter circuit, [7], as shown in Fig. 5. The externally, provided single-ended LO signal is coupled into the circuit through the transformer, $TF1$, which makes the LO signal differential. The single-ended matching of the LO inputs is provided through C_{M1} and C_{M2} and is necessary in order to be able to connect the transformer to ground. C_{IN} provides matching between the transformer and the input buffer consisting of two parallel emitter followers, Q_1 and Q_2. The capacitors C_c acts as DC blocks such that the emitter followers can be biased through the R_B resistors.

As the poly-phase filter is inherently lossy, LO drivers are needed to provide the two mixers with an adequate LO signal swing. The LO drivers are implemented as bipolar differential stages (Q_6 and Q_7) using double the amount of tail current

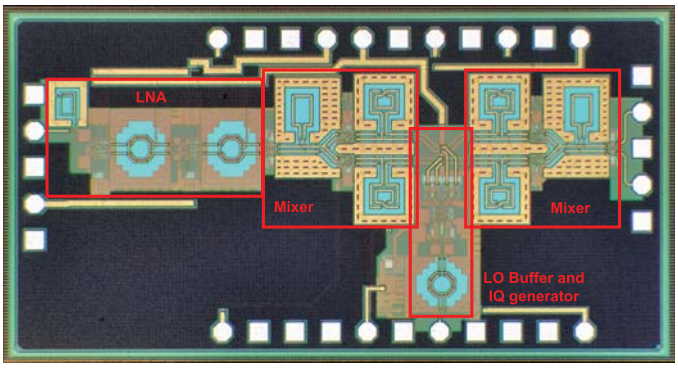

Fig. 6. Chip photo of the VSD IC fabricated in the IHP SG25H3 SiGe:C BiCMOS technology.

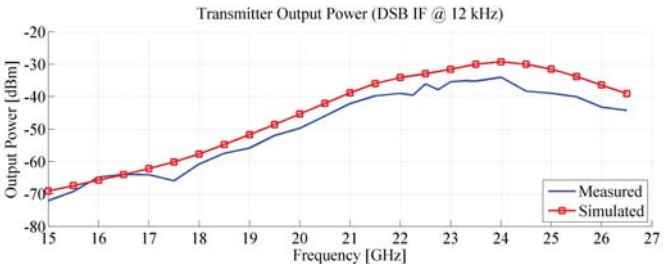

Fig. 7. DSB output power as function of LO frequency at an IF drive level of 26 mVpp at 12 kHz. LO input power was set to 0 dBm.

as the input buffers. The bases of the differential pair are biased directly through the emitter DC voltage of the emitter followers and thus do not need an additional bias voltage. Current sources for the entire LO input chain is provided through a bipolar current mirror setup using the same reference (Q_5). Degeneration resistors, R_{DEG}, are used for higher output resistance in the current sources. Both the buffer bias voltage, $V_{buf,bias}$, and the current mirror reference supply, $V_{buf,cm}$ are externally fed to the circuit in order to be able to adjust the biasing when testing the IC.

IV. Experimental Results

Fig. 6 shows a photo of the manufactured VSD chip with the different circuit blocks marked by rectangles and labels. The dimensions of the IC is 1390 $\times$ 2690 μm^2. The chip has been measured on-wafer and consumes a power of approximately 164 mW.

At first the transmitter block has been tested using an Anritsu MG3694A 40 GHz signal generator for the LO input and a TTi TG120 20 MHz function generator for the IF input. The RF output power has been measured on an HP 8563E spectrum analyzer taking into account all losses related to cables and interconnects. Throughout the testing the IF frequency was set to 12 kHz. Fig. 7 shows the measured output power including both sidebands from the transmitter using a 0.26 mVpp IF signal and 0 dBm LO power. As seen, the transmitter has a center frequency of approximately 24 GHz as intended. However, the output power is approximately 5 dB lower than simulations. The reason for this could be an underestimation of the losses in the critical matching inductors of the mixer and a lowering of the LO drive level provided by the LO buffer network. The output power as a function

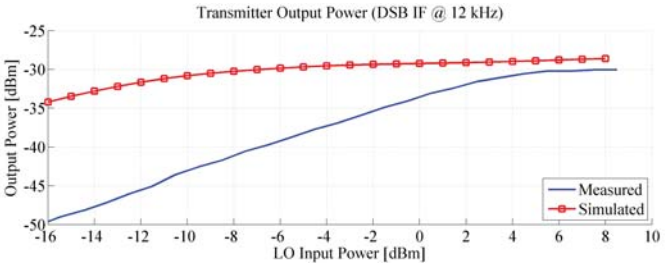

Fig. 8. DSB output power as function of LO input power at 23 GHz with all other parameters constant.

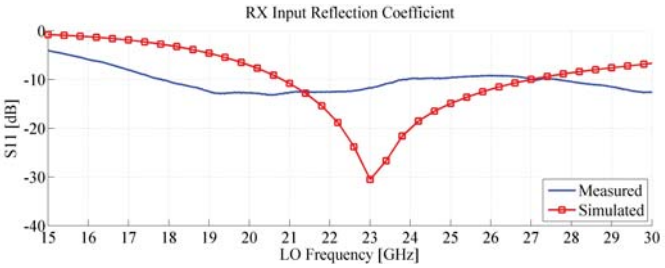

Fig. 9. Reflection measurements versus frequency at the receiver input.

of LO input power at 23 GHz is shown in Fig. 8. A large difference between measured and simulated output power is observed especially at lower LO input power levels. This indicates that the model employed for the passive MOS devices in the switching quad is inaccurate in the quasi-linear region. It is also observed that the LO buffer network is not fully saturated at 0 dBm LO power which may explain part of the observed difference in Fig. 7. At the maximum drive level (10 dBm) provided by the Anritsu RF generator, the output power is approximately -30 dBm. The image rejection was tested at 1 kHz where an IF quadrature splitter was available and gave an suppression of the unwanted sideband of more than 40 dB. This shows that the IC with the correct IF circuitry can be configured to function as a single-sideband transmitter.

The return loss of the receiver, as shown in Fig. 9, has been measured on an Anritsu ME7808B VNA. Although comparison to simulation reveals a small down-shift in frequency and a poorer match, the return loss remains better than 10 dB for the band between 18 and 24 GHz. This is acceptable for the targeted application. The down-conversion operation of the receiver has been measured in a loop back test, where the output of the transmitter has been connected to the input of the receiver. Fig. 10 shows the measurement of the receiver gain when the variations in the transmit power has been compensated for. It is seen that the receiver is shifted slightly down in frequency, with a peak gain of 13.3 dB at around 22.15 GHz. Nonetheless, the receiver produces sufficient gain through the down-conversion process and it can be concluded that the chip seems usable in a VSD system.

V. Conclusion

A 24 GHz SiGe BiCMOS VSD radar front-end chip has been presented. The chip integrates a low-IF heterodyne radar transceiver and can be configured for single-sideband transmission by providing IF signals in quadrature phase. The chip is designed for a high carrier frequency of 24 GHz

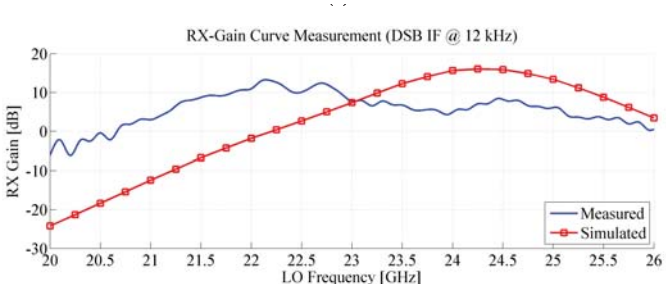

Fig. 10. Receiver gain measurements performed with a loop-back test of the transmit signal.

potentially reducing size and increasing the sensitivity of future VSD sensor networks.

Acknowledgment

The authors would like to thank the Danish fund, H. C. Ørsteds Fonden, for financial support.

References

[1] J. C. Lin, "Microwave Movement Sensing of Physiological and Volume Change: A Review," Bioelectromagnetics, vol. 13, No. 6, pp. 557-565, 1992.

[2] A. Droitcour et al., "Range Correlation and I/Q Performance Benefits in Single-Chip Silicon Doppler Radars for Noncontact Cardiopulmonary Monitoring," IEEE Trans. Microwave Theory and Tech., vol. 52, No. 3, pp. 838-848, March 2004.

[3] B. S. Jensen, S. P. Jonasson, T. K. Johansen, and T. Jensen, "Vital signs detection radar using low intermediate-frequency architecture and single-sideband transmission," in Proc. 9th European Radar Conference, pp. 67-70, Amsterdam, The Netherlands, Nov., 2012.

[4] F. Carrara et al., "Design Methodology for the Optimization of Transformer-Loaded RF Circuits," IEEE Trans. Circuits and Systems, vol. 53, pp. 761-768, April 2006.

[5] V. Ragonese et al., "A SiGe BiCMOS 24-GHz Transceiver Front-end for Automotive Short-Range Radar," Analog Integrated Circuits and Signal Processing, vol. 67, pp. 121-130, Oct. 2011.

[6] C. Song et al.,"0.18-μm CMOS Wideband Passive Mixer", Microwave and Optical Tech. Letters, vol. 55, no.1, Jan. 2013.

[7] J. Kaukovuori et al., "Analysis and Design of Passive Polyphase Filters," IEEE Trans. Circuits and Systems, vol. 55, pp. 3023-3037, Nov. 2008.