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Strain at a semiconductor nanowire-substrate interface studied using geometric phase analysis, convergent beam electron diffraction and nanobeam diffraction

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Semiconductor nanowires have been studied using electron microscopy since the early days of nanowire growth, e.g. [1].

A common approach for analysing nanowires using transmission electron microscopy (TEM) involves removing them from their substrate and subsequently transferring them onto carbon films. This sample preparation method is fast and usually results in little structural change in the nanowires [2]. However, it does not provide information about the interface between the nanowires and the substrate, who's physical and electrical properties are important for many modern applications of nanowires. In particular, strain and crystallographic defects can have a major influence on the electronic structure of the material. In improved method for the characterization of such interfaces would be valuable for optimizing and understanding the transport properties of devices based on nanowires.

Here, we systematically investigate the interface between a nanowire and its substrate using three complementary methods for assessing strain. Results obtained using high resolution TEM for geometric phase analysis (GPA), convergent beam elecron diffraction (CBED) and nanobeam electron diffraction (NBED) are compared and contrasted. GPA measurements were acquired at 300kV in an FEI Titan 89-300 while the two diffraction methods were applied in the same microscope at 120kV. The GPA analysis software developed by C.T. Koch and V.B. Özdöl was used [3].

For samples other than nanowires, previous comparisons of GPA with CBED and NBED [4,5] have shown a high degree of consistency. Strain has previously only been measured in nanowires removed from their substrate [6], or only using GPA [7].

The sample used for the present investigation was an InP nanowire grown on a Si substrate using metal organic vapor phase deposition (MOCVD). Lattice missmatch between Si and InP is 8%. The nanowire had a diameter of approximately 100 nm in the interface area. TEM samples were prepared using a tripod polishing technique, with Ar ion milling used as the final thinning step. The resulting sample was clean and virtually free from defects from sample preparation. Measurements using all three techniques were obtained from the same well defined region of the specimen. Energy dispersive X-ray spectroscopy (EDS) maps were also acquired from the same area.

Preliminary results acquired using GPA are shown in Figure 1. Whereas the base of the wire show some strain, little strain is observed in the substrate. The influence of defects, interfacial layers and compositional variations on the GPA will be discussed.

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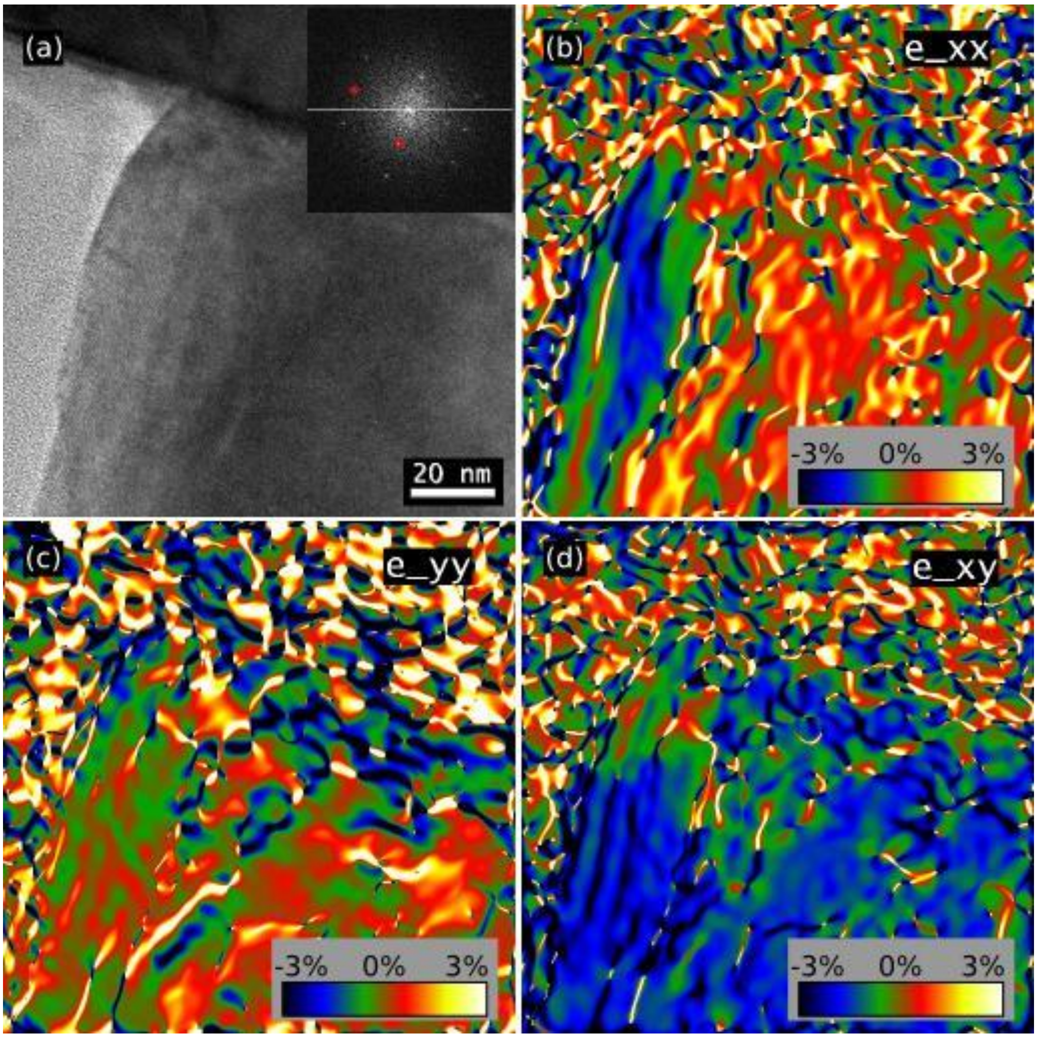

Figure 1. (a) Bright-field high-resolution TEM image of an InP nanowire/Si substrate interface. The inset shows a diffractogram and the two peaks used to determine the strain maps. **(b)** ε_{xx} strain map calculated from the same region. The area on the right shows an anomaly that may result from lateral overgrowth in this region. **(c)** ε_{yy} strain map showing little strain in the y direction in the area on the right. **(d)** ε_{xy} strain map, showing a low amount of shear.