



## **4G Mobile Networks**

An Analysis of Spectrum Allocation, Software Radio Architectures and Interfacing Technology

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4G Mobile Networks:

An Analysis of Spectrum Allocation,  
Software Radio Architectures and  
Interfacing Technology

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*Christian F. A. Lanzani*

Industrial Ph. D. Thesis

A thesis submitted for the degree of  
*Industrial Doctor of Philosophy of the Technical University of Denmark,*  
Department of Photonics Engineering, Kgs. Lyngby, Denmark  
in collaboration with the Ministry of Technology of Denmark and  
in collaboration with Radiocomp ApS, Hilleroed Denmark.





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*Christian F. A. Lanzani*

Hilleroed, Denmark

October 31<sup>th</sup>, 2010



*Dedicato alla mia splendida nonna Lina ... ci sarai sempre.*



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Christian F. A. Lanzani

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October 31<sup>th</sup>, 2010





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# Abstract

This thesis has investigated 4G radio access networks covering spectrum allocation methodologies, eNB software radios and architectures including interfacing performance aspects relevant for IMT-Advanced requirements.

Dynamic spectrum allocation is an alternative to fixed allocation methodologies. Although 100 MHz of spectrum per antenna will require frequencies re-allocation - initial rollouts with bandwidths of 40 MHz leveraging Carrier Aggregation and MIMO antenna techniques are foreseen within a 3-years time horizon. MultiRAN and high-power eNB configurations are expected to operate in the 1.7-2.6 GHz bands. Likewise, SingleRAN low-power configurations will operate in the 2.6-3.8 GHz bands allowing equipment manufactures to focus on a limited number of systems and configurations. An SCR architecture is proposed based on SoC integration of both digital and analog functions allowing modularity and flexibility with a reduced footprint and equipment cost reduction.

Baseband to radio interfaces were analyzed representing the future of open and distributed eNB architectures. A contribution on carrier grade capacity analysis and interface interoperability enhancements was presented. Likewise, system synchronization and delay management - relevant because of the remote nature of OBSAI/CPRI equipment supporting reliable multi-hop applications - were thoroughly analyzed. A new architecture for a serial receiver circuitry - the main source of interface delay measurement inaccuracy - is presented enabling 100 ps of theoretical resolution for delay variance.



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# Resume (in Danish)

Denne afhandling omhandler 4G radio access-netværk og dækker frekvenstildelingsmetoder, eNB softwaredefinerede radioer og arkitekturer, herunder signaleringsaspekter relevante for IMT-Advanced.

Dynamisk frekvensallokering er et alternativ til faste tildelingsmetoder. Selv ved 100 MHz spektrum per antenne vil det kræve frekvensomfordeling - første rollouts med båndbredder på 40-MHz udnytter sammenlægning af bærebølger, og MIMO-antenneteknikker, og er planlagt inden for en 3-årig tidshorisont. MultiRAN og høj-effekts eNB konfigurationer forventes at operere i 1.7 - 2.6 GHz-båndet. Ligeledes vil SingleRANs energibesparende konfigurationer opererende i 2.6-3.8 GHz-båndet give udstyrsfabrikanterne mulighed for at fokusere på et begrænset antal af systemer og konfigurationer. En SCR arkitektur er foreslået på grundlag af SoC integration af bde digitale og analoge funktioner, og den giver modularitet og fleksibilitet med et reduceret fodspor og reduktion af udstyrsomkostninger.

Basisbåndsfrekvens- til radiofrekvensens-grænseflader blev analyseret, og de repræsenterer fremtiden for åbne og distribuerede eNB arkitekturer. Der bliver tillige præsenteret et forslag til Carrier Grade kapacitetsanalyser og interface interoperabilitets-forbedringer. Ligeledes bliver systemsynkronisering og forvaltning af forsinkelse til understøttelse af pålidelige multi-hop-applikationer (der er relevant på grund af, at OBSAI / CPRI udstyr står fjernt fra hinanden) grundigt analyseret. En ny arkitektur for et serielt modtagerkredsløb med 100 ps teoretisk opløsning af forsinkelsesvarians præsenteres.



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# Publications

## Peer Reviewed Journal Papers

C. Lanzani, G. Bergamo, and M. Hoegdal, “Analysis of clock distribution and delay management for IMT-Advanced distributed wireless base station systems,” *Frequenz: Journal of RF-Engineering and Telecommunications*, December 2010 [1]

## Peer Reviewed Conference Proceedings

C. Lanzani, G. Bergamo, and M. Hoegdal, “Analysis of clock distribution and delay measurements for multi-hop remote radio applications,” in *6th Karlsruhe Workshop on Software Radios* (I. . K. I. of Technology Communications Engineering Lab, ed.), (Karlsruhe, Germany), pp. 146–152, March 3/4 2010 [2]

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### Refereed Conference Presentations

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C. Lanzani, “A path toward unified remote radio interface,” in *IWPC Workshop on Flexible 4G Base Station Architectures*, ([www.iwpc.org](http://www.iwpc.org)), 2008 [8]

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# Abbreviations and Acronyms

## A

**ADC** Analog-to-Digital Converter  
**AGC** Automatic Gain Control  
**AL** Application Layer  
**ASIC** Application Specific Integrated Circuit  
**ATM** Asynchronous Transfer Mode  
**AWS** Advanced Wireless Services

## B

**BBM** Base-Band Module  
**BER** Bit Error Rate  
**BF** Basic Frame  
**BOM** Bill Of Materials  
**BTS** Base Transceiver Station  
**BW** BandWidth

## C

**CA** Carrier Aggregation  
**CC** Component Carrier  
**CAPEX** Capital Expenses  
**CCM** Clock and Control Module  
**CDR** Clock Data Recovery  
**CN** Core Network  
**CoMP** Coordinated Multi Point transmission  
**COTS** Common off the Shelf  
**C-Plane** Control Plane  
**CPRI** Common Public Radio Interface  
**CLK** Clock

**CPU** Control Processing Unit  
**CR** Cognitive Radio  
**CRC** Cyclic Redundancy Check  
**C&M** Control and Management

## D

**DAC** Digital-to-Analog Converter  
**DCF** Digital Communication FPGA  
**DCU** Digital Communication Unit  
**DDC** Digital Down Converter  
**DSA** Dynamic Spectrum Allocation  
**DSL** Digital Subscriber Line  
**DSP** Digital Signal Processing  
**DUC** Digital Up Converter  
**DL** DownLink  
**DPC** Discrete Processing Core  
**DPD** Digital Pre Distortion

## E

**eNB** Evolved NodeB  
**EPC** Evolved Packet Core



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## F

**FCB** Frame Clock Burst  
**FCS** Frame Check Sequence  
**FDD** Frequency Division Duplexing  
**FSA** Fixed Spectrum Allocation  
**FS** Frequency Synthesizer  
**FSM** Finite State Machine  
**FPGA** Field Programmable Gate Array

## G

**Gbps** Giga bits per second  
**GPP** General Purpose Processor  
**GPS** Global Positioning System  
**GSM** Global System/Standard Mobile

## H

**HARQ** Hybrid Automated Repeat Request  
**HSEVB** High Speed Evaluation Board  
**HDS** Hardware Defined Sub-system  
**HSDU** High Speed Digital Unit  
**HW** Hardware

## I

**IEEE-SA** Institute of Electrical and Electronics Engineers - Standards Association  
**IC** Integrated Circuit  
**IF** Intermediate Frequency  
**IMT** International Mobile Telecommunications  
**IP** Internet Protocol  
**IPR** Intellectual Property Right  
**IQ** In-phase and Quadrature  
**ITU** International Telecommunication Union

## L

**L1** Layer 1  
**L2** Layer 2  
**L3** Layer 3  
**LC** Local Converter  
**LNA** Low Noise Amplifier  
**LO** Local Oscillator  
**LSB** Least Significant Bit  
**LTE** Long Term Evolution  
**LVDS** Low Voltage Differential Signaling  
**LU** Local Unit

## M

**MAC** Media Access Control  
**Mbps** Mega bits per second  
**MCU** Micro Controller Unit  
**ME** Mobile Equipment  
**MF** Master Frame  
**MSB** Most Significant Bit  
**MG** Message Group  
**MGT** Multi Gigabit Transceiver  
**MIMO** Multiple In Multiple Out  
**MIPS** Million Instructions Per Second  
**MC** Multi Carrier  
**MSR** Multi Standard Radio  
**MUX** Multiplexer

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## O

**OAM&P** Operation Administration Maintenance & Provisioning  
**OCXO** Owen Controller Crystal Oscillator  
**OEM** Original Equipment Manufacturer  
**OBSAI** Open Base Station Architecture Initiative  
**OPEX** Operating Expenses  
**ORI** Open Radio Interface  
**OS** Operating System  
**OSI** Open Systems Interconnection

## P

**PA** Power Amplifier  
**PAR** Peak to Average Ratio  
**PCB** Printed Circuit Board  
**PCS** Physical Coding Sub Layer  
**PLL** Phase-Locked Loop  
**PRC** Primary Reference Clock  
**PRBS** Pseudo Random Bit Sequence

## Q

**QAM** Quadrature Amplitude Modulation  
**QoS** Quality of Service

## R

**RAN** Radio Access Network  
**RAM** Read Access Memory  
**RAT** Radio Access Technology  
**RATG** Radio Access Technology Group  
**RF** Radio Frequency  
**RFM** Radio Frequency Module  
**RFT** Radio Frequency Transceiver

**RNC** Radio Network Controller  
**RNS** Radio Network Subsystem  
**RMS** Root Mean Square  
**ROM** Read Only Memory  
**RTL** Register Transfer Logic  
**RTT** Round Trip Time  
**RP** Reference Point  
**RoF** Radio over Fiber  
**RRH** Remote Radio Head unit.

## S

**SAP** Service Access Point  
**SCR** Software Configurable Radio  
**SDH** Synchronous Digital Hierarchy  
**SDR** Software Defined Radio  
**SERDES** SERializer DESerializer  
**SEM** Spectral Emission Mask  
**SF** System Frame  
**SFN** System Frame Number  
**SFP** Small Factor Pluggable  
**SOAP** Simple Object Access Protocol  
**SoC** System on a Chip  
**SPC** Soft Processing Core  
**SPI** Serial Peripheral Interface  
**S-Plane** Synchronization Plane  
**SR** Software Radio  
**SSC** Spectrum sharing and Co-existence  
**SYNC** Synchronization signal

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## T

**TBTS** Traditional Base Station System

**TDD** Time Division Duplexing

**TDM** Time Division Multiplexing

**TMA** Tower Mounted Amplifier

**TMB** Tower Mounted Booster

**TM** Transport Module

**TRX** Transceiver

**TTR** Time To Repair

**TWG** Technical Work Group

## #

**2G** Second Generation GSM Mobile Networks

**3G** Third Generation UMTS Mobile Networks

**4G** Fourth Generation LTE Mobile Networks

## U

**UMTS** Universal Mobile Telecommunication  
Standard

**UL** UpLink

**U-Plane** User Plane

**UTRAN** Universal Terrestrial Radio Access  
Network

## V

**VCO** Voltage Controlled Oscillator

**VHDL** Very High Speed Hardware Descrip-  
tion Language

**VCXO** Voltage Controlled Crystal Oscillator

## W

**WINNER** European Wireless World Initia-  
tive New Radio

**WiMAX** Worldwide Interoperability Multiple  
Access

**WCDMA** WideBand Code Division Multiple  
Access

**WRC** Worldwide Radio Conference

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# Preface

Access to information anywhere and anytime will characterize new kinds of information systems in the 21st Century. In the last decade, rapidly emerging communications systems - of which many are based on radio frequency transmissions such as cellular telephony, personal communications systems, and wireless local and metropolitan area networks - have been growing rapidly. In today's lifestyle there is a common need to access a multitude of information over the Internet. Search engines, email, and voice communications, video and music streaming or sharing, social networking, and online gaming but only few examples of this demand.

Over the last 15 years several wireless standards have been introduced into the cellular market and each geographical region has developed a different set of radio access technologies based mostly on Global System Mobile (GSM) and Code Division Multiple Access (CDMA) because of specific regional frequency allocation and policies. At the same time, the Wireless Local Area Networks (WLAN) have introduced shorter-range data connectivity technologies based on Orthogonal Frequency Division Multiple Access (OFDMA) modulation schemes. WLANs support a continuously increasing traffic capacity albeit with limited coverage and at a reduced performance regarding mobility.

The Global System/Standard Mobile (GSM) technology, also known as second-generation (2G) networks, has been the critical step toward mass introduction of mobile voice services, in part driven by the introduction of roaming between different national networks. This in turn has enabled the worldwide spread of devices that can be used seamlessly across different geographical regions. The GSM systems were initially meant to carry mostly voice and short text traffic using a small available bandwidth. Later, third generation (3G) systems were introduced and were intended to deliver data-oriented services with higher throughput and mobility. However, initial 3G system did not reach high theoretical data rates targets and have since been subjected to a multitude of relatively costly upgrades for enhancing the performance, including High Speed Packet Access (HSPA). Any further increase of performance meeting 4G network requirements must include increased spectrum availability, requiring larger portions of spectrum and new dynamic access methodologies enabled by open base station architectures and advances in radio technology.

Based on 3G and the increasing popular demand for data services, the latest advances in radio and software engineering have been driving the mobile & wireless network industry toward a fourth generation of networks (4G).

4G networks are characterized by an expansion in available bandwidth and by simplified radio access systems with flat, IP-based network architecture. The radio access part includes not just one technology or standard, but rather consists of a collection of technologies and protocols that will enable high throughputs and performance for a given spectrum availability. 4G radio access also needs to support legacy systems using existing standards.

Despite the fact that such a process of convergence is likely to take the next five to ten years to be fully established, the work towards designing 4G network architectures already started few years back. Today, research and development from commercial industry players as well as the academic community is being incorporated into the first generation of 4G products for open and distributed eNb architectures, the latter specifically making use of remote radio head concepts. The increased market demand for broadband mobility and flat rate data subscriptions have however created a gap between the network costs and the aggregate network revenue, requiring of operators that they employ new cost-effective and future proof broadband radio access technologies in order to return to profitability. Fig.1 shows the de-coupling between the increase of traffic volume and revenue in the change from late 3G systems toward 4G, driving the industry to adopt more cost-efficient technologies to ensure that new network investments are profitable.

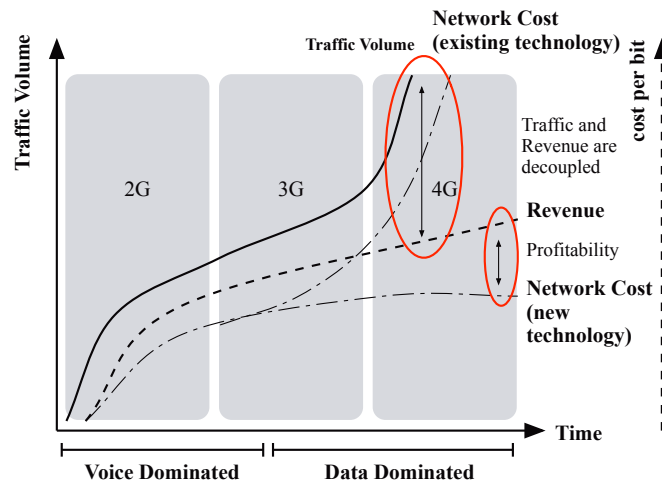


Figure 1: Trend in Traffic Volume, Revenue and Cost per bit from 2G voice dominated networks to 4G data dominated networks. It shows the decoupling between the traffic and revenue due to the flat data rate services demand. Network equipment and operations cost has to be minimized to ensure network profitability.

The fragmentation of standards across the respective geographical locations and nature for both the cellular and WLAN technology paths are shown in Fig.2. Each path evolved its performance in separate stages over time, as in their initial releases each standards theoretical peak data rates were not met in practical deployments.

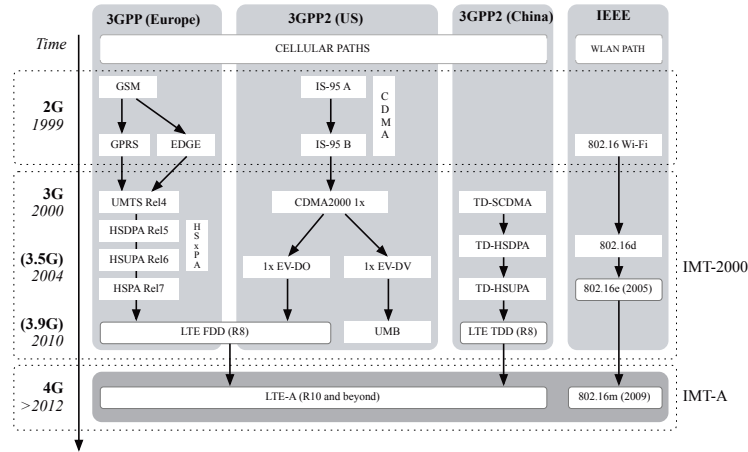


Figure 2: Mobile and WLAN technologies evolution paths toward 4G mobile wireless networks. 3G networks were characterized by a large standard fragmentation according to the geographical regions. 4G aims at converging the evolved 3G standards into a common IMT-Advanced technology based on LTE / LTE-Advanced and 802.16m standards.

The 3GPP Long Term Evolution (LTE) and the IEEE Worldwide Interoperability for Microwave Access (WiMAX) 802.16x are the two major evolutionary paths for mobile broadband wireless for the next 10 years. The 3GPP LTE-Advanced (LTE-A) Release 10 and the IEEE 802.16m (WiMAX2) are the respective candidate standards for IMT-A approval submitted in late 2009.

The splitting of the macro base station into separate pieces has allowed the major components of these distributed base station topologies to be considered as subsegments of the overall wireless infrastructure hardware market. This transformation has been accompanied by a change in the perception of remote radio heads in the overall evolved NodeB (eNB) hierarchy as efficiency, small size, ease of placement in relation to antennas, and the desire to promote diversity operation have collectively become more important. The latter point will, in fact, become a necessity for current and future LTE systems.



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# Chapter 1

## Introduction

The growth of existing and new broadband services - in recent years exemplified by the explosion in the number of users that are accessing the Internet - will continue to increase network traffic and will thus require more and more bandwidth.

In the evolution from 3G to 4G, wireless radio access networks meeting IMT-Advanced requirements will converge to fewer variants. This will increase the economies of scale for both for user and base stations equipment and will reduce the network costs. Long Term Evolution (LTE) and LTE-Advanced [14] are expected to meet and exceed the IMT-A requirements [15, 16] for throughput, capacity, and mobility at the cost of increasing the portion of used spectrum up to 100 MHz and by exploiting multi-antenna and carrier aggregation [17, 18] techniques for achieving the capacity targets.

Spectrum availability and harmonization across geographical regions - together with the expected capacity growth - represent the major challenges for realizing adequate access networks. Dynamic spectrum allocation and advanced techniques for radio channel capacity improvement are required to maximize frequency flexibility and channel capacity [19]. These techniques impact the total bandwidth demand and the realization of a properly dimensioned physical radio access layer.

It is expected that reaching the full 4G requirements will take 5 to 10 years. However, it is relevant for this project to identify the key frequencies, bandwidths, operational modes, and architectures that will become a fundamental part of 4G radio access networks in the shorter term. The identification of these market driven aspects and configurations are significant and worth analyzing due to their influence on the next 5 years of networks rollout.

The boundary between software defined [20] and software configurable [21] radios is subject to discussion because of the limitations of current commercial radio technologies [22]. The major limitation is that software flexibility on frequency dependent functions like up and down con-



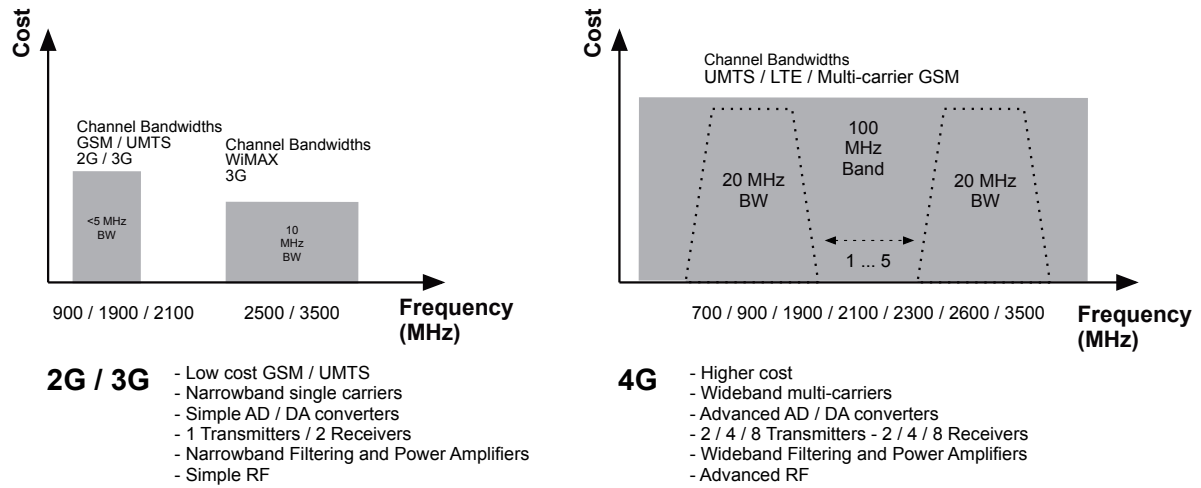


Figure 1.1: Radio Access Spectrum and Configuration Cost Trend Comparison between 2G/3G and 4G. 4G networks requires multi standards support, large bandwidths and dynamic allocation of the frequency spectrum.

version, power amplification, and filtering are possible at a reasonable cost only over a limited frequency range, and thus require several radio variants in order to cover wider bands. As IMT-A requires access to a portion of spectrum as high as 100 MHz, this requirement constitutes a considerable extension impacting mostly the system processing power and capacity as well as DA / AD technology available today [9]. It is thus of great interest to identify an architecture that could introduce much software flexibility within the existing technology base without compromising or delaying equipment commercialization.

4G mobile networks will adopt the distributed and open eNb base station architecture model as their radio access systems foundation [23]. The most relevant interface exists between the base band processing module and the remote radio module based on either CPRI/ORI or OBSAI RP3-01 definitions [24, 25, 26, 5].

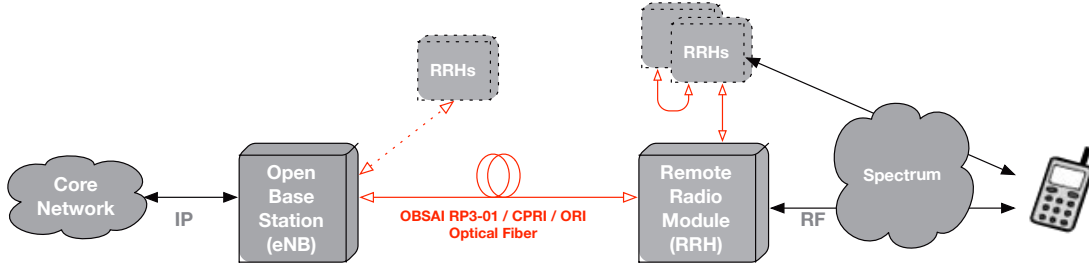


Figure 1.2: Network Architecture Overview of Open eNB with Remote Radio Heads using OBSAI RP3-01 / CPRI / ORI interfacing standards over optical fibers. The RRH can be chained to each other in a multi-hop topology enabling easier and more efficient installations.

The remote communication introduces complexities in the interface system with regards to synchronous operation and management, and the selection of either interface dictates whether such complexities must be included on the base band side (OBSAI RP3-01) or on the radio side (CPRI/ORI). Thus the analysis of the CPRI/ORI and RP3-01 protocol structure and carrier capacity is required for correct radio sub-network dimensioning calculations.

Until today the main obstacle on the road to plug-and-play interaction between base band and radio equipment has been the lack of a complete, fully specified, and vendor agnostic interface definition that the entire industry can accept unambiguously.

Historically, the barrier has been that - prior to the adoption of OBSAI or CPRI based technologies and for more than the last decade - each OEM has been implementing proprietary interfaces with the purposes of market differentiation and business protection.

Interoperability between vendors has been difficult due to the lack of system test specification procedures and dedicated test equipment to verify the base band and RRH module interfaces due to the niche market segment. A methodology based on standard profiling [6] and enhancement of the interface specifications [5] will contribute to reducing interoperability efforts leading to faster equipment integration and improved reliability. The synchronization between base band and radio modules of a eNB becomes critical when the base band is located remotely from the radio unit [10]. Hence configuration and management procedures for data flows, link start-up, and data path delay measurement are of critical importance to ensure error-free and reliable inter-module communications.

The capacity required for IMT-Advanced [27] will require further line rate extensions from the current rate of 6.144 Gbps supported from OBSAI RP3-01 and CPRI / ORI standards, and it is expected that rates will be further pushed in a near future to 9.830 Gbps [26] to deal with large carrier bandwidths and multi-hop radio topologies. We will show in the report that serial

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rates as high as 12.288 Gbps will be required to meet the bandwidth demand of IMT-A. In analyzing the delay paths for either CPRI/ORI or OBSAI RP3-01, the receiver part of the serial interface is the critical component of each link. If it is not designed properly delay inaccuracy will be introduced and will be additive for each hop [1]. It is thus important to consider a generic serial receiver architecture that provides sub-nanosecond delay measurement resolution and is equally applicable to either interface, while it must be implementable in any RTL technology including cost-effective low-end FPGAs.

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## Thesis Structure

This Industrial Ph. D. project focuses on system and interface level architectures for radio modules to be used in commercial 4G radio access applications, where a trade-off between performance and cost is of paramount interest in the development of commercially viable solutions. The current technical and economic approach leading to high-performance and low-cost optimized solutions is strongly relevant for RadioComp ApS. Technology leadership and innovation are business critical aspects for RadioComp ApS and will lead to the development of cost effective solutions. Thereby, Radiocomp will be able to maintain a strong position on the market for 4G radio systems. This thesis' structure is shown in Fig.1.3.

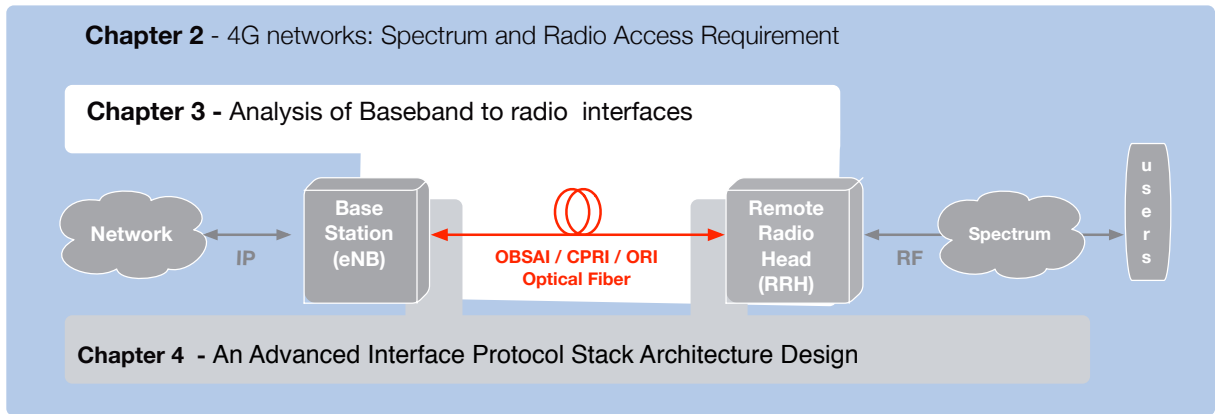


Figure 1.3: Visual structure of the wireless network areas covered by this thesis report including the spectrum resource, eNB/RRH radio access systems and the interface between the eNB and the RRH.

The thesis is organized into chapters each covering a specific area related to 4G radio access networks and presented in a top-down system level order. The overview and background for each topic is provided when necessary in the first section of each chapter. Supplementary background material for each topic is available in the appendices to complement each chapter. In each chapter the sub-section structure addresses the topic background, the problem statement(s), the review of the state-of-the-art in each area, and then elaborating on the original contributions and results obtained. The final section of each Chapter summarizes the original contributions for each topic discussed. The last chapter concludes this thesis and summarizes the overall contributions and suggesting future related work.

*Chapter two* presents an up to date overview of 4G network requirements and configurations. Many wireless standards have been introduced by the industry to cope with several different applications and sharply rising user traffic loads. Today's way of using spectrum is fixed and

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poorly harmonized. This has introduced significant market and technology fragments on a geographical basis. A more flexible utilization of spectrum can enable increased performance and efficiency. The chapter highlights the relevant IMT-A performance requirements as defined by regulatory and standardization bodies. Candidate techniques aiming at improving the efficiency of spectrum utilization and capacity increases are presented. They are needed for the physical layer dimensioning of an advanced radio module architecture supporting multi-standard and multi-band operations (MultiRAN) using Remote Radio Heads (RRHs). RRHs are highly integrated and complex modules that present several realization challenges. RRHs combine technologies and disciplines from software, digital, radio, mechanical and thermal engineering tightly integrated together. The chapter presents an optimal and standard agnostic remote radio architecture based on SoC.

*Chapter three* presents an in-depth analysis of the interface protocol between the base band and radio module of a eNB. It includes a detailed comparison of the RP3-01 and CPRI standards identifying the advantages and disadvantages of each seen from a system level and implementation perspective. The chapter also deals with the concept of interoperability presenting a review of the weak points of current interfacing technology and propose solutions to overcome them. As the complexity for an OBSAI RP3-01 implementation resides in the synchronization procedures, an analysis was made focusing on the synchronization mechanisms and system start up sequencing. This is important in architecting a reliable eNB system that takes data path delay inaccuracies into account.

*Chapter four* deals with an advanced modular interface protocol architecture common for both RP3-01 / CPRI interface controllers. The controller design supports increased serial baud rates for any RTL technology like FPGAs or ASICs. The design architecture has been verified to operate correctly at 6.144 Gbps and at 9.830 Gbps line rates using high-end FPGA technology and will in the future be able to support up to 12.288 Gbps rates. The delay requirements have been investigated together with the potential sources of measurement inaccuracies at the serial to parallel receiver level. Traditional methodologies for delay measurement revealed not being sufficient to meet the requirements for multi-hop configurations. A generic and advanced serial to parallel receiver circuit has been proposed applicable to both RP3-01 and CPRI interfaces that allows for the use of deterministic latency measurement blocks and implementable for any RTL technology.

*Chapter five* concludes this thesis work summarizing the overall scientific contributions and discussing future work.

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## Chapter 2

# 4G Networks: Spectrum and Radio Access Requirements

This chapter is based on the work done by the Author and presented in:

- C. Lanzani, M. Hoegdal, and N. Behjou, “Analysis of multi-mode transmission RF IC for base stations,” tech. rep., Radiocomp ApS, 2010 [9]. The Author’s personal contribution consists of the market and systems requirement analysis as in section two [9] and section three [9] respectively.

### 2.1 Overview of Bandwidth Demand

The definition of Beyond 3G (B3G) is in use in Europe referring to the upcoming wireless network systems that will go beyond the third generation (3G). In Asia, such systems are defined as the fourth generation (or simply as 4G), while in Japan they are referred to as the Super 3G (S3G). This thesis will adopt the 4G terminology for convenience covering all the above definitions. Conceptually, the expression 4G indicates a generation of future mobile network system enabling true broadband wireless access with peak data rates of 100 Mbps in high-mobility and one (1) Gbps in low-mobility applications [15]. The main driver for these targets is the tremendous traffic growth caused by the mobile subscribers increased dependency on Internet services. Reaching these targets requires a new approach in spectrum allocation and access to larger portions of spectrum. Spectrum allocation as of today is fixed with several dispersed band fragments across geographical regions that are used by different standards. These fragments are supporting blocks of 5-10 MHz for each operator and they are not sufficiently wide-band for enabling high throughputs for the 100 MHz single operator blocks envisaged in 4G. Moreover frequency harmonization, global roaming, and interoperability are consistent challenges. A sufficiently flexible broadband radio technology will be enabled by Dynamic Spectrum Access (DSA).

The International Mobile Telecommunication Advanced (IMT-A) initiative was introduced by [15] was identified using a methodology developed by the International Telecommunication Union - Radio (ITU-R) [28]. The European Wireless World Initiative New Radio (WINNER) project [19] provided a major contribution for calculating the spectrum demand under several scenarios and identified the major building blocks of future systems. The market studies on future services predicted a strong growth in the per user and aggregate traffic volumes in the 2010-2020 period [29]. The major contribution is coming from data applications [30] originating from both voice and non-voice traffic. Therefore IMT-A was initiated. All the evolutionary stages aimed at further improving the data throughput, coverage, and QoS factors like throughput and latency however have a considerable impact on the operators site upgrade costs. While voice continues to be a core and universal application, several clear application trends will influence mobile communications over the next few years as below and illustrated in Fig.2.1:

- Internet access for browsing, mobile office and system upgrades.
- Mobile TV and video distribution by use of streaming services like YouTube.
- Mobile interactive remote gaming and real-time gaming are emerging entertainment applications.
- Peer-to-peer voice and video conferencing over IP applications.
- Service bundles of video, data and voice from previous DSL providers are entering the mobile market. This is replacing traditional fixed line voice services by mobile voice services both at home and in business environments.

Broadband Internet access and mobile TV are expected to become major contributors along this way. Fig.2.2 describes the expected growth of user traffic, calculated as minutes times Gbps per day between 2010 and 2020 in three different economical development scenarios: smooth development <sup>1</sup> (optimistic), economic stagnation (pessimistic) <sup>2</sup> and constant change (realistic) <sup>3</sup> [32].

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<sup>1</sup>The economies are unite to provide growth and development, in a fair and managed way that brings prosperity across all nations.

<sup>2</sup>This definition considers an economy in slow decline, such as e.g. Japanese economy between 1988 and 2003. Outputs gradually shrink and government policy reactions to strong deflation were unsuccessful or froze. EU economic growth falls behind that of Asia.

<sup>3</sup>The economy overall follows a moderately positive trend, with ups and downs. Ad hoc growth and recession often happen in parallel in different areas or countries, with stop-go progressions and regressions in specific areas of the EU. However, prosperity slowly increases for many in the EU.

## 2.1. Overview of Bandwidth Demand

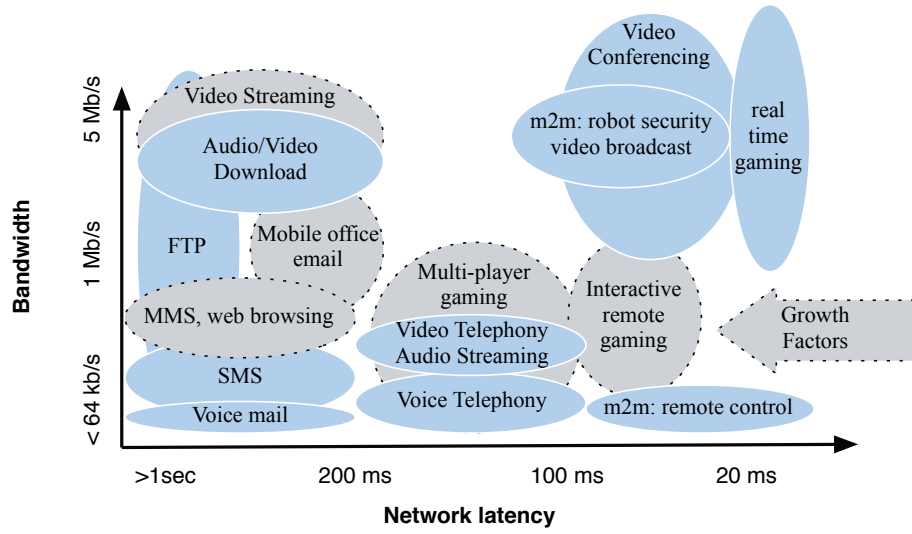


Figure 2.1: Throughput (Mbps) vs. latency (ms) of the most common Internet services with highlighted the capacity growth driving services that will require an extension of existing network's capacity. A major impact is driven by the growth of Video Streaming services [31].

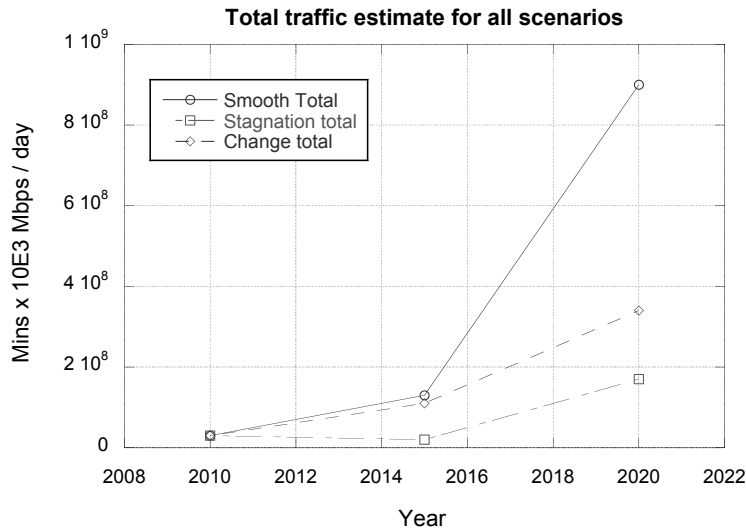


Figure 2.2: Total wireless mobile traffic volume estimates for 4G ranges between  $2 - 8 \times 10^8$  Mbps/day between 2010 and 2020. Supporting such volume increase will require a new a more powerful network infrastructure at both the core and radio access sides,[31].



## 2.1. Overview of Bandwidth Demand

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Spectral bands allocated by IMT-2000 will not suffice the predicted 4G network traffic demand [31] and new spectrum has to be allocated. In [15] it was decided that the spectrum calculation methodology for the future development of IMT-2000 and IMT-Advanced should include the flexibility to handle both emerging technologies and well-established systems. Recommendation ITU-R M.1768 [33] sets out guidelines for a technology neutral and generic methodology. Accordingly, the concept of Radio Access Technology Groups (RATG) was introduced in Report ITU-R M.2074 [29] to address different types of systems with and without a detailed specification that may be introduced later. Therefore RATG can be defined as a reference system model best accommodating a particular area of capabilities identified in Recommendation ITU-R M.1645 [15]. The RAT Groups of interest are the following:

- RAT Group 1 (RATG1): Pre-IMT systems, IMT-2000 and its enhancements. This group covers the cellular mobile systems, IMT-2000 systems and their enhancements.
- RAT Group 2 (RATG2): IMT-Advanced as described in Recommendation ITU-R M.1645 [15] (e.g., new mobile access and new nomadic/local area wireless access), but not including systems already described in other RATG.
- RAT Group 3 (RATG3): Existing radio LANs and their enhancements.
- RAT Group 4 (RATG4): Digital mobile broadcasting systems and their enhancements.

The predicted aggregate spectrum bandwidth requirement for both the RATG1 and RATG2 for the year 2020 [33] assuming a single network deployment per country, will range between  $1280\text{MHz}$  as the least necessary up to  $1720\text{MHz}$  as shown in Fig.2.3 (including spectrum already in use, or planned to be used, for both RATG1 and RATG2) [31]. These values represent the lower and higher market requirements in the long term. Note in Fig.2.3 the division between ITU-R geographical regions as Region 1<sup>4</sup>, Region 2<sup>5</sup> and Region 3<sup>6</sup>.

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<sup>4</sup>Region 1 comprises Europe, Africa, the Middle East west of the Persian Gulf including Iraq, the former Soviet Union and Mongolia.

<sup>5</sup>Region 2 covers the Americas, Greenland and some of the eastern Pacific Islands.

<sup>6</sup>Region 3 contains most of non-former-Soviet-Union Asia, east of and including Iran, and most of Oceania.

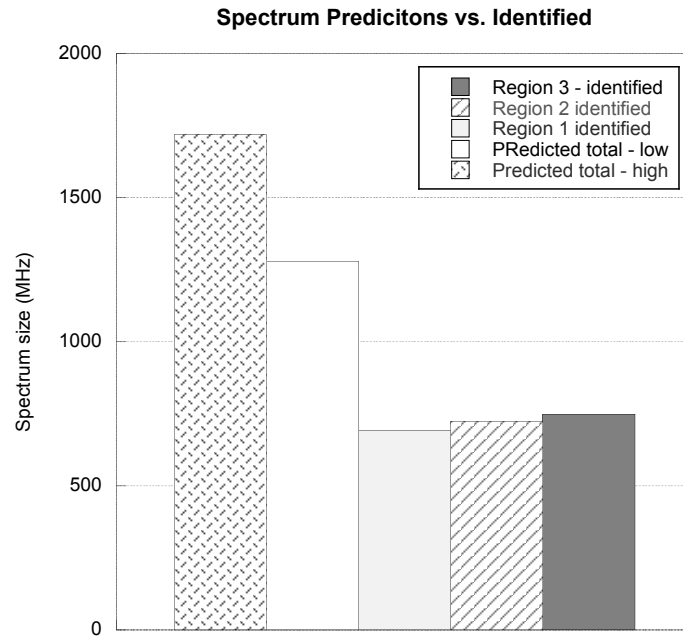


Figure 2.3: 4G networks spectrum vs. availability in MHz of bandwidth for the ITU geographical regions 1,2,3 (See footnotes for the regions definition).

The best-case and worst-case predictions of total spectral demand have been presented to highlight the need for accessing larger portions of spectrum for IMT-A systems to full-fill their performance capabilities. New spectrum can be accommodated by the introduction of new bands or by reallocating existing bands.

## 2.2 Spectrum Allocation Methodologies

Meeting or exceeding the IMT-A performance targets requires access to an increased portion of spectrum and more efficient ways to handle its allocation. Spectrum is the lifeblood of the mobile and wireless industry, but unfortunately spectrum is a limited and scarce resource that needs careful global, regional, and national planning as well as regulation.

In this section methodologies for allocating spectral resources are introduced. The current method of assigning spectrum to different radio systems is based on fixed spectrum allocation schemes. Section 2.2.1 discusses fixed spectrum allocation and its limitations. Dynamic Spectrum Allocation (DSA) concepts represent the state-of-the-art for enabling higher data throughput and more efficient ways of handling the spectrum. DSA will be an integral part of 4G networks and is introduced in 2.2.2. Finally, in Section 2.2.3 the short-term requirements for frequency bands and coverage are collected, highlighting the expected radio frequency system configurations for the next 5 years. These requirements are the foundation for the design of the advanced radio module later described in section 2.4.

### 2.2.1 Fixed Spectrum Allocation Limitations

In traditional networks - for example the 3GPP UMTS / HSPA - a block of radio spectrum is allocated for a particular Radio Access Technology (RAT). Normally, such a block of resources is for individual operator use. These spectrum blocks are of fixed size and are separated by fixed guard bands, and are reserved solely for the use of the radio license owner until the end of the license period. The fixed allocation of guard bands controls interference between different networks accessing contiguous spectrum and it is thus a simple and easily regulated way of managing spectrum resources.

ITU-R is responsible for the global regulation of the frequencies allocated on a geographical base, whereas the use of spectrum in each country is nationally regulated by the corresponding government agencies with the power to make spectrum available for particular use within their operational area. Spectrum allocation introduces challenges for eNB equipment manufacturers to supply off-the-shelf products covering most frequency bands.

A globally harmonized spectrum across all ITU-R regions is the key mass-market enabler ensuring global roaming and reduction in equipment costs. A harmonized spectrum enables radio equipments to support a bigger market scale covering specific regional frequency bands. A radio access technology so flexible in frequency that can cover the full range of frequencies from 400 MHz up to 4 GHz is of academic and commercial interest for Software Defined Radio

## 2.2. Spectrum Allocation Methodologies

research since it could potentially cover all the major frequency bands. However, because of the cost pressures on commercial solutions, such costly network elements would become practical only for military applications. It is thus critically important to find a technological compromise between desired flexibility and cost targets.

Spectrum frequency allocations should simplify global roaming while benefitting the economies of scale for affordable user equipment and enabling a wider choice of service providers and brands of devices for consumers. A common IMT spectrum demand is arising from the following considerations:

- Spectrum resources are scarce and almost all assigned / occupied on regional levels and not sufficient to meet IMT-A minimum targets.
- New standards (such as IEEE 802.16e Mobile WiMAX and beyond) were added to the approved IMT-2000 technologies in 2008 and are now part of the “IMT bands”.
- IMT frequency bands could be re-used and shaped to enable smooth network upgrade and migration paths for running multiple standards simultaneously, as for example UMTS, LTE and GSM (MultiRAN approach).

In the history of Worldwide Radio Conferences (WRCs) from 1995 we can see the major former and expected future decisions with regards to spectrum as shown in Fig. 2.4.

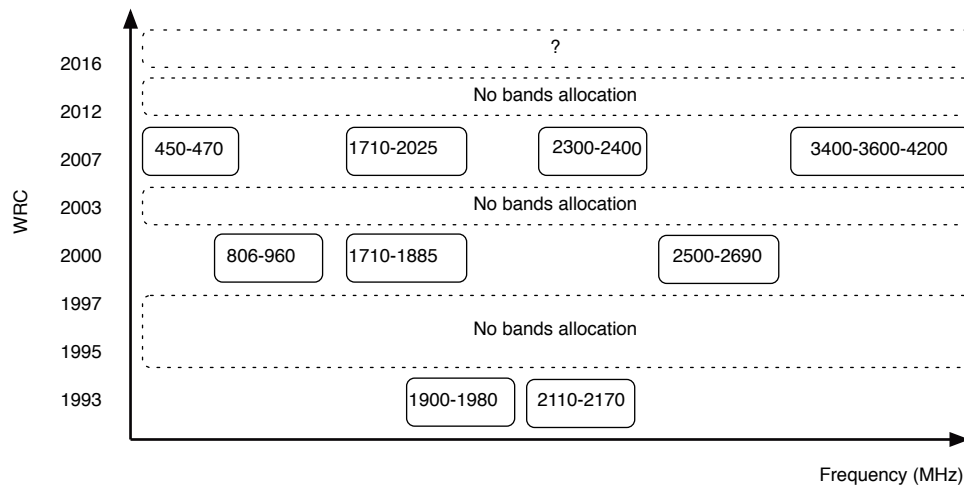


Figure 2.4: WRCs identified and targeted bands from year 1995 to 2016. It is expected that 4G will space across all bands and re-farming of each band will enable the wide band IMT-A operations.

The expected spectrum extensions for the LTE and LTE-Advanced systems will thus be defined in WRC-2000 and WRC-07. In WRC-07 it was defined that the standards covered by

## 2.2. Spectrum Allocation Methodologies

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the IMT-2000 and IMT-A initiatives would be sharing the same "IMT" regulated spectrum bands, with no plans for IMT-A exclusive bands. The decision was made mainly because of a global roaming and possible reuse of existing technology, which is important for equipment and component vendors.

WRC-07 defined new bands of interest for IMT technologies for the whole of 392 MHz in Europe and 484 MHz in the Americas, resulting in an additional 500 MHz and 1 GHz spectrum for all ITU Regions as shown in Fig.2.2. The additional candidate bands for IMT identified in WRC-07 [34] are reported below and different regulatory provisions apply to each band with expected regional deviations. They are relevant since 4G networks will utilize these spectral components and commercial SDR will need to operate and to be optimized to enable flexibility across the said frequencies:

- 450-470 MHz band
- 1710-2025 MHz band
- 2.3-2.4 GHz band
- 2.5-2.7 GHz band
- 3.4-4.2 GHz band
- 4.4-5.0 GHz band

However, the amount of spectrum available it is not adequate to meet IMT-A minimum requirements and the spectrum blocks - normally 5 MHz or 10 MHz wide for UMTS / WiMAX or early LTE systems - are not wide enough to support the large IMT-A bandwidths up to 100 MHz for individual operator's use [19]. The usage of spectrum in a flexible manner from a common pool of spectrum is envisioned to be essential for reaching 4G targets [16].

The existing 3GPP bands for 2G and 3G networks in the 900 / 100 MHz region will be later used for 4G, and IMT spectrum will support multiple Radio Access Technologies (RATs) across multiple bands. The Multi Standard Radio (MSR) - or MultiRAN (Multi Radio Access Network) - eNB station requirements are introduced in [35]. An MSR application is intended for Wide Area scenarios (Macro/Micro). MSR support for GSM/EDGE is provided by multi-carrier BTS classes. The concept of MSR is shown in Fig. 2.5, where a specific portion of spectrum is divided into band categories.

The band categories are defined according to the standards and duplex mode [35]:

- Band Category 1: Bands for E-UTRA FDD and UTRA FDD operation.

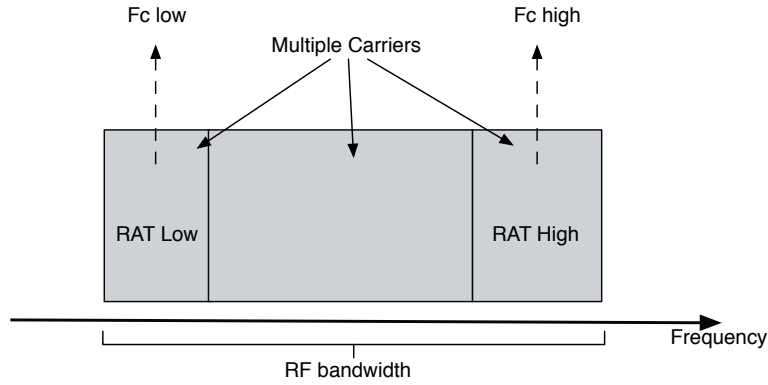


Figure 2.5: Radio Frequency definitions for Multi-standard radio spectrum utilization by separate and coexisting RATs [35] having multiple center carrier frequencies  $F_c$  in the high and low portion of the spectrum.

- Band Category 2: Bands for E-UTRA FDD, UTRA FDD and GSM/EDGE operation.
- Band Category 3: Bands for E-UTRA TDD and UTRA TDD operation.

The bands are divided according to the media access scheme used <sup>7</sup> used and reported below. Two methods are defined: the Frequency Division Duplexing (FDD) on paired spectrum and Time Division Duplexing (TDD) on unpaired spectrum. The list of bands are available in Appendix B.1 and Appendix B.2 collecting the definitions for MSR operations with GSM, UMTS (UTRA) and LTE (E-UTRA) standards. In WRC 2016 it may be expected a re-organization of different bands boundaries and sizes (specifically for the most common bands at 850 MHz, 900 MHz, 1800 MHz, 1900 MHz, AWS, 2000 MHz, 2600 MHz, etc.), aiming at enabling more advanced IMT technologies in existing spectrum.

Fixed Spectrum Allocation (FSA) has some disadvantages [36]. As a general remark, most communications networks are designed to support a maximum amount of traffic, and the dimensioning of the network is based around the busy-hour, which is the time of the estimated peak use of the network. If a network uses its allocated spectrum fully during this hour, then the rest of the time the spectrum is not fully used resulting in a waste of network resources.

The demand for different services on different networks depends also on location, leading to a spatial variation in the spectrum usage. It can therefore be seen that the radio spectrum, while scarce and economically valuable, is often underutilized or idle at certain times or in certain areas. This is the main motivation behind the need for a more spectrally efficient allocation technique, called Dynamic Spectrum Allocation (DSA) [36].

<sup>7</sup>Existing duplex method in each region will be maintained to ease the upgrade to new RATs.

### 2.2.2 Dynamic Spectrum Allocation Principles

Dynamic Spectrum Allocation (DSA) is an alternative to fixed spectrum access methods. DSA creates a balance between the data pipe and the available spectrum. As spectrum availability is scarce, IMT-A capacity requirements need frequency agile radio technologies that are able to aggregate bandwidth on demand, enabling flexible usage of the spectrum and to operate across any band. DSA can support contiguous and fragmented configurations and each has a direct impact on the complexity of the physical layer for radio transmission and reception, as well as access network architectures [36].

DSA is a key enabler to gain access to more spectrum and thus enabling increased data rates. There are two main methods of DSA:

- 1) *Spectrum Sharing and Coexistence (SSC)*. The purpose of this method is to simplify the coexistence of different wireless systems within the same frequency band. SSC may enable different operators to share resources within the allocated band across the same standards and offer services to users using higher bandwidths. In addition, SSC may enable deployments in mobile bands that are not exclusively allocated to IMT, across different Radio Access Technologies (RATs) as shown in Fig.2.6.

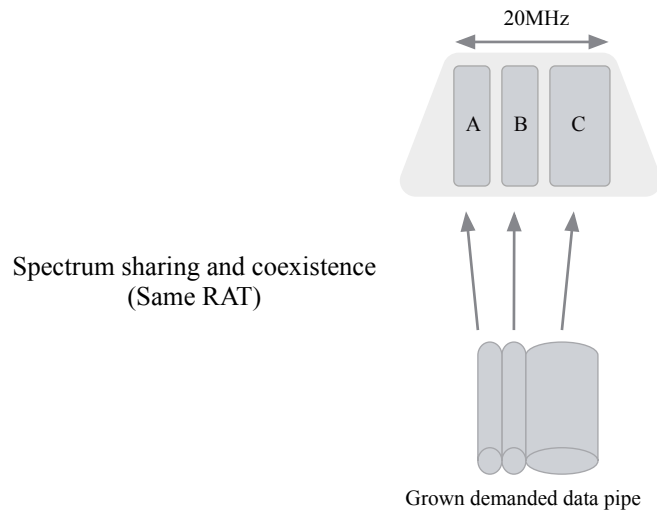


Figure 2.6: Illustrative example of spectrum sharing and coexistence (SSC) concept. A demand of an increased data pipe may be redirected across multiple carriers A, B or C within the same RAT. An example it could be LTE 20 MHz spectrum band divided into 10 + 5 + 5 MHz carriers.

- 2) *Flexible Spectrum Use (FSU)*. This is aimed at regulating spectrum access between different radio access networks (RAN) within the same radio access technology (RAT) [37]. Flexible use of the radio spectrum is seen as a promising technique for increasing spectrum

utilization. FSU allows the sharing of spectrum within the same radio access technology. It is based on the assumption that when one network operator needs spectrum another network operator might have spectrum available. Therefore the utilization of the unused spectrum or sharing of the spectrum from a common pool leads to a more efficient utilization of spectrum. There can be a single operator and a multi operator FSU. The purpose of single operator FSU is to reach a high performance in uncoordinated deployments, and enables different Uplink/Downlink (UL/DL) switching points for time division duplex (TDD) operations to enhance spectrum usage. The multi operator FSU simplifies different operators to access the common spectrum pool in flexible manner based on their individual traffic requirements [16] as shown in and Fig.2.7.

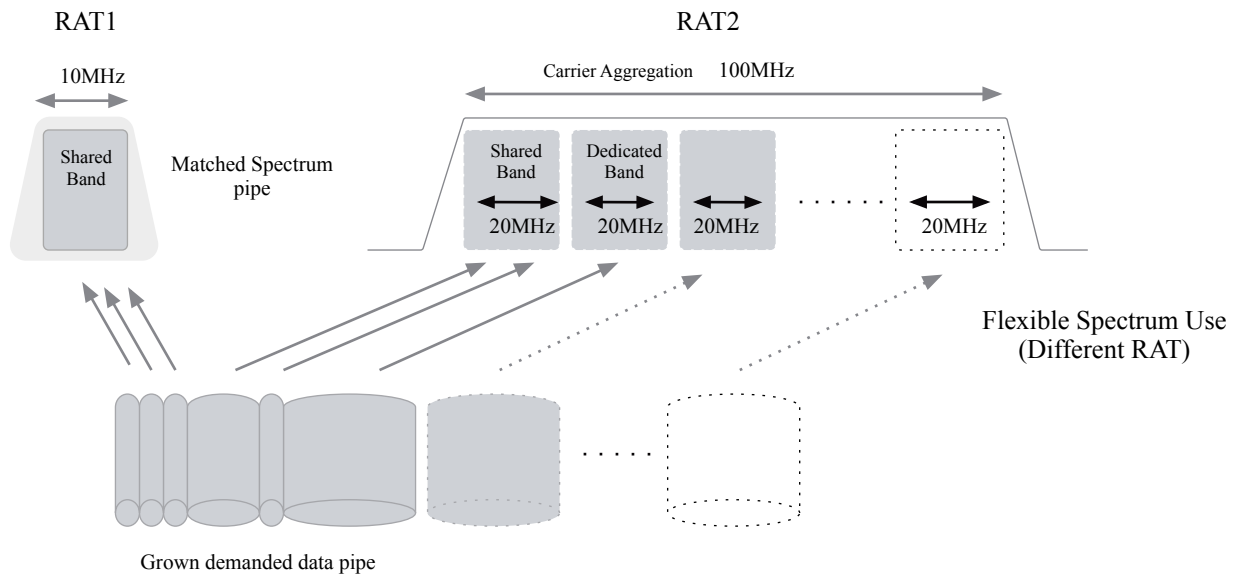


Figure 2.7: Illustrative example of Flexible Spectrum use (FSU) concept. A demand of an increased data pipe may be redirected across multiple RATs each consisting of a shared band and dedicated bands for increased traffic. An example it could be LTE-Advanced services demanding more than 20 MHz spectrum band with Carrier Aggregation (CA) addressed in section 2.3.2.

These concepts are needed enablers of the 4G technological convergence earlier introduced, since multiple and independent standards from both the 3GPP and the IEEE can then co-exist on the same IMT bands either independently or simultaneously providing enhancements to network performance and maintaining backward compatibility with existing standard until the migration process is completed.



### 2.2.3 Considerations on Short-Term Spectrum and Coverage Requirements

The fulfillment or exceeding of the IMT-A requirements as expected with LTE-Advanced will require spectrum re-allocation, over an expected time line of between 5 and 10 years. It is however very important for the early IMT-A systems to identify the short-term requirements for systems in use within a time horizon of the next 3-5 years. This section will focus on the identification of the most important frequency bands, capacity, and architectural/usage requirements that will apply to the upcoming radio access systems.

IMT spectrum will include a large set of paired and unpaired bands that are listed in Appendix B for reference where the MSR requirement are also included. The spectrum portion between 1.7 GHz and 2.6 GHz is considered the one with the largest prospective market share worldwide across all ITU geographical regions due to the existing utilization in 3G networks. Within a short-term horizon of 3-5 years, the gathered sub-bands and configurations of greatest relevance are reported in Table 2.1:

	China	Japan	India China	US India Africa	Europe
<b>Standard</b>	LTE-TDD	S3G	3G	LTE/802.16e	3G/LTE
<b>Output Power</b>	20W	>20W	1x60W	10W	>20W
<b>MIMO</b>	2x2	2x2	1x2	2x2/4x4	2x2/4x4
<b>Duplex Mode</b>	TDD	FDD	FDD	TDD	FDD
<b>Frequency</b>	2300-2400 MHz	800 MHz	1920-1980 MHz	2300 MHz	2100 MHz
		1500 MHz	2110-2170 MHz	2500 MHz	2600 MHz
		1700 MHz		3500 MHz	850 MHz
		2000 MHz		700 MHz	
<b>BW</b>	20-40MHz	20MHz	20MHz	20MHz	20-40MHz
<b>Multi-carrier</b>	Yes	Yes	Yes	Yes	Yes
<b>Multi-mode</b>	Future	Yes (LTE+UMTS FDD)	Future	Future	Yes

Table 2.1: Summary of the key market requirements for RANs considering geographical region, standards, coverage and antenna/carrier configurations, frequencies, RF bandwidth [9].

The Multi-RAN scenario is of great importance for new network rollouts. The goal is to have a future proof eNB that can run multiple standards simultaneously meaning 2G generation (GSM), 3G (UMTS) and 4G (LTE). This will allow migration to larger bandwidths at a point in time when the 2G and 3G networks will fade out. The 2.3-2.4 GHz band in China is expected to be the first band to utilize the full 100 MHz bandwidth in a mid to long term horizon due to its use in China for the TDD LTE technology.

For the new mobile access, high data rates would result in a smaller cell size because of

## 2.2. Spectrum Allocation Methodologies

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link budget conditions that will determine the maximum modulation possible. The cell size also decreases at higher frequencies because of propagation. These considerations would lead to an increased number eNB required and hence a higher deployment cost. It would therefore be preferable for the frequency bands supporting the wide area mobility capability of 4G systems to be reasonably close to the bands already identified for IMT-2000 between 700 MHz and 2400 MHz. For bands above the 3 GHz region, due to propagation, networks might operate with lower output power having smaller but high-throughput cells.

Generally, lower frequency bands shall be utilized to increase coverage (higher radio transmission power), while higher frequency bands shall be used to deliver a broadband experience for smaller cell sizes (lower radio transmission power) and low mobility. For in-building (indoor) solutions, femto & pico base stations solutions are relevant since it is expected that most data users will be indoors. Delivering a high in-building throughput performance with up to 2.6 GHz macro networks is expected to be challenging because of the uplink terminal power limits. Therefore it is expected that at eNBs at lower power with frequencies above 2.6 GHz will be considered for pico and femto coverage. The identified configurations for coverage and frequency are reported in Table 2.2:

Scenario	Frequency	Output Power	Nr. Users per Sector	Data rates
Macro	700 - 2400 MHz	20 / 40 / 60 / 80 W	High	Medium
Micro	700 - 3800 MHz	4 / 10 / 20 W	Medium	High
Pico / Femto	2300 - 3800	<1W	Low	High

Table 2.2: Summary of eNB applications for coverage, frequency, users and data rates [9]

Fig.2.8 and Fig.2.9 shows the market share expectations for 2009 and 2014 based on output power classes for radio access sites [38]:

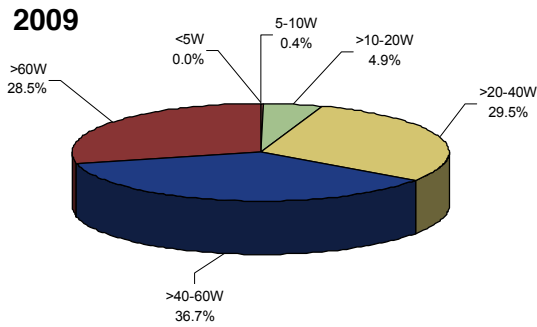


Figure 2.8: eNB site deployments forecast according to output power (in Watts per antenna) in 2009 [38]

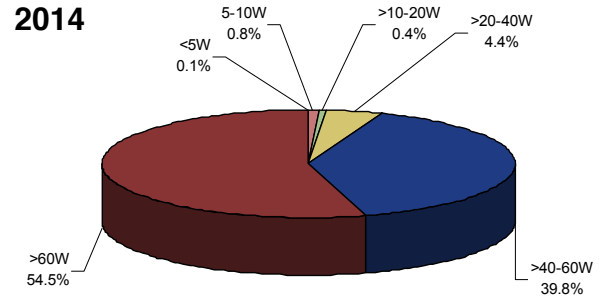


Figure 2.9: eNB site deployments forecast according to output power (in Watts per antenna) in 2014 [38]

## 2.3 Methods for Increasing the Capacity of 4G Networks

IMT-A aims at providing access to a wider range of advanced telecommunication services supported by mobile and fixed networks, which are increasingly broadband and packet-based. The main goals of IMT-A are to support low to high mobility applications and a wide range of device demands in multiple user environment while coping with the demands from different levels of the network value chain:

- *End users.* Demand for ubiquitous mobile and always-on broadband data access.
- *Network operators.* Demand for optimized spectrum resources, flexible network configuration, reduced cost of network equipment and technology reuse.
- *Equipment manufactures.* Demand for a reduced cost of equipment, differentiation via software services, open physical and logical interfaces, programmable platforms that enable fast and low cost developments.
- *Component Industry.* Higher integration of functionality, sharing components across multiple technologies, software programmability, and cost-effective configurations.

The three main performance requirements of IMT-A networks are defined in [39] and listed below:

- Higher peak data rates. The expected growth is shown in Fig.2.10.
- Lower data and control planes latency shown in Fig.2.11.
- Profitable networks with lower overall cost per bit as in Fig.1

## 2.3. Methods for Increasing the Capacity of 4G Networks

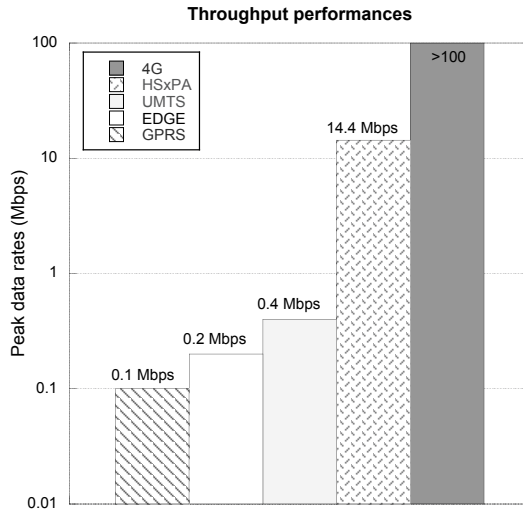


Figure 2.10: Throughput performance evolution path (Mbps) of different technologies toward 4G [40]

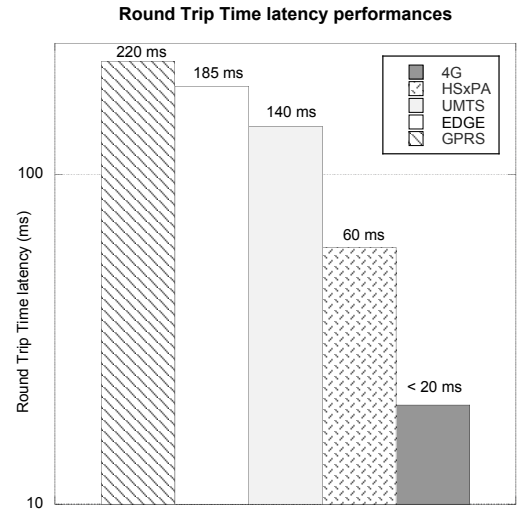


Figure 2.11: Latency performance evolution path (ms) of different technologies toward 4G [40]

The requirements of IMT-A and LTE/LTE-A are shown in Table 2.3 below:

Quantity	IMT-Advanced	LTE	LTE-A
Peak Data Rate	-	DL:300Mb/s UL:75Mb/s	DL:1Gb/s UL:500Mb/s
Spectrum allocation	Up to 40 MHz	Up to 20 MHz	Up to 100 MHz
Latency U-Plane	10ms	5ms	< 5ms
Latency C-Plane	100ms	< 100ms	50ms
Pk. spectr. eff.(bps/Hz)	DL:15 UL:6.75	DL:> 5 UL:> 2.5	DL:> 30 UL:> 15
Av. spectr. eff.(bps/Hz/cell)	DL:2.2 UL:1.4	DL:1.6-2.1 UL:0.66-1	DL:2.4-3.7 UL:1.2-2.0
Cell-edge spectr. eff.(bps/Hz/User)	DL:0.06 UL:0.03	DL:0.04-0.06 UL:0.02-0.03	DL:0.07-0.12 UL:0.04-0.07

Table 2.3: Summary of IMT-A, LTE and LTE-Advanced efficiency requirements. [27]

An increased need for spectrum with dynamic utilization and increased efficiency has been addressed at the WRC-07 [41]. Dynamic Spectrum Allocation (DSA) access can increase the spectral resource utilization and efficiency across several frequency bands and technologies as discussed in section 2.2.2. Increased spectral efficiency can be accomplished with MIMO, as discussed in section 2.3.1 and Carrier Aggregation (CA) as discussed in section 2.3.2 [27] to provide the bandwidth increase needed. However, 4G systems require the availability of adequate spectrum to support high-throughput services and the spectrum requirements have been set considering:

- Traffic projections and requirements including ratio of asymmetry
- Spectrum efficiency targets
- Radio transmission characteristics including duplexing scheme, modulation, access schemes

- Global roaming requirements and harmonized use of spectrum
- Techniques of dynamic spectrum sharing

Generally, the spectrum demand is determined by several factors, as data rate targets, modulation and coding schemes to get certain coverage and capacity, advanced antenna techniques for enhancing capacity, allocated guard bands and frequency bands as well as deployment conditions as part of the network planning phase.

It is realistic to expect that initial 4G rollouts will access less spectrum than what has been predicted since spectrum is limited and because it will take some time until proper reallocation and licensing is done [42]. A network software and hardware upgrade path will over time add new features and increased bandwidth with some degree of legacy to previous 2G and 3G standards.

### 2.3.1 Multi-Antenna Techniques

Wireless communication channels are subject to fundamental limitations in capacity mainly specified by bandwidth and Signal-to-Noise Ratio (SNR). Related to the channel capacity of 4G, this section addresses the channel capacity gain provided by multi antenna techniques - Multiple Input Multiple Output (MIMO) - aiming at improving the SNR, while section 2.3.2 addresses the bandwidth factor with Carrier Aggregation (CA), that aims to enlarge the system bandwidth to increase the communication channel capacity. The theoretical limit of the channel capacity for communication systems is given by the Shannon channel capacity. The Shannon-Hartley error-free channel capacity can be expressed by the formula [43]:

$$C = B * [\log_2(1 + SNR)] \quad (2.1)$$

Where:

$$\begin{aligned} C &= \text{channel capacity} \\ B &= \text{Occupied bandwidth in Hz} \\ SNR &= \text{The linear signal-to-noise ratio} \end{aligned}$$

It can be seen that the channel capacity increases linearly with respect to an increase in bandwidth, and is logarithmically related to changes in SNR. Link budget improvements are possible either by using additional bandwidth as a means to improve the coding/modulation efficiency and/or by improving the SNR factor by using Multi Antenna techniques.

The bandwidth of a communication channel is a linear function of its symbol rate. Thus, increasing the symbol rate of the channel increases throughput at the expense of requiring additional bandwidth and larger spectrum access. This topic is addressed in section 2.3.2. For a

### 2.3. Methods for Increasing the Capacity of 4G Networks

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given cell coverage, the SNR of a digital communication channel affects the throughput of the system by limiting the modulation scheme that can be used. Thus, increasing the performance efficiency of the modulation scheme in use can increase the system throughput without affecting the channel bandwidth. Increasing the bit rate of a wireless communications system brings increased power consumption and smaller cell sizes since the same amount of energy is now spread over a larger bandwidth resulting in lower channel output power. Broadband coverage using multiple wide-band carriers requires higher output powers for covering the same given area. Moreover, the signal strength in indoor environments may be lower due to building penetration loss, which often nullifies the high data rate features. However, modulation schemes of higher order like 16-QAM and 64-QAM can be used only in communications channels with a high SNR. This is necessary because subtle changes in the phase and amplitude of the signal cannot be accurately determined in noisy channels with low SNR.

The SNR factor can be improved in several ways, for example by using relay/repeater stations that can expand the service area and improve throughput for indoor coverage [44] [43], by using multi antenna techniques which is the main topic of this section.

MIMO (multiple input, multiple output) is a multi antenna technology for wireless communications in which multiple antennas are used at both the source (transmitter) and the destination (receiver). The key advantage of MIMO systems is many orders of magnitude of the SNR at no extra bandwidth - only hardware and software processing complexity are added at both transmitter and receiver. In fact MIMO systems have the ability to turn multi-path propagation, traditionally a pitfall of wireless transmission, into a benefit for the user [45]. MIMO effectively takes advantage of random fading [46, 47, 48] and when available, multi-path delay spread [49, 50], for multiplying transfer rates.

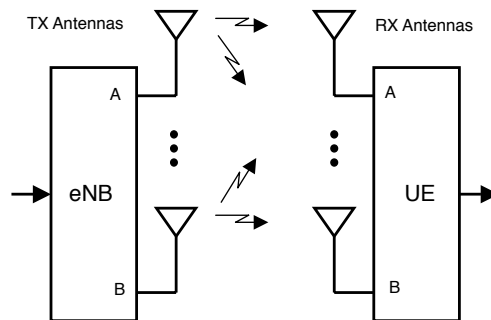


Figure 2.12: Block diagram of a generic MIMO system with multiple transmit at the eNB and multiple receive antennas at the UE.

### 2.3. Methods for Increasing the Capacity of 4G Networks

Equation 2.1 assumes a communications channel with one transmitter antenna and one receiver antenna. Thus, Shannon's equation can be expanded to account for systems with multiple antennas, like MIMO as in Equation 2.2 showing the mathematical representation of the throughput of a perfectly ideal communications channel using multiple antennas can be shown with the following equation:

$$C = \text{Antennas} * B * [\log_2(1 + \text{SNR})] \quad (2.2)$$

Where:

$C$  = channel capacity

$\text{Antennas}$  = Number of antennas in use

$B$  = Occupied bandwidth in Hz

$\text{SNR}$  = The linear signal-to-noise ratio

The basic premise of MIMO antenna systems is that the effective SNR of the system can be increased by transmitting unique bit streams with multiple transmit antennas in the same physical channel. This is referred to as spatial multiplexing and an example is shown in Fig 2.13:

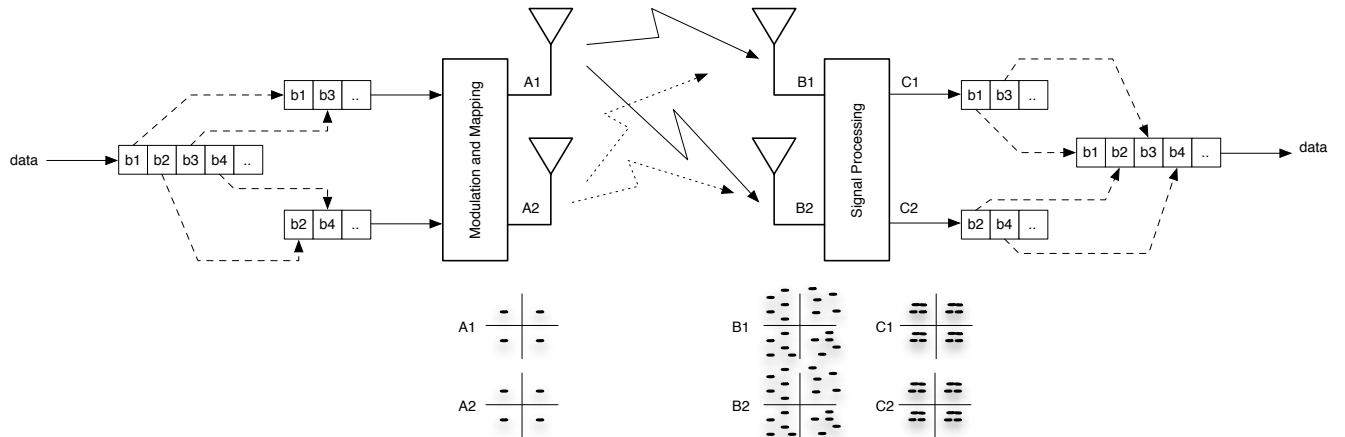


Figure 2.13: 2x2 MIMO Communication System. Basic spatial multiplexing (SM) scheme with three TX and three RX antennas yielding three-fold improvement in spectral efficiency.  $A_i$ ,  $B_i$ , and  $C_i$  represent symbol constellations for the three inputs at the various stages of transmission and reception [45].

There are two main ways of exploiting MIMO antenna benefits: (a) using MIMO *Matrix A* methodology to improve coverage, or (b) using MIMO *Matrix B* methodology for increasing channel capacity.

## 2.3. Methods for Increasing the Capacity of 4G Networks

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When Matrix A is used - for example in a 2x2 antenna configuration as in Fig.2.13 (2 transmitter antennas, 2 receiver antennas) -, the same data stream is transmitted in parallel over the two paths. A mathematical algorithm known as Space Time Block Codes (STBC) [51] is used to encode the data streams of the two antennas to make them orthogonal to each other. This improves the SNR at the receiver side enabling to either increase the cell radius, or provide better throughput for subscribers that are difficult to reach. For terminals which already experience good signal conditions Matrix A has the benefit that higher order modulation (e.g. 64QAM) can be used and fewer error correction bits are necessary which in turn increases the bandwidth to that subscriber.

When Matrix B - also known as Spatial Multiplexing MIMO (SM-MIMO) - is used, an independent data stream over each antenna is sent. Thus, in case signal conditions are excellent, the data rate is directly proportional to the number of antennas used in both the transmitter and receiver.

Multi-antenna techniques such as MIMO combined with carrier aggregation provide a mean for future networks to get closer to their data rate targets; optimizing the reception and expanding the total bandwidth available for data transmission. Currently, the link performance (in terms of channel capacity) of cellular systems is already close to the theoretical Shannon limit, meaning that higher rates can only be obtained in a reasonably cost efficient way by a further increase of the transmission bandwidth. This consideration has been driving the definitions of IMT-A requirements toward usage of up to 100 MHz of spectrum using Carrier Aggregation techniques that will be addressed in section 2.3.2.

The definition of link budget in a communication system accounts for all the gains and losses from the transmitter to the receiver. For any link-budget improvement, the very high data rates targeted by IMT-A need a higher Signal-to-Noise Ratio (SNR) than what is typically the case in wide-area cellular networks and especially improvements at the cell edge are of interest to enhance the user experience [17]. In this situation, usage of MIMO techniques are of great interest and to some degree already in use today including receiver diversity for 3G UMTS networks.

### 2.3.2 Carrier Aggregation Techniques

Carrier Aggregation (CA) is a technique that allows the aggregation of multiple carriers within a given instantaneous RF bandwidth. CA differs from existing multi-carrier techniques used in WiMAX for example where the instantaneous bandwidth available for multi-carrier is maximum 20 MHz. CA enables higher data rate transmissions by using multiple frequency blocks called



### 2.3. Methods for Increasing the Capacity of 4G Networks

Component Carriers (CC) with 20 MHz of bandwidth each to be backward compatible with previous generations. CC can be combined in up to five CC blocks to fit into a spectrum portion up to 100 MHz as defined by the IMT-A. In fact, a CC of 20 MHz enables backward compatibility with previous generation of devices, allowing simultaneously newer devices to support multiple CC blocks [18]. The benefits of CA are high data rate peaks, while it also maintains backward compatibility with LTE systems, where each CC can be configured to be backwards compatible with Rel-8 LTE devices.

Early IMT-A deployments with LTE Rel.10 are expected to support two 20 MHz CCs covering up to 40 MHz of spectrum where available. Extensions up to 100 MHz covered by five CC will become available in the longer term because of the lack of available spectrum in all bands (as well as the lack of cost-effective technology to support such demands).

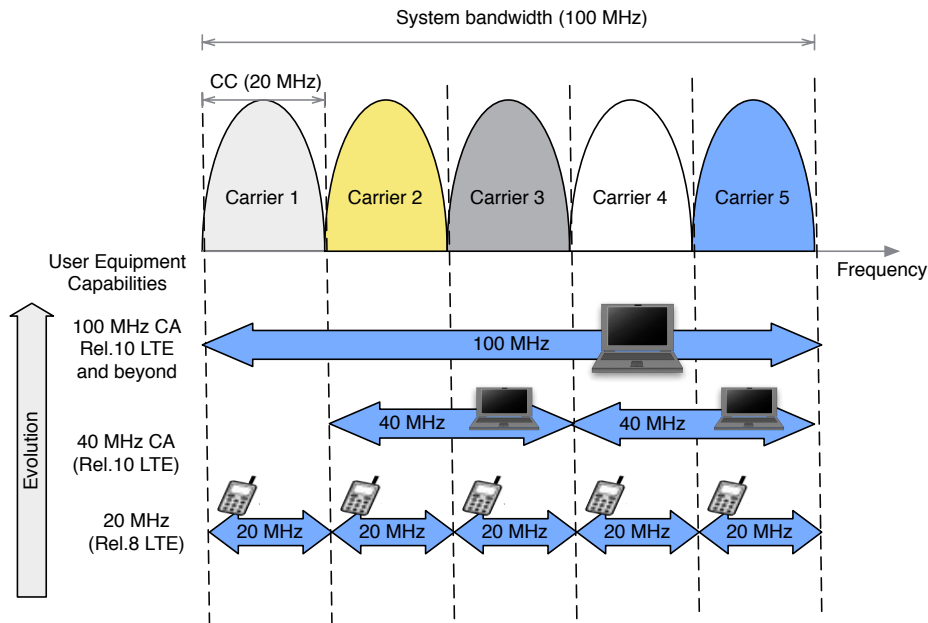


Figure 2.14: Carrier aggregation example with different user equipment bandwidth capabilities. Advanced LTE Rel.10 systems with higher performance can be introduced later on while maintaining compatibility with LTE Rel.8 and 9.

### 2.3. Methods for Increasing the Capacity of 4G Networks

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Three different scenarios are identified for CA techniques in the DSA scheme:

- Support for contiguous spectrum configurations as illustrated in Fig.2.15 a).
- Support for non contiguous spectrum configurations as illustrated in Fig.2.15 b).
- Support for asymmetric bandwidth for FDD flexible spectrum usage as illustrated in Fig.2.15 c).

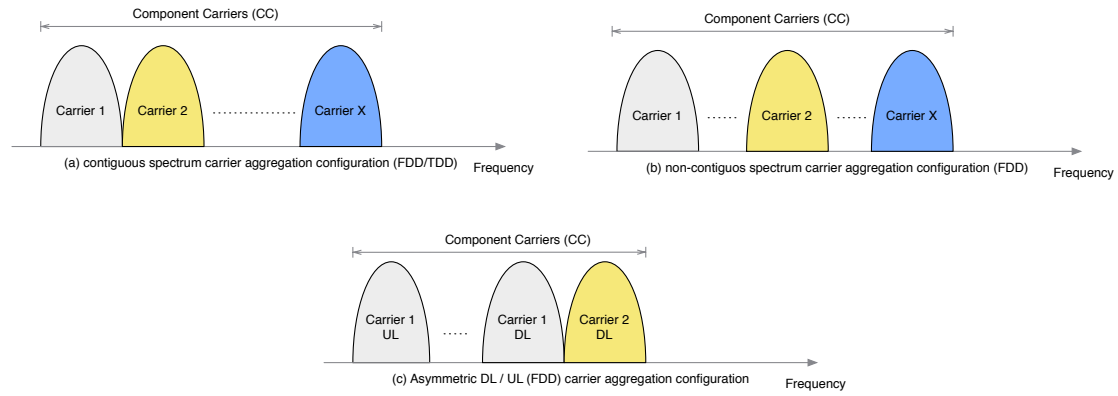


Figure 2.15: Different configurations of Carrier Aggregation (CA): a) contiguous (CC are operated in the same instantaneous bandwidth of a given band), b) non-contiguous (CC are operated in different bands) and c) asymmetric DL/UL (CC are operated asymmetrically in DL and in UL in the same band.) [27]

The continuous CA scheme configurations have a direct impact on the physical layer baseband and RF requirements for the eNB. Depending on the amount of spectrum available, each CC might be processed by the same eNB in a parallelized processing scheme across multiple base band module. CA heavily increases the baseband processing requirements. Modular and scalable baseband processing cards can be configured in parallel to process each CC independently or processing can be done in a distributed architecture.

### 2.3. Methods for Increasing the Capacity of 4G Networks

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*It is important to note that when IMT-A require a system bandwidth of up to 100 MHz, as an aggregation of multiple component carriers, this is intended per antenna.* When MIMO techniques are used, the bandwidth scales with the number of antennas. This aspect has a major impact on the entire system dimensioning in terms of processing power and RF requirements as well as transport interface capacity.

The total bandwidth  $B_{tot}$  need between the base band and the radio module will depend on several configuration factors like the amount of CC enabled, number of MIMO antennas. CA has a considerable impact on the amount of bandwidth required in the most common contiguous CA configurations - multiple of 20 MHz as in Equation 2.3 - in terms of number of CC and number of Antennas are shown in Table 2.4 below.

$$B_{tot} = Antennas * B_{CC}(MHz) * CC \quad (2.3)$$

where:

$$B_{tot} = \text{Total Bandwidth (MHz)}$$

$$Antennas = \text{Number of antennas in use}$$

$$B_{CC} = \text{Component Carrier Bandwidth (20 MHz)}$$

$$CC = \text{Number of CC in use}$$

$B_{CC} * CC$ (MHz)	CC	$B_{tot}$ 2 Antennas (MHz)	$B_{tot}$ 4 Antennas (MHz)
20	1	40	80
40	2	80	160
60	3	120	240
80	4	160	320
100	5	200	400

Table 2.4: Total bandwidth required for continuous CA configurations using 2x2 MIMO or 4x4 MIMO antennas configurations for each radio node for both DL and UL. Total bandwidth scales with the number of antenna paths in use assuming a single radio node.

Each CC has to be tuned to the right center frequency and this is done in the radio module of each eNB. The processing power requirements are proportional to the actual bandwidth, number of CC per antenna path, and number of antenna paths. The conversion and conditioning digital functions architecture of a radio module will be introduced in chapter 3.

The non-contiguous CA scenario is very relevant for dealing with the existing spectrum allocation policies and the fact that the spectrum availability is scarce in the low frequency band (< 4 GHz, making it difficult to allocate continuous portions of spectrum up to 100 MHz for mobile networks. The non-continuous CA technique is promising form a theoretical perspective.

### 2.3. Methods for Increasing the Capacity of 4G Networks

However, the aggregation of non-contiguous spectrum is challenging from an implementation and cost perspective because of the available radio technologies. An implementation will be strongly constrained, including specification of only a limited number of aggregation scenarios and aggregation over dispersed spectrum only being supported by the most advanced terminals [18].

The support of broadband data transmission under the non-continuous CA approach requires that multidimensional resource allocation and management schemes adjusting transmission power, modulation, and coding schemes for different component carriers. The Transmission Blocks (TBs) from different component carriers can be aggregated at either the medium access control (MAC) or physical layer. This is shown in Fig. 2.16.

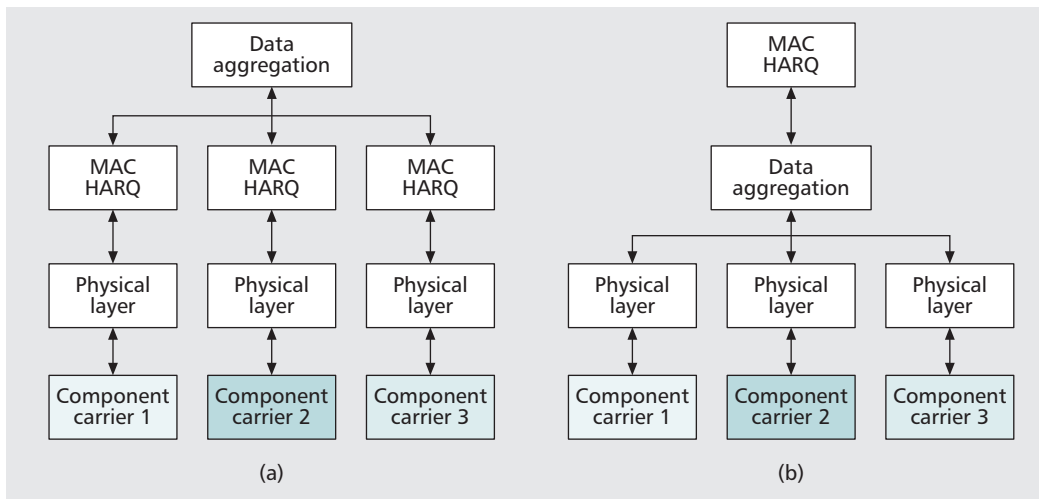


Figure 2.16: Different types of Carrier Aggregation: a) MAC Layer CA and b) Physical Layer CA [27]

Compared to the physical layer scheme, the transmission parameters are configured independently for each component carrier under the MAC layer data aggregation scheme. So the latter can support more flexible and efficient data transmissions in both uplink and downlink, at the expense of multiple control channels. In this way backward compatibility is guaranteed, since the same physical layer and MAC layer configuration parameters and schemes for the LTE systems can be used in future LTE-Advanced systems.

The LTE-Advanced systems working in time-division duplex (TDD) mode, besides the above schemes using different numbers of component carriers, supports asymmetric uplink and downlink channels. Asymmetric CA can also be achieved by adjusting the ratio of allocated time slots for uplink and downlink transmissions. This scheme simplifies the resource allocation relationship between the uplink and downlink channels. In typical TDD deployments, component carriers and the bandwidth of each component carrier in UL and DL will be symmetric.

For a component carrier to be accessible by an LTE release-8 terminal, synchronization signals and broadcast channels need to be present. However, for an LTE-Advanced terminal capable of receiving multiple component carriers, it can be adequate if these signals are available on one of the component carriers only. Hence, an operator can, by enabling/disabling these signals, control which part of the spectrum that should be accessible to LTE terminals. Whether carrier aggregation is used or not, the component carriers configuration is provided to the LTE-Advanced terminals as part of the system information [18].

Some of the expected CA scenarios for flexible spectrum use in the mid-term to match the available spectrum in certain bands:

- *Single band and contiguous allocation for FDD.* It is expected up to 80 MHz in DL and 40 MHz in UL with asymmetric allocation as in Fig. 2.15.
- *Single band contiguous allocation for TDD.* It is expected 100 MHz DL/UL only in the 2300-2400 MHz band for the Chinese market.
- *Multi band non-contiguous allocation for FDD.* It is expected up to 40 MHz in DL and 40 MHz in UL.
- *Multi band non contiguous allocation for TDD.* It is expected up to 90 MHz DL/UL.

In the next section 2.3.3 we highlight the most high priority configuration scenarios identified for the early 4G networks carrier aggregation configurations for the most relevant frequency bands.

### 2.3.3 Discussion on Bandwidth Demand

As earlier discussed, IMT-Advanced eNB will need to access up to 100 MHz of spectrum for antenna to deliver the demanded throughputs. Considering MIMO configurations for 2x2 and 4x4 scenarios, the need for bandwidth transport for IMT-A is up to 2 x 100 MHz (200 MHz) and 4 x 100 MHz (400 MHz) for a eNB with two (2) or four (4) antennas respectively as shown in Table 2.4. According to [14] some high priority scenarios of LTE/LTE-Advanced for existing bands with carrier aggregation have been defined already as in Table 2.5 below for the mid-term horizon of 4G networks evolution:

Item	Band	Duplex	CC Configuration
1	2.3 GHz (Band 40)	TDD	Contiguous 5 x 20MHz
2	900 MHz (Band 8)	FDD	DL/UL: Non-contiguous 5+5 MHz
3	2.6 GHz (Band 38)	TDD	Non-Cont. 2x20 + 2x20 MHz
4	3.5 GHz	TDD	Contiguous 5 x 20 MHz
5	3.5 GHz	FDD	DL: Non-Cont. 2x20 MHz + 2x20 MHz CC UL: Non-cont. 20+20 MHz
6	3.5 GHz	FDD	DL: Contiguous 4x20 MHz CC UL: Contiguous 2x20 MHz

Table 2.5: High priority scenarios of LTE/LTE-Advanced for existing bands with carrier aggregation [14] for the 2015 horizon for 3.5 GHz and 2.5 GHz and below frequencies. Actual available spectra are different according to each region or country and support for flexible deployment scenarios including DL/UL asymmetric bandwidth allocation for FDD and non-contiguous spectrum allocation is required.

Because of the inherent implementation complexity of configurations with more than two antennas like 4x4 MIMO, a 2x2 MIMO antenna configuration is seen as the most common one for radio modules in the field in the short term. According to the available spectrum utilization, different bands will likely support different operational bandwidths as can be seen in Table 2.5. Assuming a 100 MHz bandwidth per antenna, there is a need for at least 200 MHz of total bandwidth to support the highest IMT-A throughput requirements. A configuration with 2x2 MIMO and maximum 40 MHz operating instantaneous bandwidth per antenna is by far the most realistic option bridging the gap of the next 3-5 years. This configuration will be in use on both FDD and TDD networks and it will support multi-carriers in several configurations (for example 20 + 20, 20 + 10 + 10, 20 + 10 + 5 + 5).

A distributed eNB solution with RRH has to transport this bandwidth for each single node through the serial optical connection between the BBM and RRH modules. The bandwidth demand will increase if multi-hop RRH scenarios are utilized. The current bottleneck is the baseband to radio interface carrier capacity supporting only 100 MHz bandwidth in total per link, assuming a CPRI interface running at 6.144 Gbps rate with 15 bits samples [7]. Higher serial line rates will be required up to 12.288 Gbps to provide the required bandwidth needed for IMT-A. This is further analyzed in chapter 3.

## 2.4 Software Radio Architecture

The discussions in this section are based on the work done by the Author in the articles:

- G. Kardaras and C. Lanzani, “Advanced multimode radio for wireless and mobile broadband communication,” in *Wireless Technology Conference, 2009. EuWIT 2009. European*, pp. 132–135, IEEE Computer Society, sept. 2009 [3] where the personal contribution is on the digital system interfacing and processing architecture.
- C. Lanzani, M. Hoegdal, and N. Behjou, “Analysis of multi-mode transmission RF IC for base stations,” tech. rep., Radiocomp ApS, 2010 [9] where the personal contribution is on the system architecture requirements.

### 2.4.1 Software Defined Radios

By its definition, a Software Defined Radio (SDR) is a radio communication system, which can tune to any frequency band and receive any modulation across a large portion of frequency spectrum through programmable hardware that is controlled by software. Technology advances have ushered in new radio capabilities that require an expansion of the essential communications functions of source coding and channel coding. In defining a SDR platform one key architectural question is the degree of programmability required for the intended market niche and main focus of this section.

In a broader perspective, SDR is a collection of hardware and software technologies that enable reconfigurable wireless infrastructure and user terminals. SDR is applicable across a wide range of areas within the wireless industry [52]. In addition, SDR at the RF access means having increased flexibility in the frequency range and bandwidth selection.

Contemporary radio designs vary across the technology frontier, comprising a mix of ASIC, FPGAs, DSP, and General-Purpose (GP) processing elements using ADCs and DACs at base-band or Intermediate Frequency (IF) rates [21]. In its most basic form, SDR may be viewed simply as an implementation technique in which signal processing hardware is replaced by programmable devices such as digital signal processors or field programmable gate arrays (FPGA).

## 2.4. Software Radio Architecture

The evolution phases of SDR system are shown in Fig.2.17.

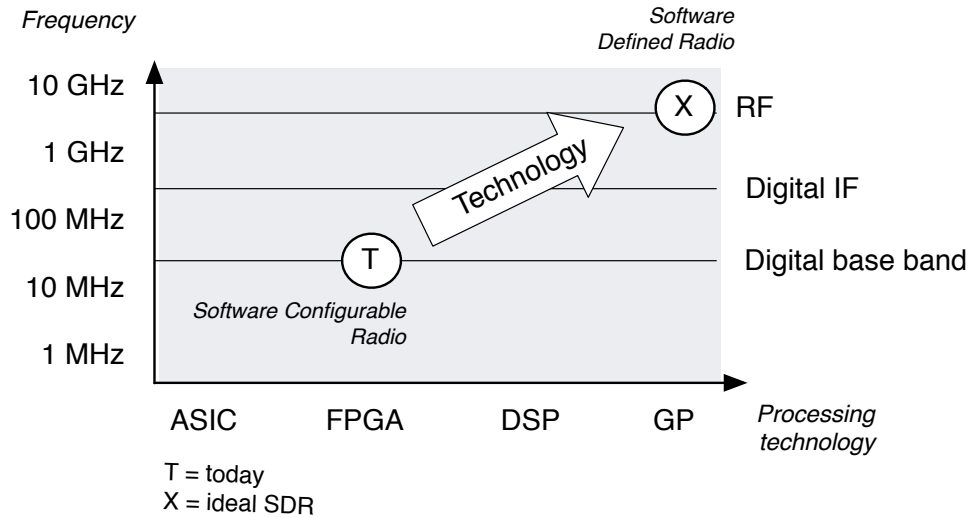


Figure 2.17: Evolution phases for SDR systems from a frequency and implementation technology perspective[20]. Today SCR operates within the 100 MHz base band processing domain using FPGA/DSP technology. Integration and higher processing power are pushing the processing toward high IF in the sub-GigaHertz range.

When functions, interfaces, components, and/or design rules are defined and published, the resulting architectures are called open. The economic benefits of an open architecture require a large commercial base, which sometimes fails to emerge despite openness. The challenge is to balance the generic needs of open architecture versus the specific needs of market segments. The new aspects are captured in the SDR functional model that was introduced by SDR pioneer Mitola in [20] in where three fundamental limitations to SDR:

- RF access.
- Digital access bandwidth.
- Digital processing (flexibility and capacity).



## 2.4. Software Radio Architecture

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Some of the critical high level design parameters are identified in Table 2.6:

Critical Parameter	Remarks
<i>Number of Channels</i>	Number of RF, IF, and/or baseband channel
<i>RF Access</i>	Continuous coverage from a minimum to maximum RF
RF Performances	SEM, Blocking, TX Output Power and EVM
Dynamic range	End to end, including RF, IF, ADC,AGC and processing
<i>Interconnect Bandwidth</i>	Bandwidth of critical buses, serial ports, back planes, etc
<i>Timing</i>	The precision and stability of system clock(s) and timing references
<i>Delay accuracy</i>	Availability of deterministic latency measurement features
Frequency Performance	RF, IF, and local oscillator (LO) accuracy and stability

Table 2.6: Key critical design parameters of a radio system. *Number of Channels* and *RF Access* have been investigated in section 2.2 and section 2.3. *Interconnect Bandwidth* is a topic discussed in details in chapter 3 while the Timing and Delay accuracy component is discussed in details in section 4.4.

The *Number of Channels* and *RF access*, as well as *Interconnect Bandwidth* and *Timing and Delay Accuracy* are very relevant for this thesis. As system complexity increases, the architecture becomes more critical: a powerful architecture will simplify system development while a weak architecture will impede progress. Software-defined radios are a powerful technology for the rapid deployment of new services and some SDR architectures favor the rapid insertion of new technology.

## 2.4. Software Radio Architecture

The reference hardware model for a typical RF access portion of a SDR / SCR system is shown in Fig.2.18 below:

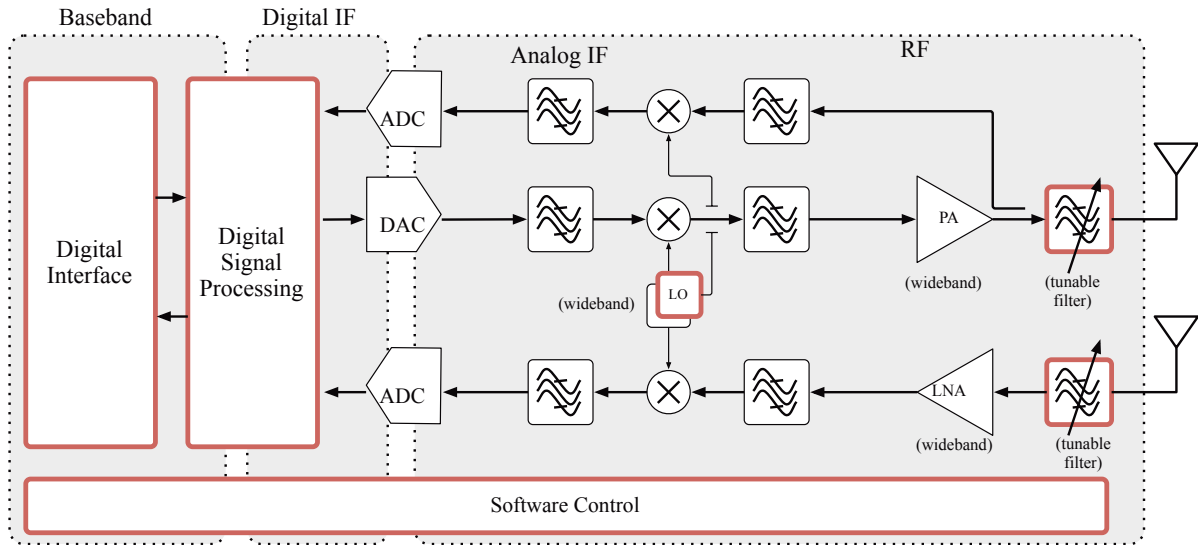


Figure 2.18: Typical Hardware Reference Design for SDR. Highlighted in bold the analogue and digital blocks that can benefit of Software Configuration like Local Oscillators for Carrier Frequency tuning, Tunable Front End Filters for interference and SEM matching, as well as Interface and DSP Blocks.[20]. This will enable flexible operations in frequency across a given band, as well as wider channels.

The industry, however, is far from being unanimous on the strategy for open architectures. Some would like to define a few critical interfaces, while others would like to see a more comprehensive functional model. Some see flexibility for future-proof operations while others see cost effectiveness of application specific solutions as fundamental to growth of the market. Different market segments need different implementations, so a truly useful industry-wide SDR architecture will have to accommodate different product areas solutions [20].

Given that SDR will continue to become more and more capable, one can ask whether they will have some fundamental impact on the approach to the use of the radio spectrum. DSA techniques will enable advanced SDR, as Cognitive Radio (CR) [53] concepts. CR offers a mechanism for the flexible pooling of radio spectrum using a new class of protocols called radio etiquettes [20] and terminals may efficiently benefit of different networks access based on location awareness and power savings.

### Boundary between Software Defined and Software-Configurable Radios

Commercial radio equipment faces with several limitations when compared to the typical SDR introduced in the previous section, and a more suited definition for the equipment could be Software Configurable Radios (SCR) where the programability/flexibility degree of certain RF components might be limited. This section presents the major limitations of current commercial radio technology introducing the state-of-the-art in remote radio head architectures and degree of reconfigurability can be offered when targeting multi-mode operations. With the introduction of RRH modules, the system architecture and function partitioning is identified as below in Fig.2.19:

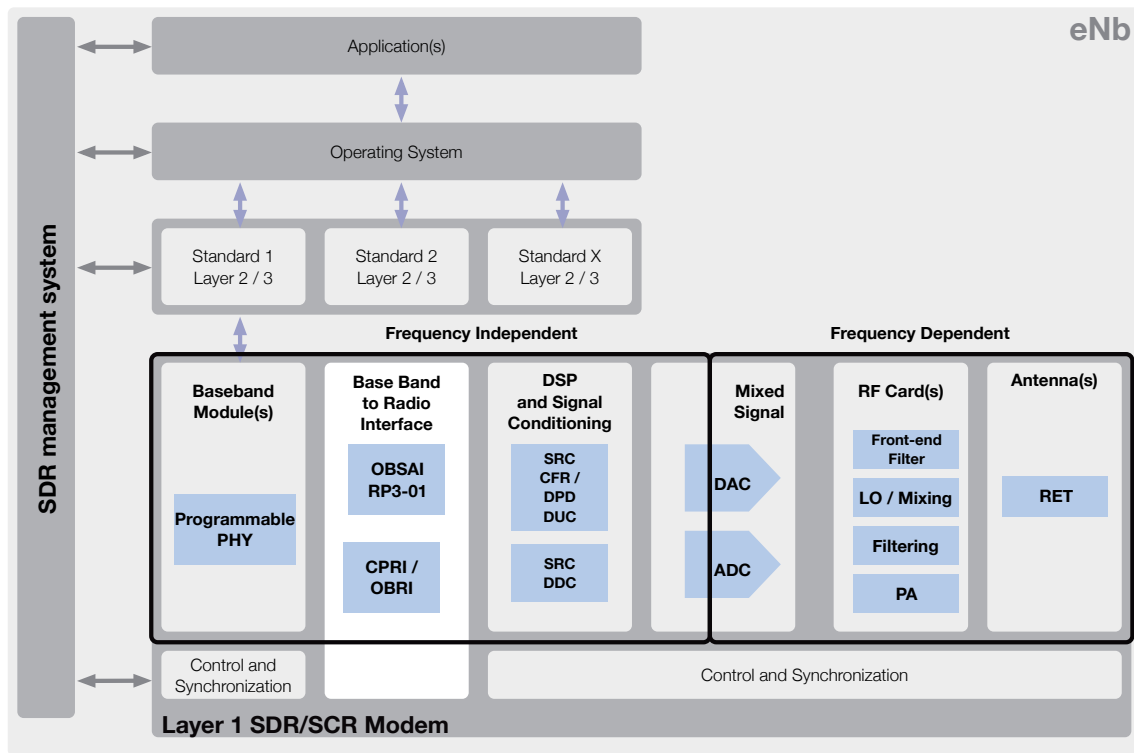


Figure 2.19: Software Defined / Configurable Multi-RAN eNB architecture with boundary between frequency independent functions and frequency dependent functions. The mixed signal, RF and Filtering and Antennas areas lie in the frequency dependent domain.

In Fig.2.19 there is a boundary between frequency independent functions and frequency dependent functions. The software configurability of frequency dependent functions is subject to technology and cost limitations that are presented in the next Section 2.4.2.

### 2.4.2 Limitations of Software Configurable Radios

The first discussion regarding limitations of SDR concerns the concepts of software upgradability and reconfigurability [54]. When applied to the base band processing, software upgradability means that through a software upgrade, one can update the processing baseband technology to support different waveforms. This terminology has often been used to describe base stations that can transition from GSM to UMTS/HSxPA and then to LTE. However, often the RF portion of the base station is not fully software configurable and thus not obeying to the true SDR definition because the radio portion is still hard-wired including limited frequency range for frequency synthesizers, power amplification, front end filtering and duplex mode of operations. Although software upgradeability enables technology changes in the baseband, the radio head portion of the eNB would need to be replaced to reflect new frequencies bands and operating range, larger channel bandwidths, different output powers etc.

In recent years this trend has been changing since RF equipment vendors, because of open architectures definitions and programmable FPGA technology have introduced digital radios solutions bringing a higher degree of reconfigurability pulling into the digital domain as many as possible of the RF functionalities.

Current state-of-the-art in commercial SDR is supporting different technologies stand-alone or simultaneously by using software control into a Single/Multi-RAN eNB environment. One key enabling factor for the commercial availability of such solutions has been the reduction in the cost of key critical radio components such as multi-carrier power amplifiers, wide-band converters, and filters as well as digital components like FPGAs combined with a higher integration of functionalities into a single IC. This combination enabled moving from simple upgradeability in the baseband to complex radio head reconfigurability, but it is still retaining several limitations when compared to SDR.

*The first limitation that still exists with software reconfigurable radios is the operation over a given frequency band or sub-band leading to logistic issues in case of spectrum re-allocation or radio planning.* Currently operating bandwidths rarely exceed 100 MHz of carrier frequency tunability. Among other reasons, this is due to the 3GPP fixed spectrum allocation policies and interference regulations. Sharp filtering and trade-offs are required in the RF architecture used for the up and down conversion (digital IF vs Heterodyne approaches). Furthermore, the limited linearity of standard power amplifiers across a wide-band is only provided only from efficient and costly GaN power transistors technology. Only the WiMAX TDD band in the 3.4 - 3.6 GHz range is having a 200 MHz operational bandwidth.

## 2.4. Software Radio Architecture

The second limitation is given by the instantaneous bandwidth that can be supported today with commercial AD and DA converters. Latest RRH generations provide up to 20 MHz of instantaneous channel bandwidth and it doesn't allow sufficient flexibility in supporting multiple technologies and frequencies using the same radio module. Although the radio head can be shared between technologies and the channel bandwidths can be switched through software depending on the technology, for wider bandwidths the linearity [55] and cost of wide-band DA and AD converters, as well as of several other components like RF and Power Amplifiers (PA) have to be improved. Therefore modern SDR base stations can support multiple technologies right from WCDMA, and LTE simultaneously, *but only in the same frequency band with limited bandwidth chunks of around 70-100 MHz* limiting the capability of SDR base stations today where for each spectrum band to cover, a separate radio unit is required.

Fig.2.20 shows an overview of commercial SCR / SDR radio components vs cost of the technology. The key components are the Interfacing technology, Digital Signal Processing (DSP), ADC/DAC, RF (Radio Frequency), Power Amplifier (PA) and Front End Filter with associated the key performance indicators and cost.

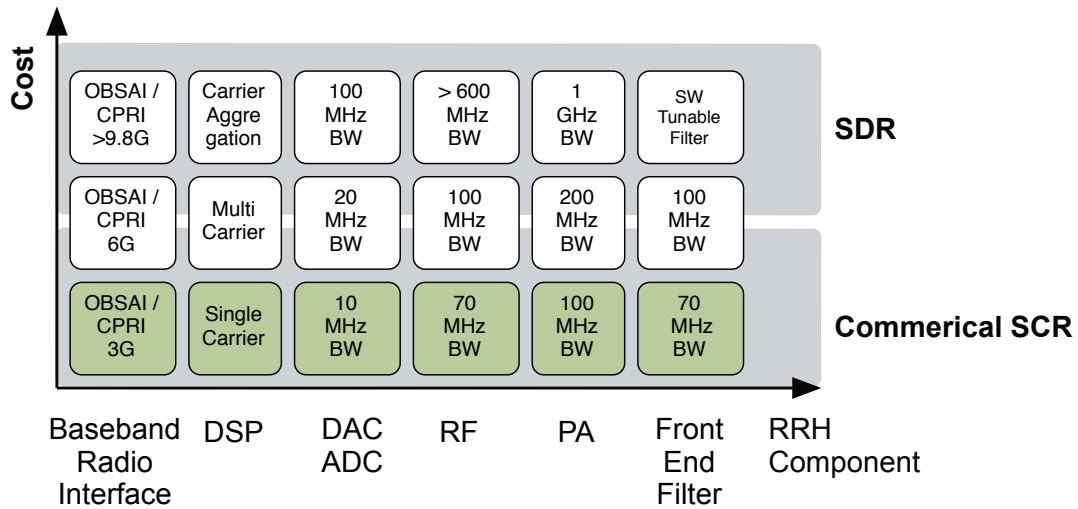


Figure 2.20: Overview of commercial SCR / SDR radio components vs cost of the technology. The key components are the Interfacing technology, Digital Signal Processing (DSP), ADC/DAC, RF (Radio Frequency), Power Amplifier (PA) and Front End Filter with associated the key performance aspect and cost.

In practical installations, however in reality only a portion of a deployed network can take advantage of remote SDR modules depending on what spectrum bands are in operation across that network. Reconfigurability, simultaneous operation, and single unit form factors are appealing for both Single/MultiRAN eNBs. Equipment vendors clearly see the advantages of SDR streamlining their manufacturing costs across multiple platforms, but in reality only few eNB sites can take advantage of the single SDR MultiRAN unit due to the component cost and fixed frequency allocation.

In understanding the real value proposition of SDR, the cost saving coming from logistic/manufacturing efficiencies for multi band modules that can be configured on the field / production and environmental/power consumption advantages of Single/Multi RAN base stations is appealing to operators. As LTE networks and beyond will start to rollout, with most LTE base stations being Single/MultiRAN capable, true SDR RF technology (not just reconfigurability) will start to have space into operator networks but still facing with the technology cost. Regulator bodies also have a key role to play in pushing SDR technology with sharing spectrum bands like 1800 MHz, 2100 MHz, 2600 MHz or 3500 GHz across multiple standards within the same eNB.

To conclude, SDR needs better branding in the wireless infrastructure space, and if SDR has to move away from its legacy as a military-grade technology to become a widely deployed commercial-grade technology, it needs to adapt to the use that operators can make of it today given the current technology and cost limitations as shown in Fig.2.20. Current SCR architecture may suffice to operators needs provided that a single eNB that can fully cover a limited band of operation in which Multi-RAN like UMTS / LTE can be supported. GSM support, Multi Carrier and Carrier Aggregation, as well as tunability across a large bandwidth affects component cost considerably and it is today not yet a commercial reality. Modularity and scalability concepts are important to ensure as much as possible of Hardware and Software re-use from the equipment vendors for more advanced configurations.

### 2.4.3 A Multi-RAN Remote Radio Architecture

This section will present a contribution on an ideal block architecture for an advanced remote radio head supporting a higher level of functionality integration and scalability supporting either 2x2 or 4x4 configurations.

#### System Partitioning, Interfaces and Functions Integration

The ideal high level partitioning is made using a modularity concept isolating the RF frequency dependent functions from the frequency independent functions as illustrated in Fig.2.19. This division is made to re-use the digital portion of the system across different frequency band system variants by only replacing the frequency dependent part. Modularity is also providing access to connect in parallel up to two 2x2 MIMO RF cards for reaching a 4x4 configuration. The system architecture is shown for reference in Fig.2.21.

The frequency independent functions include all the digital interface, control and signal processing functions shall be integrated into a single device ASIC or FPGA. The serializer, clocking circuitry and optical modules shall be external.

The frequency dependent functions include the AD and DA conversion stages, frequency up and down conversion and filtering, power amplification and front end filtering. The RF functions shall be integrated in RF TX and RX ICs for maximum flexibility and cost but they will not be here discussed in details.

The goal is to have a flexible and modular radio system supporting multiple radio standards like UMTS, LTE and GSM across several frequency bands and output powers in a MultiRAN system. From an interface perspective, both OBSAI RP3-01 and CPRI interfacing standards (See appendix C) are providing multi standard transport support except for CPRI and GSM support, which is expected to be in the specification by early 2011. Multi-channel bandwidths need to be supported (for example LTE 2.5/5/10/15/20 MHz plus UMTS 5 MHz and Multi-carrier GSM) in the same radio platform implementation, using only pure software reconfiguration to switch between them. In addition, support multiple carriers assigned to the same channel in a multi-carrier fashioned system is also required. To achieve this, the designer has to select between using a different clock domain for each rate or using one single-clock domain with specialized DSP blocks that enable software flexibility.

The single-clock domain technique using DSP blocks is very flexible and elegant [3]. Its advantage is that it can efficiently convert any sample rate into a common system rate lowering the design complexity. The sampling rate conversion (SRC), as in Fig.2.21, is achieved with

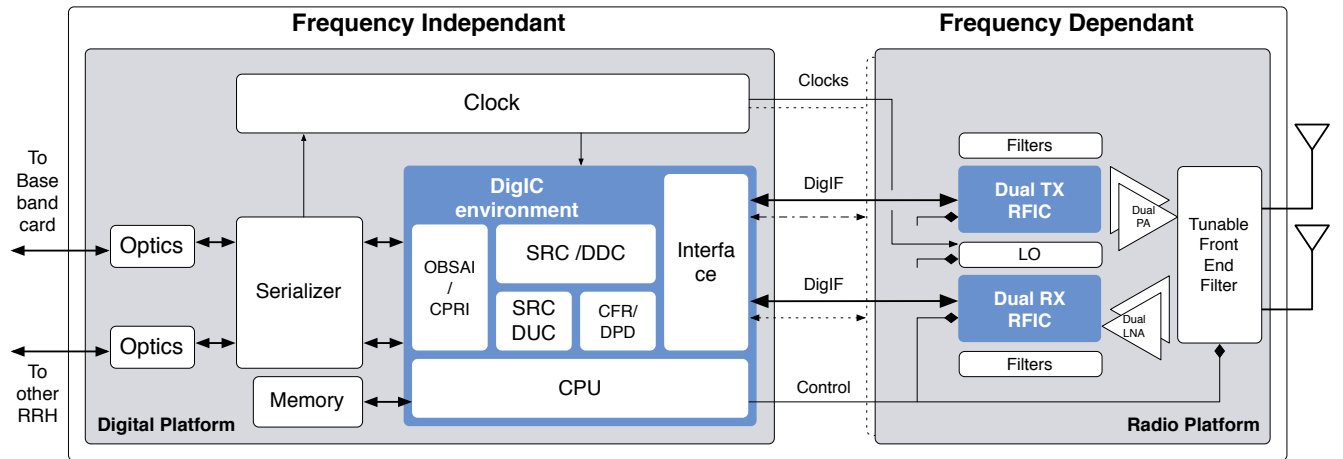


Figure 2.21: Architecture for a flexible and integrated remote radio head environment made essentially by three chips: a) a digital chip (serializer might be integrated in the digital chip in the future) containing the interfacing, DSP and control blocks - b) a RF TX Integrated Circuit (IC) including multi-channel transmission and DPD feedback path and c) a RF RX IC including multi-channel receiver paths and gain control.

Farrow filters that can efficiently implement arbitrary resampling rates. These are optimized for highest performance as well as low logical resources consumption. When these are combined with the multi-channel digital up-conversion (DUC) or digital down conversion (DDC) in the uplink direction case, they enable multiple sample rates to be processed concurrently and in the same clock domain of the digital-to-analog converter (DAC) or analog-to-digital converter (ADC). In this way, this method enables flexibility by supporting both single-clock and multiple-clock techniques. For example, the typical sample rate for a 10 MHz channel bandwidth of a WiMAX OFDMA signal is 11.2 MHz. Using a sampling rate converter the sample rate can reach 122.88 MHz with noise added by sampling kept below 74 dB [3]. For an LTE signal of 10 MHz, the sample rate will be 15.36 MHz and the SRC will require only a software reconfiguration of the filter coefficients for the given conversion ratio. Control functions shall be managed from a CPU which can be integrated in the digital environment. The functions for controls are initialization, configurations, monitoring and alarms.



## 2.5 Summary

In the evolution from 3G to 4G wireless networks, radio access standards meeting IMT-A requirements like LTE-Advanced are converging to a fewer number of options for growing the economies of scale for both user and base station equipment, thus reducing costs.

Spectrum availability and geographical harmonization, together with the expected capacity growth represent the current major challenge for the realization of adequate access networks. The large and fragmented number of frequency bands operating in either FDD or TDD modes is limiting the realization of true SDR equipment. The current fixed spectrum allocation has several limitations on flexibility and optimal frequency use leading to non-optimized traffic load sharing and in several regions not having frequency blocks sufficiently wide to accommodate larger channel bandwidths. Dynamic spectrum allocation and advanced techniques for radio channel capacity improvement like MIMO and Carrier Aggregation (CA) have been addressed as they maximize channel capacity and throughput, thus impacting the bandwidth demand and the realization of a properly dimensioned physical radio access layer.

IMT-Advanced technology will mature into its full capabilities within the next 5-10 years, however the key frequencies between 1.7-2.7 GHz and total bandwidth requirements up to 40 MHz have been identified as the most important on a geographical basis for the next 3-5-years. Early deployments will be in the 2300-2400 MHz band for China, 2.1 GHz and 2.6 GHz in Europe and US. On such time scales, a configuration with 2x2 MIMO and 40 MHz operating bandwidth per antenna is by far the most important and relevant one for use in both FDD and TDD networks and supporting multi-carriers in several configurations (for example  $20 + 20$ ,  $20 + 10 + 10$ ,  $20 + 10 + 5 + 5$ ).

The boundary between software defined and software configurable radios has been investigated presenting the limitations of current commercial radio technology. Functions have been partitioned in frequency independent and frequency dependent parts, where the latter is the limiting factor for having full SDR applications. The major limitation identified are operations over a limited frequency range and thus requiring several radio variants for larger bands coverage. IMT-A requires access to portion of spectrum as high as 100 MHz, and this constitutes a considerable extension impacting mostly the DA and AD technology available today. Multi-RAN operations are possible, but only in the same frequency band, limiting the capability of SDR base stations today where for each spectrum band to cover, a separate radio unit is required. Finally, a proposal for a highly integrated radio module was presented. The system presents a digital environment, with a digital chip that hosts interfacing and digital signal processing / conditioning functions for 4 transmitter and 4 receiver channels. The digital chip interfaces to generic RF environments, where the TX and RX analog chain are grouped in a TX RF IC and RX RF IC with power amplification. This solution offers modularity and scalability, enabling to support 2x2 or 4x4 configurations by just adding another RF card.

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## Chapter 3

# Base Band to Radio Interface Analysis

The discussions in this chapter are based on the work done from the Author in the following articles:

- C. Lanzani and et al., *RP3 / RP3-01 Interface Profile Document*. OBSAI, [www.obsai.com](http://www.obsai.com), May 2009 [6] where the personal contribution was the project proposal and lead including delay measurement and sample mapping methodology.
- RP3-TWG, *OBSAI RP3 Specification v.4.2*. OBSAI, [www.obsai.com](http://www.obsai.com), v.4.2 ed., March 2010 [5] where the personal contribution is about the delay measurement procedure.
- C. Lanzani, “A path toward unified remote radio interface,” in *IWPC Workshop on Flexible 4G Base Station Architectures*, ([www.iwpc.org](http://www.iwpc.org)), 2008 [8] where the personal contribution is about the interoperability and 10G interface rate needs.
- C. Lanzani, “Open base station architecture: Can standardization enable true innovation?,” in *PCIA 2008*, ([www.pcia.com](http://www.pcia.com)), 2008 [7] where the personal contribution about is the entire interfacing technology presentation highlight.

## 3.1 Overview of open eNB interfacing standards

An open interface definition between base band and radio equipment is a catalyst for standardization bringing several cost and logistic benefits for the consumer. Standardization enables a specialized ecosystem of suppliers focused on module and components level. Innovation and product differentiation will focus on solving narrow and specific customer problems in a cost effective manner rather than maximize performances and flexibility. This was the motivation behind organizations like the OBSAI and the CPRI industry forums to support such vision.

The Common Public Radio Interface (CPRI) [24] together with it's Open Radio Interface (ORI) extension [26, 56], and OBSAI RP3-01 interfaces [57, 5] will find greater applications in future 4G networks with distributed base stations due to the multitude of frequencies and installment scenarios where open base stations will bring advantages. A detailed overview of the open base station interface standards is provided in Appendix C. Historically, the selection of either CPRI or RP3-01 interface from OEMs or System Integrators has been mostly a political decision based on legacy with existing systems for reduced engineering efforts and based on differentiating product lines between vendors. Overall, the CPRI standard seems to prevail in the market over OBSAI RP3. From a technical perspective, the interface selection requires an evaluation of actual network system requirements in terms of dimensioning for coverage, user capacity, throughput and installation topology.

Both CPRI and RP3-01 standards have been engineered to efficiently transport base band data, synchronization and control flows between base band processing and radio modules of an eNB as in Fig.3.1.

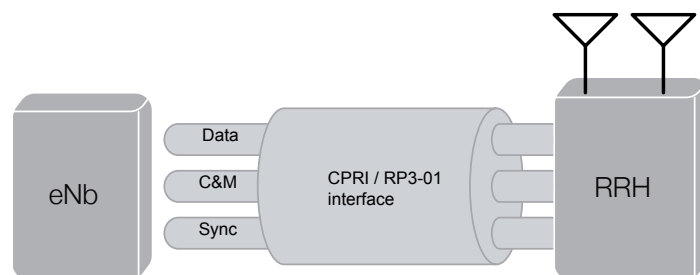


Figure 3.1: Base band to radio interface concept showing a link with embedded data, synchronization and control channels between the eNB station and a Remote Radio Head (RRH).

### 3.1. Overview of open eNB interfacing standards

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This section focuses on analyzing the state-of-the-art CPRI / ORI and RP3-01 protocols including framing and mapping schemes and provides metrics for understanding and selecting the proper system configuration and topology. In the protocol analysis, the four major areas will be subject of discussion in this section:

- Protocol structure.
- Data carrier capacity.
- Logical synchronization mechanisms.
- Delay measurement procedures.

As the expected capacity growth of IMT-A networks is considerable and can be seen already today in the early LTE systems, analysis of the CPRI and RP3-01 protocol structure and carrier capacity is required for the radio sub-network dimensioning. Given the amount of antenna and bandwidth configurations that was presented in chapter 2, a metric for an appropriate interface selection and configuration is required for understanding the impact that 4G requirements will end up having on the interfaces.

A daisy chained RRH topology requires flexible carrier and C&M routing control and configuration. Furthermore synchronization complexity between eNB and multiple radio modules increase, and in theory it shall be achievable easily and providing robustness and stability over time. Synchronization accounts for both physical and logical radio frame synchronization [24, 57, 5]. In addition due to the remote nature of the data communication the delay management procedure plays an important role. Logical synchronization mechanisms are analyzed in this section describing the advantages and constraints for both CPRI/ORI and RP3-01 interfaces. As no relevant studies available on this subject have been found, the novelties in these contributions are the detailed protocol analysis for each of the two standards providing an apple-to-apple comparison in terms of carrier capacity, synchronization and delay measurement methodologies and work done by the Author in the standardization forums to improve usage of the interfaces.

### 3.1.1 CPRI Protocol Structure

In CPRI the time slot basic structure as in Fig. 3.2 is the basic frame made of 16 bytes, which includes both the control words and the IQ block made of independent samples from each of the antenna carriers in TDM - e.g I1Q1 I2Q2 I3Q3 I4Q4 etc. As an example, the CPRI 614.4 Mbps basic rate defines an IQ data block of fifteen (15) bytes, 120 bits capable of containing eight (8) samples of 15 bits each. Four (4) carriers at 15 bits resolution and 3.84 Msps sample rate can be transported into the IQ data block portion of the basic frame structure using 120 bits for a total of hundred (100) samples per carrier. The CPRI frame structure meets the RP3 MG structure every twenty-five (25) Basic Frames, thus 5.21  $\mu$ s. CPRI frame duration is 10 ms and it is composed from 150 HyperFrames. Each HyperFrame contains 256 Basic Frames as shown in Fig.3.3.

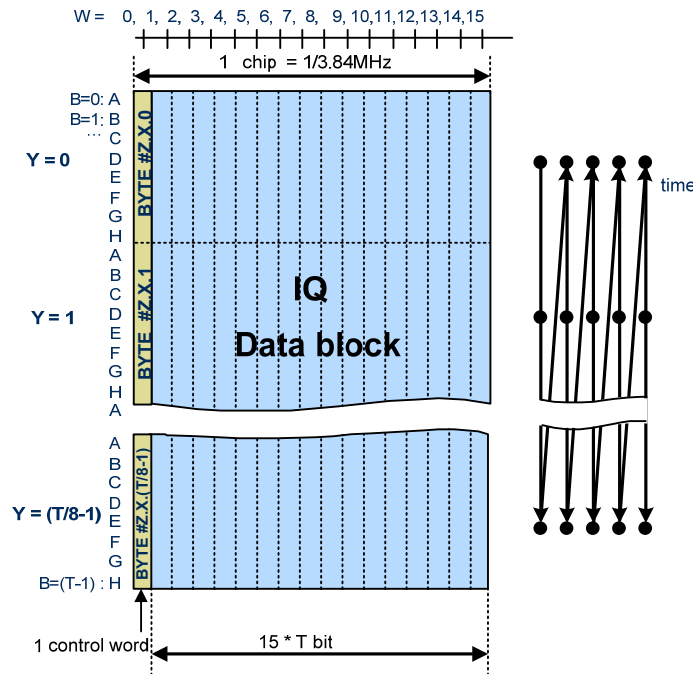


Figure 3.2: Generic definition of CPRI basic frame that scales with the line rate weight [24].

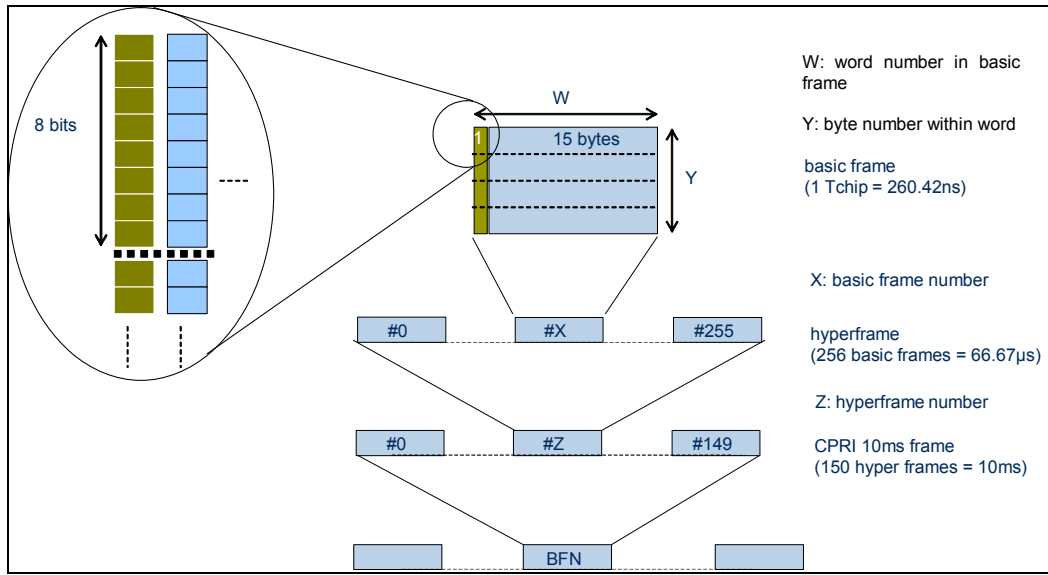


Figure 3.3: Generic definition of CPRI basic frame that scales with the line rate weight [24].

#### 3.1.2 RP3-01 Protocol Structure

The RP3 / RP3-01 frame structure format is defined from [6, 5] by selecting the M\_MG, N\_MG and K\_MG parameters. The frame size in bytes scales with the "i" parameter representing the factor of multiple of the basic line rate of 768 Mbps. The basic structure is the RP3 message fixed 19 bytes. It includes 3 bytes of header and 16 bytes of data payload. The RP3 message period at the basic rate of 768 Msps corresponds to the UMTS time slot duration of 260 ns. RP3 Header is subdivided into ADDRESS, TYPE and TIMESTAMP fields. For detailed description of RP3 HEADER format please refer to [5].

In RP3 the basic clock frequency is 38.4 MHz, which is a factor of 1.25 higher of the CPRI basic clock frequency of 30.72 MHz ( $8 \times 3.84$  MHz). This increase is required for the extra header bytes bandwidth within the same time-slot period. A message group (MG) is the overlaying structure that is made of twenty (20) messages of IQ data and one (1) message of control and one (1) K-char. The period of a MG is  $5.21\mu s$ <sup>1</sup>.

<sup>1</sup> $MG_{period} = \frac{10}{1920}ms$

### 3.1. Overview of open eNB interfacing standards

The structure is illustrated in Fig. 3.4 below:

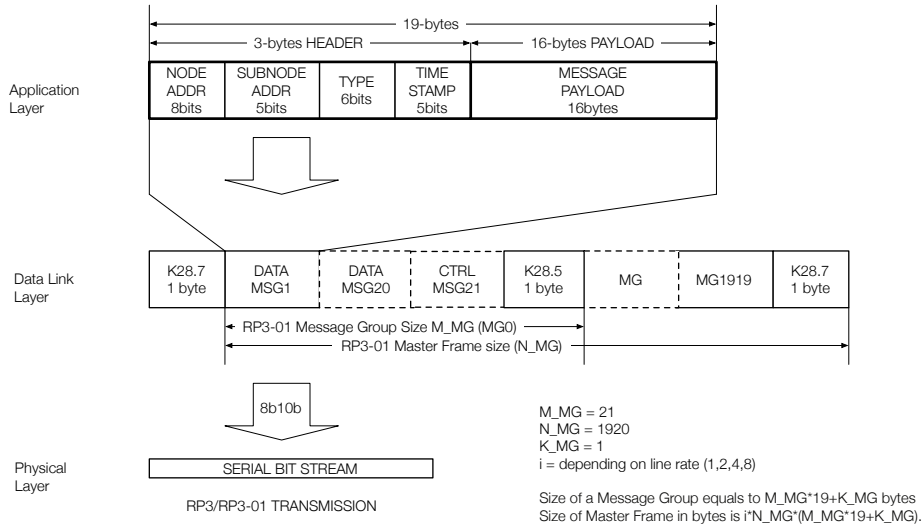


Figure 3.4: RP3 / RP3-01 Frame structure overview with RP3 message, RP3 Message Group and RP3 Frame.

The key property of RP3 messages is that the RP3 message PAYLOAD (16bytes) carries consecutive samples from the same antenna carrier targeting an individual antenna-path defined from the node/sub-node address file in the RP3 HEADER. The envelope (container) of the sample is *fixed* at 8-bits for UMTS and 16 bits for LTE, allowing to map eight UMTS sample pairs or four LTE sample pairs respectively. Since in OBSAI the sample envelope is fixed to 16 bits, in case 15-bits samples are used for LTE for example, one bit will be left unused for each sample and this bandwidth will be lost, unlike what happen in CPRI.

#### 3.1.3 Digitized Baseband Signals Representation

Base band data carrier capacity for CPRI/ORI and RP3-01 it is essentially defined by the amount of digitized base band carrier signals that could fit over a link at a given interface line rate. Both interfaces operate on base band signals as this format represents a bandwidth efficient usage for the transport. Other approaches may consider digitized Intermediate Frequency (IF) with rates around 100 - 200 MHz or analogue Radio frequency over Fiber (RoF). These approaches are introducing several challenges for the transport and they will not be further discussed here. Base band signals transport can be further optimized using compression techniques that operate on the Peak to Average Ratio of the signal and thus reducing the bit resolution required for each sample pair. This results in CPRI in additional transport bandwidth available for additional carriers Although performing algorithms will minimize the signal distortion

### 3.1. Overview of open eNB interfacing standards

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introduces by the compression / decompression phases, compression techniques will also lead to proprietary mapping schemes going against standardization. This section will only focus on the transport of standard base band signals *non-compressed*.

In every wireless standard, a base band carrier can be efficiently defined by its In-Phase (I) and Quadrature (Q) components representing a RF channel bandwidth defined from the modulator block configuration with a given sample resolution and sample rate. I/Q representation is a rectangular representation of the polar diagram. On a polar diagram, the I axis lies on the zero degree phase reference, and the Q axis is rotated by 90 degrees. The signal vectors projection onto the I axis is its I component and the projection onto the Q axis is its Q component as shown in Fig.3.5

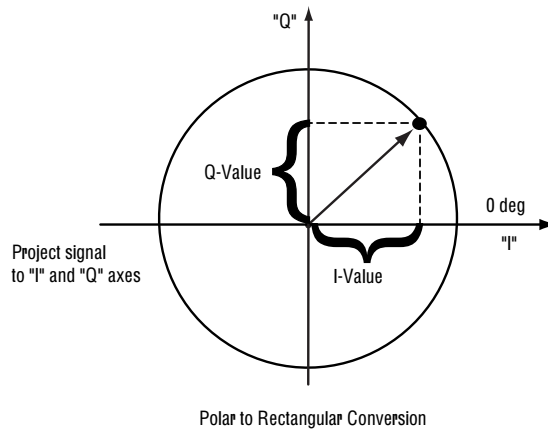


Figure 3.5: I/Q Format illustration of polar to rectangular conversion.

Digital modulation is easy to accomplish with I/Q modulators that maps the data to a number of discrete points on the I/Q plane known as constellation points. For transmitters, the main advantage of I/Q modulation is the symmetric ease of combining independent signal components into a single composite signal and later splitting such a composite signal into its independent component parts. For a receiver, the composite signal with magnitude and phase (or I and Q) information arrives at the receiver input. The input signal is mixed with the local oscillator signal at the carrier frequency in two forms. One is at an arbitrary zero phase. The other has a 90 degree phase shift. The composite input signal (in terms of magnitude and phase) is thus broken into an in-phase, I, and a quadrature, Q, component. These two components of the signal are independent and orthogonal. The concept is illustrated in Fig.3.6:



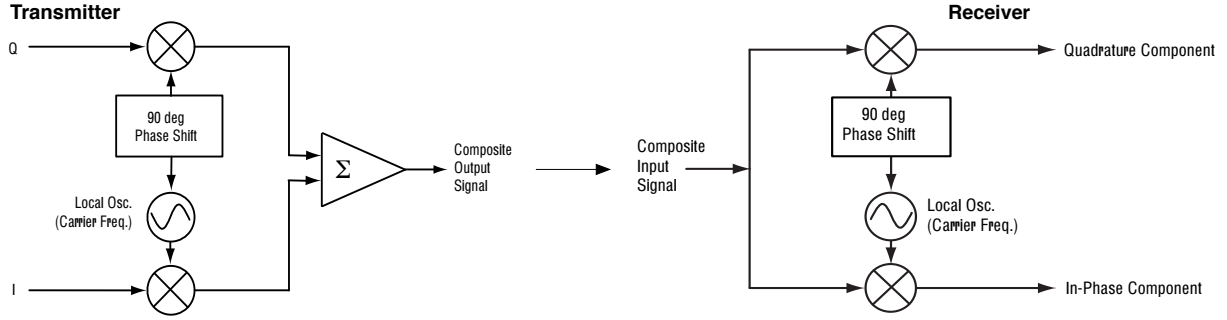


Figure 3.6: I/Q Format in a digital radio transmitter and receiver.

## 3.2 CPRI / RP3-01 Framing Structures Comparison

In a single carrier radio configuration scenario each I/Q carrier signal can be assigned to an individual antenna within a radio module. In a multi-carrier scenario instead more than one carrier can be assigned to an individual antenna within the same instantaneous bandwidth. Carrier and antenna assignment is made at eNB configuration. Each radio can support one or multiple antennas depending on the configuration, and as well one or multiple carriers per antenna as discussed in Section 2.3.1. From a pure digital transport perspective the following signal characteristics shall be known at system design and configuration as in in Fig.3.2 and listed below:

- Radio standard in use.
- Channel Bandwidth (MHz).
- Amount of I/Q Carriers.
- I/Q Carrier sample rate (Msamples/sec).
- I/Q Carrier sample resolution (Bits).

The effective (usable) bandwidth on CPRI / RP3-01 interfaces is calculated after the 8b10b channel coding [58] that uses 25% of the total bandwidth for improving the data transmission. The amount of carriers that can fit over a link depends on how much data bandwidth is available for a given sample rate and the sample width of choice together given the mapping scheme and protocol framing structure. Carrier capacity can be increased using higher transmission line baud rates and in some cases by optimizing the data mapping to use the given bandwidth more efficiently. The I/Q sample resolution measured in bits it is a key parameter in defining the amount of bandwidth that will be utilized for each I/Q carrier.

### 3.2. CPRI / RP3-01 Framing Structures Comparison

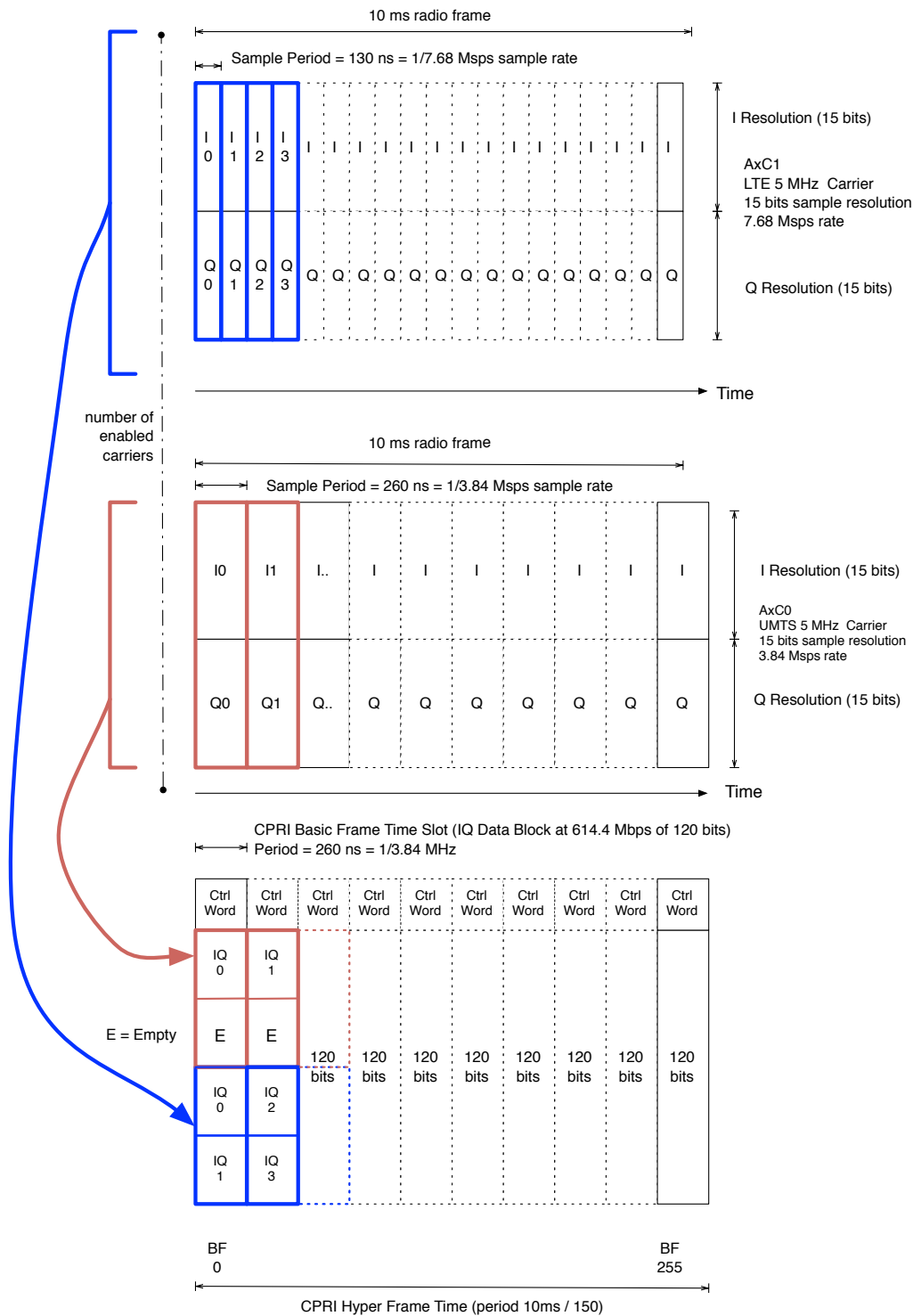


Figure 3.7: Example of configuration parameters with two I/Q carriers. In the figure it is shown an LTE 5 MHz carrier with 7.68 Msps sampling rate and 15 bits resolution as well as a UMTS 5 MHz carrier with 3.4 Msps sampling rate with 15 bits resolution. For both UMTS and LTE the radio frame duration is 10 ms. The selected CPRI rate is the lowest one at 614.4 Msps with Mapping Method 3 Backward compatible.

### 3.2. CPRI / RP3-01 Framing Structures Comparison

Different wireless standards and RF requirements relate - among a number of other factors related to the signal properties - to channel bandwidth, SEM compliance, output power and dynamic range for transmission. For reception, they relate to sensitivity and modulation requirements leading to different IQ sample bits resolutions. For a Multi-RAN system it is possible to calculate the amount of required bit resolution to achieve a given target performances. The calculation are addressed in the report [9] made from M. Hoegdal and N. Behjou from Radiocomp ApS for a Multi-RAN radio transmitter and receiver. Table 3.1 identifies the results highlighted in [9] from for a transmitter and receiver assuming different margins from the SEM compliance. We will assume that a 5 dB margin will suffice for most Multi-RAN applications that includes UMTS and LTE simultaneously.

Ch.BW (MHz)	ENOB (10dB Mrg.)	ENOB (5dB Mrg.)	ENOB (0dB Mrg.)
20	12.6	11.8	11.0
40	13.1	<b>12.3</b>	11.5

Table 3.1: Number of bits required for the DAC (Downlink path) of a Multi-RAN radio module with UMTS / LTE at 40 MHz channel bandwidth assuming a worst-case 49 dBm output power meeting the MC-GSM SEM compliance mask with a signal PAR = 7.5 dB and a sampling frequency of 983.04 MHz (8x 122.88 MHz)[9].

From the above table it can be observed that an ENOB of 12.3 bits is required with a margin of 5dB to the SEM for up to 40 MHz BW signals. In Fig.3.2 instead the required bits for ADC in Multi-RAN applications are shown taken from [9]:

Ch.BW (MHz)	ENOB (10dB Mrg.)	ENOB (5dB Mrg.)	ENOB (0dB Mrg.)
20	10.8	10.0	9.2
40	11.3	<b>10.5</b>	9.7

Table 3.2: Number of bits required for the ADC (Uplink path) of a Multi-RAN radio module with UMTS / LTE at 40 MHz channel bandwidth assuming 4 multi carriers, maximum sensitivity of -101.5 dBm and 122.88 MHz sampling frequency [9].

It can be seen from the figure above that an ENOB of 10.5 bits in Uplink should suffice for the Multi-RAN configuration. If we exclude the MC-GSM case, which a UMTS / LTE Multi-RAN system can be safely configured using a 15 bits sample envelope for the transport over the base band to radio interface of choice [26]. The next sections will use the 15 bits figure for all the discussions related to compute the transport interface bandwidth requirements.

The above analysis on the effective number of bits (ENOB) requires for Multi-RAN is important when comparing OBSAI and CPRI/ORI. The basics of OBSAI RP3 and CPRI/ORI frame structure are here briefly introduced for reference in section 3.1. With regards to the mapping,

### 3.2. CPRI / RP3-01 Framing Structures Comparison

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the major difference between the two standards is the way I/Q samples are mapped into the user data. The data container is named IQ Data Block in CPRI and RP3 Message Payload in OBSAI RP3 / RP3-01.

In RP3-01 the I/Q container is fixed at 16 bits. This has major implications on the capacity of either interface and will be discussed in the next sections. We will assume, based on the results shown in Fig.3.1 and Fig.3.2 that 15 bits sample size will suffice for UMTS / LTE Multi-RAN configuration in either downlink or uplink paths.

#### 3.2.1 Interface Capacity Comparison: RP3-01 vs. CPRI

In general the two framing structures differ mainly by CPRI being TDM based and RP3-01 by being packet based. Both interfaces were initially designed around the 3GPP UMTS WCDMA standard rates, where the time-slot definition was the UMTS chip, lasting 260.4 ns of period for a chip rate of 3.84 Msps. The UMTS frame duration is 10 ms. Similarly both interfaces use clock rates that are multiples of the 3.84 MHz base frequency and both use 10 ms reference frame timing. Note, standards like 802.16 and 3GPP LTE were added recently to the interface specifications and maintains the basic framing definitions for backward compatibility and legacy issues.

The RP3-01 interface carrier capacity is defined by the parameter "X" in the standard [5] which indicates the integer number of carriers for each given sample rate at 16 bits that can fit on a given line rate. In appendices D,F and G of [5] are defined the "X" values for each standard and sample rate.

Likewise, CPRI the UMTS / LTE carrier capacity can be computed with the following formula in Eq.3.1 representing the Basic Mapping mode defined in [24]:

$$Number\_of\_carriers = \frac{bits\_in\_IQ\_container\_block}{2\_samples\_ (IQ) * sample\_size * oversampling\_ratio} \quad (3.1)$$

where:

$$\begin{aligned} bits\_in\_IQ\_container\_block \ (bits) &= \text{According to CPRI line rate in use [24]} \\ 2\_samples\_ (IQ) &= I \ segment \ and \ Q \ segment \ for \ each \ sample \\ sample\_size \ (bits) &= sample \ size \ in \ use \\ oversampling\_ratio &= multiples \ of \ 3.84 \ Msps \ LTE/UMTS \ rate \ up \ to \ eight \ (30.72 \ Msps). \end{aligned}$$

### 3.2. CPRI / RP3-01 Framing Structures Comparison

When using a higher CPRI line bit rate like 2.4576 Gbps, the IQ container block is made of 480 bits. If we want to calculate how many 20 MHz carriers @ 30.72 Msps (8 times oversampling ration of UMTS 3.84 Msps rate) will fit using a 16 bits and a 15 bits sample size in a I/Q representation (sample pair) using Eq.3.1 it will give:

$$Number\_of\_carriers = \frac{480}{2 * 16 * 8} = 1.875 \quad (3.2)$$

$$Number\_of\_carriers = \frac{480}{2 * 15 * 8} = 2 \quad (3.3)$$

The results of Eq.3.2 and Eq.3.3 are illustrated in Fig.3.8 and Fig.3.9 respectively. In CPRI, the IQ Data block bit size can be optimized depending on the sample resolution from 4 bits up to 20 bits. As an example, let's consider the mapping of 2 LTE 20 MHz carriers (AxC0 and AxC1) with a sample rate of 30.72 MHz (8x oversampling ratio) over a CPRI Basic Frame. We use a 2.4576 Line bit rate and the basic mapping mode [24] with 16 bits (3.8) and with a 15 bits (3.9) IQ sample size. This result in an envelope of 32 bits and 30 bits respectively per sample pair.

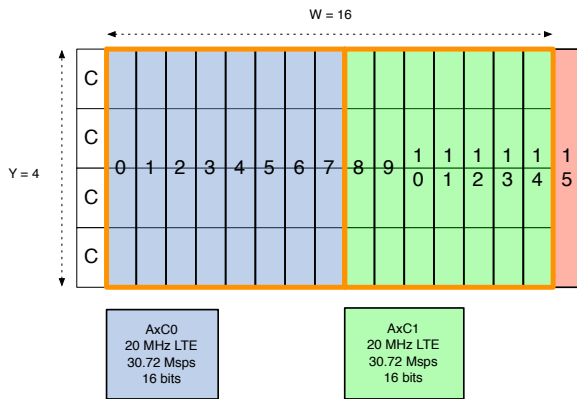


Figure 3.8: CPRI 20 MHz LTE Mapping with 2.4576 Gbps line rate and 16 bits sample size calculated using Eq.3.1 assuming a single carrier per antenna. It is shown that AxC1 last sample does not fit with the IQ Data block size exceeding the available bandwidth. This configuration does not enable a single hop RRH with 2x2 MIMO LTE 20 MHz per antenna.

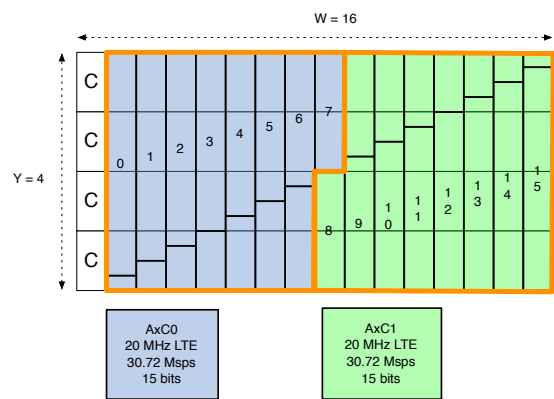


Figure 3.9: CPRI 20 MHz LTE Mapping with 2.4576 Gbps line rate and 15 bits sample size using Eq.3.1 assuming a single carrier per antenna. It is shown that AxC1 matches with the IQ Data block size enabling full mapping of the two carriers. This configuration enables a single hop RRH with 2x2 MIMO LTE 20 MHz per antenna.

### 3.2. CPRI / RP3-01 Framing Structures Comparison

In RP3 at the 768 Mbps basic rate, using UMTS mapping in downlink 16-bits resolution and 3.84 Msps sample rate enables to transport  $X = 4$  carriers into each MG structure for a total of 100 samples per carrier using the Index / Modulo mapping rules. In uplink mapping the UMTS sample size is 8-bits, however with a 2x oversampling factor with respect to the chip rate, so the  $X = 4$  is maintained for uplink as well. For sample rates not-integer multiples of 3.84 Msps, Dual Bit Map rules are then used. As a further example, let's consider the case of a OBSAI RP3-01 line rate using LTE 20 MHz carrier at 15 or 16 bits sample size. According to [5] Appendix F Table 59,  $X = 4$  and it will be the same for either sample size in use.

Analyzing the framing structure it is possible to see how the frame bandwidth it is utilized in either interface and compare the carrier grade capacity as shown in Fig.3.10 and Fig.3.11.

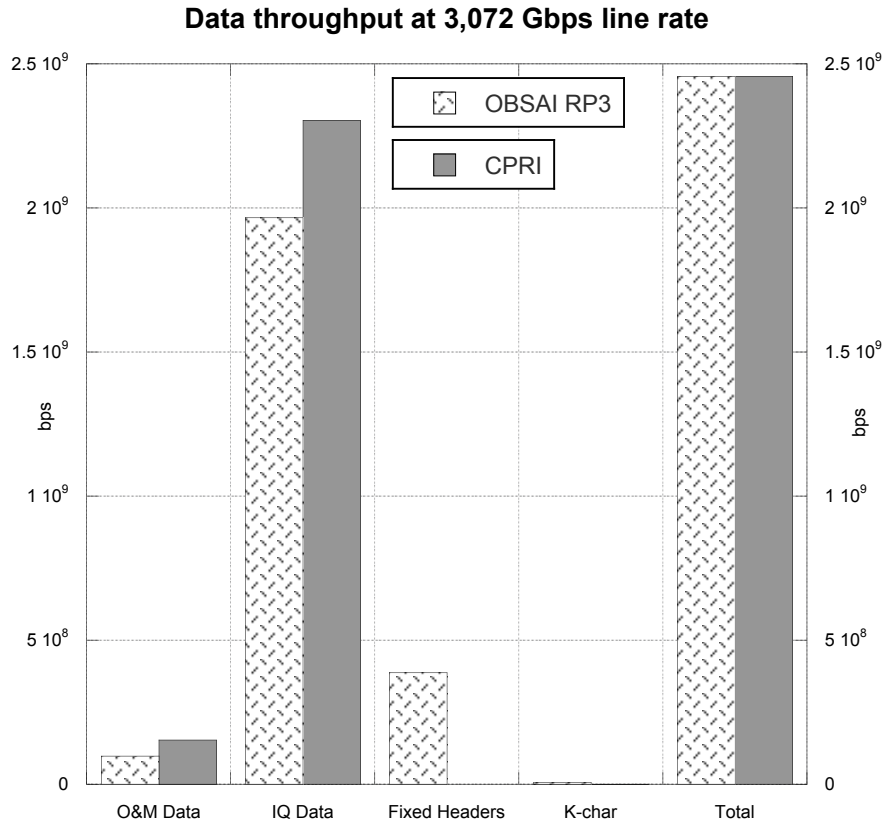


Figure 3.10: Types of data flow throughputs for OBSAI RP3-01 and CPRI. In the graph are shown O&M data, IQ data, Fixed Headers, K-Characters and Totals. It is shown that RP3-01 has more header overheads than CPRI, and this results in a lower bandwidth available for carriers.

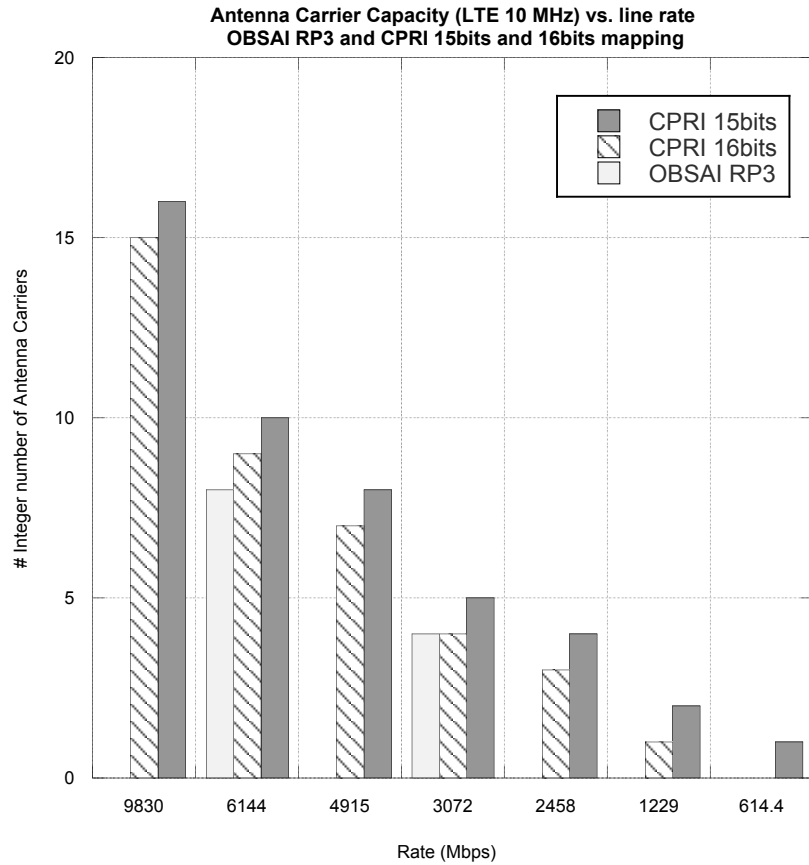


Figure 3.11: Carrier grade capacity for OBSAI RP3 and CPRI using 15 and 16 bits samples configurations for rates up to 9.830 Gbps for CPRI. It is shown that CPRI has slightly higher capacity for transporting an additional antenna carrier.

### 3.2. CPRI / RP3-01 Framing Structures Comparison

Likewise, it is easy to calculate the carrier capacity for a number of bandwidths and antenna configurations including 2x2, 4x4 and 8x8 modes for the different available line rates at 9.830 Gbps (in CPRI/ORI only [26]), 6.144 Gbps and 3,072 Gbps [24, 26, 5]:

Line	Antenna	Channel			
Rate	Configurations	BWs			
<b>3.072 Gbps</b>		<b>20 MHz</b>	<b>40 MHz</b>	<b>80 MHz</b>	<b>100 MHz</b>
	2x2	1 RRH	-	-	-
	4x4	-	-	-	-
	8x8	-	-	-	-
<b>6.144 Gbps</b>					
	2x2	2 RRH	1 RRH	-	-
	4x4	1 RRH	-	-	-
	8x8	-	-	-	-
<b>9.830 Gbps</b>					
	2x2	4 RRH	2 RRH	1 RRH	<b>X</b>
	4x4	2 RRH	1 RRH	-	-
	8x8	1 RRH	-	-	-

Table 3.3: Number of RRH supported based on different antenna configuration and CPRI/ORI interface rates at 9.830 / 6.144 / 3.072 Gbps with 15 bits sample size using LTE 20 MHz Component Carriers calculated using Eq.3.1 assuming a single carrier per antenna.

From Table 3.3 it is possible to conclude that the full IMT-A bandwidth of 100 MHz per antenna even in a single 2x2 MIMO antenna configuration *can not be met with the current line rate definitions of 6.144 Gbps and upcoming 9.830 Gbps*. This is of great relevance in the dimensioning study of the interconnectivity bandwidth requirements.

In order to obtain a 2x2 MIMO 100 MHz remote radio system, the interconnectivity bandwidth has to be increased and a suited line rate required is 12.288 Gbps as shown in 3.4:

Line	Antenna	Channel			
Rate	Configurations	BWs			
<b>12.288 Gbps</b>		<b>20 MHz</b>	<b>40 MHz</b>	<b>80 MHz</b>	<b>100 MHz</b>
	2x2	5 RRH	2 RRH	1 RRH	<b>1 RRH</b>
	4x4	4 RRH	2 RRH	-	-
	8x8	1 RRH	-	-	-

Table 3.4: Number of RRH supported based on antenna configuration and CPRI interface at 12.288 Gbps with 15 bits sample size calculated using Eq.3.1 assuming a single carrier per antenna.



A 12,288 Gbps rate enable a single-hop high bandwidth connection between one (or more) base band processing unit and a single radio module capable of true broadband operations meeting IMT-Advanced requirements.

## 3.3 Study on Protocol Interoperability

Until today the roadblock toward plug and play interaction between base band and radio equipments was the lack of a complete, fully specified and vendor agnostic interface definition that the entire industry would accept unambiguously. Historically the barrier has been that prior to the adoption of OBSAI or CPRI, for more than the last decade each OEM has been implementing proprietary interface flavors.

OBSAI RP3-01 and CPRI interfaces can be considered for for many aspects complementary standards but some of their openness, interpretation and richness of options have been the source of several debates and slow adoption in the industry, overall leading to:

- Greater Engineering work to convert from proprietary to standardized interfaces.
- Efforts invested in management systems definition, development and verification.
- High NRE costs for integration of third party equipment.
- Longer lead times for equipment availability and operations.

In general, as in every layered protocol, interoperability factors can be addressed on a layer-based approach, where for both RP3 and CPRI standards the grouping of functionalities into layers is similar according to the OSI model [59]:

- Physical Layer or L1
- Data Link Layer or L2
- Transport Layer (often in implementations tightly integrated with L2 or L3 functionalities)
- Application Layer or L3, which is also known as Control & Management layer.

The implementation of L1 and L2 is generally hardware oriented, while L3 is normally the software application acting on the top. The distinction between L2 and L3 is not always visible for a given implementation.

#### 3.3.1 Limitations of Equipment Interoperability

The problem of equipment interoperability concerns most of the ecosystem of providers and developers that wish to source base band or radio equipment from third party companies and faces with challenges in integrating them together. The main causes of interoperability problems can be summarized as it follows:

- Interpretation, ambiguity and lack of clarity of the specifications leading to different implementations.
- Richness of options in the specifications and selection of mandatory and accessory options.
- Configuration options.
- Specification of Control & Management and Synchronization layer.
- Number of proprietary variations to be supported.

Interoperability is playing a major role in an interfacing standard. The Author discovered a number of issues in the RP3 specification limiting the extent of interoperable and plug & play system operations. The major discovery was an unclear definition of the reference measurement points for RTT delay measurements at the physical layer. The major delay components are shown below in 3.12:

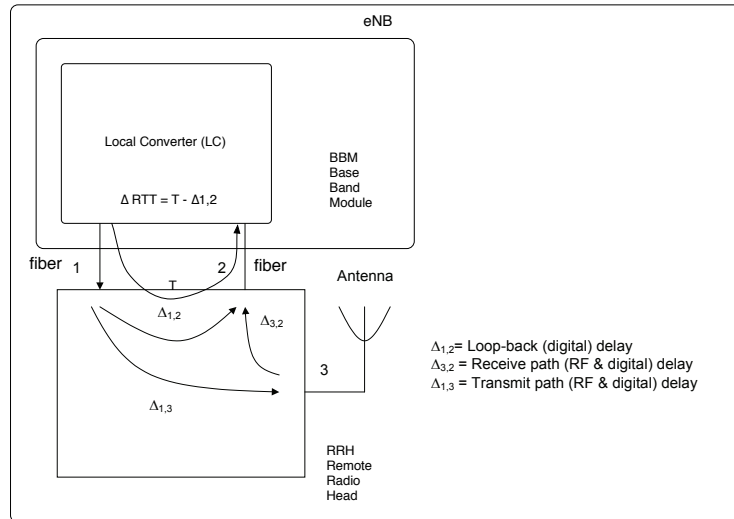


Figure 3.12: Delays in an eNB between a BBM/LC and a RRH. LC is responsible to calculate the  $\Delta_{RTT}$  which is the difference of the total Round Time (T) and the internal RRH delay  $\Delta_{1,2}$ [5]

### 3.3. Study on Protocol Interoperability

The RP3 standard does not clearly define reference points for RTT measurement at RRH side. Likewise, at the eNB side, the measurement points for RTT were not detailed and RTT procedure was approximating a symmetrical (50% DL / 50% UL) propagation delay over the link (fiber) as well as into the system. Depending on placement of reference measuring points at both LU and RRH this assumption may be valid (symmetrical case) or not (non-symmetrical case). Moreover, compensation of fixed / variable delays into  $\Delta_{1,2}$  is not defined in RP3. Depending of availability of measurements of all fixed / variable components in PCS layer, inaccuracy of the measurement is introduced. The inaccuracy accumulates for each RRH hop. The two main issues discovered were related to the following:

- The reference measurement point for delays - if not clearly specified - can be located after:
  - *Cable\_Delay*
  - *Cable + OE\_Conversion + PCB\_Trace\_Delay*
  - *Cable + OE\_Conversion + PCB\_Trace\_Delay + SerDes\_Input\_Buffer\_Delay*
  - *Cable + OE\_Conversion + PCB\_Trace\_Delay + SerDes\_Input\_Buffer\_Delay + Internal\_Logic\_Delay*

An example to see the issue regarding the correct placement of the reference measurement points is given below in Fig.3.13 and Fig.3.14:

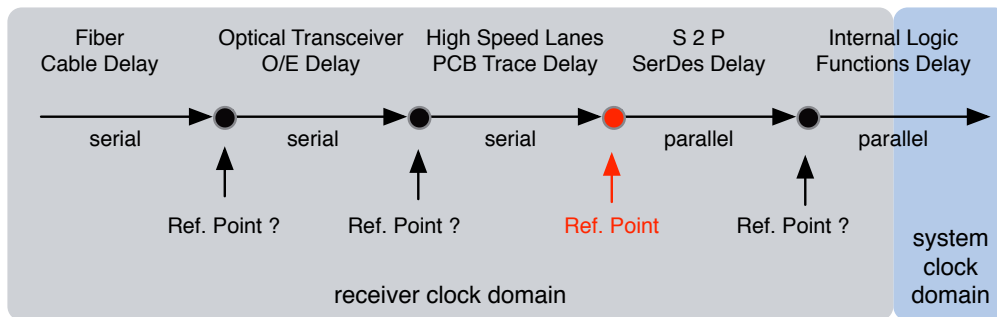


Figure 3.13: Reference points for delay measurement for a generic serial receiver suited for RP3-01/CPRI/ORI interfaces.

The reference delay measurement point should be thus clearly defined and positioned. The most commonly used placement is the *Cable + O/E\_Conversion + PCB\_Trace\_Delay + SerDes\_Input\_Buffer\_Delay*, however it was not clearly stated in RP3 v.4.1 specification and before, leading thus to an interoperability issue affecting the reliability of the measurements.

- RTT measurement accuracy requirements:
  - Need for compensation of variable delays

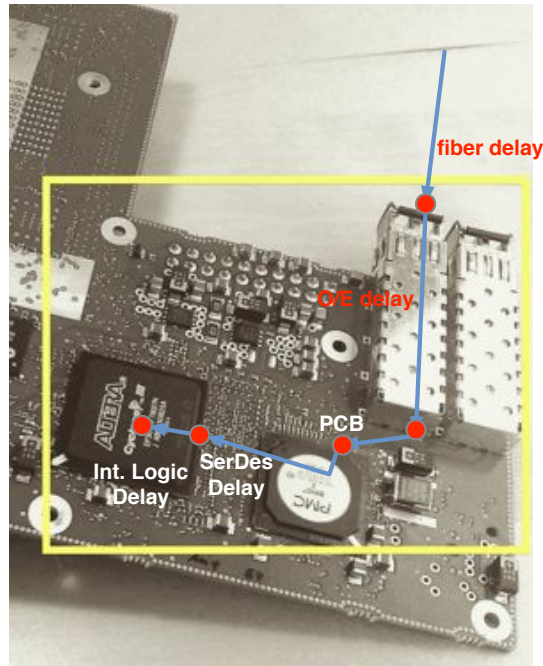


Figure 3.14: Reference points for delay measurement of a receiver for the Radiocomp HSDU RRH Hardware card.

- Variable delays are caused by phase compensation and in some cases bit/byte word alignment within an ASIC or FPGA.
- Variable delay could be different in the RX and TX path
- If strict accuracy requirements are defined, the variable delays needs to be measured and compensated both in the RTT measurement request and reply message.
- Due to the fact that variable delay could be different between TX and RX paths there must be some slack in the measurement accuracy requirements. Now the media delay is divided in two in-order to calculate one way delay. In that case the difference in TX & RX delay is equally divided in to the one way delay.

The proposed methodology for addressing interoperability was to work closely with the OBSAI Forum and RP3 Technical Work Group to improve the RP3 standard specification as well to complement it with an extension of RP3 document with guidelines for interface utilization depending on the application.

Section 3.3.2 presents the methodology and the work initiated from the Author together with the participants of the OBSAI RP3-01 Air-Interface Profile Project [6] contributing in reducing interoperability efforts related to the first three bullets above applied to RP3-01 interfaces. Complementary work regarding interoperability of OBSAI RP3 interface can be found in [60].

#### 3.3.2 Methodology for Interoperability

The selected methodology for solving the interoperability problems identified by section 3.3.1 is the definition of an interface configuration profile according to the wireless standard in use. The OBSAI Air-Interface Profile project was initiated from the Author within the OBSAI Technical Work Group (TWG) with the scope of enabling multi-vendor interoperability of equipments solving specific issues related to specification interpretation and interface configuration. The profile concept was inspired from the WiMAX Forum where they complemented the massive IEEE 802.16d/e specification with a system profile document selecting only a limited sub-set of essential and optional features as reference to be supported by third party vendors in commercialized equipments. The project team lead by the Author and the group was formed from 20 professionals coming from both OEM and module vendors. The project has been submitted for approval to the OBSAI Forum committee and published in 2009.

The profile activity applies to RP3-01 interfaces providing guidance and definitions for Air-Interface related and/or Vendor Specific related definitions and at the same time guaranteeing backward compatibility. The work is documented in [6]. The adoption of Air-Interface profile features will leverage interoperability between OBSAI Forum members, while the adoption of Vendor Specific profiles will leverage interoperability with a specific vendors. Whenever it is not explicitly stated, a specific air-interface profile feature is also valid as vendor specific feature. Adoption of the recommended air-interface profile features for specific applications and configuration it is optional and RP3 specifications remains the main reference.

#### 3.3.3 Results on Interoperability Enhancement Study

The profile document describes a sub-set of recommended RP3-01 interface configuration and functionalities on a layer-by-layer base taken from [57, 5]. The main scope of the profile is to easier integration between the Base Band Modules(s) (BBM) / Local Converter (LC) and RRH unit coming from between different vendors. The main areas subject of the review and definition work have been on:

##### Physical Layer

At physical layer the Author identified and presented an issue with link delay measurements to the profile project, and the conclusion was that such issues were subject for discussion and inclusion rather into the RP3 specification [5] and not into profile document [6].

The RP3 specification v.4.1 did not clearly state reference measurement points for RTT

### 3.3. Study on Protocol Interoperability

and compensation methods applying to both LC and RRH and affecting the following delay components (See Fig. 3.12):

- $\Delta \text{RTT} = T - \Delta_{1,2}$
- $\Delta_{1,2}$
- $\Delta_{1,3} / \Delta_{3,2}$  etc.

Interoperability and system performance between multiple module vendors require the same reference measurement point on both ends else an error inaccuracy in the measurement will be introduced. In RTT measurement procedure [5] only delays over the fiber can be approximated as symmetrical in DL/UL, and this approximation is valid only if the measurement point are placed at input/output ports (optical or electrical) and local compensation is made on both  $\Delta_{1,2}$  and  $T$  measurements for both DL and UL internal delays including SerDes + PCS + internal logic, since they are not always symmetrical in DL/UL depending on implementations. Different placement of measurement points in LU/RRH module from different vendors will be cause of measurement errors. The  $\Delta \text{RTT}$  link delay budget is illustrated as in Fig.3.15 :

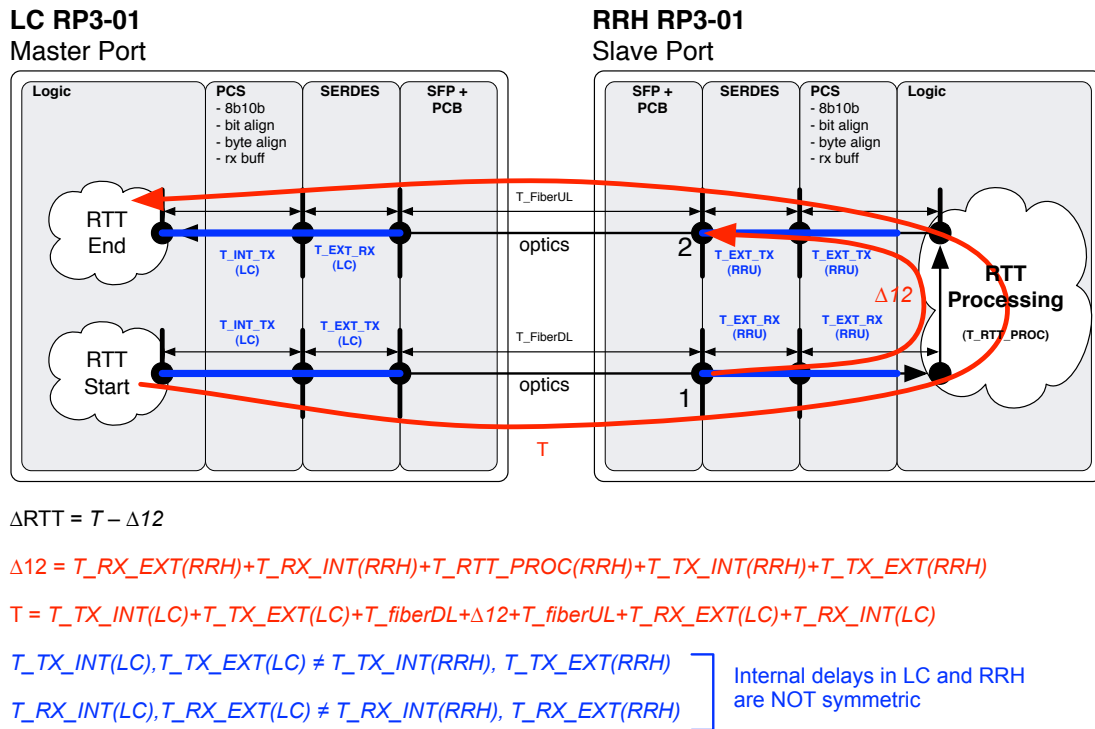


Figure 3.15: Illustration of the Round Trip Time (RTT) Measurement Concept in RP3-01 interface.

### 3.3. Study on Protocol Interoperability

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The Author's proposal to the RP3 TWG was concerning the correct placement of reference measurement points shall be defined unambiguously in [5]. Specifically, the measurement reference points shall have been defined at the input / output serial ports (electrical) of the physical layer serializer block (transceiver), as normally the serializer receiver and transmitted delay from serial to parallel is specified from the component vendor and the value can be used in the delay compensation function, while it is very challenging measuring the delay over PCB traces and optical transceivers. This definition however implies that Fiber and SFP (O/E and E/O conversion) are assumed to be symmetrical and may be considered part of propagation delay and since PCB traces delay may be different in DL/UL and in LU/RRH the general recommendation is for symmetric high-speed PCB traces designs and compensation of  $T$  (on LU side) and  $\Delta_{1,2}$  (on RRH side) shall be defined accounting for:

- $T_{RX\_INT}$  (PCS+logic) and  $T_{RX\_EXT}$ (SerDes)
- $T_{TX\_INT}$  (PCS+logic) and  $T_{TX\_EXT}$ (SerDes)

On top of that, it was suggested that a multi-node RTT procedure shall have been defined in [5]. The Author's contribution to the [5] in Section 6.2.6 has been the addition of the following wording:

*The reference point for the measurement shall be defined at the physical layer input / output electrical ports of the serial link (SerDes). These reference points shall apply to RRH internal delay measurements (Section 6.2.6.1) as well as to LU and RRH RTT measurements (Section 6.2.6.2).[5]*

The Author's contribution to the [5] in Section 6.2.6.2 has been the addition of the following wording:

*In the  $\Delta_{RTT}$  time calculation, the SerDes and PCS/Internal logic delays in both DL and UL paths shall be compensated in the measured  $\Delta_{RTT}$  and  $\Delta_{12}$  values. In particular, at the LC (Local Converter) physical layer the internal logic / PCS / SerDes delays in both DL and UL paths between the reference measurement point as defined in Section 6.2.6 and the internal measurement point shall be removed from the measured  $\Delta_{RTT}$  value. At the RRH node physical layer, the internal logic / PCS / SerDes delays in both their DL and UL paths between the reference measurement point as defined in Section 6.2.6 and the internal measurement point shall be included in the measured  $\Delta_{12}$  value that will be reported into the RTT message reply. The method described above accounts for situations in which the internal delays (internal logic/PCS/SerDes) may not be approximated as symmetrical in their DL / UL components. In a RP3-01 optical link, the delay of O/E and E/O conversion and PCB differential traces may be accounted*

### 3.3. Study on Protocol Interoperability

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*as propagation delay and included in the  $\Delta_{RTT}$  budget. This is an approximation assuming a fixed and symmetrical DL/UL delay contribution from the E/O and O/E conversion module and PCB traces provided they are having the same length [5].*

This improved wording has been accepted and approved from the OBSAI TWG and Steering Committee for inclusion and incorporation in the latest RP3 Specification v.4.2 [5], which also then included the requested RTT Multi-hop procedure definition. In Section 4.4 a generic physical receiver layer architecture will be presented.

#### **Data Link Layer**

No major issues was found at data link layer affecting interoperability. The RP3 framing structure defined by M\_MG = 21, N\_MG = 1920, K\_MG = 1 parameters have been defined for all included wireless standards already in [5] to ensure the same frame structure will apply. The only parameter that received attention is the MAX\_OFFSET, that has been assigned being a programmable value depending on the line rate (i parameter) in use.

#### **Transport Layer**

At this layer the major contribution was to isolate the features according to a module's applicability. The RP3 specification includes in fact a number of functionality that are module dependent, but the Message Multiplexer and Demultiplexer as well as Summing unit functionalities have been isolated in the base station side of the interface only and explicitly mentioned that they do not apply in RRH modules.

#### **Application layer**

At this layer a number of areas have been identified as subject of attention as in Fig.3.16:

- Usage of transmission rules for Downlink (DL) and Uplink (UL) paths.
- Definition of mandatory and accessory RP3 Message TYPE fields.
- Time stamp field alignment.
- Samples mapping as in Fig.3.17.
- Synchronization configuration



### 3.3. Study on Protocol Interoperability

Item		Parameter Value(s)		Applicability
1	Air-Interfaces	802.16 WiMAX		Based on application
		WCDMA-FDD		
		LTE		
		GSM / EDGE		
2	Message transmission rules Dual Bit Map	WCDMA-FDD	DL	Optional
			UL	Not required
		WCDMA-FDD	DL	Not required
			UL	Not required
		LTE	DL	Required only for 15 MHz
			UL	Not required
		GSM / EDGE	DL	Not required
			UL	Required
3	RP3 Type field	WCDMA-FDD		Based on application
		802.16		
		LTE		Required
		GSM/EDGE		
		RP3 Generic Type		
		Measurement		
		Control		
		Ethernet		
		FCB		
		Virtual HW Reset		
RTT				
4	Timestamp field	The time-stamp start position 0 is aligned with the air-interface boundary		Required

Figure 3.16: OBSAI RP3-01 Air-Interface profile application layer parameters of relevance for interoperability.

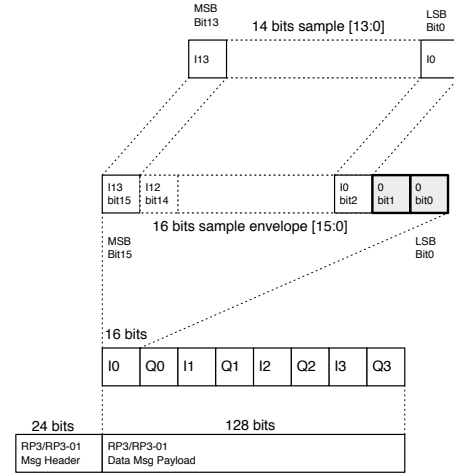


Figure 3.17: Illustration of LTE / 802.16 14-bits IQ Sample Payload Mapping rule in 16-bits sample envelope.

As shown in Fig.3.17 in standards other than WCDMA where the envelope size of the sample (16 bits) is not fully utilized by the actual sample value (may be due to lower resolution requirements of the signal sample in use) the MSB of each sample shall be aligned with the MSB bit position of the sample envelope. All unused bit positions in the LSB part of the envelope shall be set with zeroes ('0's). One advantage of the alignment to MSB is that the overall digital power signal level will be maintained in the system and the resolution may be increased by treating the LSBs as valid bits. DL and UL links may have different independent sample sizes. In terms of RP1 synchronization, the profile contribution has been to specify only a selected number of supported FCB types.

Interoperability has been studied at the protocol level between third party equipments. An interface profile definition and specification enhancement approach was selected for selected air-interface standards to reduce the amount of critical areas during the interface implementation and configuration. The physical layer definitions in [5] for the reference measurement points have been subject of review and clarification. The transport and the application layers have been enhanced with a details on the required module configuration removing multiple options and defining data mapping and synchronization configuration for specific air-interface related applications.

### 3.3. Study on Protocol Interoperability

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#### Summary

The Author's contributions to improve interoperability for OBSAI RP3-01 interfaces are incorporated in [6] and the personal contributions summarized in Table 3.5 as below:

Item	Contribution
Interface Profile	Document describing each layers' configuration.
$\Delta_{1,2}$	Correct placement definition at the electrical I/O of SerDes IC.
$\Delta_{1,3}$	Correct placement definition at the electrical I/O of SerDes IC.
$\Delta_{3,2}$	Correct placement definition at the electrical I/O of SerDes IC.
$\Delta_{RTT}$	Detailed RTT procedure definition.
Application Layer	Configuration of timing and mapping of smaller samples.

Table 3.5: Summary of contributions toward RP3-01 interface interoperability.

## 3.4 Interface Start-up Sequencing

The discussions in this section are based on the work done from the Author and presented in the following publications:

- C. Lanzani, *Base Station Management Procedures for OBSAI RP3-01 and CPRI Interfaces*. Radiocomp ApS, [www.radiocomp.com](http://www.radiocomp.com), January 2010 [10] where the personal contribution of each is the entire base station interface synchronization procedure.
- C. Lanzani and et al, *OBSAI RP3-01 IP Core User Manual*. Radiocomp, [www.radiocomp.com](http://www.radiocomp.com), v.2.0 ed., August 2010 [12] where the personal contribution is the system architecture and functional requirements.
- C. Lanzani and et al., *CPRI v.4.1 IP Core User Manual*. Radiocomp, [www.radiocomp.com](http://www.radiocomp.com), v.2.3 ed., September 2010 [12] where the personal contribution is the system architecture and functional requirements.

This section addresses an important issue discovered from the Author in the OBSAI RP3-01 standard definition during the eNB start-up procedure when link delay is measured and calibrated and resulting into an inaccuracy introduced in the delay link budget. In order to ensure deterministic measurements the delay performance between each start up of the system, normally the eNB module software management layer is required to execute a start up sequence cycling through different synchronization states until delay is measured and calibrated and interface is correctly synchronized at both BBM and RRH ends. This section gives a brief overview on eNB system architecture and synchronization, identifying a start-up sequence problem and analyzing its impact on the system. Finally, it provides a correction of the start-up sequence enabling correct operations.

### 3.4.1 System Synchronization Overview

This section describes the interface between a wireless base station (eNB) and remote radio unit (RRH) module for LTE (3GPP-R8) standard and beyond. In particular it focuses on the Local Converter (LC) and RRH configurations and management showing data, timing and control paths. Later the section focuses on the link start-up procedure illustrating the system-start up sequence and procedure to measure the data path delay. The start-up sequence subject is beyond the content of the interface standard specifications and it is worth analyzing in this thesis. Fig.3.18 a two-sector generic eNB architecture based on OBSAI definitions and consisting of six main modules. This architecture may fit well conceptually to CPRI based as well.

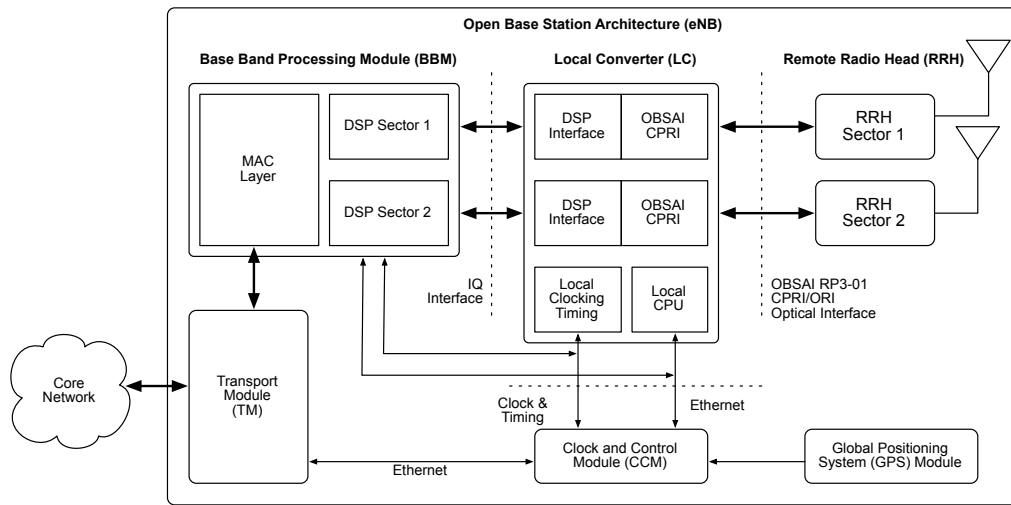


Figure 3.18: Generic and open eNB modular architecture illustrating the major blocks and interfaces. The intelligence is located in the CCM that is the major block responsible for eNB administration and synchronization. It controls and synchronizes the BBM, LC and indirectly the RRH modules through the interface. It is interconnected to GPS modules normally for a global timing reference and alternatively it synchronizes to the core network via the TM.

The principal internal modules are:

- Transport Module (TM)
- Base Band Processing Module (BBM)
- Clock and Control Module (CCM)
- General Purpose Module (GPS)
- Local Unit (LU)
- Remote Radio Unit (RRH)

### 3.4. Interface Start-up Sequencing

The software intercommunications between the different eNB modules is illustrated below in Fig.3.19 where the central control is located in the CCM which is responsible to handle the start-up during the system configuration.

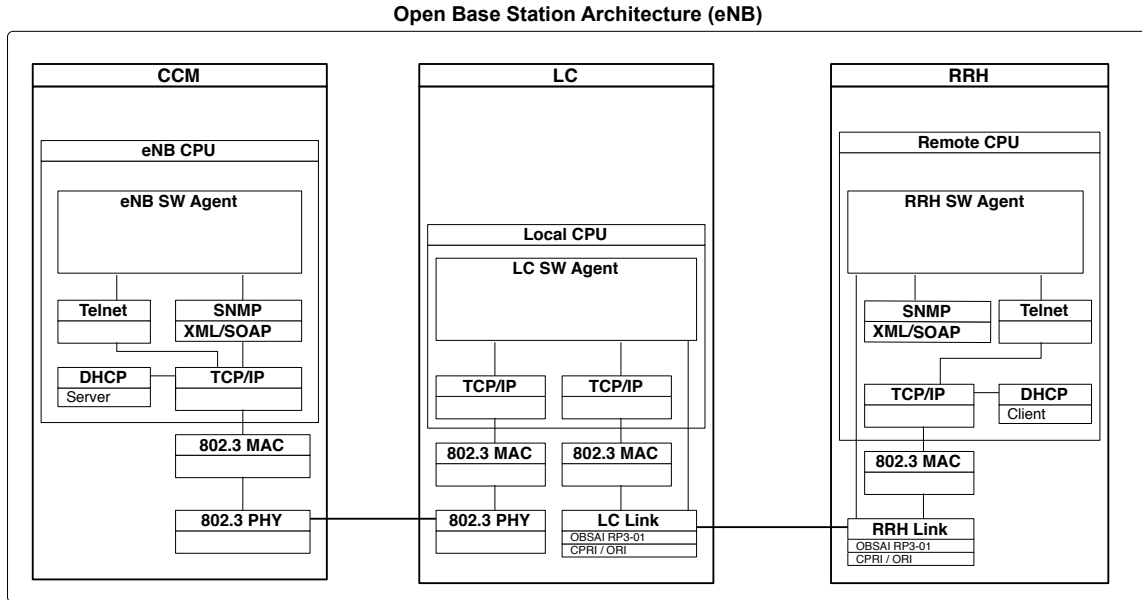


Figure 3.19: Example of common software protocol communications between internal eNB modules. The CCM host the BS SW agent module which via SNMP / XML / SOAP messaging protocols is controlling the LC and the remote RRH agent. Underlying transport is TCP / IP based on Ethernet.

The general internal software architecture of the RRH module is shown below in Fig.3.20 where the CCM controls the different modules, including the LU and RRH using the Ethernet O&M messaging channel:

### 3.4. Interface Start-up Sequencing

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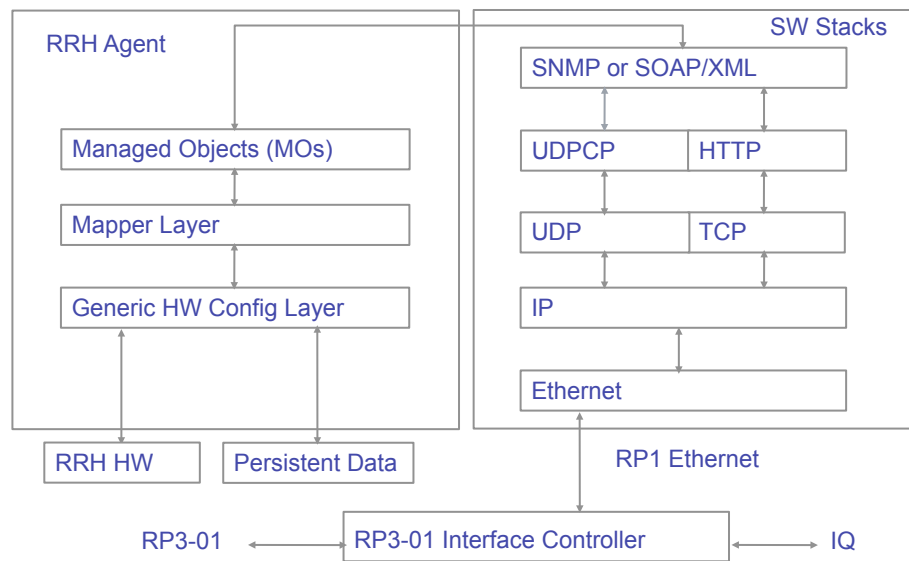


Figure 3.20: Example of detailed software architecture in a remote radio head unit showing the software protocol stack and communication flows from interface to the hardware.

At the RRH node, the RP1 Ethernet configuration and status messages are extracted from the interface controller and processor by a local CPU that is parsing the content against the Generic HW Config Layer controlling the HW and persistent module data. Fig.3.21 and Fig.3.22 illustrate the basic system architecture for OBSAI base stations made of the base band and the remote radio modules.

### 3.4. Interface Start-up Sequencing

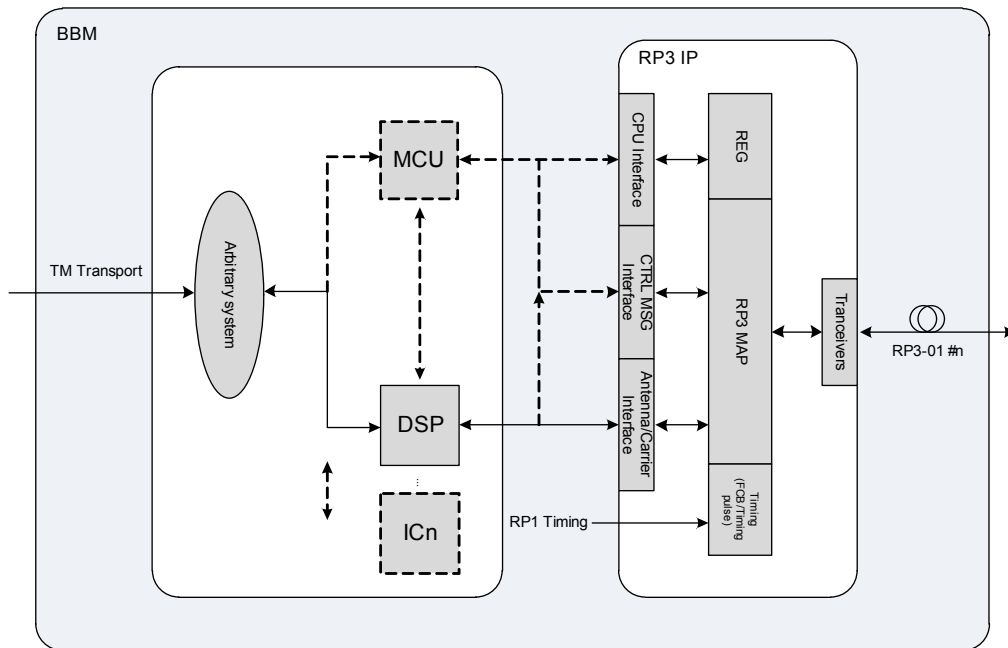


Figure 3.21: Conceptual BBM internal synchronization architecture showing data path, control path with MCU.

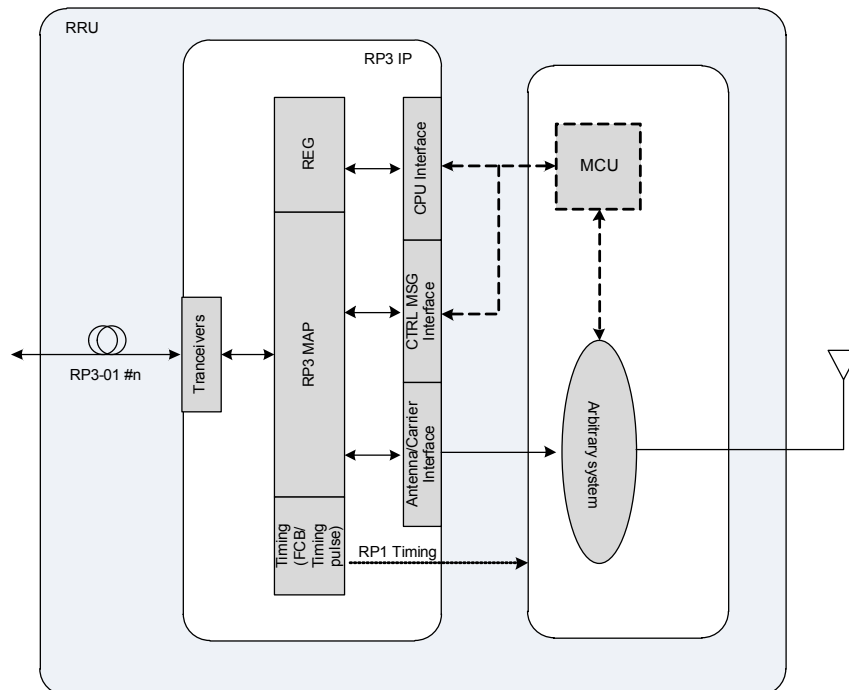


Figure 3.22: Conceptual RRH internal synchronization architecture showing data path, control path with MCU.

### 3.4. Interface Start-up Sequencing

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The figures are conceptual since the system architecture illustrates the main functional entities within a system that is using RP3-01 interfaces. The interfaces may also easily be utilized in parallel, serial and also within the units, in order to achieve an optimized system architecture. These including Micro Controlling Unit (MCU) and with one or more Integrated Circuits (ICs) DSP interfacing to a RP3/RP3-01 Intellectual Property (IP) core), RP3-01 Mapping and RP1 Timing interfaces and CPU interface.

#### 3.4.2 Start-Up Sequencing and Delay Measurements

This section addresses an important issue discovered by the Author that is not clearly defined/addressed in either OBSAI RP1/RP3 [57, 5] specifications and affects the RTT procedure and delay measurement accuracy during the system initialization phase. The system start-up sequence has been divided into three main stages:

- OFF State
- INIT State (Link initialization state)
- SYNC State

where, the INIT State has an internal sub-state structure. If synchronization is lost for any reason, the procedure shall be repeated to ensure correct timing alignment. The system link start sequence for a RP3-01 link between LU and RRH module is illustrated below in Fig.3.23:

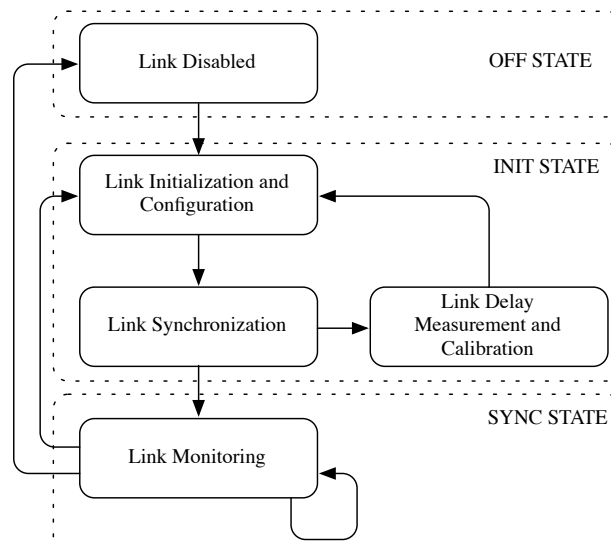


Figure 3.23: RP3-01 Link Start-up FSM sequence phases.



### 3.4. Interface Start-up Sequencing

The entire Finite State Machine (FSM) states are described in more details in Appendix D. We focus in this section on the INIT state in the transition from the *Link Delay Measurement and Calibration* phase to the *Link Initialization and Configuration* phase.

Actual data transmission over the link will be initiated in SYNC state only after all the measurement and calibration operations of the INIT state. It is also important that frame timing and IQ timing are separate aspects and their alignment shall be handled from the CCM independently before actual interface transmission is initiated.

The block diagram of a serial to parallel physical layer receiver chain is shown in Fig.3.24 for reference:

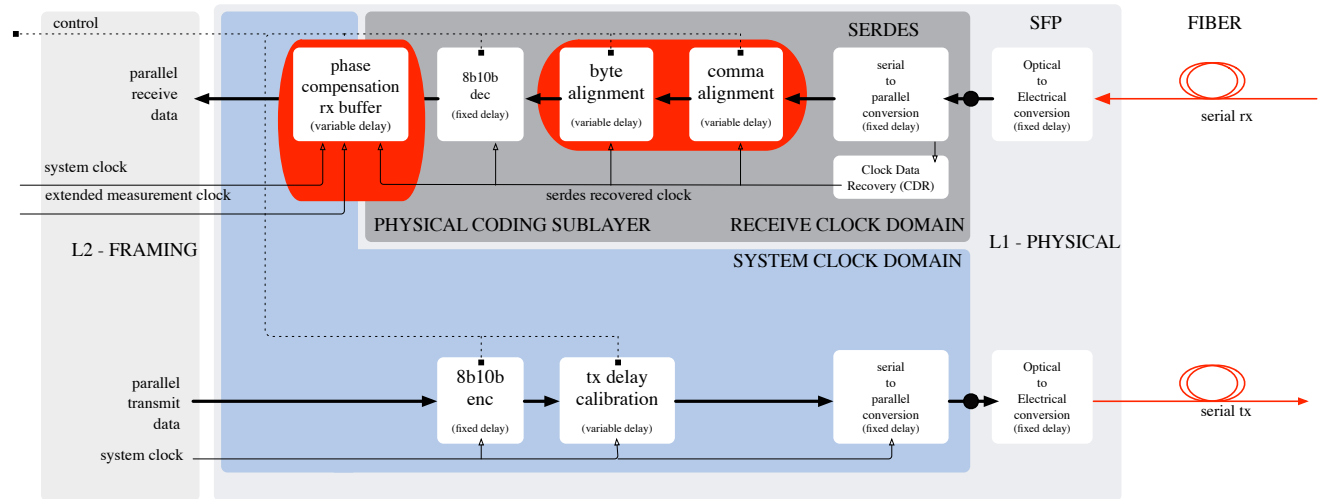


Figure 3.24: Block diagram architecture of a serial to parallel physical layer receiver chain. It shows in red the critical blocks with variable latency that requires advanced delay measurement features like bit and byte alignment, receive buffer and cross clock domain.

### 3.4. Interface Start-up Sequencing

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The variable delays in the interface receiver that will change every time the link is passing from OFF to IDLE or SYNC state are:

- Bit pattern alignment delay. This delay is the time that will take to the alignment block to discover the 10 bits K28.7/K28.5 pattern. It can vary between 0 and 9 line rate bit periods depending on the positioning of the first arrival bit.
- Byte pattern alignment delay. This delay is the time that it takes to align the K28.7/K28.5 characters to byte position 0 in the byte position 0 of the 32-bits data path. It can vary between 0 and 3 system clocks byte periods at 1/40 of the line rate.
- Receiver Buffer level indicated by the difference between the write and read pointers in the buffer.
- Phase difference between recovered clock and system clock (worst case of 1 byte clock period).

The formula to calculate the data alignment delay is shown in Eq.3.4:

$$AlignDelay_{Max} = BitAlign_{Delay} + ByteAlign_{Delay} \quad (3.4)$$

where:

$$BitAlign_{Delay} = [0..9bits] * Bit\_Line\_Rate\_Clk\_Period(ps) \quad (3.5)$$

$$Bit\_Line\_Rate\_Clk\_Period = \frac{1}{LineRate(MHz)} \quad (3.6)$$

$$ByteAlign_{Delay} = [0..3bytes] * Byte\_Clk\_Period \quad (3.7)$$

$$Byte\_Clk\_Period = \frac{1}{\frac{Line\_Rate(MHz)}{Data\_Path\_Size(bits)}} \quad (3.8)$$

As an example - assuming a 3,072 Gbps line rate and a 40 bits data path - in evaluating the alignment delays we have the following values out of Eq.3.6 and Eq.3.8:

$$Bit\_Line\_Rate\_Clk\_Period = \frac{1}{3072MHz} = 325.5ps$$

$$Byte\_Clk\_Period = \frac{1}{\frac{3072MHz}{40bits}} = 13,02ns$$

### 3.4. Interface Start-up Sequencing

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If we insert the calculated *Bit\_Line\_Rate\_Clk\_Period* and *Byte\_Clk\_Period* values in Eq.3.5 and Eq.3.7 - assuming a worst case delay of 9 bits for bit alignment and 3 bytes for byte alignment - we get:

$$BitAlign_{Delay} = \pm 9bits * 325.5ps/bit = \pm 2.92ns \quad (3.9)$$

$$ByteAlign_{Delay} = \pm 3bytes * 13.02ns/byte = \pm 39.06ns \quad (3.10)$$

Substituting these values in Eq. 3.4 we get:

$$AlignDelay_{Max} = BitAlign_{Delay} + ByteAlign_{Delay} = \pm(2.92ns + 39.06ns) = \pm 41.98ns \quad (3.11)$$

When comparing this inaccuracy with the RP3 requirements of  $\frac{1}{614.4MHz} = \pm 1.627ns$  [5] or the CPRI requirement R-19 of  $\pm 8.16ns$  [24] it is evident the requirements violation even for a single hop. This inaccuracy may be introduced at each hop at the receiver, resulting in a potential and much larger link delay budget inaccuracy that shall be avoided.

The buffer level and clock phase difference can be measured with a number of techniques and this topic will be addressed in section 4.4. The importance of a correct initialization phase will help avoid an inaccurate delay measurement if the bit and byte alignment delays as well as receive buffering level and clock phase will change during the link delay measurement and link configuration phase. The principle is that the alignment delays and the clock phase difference between recovered clock and system clock at the radio node will not be the same every time the link is passing from the SYNC state to the OFF state and back to the SYNC so when initializing and calibrating the link this transition shall be avoided. A solution is presented in the next section 3.4.3.

#### 3.4.3 A Link Start-Up Sequence with Deterministic Delay

The generic system start-up sequence is presented and the entire state description can be found in Appendix D. The optimal INIT STATE procedure is presented in details in this section. The proposed procedure enables deterministic delay measurements with the RTT procedure as described in [5].

#### Link Configuration and Activation

In this phase, the link is initialized and configured with the default / calculated  $\Delta$  and  $\Pi$  values. When the SFP module is detected, LU will configure the Link(n) with default  $\Delta$  and

### 3.4. Interface Start-up Sequencing

II values. LU will start transmitting idle K28.5 pattern sequence to RRH (TX IDLE FSM). RRH will receive pattern sequence IDLE bytes (RX FSM IDLE) and will start transmitting K28.5 IDLE bytes back (TX FSM IDLE). The idle transmission from both ends is very important for ensuring that clock synchronization is recovered in LU/RRH and that both bit and byte alignment blocks in both eNB and RRH will be in a stable state with deterministic delay conditions. If LU will receive correct K28.5 IDLE bytes back will then move to Link Synchronization sequence otherwise it shall go back to OFF state of no idle bytes are received back after a timeout period. This is shown in Fig.3.25. When going to OFF state, the delay information of alignment blocks are lost and the procedure shall be repeated again.

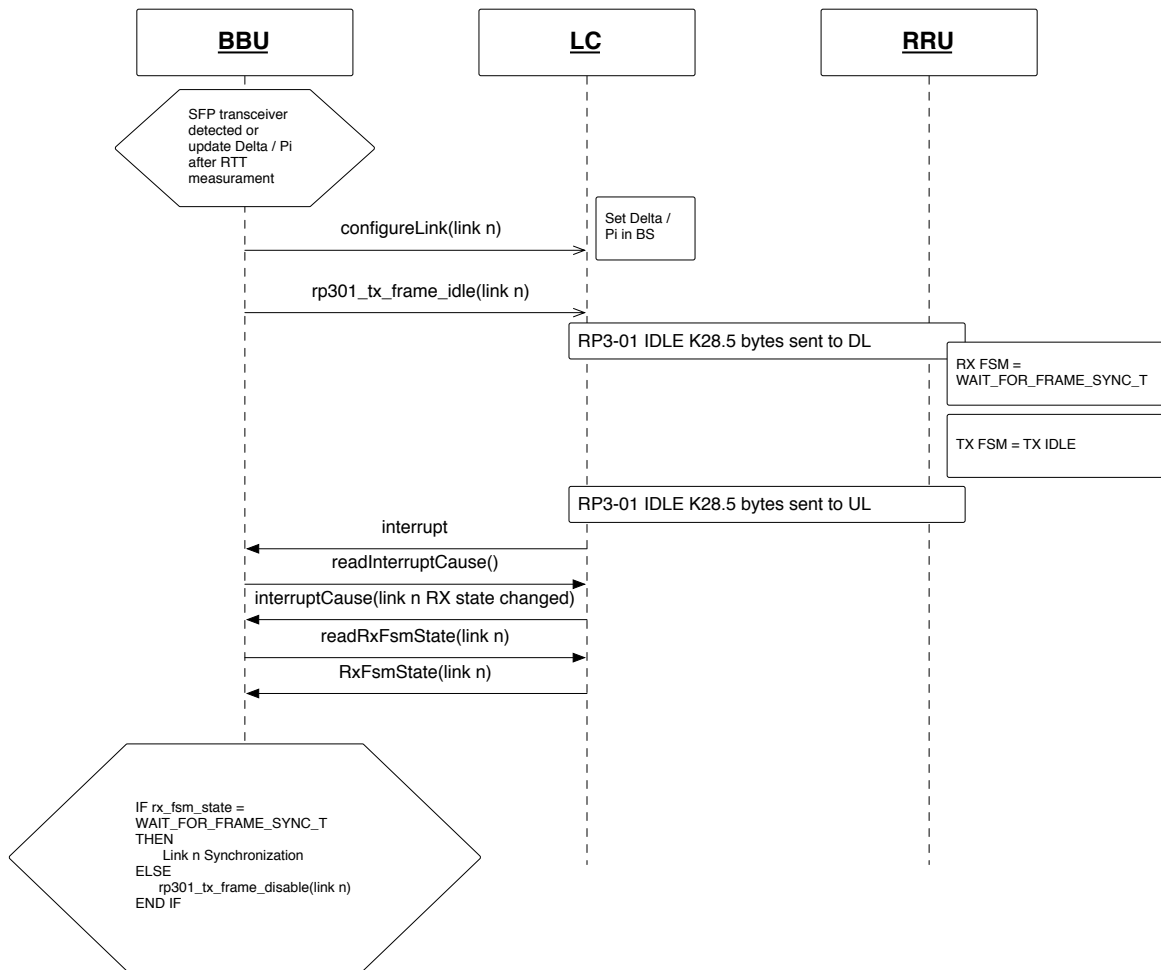


Figure 3.25: Link Configuration and Activation phase.

#### Link Synchronization

If IDLE bytes are received from RRH, then LU will move the RP3-01 TX FSM form IDLE to SYNC STATE. In SYNC state RP3-01 FCBs for RP3 type and air-interface type shall be sent continuously. This is shown in Fig.3.26.

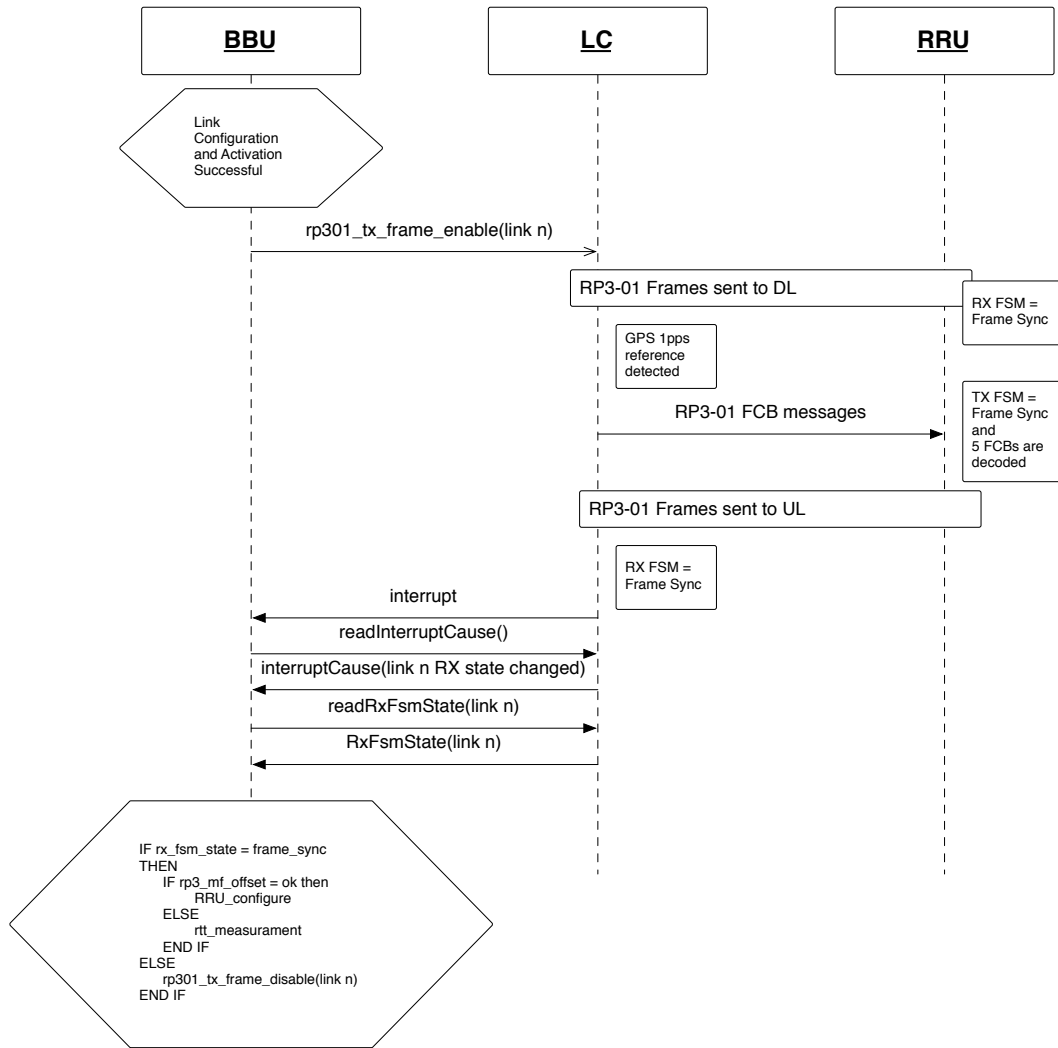


Figure 3.26: Link Synchronization phase.

### 3.4. Interface Start-up Sequencing

If RRH RX FSM is in FRAME SYNC and minimum five (5) FCBs are decoded correctly, then the RRH shall move the TX FSM in TX SYNC STATE accordingly. In this state, both LU and RRH are synchronized and messages can be exchanged. The RTT procedure shall be executed in the "Link Delay Measurement and Calibration" sub-state as described in the next sub-section.

#### Link Delay Measurement and Calibration

When the RP3-01 link is in RX SYNC STATE in both eNB and RRH, the eNB shall initiate a RTT measurement to calculate the fiber delay. The procedure is well described in [5]. OBSAI RP3-01 shall be able to provide the RTT measured value and the application software shall use that value plus the compensation for the local delays to calculate the fiber delay to use in the RRH. The RTT procedure is also used to calculate the correct  $\Delta$  and  $\Pi$  values. This is shown in Fig.3.27.

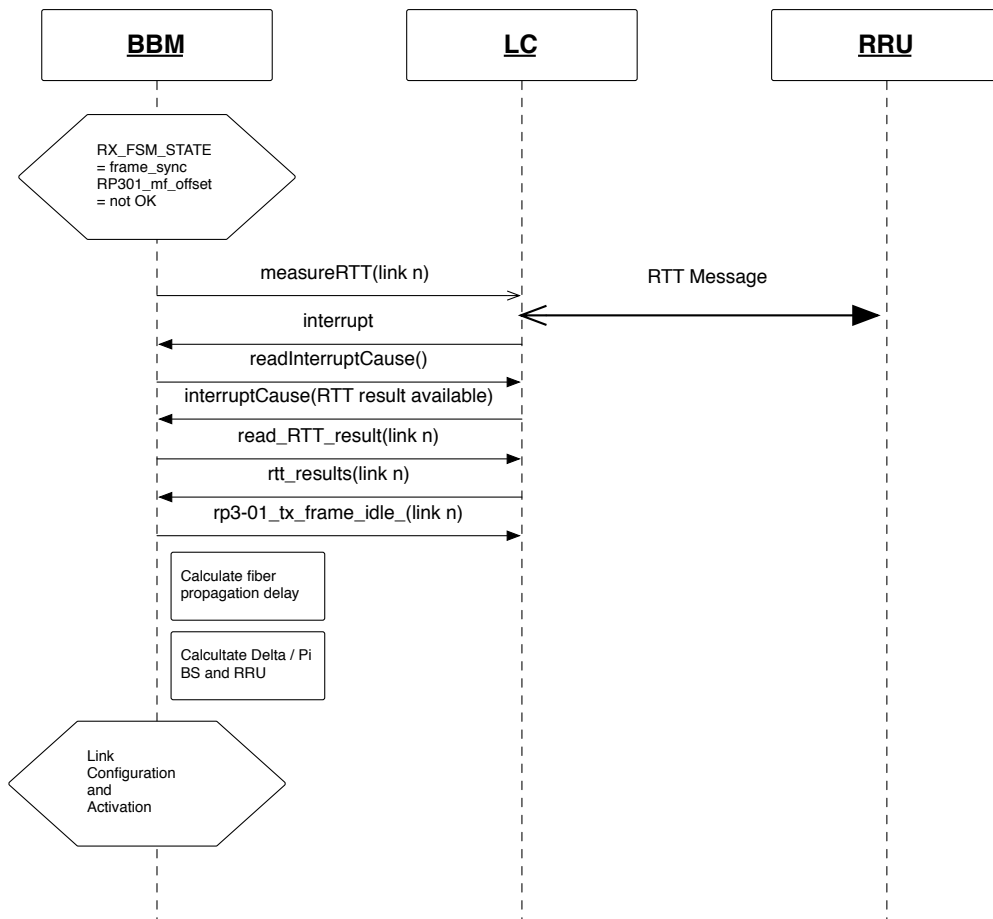


Figure 3.27: Link Delay Measurement and Calibration phase.

This section described an improvement of the link start-up sequence for OBSAI RP3 interface and equally applicable to CPRI interface. The proposed sequence is removing the alignment delay variation between OFF and SYNC state that can during the INIT state before and after the RTT procedure execution. This enables to ensure deterministic delay measurement in compliance with RP3 and CPRI specifications.

## 3.5 Summary

4G networks are going to adopt the distributed and open eNB base station architectural model as foundation of the upcoming radio access systems. The interfaces of most relevance is the one between the base band processing module and the remote radio module based on either CPRI/ORI or OBSAI RP3-01 definitions. The remote nature of the communication introduces a complexity in the interface system for operating synchronously, and the selection of either interface basically dictates if this complexity shall be placed in the base band side (OBSAI RP3-01) or in the radio side (CPRI/ORI).

Based on the analysis made, CPRI/ORI enables slightly higher capacity at the cost of a more complex routing, delay and synchronization management when compared to OBSAI RP3-01. On the other hand it has been identified that OBSAI RP3-01 enables more flexibility with its built-in features at the cost of a slightly lower capacity. In either case, it has been identified that unless serial baud rates will be increased to 12,288 Gbps (current definitions are limited to 6.144 Gbps), the long term IMT-A requirements of delivering up to 100 MHz bandwidth with multi-antenna configuration will not be met unless IQ compression is used or carriers are split into multiple parallel links increasing cost and buffering/synchronization requirements at the RRH. Interoperability between third party vendors for long time has been challenging real implementation due to the lack of a system test specification procedure and lack of dedicated test equipment to validate the base band and RRH module interfaces. The contribution focus has been on enhancing and complementing RP3 standard with the air-interface profile specification along with improvements in the specification itself covering the most relevant configuration aspects for each protocol layer.

As the complexity of an OBSAI RP3-01 implementation resides in the synchronization procedures, an analysis has been made focusing on system start up sequencing in an OBSAI RP3-01. The problem discovered is that an incorrect start-up sequence will lead to non-compliance with the RP3 specification with regards to link delay measurement accuracy. A proposal for an improved start-up sequence has been made to ensure deterministic delay measurements in both DL and UL directions without introducing additional inaccuracies.

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## Chapter 4

# An Advanced Interface Protocol Stack Architecture Design

The discussions in this chapter are based on the work done from the Author and presented in the following publications:

- C. Lanzani, “OBSAI RP3-01 6.144 Gbps Implementation,” in *4th FPGAworld Conference Proceedings 2007* (L. Lindh and V. Mooney, eds.), pp. 10–15, FPGA World, October 2007 [4] where the personal contribution is the entire article.
- C. Lanzani, G. Bergamo, and M. Hoegdal, “Analysis of clock distribution and delay management for IMT-Advanced distributed wireless base station systems,” *Frequenz: Journal of RF-Engineering and Telecommunications*, December 2010 [1] where the personal contribution is the system overview and delay measurement section.
- C. Lanzani, G. Bergamo, and M. Hoegdal, “Analysis of clock distribution and delay measurements for multi-hop remote radio applications,” in *6th Karlsruhe Workshop on Software Radios* (I. . K. I. of Technology Communications Engineering Lab, ed.), (Karlsruhe, Germany), pp. 146–152, March 3/4 2010 [2] where the personal contribution is the system overview and delay measurement section.
- C. Lanzani, *Single and Multi Hop CPRI Interface Applications using Radiocomp’s CPRI v.4.1 IP Core*. Radiocomp ApS, [www.radiocomp.com](http://www.radiocomp.com), v.1.4 ed., May 2009 [11] where the personal contribution is the entire document.
- C. Lanzani and et al, *OBSAI RP3-01 IP Core User Manual*. Radiocomp, [www.radiocomp.com](http://www.radiocomp.com), v.2.0 ed., August 2010 [13] where in both the personal contribution is covering most of the document.
- C. Lanzani and et al., *CPRI v.4.1 IP Core User Manual*. Radiocomp, [www.radiocomp.com](http://www.radiocomp.com), v.2.3 ed., September 2010 [12] where in both the personal contribution is covering most of the document.



### 4.1 Overview of a Generic Interface Architecture

There are several considerations to account for in architecting a fully flexible and future proof digital interface protocol for CPRI or OBSAI RP3-01 interfaces. Using the specification as the reference, it is necessary to identify the division boundary between hardware and software related functionalities for each layer. The functions identified in hardware will be part of the controller engine, and SW related functions will be part of the application module and this is a relevant SDR aspect in relation to software configuration and flexibility of the interface. The key considerations to be accounted for are the following:

- Identification of application space (base band side or radio side or both).
- Performance targets and future envisaged extensions (Line rates, Mapping schemes)
- Identification of common shared functions and protocol specific functions for each layer (Important for architecture definition and final solution logical size).
- Identification of mandatory and optional functions within the interface specification.
- Separation between hardware and software functions (Important for SDR ability of changing interface configurations).
- Target implementation technology (Hi/Low end FPGAs or ASICs) and RTL language of choice.
- Clocking and data path size selection (Key decision).
- Modular configuration requirements (Key decision).
- Testing and interoperability requirements
- Cost targets and availability of Common Off The Shelf (COTS) technology components like serializers, optical modules, FPGAs etc. for the implementation.

The following section 4.2 deals with the state-of-the-art in digital interfaces with regards to available solutions and choices, elaborating on the performances and limitations of such with reference to the considerations made above.

## 4.2 State-of-the-Art Interfaces Implementations

Current implementations of CPRI or RP3-01 are mostly targeting a FPGA-based implementations. The reason is that due to the openness and to the proprietary flavors of eNb environments it is important to keep the flexibility in updating or upgrading base station designs. This is opposed to fixed non-upgradable design and FPGAs provides such updates flexibility. In this section we review the state-of-the art in interface implementations. General considerations are made on data path dimensioning selection.

### 4.2.1 Data Path Dimensioning

The selection of the data path size for the implementation of either CPRI or RP3-01 is a key design decision that will impact the target technology that will host the protocol and consequently on the cost of the implementation and future proof-ness of the solution. Since FPGA technologies have limitations in terms of maximum operating frequency of the logic and on the number of Input / Outputs (I/O) pins, selection of the data path size will affect the maximum line rate achievable within a given technology. Due to the 8b10b channel coding, the clock frequency for a specific line rate is given by Eq.4.1:

$$f_{clk} = \frac{1}{x} * bit\_line\_rate \quad (4.1)$$

where  $x$  is the data path size in bits of encoded data before the 8b10b block. In Table 4.1 we list the most common line rates for both CPRI and RP3-01, including extensions for future rate of 9.8 Gbps for CPRI. For each rate, the clock frequency is calculated with Eq.4.1 assuming 8b10b coding scheme with either  $x = 10$  for 10 bits data path (8 bits decoded) or  $x = 20$  for 20 bits data path (16 bits decoded) sizes. These sizes are the common choices available by existing reference design implementations from Xilinx [61] and Lattice [62].

Rate (Mbps)	10 bits DP clk (MHz)	20 bits DP clk (MHz)
9830 (C)	983	491.52
6144 (CO)	614.4	307.2
4915.2 (C)	491.52	245.76
3072 (CO)	307.2	153.6
2457.6 (C)	245.76	122.88
1536 (O)	153.6	76.8
1228.8 (C)	122.88	61.44

Table 4.1: CPRI (C) and OBSAI (O) RP3-01 core clock frequencies for 10-bits and 20-bits encoded data paths implementations respectively using Eq.4.1 for the most common line rates versus the implementation technology from low end FPGAs to ASICs.

As shown in Table 4.1, the limitation imposed by these data path sizes is that they require

## 4.2. State-of-the-Art Interfaces Implementations

fast clocks and high end FPGAs or ASICs to be able to support rates higher than 3,072 Gbps as illustrated in Fig. 4.1 and Figure 4.2:

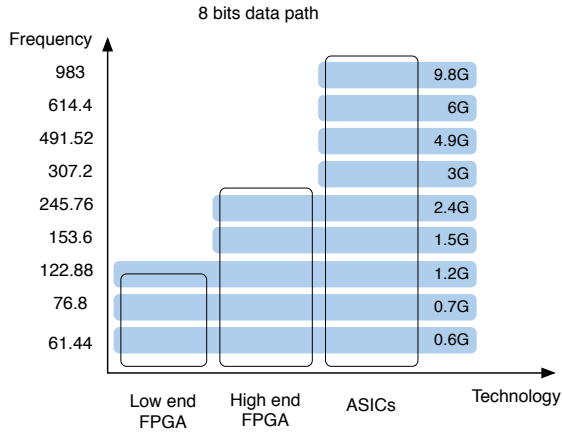


Figure 4.1: 8 bits data path illustration of line rate, clock frequency and RTL technology.

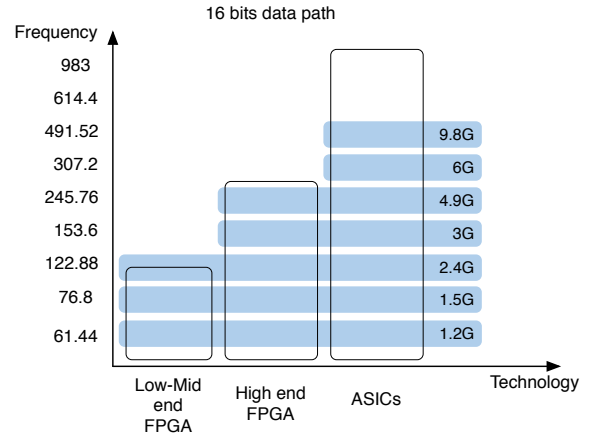


Figure 4.2: 16 bits data path illustration of line rate, clock frequency and RTL technology.

As seen above in Fig.4.1 and Fig.4.1, these data paths requires high-end FPGAs or ASICs to run rates beyond 3.072 Gbps. High end FPGAs are relatively expensive components, and this cost is hard to accommodate for RRH applications. Interface rates at 3 Gbps line rate, which is the most popular rate in 3G due to it's carrier capacity, enables to map up to ten 5 MHz UMTS carriers. 4G carrier capacity demand adds a considerable cost factor into the system. Thus moving to ASICs implementations is desirable for higher line rates than 3 Gbps. On top of that, line rates higher than 4 Gbps, requires that the SFP (Small Form-Factor Pluggable) optical transceivers that are commonly used in optical communications for both telecom and data communication applications are replaced by the latest generation called Enhanced Small Form-Factor Pluggable or SFP+. SFP+ has the same form-factor and supports higher data rates up to 10 Gbps with lower power consumption and less complexity. Furthermore SFP+ is as a lower cost alternative to the 10-Gbps XFP form factor<sup>1</sup>. COTS availability of devices with 10G capability in such compact footprint enabled OBSAI and CPRI serial high speed interfaces to increase their speed up to the physical limitations of SFP+ technology in the 10 Gbps space and hence to support the required capacity growth demanded from IMT-A requirements. On the optical transceiver side, there is a remarkable cost difference between traditional SFP up to 4.25 Gbps and SFP+ up to 10 Gbps. From a cost perspective, 6 Gigabit SerDes (as discrete components) are now comparable to 3G SerDes modules. 10 Gigabit SerDes devices instead for these applications are only part of costly high-end FPGAs.

<sup>1</sup>10 Gigabit Small Form Factor Pluggable - Vendors in the cost-sensitive 10-Gigabit Ethernet (10 GbE) market are making a strong push to standardize SFP+ technology for use in 10 GbE applications and similar as an alternative to the XFP form factor.

## 4.2.2 Functional Block Architecture

### CPRI Implementations

The reference state of the art implementation is the CPRI v.4.0 reference design and is provided from Xilinx as a vehicle for their FPGA sells [61]. There are no other commercially available solution known by the Author for comparing other than Xilinx and Lattice. We will focus on the Xilinx core [61], since the Lattice solution is very basic and compliant to CPRI v.2.1 only. Later, we will compare these solutions to the Radiocomp ApS IPR architecture, which has also been purchased from Altera Corporation as a proof or a reliable and complete solution.

Xilinx's CPRI design is mainly composed by three blocks: GT transceiver, CPRI framer core, Mapping module only for UTRA FDD supporting up to twenty-four (24) UMTS carriers. The core module includes access to C&M consisting of VSS, Ethernet, HDLC via direct interfaces and for the two latter requiring Media Access Control (MAC) engine externally. Access to registers is provided from the management interface. The block diagram of the Xilinx CPRI IP [61] is shown below in Fig.4.3 for reference:

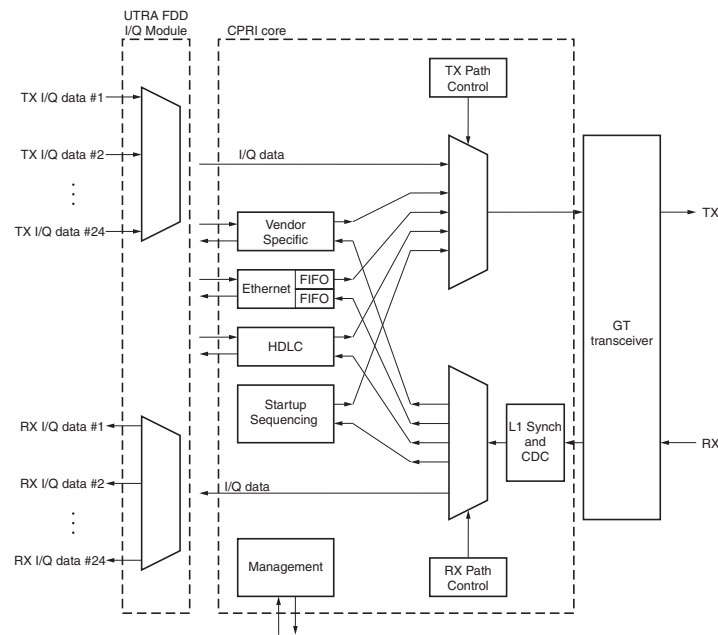


Figure 4.3: Architecture of the Xilinx CPRI IP block [61].

In Fig.4.3 the limitations are that the I/Q module is supporting only UTRA FDD (3G UMTS) and the data-path is made of 20-bits encoded (16 bits unencoded). further more a direct low latency interface for daisy chaining it is not provided.

### OBSAI RP3 Implementations

The same concepts addressed in section 4.2.2 also applies to OBSAI RP3-01 interface cores available on the market from either Xilinx [63] or Lattice. Radiocomp's / Altera's solution provides superior performance and reliability as well as being a fully featured and future proof solution.

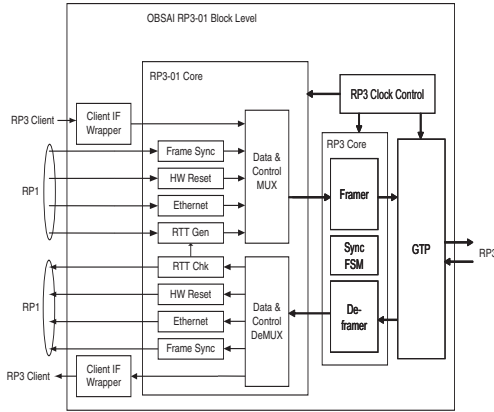


Figure 4.4: Architecture of the OBSAI RP3 v.4.0 Xilinx IP Block [63].

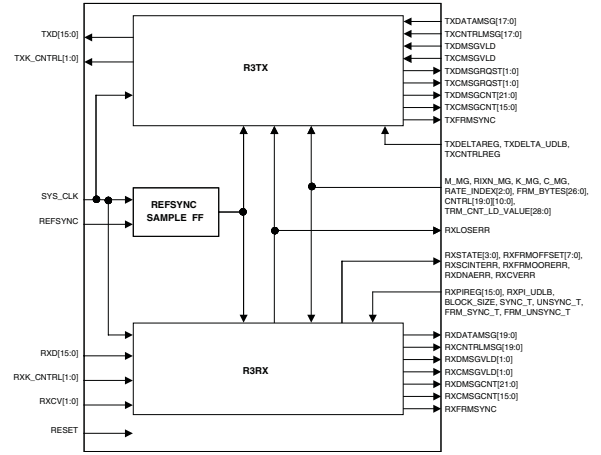


Figure 4.5: Architecture of the Lattice OBSAI IP architecture.

### Limitations and Requirements for Future Proof Interface Design

The main limitations of these implementation from Xilinx and Lattice have been generally identified by the following statements:

- Using 10 or 20 bits data path increase the requirements on the maximum clock tolerated into the system. This means that 6 Gigabit rates or more will require a very expensive FPGA. Increasing the parallelization level shall be considered for supporting high speed line rates with a relatively low clock frequency.
- External MAC blocks for FPGA are normally standard triple speed MACs up to Gigabit Ethernet, which rate is exceeding the bandwidth reserved in the protocol itself for the in-band Ethernet channel and using considerable amount of extra logical resources. A 10/100 Mbps Ethernet MAC would suffice to the Ethernet needs of RP3-01 and Ethernet interfaces.
- The CPRI mapper module supports only UTRA-FDD with limited does not support advanced mapping methods as in [24] for WiMAX, LTE and backward compatible methods. It therefore can be seen only covering a limited subset of the CPRI specification and dedicated mappers shall e built from the user.

- The OBSAI solutions from Xilinx they do not support I&M and Dual Bit Map mapping layer that shall be provided externally. Integrating such layer will result in a self-contained interface solution.
- The solution does not provide a low latency interface for daisy chaining two or more core instances.

## 4.3 An Advanced Interface Controller Architecture

This section will discuss the original contribution made from the Author in architecting an advanced OBSAI RP3-01 and CPRI generic implementation that supersedes the limitations previously described and is today the world's market-leading commercial solution available. The controller architecture is shown in Fig.4.6

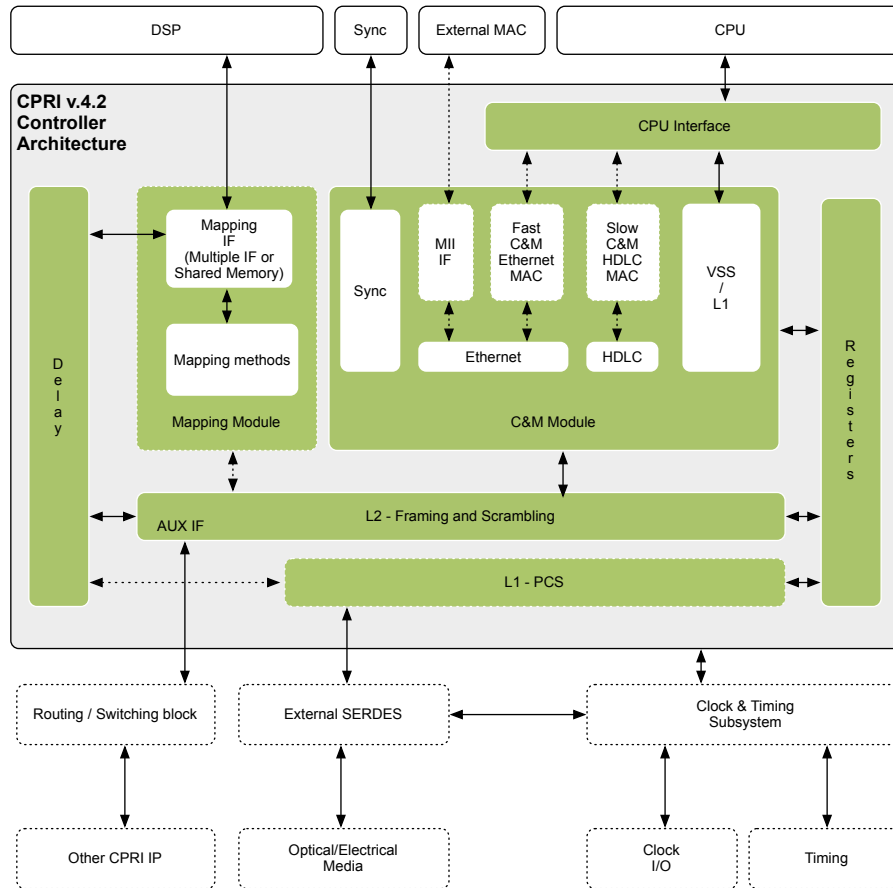


Figure 4.6: CPRI v.4.2 Controller Architecture. The main blocks are L1 PCS that includes 8b10, alignment and buffering, L2 Framing and scrambling, Mapping and C&M Module. The relevant interfaces are the SerDes, Auxiliary, Mapping and CPU interface.

The controller is designed with 40-bits encoded (32-bits unencoded) data path to enable a lower core clock frequency. Functions are partitioned into block according to CPRI standard layer definitions and operations are fully controllable through register interface.

#### 4.3.1 10-Gigabit Line Rates and Beyond

In 2007 the need for higher carrier capacity in radio systems was forecasted. This was due to the introduction of 2x2 MIMO techniques and WiMAX systems with channel bandwidths up to 20 MHz per carrier, as well a need for radio daisy chaining (which extended considerably the bandwidth from the single/dual carrier UMTS systems with 5 MHz of bandwidth). With this in mind, it was clear that interface systems would have to be extended to support rates beyond 3.072 Gbps rates. Based on that, the Author presented studies at the FPGA World Conference in 2007 [4] suggesting an OBSAI RP3-01 6.144 Gbps interface implementation based on existing technology. At that point in time an Altera Stratix2GX FPGA was just released with 6.125 Gbps transceivers and SFP+ beta transceivers from Finisar. In this work the importance of a highly parallelized internal data path at the interface for 6G rates and beyond (10G rates) was stressed. This is described in details in Section 4.3.2 and Section 4.3.3. Note that 6.144 Gbps rates for either RP3-01 and CPRI/ORI interfaces they were standardized later in 2008, so the work addressed in have been anticipating the standardization process [4].

With the introduction of LTE standard requirements into 4G networks since 2009, the bandwidth growth was expected to reach the 10 Gbps threshold, with the first obvious option being 9.8304 Gbps line rates for CPRI/ORI. This intuition was presented by the Author at the IWPC workshop for Flexible Base Stations in 2008 [8]. In this areas the need for a truly open interface was also addressed, including high capacity up to 10 Gbps and open Control & Management definitions. These topics were incorporated today in the ORI standardization initiative as in [26] and [56]. At the time of this writing, similar work is currently ongoing from the Author for demonstrating a laboratory test bed based on Altera Stratix4GT FPGA with integrated transceivers with rates up to 11.5 Gbps.

The CPRI or RP3-01 interface protocols can be integrated in several base band or radio environments and the need for Ethernet and HDLC access needs to fit with existing CPU implementations. The most common configurations are a CPU with either a CPU interface (with data read and write, address bus, chip select) that requires a MAC block - or - a CPU with integrated triple speed MAC with external xMII interface (either RMII, GMII or simply MII). For this reason an interface block shall be flexible enough to fit either into an existing implementation and being optimized in logical resource consumption. For this reason an optimized MAC block for both Ethernet and HDLC shall be considered a part of the interface, and its instan-

tiation shall be programmable at compilation time. Another requirement is a silicon agnostic implementation and therefore the code shall be synthesizable from any synthesis tool either for FPGAs or ASICs. Technology specific blocks like memories and macros shall not directly be part of the code but rather a well-defined interface shall be realized and the selected RTL language was VHDL-83.

The daisy chaining of radio equipment is an operation that would require selected data to be routed from one interface to another in each direction. The routing has to face with timing and alignment configurations, but as well it require a low latency for the transfer as low as 5 us in round trip setup [24]. Since data that are going to be de-mapped are going through buffering for collecting the sample streams, it will not be possible to de-map and re-map data into the next hop due to the higher latency introduced. Therefore it is desirable having a dedicated auxiliary interface for the daisy-chaining that allows to grab data at the receiver of first link after the framer block and route them directly into the frame transmitter of the second link. A bit mask will apply for enabling only specific bits to be written into the transmitter.

#### 4.3.2 A Highly Parallel Data Path Design Proposal

To design with lower cost FPGA technology while maintaining the same serial throughput, the Author chosen for an implementation a higher data-path parallelization to lower the operating core clock frequency.

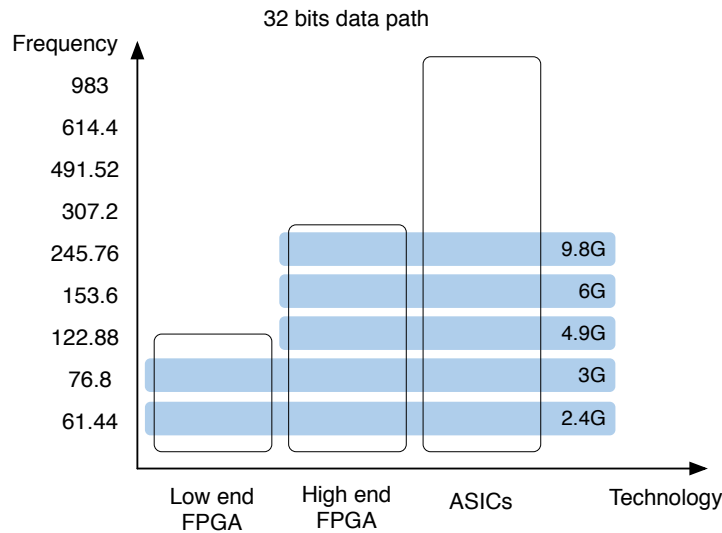


Figure 4.7: 40-bits (32-bits unencoded) data path illustration of line rate, clock frequency and RTL technology.

In this design 32 bits unencoded data-path is chosen, leading for 6.144 Gbps rates to a core



### 4.3. An Advanced Interface Controller Architecture

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frequency of 153.6 MHz frequency that might enable usage of the RP3-01 block also in low-cost FPGA devices. This helps in reducing considerably the overall system cost while benefiting of the increased carrier capacity. In this case an external physical layer SerDes technology it is required (e.g.PMC-Sierra SynthPHY). In addition, as shown in Fig.4.7, the 32-bits data path allows to run higher rates that 6.144 Gbps with clock frequency as low as 245.76 MHz or 307.2 MHz for 9.830 Gbps and 12.288 Gbps respectively which are suited for fast FPGAs or ASICs technologies. The Radiocomp's solution is the High Speed Digital Unit (HSDU) slave radio card as well as Radiocomp's Local Converter (LC) master base band card, and they currently supporting rates up to 3.072 Gbps. Radiocomp's HSDU and Local Converter are shown below in Fig. 4.8 and 4.9 respectively for reference:

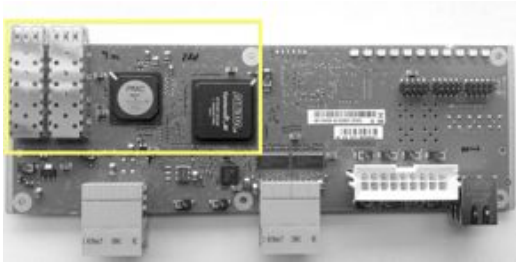


Figure 4.8: Local Converter - Highlighted are shown the SFP transceiver cages, the PMC-Sierra 3.072 BRIC2 SerDes and the low-end Altera Cyclone 3 EPS3C80780 FPGA.

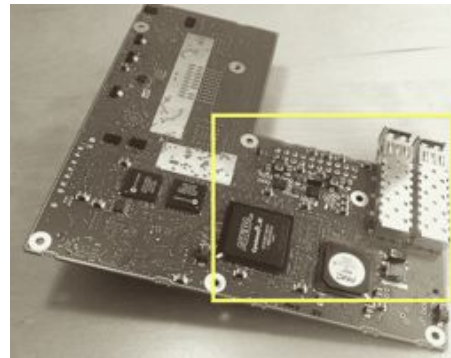


Figure 4.9: High Speed Digital Unit - Highlighted are shown the SFP transceiver cages, the PMC-Sierra 3.072 BRIC2 SerDes and the low-end Altera Cyclone 3 EPS3C80780 FPGA.

### 4.3.3 Measurements Results of 6.144 Gbps RP3-01 Signal

This section summarizes the work made by the Author in [4]. The physical electrical layer is implemented by the Altera Stratix II GX device [64], which combines up to 20 duplex channels capable of operating between 600 Mbps and 6.375 Gbps into a single FPGA. The low power transceivers offer appropriate signal integrity and provide a number of features such as Dynamic Pre-emphasis, Equalization and Adaptive Equalization, which use however have not been required for this test. The transceivers also provide appropriate jitter performance, meaning they comply electrically with the majority of serial standards being used today, including many of the telecom standards including OBSAI RP3-01 and CPRI as shown in the work made from the Author and M. Hoegdal and G. Bergamo in [1, 2] and reported in Appendix E.

For OBSAI RP3/RP3-01 applications, they offer compliance to the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae [65] up to 3.072 Gbps and to the Common Electrical I/O (CEI) [66] for both the Short Reach and Long Reach 6.25 Gbps standards (CEI-6G-SR and CIE-6G-LR), which is a suitable standard recommendations for applications above 3.072 Gbps. The GXB transceiver includes dedicated blocks to support a number physical layer functionalities of many key protocols built inside the transceiver. In the case of OBSAI RP3/RP3-01, the 8b10b encoding and word alignment blocks and synchronization/phase alignment buffers are embedded in the transceiver block and do not need to use dedicated FPGA logic. The relevant GXB transceiver configuration used is as it follows in Table 4.2:

<b>GXB Configuration Parameter</b>	<b>Value</b>
double data mode	true
data rate	6144
protocol	6G basic
equalizer	0
pre-emphasis	0
8b10b enc/dec	cascaded
ref clk	153.6 MHz
rx cru pll	tx clk

Table 4.2: Altera Stratix2 GXB Transceiver configuration for 6.144 Gbps rate

### 4.3. An Advanced Interface Controller Architecture

Dynamic reconfiguration of each transceiver from one operating mode to another is supported. This mode reconfiguration involves reconfiguring of the data rate, data path, or both. For this implementation fixed double-width data-path of 32-bits is chosen and only data rate settings are set being dynamically reconfigurable by the user<sup>2</sup>.

Fig.4.10 shows an eye diagram measurements of 3.072 Gbps and 6.144 Gbps electrical signals on the SIIGXAV<sup>3</sup>. The signal measured consist of valid RP3-01 frame structure<sup>4</sup> with data in every RP3-01 message slot.

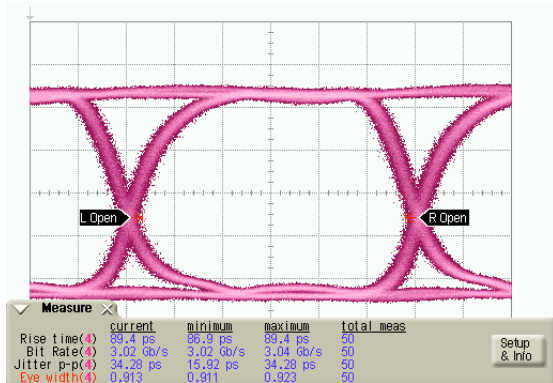


Figure 4.10: 3.072 Gbps RP3-01 electrical signal eye diagram measurement.

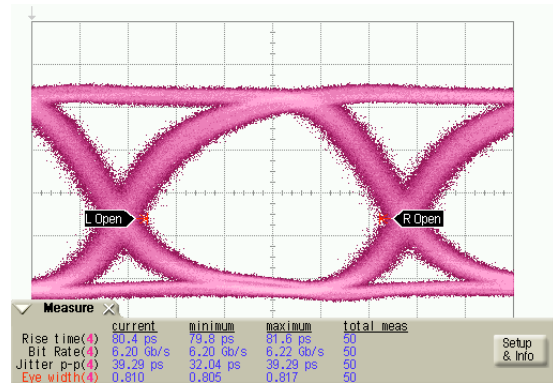


Figure 4.11: 6.144 Gbps RP3-01 electrical signal eye diagram measurement.

These measurements are taken using Agilent 89105 DSO equipment that has been configured with a 153.6 MHz trigger reference synchronized to the transmitted data, which consist of valid RP3-01 data messages. In [5] the values for eye mask compliance relative to the eye width for OBSAI RP3 transmitter / receiver are 0.65 UI / 0.45 UI respectively using 3.072 Gbps rates and they are 0.7 UI / 0.4 UI using 6.144 Gbps rates. The eye diagram measurement at electrical 3.072 Gbps rate shows a peak-to-peak jitter value at 34.28 ps with a eye width value of 0.913 UI. The eye diagram measurement at electrical 6.144 Gbps rate shows a peak-to-peak jitter value at 39.29 ps with a eye width value at 0.810 UI. Both these measurements show mask compliance of the OBSAI RP3/RP3-01 transmitted and received signal.

The test setup block architecture is illustrated in Fig.4.12 where two S2GXAV boards are connected to implement a full duplex optical communication at 6.144 Gbps of valid RP3-01 traffic. The measurements was also performed at 3.072 Gbps for comparing the 6.144 Gbps line rate results to the existing RP3 specifications Setup options for the RP3-01 IP and GXB

<sup>2</sup>In case of dynamic reconfiguration enabled in double-width mode, only the 768 Mbps line rate is not supported from the transceivers since only line rates between 1 Gbps and 6.25 Gbps are allowed.

<sup>3</sup>These measurements are performed with the standard analog pre-emphasis and equalization settings on the ALT2GXB Megawizard tools.

<sup>4</sup>Which includes frame boundary marking characters (K28.7) and Message Group boundary marking characters (K28.5).

### 4.3. An Advanced Interface Controller Architecture

transceivers are done via DIP switches. External clock generator is used to generate 153.6 MHz for both the boards and the trigger signal to the 89105 DSO.

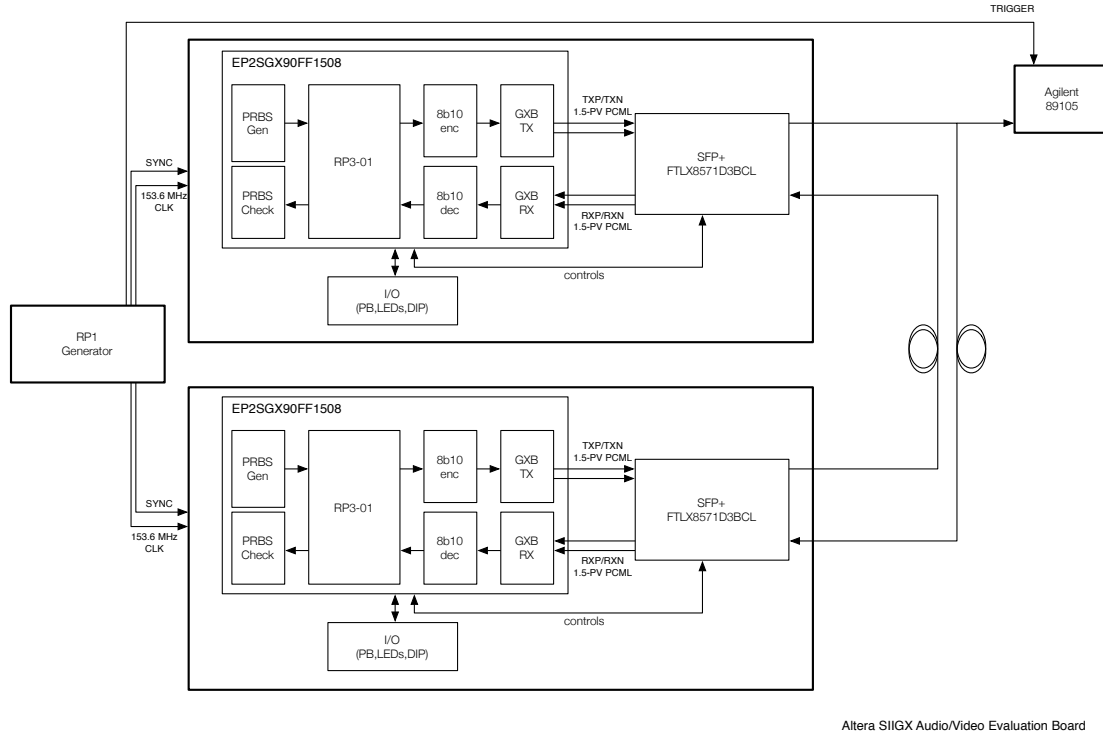


Figure 4.12: Block diagram of the 6.144 Gbps hardware test setup with two Altera S2GX board connected back to back and clocked from a common clock source.

The Pseudo Random Bit Sequence (PRBS) generator blocks implements a simple 3-bytes counter for the RP3-01 message header and a 16-bytes counter for the RP3-01 message payload for each message slot<sup>5</sup> in a Message Group. A PRBS validator checks the received messages counters values and the BER counter measures the amount of bit errors received. The system setup is given in Fig.4.13, where the 7-segments display on each board shows the BER counter values and the LED bank shows that the system is correctly operating according to the mapping in Table 4.3.

The results indicate that the transmission at 6.144 Gbps over each link is error free (BER of zero value is monitored constantly on both receivers) and measured over a time window of a few days and without using any additional bit-level scrambling layer between data link layer and 8b10b coding blocks. It has been possible to verify the correct operational status of the interface through the LED bank status indication that are mapped as indicated in Table 4.3 and they all show “low” logic values as expected.

<sup>5</sup>RP3/RP3-01 message slot size is defined as 19 bytes[5].

### 4.3. An Advanced Interface Controller Architecture

LED	Signal	High	Low
1	TX PLL	unlocked	locked
2	RX PLL	unlocked	locked
3	RP3-01 RX IDLE	false	true
4	RP3-01 RX SYNC	false	true
5	PRBS Errors	present	not present
6	LCV Errors	present	not present
7	RE-SYNC	on	off
8	not used	-	-

Table 4.3: Status LED mapping.

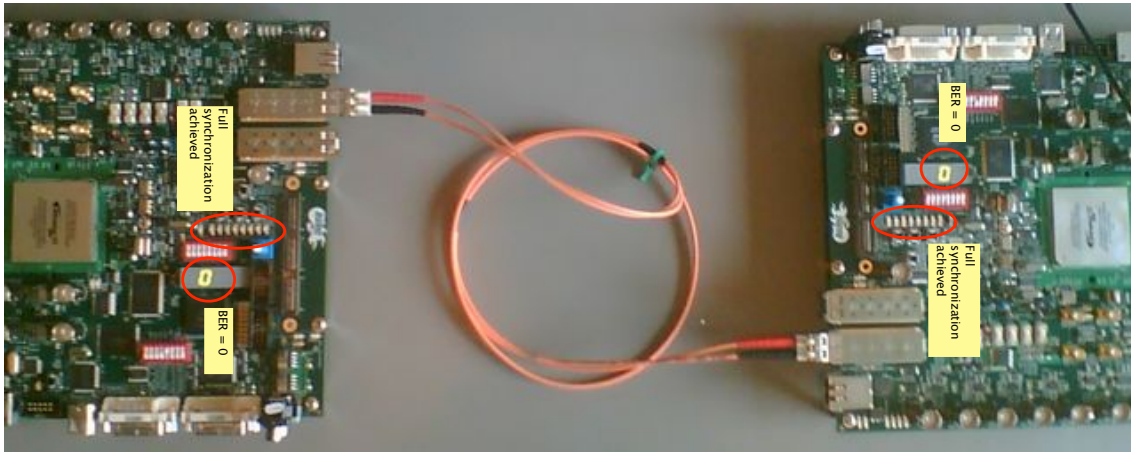


Figure 4.13: 6.144 Gbps Hardware test setup with the two Altera S2GX board connected back to back.

A 6.144 Gbps OBSAI RP3-01 point-to-point full-duplex transmission test setup was built running at 153.6 MHz bus clock. Radiocomp’s OBSAI RP3-01 IP is supporting all OBSAI RP3-01 line rates including the 6.144 Gbps extension via a parameter configuration only. Stratix II GX dynamic channel reconfiguration also is supporting multiple rate configurations and backward compatibility with 3.072 Gbps link have been demonstrated using SFP+ FTLX8571D3BCL optical transceivers as RP3-01 physical layer. The measurements of the signal integrity compare the 3.072 Gbps with the 6.144 Gbps eye diagram with acceptable signal’s eye quality, proving an error-free communication with internal BER measurement.

## 4.4 A Novel Physical Layer Receiver Circuitry with Deterministic Latency

This section analyzes the receiver part of a serial interface as the critical point for the delay accuracy and is presenting a novel approach for the design of a generic serial receiver architecture providing sub-nanosecond delay measurement resolution. The receiver architecture is generic and equally applicable to either CPRI or OBSAI RP3-01 interfaces and implementable in any RTL technology including cost-effective low-end FPGAs. This work has been published on the German journal Frequenz [1].

As addressed in chapter 2, wireless access eNBs use TDD or FDD duplex access mode to the air-interface. The TDD mode specifically requires accurate synchronization of frame timing over time to ensure that multiple radio nodes and user equipment can access the downlink and uplink portion of the airframe synchronized and not interfering with each other. For both access modes advanced data processing techniques are applied at base band level to enhance the channel capacity. Such techniques like MIMO and, new schemes as CoMP transmissions [17, 18] are based on the knowledge of channel delay variation in multi-path environments, and the internal delays of sample transporting between base band processing module and the RRH module must be known very accurately.

The knowledge of such delays plays an important role for the eNB to increase the cell throughput to specific users and optimize coverage depending on the actual radio resource utilization. Therefore, constant measuring and monitoring of the eNB internal delay including optical medium is required. Ambient temperature variations over the fiber across distances (up to 20 km) will result mostly in slow phase variations of the signal over time (wander), as well as jitter.

The knowledge of such delay variations is hence of great importance for optimizing 4G wireless access networks and will be presented and analyzed in the following sections.

### 4.4.1 Physical Layer Receiver and Data Path Delays

The data path delay can be measured as the delay from when the first bit of a radio frame byte boundary (comma character) arrives on the electrical receive interface until the radio frame pulse is released internally, indicating the detection of an alignment byte pattern on the module synchronization interface. The delay components can be subdivided into three categories according to their properties over time:

- Fixed known delay (Constant)

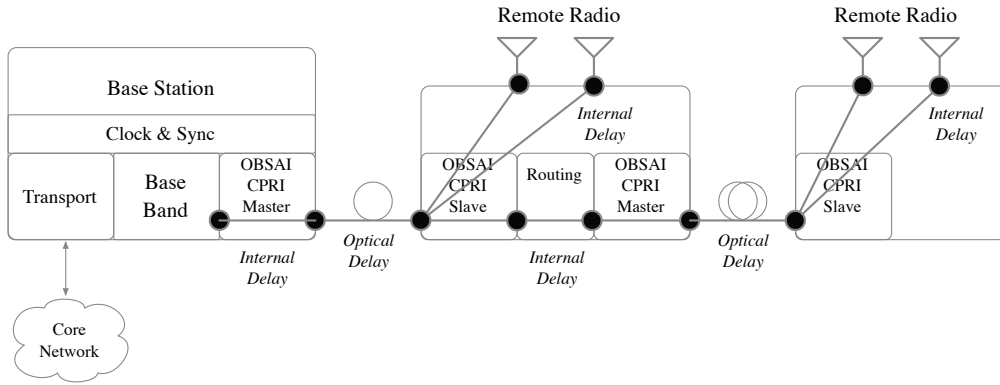


Figure 4.14: eNB with RRHs in multi-hop configuration showing the different delay path components.

- Measurable delay (Variable)
- Not measurable delay (Variable)

where the last part will contribute to the link delay inaccuracy. In multi-hop applications, the variable not measurable delay may add up at each node and it may cause the total delay to exceed the requirements stated in the standards. Variables not measurable delays in both eNB / RRH and master / slave ports can be:

- Data delay in comma alignment function
- Data delay in byte alignment function
- Data delay in clock phase synchronization buffer
- Phase difference between SerDes recovered clock
- Inaccuracies of Serial to parallel conversion between optical / analog / digital domains and system clock

The first three delays in the list above will not typically be measurable when the associated function is part of SerDes PCS made for traditional communication systems, where measurement of delay is not required. In the radio module, the normal phase (e.g. average phase in absence of jitter) between the recovered clock and central clock will be known, since the recovered clock used as input to the interface module is also used as phase reference to generate the central clock. It is required that the clock path following the serial data stream and clock path used as PLL reference clock for central clock generation does not contain any unsynchronized dividers. The length of the buffer takes constraints from delay shifts that are caused by the optical cable length and variable delays. The impact of these variable delays has less relevance at the radio

module slave port since the buffer contents are read with the jitter cleaned recovered clock from the incoming link. Here, the assumption is that the clock drift caused by the variation in cable length is so slow that clock recovery is always stable during the timing shift.

At the eNB master receiving port, if the phase is not known there will be a delay inaccuracy at one clock period of the receive clock, whose frequency is related to the rate. The lower the rate is, the larger is the inaccuracy introduced. Hence, it is required to know the phase difference between the receive clock and transmit clock.

The buffer is relevant though in the eNB side. In a master to slave transmission in time, with a long cable the variation in length could cause shift of several clock cycles in received data at the slave port. The remote module is totally unaware of that, since its master clock is locked to the recovered clock from the interface and it will follow the data. At the RRH side the recovered clock from the interface is jitter-cleaned and it is used for re-transmission of data back to the eNB, which instead will then see possible clock shifts in the receive buffer. At eNB, without a properly sized buffer there would be either underflow or overflow of the receive buffer read. The resolution of under- or overflow is an absolute number of clock cycles in either negative or positive direction. The eNB read buffer alignment related to the transmit clock should be large enough to compensate also for the maximum negative shift (cable shortening due to temperature variations). During system startup it is not possible to say if the cable length is currently at maximum or at minimum. That is why the receiver buffer alignment at base station startup should be at least two times the maximum one-way delay variation. There is here the assumption that remote module master clocks are always synchronized to the recovered clock and no other clock shift is occurring in the designs. The sample buffering in the receive ports has effect mostly to the eNB receive branch, since RE clock offset is drifting along with the cable length.

The clock frequency remains stable enough at the remote module despite the drifting, meaning that the relative timing is stable, but absolute timing is shifting. Assuming a simple case of a single RRH connected to the BBM, when TX diversity (or MIMO) data streams are received through one link and by one RRH, the drifting does not have effects to the relative timing requirement of  $\frac{T_c}{4}$  period time that it is then reduced by eight in the specifications to allow other inaccuracies at the antenna path i.e.  $\frac{T_c}{32}$ . In the situation where a single remote module is served through two concurrent links using TX diversity, then there will be an impact on the relative timing between data stream from each of the links.



### 4.4.2 Design of a High-Precision Receiver Digital Delay Measurement Circuit

We present a generic architecture for a MGT (Multi Gigabit Transceiver) physical layer receiver circuitry with delay measurement precision below 1 ns of resolution calculated from averaging a number of measurements in a pre-defined measurement period.

The novelty of the proposed solution is a delay average measurement circuit as opposed to real-time high-speed clock measurements, with the assumption that on an optical link between a eNB and a RRH the delay variations over optical the medium - due to temperature variations - will be rather slow over time, and the system will need to re-synchronize anyhow if the thresholds will be reached or internal compensation of timing will apply. The solution is generic and applicable to either OBSAI RP3-01 or CPRI interfaces (based on XAUI signaling), and is RTL based and can be implemented in any FPGA or ASIC technology. It lowers the requirements on the maximum clock frequency required to run the measurement for very high baud rates as high as 6.144 Gbps and supporting further line rate extensions up to 9.8304 Gbps. On the data path, a 32-bits wide size was chosen (40-bits before the 8B/10B coding). This enables to run even the highest line rates using a relatively low clock frequency with a factor of  $\frac{1}{40}$  of the line rate enabling cheaper FPGA implementations. The block diagram of the receiving path is provided below in Figure 4.15:

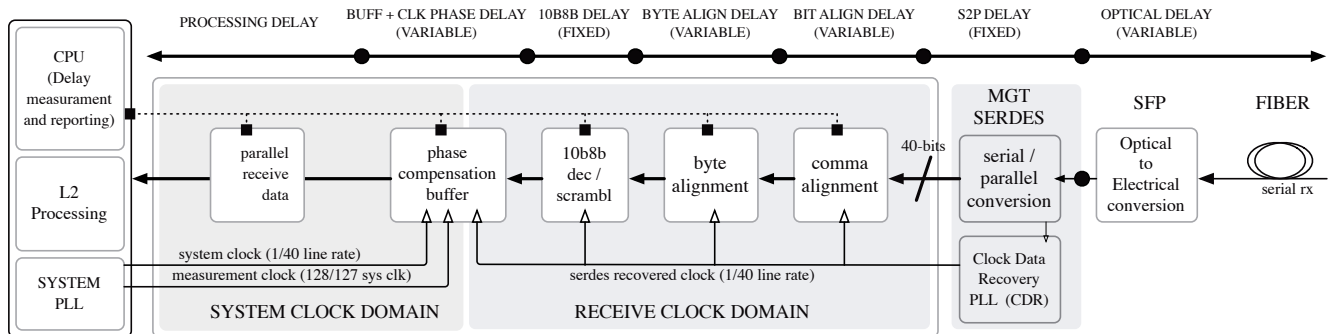


Figure 4.15: Serial to parallel receiver circuit with deterministic delay latency and measurement features.

In the receiver path, comma alignment and byte alignment have a variable measurable delay. When an MGT receives serial data, it needs to determine the byte boundaries of the data before it can present the data as parallel bits. An alignment block typically performs this function. The exact method used for alignment depends on the type of encoding used for the data; for comma alignment of 8B/10B the receiver searches the incoming serial stream for commas, which are

8B/10B Control characters that cannot be created by concatenating other characters. When it finds a comma after a certain search time, it lines up the comma boundary to its byte boundary, so that all the data that follows are aligned. The actual delay of these functions shall be readable from a register from the management system.

The next block, the 8B/10B-decoding block, has a fixed and static delay. At the phase synchronization buffer block, the latency of data depends on the number of 32-bit words stored in the buffer and the phase difference between the recovered clock (receive clock) and the system clock (transmit clock). A register-based access is used to read the current buffer fill-up with a resolution of 32-bit words, or 40-bit words before 8B/10B decoding. However the exact delay also depends on the phase between recovered receive clock used to write data into the buffer and the system clock used to read from the buffer. Often this phase is not known, and even if the phase is known it is not possible to decide on the delay value if the phase is near zero. That means there often will be a delay inaccuracy at one data word delay. The fill level of the receive buffer is normally measured once every system clock cycle. Since the core clock is  $\frac{1}{40}$  of the recovered clock (which has not been jitter cleaned), assuming for example a 614.4 Mbps line rate the clock period is lasting 65 ns, and the  $\pm 32.5$  ns represents the maximum inaccuracy can be introduced by a one clock period phase shift. CPRI compliance requires  $\pm 8.16$  ns inaccuracy for each hop.

We present a method that enables to measure the receive buffer and clock phase difference between the write and read domains very precisely. This can apply on any serial receivers at the master or slave side (either at eNB or RRH in multi-hop environments). This feature is using an additional external clock signal (*ex\_clk*) for the measurement and it will typically be generated from the system clock (*clk*) and being phase aligned with it, such that it has an N times higher frequency or an odd N/M frequency.

An integration period shall be defined to a value N, such that N clock periods of the external delay measurement clock are exactly equal to the amount M of system clock periods. The result of the delay measurement can be read after such integration period in a status register and the measurement may be repeated at regular intervals. The Equation 4.2 provides the resolution of the measurement with a given extended clock (*ex\_clk*) period as indicated in Eq. 4.3:

$$Resolution = T_{CLK} * \frac{GDC(M, N)}{M} \quad (4.2)$$

$$T_{EX\_CLK} = T_{CLK} * \frac{M}{N} \quad (4.3)$$

As an example, we can select a measurement clock frequency  $8/7$  of the system clock. This means that during seven (7) system clock cycles, we will get eight (8) fill level samples measured, but at different phases of  $clk$  with  $ex\_clk$ . If these eight (8) measurements are averaged over seven (7) system clock periods, we will have a much more accurate measurement of the average fill level of (and thereby delay through) the elastic buffer during the seven (7) cycles.

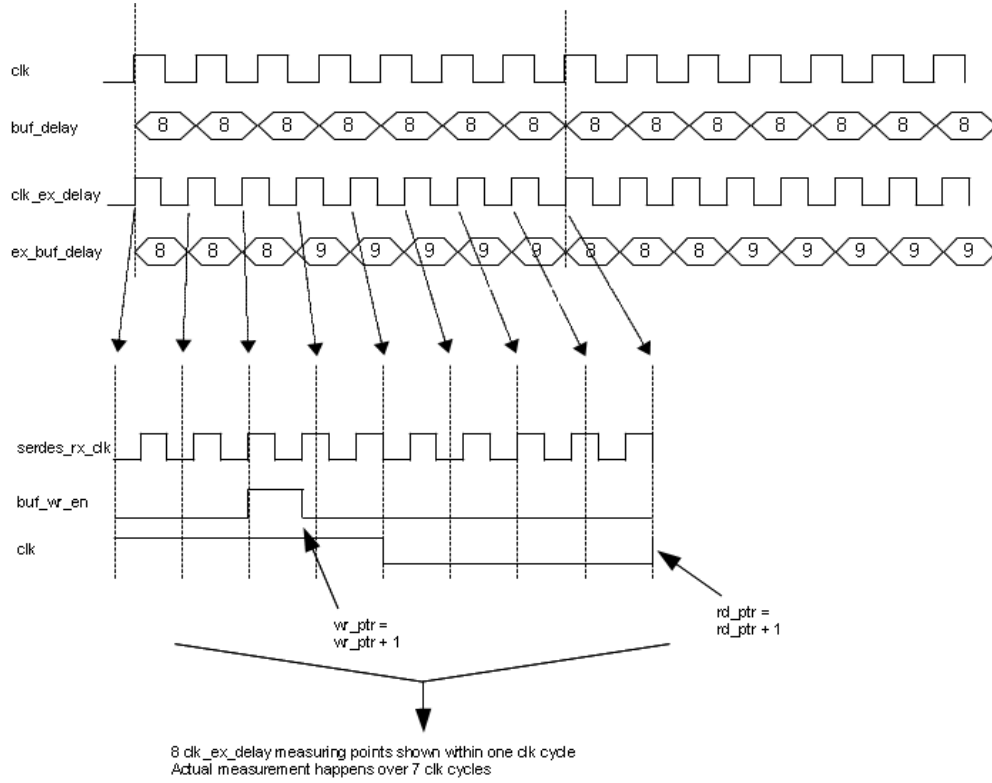


Figure 4.16: Example of Extended delay measurement using  $N = 8$  and  $M = 7$ .

At the bottom part of the figure this is illustrated but compressed to one system clock cycle (for simplicity, system clock in Fig.4.16 is  $\frac{1}{10}$  of recovered clock). At the fourth recovered clock cycle, the buffer is written, causing the fill level to increase, and at the rising edge of the system clock, the buffer is read and the fill level will decrease. If only the system clock is used for the delay measurement, then the variations in fill level will not be caught, just as the "write time" may move without being measured. Since the extended delay measurement clock measures at eight (8) different phases of the system clock, this is much more accurate. In the example above in Fig.4.16, we would accumulate the eight (8) measurements of the buffer fill up level  $3 \times 8 + 5 \times 9 = 69$  and then divide it by eight (8) to get the average delay over the seven (7) system clock cycles (and system clocks periods is the measuring unit). So we would measure an average delay of  $69/8 = 8.625$  system clocks cycles. The resolution of the new measurement is  $1/8$  of  $T_{clk}$ . In order to know the resolution of the measurement, it is a necessity that the relation

#### 4.4. A Novel Physical Layer Receiver Circuitry with Deterministic Latency

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between system clock and extended measurement clock is known. If the relation is not known, it cannot be guaranteed that all the possible phases are covered during the integration period and the accuracy of the resolution will decrease. The accuracy will increase by the closer the relationship  $N/M$  of extended measurement clock to system clock is to the unit. For instance, if the relationship is 128/127, the resolution of the measurement will be  $T_{clk}/128$ . Averaging over a fairly large number of cycles is accurate enough since the variations on receive clock are primarily caused by delay variations on the transmission fiber. These are in turn caused by temperature variations and the like, meaning that the phase will not change significantly within the integration period. To illustrate the resolution performances, we provide here below few examples.

We selected a 1.2288 Gbps as in Table 4.4.2, a 3.072 Gbps as in Table 4.4.2 and 6.144 Gbps rate as in Table 4.4.2 and we provide a set of different theoretical delay measurement resolutions using a data path clock frequency at  $\frac{1}{40}$  of the line rate due to the 40-bits data path size. We present as examples the resolution that is possible to achieve with an odd ratio clock and high frequency clock for each rate.

M	N	T_CLK	T_EX_CLK	Theoretical Resolution
128	127	32.55 ns	32.80 ns	254 ps
64	63	32.55 ns	33.06 ns	508 ps
8	7	32.55 ns	37.2 ns	4.06 ns
1	4	32.55 ns	8.13 ns	<b>8.13 ns</b>
1	2	32.55 ns	16.26 ns	<b>16.26 ns</b>

Table 4.4: 1.2288 Gbps resolution with odd ratio external clocks 12/127 or 64/63 of system clock frequency at 30.72 MHz - and with high frequency external clock at 2x or 4x of system clock frequency of 30.72 MHz. It can be seen that measurements made with higher frequency clocks will result in a non-compliance to the CPRI requirements even for a single hop.

M	N	T_CLK	T_EX_CLK	Theoretical Resolution
128	127	13.02 ns	13.12 ns	101.7 ps
64	63	13.02 ns	13.22 ns	201 ps
8	7	13.02 ns	14.88 ns	1.62 ns
1	4	13.02 ns	3.25 ns	3.25 ns
1	2	13.02 ns	6.50 ns	6.50 ns

Table 4.5: 3.072 Gbps measurement resolution with odd ratio external clock and with high frequency external clock. It can be seen that measurements made with higher frequency clocks will result in a non-compliance to the CPRI requirements right after the first/second hop.

## 4.5. Summary

M	N	T_CLK	T_EX_CLK	Theoretical Resolution
128	127	6.51 ns	6.56 ns	50.85 ps
64	63	6.51 ns	6.61 ns	101.7 ps
8	7	6.51 ns	7.44 ns	813 ps
1	4	6.51 ns	1.62 ns	1.62 ns
1	2	6.51 ns	3.25 ns	3.25 ns

Table 4.6: 6.144 Gbps measurement resolution with odd ratio external clock and with high frequency external clock. It can be seen that measurements made with higher frequency clocks will result in a non-compliance to the CPRI requirements right after the third/fourth hop.

It can be seen that especially at the low rates, the odd ratio delay measurement is providing a very accurate resolution of the measurement that cannot be obtained with higher frequency clocks. Even at higher rates, the extended delay measurement provides a very accurate measurement. The extended delay measurement is seen especially when applied to multi-hop systems, where the inaccuracies will add up for each node, and limiting the number of units that can be chained. This method enable to improve the reliability of the entire eNB system.

## 4.5 Summary

An advanced modular interface protocol architecture for both RP3-01 / CPRI interface controllers is presented. It supports increased serial baud rates increase up to 12.288 Gbps over either FPGA or ASIC technology. The design architecture has been verified to operate correctly at 6.144 Gbps and at 9.830 Gbps line rates using high end FPGA technology. The 12.288 Gbps rates requires appropriate SerDes availability which is not in place at the time of this writing.

The delay measurement circuit proposed enables significant improvements delay measurement accuracies up to 100 ps when compared to traditional real-time measurements made with high frequency clocks. The delay measurement solution is silicon agnostic and can run in any RTL technology. The circuit implementation is future proof and applicable to either CPRI or OBSAI RP3-01 standards. The software programmability enable a system designer to decide on the required accuracy targets by selecting appropriate values for the N and M factors on the extended clock frequency selection. The configuration can be controlled the software management layer, and it depends on the available system PLL configurations settings for delivering the correct measurement clock frequency. Overall, the solution provided enables cheaper and more reliable radio networks deployments.

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## Chapter 5

# Discussion and Conclusions

In the evolution from 3G to 4G wireless networks, radio access standards meeting IMT-A requirements are converging to a fewer number of options in order to enlarge the economies of scale for equipment - both for users and base stations - thus reducing costs. LTE and LTE-Advanced are expected to meet and exceed the IMT-A requirements for throughput, capacity, and mobility at the cost of increasing the portion of used spectrum up to 100 MHz and by exploiting multi-antenna techniques for achieving the targets. Spectrum availability and geographical harmonization - together with meeting the expected capacity growth - represents the current major challenge for the realization of adequate access networks. The large number of fragmented frequency bands operating in either FDD or TDD modes and the current fixed spectrum allocation has several limitations in terms of flexibility and optimal frequency use leading to non-optimized traffic load sharing. In several regions there are not enough frequency blocks of sufficient width to accommodate larger channel bandwidths.

A dynamic spectrum allocation and advanced techniques for radio channel capacity improvement was introduced to maximize channel capacity, but this scheme impacts the total bandwidth demand and the realization of a properly sized physical radio access layer. Despite the fact that IMT-Advanced technology likely will mature fully within the next 5-10 years, key frequencies between 1.7-2.6 GHz and total bandwidth requirements up to 40 MHz have been identified as intermediate targets applicable for the next 3-5 years. The 2.3-2.4 GHz band for TDD LTE operation in China is expected to be the first one to potentially benefit the IMT-A technology enabling spectrum use of up to 100 MHz for each antenna.

The boundary between software defined and software configurable radios have been investigated presenting the key limitations of the current commercial radio technology. Functions are partitioned in frequency independent and frequency dependent, where the latter is the factor limiting full SDR applications. The major limitations identified are operations over a limited frequency range thus requiring several radio variants for larger bandwidth coverage. As IMT-A

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requires access to portions of spectrum as high as 100 MHz, this requirement constitutes a considerable extension impacting mostly the DA and AD technology available today. Multi-RAN operations are possible but only within the same frequency band, limiting the capability of SDR base stations today, where for each spectrum band covered, a separate radio unit is required. An architecture proposal for a highly integrated radio module has been made. The system presents a digital environment implemented by a digital chip hosting interface and digital signal processing and conditioning functions. The digital chip interfaces to one or more RF environments, where the TX and RX analog chain are grouped in a TX RF IC and RX RF IF respectively with power amplification. This solution offers modularity and scalability, enabling support for 2x2 or 4x4 configurations.

4G networks will adopt the distributed and open eNb base station architectural model as the foundation of future radio access systems. The interface of most relevance is the interface between the base band processing module and the remote radio module based on either CPRI/ORI or OBSAI RP3-01 definitions. The remote nature of the communication introduces a complexity in the interface system for operating synchronously, and the selection of either interface basically dictates if this complexity must be placed in the base band side (OBSAI RP3-01) or in the radio side (CPRI). Based on the analysis made, a 15 bits sample envelope with CPRI enables slightly higher carrier-grade capacity. Overall CPRI comes with a more complex routing, delay, and synchronization management for the remote end. On the other hand it has been found that OBSAI RP3-01 enables more flexibility with its built-in features at the cost of a slightly lower carrier capacity. In either case, it has been identified that unless serial baud rates increased to 12.288 Gbps (current definitions are limited to 6.144 Gbps), the long term IMT-A requirements of delivering up to 100 MHz bandwidth with multi-antenna configuration will not be met unless baseband IQ compression techniques are used.

Interoperability between third party vendors has for a long time been an impediment to real implementations due to the lack of a system test specification procedure and lack of dedicated test equipment to validate the base band and RRH module interfaces. This study has focused on RP3-01 interfaces and has introduced the concept as well as co-developing an air-interface profile specification along with improvements in the specification definitions covering the most relevant aspects for each protocol layer. As the complexity of an OBSAI RP3-01 implementation resides in the synchronization procedures, an analysis has been carried out focusing on the mechanisms utilization, and system start up sequencing in an OBSAI RP3-01 has been studied and modeled. A proposal for an improved start-up sequence was made to enable deterministic delay measurements in both DL and UL directions without introducing additional inaccuracies.

An advanced modular interface protocol architecture for both RP3-01 / CPRI interface controllers was presented supporting increased serial baud rates with existing RTL technology like FPGAs or ASICs. The design architecture has been verified to operate correctly at 6.144 Gbps and at 9.830 Gbps line rates using high-end FPGA technology. The design is future proof and can support rates up to 12.288 Gbps as they become standardized in a near future. The delay requirements have been investigated together with the potential sources of measurement inaccuracies at the serial to parallel receiver level, revealing that traditional methodologies for delay measurement are not sufficient to meet the requirements in multi-hop configurations. A generic and advanced serial to parallel receiver circuitry has been proposed applicable to both RP3-01 and CPRI interfaces enabling the use of deterministic latency measurement blocks and implementable for any RTL technology.

## 5.1 Summary of Contributions

- The spectrum portion between 1.7 GHz and 2.6 GHz was identified as having the largest worldwide utilization. Specifically the TDD band between 2.3-2.4 GHz in China and the FDD band between 2.5-2.6 GHz in Europe are expected to be the first ones to roll out IMT-A services with LTE-Advanced.
- Legacy 2G and 3G services will be maintained while fading out over time, and the requirements for MultiRAN eNb equipment will be to run multi carrier GSM, UMTS and LTE simultaneously over the same or over different frequency bands.
- Macro eNb applications with more than 40W per antennas will operate at frequencies up to 2.7 GHz aiming at increasing coverage and number of users, while Micro and Indoor applications will be able to provide coverage at higher frequencies up to 3.8 GHz with high data rates but lower number of users per cell.
- The IMT-A long term capacity requirements up to 100 MHz and 4x4 MIMO antenna configurations for a total of 400 MHz are exceeding the transport bandwidth that can be provided with today's interfacing technology at 6.144 Gbps between the base band and remote radio module.
- The IMT-A short term capacity requirements have been identified at 40 MHz of bandwidth and 2x2 MIMO configurations for non-contiguous Component Carriers (CC) up to 2.6 GHz of operations with multi-carrier transmission.
- The next generation of radio modules for 4G networks will increasingly leverage the integration of different functions into a SoC. A remote radio module made with discrete components can be substantially reduced to three integrated chips including most of the



## 5.1. Summary of Contributions

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functionalities: a) a digital chip integrating interfacing protocol, signal processing and control b) a multi-channel Transmission RF IC and c) a Receiver RF IC. Power amplification and filtering will be external to the integrated environments.

- The analysis and comparison of the CPRI/ORI and RP3-01 interfaces has shown for CPRI/ORI an higher carrier grade capacity when 15 bits samples are used, while RP3-01 interface has been found more flexible for synchronization and transport management at the cost of a slightly lower carrier grade capacity.
- For MultiRAN eNb, the sufficient Effective Number Of Bits (ENOB) for both downlink and uplink paths assuming 40 MHz of bandwidths, is found to be 15 bits. The 15 bits size enables more bandwidth efficient mapping of samples over CPRI/ORI enabling room for an additional carrier in some cases.
- To full-fill IMT-A requirements with signals up to 100 MHz of spectrum including daisy chaining assuming 15 bits sample size a rate increase up to 12.288 Gbps or baseband IQ signal compression techniques is required.
- Interoperability challenges can be reduced by defining an air-interface usage profile that includes interface configuration and operation guidelines. Likewise, further contributions towards easier interoperability is provided by improving relevant wordings in the main specification for delay measurement definitions.
- A RP3-01 synchronization architecture of the remote radio head based on synchronized buffering scheme was proposed allowing deterministic delay knowledge for both the downlink and the uplink paths.
- An improved link start up initialization sequence has been proposed to ensure that delays will remain constant after the RTT procedure is completed and a new Delta/Pi setting is applied on the remote radio module.
- Data path size of 32-bits have been chosen for implementing an advanced interface protocol controller supporting either RP3-01 or CPRI standards. This allows running the core at 6.144 Gbps into a low cost FPGA device and to support rates as high as 12.288 Gbps with reasonably low clock frequency at 307.2 MHz into high end FPGA or ASIC technology. In addition, the inclusion of optimized Ethernet / HDLC MAC and end-to-end delay measurement circuit allows the controller to be easy to use and self contained.
- The 6.144 Gbps functionality over a 32-bits data path was demonstrated in hardware in 2007. After that, 6.144 Gbps line rates were standardized enabling the increase of capacity for the WiMAX / LTE applications with daisy chaining topologies.

- A new serial receiver circuitry enabling sub-nanosecond and high-resolution delay measurements averaged over a programmable integration period was proposed. This enables cheaper and more reliable radio networks deployments.

## 5.2 Future Research

The bandwidth capacity grow addressed in this thesis will require OBSAI RP3-01 and CPRI/ORI rates as high as 12.288 Gbps to meet IMT-A standards requirements. In this respect, investigations on low cost optical technology, clock recovery and delay measurement are of great interest.

In 4G access networks infrastructure inter-eNB communications are important for efficient handover, resource optimization and coordination. Coordinated Multi-Point transmission and reception (CoMP) is a relatively new technique being extensively discussed within the context of LTE-Advanced [17, 18]. The basic idea behind CoMP is to apply tight coordination between the transmissions from different cell sites to the same terminal, thus creating higher system capacity and especially improved data rates at the cell-edge. There are several ways in which CoMP can be realized using different transport methods. CoMP concept fits well with distributed base station architectures. Already in current 3G networks, multiple, geographically dispersed remote radios connected to a central baseband processing unit are used as a cost-efficient way of building networks. Such structures allow for new transmission strategies. With the base band processing located in a single node, CoMP can be deployed as illustrated in Fig.5.1. In the downlink it implies coordination of the transmissions from multiple transmission points. Fig.5.1 shows a distributed eNb architecture using the RRH approach:

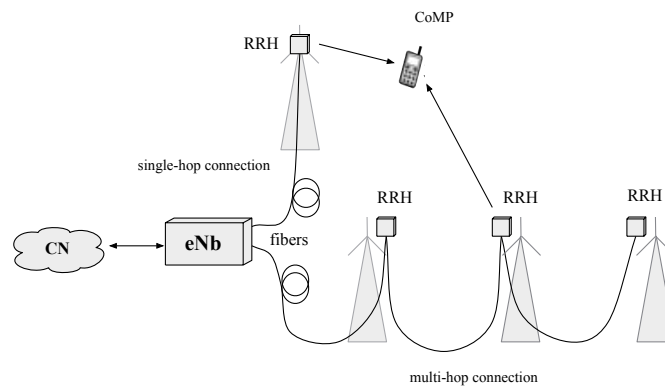


Figure 5.1: CoMP transmission with distributed eNb using multi-hop remote radio heads.

For transmission to be effective, it is important that data at each antenna port of each cell are aligned accurately. The remote topology of the radio head network with optical fiber,

makes the data delay between base band and antenna port subject to time and phase variations. Inaccuracies in the delay measurement and calibration will impact performances and it is thus important to realize a methodology for measuring the data delay very accurately. The delay measurement methodology is discussed in details in Chapter 3. For the uplink, coordinated multi-point reception is mainly a question of applying the relevant signal processing at the receiver. In many respects, this is similar to macro diversity, used already today in many cellular systems.[17]

Another topic for future research is shown in Fig.5.2 representing the concept of Cloud Radio Access Network (RAN) computing. This is a more advanced setup where one option is where the CPRI interface is embedded directly over the Optical Transport Network (OTN) using ODU Flex [67] [68] containers. This enables re-use of existing unused (black fiber) or re-framed fibers on existing fiber rings.

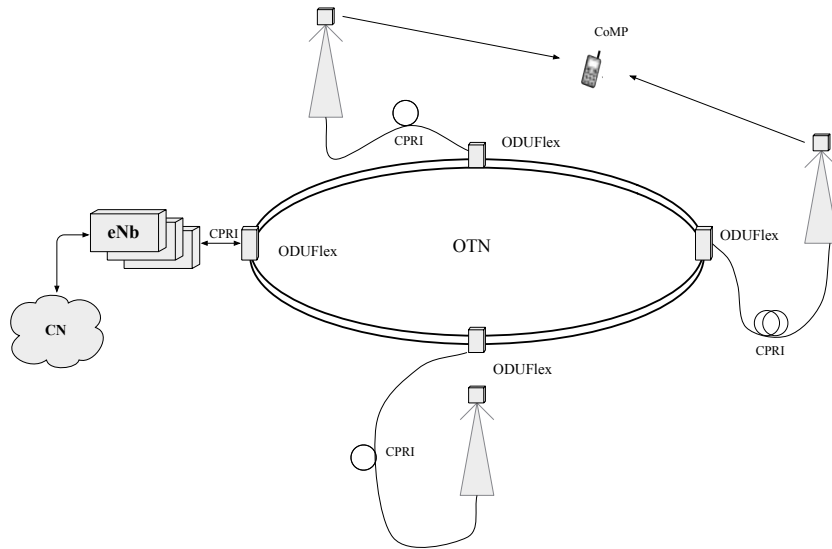


Figure 5.2: CoMP transmission with centralized eNb and remote radio heads with CPRI interface over OTN using ODU Flex[67]

For OTN, investigations of the effect of delays for the CPRI interface requirements are of great interest. OTN networks do not require full knowledge of delays for operations, and therefore the impact of CPRI frame mapping over OTN with ODU Flex is required.

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# Appendix A

## 4G networks overview

### Convergence of wireless access standards

Over the last 15 years several wireless standards had been introduced into the cellular market and each geographical region had developed a different set of radio access technologies based mostly on Global System Mobile (GSM) and Code Division Multiple Access (CDMA) because of specific regional frequency allocation and policies. At the same time the Wireless Local Area Networks (WLAN) path introduced shorter-range connectivity technologies based on Orthogonal Frequency Division Multiple Access (OFDMA) modulation schemes and supporting an always increased traffic capacity under limited coverage and mobility performances. Fig.A.1 shows the standards' fragmentation according to the respective geographical locations and nature for both the cellular and the WLAN paths. Each path evolved its performances in separate stages over time, as in their initial releases each standard's theoretical peak data rates were not met in practical deployments.

Overall the success of 3GPP standards is demonstrated by the economy of scale for their deployments.

The two main standardization paths are the 3rd Generation Partnership Projects (3GPP/3GPP2) and the Institute of Electrical and Electronics Engineers - Standards Association (IEEE-SA). The 3GPP Long Term Evolution (LTE) and the IEEE Worldwide Interoperability for Microwave Access (WiMAX) 802.16x are the two major paths for mobile broadband wireless for the next 10 years. The 3GPP LTE-Advanced (LTE-A) Release 10 [14] and the IEEE 802.16m (WiMAX2) [69] [70] are the respective candidate standards for IMT-A approval submitted in late 2009.

Both technologies are similar but with different implementations such as FDD versus TDD, 1 msec versus 5 msec frames, etc where design choices have been made for a variety reasons. From a

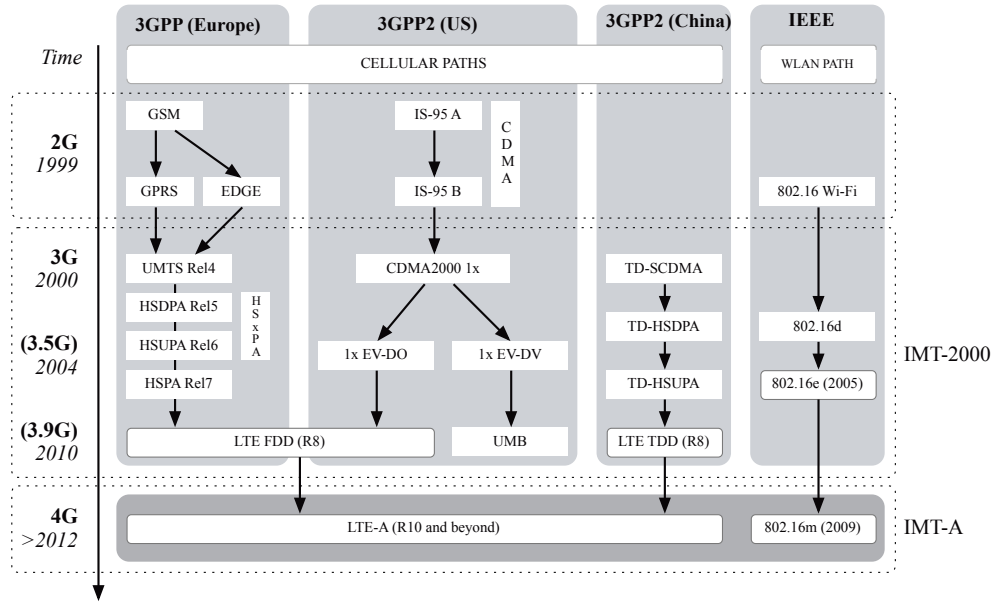


Figure A.1: Mobile and WLAN technologies evolution paths toward 4G mobile wireless networks

systems architecture standpoint they deploy similar functional decomposition (such as separating radio resource management from IP management and locating Radio Resource Management (RRM) in the BS and IP management in an access gateway). However, the specific protocols used between these elements are considerably different (motivated partly by the existing protocols in systems and to facilitate backward compatibility with already deployed systems). The fact that both technologies use OFDMA and MIMO would lead to comparable spectral efficiency up to first order of approximation. However, design choices about protocol overheads, control channel overheads, would determine the resulting efficiency. LTE appears to be clear choice for operators with FDD spectrum as well as operators with existing (GSM) deployments. WiMAX appears to be the clear choice for operators with TDD spectrum as well operators with frequency in the 2.5 GHz and 3.5 GHz band and operators with little or no legacy cellular deployments (mostly in emerging markets) [71].

All the fragmented 3GPP/3GPP2 cellular paths shown in Fig.A.1 will converge to 3GPP LTE-Advanced, which will be primarily considered in this thesis. Because LTE and LTE-A is the evolution of UMTS, LTE equivalent components are called Evolved UTRA (E-UTRA) and Evolved UTRAN (E-UTRAN) as these are the formal terms used to describe RAN. According to [72], "the evolved UTRAN consists of eNBs, providing the evolved UTRA U-plane and C-plane protocol terminations towards the UE. The eNBs are interconnected with each other by means of the X2 interface. It is assumed that there always exist an X2 interface between the eNBs that need to communicate with each other, e.g. for support of handover of UEs in LTE\_ACTIVE. The eNBs are also connected by means of the S1 interface to the EPC (Evolved Packet Core). The S1 interface support a many-to-many relation between aGWs and eNBs." The architecture is shown below in Fig.A.2:

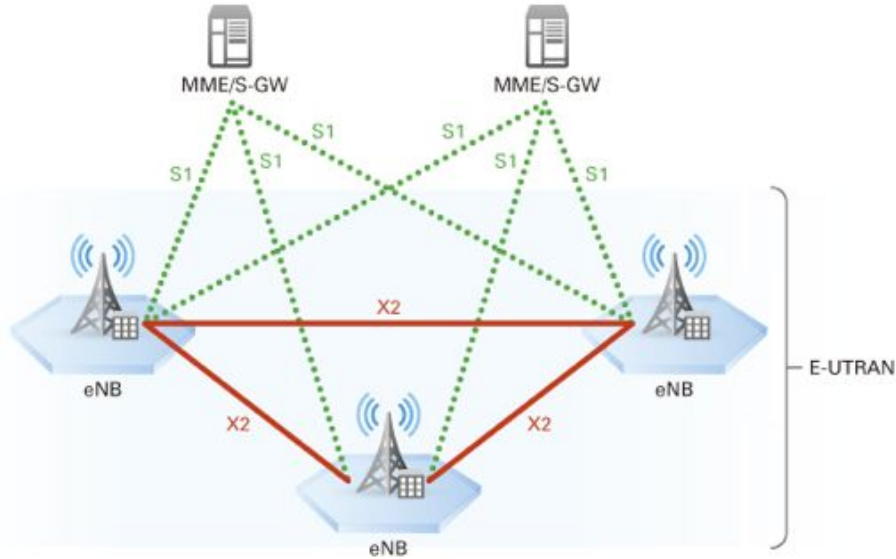


Figure A.2: E-UTRAN Logical Node Architecture [72]

In the E-UTRA, the Evolved NodeB (eNb) is the base station radio access node. The system is part of a larger 3GPP project called System Architecture Evolution (SAE) which is defining a new all-IP packet only Core Network (CN) generally known as the Evolved Packet Core (EPC). The combination of the EPC and evolved RAN (E-UTRA and E-UTRAN) is the evolved Evolved Packet System which is the correct definition for the entire system. Some guidance on LTE vocabulary can be found in [73].

From 2010/2011 each path is expected to adopt LTE R-8 to start with in either its E-UTRA FDD or TDD variant depending on the geographical region and later smoothly migrating to LTE-A (R-10 and beyond). On the other front, the IEEE WLAN path has recently been matur-

ing its 802.16m version of the WiMAX standard supporting more data-centric applications with enhanced mobility and supporting higher data rates as well. WiMAX and LTE radio technologies have many similarities on the air-interface [71]. For WiMAX the primary operation mode is TDD. The trends for mobile communication systems in terms of mobility versus the peak target rates are outlined in Figure A.3 below.

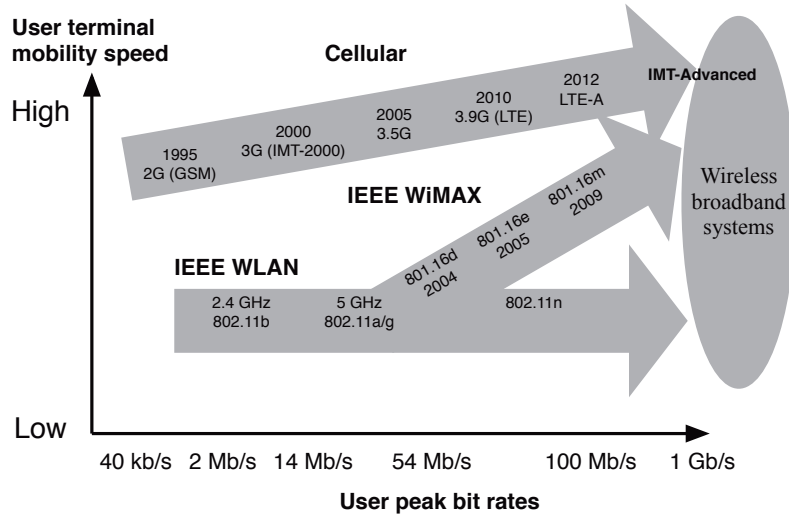


Figure A.3: Trends of mobile communication systems toward increased mobility and throughput [44]

The existing 2G/3G mobile networks were geographically fragmented and were designed and engineered based on the spectrum calculations made from ITU in the early Worldwide Radio Conference in 1997 (WRC-97). They were meant to support voice-based traffic as well as for low-speed, best-effort data services without scalability and support for higher performances. Convergence toward a single technology is expected reducing the number of equipment variants delivering high data rates and performances. Ultimately 4G networks will empower standard agnostic radio access equipments capable to run several wireless standards either independently or simultaneously, while being backward compatible with previous generations of 2G and 3G systems.

# Evolution of wireless networks infrastructure

4G radio access networks will consist of an overall improved and simplified packet switched network architecture (EPC) based on the experiences and learnings gathered from the wireless industry from the existing 2G and 3G deployments. The evolution of the network infrastructure toward LTE based systems is shown below as in Fig. A.4:

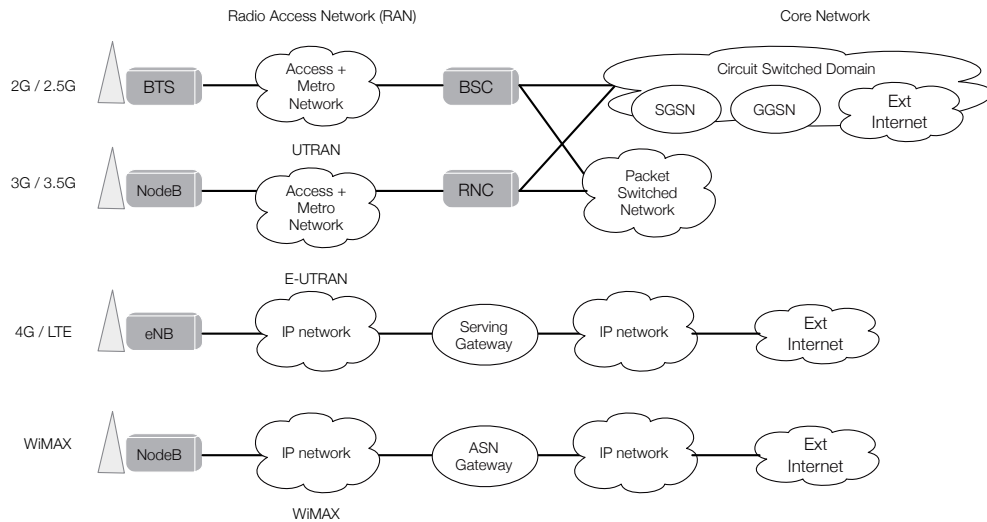


Figure A.4: Network evolution from GSM to UMTS/HSPA[23]

As of today the usage of different and separate access network infrastructure is commonly used as shown in Fig.A.5 for fixed and metro access, mobile wireless access for 2G and 3G and WiMAX access.

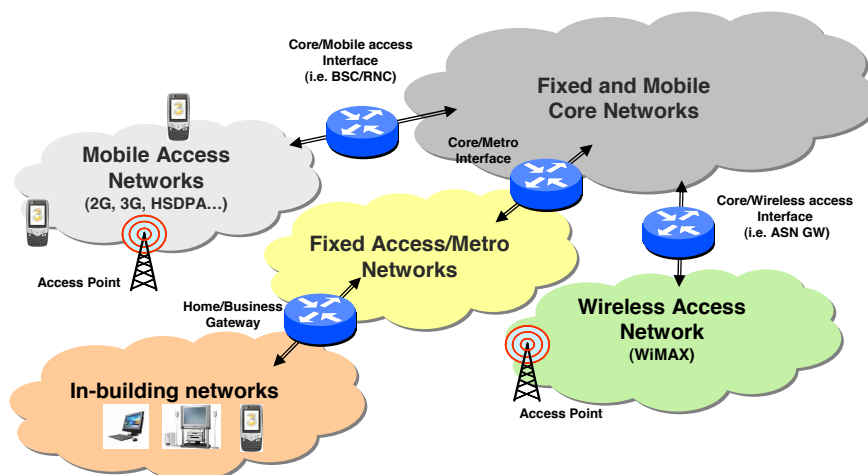


Figure A.5: View of today access networks: three different infrastructures for fixed/metro, mobile and wireless access networks[23]

At the same time, evolution of radio access base station (eNb) hardware has evolved from supporting a single technology and single frequency to support multiple technology and multiple frequency radio systems providing higher throughputs with the introduction of HSxPA and LTE technologies. The objectives overall were to reduce OPEX saving energy<sup>1</sup> and limit on-site interventions and simplify deployments with lighter equipments, fewer operations and easier cabling. Another objective was the sharing of equipments between GSM and 3G/4G anticipating also evolution for later standards. These are the main objectives of the distributed eNb architecture, also called base station hoteling as shown in A.6.

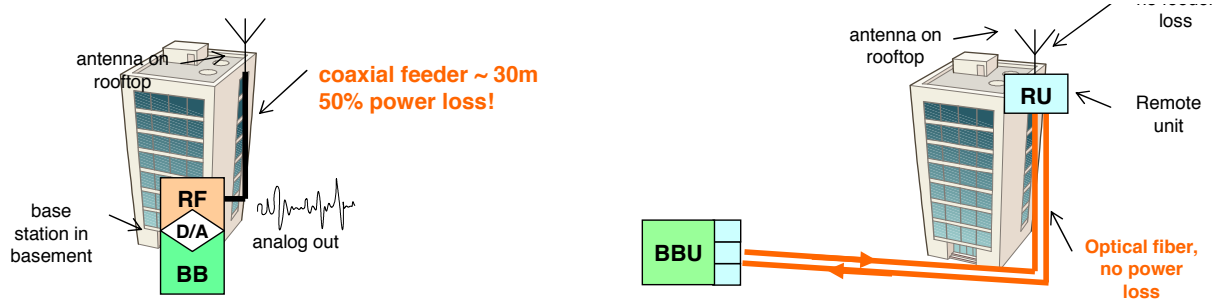


Figure A.6: Base station evolution toward distributed eNb[23]

An important requirement for communication systems and networks is interoperability between different vendor's user equipments. The main advantage of interoperability is that resources are exploited in an efficient way and economies of scale can prevail.

The concept for future networks is based on *logical nodes* and *interfaces*. The logical node architecture is a framework that describes functions and group them as logical nodes and connects them by well-defined, open interfaces. An example is the 3GPP LTE/SAE (System Architecture Evolution) [74] with the concept of the Evolved Packet Core (EPC) [75] as shown in Fig.A.7 and introduced in Section A.

EPC is an all-IP mobile core network concept coming with a converged framework for packet-based real-time and non-real-time services which have been introduced from 3GPP LTE R-8 in 2009 [Reference]. The EPC provides mobile core functionality that, in previous 2G/3G mobile generations, has been realized through two separate sub-domains: circuit-switched (CS) for voice and packet-switched (PS) for data. As shown in Fig.A.7, in 4G these two distinct mobile core sub-domains, used for separate processing and switching of mobile voice and data, are unified as a single IP domain.

<sup>1</sup>Typical BS energy consumption is around 1-1.5 kW with 50% power losses along the coaxial cable and 30-50% of BS energy consumption due to the Power Amplifier (RF part) [23]



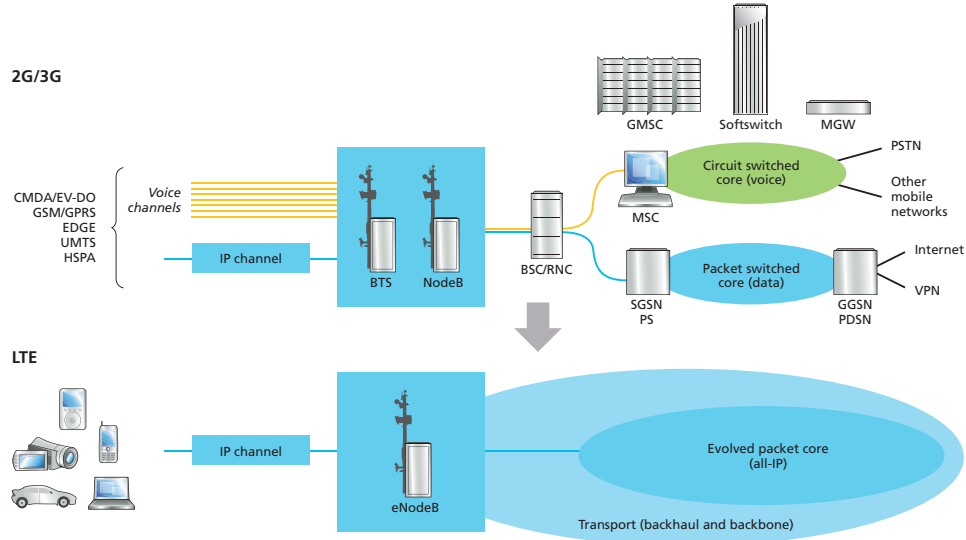


Figure A.7: 3GPP LTE/SAE evolution - Evolved Packet Core (EPC)

*EPC is essential for end-to-end IP service delivery across 4G networks and it is instrumental in allowing the introduction of new business models such as partnering/revenue/equipment sharing with third-party content and application/service providers.* LTE introduces significant technological advances on the radio node with enhanced NodeB (eNb) station, which area will be the focus of this report. As LTE provides more efficient use of the spectrum with wider spectral bands, this results in greater system capacity and performances. At the same time, the mobile core needs to change in order to provide higher throughput and low latency. EPC provides a simplified and improved all-IP flat network architecture enabling to meet such requirements [76].

Standard-agnostic radio solutions are bringing consistent cost advantages to operators due to the economy of scale as well as flexibility in a future proof technology. This is enabled by open radio interfaces and modular / scalable eNb systems with software defined radio personalities applied from a centralized network management system which will be later analyzed in Chapter 2.4.

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## 4G vision and targets

The fourth generation networks requirements have been introduced from the International Telecommunication Union - Radio Sector (ITU-R), which is the entity responsible to regulate and standardize international radio communications. ITU-R established in 2003 the International Mobile Telecommunications Advanced (IMT-A) initiative introducing the 4G networks targets with the [15] recommendation for wireless systems beyond IMT-2000.

Since its early days, 4G-networks vision did not include only an individual new radio access technology, but it rather incorporated in its vision a set of different radio standards that cooperate between each other and sharing a common packet-based core network infrastructure. With its multiple radio access technology vision, IMT-A comprehend 2G cellular systems, IMT-2000, fixed RLAN/WLAN and fixed xDSL accesses, digital broadcasting and a new radio access interface that inter-works together. All radio accesses are serviced from the same packet-based core network, supporting multiple services and applications. With this vision, the network equipment including the radio access, is expected to be generic and application-independent. The 4G-network concept is illustrated below in Fig.A.8, and the focus is on the new radio interface concepts.

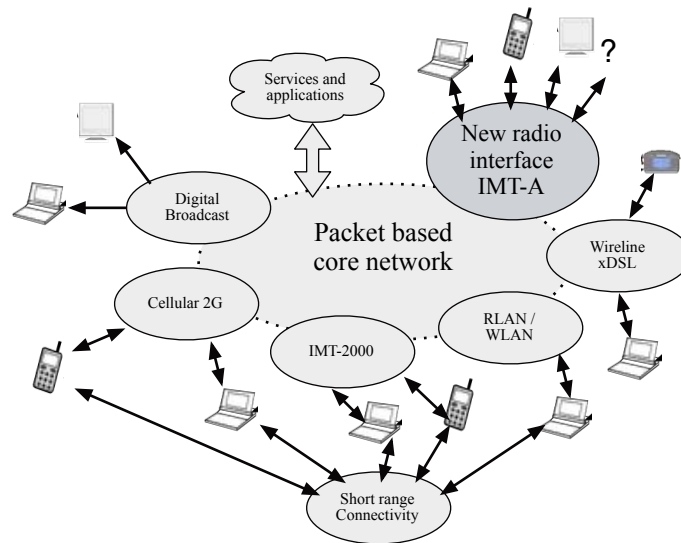


Figure A.8: Overview of the IMT-A 4G network concept with a variety of potential inter working radio access systems for long and short range connectivity [15]

The need for a new radio interface was raised from ITU-R mainly for two main reasons. The first reason was that the underlying and insufficient transport and access network infrastructures[33] was not adequate to support the large growth of the Internet traffic. The 2G and 3G technologies were not suited to support such rapid and heavy traffic growth in their



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# Appendix B

## 3GPP Frequency Bands

We report in this appendix the list of the relevant 3GPP frequency bands for both FDD and TDD systems and technology in use between GSM, UTRA and E-UTRA.

MSR and E-UTRA Band number	UTRA Band number	GSM/EDGE Band designation	Uplink (UL) BS receive UE transmit	Downlink (DL) BS transmit UE receive	Band category
1	I	-	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	1
2	II	PCS 1900	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	2
3	III	DCS 1800	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	2
4	IV	-	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz	1
5	V	GSM 850	824 MHz – 849 MHz	869 MHz – 894MHz	2
6 <sup>(1)</sup>	VI	-	830 MHz – 840 MHz	875 MHz – 885 MHz	1 <sup>(1)</sup>
7	VII	-	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	1
8	VIII	E-GSM	880 MHz – 915 MHz	925 MHz – 960 MHz	2
9	IX	-	1749.9 MHz – 1784.9 MHz	1844.9 MHz – 1879.9 MHz	1
10	X	-	1710 MHz – 1770 MHz	2110 MHz – 2170 MHz	1
11	XI	-	1427.9 MHz – 1447.9 MHz	1475.9 MHz – 1495.9 MHz	1
12	XII	-	698 MHz – 716 MHz	728 MHz – 746 MHz	1
13	XIII	-	777 MHz – 787 MHz	746 MHz – 756 MHz	1
14	XIV	-	788 MHz – 798 MHz	758 MHz – 768 MHz	1
15	XV	-	Reserved	Reserved	
16	XVI	-	Reserved	Reserved	
17	-	-	704 MHz – 716 MHz	734 MHz – 746 MHz	1 <sup>(2)</sup>
18	-	-	815 MHz – 830 MHz	860 MHz – 875 MHz	1 <sup>(2)</sup>
19	XIX	-	830 MHz – 845 MHz	875 MHz – 890 MHz	1
20	XX	-	832 MHz – 862 MHz	791 MHz – 821 MHz	1
21	XXI	-	1447.9 MHz – 1462.9 MHz	1495.9 MHz – 1510.9 MHz	1
NOTE 1: The band is for UTRA only.					
NOTE 2: The band is for E-UTRA only.					

Figure B.1: Paired bands in E-UTRA, UTRA and GSM/EDGE [35]

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MSR and E-UTRA Band number	UTRA Band number	Uplink (UL) BS receive UE transmit	Downlink (DL) BS transmit UE receive	Band category
33	a)	1900 MHz – 1920 MHz	1900 MHz – 1920 MHz	3
34	a)	2010 MHz – 2025 MHz	2010 MHz – 2025 MHz	3
35	b)	1850 MHz – 1910 MHz	1850 MHz – 1910 MHz	3
36	b)	1930 MHz – 1990 MHz	1930 MHz – 1990 MHz	3
37	c)	1910 MHz – 1930 MHz	1910 MHz – 1930 MHz	3
38	d)	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz	3
39	f)	1880 MHz – 1920 MHz	1880 MHz – 1920 MHz	3
40	e)	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	3

Figure B.2: Unpaired bands in E-UTRA and UTRA[35]

We list here a short description of the WRC-07 bands that have been identified:

- *450-470 MHz band.* The first band, 450-470 MHz, has very limited bandwidth with only 20 MHz available. That means that if the bandwidth is limited, operators that can use this band are reduced; and the capacity of the network is limited, however this band has the benefit of greater coverage and might have interest for military applications as well. In some countries, such as most countries in the Middle East, this band is not allocated for mobile services, but for security, public safety, therefore this band in many countries might not be used for 4G in the near future.
- *1710 to 2025 MHz band.* This is presently being used for CDMA and the other part of this band is being used for UMTS.
- *2.3-2.4 GHz band.* 100 MHz in the band 2,300 - 2,400 MHz (globally). An unpaired TDD arrangement seems to be the most capable solution for delivering high bit-rates. Therefore, NGMN supports TDD in this band. Mixing of FDD and TDD arrangements is not supported by NGMN in this band. The 2300 to 2400 MHz band is not available in most countries because this band has been historically available for public safety. For some countries, especially in Middle East, Latin America, and Europe it might be difficult to make this band available in the near future for 4G. However, for other countries, such as India and China, this band is under consideration for 4G. And if those big markets start using this band, maybe many other countries will start considering this band for IMT services. Also, this band has been opened to WiMAX in Korea, Malaysia and few other countries for some time now. Specifically in the perspective of IMT-Advanced and its expected capability of providing larger channel bandwidth (40 ... 100 MHz), this band will be one of the focuses for such usage. All other bands identified or allocated for IMT

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are relatively limited in their ability to support multi operator operation of such large carrier bandwidth within one single band. Additional solutions to this requirement include future carrier bandwidth aggregation.

- *2.5-2.7 GHz band.* The 2500 to 2690 MHz is the band which is presently available for IMT services in most countries, similar to Europe, Americas, APAC and Middle East; so this is considered with high priority for mobile broadband. Since it is 190MHz there is plenty of spectrum, so it will be able to offer good data rates, good capacity, and therefore seen in most countries for IMT and IMT advanced services.
  
- *3.4-4.2 GHz.* The 3.4-3.8 GHz also called "C-Band" is allocated to mobile and identified to IMT. The low band 3400-3600 MHz is allocated to Regions 1 and 3 already appointed for mobile broadband usage in EU/CEPT. The high band 3600-3800 MHz is allocated to mobile in Regions 2 and 3 decided for mobile broadband in EU/CEPT by year 2012 and both supports paired and unpaired arrangements. They are suited for very high data rate multimedia mobile broadband services for FDD 100 MHz duplex spacing for both bands using channel bandwidths > 20 MHz per operator. Both CEPT and ITU are currently developing channelling arrangements for the 3,400-3,600 MHz band. Moreover NGMN supports a band plan which would allow an extension to 3,800 MHz and possibly up to 4,200 MHz for use in countries where terrestrial mobile use is permitted.
  
- *4.4-5.0 GHz band.* Reserved for future usage.

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## Appendix C

# Open Base Station Interface Standards

### Distributed eNb and Remote Radio Heads

Remote radio heads (RRH), also called Remote Radio Units (RRU) in OBSAI [5] and Remote Equipment (RE) in CPRI[24], are certainly one of the most important parts of the new distributed base station topology. They are essentially the RF section of a modularized open architecture base station. A RRH consists of remote RF transceiver with transport interface over fiber/copper/wireless media at on one side and antenna connectors on the other side. The fiber may carry analog modulated signal (Distributed Antenna System - DAS) or a digital high speed serial signal between the base band and radio itself. RRH approaches are widely used today in 2G and 3G networks (UMTS / GSM / CDMA2000 / WiMAX / LTE) and a real installation is shown in Fig.C.1 for reference.

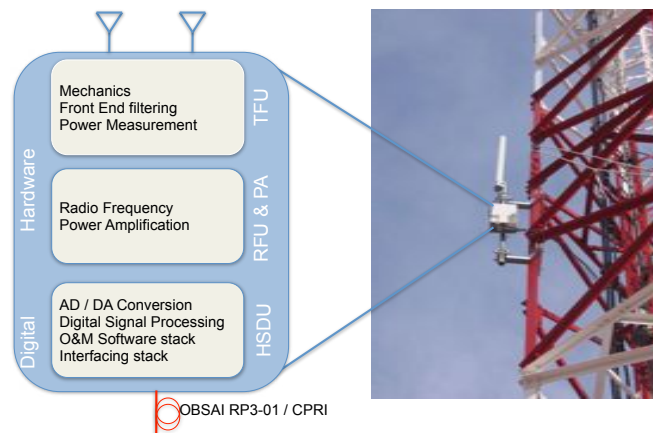


Figure C.1: Remote Radio Head module for Multi-RAN applications.

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A modularized architecture is critical for flexible BS, and standardized interface between the RRH would allow formation of an ecosystem of vendors to create interoperable RF and baseband processing modules [78]. The RRH brings advantages in having radio head near the antenna, which turns into higher transmit power in the downlink, better receiving performance in the uplink and elimination of heavy, costly antenna cabling and additional equipments like Tower Mounted Amplifiers (TMA) and Tower Mounted Boosters (TMB) [38]. Centralization of BB processing provides management and remote equipment upgrade advantages. In Distributed Antenna Systems (DAS) could also benefit from simulcast, neutral hosting, and multipoint to multipoint operations [7]. Among others, the major benefits that RRH provide are the following:

- Reduced RF loss
- MIMO and diversity operation
- Higher efficiency
- Flexible location capability

Typically, the RF receive and transmit signals are converted to a digital format and transported to the other base station subassemblies via optical fiber. The key internal functions of a RRH are as below:

- The receiver low-noise amplifier and transmitter RF power amplifier are mounted in a separate common unit that is located external to the eNb. Normally, this enclosure is weatherproof.
- The RRH contains a TDD switch or duplexer at the front end to facilitate receive and transmit functions to a single antenna.
- The RRH contains up and down converters to change the high RF frequency receive and transmit signals to a lower frequency that can be more easily processed.
- The RRH has digital-to-analog and analog-to-digital converters for use in the transmit and receive paths to convert the digitally formatted signals to their RF analog counterparts.
- The RRH has an I/Q and optical interface to connect to the main BTS via optical fiber. The RRH has some degree of O&M processing.

Remote radio heads have only recently become a true market. Historically, for the most part, they have been considered parts of base station systems and it was difficult to separate them from the base station as a whole. RRHs will be SDR-controllable and operate over multiple air interfaces becoming a common subsystem of distributed base stations.



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The decentralization of the macro base station into separate pieces has allowed the major components of these distributed base station topologies to be considered as subsegments of the overall wireless infrastructure hardware market. This transformation has been accompanied by a change in the perception of remote radio heads in the overall BTS hierarchy as efficiency, small size, ease of placement in relation to antennas, and the desire to promote diversity operation have collectively become more important. The latter point will, in fact, become a necessity for LTE systems and beyond. Service operators are also now purchasing RRH on a standalone basis as they fine-tune their networks for coverage and other operational issues. All of these factors point to the remote radio head becoming an independent marketplace at the subsystem level.

## Open base station standard interfaces

Standardization of the base band to radio interface has been for long time one of operators' main wishes. There are several reasons that have been pushing a standardization of base station forward:

- Less costly equipment upgrades of each site - Mast mounted equipments like antennas and tower mounter amplifiers it is a very costly operation and it is desirable to be minimized or even avoided. A remote radio head with remote firmware upgrade features offers the required flexibility in accommodating new features.
- As reported in Chapter 2, the multitude of frequency bands for meeting IMT-A requirements as well as the coverage requirements demands flexibility in equipment and vendor selection, and with standardized interfaces such selection process it is smoother.
- Merges or acquisitions of operators or OEMs with different vendor equipment may cause the necessity to interface equipment from another vendor. Likely it is desirable having mast mounted equipment from one vendor to be interoperable with several base band module suppliers with different features and performances through a standardized interface without requiring removal.
- Termination of a product line from a certain vendor may force an operator to introduce equipment from another vendor, therefore it would be beneficial having a standardized interface between two equipments.
- Reducing relative cost of radio modules by introducing competition of several specialized suppliers.

All the above cases are assuming that by avoiding to replace the whole BS equipment chain, at least some part of the capital investments can be saved making the network upgrade less

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costly. An open interface between BBM and RRH would allow only a limited amount of parts to be replaced, subject to a functional/hardware enhancement bringing valuable savings in resources, commodities and ecological aspects.

Open architectures have recently been introduced in wireless infrastructure networks for distributing and de-centralizing Base Transceiver Stations (BTS). Such approaches aim mainly at reducing the relative capital (CAPEX), operating (OPEX), development expenditures and efforts while increasing system performances and flexibility by defining a modular and standardized interfaces and internal BTS architecture.

The BTS is an integral part of the radio access network and is the bridge between the handset and the wireless infrastructure core network. In a distributed BTS network architecture, the radio module is remote relative to the channel card (base-band processing) and communicates with the channel card via a standardized digital optical interface. Distance over the fiber vary from indoor coverage up to a few kilometers. This is done to improve site performances and reduce site footprint as well as enable high efficiency sector coverage with multiple remote radio nodes. There are several standard for exchanging base band or intermediate frequency digitized signals between base band and radio module [79].

The Original Equipment Manufactures (OEMs) had introduced the OBSAI (Open Base Station Architecture Initiative) and the CPRI (Common Public Radio Interface) as a mean to enable the advantages of open base stations, however both these standards have been and still are considered semi-standards since for many aspects they are not providing to the end user the interoperability and completeness required for an easy deployment and as a matter of fact colliding with their own reason for being adopted. To overcome such interoperability challenges, ORI (Open Radio Interface) came as an extension of CPRI including only a selected number of configurations supported at L1 and L2 as a sort of profile and on top defining all the relevant L3 C&M functions which were really lacking and still being vendor dependent.

OBSAI RP3/RP3-01 and CPRI protocol are almost a decade-old technology that was introduced in 2002 and enhanced over time following the evolution from 2G to 3G and 4G systems. Both interfaces are based on the OSI layered protocol definition utilizing high-speed serial full-duplex and synchronous communication using line coding, framing and data mapping schemes. The data planes are including user data flow according to the In-phase and Quadrature (I&Q) base band format and also embedding Control & Management (C&M) and Synchronization flows definitions.



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- Reference Point 3-01 (RP3-01)

OBSAI defines the Remote RF Block or also called Remote Radio Head (RRH) concept as a radio module connected to the base-band through the Reference Point 3-01 (RP3-01) interface. The RP3-01 interface realizes a high speed optical communication link between the Local Converter (LC) module and the RRH. This interface is used to provide bi-directional transfer of digitized base-band radio data together with control and air-interface synchronization information.

RP3 Specification v.4.1 included point-to-point serial interface up to 6.144 Gbps for Up-link/Downlink Data, Control & Sync. The interface supports most of the common air-interface standards like GSM/EDGE, WCDMA/LTE, 802.16d/e and CDMA2000. The protocol stack is based on a packet concept using a layered protocol with fixed length messages and fixed IQ Sample envelope size.

OBSAI has the advantage compared to CPRI of specifying a complete framework for the communication between all the BS modules and reference test specifications. The RP3-01 interface in particular defines a feature richer application and transport layers, leveraging on advanced protocol embedded features like RP3 message headers, RP3-01 FCB (Frame Clock Burst) for synchronization and RTT (Round Trip Time) for delay measurement and providing thus higher flexibility in the system configuration.

## Common Public Radio Interface - CPRI

The Common Public Radio Interface (CPRI) is a closed industry group started in 2003 from Ericsson. The specification includes a point to point interface definition between Radio Equipment Controller (REC) module and Radio Equipment (RE) modules. CPRI, unlike OBSAI, focuses on the interface only and does not extend its efforts into the full eNb architecture. CPRI it is comparable to OBSAI RP3-01 interface. It includes User Data, Control and Management Planes and Synchronization transport mechanisms. The CPRI scope is to provide a relatively simple and cost efficient solution supporting independent technology evolution with a limited need for hardware adaptation.

The wireless standards supported are 3GPP UTRA FDD, WIMAX Forum Mobile System Profile v1.1.0 and both FDD and TDD LTE in the CPRI Specification v.4.1. The User Plane Data has programmable IQ sample envelope size between 4 and 20bits for optimized bandwidth allocation but in practice only a limited subset is supported from commercial REC /RE appli-

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cations. The C&M channel supported are the Slow C&M Channel based on HDLC and the Fast C&M Channel based on Ethernet. In addition there is a Vendor Specific Sub-channel and L1 In-band channel. Synchronization words (K-char) and BFN and HFN frame counters are also provided.

CPRI specification defines only the physical and link layer communication protocol between radio equipment controller (REC) and radio equipment (RE) modules leaving open to the vendor the upper layers definitions since CPRI itself does not focus on the Control & Management plane definition but only on data transport including L1 and L2 functionalities with several data mapping options.

CPRI, probably due to its TDM (Time Division Multiplexing) and open nature, is more diffused than the OBSAI RP3 standard, which is based instead on a packet concept derived from the Nokia internal semi-proprietary implementations. This simplicity property of CPRI allowed a much faster penetration in the market compared to OBSAI RP3, along with some key features enabling slightly higher carrier capacity. The drawbacks of CPRI are the large number of data mapping options and the complexity that is involved in providing carrier routing and automated network management, which drawbacks are the essence of the Open Radio Interface (ORI) initiative from operators, which is introduced in the next section.

## Open Radio Interface - ORI

The Open Radio Interface (ORI) [56] and [26] is a very recent ETSI initiative started in 2010 and leaded from operators to complement the CPRI standard with a fully open and standardized Control & Management (C&M) flow definitions. ORI is based on the previous Open Base Band to Radio Interface (OBRI) work made from the NGMN group. It is potentially a low cost and truly open C&M flow definition for the internal eNb radio management. Mobile communication networks have evolved from their's second generations and now, many operators are preparing to introduce LTE as the 4G standard. Economical and efficient deployment of base stations is one of key issues for the success of mobile services. Operators also consider ecological aspects when renewing a system.

Current interfaces between BBU and RRH are provided in a semi proprietary nature, although based on industry standards like CPRI or OBSAI. In order to gain flexibility operators are looking for distributed base station architectures with separate BBUs and RRHs. In order to gain interoperability, BBU and RRH preferably should adopt ORI for radio system management. ORI is built using CPRI as sublayers complying with CPRI specification version 4.1 of

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CPRI forum. Recommendations C&M aspects to enable open BBU-RRH interface, which are not specified in the CPRI specification, are defined. ORI focuses on 3GPP radio access technologies like UTRA-FDD, E-UTRA-FDD and E-UTRA-TDD and considering also multiplexing between UTRA-FDD and E-UTRA-FDD. Addition of multi carrier GSM will also be included later from ORI.

ORI mainly defines the *Ir* interface in the LTE radio access network, including specification of the following requirements:

- Function requirements
- Capability requirements
- Service requirements
- Interface requirements
- Operational & maintenance requirements
- Mechanical & environmental requirements
- Synchronization requirements
- Power & grounding requirements

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## Appendix D

# Example of RP3-01 System Start-up Sequence Diagrams

### OFF STATE

In the OFF state the RP3-01 TX FSM of the LC/BBM is in TX OFF STATE. The state is initially set by reset. Frame data is not transmitted or received. The RRU is also not sending frames. At the RRU, the frame structure transmission state is following the state of the received signal. The RRU reset state is TX OFF STATE.

The state transition to the INIT STATE should be initiated as soon as the system has completed startup. The INIT STATE is an initialization state, where the transmitter and the receiver is configured as preparation for the transmission of the air interface frames. All configurations, line rate auto negotiation algorithms and delay measurements should be completed before the state transition to the SYNC STATE. The system configuration, number of SFP links is external configuration to the interface. The system should hold such information in its registers in-order of having an working system start-up sequence. Fig.D.1 is informative and shows one example of handling the transition to the Init State.

### INIT STATE

#### RRH Configuration

When link and RRU have been correctly initialized, the BS can initiate to send DL data and to receive UL data from RRU. This is shown in Fig.D.2.

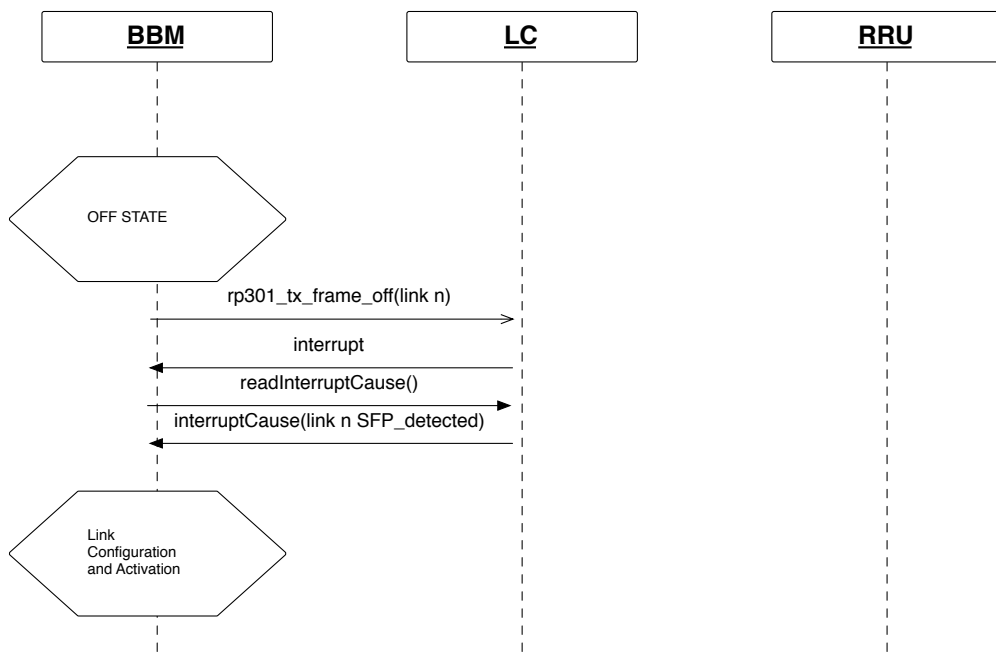


Figure D.1: OFF State. Transition to Init state

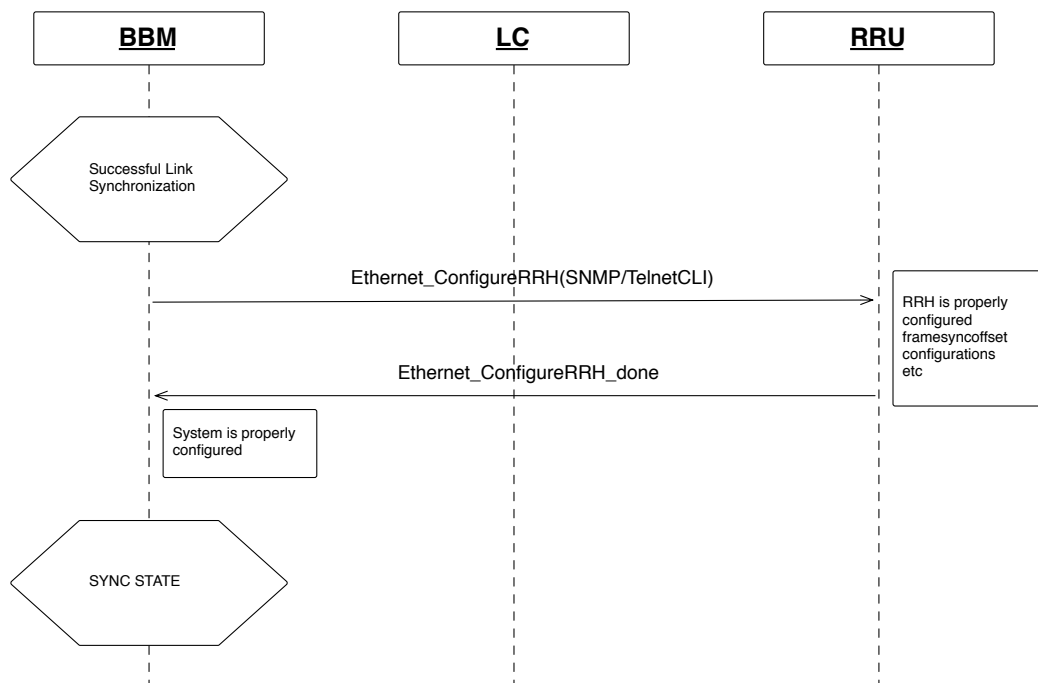


Figure D.2: RRU Configuration



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## SYNC STATE

When link and RRU have been correctly initialized, the BS can initiate to send DL data and to receive UL data from RRU. This is shown in Fig.D.3.

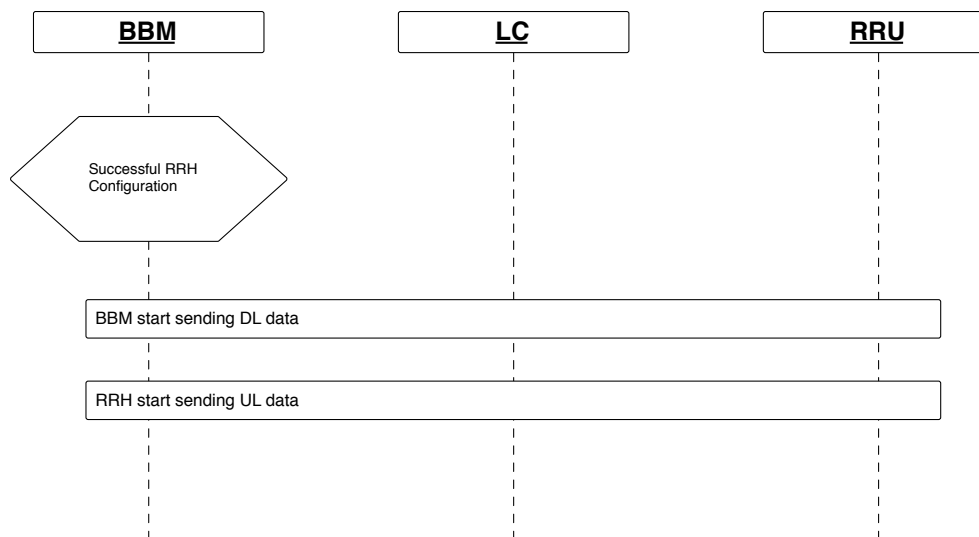


Figure D.3: SYNC state definition

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## Appendix E

# Clock Distribution in Multi-Hop Radio Applications

The discussions in this chapter are based on the work done from the Author in collaboration with M. Hoegdal and G.Bergamo from Radiocomp ApS and presented in:

- "Analysis of clock distribution and delay management for IMT-Advanced distributed wireless base station systems" [1]
- "Analysis of clock distribution and delay measurements for multi-hop remote radio applications" [2]
- "C. Lanzani, *Single and Multi Hop CPRI Interface Applications using Radiocomp's CPRI v.4.1 IP Core*. Radiocomp ApS, [www.radiocomp.com](http://www.radiocomp.com), v.1.4 ed., May 2009" [11]
- "C. Lanzani and et al., *CPRI v.4.1 IP Core User Manual*. Radiocomp, [www.radiocomp.com](http://www.radiocomp.com), v.2.3 ed., September 2010" [12]

## Overview

This section analyzes the clock recovery and delay measurement blocks when applied to single-hop and multi-hop RRH applications, the latter representing the worst-case scenario delay and clocking performance wise. The section analyzes the clock recovery PLL blocks in a single-hop connection and we present a simulation model for cascaded PLLs and the achieved results. Multi-hop connections consist of a REC subsystem connecting one or more master ports to two or more RE subsystems in chained configuration. We will limit the discussion to a topology using only two RE nodes in a chained configuration for convenience. The concept will apply

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to configuration with more than 2 hops as well. The first RE (RE#1) has a single slave port and a single master port. The second RE (RE#2) has a single slave port only. RE#1 is also known as a "networking" RE configuration. When a RE sub-system is used into a "networking" application, there may be a "simple" solution and a "general" solution. In the "simple" solution will be analyzed in this section and it consists of an RE having one slave port and one master port that are both using the same line bit-rate. In the "general" solution, an RE is characterized by that it may have several slave ports and several master ports and in principle different line rates between the slave port and the master port but it is not considered here since it is an unpractical setup.

More complex applications require a vendor-specific management system for the delay management, and they require external routing controlling blocks connected to an AUX interface and how to configure the frame timing to match the CPRI specification requirements. Measurement and control of the delay is required for appropriate recovery of the synchronization references and system configuration.

## Clock Distribution Analysis

The modular eNB concept is highlighted in Fig.4.14 showing the eNB and the RRHs in a multi-hop network topology. Each serial interface acts as a point-to-point (P2P) link with a master port and a slave port for each node (also called hop). The economical attractive RRH approach introduces challenge though. A clean, precise and stable clock signal must be provided to the AD, DA and carrier frequency generation blocks as frequency and phase reference for each node. Such clock reference serves as source for the frequency synthesizers, which must generate the radio (RF) carrier frequencies within a  $\pm 0.05ppm$  limit [80, 81, 82]. Specifically the quality of clock highly affects the performance of a sampled system, e.g., AD and DA, contributing to the overall *SNR* [83]. IMT-Advanced candidate technologies such as 3GPP Long Term Evolution (LTE) and LTE-Advanced are based on OFDMA schemes in the in downlink, and thus particularly sensitive to time variations since they utilize time and frequency synchronization [84]. Importantly, the error vector magnitude (EVM) requirements can be as low as 2.8% for complex modulation formats like 64 – *QAM* for mobile WiMAX 802.16e-2005. The EVM suffers with the effects of its clock reference and such frequency variations are often referred to as phase noise in RF designs. In wireless access eNBs the air-interface access can be TDD or FDD. The TDD mode specifically requires accurate synchronization of frame timing over time to ensure that multiple radio nodes can access the downlink and uplink portion of the airframe simultaneously. This is normally achieved by providing each eNB with a GPS derived reference delivering a master clock frequency reference (10MHz) and a timing reference (1PPS).

Wireless communications for the mobile access require a very accurate system clock. However, an excessive phase noise may lead to adjacent channel interference thereby jamming the neighboring subcarriers. The performance can be measured with BER (Bit Error Ratio) parameter, which is associated with the phase noise of the receiver [85]. Consequently, in RRH modules, clock accuracy in terms of phase noise plays a prime role and the clock circuitry design must be carefully considered since the clock reference is recovered from the bit transitions of the serial received OBSAI or CPRI link. Both interfacing standards define in fact a serial protocol communications, which on the physical layer or Layer-1 (L1) share the same architecture and functional blocks supporting a number of serial baud rates according to the demanded system carrier capacity. Due to the remote nature of the RRH, a clock recovery scheme as shown in Figure E.1 is required. This is opposed to a direct clock source scheme used in traditional centralized base station solutions where the accurate clock reference is delivered over, e.g., a chassis backplane. The serial link is realized by use of generic MGT (Multi Gigabit Transceivers) technology.

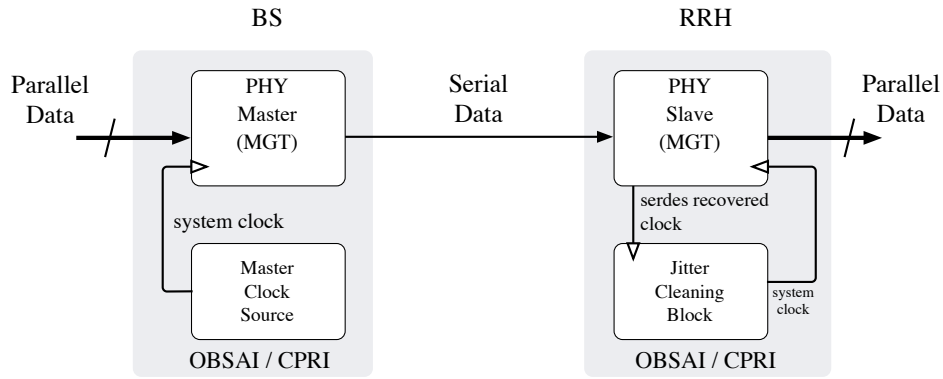


Figure E.1: Clocking architecture between Master / Slave ports in the parallel to serial / serial to parallel conversion

The central clock for frequency generation in the radio module is synchronized to the bit clock of the serial link acting as the slave receiving port. CPRI specifies that, with the use of 8B/10B line coding scheme, the bit clock rate of the interface shall be a multiple of  $38.4MHz$ , to allow a simple synchronization mechanism and frequency generation [5]. Moreover, the reference point for the jitter and phase noise specification is a stable clock signal at the service access point (SAP), which is the interface master clock input. We note that OBSAI RP3 also specifies that 8B/10B transmission coding over the link must provide a mechanism for serialization and clock recovery. For both CPRI and OBSAI, the performance is measured in terms of BER, where OBSAI RP3 states a BER of  $10^{-15}$ , while CPRI states a BER of  $10^{-12}$  respectively. In terms of clock requirements, the CPRI specification refers to the mobile specifications [80, 81] in order to justify the GPS based timing mechanism in the eNB side. This also imposes that

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the way the frequency accuracy is transferred to the RRH is signified by the phase noise of the recovered clock from the high-speed serial link. In other words, the system clock of the RRH has to be the recovered clock from the high-speed serial link and, at the same time, it must keep the accuracy of the clock from the eNB. The equation used for modeling this aspect relies on the phase noise of the recovered clock and must meet the equation below:

$$\frac{\Delta f}{f_0} = \frac{1}{f_0} * \sqrt[2]{\int_0^{f_{cut}} f^2 * 2 * 10^{\frac{L(f)}{10dB}} df} \quad (E.1)$$

where  $\Delta f$  is the total rms frequency deviation in a defined bandwidth used to specify the frequency stability of an oscillator. The frequency  $f_0$  is the system clock or reference frequency in the remote radio, thus the recovered and stable clock. The cut-off frequency  $f_{cut}$  is  $300MHz$  and it sets the bandwidth range within which the single-sideband phase-noise  $L(f)$  (in  $dB$  or often  $dBc$ ) is evaluated.

$$\frac{\Delta f}{f_0} \leq \pm 0.002ppm \quad (E.2)$$

$f$  is the offset frequency from the reference frequency,  $f_0$ . Normalizing by  $f_0$  extends it to any chosen reference frequency. The cut-off frequency of  $300Hz$  is chosen so that a standard crystal oscillator suffices as reference clock of the remote radio [24]. In order to fulfill the stringent standard requirements, the traditional mobile base station often uses precise clock sources that have the accuracy in the range of BER  $10^{-11}$  meeting ITU-T G.811 and ANSI Stratum 1 performance levels. Such precision level could be obtained by using GPS disciplined OCXOs [86]. As a consequence, RRHs employ clock data recovery (CDR) circuits and consist of a PLL and a decision circuit [87]. The PLL recovers the clock from the incoming data stream and the decision circuit determines the sampling point dynamically based on the signal transitions. The 8B/10B encoding guarantees sufficient amount of bit transitions in order to safely recover the clock. In order to estimate the returned clutter power two main aspects have to be taken into account: the type of the environment and the terrain shape. The type of environment is accounted for by using different clutter models the most common being the semi-empirical and the statistical clutter models.

## Clock Distribution Model

On the eNB side, the GPS timing master source drives a clock synthesizer, which does the clock distribution feeding the PLL of the SerDes transmitter. Thus, it can be seen as a chain of two PLL as shown in Fig.E.2. To build a real model of the system the following commercial components were chosen. The GPS disciplined oscillator module is the C6350A1-0002 from Vectron, which is able to provide a  $10MHz$  clock source with  $10^{-12}$  of accuracy when locked to

a GPS system. A high performance clock synchronizer (CDCM7005) from Texas Instruments (TI), which is combined with a Silabs Si550 VCXO and a third order loop filter, realizes the PLL for clock distribution. The CDCM7005s output clock feeds the input for the serializer TX PLL. The serializer component is the Altera FPGA Stratix IV GX device with embedded transceivers. Note, state-of-art SerDes cores are normally designed with dedicated PLLs for high-speed serial transceivers. The Stratix IV device produces the streamed output data at  $3072\text{Mbps}$ , delivering it to an electrical-to-optical transceiver (SFP not shown in Fig.E.3) before reaching an optical fiber. Likewise, the remote radio behavior is modeled as a chain of PLLs. The CDR is the first PLL, which delivers a recovered clock to the second, a Jitter Cleaner PLL. This PLL has the important task of jitter removal by employing a very narrow loop bandwidth. After this stage, the clock quality must meet the CPRI/OBSAI specification and serves as a system clock for the remote radio and the next hop as SerDes transmitter PLL reference clock, as in Fig.E.4. Again, CDR and SerDes functionalities are carried out by the FPGA integrated transceiver and a CDCM7005, Si550 VCXO with third order loop filter play the role of Jitter Cleaner PLL. The tool used to model is provided from TI, TI-PLL-Sim, which is built based on National Instruments LabVIEW. This tool allows modeling and evaluating the performance of PLLs. It offers the possibility of specifying key design parameters such as VCXOs tuning slope, both reference clock and VCXOs phase noise vectors, loop filter characteristics, frequency dividers/multipliers, charge pump current and so forth.

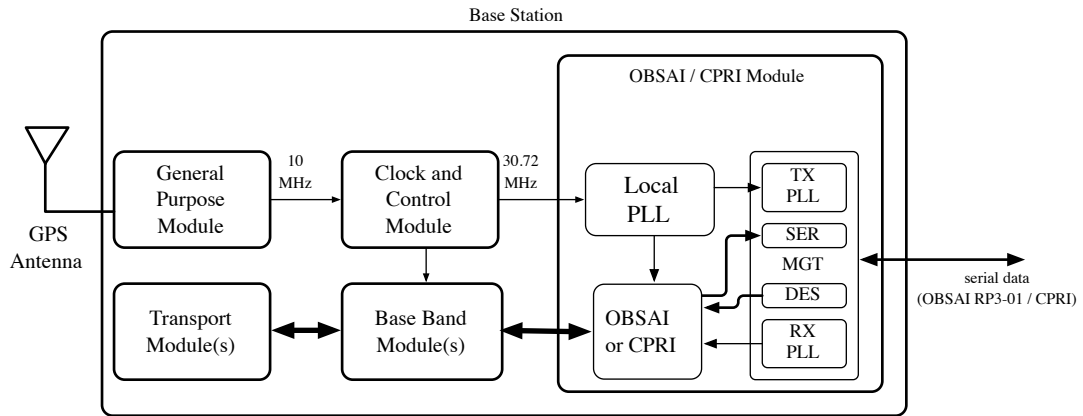


Figure E.2: Clock system architecture in eNb LC/REC module

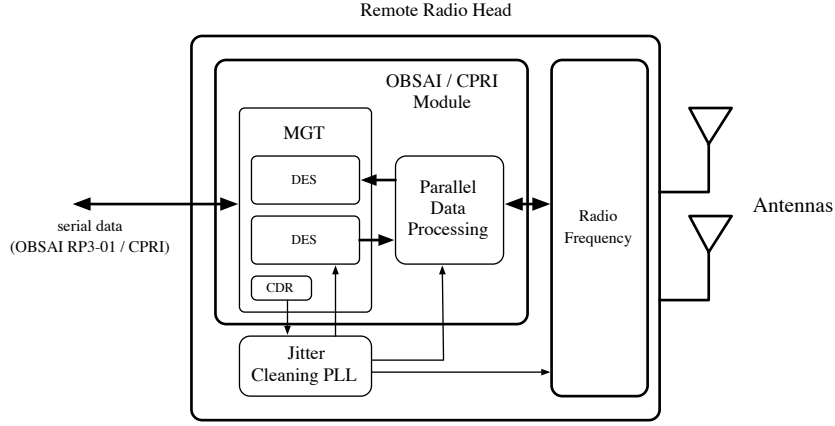


Figure E.3: Clock system architecture in eNb RRU/RE module

The proposed framework analyzes the clock quality based on the PLLs phase noise curve. So, for each PLL, there are two phase noise curves, one corresponding to its input reference clock and another for its VCXO. At the PLL output, the resulting phase noise curve serves as input for the next PLL. An offset frequency and a power level from the reference clock compose each phase noise curve. For instance, the base station  $10\text{MHz}$  reference clock has the phase noise curve shown in Fig.E.4 below:

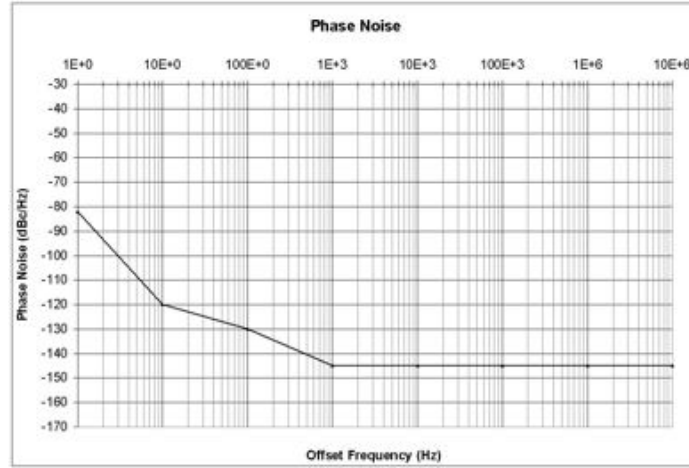


Figure E.4: Phase noise curve of Base Station 10MHz Ref Clock [4]

It is worth mentioning though that phase noise curves for different clock frequencies are not straightforward comparable. According to [82], an equation must be employed in order to bring the phase noise from reference frequency to another and then compare both the phase noise curves at the same reference frequency.

## Modeling results

In terms of results, the tool gives relevant PLL characteristics such as open and closed loop curves, phase margin, loop bandwidth, gain peaking, PLLs phase noise curve and the periodic RMS jitter. Fig.E.5 shows the results of PLL calculations using TI-PLL-Sim tool. It verifies a good PLL stability due to the phase margin of 87 and a very low jitter transfer due to a gain peaking of only 0.05dB. Fig.E.6 illustrates the PLLs output phase noise evaluation (dashed line curve). It shows that, even though, PLLs phase noise seems dominated by the VCXOs phase noise a considerable amount of phase jitter is attenuated in the higher phase noise range, the closest offset from the carrier ( $1 - 100Hz$ ). The circuit shows a reduction from 11ps to 3.3ps in the jitter considering a  $1 - 10MHz$  bandwidth.

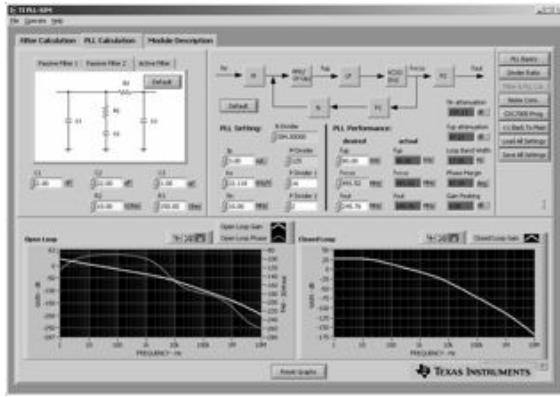


Figure E.5: TI-PLL-Sim tool - PLL calculation

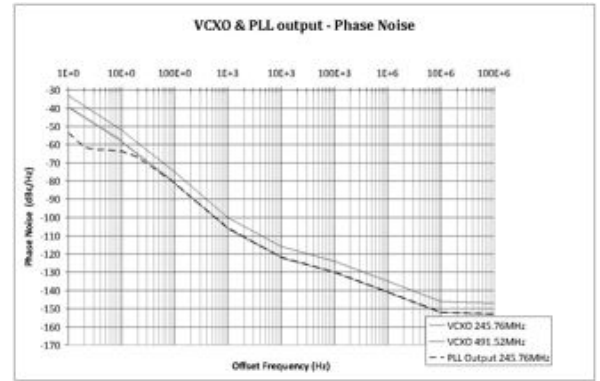


Figure E.6: PLLs phase noise evaluation curves

In the next stage, this clock is driving the serializers transmitter PLL, in this case, the Altera Stratix IV GT. TX PLL model is built based on the phase noise characteristics for its voltage-control ring oscillator ( $-94dBc/Hz$  at  $1MHz$ ) and a RMS jitter ( $180MHz$ ) at  $1.08ps$ , found in [88], as well as, the jitter transfer curves from [64]. However, this model suffers some limitations due to the lack of complete information. The simulation estimates that the embedded clock in the line bit rate of 3072 Mbps has around  $66.8ps$  of jitter, which corresponds to  $0.21UI$  of the line bit rate period. Therefore, it is less than  $0.35UI$  stated in CPRI [24]. Another assumption is that the channel does not degrade considerably the clock quality, due to the possible equalizer compensation and to the close distance between optical-to-electrical transceiver and FPGA chip. Hence, CDR input receives an equivalent clock with  $0.21UI$  of jitter as depicted in Fig.E.7 where it is also shown the phase noise curve for recovered clock running at  $76.8MHz$ . This clock drives then the Jitter Cleaner PLL. The model confirms that the Jitter Cleaner PLL removes a significant amount of jitter, as its phase noise levels show in Fig.E.8. It is even more evident the clock quality when it is compared in Fig.E.8 with a Figure of Merit device, which is designed to recover the clock for the CPRI link.



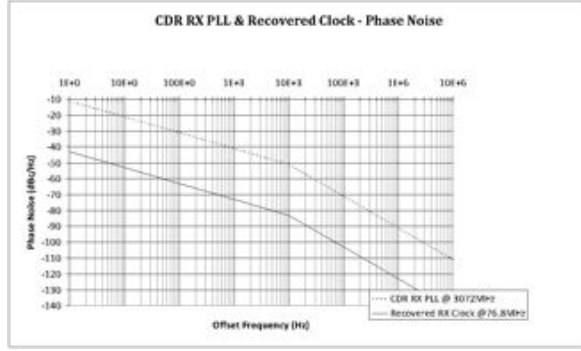


Figure E.7: CDRs phase noise evaluation curves

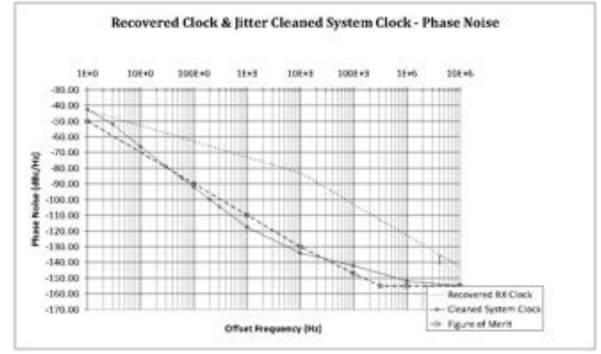


Figure E.8: Recovered Clock, Jitter Cleaned Clock and Figure of Merit - phase noise evaluation curves.

Thus, based on the phase noise curve obtained, it is possible to compute the value of Equation 1. The obtained value  $\frac{f}{f_0} = 0.001ppm$  demonstrates that this clock meets the CPRI requirements [10] and can be used as a system clock in the remote radio. For the next remote radio in the hop, the simulation foresees that CDR combined with Jitter Cleaner PLL obtains the same results shown in Fig.E.7 and Fig.E.8. Considering multiple hops, the way to determine jitter accumulation can be estimated via the jitter transfers [89]. However, as the Jitter Cleaner PLL acts as low jitter local source, it retimes the clock and practically resets the jitter budget. It achieves that by having a gain peak of  $0.05dB$ , permitting several remote radio hops. For instance, in synchronous digital hierarchy technology, the repeaters equipment must comply within a  $0.1dB$  gain peak in order not to add substantial jitter to the link. Hence, by comparing the two gain peak values, it is possible to interpret that the multi-hop can be extended for many hops and the accumulated jitter is given by the small fraction of the jitter transfer. Practically, measurements will be carried out in the near future in order to confirm the simulations.

## Jitter in multi-hop configurations

When looking at the jitter in a multi-hop configuration we can roughly divide the jitter into two contributions:

- Accumulated jitter within the Jitter Cleaner PLL loop bandwidth of the RRH
- Jitter outside the Jitter Cleaner PLL loop bandwidth

The jitter outside the Jitter Cleaner PLL loop bandwidth is determined only by the jitter-cleaned clock. Assuming identical jitter gains and Jitter Cleaner PLL loop bandwidths of the RRHs in a multi-hop configuration we can express the total jitter inside the Jitter Cleaner PLL loop bandwidth in a multi-hop configuration at the  $n^{th}$  RRH,  $J_{tot}$ , as:

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$$J_{tot} = J_b * G_j^n \quad (\text{E.3})$$

where  $J_b$  is the jitter generated by the Base Station in the frequency band inside the Jitter Cleaner PLL loop bandwidth, and  $G_j$  is the jitter gain in the Jitter Cleaner PLL of the RRH. It can be seen that as the number of daisy chained RRHs increase the requirements to the jitter generated by the Base Station increases accordingly. If we, as a worst-case assumption, assume that the total jitter is only contributed by the jitter inside the Jitter Cleaner loop bandwidth then we can calculate the number of RRHs that we as minimum can daisy chain. With a jitter gain of  $0.05dB$  as found above and a peak-to-peak jitter that correspond to  $0.21UI$  for one RRH we can at least daisy chain 44 RRHs before reaching a peak-to-peak jitter corresponding to  $0.35UI$ .

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## Appendix F

# CPRI and RP3-01 Synchronization and Delay Background

OBSAI RP3 and CPRI interfaces differ from traditional telecom standards not only on being tighter on clock accuracy requirements, but also by imposing strict conditions on the delay measurement accuracy of the data path to enable sufficient margin absorbing further unavoidable inaccuracies in the RF portion of the system.

The reference for delay measurement is the frame boundary identified by its specific comma characters from the 8b10b coding block. CPRI frame boundary is identified from the K28.5 comma character, while RP3-01 frame is identified from the K28.7 character.

When it comes to serialization, an accurate delay measurement is not supported by traditional telecom serialization devices since in these applications delay knowledge it is not required. The delay measurement features refer to L1 and shall be part of the so called Physical Coding Sub-Layer (PCS) block; functions as comma alignment, byte alignment and synchronization buffer level, as well as phase difference knowledge between the receiver recovered clock and the system clock are often not able to report their internal delay value. These delays are variable at every start-up of the link if they are not measurable, inaccuracy is thus introduced at the receiver path. In multi-hop applications the inaccuracy is additive at every hop resulting to easily exceeding the budget defined from the CPRI specification and typically in the order of 8.16 ns [24].

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## Base station delays definitions

### Downlink path delays

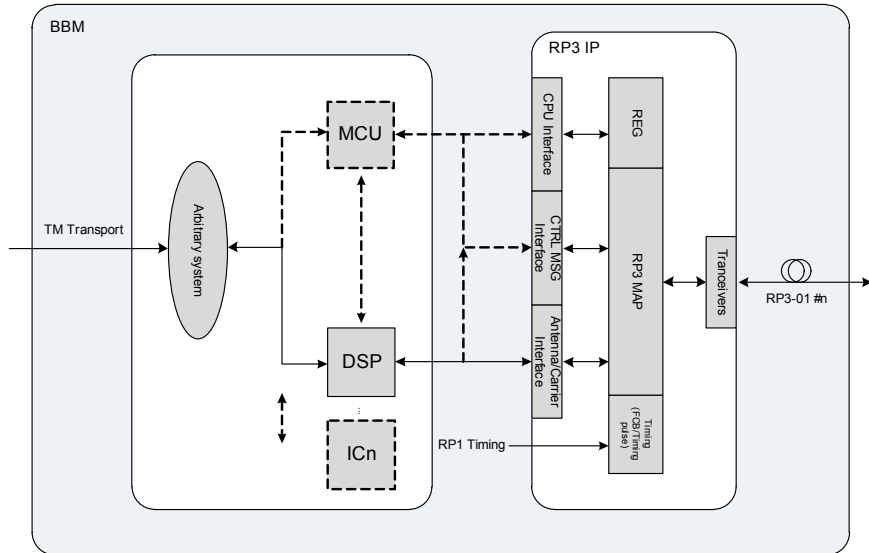


Figure F.1: Conceptual BBM internal synchronization architecture.

- The interrupt processing delay is a delay that is caused by the time consumed to serve the internal timer interrupt or the external buffering threshold interrupt. Some overhead should be added for generic processing delay at the DSP/MCU.
- The DSP Read/Write Delay is the delay that the DSP requires to serve the buffering threshold interrupt generated by the OBSAI block. The delay is variable delay, where the worst-case delay should be used for calculating the used timing overhead for the buffer read/write operations. The DL path delay i.e. the DSP write operation is the most critical from the timing point-of-view.
- The Clock Domain Crossing Delay is an optional delay. The clock domain crossing delay applies when the DSP interface clock rate or the DSP interface clock phase is different than the used internal clock at the controller block. The delay variation depends on the used clock rates. The clock domain crossing worst case delay should be used for calculating the timing overhead for the buffer read/write operations.

- The buffering threshold is an optional delay. When buffering threshold is enabled, the controller block will generate sequential interrupts that are triggered when the transmission or reception buffers have reach a certain limit of the amount of received samples or the amount samples left to be sent through the RP3-01 line.
- If threshold levels are not used, the DSP should keep track of the timing by using sequential timer interrupts of the read and write operations in-order of avoiding any buffer over- or underflow. The buffering threshold delay value should be significantly higher than the DSP Read/Write delay, clock domain crossing delay and interrupt processing delay combined.
- Transceiver delays are caused by the delays within the interface controller block and the delay in the fibre. The transceiver delays are the first point of concern when appropriate delay management is implemented in the BBM Unit.

## Uplink path delays

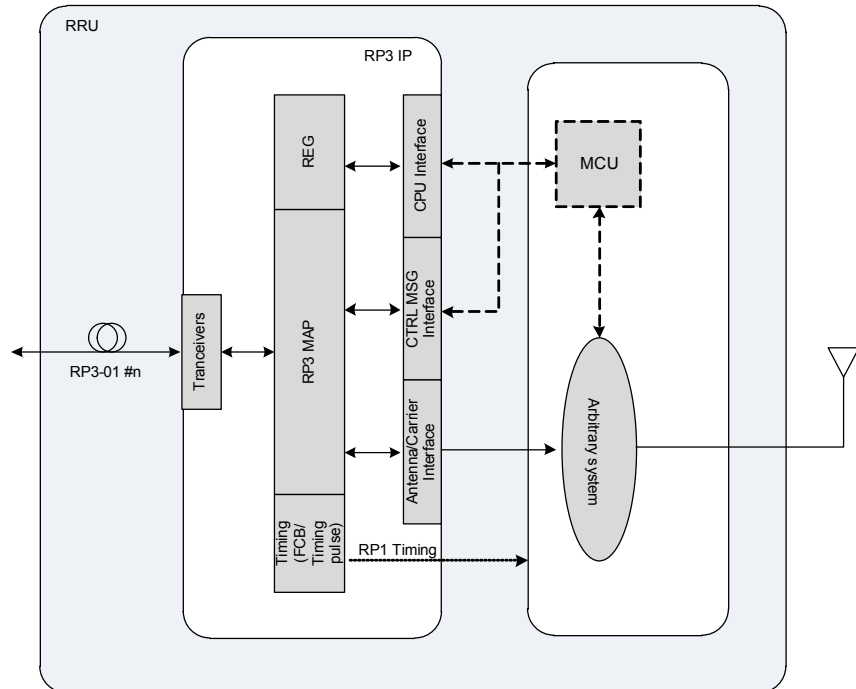


Figure F.2: Conceptual RRH internal synchronization architecture.

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- The interrupt processing delay is an delay that is caused by the time consumed to serve the internal timer interrupt or the external buffering threshold interrupt. Some overhead should be added for generic processing delay at the DSP/MCU.
  - The DSP Read/Write Delay is the delay that the DSP requires to serve the buffering threshold interrupt generated by the OBSAI block. The delay is variable delay, where the worst-case delay should be used for calculating the used timing overhead for the buffer read/write operations. The DL path delay i.e. the DSP write operation is the most critical from the timing point-of-view.
  - The Clock Domain Crossing Delay is an optional delay. The clock domain crossing delay applies when the DSP interface clock rate or the DSP interface clock phase is different than the used internal clock at the controller block. The delay variation depends on the used clock rates. The clock domain crossing worst case delay should be used for calculating the timing overhead for the buffer read/write operations.
  - The buffering threshold is an optional delay. When buffering threshold is enabled, the controller block will generate sequential interrupts that are triggered when the transmission or reception buffers have reach a certain limit of the amount of received samples or the amount samples left to be sent through the RP3-01 line.
  - If threshold levels are not used, the DSP should keep track of the timing by using sequential timer interrupts of the read and write operations in-order of avoiding any buffer over- or underflow. The buffering threshold delay value should be significantly higher than the DSP Read/Write delay, clock domain crossing delay and interrupt processing delay combined.
  - Transceiver delays are caused by the delays within the controller block and the delay in the fibre. The descriptions of the delays that are caused by transceivers are in the following chapters. The transceiver delays are the first point of concern when appropriate delay management is implemented in the BBM Unit.
  - The delays of RRH unit should be also handled in the BBM unit. For setting up the BBM unit it is not enough to handle only the BBM unit internal delays. The delays of RRH unit should also taken into account when Delta and Pi values are set for the system. The delays of the RRH unit are always system specific and they should be known before

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setting up the BBM unit.

- The generic top-level architecture of the RRH unit consists of external interfaces to the BBM Unit and the antenna(s). In this section, the synchronization issues are concentrating to the delay setup of the BBM unit, however there are certain delay aspects that should be recognized from the RRH unit point-of-view for the setup of the system timing.
- The RRH unit use an approach where timing information is received by the remote unit by an dedicated FCB message. The message contains information that can be used for regeneration of the timing pulse within a remote unit. The recovered timing pulse will be used for timing of the UL direction RP3-01 transmission and for timing of the IQ sample transmissions to the air interface.
- The timing pulse can be accurately reconstructed based on the received FCB message from the BBM Unit after the RTT delay has been measured and when the delay has been compensated at the reconstructed timing pulse. The Timing pulse and the delay management principles in the RRH unit is identical to the timing pulse and delay management principles at the BBM unit. The Delta delay and the Pi measurement principles that are described earlier in this chapter applies also for the RRH unit.

## CPRI Delay Requirements

CPRI [24] defines the delay and synchronization management in the following sections:

- [24] Section 3.5 Synchronization / Timing
- [24] Section 3.6 Delay Calibration
- [24] Section 6.1 Delay Calibration Example
- [24] Section 6.3 Networking

The CPRI specification [24] section 3.5 and 3.6 contain a number of delay accuracy requirements which mostly relate to the physical layer functions. Specifically R-17, R-18 and R-18A as defined in [24] section 3.5.1 define jitter and frequency accuracy for generation of the central RE clock used for Radio transmission. The clock synchronization for RE will typically be performed using an external PLL with crystal VCXO, while for REC the clock will typically be provided

from a OCXO reference common to all base station sub-modules. Requirement R-17 and R-18 in [24] section 3.5.1 defines jitter and frequency accuracy for generation of the central RE clock used for Radio transmission. These requirements are not directly related to the CPRI controller module as it does not include any PLL or clock generation circuitry.

Requirement R-19 in [24] section 3.5.3 it is related to the receive delay budget and it imposed that inaccuracies shall be avoided. Overall requirements R-19, R-20 and R-21 [24] relates to the variable delay in the receive interface. Round Trip Time (RTT) delay, as a measure of the time between the transmitted and received frame byte boundary, requires knowledge of the transmission and receiving paths delay components. The reference measurement points at the serial transceiver ports input / outputs are defined so that can be assumed that half of the delay is downlink and other half is uplink optic cable delay. The requirements R-19 and R-21 [24] define the highest measurement accuracy for the link as low as to  $\pm 8.138ns (= \pm \frac{T_C}{32})$ .

At the RE side, the clock frequency recovery remains stable enough though the drifting, meaning that relative timing is stable, but absolute timing may be shifting. Assuming a simple case when one REC transmits to a RE using TX diversity or MIMO, multiple antenna carrier data streams are received through one link the drifting does not have effects to the relative timing requirement of  $\frac{T_C}{4}$  period time, which is then reduced by eight in the specification to allow other inaccuracies at the antenna path i.e.  $\frac{T_C}{32}$ .

## CPRI Reference Point Definitions

The definition of the reference points for the measurement is important in order to ensure correct interoperability between different implementations. The reference points for cable delay calibration are the input and the output points of the equipment, i.e. the connectors of REC and RE as shown below the single-hop configuration. In a single hop configuration the reference points are defined as below in Fig.F.3 and in Fig.F.4: taken from [24]:

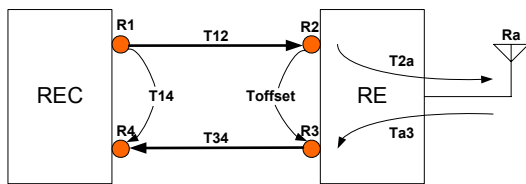


Figure F.3: Single-Hop CPRI frame timing reference points [24]

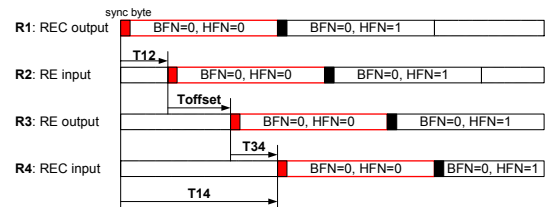


Figure F.4: Single-Hop CPRI Frame Timing Diagram [24]

The  $T_{12}$ ,  $T_{34}$ ,  $T_{14}$  and  $T_{offset}$  delays can be calculated according to the formulas defined in the next sections. It is here assumed that the approximation of  $T_{12} = T_{34}$  is valid. It may



be not straightforward to measure the frame timing at R1/R4 or R2/R3 directly because the signals at these points are optical or electrical high speed signals and may require expensive measurement equipment, however it is feasible to measure the timing difference at the SAP(s) in REC/RE and to compensate the internal timing difference between measurement points and R1/R4, RB2/RB3, RB1/RB4, R2/R3 manually by the middleware O&M layer. The frame timing in a multi-hop is more complex and the in a REC-RE-RE configuration the reference points are defined as below in Fig.F.5 and F.6:

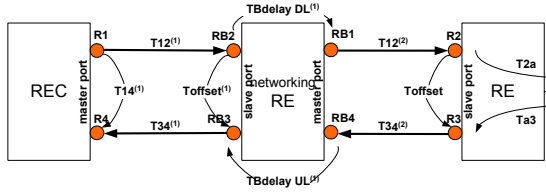


Figure F.5: CPRI REC-RE-RE Delay measurement reference points [24]

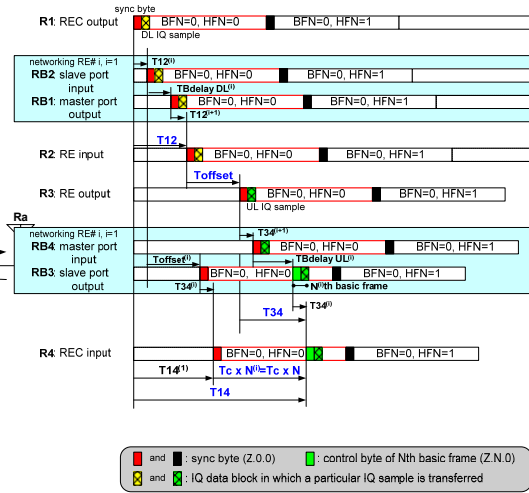


Figure F.6: Relation between downlink and uplink timing in a multi-hop configuration [24].

## RP3-01 Synchronization and Delay Requirements

In 3GPP LTE both FDD and TDD operations are supported and the radio frames are defined having a length of 10ms. The 10 ms reference can be locked to a centralized timing reference normally derived from the core network transport infrastructure or alternatively from the GPS 1 pps reference or to the eNb system frame number reference.

- Radio frame timing it is used from the BTS to generate OBSAI RP3-01 and CPRI frames of 10ms. RP3-01 and CPRI frame timing is used for the following operations
- Delay measurement of optical fiber cable with RTT procedure as described in RP3 and CPRI standards
- Local radio data path delays from serdes to antenna (DL) and from antenna to serdes (UL)

- 
- Data alignment between different channels in either the same RRH or separate radio nodes (synchronized buffering using RP3 timestamp or CPRI HFN references)
  - Data alignment between I and Q branches within the same channel (required for MIMO operations in both DL and UL)
  - DSP processing requirements for data alignment
  - DL/UL ratio in TDD

In OBSAI mode of operations, RP3 and RP1 standard definitions are used. There shall be at least one OBSAI RP3-01 full-duplex optical link between the LU and each RRH. The LU functionality is often included into the BBM module via a companion FPGA and high-speed transceivers (FPGA internal or external).

Each RP3-01 optical link carries RP3 data messages (containing I/Q sample pairs of radio carrier(s)), RP1 Ethernet and RP1 FCB synchronization messages in RP3-01 format, as well as RP3-01 synchronized control messages such like RTT and loopback and Virtual Hardware Reset.

The BS timing and clock frequency reference is a GPS coming from a GP (General Purpose) module in the BS via RP1 interface as indicated in the OBSAI System Reference Document [25].

RP1 timing references are required from the BS system to ensure that:

- Air access operations in TDD mode between different BS or between different sectors of the same BS will not overlap each other causing unwanted interference and destroying data communications between MS and BS.
- Clock and radio frame synchronization between BBM/LU and RRH can be obtained irrespectively of the distance over the fiber.
- Accurate frequency synchronization of the carriers will be enabled ensuring easier handover and PLL lock between MS traveling from one sector to another.
- Measurement functions of gain control can be synchronized with frame timing if required.

The eNb radio frame timing reference is a 1 pps (pulse per second), which triggers the generation of the RP1 [57] frame clock burst synchronization packets as defined in [RP1] Section xx. RP1 FCB packets required shall be RP3 TYPE (10ms), WiMAX TYPE (5ms) or LTE TYPE (10ms). In addition other types of FCBs shall be generated from CCM, however not necessarily being synchronized with the reference from GPS. Such FCBs shall be:

- RP3 TYPE (0x1) indicating the 10ms RP3 Bus frame reference (locked to radio frame or free running) [57].
- ToD TYPE (0x8) indicating the Time of the Day as specified in [57] (optional).

In OBSAI RP3, the algorithm that enables transfer of RP1 Frame Clock Burst synchronization packages is defined in [5]. This algorithm enables to recover the radio frame timing into the RRH node without accounting for the impact of the one-way fiber propagation delay. The RTT (Round Trip Time) procedure described in the [5] enables the eNb to calculate the one-way propagation delay. This delay shall be communicated to the RRH, which will compensate the air-interface timing regeneration and thus ensuring that the radio frame timing will be aligned in both the eNb and RRH. This example is shown in Fig. F.7 below:

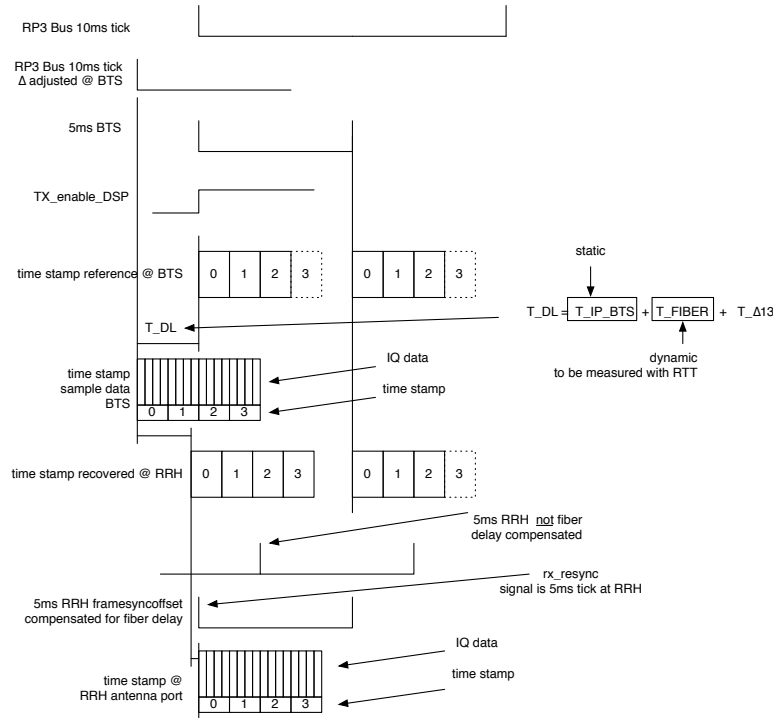


Figure F.7: RP3 FCB delay

In OBSAI RP3 specification [5], it is stated that all measurement shall be made with 1/614.4 MHz periods equivalent to 1.62 ns of resolution. Often in real implementations the selected implementation technology (often implemented in low and mid end FPGAs) does not support such high frequency for clocking the logic, and therefore the measurements are made with a lower divider ( $/2$  or  $/4$ ) of such frequency, and then the measurement is reported in 1/614.4 MHz resolution by scaling up the measured value depending on the scale factor. Therefore in order to ensure compliance to the above, real implementation shall target resolutions better or equal than 1.62 ns.

---

## DL Delay Measurement

For the main transmission path delays in BBM unit, refer to Fig.F.8. In the figure, there are four main sources for the delays in the transmission path at the BBM unit:

- Word alignment delay
- 8B10B Encoder delay
- Phase alignment delay
- Parallel to serial conversion delay

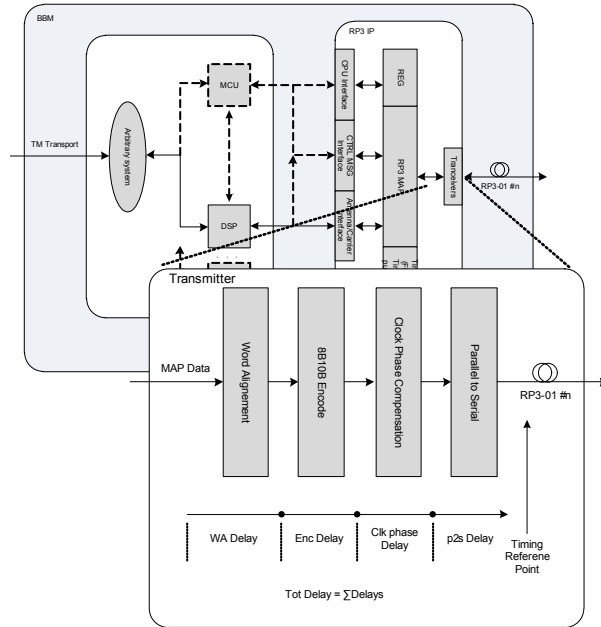


Figure F.8: BBM Transmission Path Delays

Where:

- the word alignment is optional, not commonly used in transmission paths.
- the clock phase alignment delay is optional, since the need of phase alignment buffering depends of the clocking structures and how deterministic the delays are between the core clock and the high-speed transmitter clock.

If the clock phase alignment is measurable, the phase of the output samples may be configured by using a bit shifting calibration block. Calibration in transmission enables bit level alignment of the IQ samples sent to the parallel to serial converter. The delay in the transmission path is

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the sum of the delays. The Delay is compensated by subtracting the total delay value from the RP3 Delta parameter i.e. The TX delay is calculated as it follows:

$$TX_{DelayBBM} = WA_{Delay} + Enc_{Delay} + ClkPhaseComp_{Delay} + p2s_{Delay} \quad (F.1)$$

and added to the total delay:

$$\Delta_{BBM} = -TX_{Delay} - \frac{RTT_{Delay}}{2} - RRH_{\Delta_{1,3}} - \Pi_{RRH} \quad (F.2)$$

Where:

$$RRH_{\Delta_{1,3}} = RRH_{IQDataBufferingThresholdDL} + RRH_{MAP2ANTDelay} \quad (F.3)$$

$$\Pi_{RRH} = RX_{DelayRRH} \quad (F.4)$$

$$RTT_{Delay} = \frac{RoundTripTime}{\left(\frac{8}{i}\right)} \quad (F.5)$$

and where:

$$i = LineRate, i1, 2, 4, 8 \quad (F.6)$$

$$RoundTripTime = MeasuredRTT_{Delay}(resolution614, 4MHz) \quad (F.7)$$

Notice that the delay values are different for each of the used line rates. Notice also that the delays does not include the delay produced by the IQ data transmission from the MAP buffers. The RP1 timing information may be used at the DSP/MCU in-order to achieve correct timing for transport to the IQ data buffers at startup of the IQ data buffering. The data buffers may then be configured to have a certain threshold values that enables a trigger for the DSP/MCU that may be used for initiating the transport to the IQ data buffers. This delay overhead should be calculated separately based on the used DSP/MCU data path delays and the overhead should be implemented to the DSP/MCU software.

Notify also that the transport path from the DSP/MCU to the IQ data buffers may contain clock domain crossing structures depending on the configuration and the clocking of the system. Clock domain crossings always produces variable timing of few clock cycles for each interface. If clock domain crossing is used between the MAP buffers and antenna branch then add the additional worst-case delay to the RRH buffering delay.

At the BBM/LC transmit configuration for the setting for the FCB message offset related to the transmit side delay is taken account by adding the transmit side delay to the Delta offset. At the RRH receive side the delay may be calibrated to a pre defined value. For the main receiver path delays in RRH unit, refer to Fig.F.9. In the figure, there are four main sources for the delays in the receiver path of the RRH:

- Serial to parallel conversion delay
- Phase alignment delay
- 8B10B decoder delay
- Word alignment delay

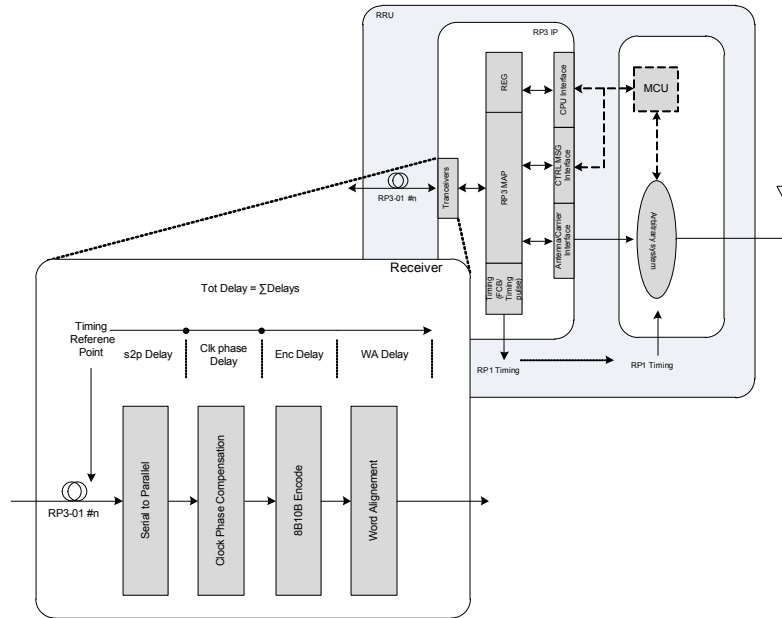


Figure F.9: RRH Receiver Path Delays

Where,

- the word alignment is optional.
- the phase alignment delay is optional, since the need of phase alignment buffering depends of the clocking structures and how deterministic the delays are between the core clock and the high-speed transmitter clock.

The clock phase alignment and the word alignment delays are usually variable delays within a system. The variable delay can be measured by using the extended delay measurement feature

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where the delay in the receiver path is the cumulative sum of the delays.

For the configuration of the OBSAI RP3-01 interface, the delay should be determined and compensated by the delay compensation parameters. The delay compensation parameter holds an value, where the delay resolution is in number of byte clocks.

Notify that the  $\Pi$  measurement is the reverse operation of the  $\Delta$  delay setting. In the  $\Pi$  measurement the receiver path the timing of the received RP3 frame is measured. The delay relative to the timing pulse is measured. The Delay is compensated by configuration of delay values:

- The delay is added to PI parameter
- The delay is added to RTT\_OFFSET parameter
- The FCB delay is added to FIBER\_RX\_DELAY parameter

For appropriate configuration of the OBSAI RP3-01 interface, the total delay should be determined and the delay should be compensated by the delay compensation parameter. The delay compensation parameter is a constant parameter for each individual system. The delay compensation parameter holds an value, where the delay resolution is a number of byte clocks. The delay in the transmission path is the sum of the delays. The Delay is compensated by subtracting the tot Delay value from the RP3 Pi parameter i.e. The RX delay is calculated as it follows:

$$RX_{DelayRRH} = WA_{Delay} + Dec_{Delay} + ClkPhoseComp_{Delay} + s2p_{Delay} \quad (F.8)$$

and added to the delay:

$$\Pi_{RRH} = -RX_{DelayRRH} - \frac{RTT_{Delay}}{2} - RRH\Delta_{1,3} \quad (F.9)$$

where:

$$RRH\Delta_{1,3} = RRH_{IQDataBufferingThresholdDL} + RRH_{MAP2ANTDelay} \quad (F.10)$$

$$RTT_{Delay} = \frac{RoundTripTime}{\left(\frac{8}{i}\right)} \quad (F.11)$$

and where:

$$i = LineRate, i1, 2, 4, 8 \quad (F.12)$$

---


$$RoundTripTime = MeasuredRTTDelay(resolution614, 4MHz) \quad (F.13)$$

Depending on the OBSAI configuration, the  $WA_{Delay} + Dec_{Delay} + ClkPhaseComp_{Delay}$  may be measured through the Extended Delay Measurement feature. The availability of the measurement depends on the system configuration. The serial to parallel conversion delay may be assumed as constant system specific delay that can be added to the measurement result. If the fibre delay is added to parameterparameter FIBER\_RX\_DELAY, then the following applies to the RRH unit Pi measurement configuration:

$$\Pi_{RRH} = -RX_{DelayRRH} - RRH\Delta_{1,3} \quad (F.14)$$

The delay value is communicated through higher layers after the RTT delay has been measured.

Notice that the delay values are different for each of the used line rates. Notice also that the delays does not include the delay produced by the IQ data transmission from the MAP buffers. The RP1 timing information may be used at the DSP/MCU in-order to achieve correct timing for transport to the IQ data buffers at startup of the IQ data buffering. The data buffers may then be configured to have a certain threshold values that enables a trigger for the DSP/MCU that may be used for initiating the transport to the IQ data buffers. This delay overhead should be calculated separately based on the used DSP/MCU data path delays and the overhead should be implemented to the DSP/MCU software.

Notify also that the transport path from the DSP/MCU to the IQ data buffers may contain clock domain crossing structures depending on the configuration and the clocking of the system. Clock domain crossings always produces variable timing of few clock cycles for each interface.

If clock domain crossing is used between the MAP buffers and antenna branch then add the additional worst-case delay to the RRH buffering delay. The above delay examples applies to the method where air interface timing is synchronized to the RP3-01 timing. If synchronized buffering method is used, then the timing of the air interface does not apply to the timing of the RP3-01 frame. In that case the RP3-01 interface may be setup separately without respect to the air interface timing. The synchronized buffering mode applies only to the RRH UL in the system.



## UL Delay Measurement

- Word alignment delay
- 8B10B Encoder delay
- Phase alignment delay
- Parallel to serial conversion delay

Figure F.10: RRH Receiver Path Delays

- the word alignment is optional, not commonly used in transmission paths.
- The phase alignment delay is optional. The clock phase alignment delay is optional, since the need of phase alignment buffering depends of the clocking structures and how deterministic the delays are between the core clock and the high-speed transmitter clock.

- Word alignment delay
- 8B10B Encoder delay
- Phase alignment delay
- Serial to parallel conversion delay

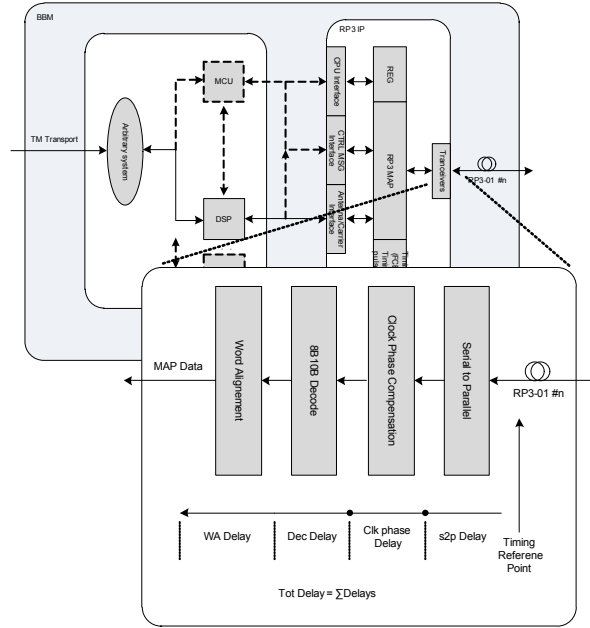


Figure F.11: BBM Receiver Path Delays

Where:

- the word alignment is optional
- the phase alignment delay is optional, since the need of phase alignment buffering depends of the clocking structures and how deterministic the delays are between the core clock and the high-speed transmitter clock.

The clock phase alignment and the word alignment delays are usually variable delays within a system. The variable delay can be measured by using the extended delay measurement feature. The delay in the receiver path is the cumulative sum of the delays.

For the configuration of the OBSAI RP3-01 interface, the delay should be determined and compensated by the delay compensation parameters. The delay compensation parameter holds an value, where the delay resolution is in number of byte clocks. Notify that the  $\Pi$  measurement

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is the reverse operation of the Delta delay setting. In the  $\Pi$  measurement the receiver path the timing of the received RP3 frame is measured. The delay relative to the timing pulse is measured. The Delay is compensated by configuration of delay values:

- The delay is added to the  $\Pi$  offset
- The delay is added to  $RTT\_OFFSET$

Delay value from the RP3 Pi parameter i.e. The BBM RX delay is calculated:

$$RX_{DelayBBM} = WA_{Delay} + Dec_{Delay} + ClkPhaseComp_{Delay} + s2p_{Delay} \quad (F.15)$$

and added to the delay:

$$\Pi_{BBM} = -RX_{DelayBBM} - \frac{RTT_{Delay}}{2} - RRH\Delta_{3,2} \quad (F.16)$$

where:

$$RRH\Delta_{3,2} = RRH_{IQDataBufferingThresholdUL} + RRH_{ANT2MAPDelay} \quad (F.17)$$

$$RTT_{Delay} = \frac{RoundTripTime}{\left(\frac{8}{i}\right)} \quad (F.18)$$

and where:

$$i = LineRate, i1, 2, 4, 8 \quad (F.19)$$

$$RoundTripTime = MeasuredRTT_{Delay}(resolution614, 4MHz) \quad (F.20)$$

Notice that the delays are different for each of the line rates. Notice also that the delays does not include the delay produced by the IQ data transmission from the MAP buffers. The RP1 timing information may be used at the DSP/MCU in-order to achieve correct timing for transport to the IQ data buffers at startup of the IQ data buffering. The data buffers may then be configured to have a certain threshold values that enables a trigger for the DSP/MCU that may be used for initiating the transport to the IQ data buffers. This delay overhead should be calculated separately based on the used DSP/MCU data path delays.

Notice that  $RRH\Delta_{3,2}$  may be discarded if the delay is compensated in the air interface timing pulse in synchronized buffering mode or when only DL path air interface is synchronized to the RP3-01 timing. Notify also that the transport path from the DSP/MCU to the IQ data

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buffers may contain clock domain crossing structures depending on the configuration and the clocking of the system. Clock domain crossings always produces variable timing of few clock cycles for each interface.

## RTT Fiber Optical Delay Measurement

The RTT delays is the round trip trip time delay measured as a two way delay starting from RP3-01 transmitter output from BBM unit to RP3-01 receiver input at the BBM unit. In the measurement the reference measurement point is in the output of the parallel to serial converter at the transmitter and at the input of the serial to parallel converter at the receiver.

All delays caused by the transmitter receiver path shall be compensated from the measurement so that the measurement result contains only the delay between the PCB traces, optical transceivers and the optical cables. The reason for this measurement is to be able of compensating all of the delay components that are existing in the transceiver paths. The measurement result may then be used for accurate timing of the transmission and different timing pulses within the RRH unit. The delay is measured in number of clock cycles, where the resolution of the measurement is 614.4 MHz. See [5] for further details in the standard.

The RTT measurement process is different in the BBM unit and the RRH unit. The BBM unit acts as an master unit in RTT measurements, the RRH unit is the slave. Simplified RTT measurement procedure:

- The RTT measurement message will be sent by the BBM unit to the DL direction. At sending time, a timer is started.
- When RRH unit receives the RTT message, it is looped back and the RRH units internal loop back delay is included into the RTT message data. The loop back delay includes the internal transceiver delays for both UL and DL path.
- When the BBM unit receives the looped back message, the timer is stopped.
- The internal transceiver delays for UL and DL path is subtracted from the timer value.
- The RRH loop back delay is subtracted from the timer value
- RTT measurement result is ready.

The RTT measurement result includes a two way delay between the BBM unit and the RRH unit. Dividing this delay by a factor of two produces the one way delay. Notify that any variable delays in the data path will be divided evenly to the one way delay.

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In BBM unit configuration, the RP3-01 RTT measurement result includes the delays of the internal transceivers. The delays and the delay variation of the transceiver paths are system specific delays. The delays should be measured or known in-order to be able to compensating the delays from the RTT measurement result.

In RRH unit configuration, the internal transceiver delays may be added as a constant to the RTT\_OFFSET. The value added to the RTT message loop back delay in-order to be able of compensating the transceiver internal delays from the RTT measurement result at the BBM unit. The delays and the delay variation of the transceiver paths in RRH unit are system specific delays. The delays should be measured or known in-order to be able of appropriate configuration of the RTT\_OFFSET.

In RRH and BBM mode the OBSAI block automatically compensates the delays caused by the scheduling of the RTT measurement message. The delay is compensated in BBM transmit scheduling, RRH loopback time and BBM receive timing. The tasks that are left for the user and the delays that are system specific delays should be compensated by the user software. The delays are:

- BBM transceiver path transmit delay
- RRH transceiver path receive delay
- RRH transceiver path transmit delay
- BBM transceiver path receive delay
- RRH buffering time

Referring to the equations in previous chapter, the following applies:

$$BBM_{TransmitDelay} = TX_{DelayBBM} * \frac{8}{i} \quad (F.21)$$

$$BBM_{ReceiveDelay} = RX_{DelayRRH} * \frac{8}{i} \quad (F.22)$$

$$RRH_{TransmitDelay} = TX_{DelayRRH} * \frac{8}{i} \quad (F.23)$$

$$BBM_{ReceiveDelay} = RX_{DelayBBM} * \frac{8}{i} \quad (F.24)$$

$$i = LineRate, i1, 2, 4, 8 \quad (F.25)$$

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The delay RRH buffering time is a value in the RTT reply message. The delays  $RRH\_ReceiveDelay$  and the  $RRH\_TransmitDelay$  are compensated automatically in the RRH unit in based on the RTT\_OFFSET value.

At BBM unit the RTT measurement is initiated by sending an control message with the type of RTT measurement. The interface block automatically counts the amount of clock cycles until an control message is received from the RRH unit. The parameter holds an delay value where the delay is calculated based on the core clock period. Referring to the above equations, the RTT measurement result is calculated based on the delay (assuming 76.8 MHz core clock):

$$Roundtriptime = (REG_{Delay} * 8) - BBM_{TransmitDelay} - BBM_{receivedelay} - RTTReplyBufferingTime \quad (F.26)$$

## Multi-Hop CPRI Delay Measurement

Multi-hop applications of remote radio modules requires that the data path delay can be measured very accurately across each hop to ensure that proper data alignment in both DL and UL and calibration can be performed accordingly and in compliance with the CPRI and wireless standard in use. The CPRI standard however only provides indications for the manual procedure that the system software management shall accomplish, and it does not provide any additional feature embedded in the protocol, unlike OBSAI RP3-01, to make this procedure more automated. RP3-01 supports in fact Multi-hop RTT measurements and automated synchronization mechanism using FCBs enables an easier multi-hop deployment.

We analyze in this section the multi-hop delay measurements using CPRI interfaces identifying the delay components in a real implementation of a networking RE module. We will use as reference's Radiocomp's CPRI v.4.1 core implementation. The "networking" RE applications is a radio module with two CPRI ports, one acting as a slave toward eNb, and the second one acting as a master to the second radio module. In this configuration, the forwarding on IQ traffic between the slave port and the master port has to be controlled from a routing controller block that is configured for selecting traffic based on frame timing and counters. The latency of this transfer has to be minimized to meet requirements as in [24]. A raw low latency AUX interface shall be the reference point for delay measurement providing data aligned with frame counters and presenting all the input / output frame synchronization information to enable accurate control of routing of AxC containers between slave and master port instances. In a multi-hop networking RE module therefore it is required identifying additional internal reference points

for frame timing delay measurements in addition to the points specified in [24] and shown in Fig.F.12:

- RB2 Slave Port input
- RB3 Slave Port output
- RB4 Master Port input
- RB1 Master Port output

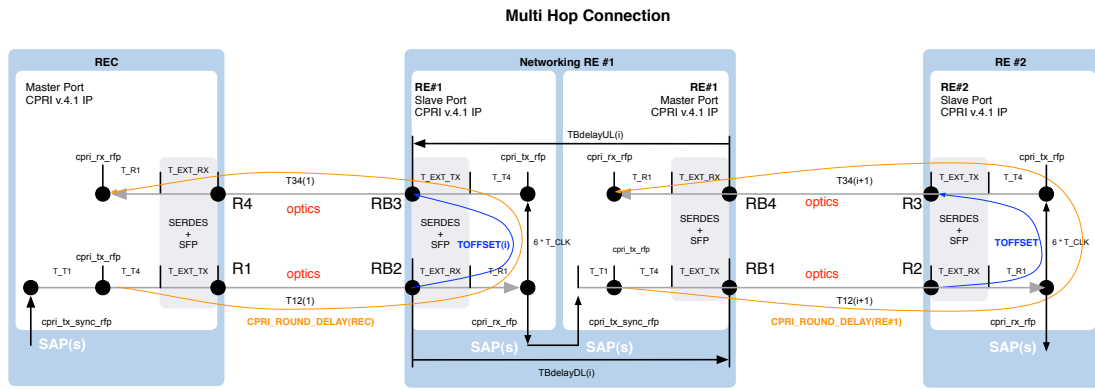


Figure F.12: CPRI-RE-RE Delay Budget

In Fig.F.12 it is also shown the  $SAP_s$  references matching the AUX interface and how to relate the [24] definitions. In downlink the IQ frame timing follows the CPRI frame timing. In uplink the IQ timing might be re-adjusted at the networking RE sub-module for compensating additional delays including TX and RX offsets of data mapping in relation to frame timing that shall be exchanged between REC and RE(s) during link startup and calibration. In a networking RE, between the slave and a master port instantiation, we can define the following internal measurement points:

- RB5 Slave AUX port output
- RB6 Master AUX port input
- RB7 Master AUX port output
- RB8 Slave AUX port input

Therefore the  $TB_{delayDL}$  and  $TB_{delayUL}$  in the case of a networking RE application can be considered as depicted in Fig.F.13:

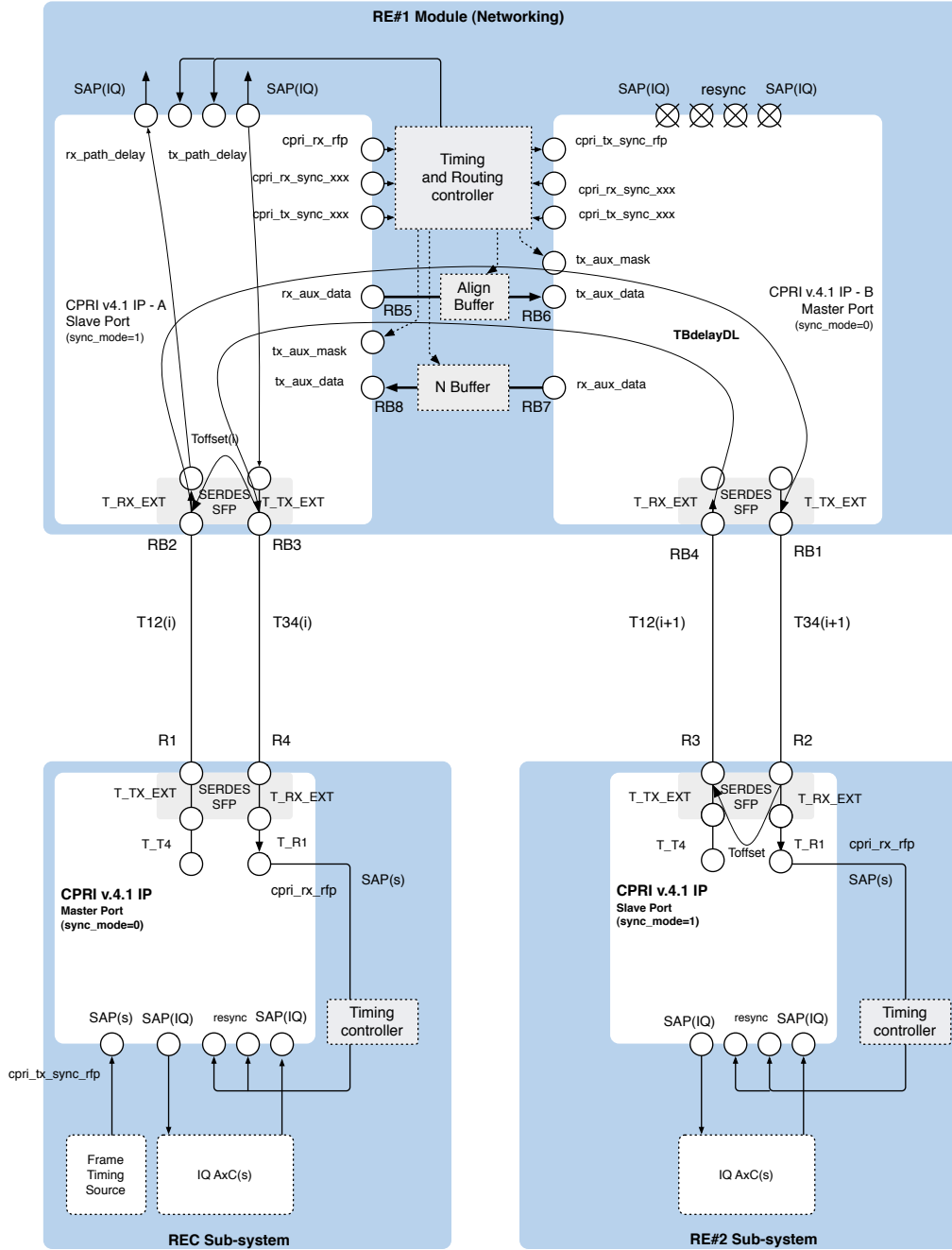


Figure F.13: CPRI-RE-RE Delay Budget



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The following definitions thus applies:

$$TB_{delayDL} = T_{25} + T_{56} + T_{61} \quad (F.27)$$

$$TB_{delayUL} = T_{47} + T_{78} + T_{83} \quad (F.28)$$

where:

Delay Name	Value
T25	T_EXT_RX(a) + T_R1(a)
56	T_EXT_BUF_DL
T61	T_T4(b) + T_EXT_TX(b)
T47	T_EXT_RX(b) + T_R1(b)
T78	T_EXT_BUF_UL
T83	T_EXT_TX(a) + T_T4(a)

Table F.1: Networking RE Internal Delays for DL and UL

and where:

Delay Name	Value
T_R1	T_RX_BIT_ALIGN + T_8B10B_DEC + T_RX.BYTE_ALIGN + T_RX_BUF + T_RX.PHASE
T_T4	T_8B10B + 6 * TCLK
T_EXT_RX	Shall be provided from SERDES vendor + optical module delay
T_EXT_TX	Shall be provided from SERDES vendor + optical module delay
T_T1	7 * TCLK
TX_OFFSET	Programmable

Table F.2: CPRI Internal and External delays

- $T_{B_{delay}DL}$  does not depend on the link delay so it is a known value for the networking RE.
- $T_{B_{delay}UL}$  depends on the link delay so it has to be measured in the field.

In Fig.F.13, in the networking  $RE\#1$  node, two instances of the CPRI controller interface are provided; one is configured as slave port (a) and one is configured as master port (b). The two instances are connected back to back via the AUX interface with some additional buffers in between the TX and RX I/Os for compensate for timing alignments. The buffering control and the  $cpri\_tx\_aux\_mask$  signals are controlled by a routing controller module, which is using the TX and RX synchronization status indications to control the data insertion and frame timing.

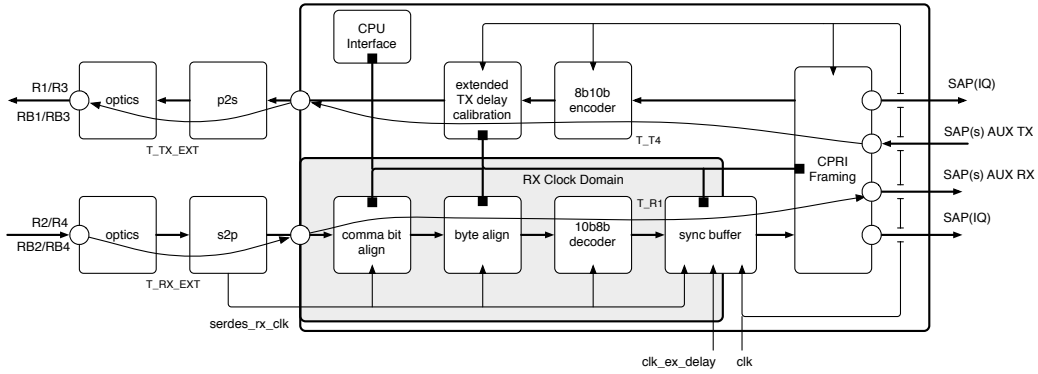


Figure F.14: CPRI Internal and External TX / RX Path delays to  $SAP_S$

The delay management requires a middleware between the O&M system and the CPRI controller. The delays needs to be constantly monitored (e.g. every 1s) and alarms shall be reported if the variations exceed a predefined user threshold. This threshold shall be dependent on specific applications.

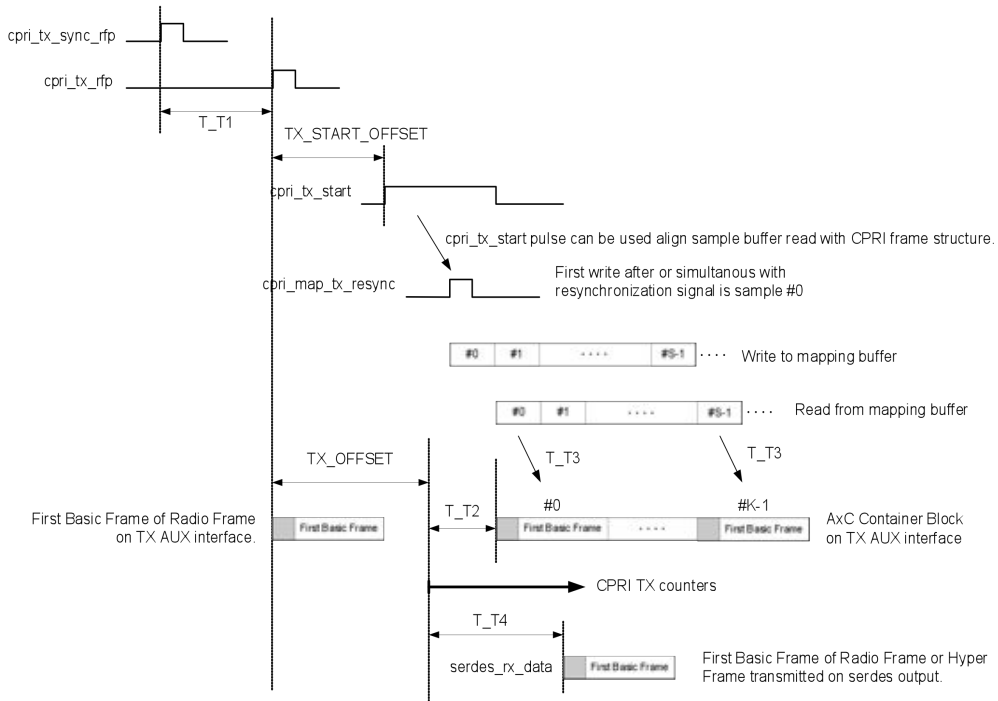


Figure F.15: CPRI TX Path delays relative to  $SAP_S$  and  $SAP_{IQ}$

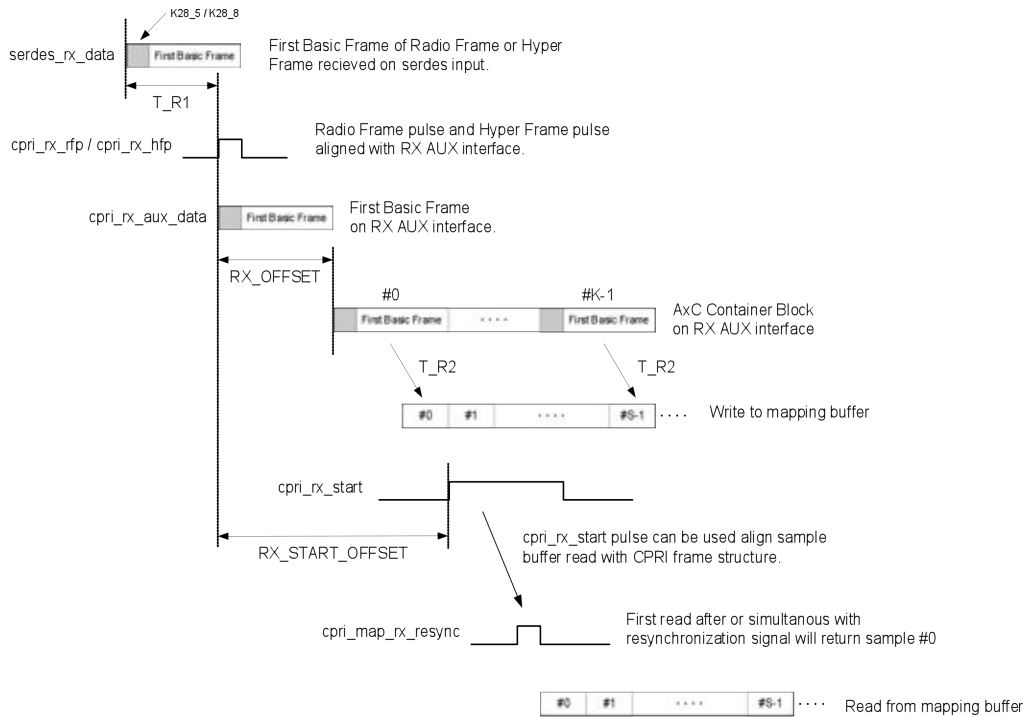


Figure F.16: CPRI RX Path delays relative to  $SAP_S$  and  $SAP_{IQ}$