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Electret Based Energy Harvesting Device with Wafer Level Fabrication Process

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Abstract.

This paper presents a MEMS energy harvesting device which is able to generate power from two perpendicular ambient vibration directions. CYTOP polymer is used both as the electret material for electrostatic transduction and as a bonding interface for low-temperature wafer bonding. The device consists of a four-wafer stack, and the fabrication process for each wafer layer is described in detail. All the processes are performed at wafer scale so that overall 44 devices can be fabricated simultaneously on one 4-inch wafer. The effect of fabrication issues on the resonant frequency of the device is also discussed. With a final chip size of about 1 cm^2, a power output of 32.5 nW is successfully harvested with an external load of 17 MΩ, when a harmonic vibration source with RMS acceleration amplitude of 0.03 g (~ 0.3 $m{\cdot}s^{-2}$) and resonant frequency of 179 Hz is applied. These results can be improved in an optimized design.

1. Introduction

Recently, energy harvesting devices have been developed based on electromagnetic [1, 2, 3], piezoelectric [4, 5], and electrostatic [6, 7, 8, 9, 10, 11, 12, 13, 14] transduction methods due to their potential to replace batteries used in wireless sensor network (WSN) technology [15, 16]. Electromagnetic energy harvesting devices are built on Faraday's law of induction, where electric power generates when a number turns of coil cut across a magnetic field. Piezoelectric harvesters utilize the piezoelectric effect of certain materials, such as PZT and PVDF, which are electrically polarized when subjected to mechanical strain. Electrostatic energy harvesters use variable capacitors which either have been pre-charged using electret materials, or biased by external voltage sources. When driven by a vibration source, the change of capacitance forces charge movement between the electrodes and therefore generates electric current through an external load resistor.

The capacitance of an ideal parallel-plate capacitor is $C = \epsilon_r \epsilon_0 A/g$, where ϵ_r is the relative permittivity of the dielectric (e.g. air), ϵ_0 the permittivity of vacuum, A the electrode overlap area, and g the air gap between the two electrodes. According to this, there are two main schemes to change the capacitances by changing either the overlap area or the gap distance between the two electrodes of the capacitor. The former scheme can be achieved by in-plane vibration of the proof mass where the overlapping area changes; while the latter scheme can be achieve by out-of-plane vibration of the proof mass to change the air gap. Since the squeeze-film air damping effect is relatively more profound than the slide-film damping under the same conditions, energy harvesting devices with in-plane vibration scheme have higher Q-factor and less energy loss by viscous dissipation, compared to devices with an out-of-plane vibration scheme.

In our previous work [13], we have developed a prototype device where an output power of 1.2 μW was successfully harvested from an external vibrations with acceleration as low as 0.014 g ($\sim$ 0.14 m·s^{-2}). However, the two parts (a silicon chip and a glass chip) of the prototype device were bonded by double-sided adhesive tape. It is neither practical for mass production nor compatible to the fabrication of sensors. In this paper, we will therefore focus on a MEMS fabrication process at wafer-level for the electret-based energy harvesting device. Thanks to the compatible processes, it is promising for the devices to be fabricated and packaged together with the wireless sensors in the future. The device described here can be further optimized for higher output power and voltage.

2. Design and Modeling

As shown in Fig. 1, we have developed an electrostatic energy harvesting device with a 4-wafer stack structure. This device includes a suspended proof mass that is confined within a fixed frame through spring structures. The springs are designed to provide a sharp resonance peak in the ambient vibration frequency range (less than 200 Hz).

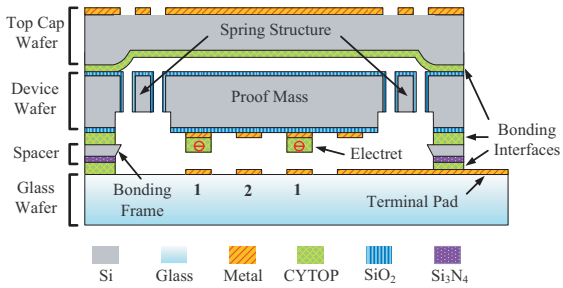

Figure 1. Schematic view of the 4-wafer stack structure for the energy harvesting device. The device is composed of four wafers, namely, *Top Cap, Device, Spacer* and *Glass*. The four wafers are bonded together with adhesive polymer in a thermo-compression bonding technique.

Two perpendicular in-plane vibration directions can drive the proof mass with this method. CYTOP polymer is used both as an electret material and adhesive layers for low-temperature wafer bonding. As the pre-charged electrets oscillate according to the vibration source, induced charges will move between the two electrodes on the counter part causing a current through the external load.

Similar to our previous work [13], we use the electrodes on single side (ESS) design in which output electrodes are located on the same side of the device. This ESS design releases the package challenge of the electrodes on both sides (EBS) design, where additional wiring or 3D structures such as metal stud bumps are demanded to lead out the signal lines from both sides of the device. Furthermore, moving parts and electrets are completely encapsulated to keep them dust- and moisture-free for better charge stability and overall performance. Unlike the previously reported prototype harvesters [9, 11, 12, 13], the device presented here is a fully packaged device entirely built at a wafer level. Besides, the gap between electrets and counter electrodes is tunable and well controlled in the fabrication phase. The small device size (1 cm $\times$ 1 cm $\times$ 0.15 cm) makes it compatible with the state-of-the-art WSN technology.

Figure 2 shows the layout of the proof mass and the beam structures. With two beams on each side, the proof mass is suspended from the frame, which allows two directional movement driven by the external vibration source. With the inclusion of stopper structures, the maximum vibration amplitude of the proof mass can be limited, to prevent fracture of the silicon beam material at high accelerations. Figure 3 shows 3-D simulations by COMSOL finite element modeling to obtain the resonant frequency (Fig. 3 a) and the stress distribution in the beams (Fig. 3 b). When a displacement of 500 μm is defined for the proof mass, the maximum stress across the beam is simulated to be 800 MPa, which is far smaller than the fracture limit of single crystal silicon (up to $\sim$7 GPa [17]), leaving a large safety margin for overload of the structure without risk of fracture. The resonant frequencies in x and y directions can be easily optimized by tuning the beam length L and the beam width w. Detailed parameters of the device are listed in Table 1.

Figure 4 shows a model of the device which contains both the electric and the

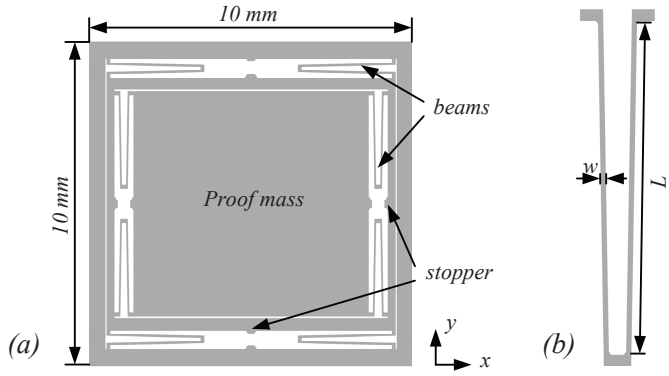

Figure 2. (a)Layout for the *Device* structure with proof mass suspended by beams in x and y directions; (b) Close-up view of the beam structure.

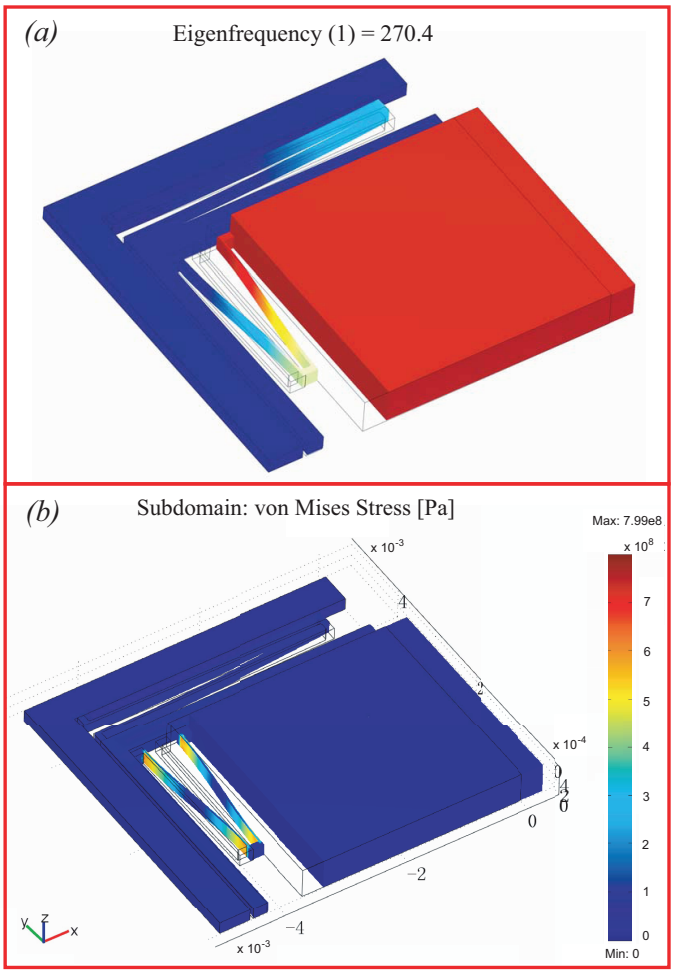

Figure 3. 3-D FEM simulations (a) Eigenfrequency study and (b) Static study. The maximum stress at the corner of the beam structure is less than 800 MPa when the displacement of the proof mass is defined as 500 μm.

mechanical domains. According to the Kirchhoff's voltage law, the voltage across the

Table 1. Parameters of the electret-based energy harvesting device.

Parameters	Value	Description
g	$100\,\mu$m	gap between the proof mass and the electrodes
d	$10\,\mu$m	electret thickness
w	$40\,\mu$m	beam width
L	2.3-2.8 mm	beam length
t_1	$280\,\mu$m	beam thickness
t_2	$500\,\mu$m	wafer thickness
m	0.06 g	proof mass
f_0	220-300 Hz	resonant frequency
ϵ_d	2	relative permittivity of the electret
σ_d	$-0.24\,\mathrm{mC/m^2}$	surface charge density
C_{min}	1.64 pF	minimum capacitance
C_{max}	1.82 pF	maximum capacitance

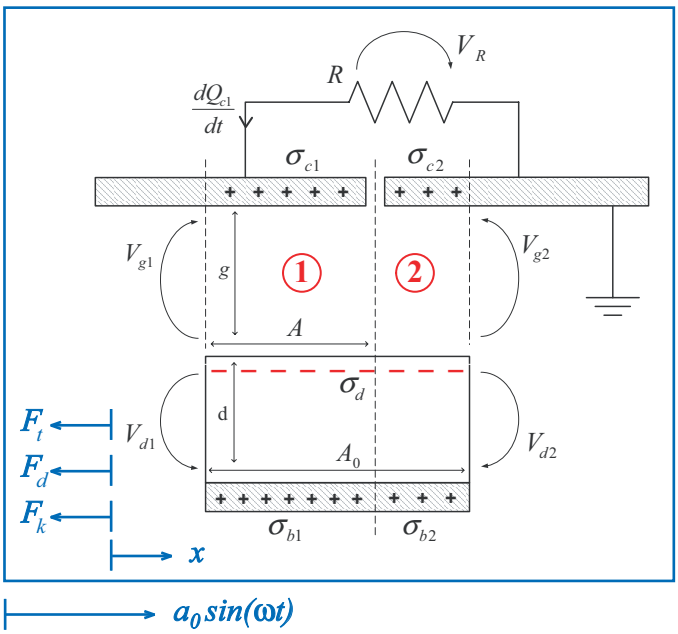

Figure 4. Model of the in-plane electret energy harvesting device.

resistor V_R fulfils

$$R\frac{\mathrm{d}Q(t)}{\mathrm{d}t} = V_\mathrm{R}(t) = V_\mathrm{g2}(t) - V_\mathrm{d2}(t) + V_\mathrm{d1}(t) - V_\mathrm{g1}(t)$$
$$= \sigma_\mathrm{c2}(t)g/\epsilon_0 - \sigma_\mathrm{b2}(t)d/(\epsilon_d\epsilon_0) + \sigma_\mathrm{b1}(t)d/(\epsilon_d\epsilon_0) - \sigma_\mathrm{c1}(t)g/\epsilon_0 \tag{1}$$

Overall charge neutrality for the individual overlap areas requires,

$$\sigma_\mathrm{d} + \sigma_{\mathrm{c}i}(t) + \sigma_{\mathrm{b}i}(t) = 0, (i \in [1, 2]) \tag{2}$$

while the constant total charge condition on the floating base electrode results in

$$A_0\sigma_\mathrm{b} = A(t)\sigma_\mathrm{b1}(t) + [A_0 - A(t)]\,\sigma_\mathrm{b2}(t) = \text{constant}. \tag{3}$$

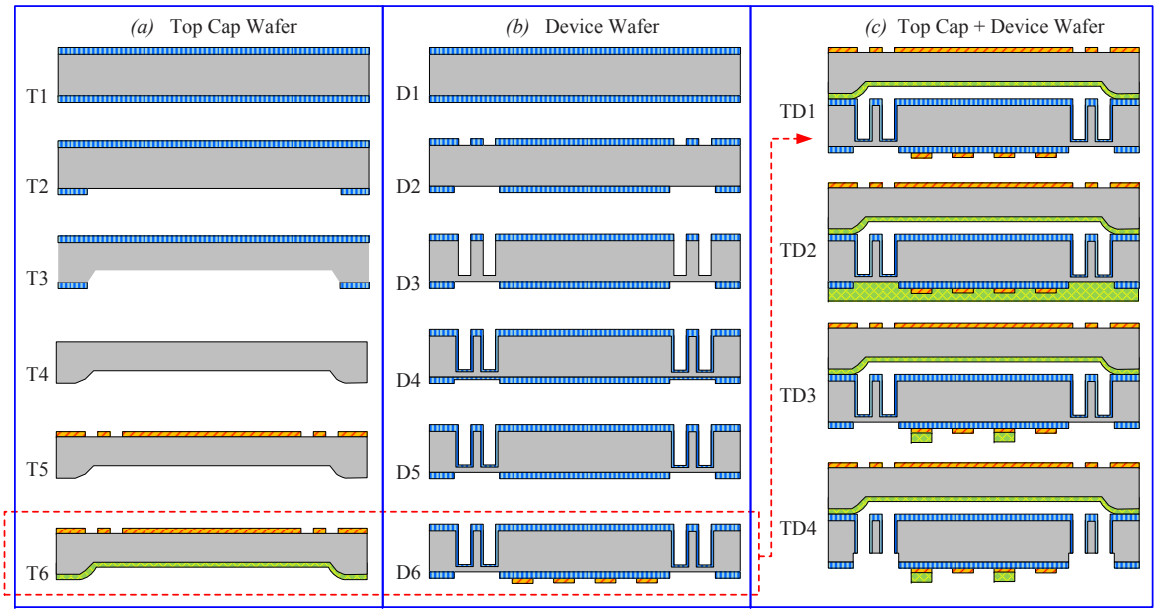

Figure 5. Process flow for the (a) *Top Cap* and (b) *Device* wafers. The two wafers are fabricated individually and then bonded together using adhesive CYTOP polymer (c).

From Eqs. 2 and 3, the governing equation for the electric behavior of the device becomes

$$\dot{Q} = \left(-\frac{d\epsilon_d + g}{R\epsilon_0\epsilon_d\tilde{A}}\, Q - \frac{d\sigma_d}{R\epsilon_0\epsilon_d} \right) \cdot \frac{A_0}{A_0 - \tilde{A}} \tag{4}$$

where $Q = Q_{c1}$ is the instantaneous surface charge on electrode 1, R the external load resistance, $\tilde{A}$ the effective overlap area, A_0 the initial overlap area. The mechanical behavior of the device can be described as

$$\ddot{x} = a_0 \sin(\omega t) - \omega_0^2\, x - 2\xi_m\omega_0\, \dot{x} + \frac{F_t}{m} \tag{5}$$

where, ω and ω_0 are the angular frequency of external acceleration and the angular resonant frequency of the spring-mass system, respectively; ξ_m is the mechanical damping factor. The coupling between the electric and the mechanical domains is related to the transduction force F_t, which may be expressed as $F_t = -\partial U/\partial x$ where U is the electrostatic energy stored in the device. Solving these equations with a driven acceleration of 0.03 g, we have estimated an out power of about 30 nW and an optimal load of 22 MΩ when a parasitic capacitance (∼40 pF) is taken into account. More detailed discussion on design, modeling and optimization of the device will be published in the near future [18].

3. Fabrication

The energy harvesting device is built with 4-inch standard MEMS fabrication techniques. There are four wafers, namely, *Top Cap, Device, Spacer* and *Glass* in the structure. The material and purpose of each wafer are listed in Table 2 and the fabrication process for each wafer will be described below in detail.

Table 2. Material and purpose of the four processed wafers in the energy harvesting device.

Type	Material	Purpose
Top Cap	silicon	protects critical parts (i.e. springs and electrets) from water leakage
Device	silicon	contains proof mass, spring system, and electret pattern
Spacing	silicon	defines the air gap thickness between electret and counter electrode patterns
Glass	fused silica	contains the counter electrode pattern, ending up in two conductive terminals where the external load can be connected

3.1. Top Cap wafer

The *Top Cap* wafer of the energy harvesting device is used to protect electrets and fragile spring structures from external agents. Fabrication of the *Top Cap* starts with a 350 μm-thick (100) silicon wafer, as shown in Fig. 5(a).

T1: The wafer is thermally oxidized to grow 0.5 μm-thick SiO_2 layers on both sides of the wafer;

T2: Then, the SiO_2 layer is patterned from the bottom side by lithography and buffered hydrofluoric acid (bHF) etching. The SiO_2 layer pattern will serve as the mask for following silicon etching;

T3: The silicon wafer is etched using a 25% KOH solution at 85 °C to an etch depth of 20 μm. The cavity depth should be controlled in a reasonable range. It should be deep enough that all the moving parts of the device are free of stiction to or collision with the cap, while it should not be too deep to spin coat a uniform CYTOP layer afterwards.

T4: All of the SiO_2 layer is stripped away using bHF etching. Afterwards, a maskless etch in KOH for 30 seconds is performed to round the edge of the cavity, which will facilitate the polymer coating to follow;

T5: Using a lift-off technique, 50 nm Aluminum is evaporated and patterned on the top side of the wafer which will serve as the fiducial marks for the later bonding process;

T6: CYTOP is spin-coated twice onto the wafer at 800 rpm for 30 seconds, which results in a thickness of about 4 μm for the adhesive polymer. The *Top Cap* wafer is now ready for the further processing.

3.2. Device wafer

The *Device* wafer is the main component in the whole device. It contains the spring-mass structure and carries the polymer electret. We start fabrication of the *Device* wafer with a 500 μm-thick (100) silicon wafer with a resistivity of about 10^{-1} Ω·m.

D1: As shown in Fig. 5(b), the wafer is thermally oxidized and 2 μm-thick SiO_2 layers are grown on both sides of the wafer;

D2: Lithography is applied to the two sides of the wafer successively. Then, the SiO_2 layers are etched by bHF;

D3: With the SiO_2 as masking layer, the silicon wafer is dry etched in a deep-RIE process shaping the beam structures. A Bosch process [19] is employed with an etch depth of about 280 μm, which will be the final beam thickness.

D4: The wafer is then re-oxidized thermally to protect the sidewalls of the beam structures during the later final release etch;

D5: RIE etching of SiO_2 is performed from the bottom side to expose the area to be released later;

D6: A metal multilayer of Cr/Au/Cr (10/300/40 nm) for guard electrodes is deposited and patterned by lift-off technique.

Afterwards, the *Top Cap* wafer and the *Device* wafer are bonded together, as shown in Fig. 5(c).

TD1: The *Top Cap* wafer and the *Device* wafer are aligned and thermally bonded in an EVG-NIL system. The bonding is done at 160 °C for 1 hour to achieve a high bonding strength;

TD2: CYTOP is spin-coated for 6 times to reach a final thickness of 10 μm;

TD3: Then, the CYTOP layer is patterned by photoresist lithography and etched in a RIE process optimized for high selectivity to the photoresist mask [20];

TD4: With another thick photoresist mask, the beam structure is released by a deep-RIE etching from the bottom side. A standard recipe for deep-RIE burns the photoresist during the etching, as shown in Fig. 6(a). This is because the heat transfer is not efficient when the spring structures are fully released. To overcome this process challenge, we use the standard recipe at the beginning and switch to a revised recipe when less than 10 μm silicon is left before the full release. As shown in Table 3, the revised recipe employs lower power with shorter etch time, and a standby step every 10 cycles during which plasma is switched off and wafer cooling is allowed. Figure 6(b) shows a microscopic view of the structure etched using the revised recipe. The photoresist is successfully stripped away and no burned resist residues can be seen on the proof mass and electret pattern.

Figure 7(a) shows an image of the wafer after bonding. Overall 44 devices have been fabricated simultaneously on the wafer and a close-up view can be seen in Fig. 7(b). The SEM images in Fig. 8 show more fabrication details about the electrets and the springs in x and y directions.

3.3. Spacer wafer

It is crucial to control the air gap between the electret and the counter electrodes to achieve a high power output without electrostatic collapse. Micro balls [12] or double-sided tape [13] were used for prototype devices but they are not applicable for wafer

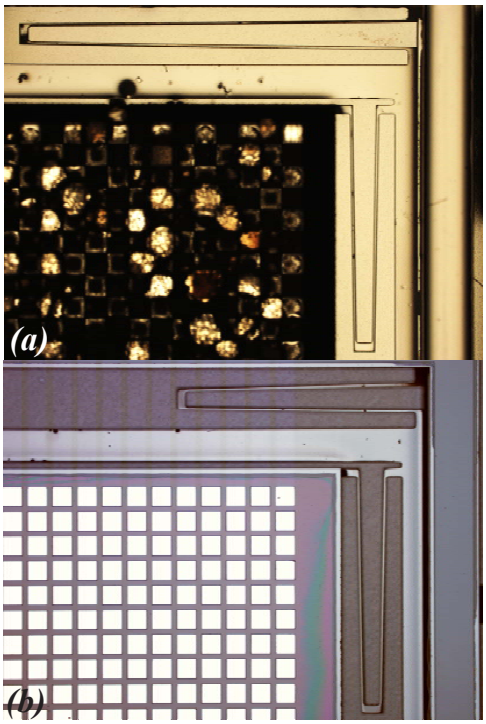

Figure 6. Microscope pictures showing release etch results with different DRIE recipes. (a): *Only standard recipe:* resist is burned on the whole proof mass and the electret pattern is degraded. Subsequent resist strip-off will leave resist residues on the substrate. (b): *Standard recipe + revised recipe:* resist is kept under a critical temperature to effectively mask the release etching process. Subsequent resist strip-off is successful and no resist residue is left on the surface.

Table 3. DRIE parameters and performance of recipes used in step TD4. A standard recipe for deep etching and a revised recipe for better cooling during the last a few μm of silicon are compared.

	Standard recipe (etch/passivation)	Revised recipe (etch/passivation)
Step time (second)	7.8 / 5.0	6.0 / 5.0
SF_6, O_2/C_4F_8 (sccm)	230, 23 / 120	200, 20 / 120
Coil power (Watt)	2800 / 1000	600 / 600
Platen power (Watt)	19 / 0	10 / 0
Platen temperature (°C)	0	20
Standby step time	N.A.	2 minutes / 10 cycles
Silicon/resist selectivity	40:1	80:1
Etch rate (μm/cycle)	1.2	0.28

level fabrication. Therefore, a *Spacer* wafer is introduced in between the *Device* wafer and the *Glass* wafer to accurately control the gap as shown in Fig. 9(a).

S1: A silicon wafer with thickness of 350 μm is first oxidized in a furnace using the same recipe as step D1. The 2 μm-thick SiO_2 will serve as the mask layer in a later KOH etching;

S2: The SiO_2 layer is patterned by photolithography and bHF etching;

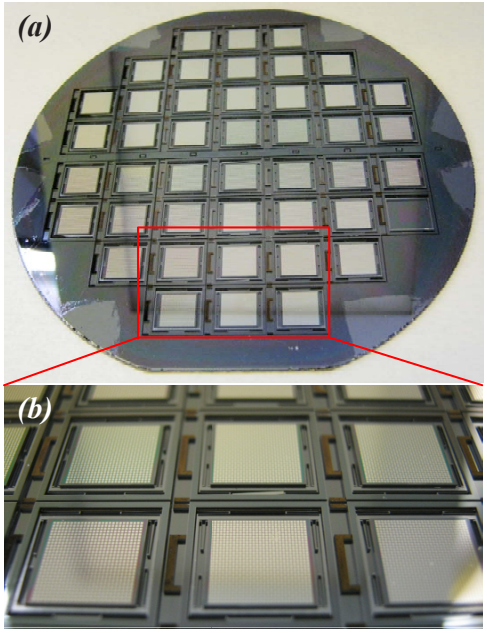

Figure 7. The *Top Cap + Device* wafer after step TD4. Overall 44 devices are fabricated on a single wafer. Full wafer view shown in (a) and a close up view in (b).

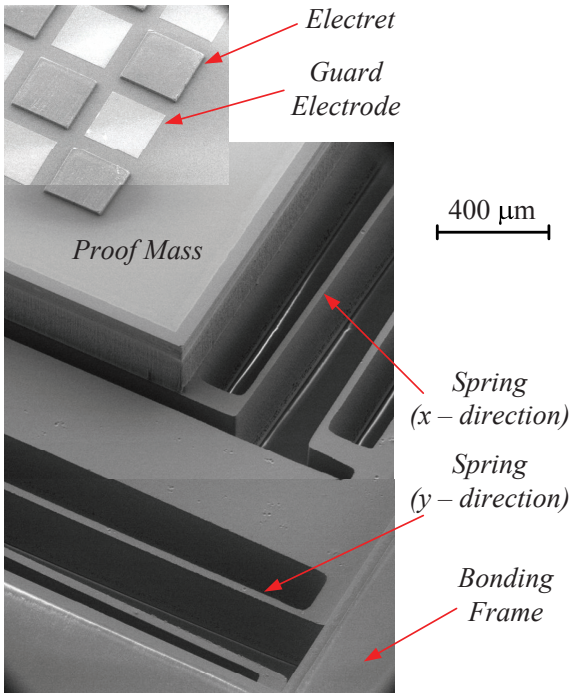

Figure 8. Multiple SEM images of device wafer's bottom side after final release of spring structure. (re-edited for better illustration.)

S3: The silicon wafer is etched in a 25% KOH solution at 85 °C to an etch depth of 100 μm. This will approximately be the gap distance between the electrets and the counter electrodes;

S4: After stripping all of the SiO_2 layer, a 200 nm layer of SiN_x is deposited on the

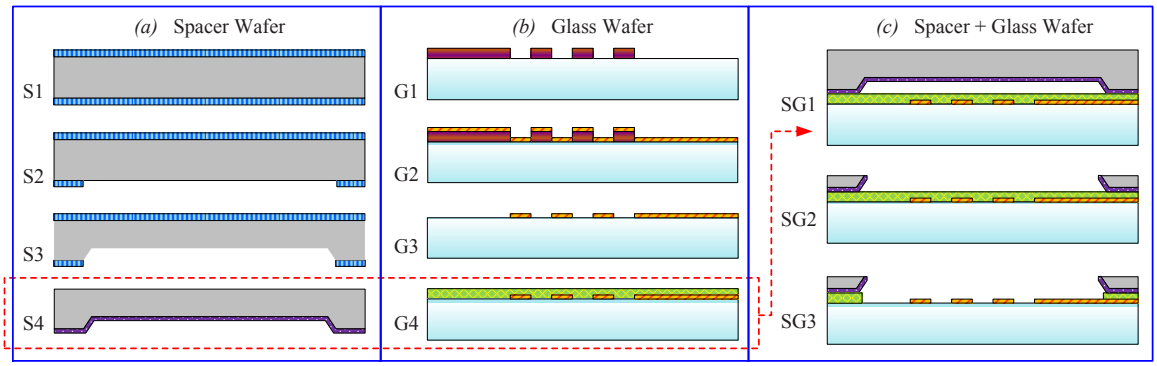

Figure 9. Process flow for the (a)*Spacer* and (b)*Glass* wafers; (c)Then, the two wafers are bonded using CYTOP.

etched cavity using a low-stress PECVD process.

3.4. Glass wafer

The *Glass* wafer contains the counter electrodes pattern, leading the current signal out to two terminals where the external load can be connected. Fused silica wafers with thicknesses of 500 μm are used and the fabrication is shown in Fig. 9(b).

G1: A negative lithography is performed with a 4.2 μm-thick photoresist layer;

G2: A metal multilayer stack of Cr/Au/Cr (10/300/40 nm) is deposited on the photoresist pattern;

G3: A lift-off process is performed in acetone and the electrodes pattern is left when all the photoresist is stripped;

G4: Then, CYTOP is spin-coated twice onto the wafer at 800 rpm for 30 seconds. As in step T6, the adhesive CYTOP layer will serve as the bonding interface in the following process.

Afterwards, the *Spacer* and the *Glass* wafers are aligned and thermally bonded (Fig. 9c, SG1).

SG2: The bonded wafer is further thinned in KOH etching until the pre-etched cavity is exposed. Figure 10 shows a microscopic view of the wafer after etching. Part of the SiN_x membrane still remains on the wafer and will be removed in the next step;

SG3: After removal of the residual SiN_x, RIE is used to etch out the CYTOP and expose the electrodes.

3.5. Corona charging and Final bonding

The *Top Cap + Device* wafer is charged in a custom-built corona charging setup as discussed in [21]. The setup consists of a high-voltage probe tip ($V_H = -10$ kV), a mesh grid ($V_g = -500$ V) and a grounded wafer stage. The surface potential of the electret

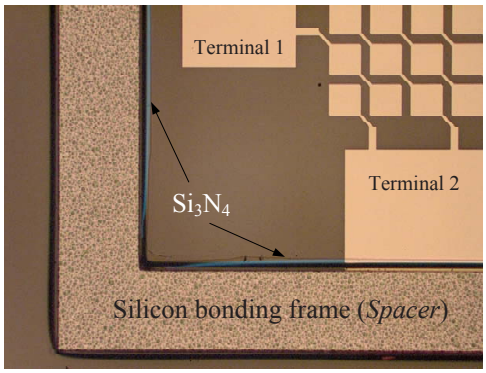

Figure 10. Microscope view of successful KOH etching (SG2). Some Si_3N_4 (blue) is still attached to the bonding frame edges and will be removed later.

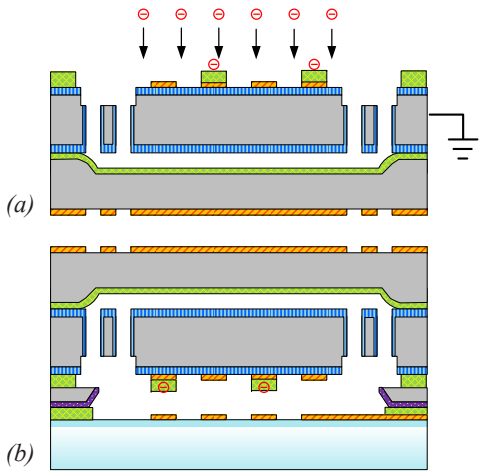

Figure 11. (a)The *Top Cap + Device* wafer is charged in a corona charging setup; afterwards, (b) the four wafers are finally bonded together at a low temperature of 120 °C for 1 hour.

(array with 200 μm $\times$ 200 μm square patterns) was measured to about -140 V after charge stabilization for a few minutes. The measured surface potential is lower than the mesh grid bias voltage. This is mainly due to the fact that the charging efficiency is lower for smaller electret patterns [14, 22].

As shown in Fig. 11(b), the *Top Cap + Device* wafer is finally bonded to the *Spacer + Glass* wafer. The bonding is processed at a low temperature of 120 °C for 1 hour to avoid any loss of the surface charge. The fabricated wafer is then diced and the final device is shown in Fig. 12. The chip size is as small as 1 cm^2. Figure 13 shows a cross-sectional view of the 4-wafer stack obtained by dicing through the middle of a device.

4. Characterization and Discussion

The performance of the energy harvester is characterized using a shaker setup to mimic the external vibration source. Figure 14(a) shows the shaker (B&K Mini Shaker 4810)

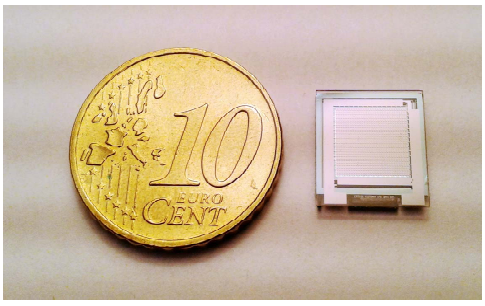

Figure 12. The final device after wafer dicing. The chip size is 1 cm × 1 cm × 0.15 cm. The photo is taken from the glass side of the device.

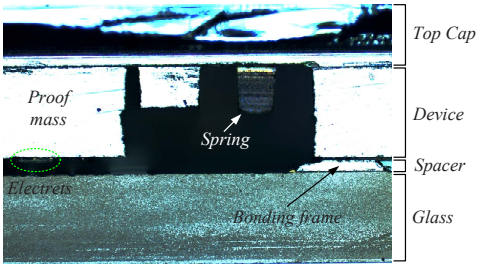

Figure 13. Cross-sectional device view from an optical microscope where a dummy device is diced in the middle of the proof mass. Proof mass, electret pattern, and a bonding frame column are seen clearly in the image. A spring connects the proof mass to the bonding frame.

with a reference accelerometer driven by an amplified sinusoidal signal from a function generator (Agilent 33220A). The two terminal electrodes are connected to an external resistor and an oscilloscope, as shown in Fig. 14(b). The root mean square (RMS) acceleration from the shaker is kept constant at 0.03 g ($\sim$ 0.3 m·s^{-2}) using feed-back control while the frequency is swept from 172 Hz to 184 Hz. The voltage output of energy harvester is recorded using an oscilloscope and therefore, the RMS power output can be derived. Figure 15 plots a typical waveform for the output voltage from the oscilloscope with $R_{\text{osc}} = 1$ MΩ and $R_{\text{test}} = 0$. Sub-peaks are observed simply because the vibration amplitude of the proof mass is large enough to overpass more than one electrode period during a cycle. At a shaker amplitude of 0.23 μm, the vibration amplitude of the proof mass was larger than 250 μm, which indicates a mechanical quality factor of approximately 1100.

Figure 16 shows the frequency response of the device and a resonant frequency of about 180 Hz is detected when the device is driven in x-direction. Similar measurements have also been performed in y-direction where a slightly lower resonant frequency of 176 Hz is detected. These frequencies are lower than the expected value of 280 Hz from calculation because a fabrication issue occurred during the deep-RIE etching of the beams (step D3 in Fig. 5). From the microscopic images in Fig. 17, we can see that the beam width decreases from 36 μm at the top to about 16 μm at the bottom of the beam. This means that the cross-section of the beam is tapered and the angle of etch

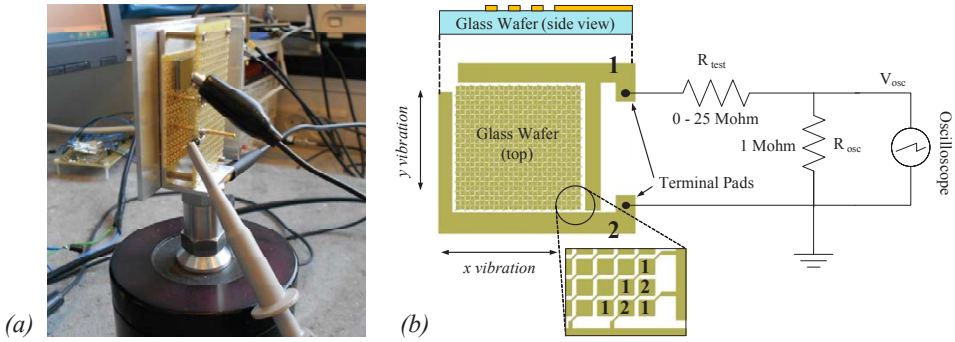

Figure 14. (a) An energy harvesting device is mounted on a shaker with a reference accelerometer and the test circuit; (b) Schematic view of the test setup. Rows of counter electrodes '1' and '2' are connected to terminal pads '1' and '2' respectively. The voltage V_{osc} is measured for different values of R_{test} to obtain an output power vs. load curve.

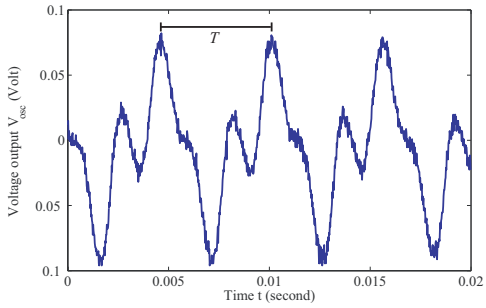

Figure 15. A typical example of the voltage output from the oscilloscope. Both a major and a minor peak is observed during a vibration cycle of the device.

profile can be calculated as:

$$90^\circ + \arctan\left[\frac{(w_1 - w_2)/2}{h}\right] \simeq 92.1^\circ \tag{6}$$

where w_1 and w_2 are the beam widths and h is the etch depth. The shrinkage of beam width will dramatically reduce the area moment of inertia and therefore decrease the spring constant k of the beam. From a mechanical modeling with Comsol, we have found that the spring constant of the beam decreases by about 57%. According to the relation $f_0 \propto \sqrt{k}$, we should expect a decrease of the resonant frequency by about 35%, which agrees very well with our measurement.

Figure 18 shows the RMS power output as a function of the external resistance. A maximum power output of 32.5 nW is achieved with an optimal load of 17 MΩ. Furthermore, it was observed that comparable output powers were extracted from two perpendicular vibration directions. Due to the effect of parasitic capacitance, both the power output and the optimal load are lower than our expectation, which will be further discussed elsewhere. Nevertheless, the normalized power density (NPD) for our device, defined as power/volume/acceleration^2 in [2], is as high as 1.8 Kg·s·m^{-3}. The calculated NPD value compares favorably to 1.0×10^{-6} Kg·s·m^{-3} and 0.09 Kg·s·m^{-3} of the macro

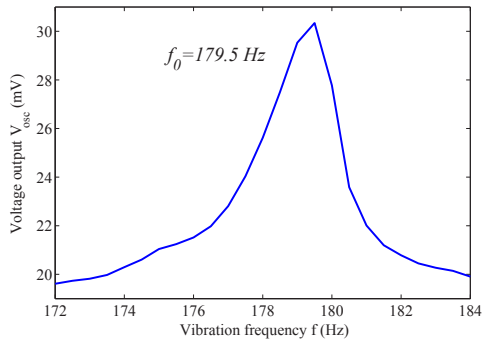

Figure 16. Voltage output from oscilloscope as a function of the driven frequency. The energy harvesting device provides a maximum voltage output when driven at the resonant frequency of 179.5 Hz.

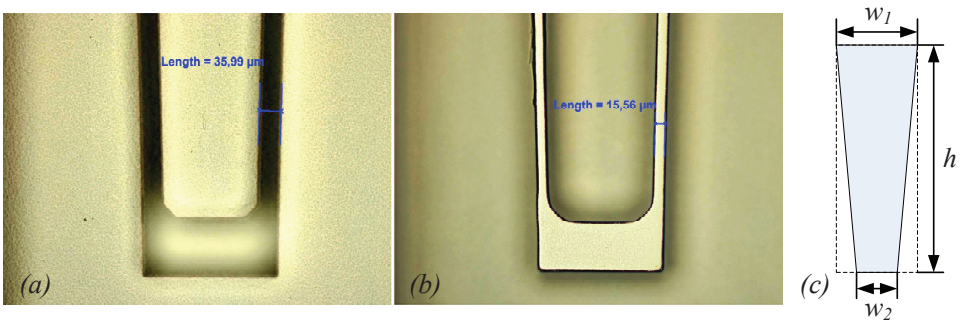

Figure 17. Beam width is measured from (a) the top side after step D3 and (b) the bottom side after step TD4. A severe shrinkage of the beam width is noticed which gives a tapered cross section of the beam, as shown in (c).

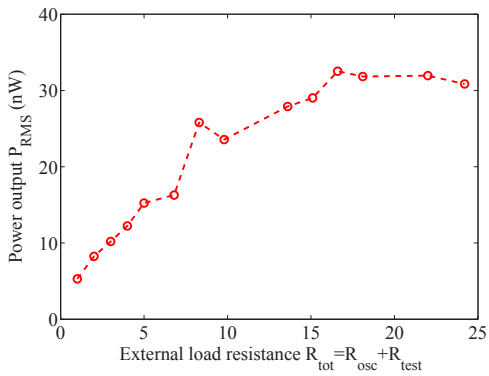

Figure 18. Harvested RMS power at 0.03 g as a function of the total external load $R_{\text{tot}} = R_{\text{osc}} + R_{\text{test}}$.

devices from [11] and [3], respectively.

Even with the reasonable NPD value for the device, it should be noted that the power output is too low for direct applications. This, however, can be improved significantly by optimizing device parameters. Firstly, the gap distance between the proof mass and the counter electrodes should be minimized. Smaller gap will give larger intrinsic device capacitances, less sensitivity to parasitic capacitances and therefore

higher output power. A gap of about 70 μm has been used previously for a prototype device [13], and an even narrower gap of 38$\sim$70 μm has been proved to be feasible [12]. Secondly, the surface charge density on the electrets should be increased by increasing both the bias voltage and the charging efficiency. Since the power output in general is proportional to the square of the surface charge density [6], we should expect 25 times higher power output when we increase the surface potential of the electret to -700 V. Last but of equal importance, the parasitic capacitance should be reduced. We have currently noticed a parasitic capacitance of about 40 pF mainly from the measurement setup, which lowers the optimal load resistance and reduces the harvested power.

5. Conclusion

A MEMS compatible process flow has been developed for wafer level fabrication of a 2D electret-based energy harvesting device. Four wafers for a device stack were designed and fabricated i.e. top cap, main device, spacer and bottom electrodes wafers, respectively. Overall 44 devices are fabricated simultaneously on one 4-inch wafer. The final device was packaged as a 1 cm^2 chip using CYTOP both as an electret material and bonding interfaces between wafers. Electrical power was generated from two perpendicular vibration directions as the proof mass was driven to its resonance frequency. In a simple test setup, a maximum output power of 32.5 nW was achieved with an external load of 17 MΩ, under a harmonic source motion with an acceleration RMS amplitude of 0.03 g ($\sim$ 0.3 m$\cdot$s^{-2}) at a frequency of 179.5 Hz. The chip harvests a relatively low power output in the current implementation due to the low intrinsic device capacitance and the large parasitic capacitance, while the normalized power density is very high thanks to the high mechanical quality factor. With further optimization, we expect a higher output power in the tens of micro watts range. The compatible fabrication process shows a promise for applications within the wireless sensor networks technology.

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