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Minimization of the transformer inter-winding parasitic capacitance for modular stacking power supply applications

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Keywords

«Parasitic capacitance», «current transformers», «dc-dc power converters», «electromagnetic devices»

Abstract

In an isolated power supply, the inter-winding parasitic capacitance plays a vital role in the mitigation of common mode noise currents created by fast voltage transient responses. The lower the transformer inter-winding capacitance, the more immune the power supply is to fast voltage transient responses. This requirement is even more critical for modular stacking applications in which multiple power supplies are stacked. This paper addresses the issue by presenting a detailed analysis and design of an unconventional isolated power supply that uses a ring core transformer with a very low inter-winding parasitic capacitance of 10 pF. Considering its output power of 300 W, this approach yields about 0.033 pF/W inter-winding capacitance over output power, approximately thirty times lower than existing approaches in the literature. This makes the converter a suitable solution for modular stacking of fast voltage switching applications. Mathematical derivation of the inter-winding capacitance and experiments are carried out to prove the validity of the approach.

Introduction

In isolated power supply applications, the transformer parasitic capacitance can have a significant effect to the converter operation [1-2]. Some of the adverse effects are distortion of the current waveform on the excitation side or a decrease in the overall converter efficiency. Subjected to high-voltage stresses, the inter-winding capacitance causes leakage currents and, consequently, EMI problems [3-6]. However, most publications about the transformer design concern the reduction in leakage inductances and high-frequency winding losses, while winding capacitances have rarely been considered effectively. Limiting the inter-winding capacitance is critical for stacking of power supplies because large inter-winding capacitance creates a significant amount of common mode noise at high frequency [6-7]. Existing transformers in a 1.2 kW converter design are reported to have 1.5 nF inter-winding capacitance [8]. An E-core transformer used in fly-back converter with a power rating of 30 W is reported in [9] to have 34 pF of inter-winding capacitance.

One of the primary applications of this work is supplying energy for ultra-fast tracking converters. Fig. 1 shows a configuration in which multiple modules of the proposed power supply provide energy to multiple modules of the ultra-fast tracking converter. The ultra-fast tracking converters are typical of

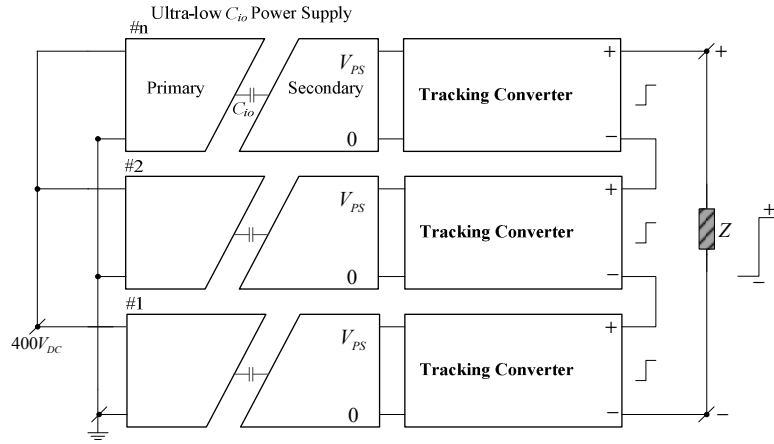


Fig. 1. A typical modular stacking application of power supplies.

radio frequency power amplifiers used in communication system based stations [10]. Due to the high dv/dt at the output of the tracking converters, there will be a large amount of conductive common mode current draw from their output. This current is linearly proportional to the input-output capacitance of the power supply:

$$i_{com} = C_{io} \frac{dV}{dt}. \quad (1)$$

Take, for example, a configuration with three stacked power supply-tracking converters. The tracking converter outputs are connected in series to increase the voltage. The rate of change at the output voltage is $1000 \text{ V}/\mu\text{s}$. Suppose we have a change from 0 to 1000 V in one micro second. The first converter output experiences a change of $333 \text{ V}/\mu\text{s}$. The second converter output experiences a change of $666 \text{ V}/\mu\text{s}$. The third one experiences a change of $1000 \text{ V}/\mu\text{s}$. The coupling current through the circuit input-to-output parasitic capacitance is as follows.

For the first converter:

$$i_{common1} = C_{io} \frac{dV}{dt} = 10 \text{ pF} \frac{333 \text{ V}}{1 \mu\text{s}} = 3.33 \text{ mA}. \quad (2)$$

For the second converter:

$$i_{common2} = C_{io} \frac{dV}{dt} = 10 \text{ pF} \frac{666 \text{ V}}{1 \mu\text{s}} = 6.66 \text{ mA}. \quad (3)$$

For the third converter:

$$i_{common3} = C_{io} \frac{dV}{dt} = 10 \text{ pF} \frac{1000 \text{ V}}{1 \mu\text{s}} = 10 \text{ mA}. \quad (4)$$

These currents are drawn from the tracking converters' output. Therefore, they distort the output current waveforms of the tracking converters, and the performance of the tracking is impaired. The adverse effects become worse when the number of stacked power supplies increases. Therefore, in order to rapidly change the tracking converter output voltage, the circuit input to output parasitic capacitance must be minimized, especially in modular stacking power converter applications. Note also that having minimal circuit input-to-output parasitic capacitance provides an advantage not only for fast changing voltage applications but also for other slower dynamic converters in terms of conducted noise immunity.

This paper studies the converter topology in Fig. 2, which was first presented in [1]. The primary goal is to attain a low transformer inter-winding parasitic capacitance; specifically, 10 pF in a 300 W output power design. Mathematical derivation of the transformer inter-winding capacitance and circuit operation will be presented.

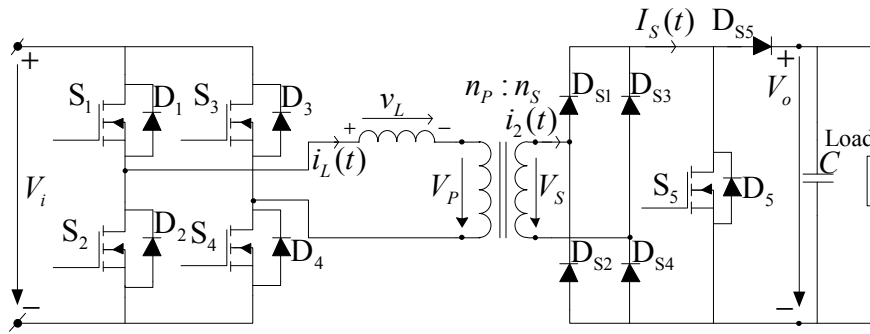


Fig. 2. Topology of the examined converter.

Circuit operation

Suppose that at the input, a power factor correction converter that converts a single phase 220 V ac into 400 V dc is used as the upstream converter. The magnitude of input voltage is therefore 400 V dc. The output voltage is 60 V dc. The output current is designed to be 5 A dc maximum. The maximum output power that is available in the output terminals is 300 W. Higher output voltage or higher output current can be achieved by stacking multiple converters in series or parallel.

The design of a transformer that possesses very low inter-winding capacitance normally involves loose coupling of the transformer windings. This results in the transformer having a relatively high leakage inductance. This high leakage inductance must be utilized with a proper selection of a suitable topology. Examples of suitable topologies are resonant converters [11-12] and the dual active bridge converter [13-14]. The proposed topology in Fig. 2. is, to some extent, similar to a single active bridge [15-16]. However, there are differences in the secondary side configuration and large differences in the control approach compared to those existing topologies. A single active bridge converter does not have the shunt switch as in the proposed converter. All of the control of the output voltage and output current in a single active bridge converter are performed on the primary side. On the contrary, with the utilization of the shunt switch S_5 as in the proposed topology, it is possible to control the output voltage independently on the secondary side; the advantage is the elimination of any necessary control feedback from one side to the other.

Existing control approaches in isolated power supplies usually involve feedback from one side to the other across the isolation boundary [11-16]. These approaches, however, introduce additional parasitic capacitance from the feedback elements, such as high frequency transformers and opto-couplers, which increase the total circuit input-to-output capacitance and degrade the immunity against fast step voltages. For that reason, in this paper, a control approach without isolated feedback is adopted to achieve minimum circuit input-to-output parasitic capacitance and maximum immunity to fast step voltage responses. The block diagram of the proposed circuit layout is shown in Fig. 3.

There are two control loops whose block diagrams are shown in Fig. 4. The secondary side controller regulates the output voltage to be constant at 60 V. The output voltage is sensed by a voltage divider and compared to a hysteresis reference to switch on and off the shunt switch S_5 . When the switch S_5 is on, shunting the secondary side, the converter operates in its shunt mode (see Fig.5a,c), and the output voltage decreases. Vice versa, when S_5 is off, the converter operates in its power mode, which is shown in Fig. 5b,c; the output voltage increases. In the primary side control, the primary side current i_L is sensed. It is rectified and filtered to produce a rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analog proportional-integrator (PI) controller. The output of the PI controller is fed to a voltage-controlled oscillator (VCO) that will automatically adjust the switching frequency to keep the rectified primary dc current to be constant at 1 A dc. The duty cycle of the primary switches is regulated at 50 %. With a turns ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc.

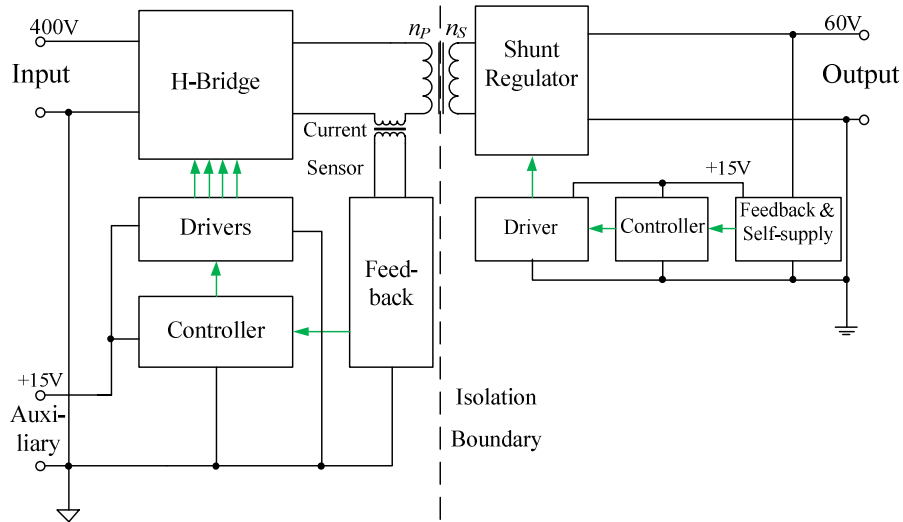


Fig. 3. Block diagram of the circuit layout.

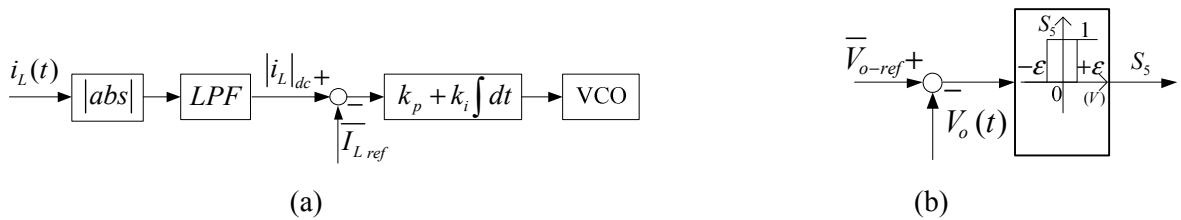


Fig. 4. Control block diagram: a) average current mode control in the primary side b) hysteresis control in the secondary side.

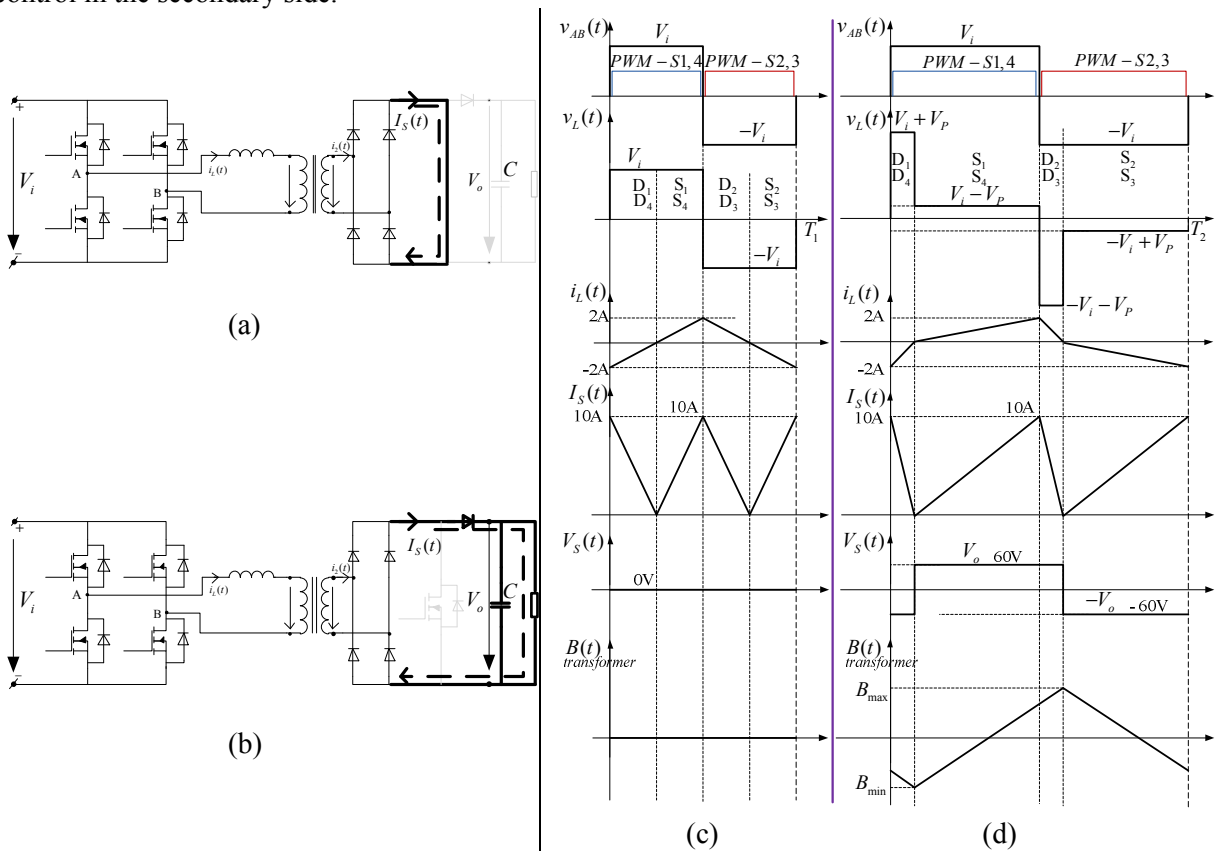


Fig. 5. Operation modes a) shunt mode, b) power mode. Analytical waveforms when converter operates in c) shunt mode, and d) power mode.

Calculation of the transformer inter-winding capacitance

The general structure of the transformer under test is illustrated in Fig. 6a, and the transformer prototype photo is in Fig. 6b. In its winding configuration, the winding with fewer turns will be placed in the geometrical center of the core. It forms a rectangular frame symmetrically around the core. The remaining winding, with more turns is wound tightly around the core. This is respectively the case of the secondary winding and primary winding in Fig. 6b.

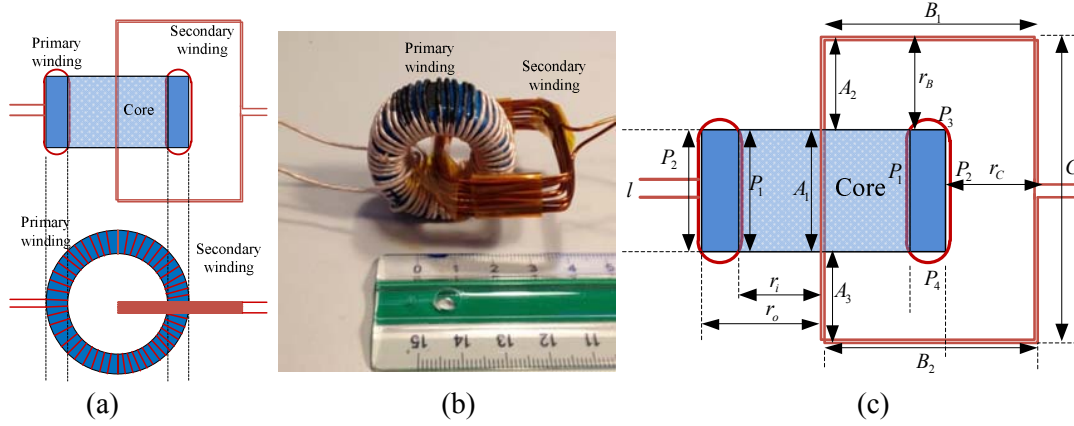


Fig. 6. Transformer structure: a) conceptual structure b) the transformer under test. c) winding geometry convention

It should be noted that, in general, ferrite does not cause a significant change in the parasitic capacitance. But ferrite with high conductivity material and very high operation frequency may cause a change on the parasitic capacitance. In this work, material N87 [17] is used for the ferrite core and is not considered to have high conductivity. Therefore, its effect on the parasitic capacitance can be ignored.

The inter-winding capacitance can be calculated by using the stored electric energy method, in which voltage distribution plays a vital role.

First, the inter-winding capacitance caused by the interaction between segment A_1 of the secondary winding through the core center to the parallel segments P_1 and P_2 of the primary winding (see Fig. 6c) will be calculated. Segments P_1 and P_2 are the winding parts around the perimeters of the inner ring and outer ring, respectively. Table I provides dimensional information of the core and winding with respect to the notations in Fig. 6c. The secondary has 11 turns stranded together, so each turn can be approximately treated as located in the center of the magnetic core, as shown in Fig. 7. The static capacitance between the inner primary turns and the secondary turns can be expressed as [4, 6]:

$$C_i = \frac{\epsilon_0 S}{r_i} = \frac{\epsilon_0 d \pi l}{2 \cdot r_i}, \quad (5)$$

where ϵ_0 is the permittivity of free air space, d is the diameter of each turns (the same size of wire is selected for both primary and secondary turns), l and r are the overlapped length and the distance between the inner primary turns and the secondary turns, respectively.

With respect to the outer primary turns, the static capacitance can be expressed with a different distance r_o ,

$$C_o = \frac{\epsilon_0 S}{r_o} = \frac{\epsilon_0 d \pi l}{2 r_o}. \quad (6)$$

Assuming that the voltage potential distribution along the primary turns varies linearly,

$$V_p[i] = \frac{i}{n_p - 1} V_p. \quad (i=0,1,2,3,\dots,n_p-1) \quad (7)$$

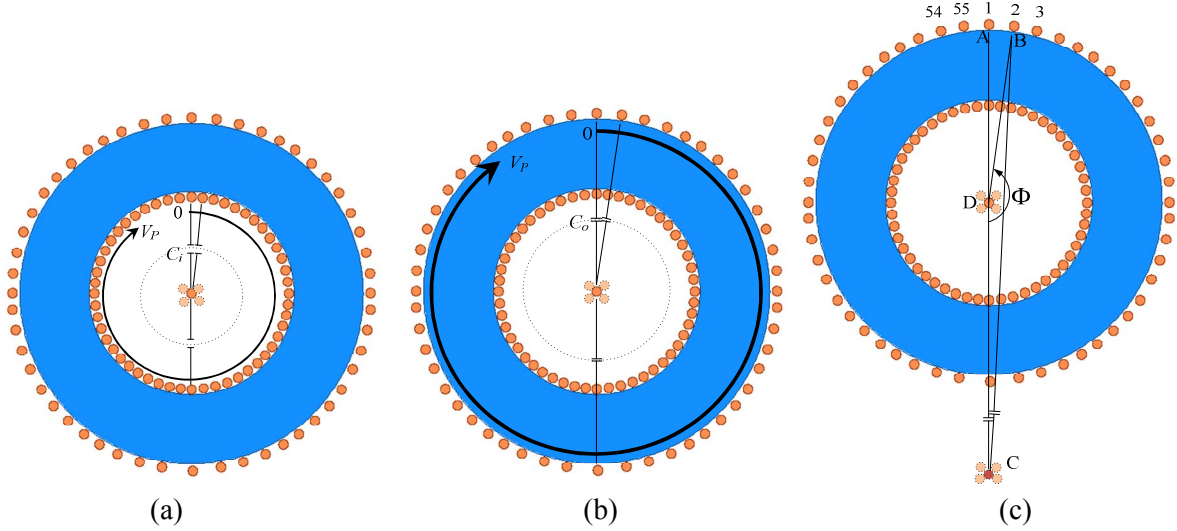


Fig. 7. 2-D cross-sectional top view: effect of parasitic capacitance from the secondary winding of a) segment A to the inner primary winding, b) segment A to the outer primary winding, c) segment C to the outer primary winding

Then the total stored electric energy between all secondary turns and the inner primary turns is:

$$\begin{aligned}
 E_i &= \frac{1}{2} C_i \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \left(\frac{V_p \cdot i}{n_p-1} - \frac{V_s \cdot j}{n_s-1} \right)^2 \\
 &= \frac{1}{4} C_i \cdot \left[\frac{V_p^2 \cdot n_s \cdot n_p \cdot (2n_p-1)}{3 \cdot (n_p-1)} + \frac{V_s^2 \cdot n_p \cdot n_s \cdot (2n_s-1)}{3 \cdot (n_s-1)} - V_p \cdot V_s \cdot n_p \cdot n_s \right]. \quad (8)
 \end{aligned}$$

With the same analytical approach, the total stored electric energy between all secondary turns and the outer primary turns can be achieved:

$$E_o = \frac{1}{4} C_o \cdot \left[\frac{V_p^2 \cdot n_s \cdot n_p \cdot (2n_p-1)}{3 \cdot (n_p-1)} + \frac{V_s^2 \cdot n_p \cdot n_s \cdot (2n_s-1)}{3 \cdot (n_s-1)} - V_p \cdot V_s \cdot n_p \cdot n_s \right]. \quad (9)$$

The capacitance caused by the side segments B_1 , B_2 to the primary winding is:

$$C_B = \frac{\epsilon_0 d \pi l_B}{2r_B}. \quad (10)$$

Segments B_1 and B_2 face the middle parts of the primary winding. It is appropriate to assume that there are five turns from the primary winding, which lie in segment P_3 or P_4 of Fig. 6c, facing segment B_1 and B_2 respectively. They are turn number $(n_p-1)/2-2$, $(n_p-1)/2-1 \dots$ to $(n_p-1)/2+2$. For example, in a specific design with 55 primary turns, or $n_p = 55$, they will correspond to turn number 25 to 29. The stored electric energy caused by B_1 and B_2 is:

$$E_B = 2 \cdot \left(\frac{1}{2} C_B \sum_{j=0}^{n_s-1} \sum_{i=(n_p-1)/2-2}^{(n_p-1)/2+2} \left(\frac{V_p \cdot i}{n_p-1} - \frac{V_s \cdot j}{n_s-1} \right)^2 \right). \quad (11)$$

Next, the contribution of segment C of the secondary winding to the outer ring of the primary winding is computed. Referring to Fig. 7c, it is helpful to express the distance from point C to the turns lying in the outer ring of the primary mathematically. In triangle CDB, distance \overline{CB} is related to other sides of the triangle by:

$$\begin{aligned}
 \overline{CB}^2 &= \overline{CD}^2 + \overline{BD}^2 - 2\overline{CD}\overline{BD}\cos(\Phi) \\
 &= (r_i + r_o)^2 + r_o^2 - 2(r_i + r_o)r_o \cos(\pi - 2\pi/n_p). \quad (12)
 \end{aligned}$$

Therefore, distance from C to the i^{th} turn of the outer-primary winding is (see Fig. 7c)

$$r_{\text{Cout},i} = \sqrt{r_o^2 + (r_o + r_i)^2 - 2r_o(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_p})}. \quad (i = 0, 1, 2, 3, \dots, n_p - 1) \quad (13)$$

The capacitance from segment C of the secondary winding to the turn number i^{th} of the outer primary winding is:

$$C_{C_{out},i} = \frac{\varepsilon_o d \pi l_c}{2r_{C_{out},i}} = \frac{\varepsilon_o d \pi l_c}{2\sqrt{r_o^2 + (r_o + r_i)^2 - 2r_o(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_p})}}. \quad (i = 0, 1, 2, 3, \dots, n_p - 1) \quad (14)$$

The total stored energy caused by segment C of secondary winding to the outer side of primary winding is then:

$$\begin{aligned} E_{C_{out}} &= \frac{1}{2} \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} C_{C_{out},i} \left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1} \right)^2 \\ &= \frac{1}{2} \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \frac{\varepsilon_o d \pi l_c}{2\sqrt{r_o^2 + (r_o + r_i)^2 - 2r_o(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_p})}} \left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1} \right)^2. \end{aligned} \quad (15)$$

Similarly, the stored energy caused by segment C of secondary winding to the inner side of primary winding is:

$$E_{C_{in}} = \frac{1}{2} \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} C_{C_{in},i} \left(\frac{V_p \cdot i}{n_p - 1} - \frac{V_s \cdot j}{n_s - 1} \right)^2, \quad (16)$$

where

$$C_{C_{in},i} = \frac{\varepsilon_o d \pi l_c}{2\sqrt{r_i^2 + (r_o + r_i)^2 - 2r_i(r_o + r_i)\cos(\pi - \frac{i2\pi}{n_p})}}. \quad (i = 0, 1, 2, 3, \dots, n_p - 1) \quad (17)$$

The total stored electric energy is then

$$E_{total} = E_i + E_o + E_B + E_{C_{in}} + E_{C_{out}} = \frac{1}{2} \cdot C_{eq} \cdot (V_p - V_s)^2. \quad (18)$$

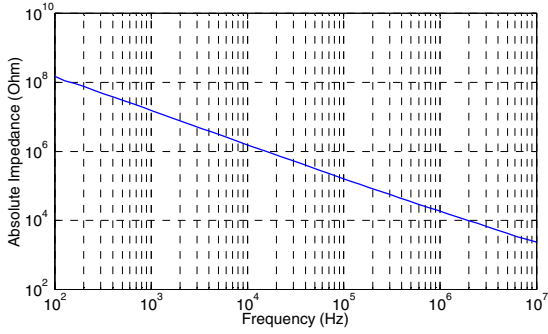
The calculated inter-winding capacitance based on the parameters on Table I is 10 pF. Table II shows the calculated energy and capacitance. It is observed that segment A_1 dominates the stored energy, and the contributions of segments B_1 and B_2 are negligible. The design guideline is that increasing the core geometry and increasing distance from segment C to the core will effectively reduce the inter-winding capacitance.

Table I: Parameters of the magnetic core and winding geometries

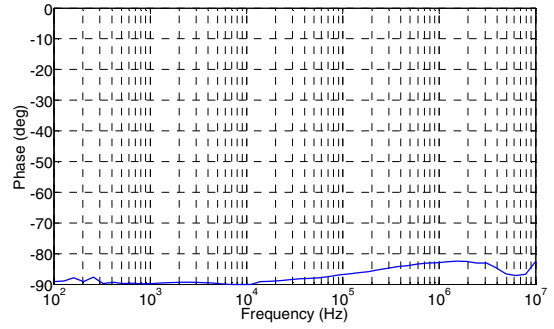
ε_0	8.85×10^{-12} F/m
d	1 mm
l	16 mm
r_i	11.5 mm
r_o	18 mm
n_p	55
n_s	11
V_p	300 V
V_s	60 V
r_B	12 mm
l_B	6.5 mm
l_c	16 mm

Table II: Calculated energy and inter-winding capacitance

Parameters	E_i	E_o	E_B	E_{Cin}	E_{Cout}	E_{total}	C_{eq}
Value	1.3e-7 J	8.4e-8 J	1.1e-9 J	3.8e-8 J	3.2e-8 J	2.9e-7 J	9.97e-12 F
$/ E_{total}$	45.9%	29.3%	0.4%	13.1%	11.3%	100%	



(a)



(b)

Fig. 8. Inter-winding impedance measurement: a) magnitude, b) phase.

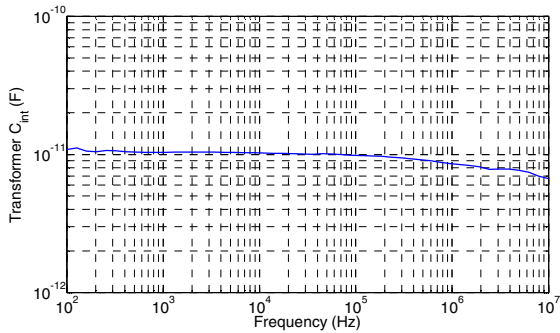


Fig. 9. Interpreted parasitic capacitance.

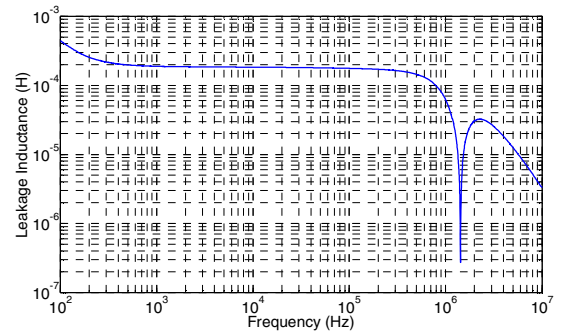
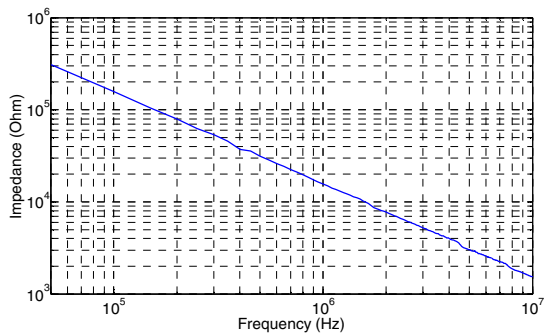
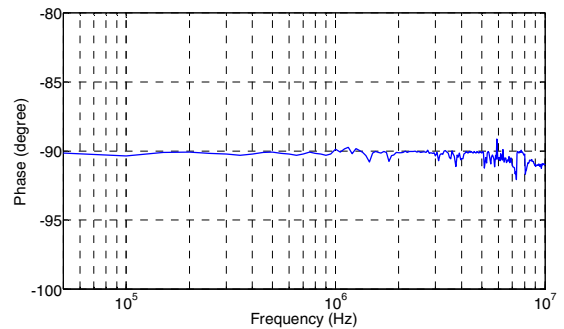


Fig. 10. The leakage inductance.



(a)



(b)

Fig. 11. Circuit input-to-output impedance measurement Left: magnitude, Right: phase.

Experimental results

The measurement of the transformer is carried out by the Agilent 4294A Precision Impedance Analyzer, which has a precision of $\pm 3\%$ as claimed by the manufacturer. The measured impedance and phase between the primary and secondary windings, with each winding terminal shorted, are shown in Fig. 8. The measured inter-winding capacitance is shown in Fig. 9. It is shown that the measured capacitance is around 10 pF from 3 kHz up to 10 MHz. The calculation and the measurements, are therefore, matched reasonably well with each other. The resulting leakage inductance is 170 μH , which is shown in Fig. 10. In the end, the overall design goal is fulfilled, which is to have a very low inter-winding capacitance of 10 pF. Fig. 11 shows the impedance magnitude and phase of the circuit. These were found by measuring the impedance between the input and the output terminals of the converter with the input and output shorted to their own return grounds. The measured circuit input-to-output parasitic capacitance is deduced from these measurements and is shown in Fig. 12. Its value is 10 pF, the same as with the inter-winding capacitance of the transformer. As a result, it can be said that the proposed circuit layout, control, and transformer design has minimized the total circuit input-to-output capacitance, making it a powerful solution for modular stacking applications. Finally, Figs. 13 and 14 show the experimental operation from power mode to shunt mode and from shunt mode to power mode. It can be seen that experiments match very well to the analysis presented in the circuit operation section. The feasibility of the converter is therefore validated.

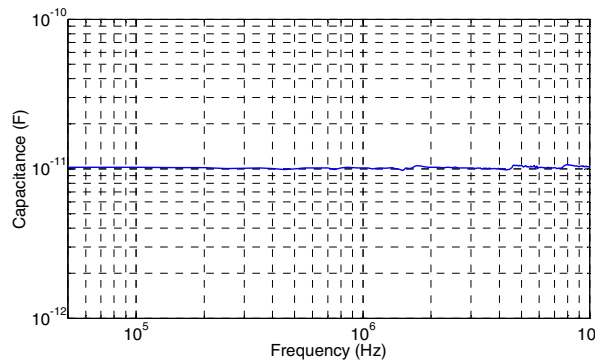


Fig. 12. Circuit input-to-output parasitic capacitance.

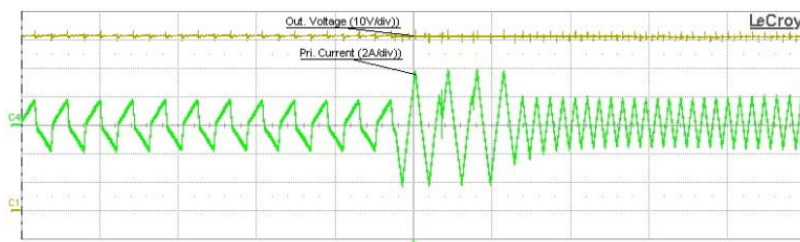


Fig. 13. Transient response from power mode to shunt mode: output voltage (10V/div), inductor current (2A/div), time scale: 20 $\mu\text{s}/\text{div}$.

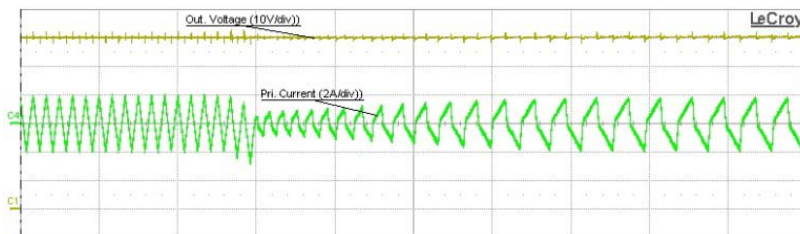


Fig. 14. Transient response from shunt mode to power mode: output voltage (10V/div), inductor current (2A/div), time scale: 20 $\mu\text{s}/\text{div}$.

Conclusion

The resulting transformer has a parasitic capacitance of 10 pF, which is extremely low compared to other existing isolated power converters of similar power rating. The mathematical derivation yields acceptably accurate results that agree well with measurement. The results also provide guidelines about how the transformer geometry should be considered when the inter-winding capacitance is of concern. Finally, the overall result achieved with the prototype provides very high immunity to the common mode noise current caused by fast voltage transients, and therefore makes the converter suitable for modular stacking applications.

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