



Forward Error Correcting Codes for 100 Gbit/s Optical Communication Systems

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Forward Error Correcting Codes for 100 Gbit/s Optical Communication Systems

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Abstract

This PhD thesis addresses the design and application of forward error correction (FEC) in high speed optical communications at the speed of 100 Gb/s and beyond. With the ever growing internet traffic, FEC has been considered as a strong and cost-effective way to improve the quality of transmission (QoT) to meet the increasing demand on the quality of service (QoS). The scientific content presented in this thesis tackles three major research problems. Firstly, the study of FEC codes becomes essential to get a high coding gain (CG) suited for 100 Gb/s optical fiber links. Secondly, low-complexity low-power-consumption FEC hardware implementation plays an important role in the next generation energy efficient networks. Thirdly, a joint research is required for FEC integrated applications as the error distribution in channels relies on many factors such as non-linearity in long distance optical fiber links, cross-talks in wavelength division multiplexing (WDM) setups and so on.

FEC with a product code structure has been investigated theoretically and experimentally. The iterative decoding method applied to FEC codes in a product code structure can effectively reduce the bit error rate (BER). Proposals on beyond bound decoding (BBD) and adaptive FEC algorithms are also presented. BBD is an add-on in some cases to help with the further reduction of the BER.

FEC aided transmission in a short distance data center link is presented. With the help of FEC and a low cost vertical-cavity surface-emitting laser (VCSEL), 100 Gb/s raw data rate is achieved, which demonstrates the possibility of building a high speed short-range link with cheap elements. FEC integration in a WDM metropolitan transmission link is also presented. The experimental performance of FEC in both linear and nonlinear regimes is demonstrated in a dual polarization (DP) 16-ary quadrature amplitude modulation (16QAM) and

coherent detection based WDM transmission over 741 km at a raw data rate of 88.8 Gb/s. FEC can compensate in both regimes, but the channel analysis does not show an additive white Gaussian noise (AWGN) channel. Besides, a denser WDM grid changes the shape of the BER curve based on the analysis of the experimental results, which requires a stronger FEC code.

Furthermore, a proof-of-the-concept hardware implementation is presented. The tradeoff between the code length, the CG and the complexity requires more consideration in the FEC code choice in a certain application. The presented adaptive FEC is one of the few published research results to enable the efficient bandwidth usage as the transmission channels can be affected by many factors.

In conclusion, the results presented in this thesis consist of proposals on FEC codes and their associated experimental demonstration and hardware implementation. The demonstrated high CG, flexibility, robustness and scalability reveal the important role of FEC techniques in the next generation high-speed, high-capacity, high performance and energy-efficient fiber-optic data transmission networks.

Resumé

Denne PhD afhandling omhandler design og anvendelse af fejlkorrigerende koder (Forward Error Correction - FEC) i optisk højhastigheds-kommunikation med transmissionshastigheder på 100 Gb/s og derover. Med den konstant voksende internettrafik er FEC blevet betragtet som en vigtig og cost-effektiv metode til forbedring af transmissionskvaliteten (quality of transmission - QoT) med henblik på at imødekomme de voksende krav til “quality of service”(QoS). De videnskabelige resultater der præsenteres i denne afhandling tackler tre grundlæggende problemer. For det første er det nødvendigt at studere fejlkorrigerende koder for at opnå det høje “coding gain (CG)” der er brug for med en 100 Gb/s optisk forbindelse. For det andet spiller hardwareløsninger med lav kompleksitet og lavt energiforbrug en vigtig rolle i næste generations energi-effektive netværk. For det tredje kræves en samlet undersøgelse af kommunikationssystemer med FEC da fordelingen af transmissionsfejl afgøres af mange forskellige faktorer som fx ulineariteter i langdistance fiberoptiske forbindelser, krydstale i WDM systemer og så videre.

Fejlkorrektion med produktkoder er undersøgt såvel teoretisk som eksperimentelt. Den iterativ dekodningsmetode der er anvendt til fejlkorrigerende koder i en produktkode struktur kan effektivt reducere bitfejsandsynligheden (Bit Error Rate - BER). Forslag til dekodning ud over de teoretiske grænser (Beyond Bound Decoding - BBD) og adaptive dekodningsalgoritmer bliver præsenteret. BBD er en udvidelse der kan anvendes i visse tilfælde for yderligere at reducere BER.

Transmission med FEC for kort datacenter links præsenteres. Ved hjælp af FEC og billige Vertical-cavity surface-emitting laser (VCSEL) kan man opnå rå datahastigheder på 100 Gb/s, hvilket demonstrerer mulighederne for at konstruere et højhastigheds korttrækkende link med billige elementer.

Integration af FEC i WDM link for metronetværk bliver også præsenteret. Den eksperimentelle ydeevne af FEC både i det lineære og det ulineære områder demonstreres med dual polarisation 16QAM og transmission over 741 km med WDM baseret på kohærent detektion og en rå datahastighed på 88,8 Gb/s. FEC kan kompensere i begge områder, men analyse af transmissionskanalen viser støj der ikke er additiv hvid Gaussisk. Desuden ændrer et tættere grid i WDM kurveformerne for de eksperimentelle resultater så der kræves en kraftigere fejlkorrigerende kode.

Endelig præsenteres en “proof-of-the-concept” hardware implementering. Trade-off mellem kodelængde, CG og kompleksitet kræver yderligere overvejelse af FEC system for visse anvendelser. Det adaptive kodningssystem der præsenteres er et af de få publicerede forskningsresultater der muliggør effektiv brug af båndbredde når transmissionskanalen påvirkes af mange forskellige faktorer.

Som konklusion indeholder denne afhandling forslag til fejlkorrigerende koder med eksperimentelle resultater og hardwareimplementering. Det påviste høje coding gain, fleksibilitet, robusthed og mulighed for skalering understreger den vigtige rolle for FEC tekniker i næste generations højhastighed, stor kapacitet, høj ydeevne og energieffektive fiber-optiske data transmissions netværk.

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Summary of original work

Original publications included in this PhD thesis

- [A] **Bomin Li**, D. Zibar, Knud J. Larsen, and I. Tafur Monroy, “Over 10 dB Net Coding Gain Based on 20% Overhead Hard Decision Forward Error Correction in 100G Optical Communication Systems,” in *37th European Conference on Optical Communication (ECOC 2013)*, paper Tu.6.A.3, 2011.
- [B] **Bomin Li**, Knud J. Larsen, J. J. Vegas Olmos, D. Zibar, and I. Tafur Monroy, “Application of Beyond Bound Decoding for High Speed Optical Communications,” in *Asia Communications and Photonics Conference 2013 (ACP 2013)*, paper AF4C.6, 2013.
- [C] Cristian Prodaniuc, **Bomin Li**, and Knud J. Larsen, “Adaptive Forward Error Correction in High Speed Optical Communications,” *Global Journal on Technology*, vol. 3, 2013.
- [D] **Bomin Li**, Knud J. Larsen, Darko Zibar and I. Tafur Monroy, “Forward Error Correction for 400 Gbps High Speed Optical Fiber Links,” submitted to *IEEE Communications Letters*.
- [E] Roberto Rodes, Michael Müller, **Bomin Li**, Jose Estaran, Jesper Bevensee Jensen, Tobias Gruendl, Markus Ortsiefer, Christian Neumeyr, Juergen Roskopf, Knud J. Larsen, M.-C. Amann, and I. Tafur Monroy, “High-Speed 1550 nm VCSEL Data Transmission Link Employing 25 GBd 4-PAM Modulation and Hard Decision Forward Error Correction,” *Journal of Lightwave Technology*, vol. 31, no. 4, pp. 689–695, 2013.

- [F] **Bomin Li**, Robert Borkowski, Jose Estaran, Molly Piels, Darko Zibar, Knud J. Larsen, and I. Tafur Monroy, “Experimental Performance of FEC for Linear and Nonlinear Optical Fiber Transmissions,” submitted to *IEEE Photonics Technology Letters*.

Contributions closely related to this PhD thesis

- [e] R. Rodes, J. Estaran, **B. Li**, M. Muller, J. B. Jensen, T. Gruendl, M. Ortsiefer, C. Neumeyr, J. Roskopf, K. J. Larsen, M.-C. Amann and I. Tafur Monroy, “100 Gb/s single VCSEL data transmission link,” in *2012 Optical Fiber Communication Conference (OFC 2012)*, paper PDP5D.10, 2012.

Remaining scientific contributions published during this PhD

- [1] J. J. Vegas Olmos, Lau Frejstrup Suhr, **Bomin Li**, and I. Tafur Monroy, “Five-level polybinary signaling for 10 Gbps data transmission systems,” *Optics Express*, vol. 21, no. 17, pp. 20417–20422, August. 2013.
- [2] J.J. Vegas Olmos, L.F. Suhr, **Bomin Li**, and I. Tafur Monroy, “10 Gbps Five Levels Polibinary Signaling for Short Range and Access Networks,” in *Asia Communications and Photonics Conference 2013 (ACP 2013)*, paper AW4G.3, 2013.

Contents

Abstract	i
Resumé	iii
Acknowledgements	v
Summary of original work	vii
Original publications	vii
Closely related contributions	ix
Remaining contributions	x
1 Introduction	1
1.1 Outline of the thesis	1
1.2 Motivation	2
1.3 Advanced techniques in high speed optical communications	3
1.3.1 High order modulation format	4
1.3.2 Coherent detection	5
1.3.3 Wavelength devision multiplexing	6
1.4 Forward error correction	8
1.4.1 Basics	8
1.4.2 Code overview	10
1.4.3 Adaptive algorithm	11
1.4.4 Hardware implementation	12
1.4.5 Applications	14
2 State of the art	15
2.1 Candidate codes	15
2.2 Adaptive FEC	18
2.3 Hardware implementation	19
2.4 FEC application	23

3	Description of papers	27
3.1	Product code	27
3.2	Adaptive FEC	29
3.3	Hardware implementation	29
3.4	FEC application	30
4	Product codes and their decoding	33
4.1	Basics of product codes	33
4.1.1	Code construction	33
4.1.2	Iterative decoding and error floor	34
4.1.3	Code performance	36
4.2	Latest achievements	37
4.2.1	Single chip FPGA implementation	37
4.2.2	FEC performance affected by channel wavelength spacing in WDM systems	40
5	Summary	45
5.1	Conclusions	45
5.1.1	Product code systems	45
5.1.2	Adaptive algorithm	46
5.1.3	Hardware implementation	46
5.1.4	FEC application	46
5.2	Future work	47
	Bibliography	61
	List of acronyms	63
	Paper [A]: Over 10 dB Net Coding Gain Based on 20% Overhead Hard Decision Forward Error Correction in 100G Optical Com- munication Systems	67
	Paper [B]: Application of Beyond Bound Decoding for High Speed Optical Communications	71
	Paper [C]: Adaptive Forward Error Correction in High Speed Op- tical Communications	75
	Paper [D]: Forward Error Correction for 400 Gbps High Speed Op- tical Fiber Links	81

Paper [E]: High-Speed 1550 nm VCSEL Data Transmission Link Employing 25 GBd 4-PAM Modulation and Hard Decision Forward Error Correction	85
Paper [F]: Experimental Performance of FEC for Linear and Non-linear Optical Fiber Transmissions	93

Chapter 1

Introduction

1.1 Outline of the thesis

This thesis is a summary of my PhD study performed at the department of photonics engineering, technical university of Denmark. Chapter 1 is an introduction to the motivation, the advanced techniques as well as FEC in high speed optical communications. Section 1.1 is the outline of the thesis, followed by the motivation in section 1.2. Section 1.3 covers the basics of high order modulation format, coherent detection and WDM that build the system framework for FEC application with proposed codes in this thesis. Section 1.4 is an overview of the concept, basics, algorithms, implementations and applications of FEC. Chapter 2 reports on the current state of the art in the key areas as below: the code development in section 2.1, the adaptive algorithm in section 2.2, the hardware implementation in section 2.3 and the applications in section 2.4. Chapter 3 describes the novelty behind each of the papers included in this thesis. The individual author contribution is included as well. Chapter 4 covers the basics of a FEC code with a product code structure. Latest achievements are included as well. The thesis is concluded by chapter 5. Section 5.1 summarizes the main achievements of the presented work. An outlook on future research options is presented in section 5.2.

1.2 Motivation

In its flagship regulatory report 2013 [1], International Telecommunication Union (ITU) confirms continued rapid expansion of tech markets worldwide. It points out that rapid growth of broadband has seen global IP traffic skyrocket from around one petabyte 20 years ago to an estimated 44,000 petabytes (44 exabytes) at end 2012. As an indicator of the sheer volume this represents, that amount of data would take 1,100 years to download over a 10 Mb/s broadband link, or more than 200,000 years over a dial-up connection. Looking forward in the coming years, Cisco Visual Networking Index forecasts that by the end of 2015, annual global IP traffic will exceed one zettabyte (capacity equivalent to one billion modern hard disks 1 terabyte each) and will reach 1.4 zettabyte per annum by 2017 [2]. Global Internet Protocol (IP) traffic has increased fourfold over the past 5 years, and will increase threefold over the next 5 years. Overall, IP traffic will grow at a compound annual growth rate (CAGR) of 23 percent from 2012 to 2017. Metro traffic will surpass long-haul traffic in 2014, and will account for 58 percent of total IP traffic by 2017.

Rich-bandwidth services such as video on demand, high definition TV and cloud computing are pushing the needs for improvements in optical transport network (OTN). This fast growing capacity consequently results in a need of higher speed or more spectrum-efficient transmission systems. High-order modulation format and coherent detection techniques are reappearing as an area of interest due to their capability to provide the capacity towards 400 Gb/s and beyond [3]. These techniques enable a high spectrum efficiency with the cost of increased complexity, which eventually leads to a higher implementation cost. WDM techniques are also intensively investigated. By multiplexing multiple optical carriers onto a single fiber with different wavelength lasers, the capacity is multiple times folded.

Yet, in the meanwhile higher loss should be expected. Losses due to for example chromatic dispersion (CD), polarization mode dispersion (PMD), nonlinear loss (NL), inter-channel interference (ICI) and intra-channel interference decrease the system performance. FEC, among many innovative methods to compensate losses, plays an important role as a cost effective solution to obtain the preferred transmission quality by using error correcting codes (ECC) [4]. It introduces redundancy in the transmission sequence to protect the valid information

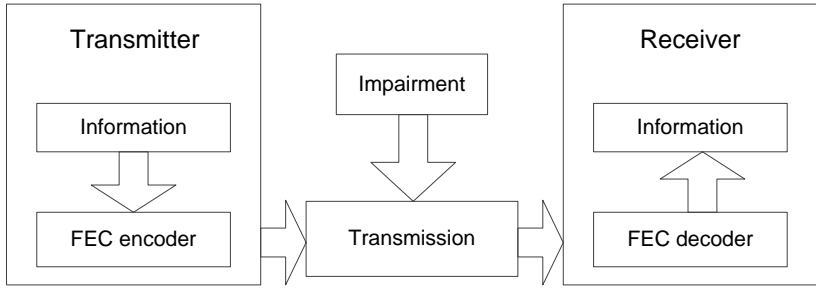


Figure 1.1: FEC integration in a transmission setup.

from being corrupted. Fig. 1.1 shows the framework of the FEC integration in a transmission setup. At the transmitter end, the information bits are encoded by adding a certain number of redundant bits based on an error-correcting mechanism. At the receiver end, within its error correcting capability, the decoder is able to recover the original information sequence by correcting errors introduced in the transmission. In today's and next generation coherent optical communication systems, powerful FEC codes will be necessary to achieve high net coding gain (NCG) larger than 10 dB at a reference BER of 10^{-15} .

FEC technology has been intensively employed in optical communication systems. By FEC integration, the system performance is improved with the cost of reduced bandwidth usage and added FEC encoder and decoder implementation expenses. Therefore, to find a balance, the candidate FEC codes have to be evaluated by but not limited to the parameters as below:

- Coding gain;
- Error floor;
- Redundancy;
- Implementation complexity;
- Encoding and decoding delay.

Details of FEC are included in section 1.4.

1.3 Advanced techniques in high speed optical communications

This chapter covers some key technologies that enable optical communications beyond 100 Gb/s. High order modulation format, coherent

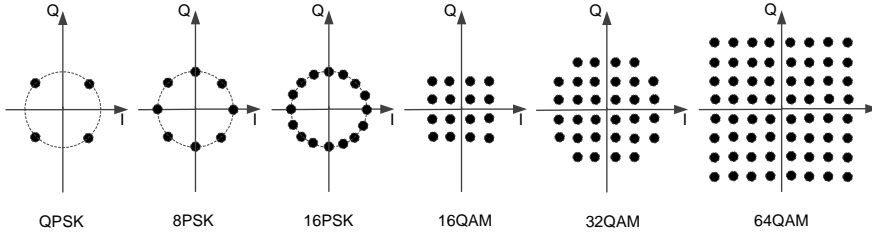


Figure 1.2: Constellation diagrams of selected higher-order modulation formats.

detection and WDM are explained in section 1.3.1, section 1.3.2 and section 1.3.3, respectively. However, there are many other techniques that are not covered by this thesis.

1.3.1 High order modulation format

High order modulation format is a modulation format that maps m bits to a symbol, where m is usually 4 or more. In the early nineties of last century, proposals of different modulation formats based on the modulation of both quadratures did not attract much attention, due to the unavailability of complex high speed electronics. Besides, the emergence of Erbium doped fiber amplifier (EDFA) offers immediate modulation/direct detection (IM/DD) systems to scale to a higher capacity. In the late nineties, driven by the interest in the transmission of longer distance and higher robustness, differential binary phase shift keying (DBPSK) became attractive because of its property of robustness against non-linearity affect [5]. High order modulation format started to play an important role when fiber optics systems evolved to 100 Gb/s. By mapping several bits to a symbol, higher spectrum efficiency and lower symbol rate can be achieved. This overcame the barrier of system upgrade limited by relatively low speed electronics. Fig. 1.2 shows some constellation diagrams of selected high-order modulation formats of phase shift-keying (PSK) and QAM. From left to right these modulation formats are quadrature phase shift keying (QPSK), 8-ary PSK (8PSK), 16-ary PSK (16PSK), 16-ary QAM (16QAM), 32-ary QAM (32QAM) and 64-ary QAM (64QAM).

QPSK was the first high order modulation format being investigated. It can provide good performance over long distance optical link and it doubles the spectrum utilization. This modulation format in

combination with digital equalization was demonstrated to have high tolerance to CD and PMD [6]. Polarization division multiplexing (PDM) QPSK was treated as a spectrally efficient solution to 100 Gb/s and beyond [7].

Commercial PDM-QPSK coherent systems at 40 Gb/s and 100 Gb/s have been reported [8]. The ASIC implemented DSP performs all-electronic CD and PMD compensation, frequency and phase locking, and polarization de-multiplexing. Experiments have shown that coherent systems with advanced modulation format return an increase in capacity of around 1 dB per year [9]. The use of high spectrally efficient phase modulation to increase both per-channel interface rates and aggregate WDM capacities is the next evolutionary step [11]. Enabled by digital coherent receivers, 16QAM, 64QAM [12] and 256QAM [13] can be employed to meet the increasing capacity demand. A transmission of a 1.1 Tb/s super channel in 100 GHz optical bandwidth based on PDM-256QAM and spatially coupled FEC is presented in [10]. The accompanied issue of reduced Euclidean distances between constellation points is expected to be compensated by FEC and coded modulation [14, 15].

1.3.2 Coherent detection

Coherent detection is a signal detecting technique of phase locking to the carrier wavelength. As shown in Fig. 1.3, the polarization controlled input and reference signals are fed into 90° hybrid, where the reference signal is commonly generated by local oscillator (LO). The signals detected by balanced photo-detectors are sampled by high speed analog-to-digital-converters (ADCs) and processed by digital signal processing (DSP), where channel equalization, carrier and phase recovery, frame demodulation can all be done in the electrical domain. Linear and non-linear digital equalizers have been proven to be helpful in dispersion compensation, which relaxes the requirements for FEC code selection [16, 17]. Furthermore, as coherent detection conveys any information (amplitude, phase, and polarization) from the optical domain to the electrical domain, the compensation on linear impairment such as CD and PMD, can be performed straightforward. Nonlinearity can also be compensated with the cost of complicated algorithms, for example digital backpropagation (DBP) [18]. Enabled by this ability, high order modulation formats like QAM uses the complex plane more effi-

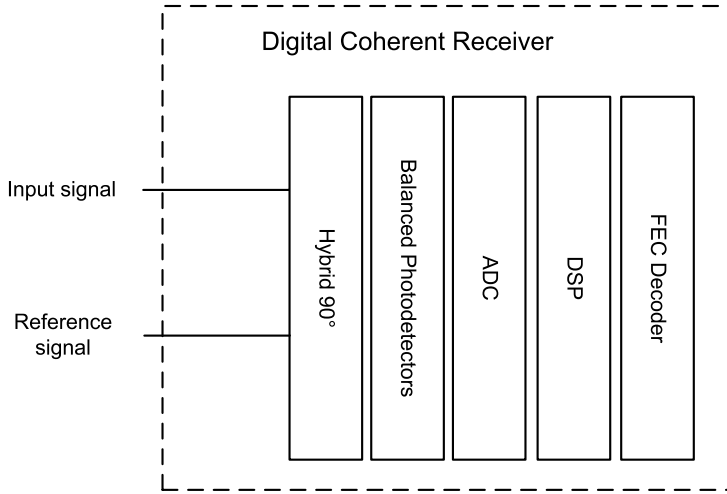


Figure 1.3: Coherent receiver.

ciently than the IM/DD format that is limited to the use of intensities. The coherent detection technique, together with high order modulation format, releases the demand of very high speed analog-to-digital converter (ADC) in 100 Gb/s transmission systems. FEC decoder is an option to further reduce the BER. The error correcting capability provided by the integrated FEC can reduce the pre-FEC BER from around $1.4 \cdot 10^{-2}$ and $4.3 \cdot 10^{-3}$ to 10^{-15} , respectively based on 20% and 7% overhead hard decision (HD) codes. Besides, the provided information by coherent detection enables soft decision (SD) FEC codes to achieve a higher coding gain compared to the same HD FEC codes, usually around 1.5 dB more.

1.3.3 Wavelength division multiplexing

WDM technology multiplexes a number of optical carriers onto a single fiber by using different wavelengths of laser light. With this method, the capacity in a single fiber channel is tens of times larger compared to using only one optical carrier in the single fiber channel. Early WDM was expensive and complicated to run. Coarse WDM (CWDM) systems provide up to 8 channels in the C-band of silica fiber around 1550 nm. The channel spacing grid for CWDM was standardized in ITU-T G.694.2 [21]. Dense WDM (DWDM) is also running in C-band, with a

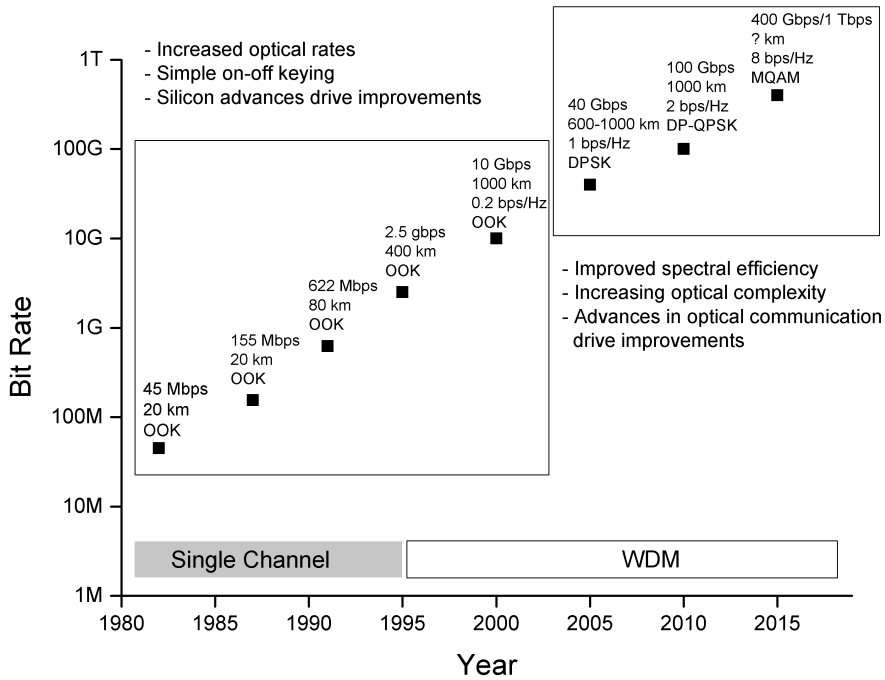


Figure 1.4: WDM development Overview [19].

higher number of channels. The fixed channel spacings ranging from 12.5 GHz to 100 GHz are defined in [22]. A typical system uses 40 channels with 100 GHz spacing, or 80 channels with 50 GHz spacing, or 160 channels with 25 GHz spacing. DWDM setups help to increase the capacity without the employment of high speed electronics (e.g. >40 Gb/s) and keep the compatibility with 10 Gb/s synchronous optical networking/synchronous digital hierarchy (SONET/SDH) equipment. Since the wavelengths are put close to each other, how to mitigate the crosstalk and inter-channel interference becomes an interesting topic.

Fig. 1.4 shows the development history of WDM technology in high speed optic-fiber transmissions. This figure is reproduced from the figure in [19]. Until the late 1990s, most optical networks were single-channel systems operating at a data rate of 10 Gb/s and below. Signals were modulated with the IM/DD format, also known as On-Off Keying (OOK). In late 1990s, WDM systems enabled capacity upgrade by transmitting multiple wavelengths in a single fiber. In 20th century, research on advanced modulation format and denser WDM transmission has managed to increase the capacity to 100 Gb/s. Even higher capac-

ity in future will be driven by the improvements in optical modulation, optical components, coherent detection, DSP, FEC and the arising topic on photonic integrated circuits (PICs) [23].

1.4 Forward error correction

FEC is considered as a cost effective method in high speed optical communications to achieve desired system performance. Today almost all applications have FEC considered as a part of the system in order to reach a certain BER with a low cost. This chapter provides an overview of various FEC aspects. Section 1.4.1 explains the basic concepts of FEC codes. Section 1.4.2 is an overview of different candidate codes. Section 1.4.3 discusses the concept of adaptive FEC. Section 1.4.4 covers the topic of hardware implementation. Section 1.4.5 shows examples of FEC applications.

1.4.1 Basics

A couple of important concepts that are often used in FEC are explained in this section.

Overhead

When FEC is integrated in a system, an ECC is applied to the original information sequence by adding redundancy. An information sequence of k bits or symbols is encoded to a longer sequence of n bits or symbols, while the original information sequence and the encoded sequence meet the requirement of one-to-one mapping. The code rate R is the ratio of bit rate without FEC to bit rate with FEC:

$$R = \frac{k}{n} \quad (1.1)$$

The overhead is the relationship of the redundancy and the information length:

$$oh = \frac{n - k}{k} = \frac{1}{R} - 1 \quad (1.2)$$

When the overhead increases, the net data rate, on the contrary, reduces if the line rate is fixed.

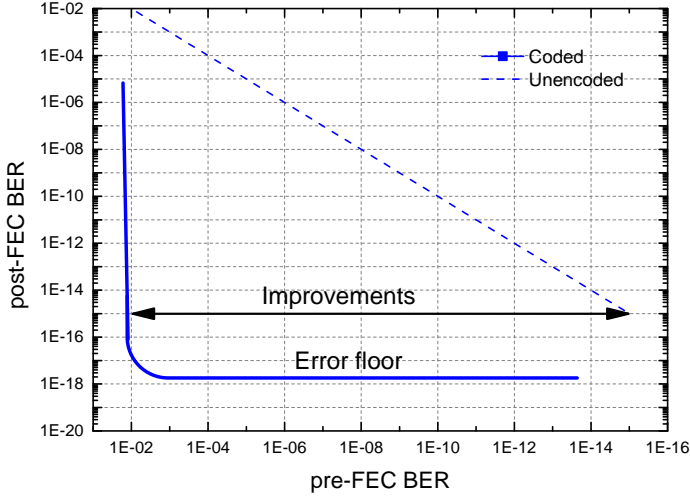


Figure 1.5: Coding gain.

Net coding gain

The definitions of CG and NCG can be found in ITU-T G.975.1 [20]. CG means the improvement of received optical sensitivity by using FEC, without considering penalty by bit rate increasing. NCG has bit rate increasing penalty considered in addition to the CG. As the code rate R is less than 1, a NCG is always smaller than the corresponding CG. NCG is characterized by both the code rate R , and the maximum allowable BER (B_{in}) of the input signal to the FEC decoder that can be reduced to a reference output BER ($B_{out} = B_{ref}$) by applying the FEC algorithm. Notice that NCG should refer to a binary symmetric channel with AWGN:

$$NCG = 20\log_{10}\left(\operatorname{erfc}^{-1}(2B_{ref})\right) - 20\log_{10}\left(\operatorname{erfc}^{-1}(2B_{in})\right) + 10\log_{10}(R) \quad (1.3)$$

with erfc^{-1} the inverse of the complementary error function :

$$\operatorname{erfc}(x) = 1 - \operatorname{erf}(x) \quad (1.4)$$

Fig. 1.5 shows an improvement on the pre-FEC BER axis between coded data and uncoded data. This improvement is translated into NCG when the corresponding pre-FEC BERs at two curves are plugged into the equation 1.3. Notice that the improvement is measured at a

post-FEC BER of 10^{-15} , where the pre-FEC BER of unencoded data is also 10^{-15} . In principle, the more NCG is, the better error correcting capability the code provides. Yet, the bit rate penalty is of great importance in real systems.

Error floor

Error floor is that the output BER of a FEC code based on a certain decoding algorithm is bounded by a threshold. The example shown in Fig. 1.5 is that the post-FEC BER is bounded by a value between 10^{-17} and 10^{-18} . It means that despite the effort of the decoder, this value is the best post-FEC BER this decoding algorithm can achieve for the code.

Besides the importance of NCG, a candidate code desires for an error floor below the reference post-FEC BER. The recommended post-FEC BER from Optical Internetworking Forum (OIF) is currently 10^{-15} [24]. A candidate code will not be regarded as suitable if it suffers from a high value error floor, for example 10^{-10} .

1.4.2 Code overview

In this section we will go through the candidate codes that are categorized into three generations. The first generation FEC uses classical HD codewords, mainly represented by Reed-Solomon (RS) code. This HD code with 6.7% overhead is a linear block code. RS(255, 239) is the most commonly used first generation FEC code, where 239 is the length of information symbols and 255 is the encoded length with redundancy. The error correcting theory shows that the minimum distance is 17 and it can correct up to 8 error symbols. It provides around 6 dB NCG for a post-FEC BER of 10^{-15} . RS (255, 239) is recommended for long-haul transmission as defined in ITU-T G.709 [25].

The second generation FEC uses also HD codes to provide a higher NCG, but with a more complicated algorithm. Fig. 1.6 shows an example of concatenated codes. At the transmitter side the information is first encoded by outer encoder and then by inner encoder. At the receiver side the decoding is done in an opposite way. Iterative decoding can be applied to concatenated codes. ITU-T G.975.1 lists some candidate codes for the second generation FEC. These HD codes have an overhead ranging from 6.7% to 25%, providing a NCG of around 8 to 10

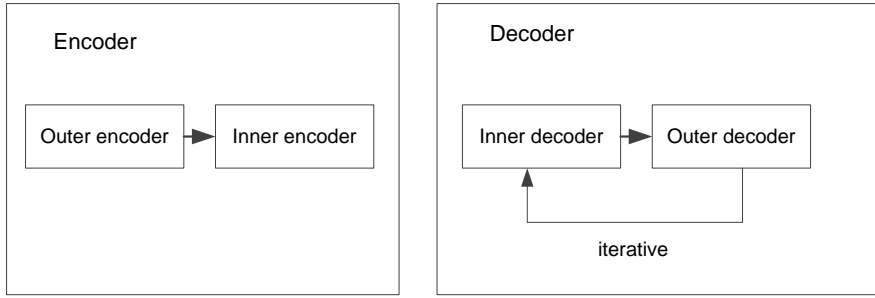


Figure 1.6: Concatenated Code.

dB. A systematic binary LDPC code with a NCG of 8.02 dB at a reference BER of 10^{-15} is also included as a candidate code in ITU-T G.975.1. It is a linear block that has the property of a few 1s in the parity check matrix with the rest a large amount of 0s. It was first introduced by Gallager in his PhD thesis in 1960s [26]. But it did not attract much attention until about fifteen years ago when the implementation of LDPC encoders and decoders becomes reasonably efficient due to the development of manufacturing process.

The third generation FEC usually uses SD method to obtain even higher NCG of over 10 dB. LDPC codes continue to be popular. Variants of LDPC codes are studied to provide NCGs close to the Shannon limit with the help of the decoding methods like sum-product [27], message passing [28] and belief propagation [29]. The variants are also studied to overcome the well-known error floor issue [30].

The proposals on new candidate codes never stop as the standardization of FEC is unclear for the next generation high speed optics-fiber communications. The fast capacity evolvement puts stricter requirements on FEC in no time. There are many other proposals besides the above mentioned ones, among which the FEC codes with a product code structure are what we study in this thesis. Details are in chapter 4.

1.4.3 Adaptive algorithm

The drastically increased transmission speed in optical communications towards 400 Gbps and beyond makes the channel impairments become more and more severe. WDM technique will be the key enabler of the next generation high capacity optic-fiber networks. As discussed before, the reduction of spacing to a smaller grid makes the impair-

ment and noise compensation more challenging. Increased nonlinear loss due to the increased power for increased number of channels will be costly to be compensated for each individual channel. Besides, the properties of all channels are not similar. Different lightwave paths experience different penalties. Furthermore, unpredictable burst errors, for example due to temperature drifting, degrade the system performance and limit the data transmission distance. Therefore, the adaptive FEC scheme would be essential to provide robustness, flexibility and high throughput for the next generation optical networks. By offering a flexible error protection capability, compared to a fixed rate FEC algorithm, an adaptive FEC algorithm usually provides:

- The capability to correct various types of errors;
- Less encoding and decoding delay in less noisy channel;
- Improved performance in noisy channel;
- Higher gain by average;
- Lower power by average.

1.4.4 Hardware implementation

Application specific integrated circuit (ASIC) is an integrated circuit designed for a specific application, not for the general purpose use. It can be any specific application and the running speed is fast and guaranteed. The improved complementary metal-oxide-semiconductor (CMOS) technology, lowered from above 100 nm in 2000 [31] to today's 16 nm FinFET [32], enables ASIC designs with smaller area, reduced power consumption, faster speed and more complicated functionality. Today some building blocks such as micro-processors can be integrated in an ASIC as well. This kind of ASIC is called system on chip (SoC) [33] and provides a strong processing ability to support more sophisticated customer's requirements. Hardware description languages (HDLs) such as very high speed integrated circuit HDL (VHDL) [34], Verilog HDL [35] and systemVerilog [36] are used to describe the in-parallel functionalities.

Field programmable gate arrays (FPGA) is an integrated circuit to be programmed after its manufacturing. It has programmable logic cells and programmable interconnects. The same HDLs are used in functional descriptions for FPGA applications. The compiled netlist can be downloaded into FPGA and verified on the test board. If bugs

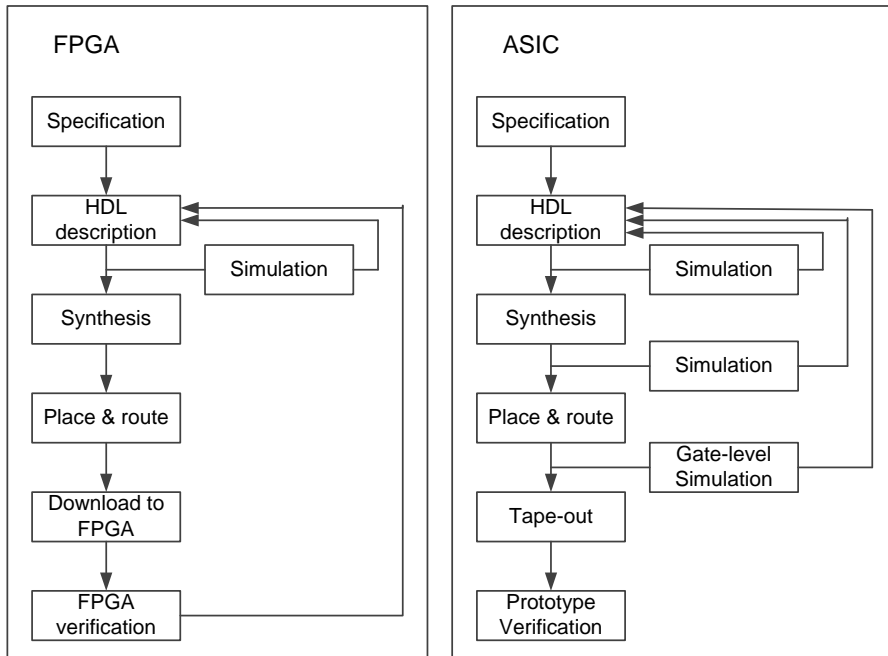


Figure 1.7: Design flows of FPGA and ASIC.

are found in the verification, the modification can be made in the functional description and the compiled netlist can be downloaded again into FPGA. The modifications can be made as many as desired, without a demand for a thorough test of the functional description. ASIC designs, on the contrary, have a strict requirement in covering the functional test as much as possible before it goes to the actual tape-out stage.

The comparison of FPGA and ASIC design flows is shown in Fig. 1.7. Though ASIC and FPGA both use HDLs to describe the functionality from the start, there are some differences between these two techniques:

- FPGA is faster in development - FPGA is a pre-factorized integrated circuit (IC);
- FPGA is more flexible - The changes can be made and verified in FPGA as much as preferred;
- FPGA is reusable - When an application is verified, an FPGA chip can be reused for other application purposes;
- ASIC is more compact - It is user defined specific application;

- Cost is dependent on the application - FPGA is more costly for large production volumes, but cheaper in the case of small amount of productions.

1.4.5 Applications

FEC is intensively considered in various applications. In WDM systems [37] that seem to be the dominant technology for high-capacity spectrum-efficient transmissions, FEC can help in applications such as the integration of low cost elements in next generation data centers [38], the deployment of advanced systems, for example RoF (radio-over-fiber) [39], in metro/access network and the extension of the transmission distance in long haul transmission systems [40, 41, 42, 43].

In recent years FEC limit has been used as a reference in experimental demonstrations to evaluate the system performance. A successful sequence recovery at 10^{-3} or even 10^{-2} would be declared error free, assuming the use of FEC codes. This is not enough as there are many limitations to prevent FEC from performing in the expected way, i.e. as for the AWGN channel. Cycle slip, non-linearity, interference, etc. will all affect the behavior of FEC in an unexpected way. Therefore it is important to have FEC integrated in any given system to illustrate the actual improvements yielded by FEC.

Chapter 2

State of the art

The study of FEC is always a branch in the study of optical communications. To fulfil the ever increasing demand in different application scenarios, the adoption of FEC has to consider many aspects, for example the properties of candidate codes, the complexity of hardware implementation and the simplicity to be plugged into a system. In this chapter we will have an overview of the development of FEC from different perspectives. Section 2.1 is the overview of proposals on candidate codes. Section 2.2 shows the research work carried out for adaptive FEC. Hardware implementation and application scenarios are presented in section 2.3 and section 2.4 respectively.

2.1 Candidate codes

This section is an overview of the three generations of FEC codes with some highlights in Fig. 2.1. The blue solid curve represents for the HD Shannon limit while the red dashed curve represents for the SD Shannon limit. The red circle spots are SD-FEC codes and the blue triangle spots are HD-FEC codes.

The first integration of RS code into a 565 Mb/s optical signal opened a door of using FEC to push margins in different aspects for optical communications [44]. RS code is a non-binary cyclic ECC invented by Irving S. Reed and Gustave Solomon. It is specified in the ITU-T recommendation G.709 how an information sequence is encoded into a RS(255, 239) code on OTN interfaces [25]. With 6.7% overhead, it provides around 6 dB NCG at a reference BER of 10^{-15} . Together

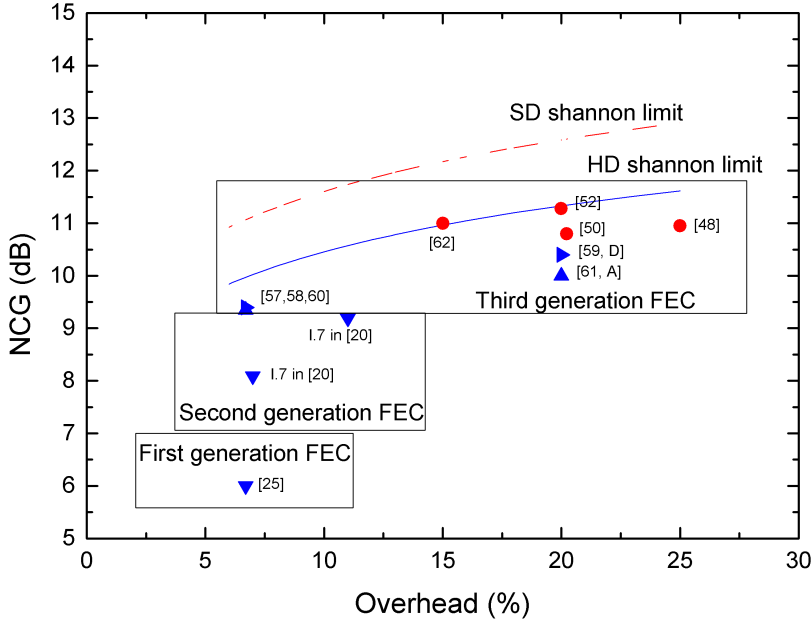


Figure 2.1: Overview of FEC codes.

with other simple linear codes such as Bose-Chaudhuri-Hocquenghem (BCH) code [45], RS code represents the first generation FEC.

LDPC codes started to attract attention for long haul optical communication in 2002 [46]. Simulations show that for a reference BER of 10^{-6} it provides 1.2 dB NCG over RS(255, 239). LDPC codes, together with some concatenated code, are specified in the ITU-T recommendation G.975.1 as candidate FEC codes for high bit-rate DWDM submarine systems [20]. However, these codes can be applied to other high bit-rate optical systems as well. These codes with a varying overhead 6.7% to 25% are called second generation FEC codes, providing NCGs from 8 dB to 10 dB.

Many other codes have been proposed ever since. They are in general called the third generation FEC. The study of the third generation FEC consists of both HD-FEC and SD-FEC. A common property of the third generation FEC codes is to provide higher NCG than the second generation FEC codes provide, usually over 10 dB, at the cost of a higher overhead than 6.7%. There are also some reports on 6.7% overhead HD-FEC codes with NCGs of around 9.4 dB.

Among the various proposals for the third generation FEC codes, LDPC codes have been a very popular candidate due to its strong decoding capability at a relatively high input BER. Besides the binary LDPC codes, the non-binary LDPC codes for optical communication systems are proposed in [47], reporting a coding gain of 9.9 dB at a reference BER of 10^{-10} , based on simulations for a 12.59% overhead LDPC code. Another example of SD-LDPC code is LDPC(24015, 19212) code of rate 0.8 with a NCG of 10.95 dB at a reference BER of 10^{-12} [48]. Long irregular SD-LDPC coded orthogonal frequency division multiplexing (OFDM) is reported in [49]. To overcome the well-known error floor issue, the concatenations of LDPC codes with other codes are studied. The concatenations of SD-LDPC and 7% overhead HD-FEC codes for application in systems beyond 40 Gb/s are presented in [50, 51]. The simulation shows a NCG of 10.8 dB for a code with around 20.5% overhead. A SD-LDPC(18353, 15296) code with a NCG of 11.28 dB at 20% redundancy is mentioned in [52].

Concatenated codes from the concatenation of RS codes and other simple linear codes are still ongoing. A serial block turbo code (BTC) that is a concatenation of RS code and Reed-Muller (RM) code is reported in [53]. The simulation is done for a binary phase shift keying (BPSK) signal over an AWGN channel. The simulation result shows that this code outperforms RS(255, 239) with around 2 dB. Concatenated codes of BCH codes are reported in [54, 55, 56]. They have similar performance compared to the second generation FEC specified in ITU-T G.975.1. But the short length of some codes may be beneficial in the hardware implementation.

Other codes than LDPC codes and concatenated codes are reported as well. A so called Swizzle code is proposed in [57]. This code has a NCG of 9.45 dB at a cost of 6.7% overhead for a reference BER of 10^{-15} . Staircase code is presented in [58, 59]. With 6.7% overhead and 20% overhead, this code can provide NCGs of around 9.4 dB and 10.4 dB. The error floor is way below 10^{-15} . The study of a continuously interleaved BCH (CI-BCH) code is reported by Vitesse [60]. This 6.7% overhead HD-FEC code yields 9.35 dB NCG at the error floor of less than 10^{-15} . The product VSC9804 is a 20% overhead version CI-BCH and its key features state a NCG of more than 10 dB [61]. A SD turbo block code (TBC) with around 15% overhead is demonstrated to be able to provide over 11 dB NCG [62]. We have also proposed FEC codes with 20% overhead that yield NCGs of from 10 to 10.4 dB at a reference BER

of 10^{-15} [A, B, D].

2.2 Adaptive FEC

The study of adaptive FEC is not mature and expands in multiple sub-areas.

In 2005, a SDH based adaptive error correction scheme for WDM networks was proposed [63]. It suggests to take the advantage of multi-channel systems and to use a dedicated channel for the redundancy transmission. This scheme provides a better performance than using fixed codes as in ITU-T G.707 and ITU-T G.709 that limit the correction capability and efficiency for different patterns. The redundant bits of payloads for all other channels are transmitted based on time division multiplexing (TDM) at a fixed rate to enable synchronization at the receiver end.

In 2007, an adaptive FEC method for high speed optical Ethernet was proposed [64]. It points out that high speed optical Ethernet has to consider the problem of physical channel errors. The probability of correctly transporting Ethernet data packets whose lengths are greater than 1280 bytes will be near to 0 when BER of the physical channel is greater than $5 \cdot 10^{-4}$. In the test FEC was considered at packet level and the redundancies from 2 bits to 32 bits were used. Packets under test were from 16 bytes to 1518 bytes. The test results show less than 1% packet loss at the channel BER of 10^{-3} .

In 2009, a rate adaptive LDPC-coded multilevel modulation with coherent detection for high speed optical transmission was presented [65]. It chooses quasi-LDPC code in the adaptive scheme. Each channel is encoded with a configurable quasi-LDPC code based on its channel condition. The simulation shows that at a target BER of 10^{-9} the NCG ranges from 9.16 dB to 10.09 dB.

In 2011, a rate-adaptive coding method for optical fiber transmission systems was presented in [66]. This rate-adaptive transmission scheme for long-haul systems uses a fixed modulation format (PDM-QPSK) at a fixed symbol rate, with the deployment of variable rate HD serially concatenated RS over a wide range. Shortening and puncturing are used for the code rate variation. Simulation results show a transmission distance of 2000 km at 100 Gbit/s with single carrier DP-QPSK modulation and coherent detection.

In 2012, we proposed a rate-adaptive coding scheme using two-layered variable rate FEC for optical fiber transmission systems, also with the fixed signal constellation and symbol rate [C]. The first level uses serially concatenated HD-RS codes to provide a CG of up to 12.25 dB. For lower signal-to-noise ratio (SNR) transmissions, a second layer of coding is employed. By using 3-bit quantization SD extended Hamming(8, 4, 4) code or RM(1, 4) code, the CGs can be extended to 15.75 dB and 18 dB respectively.

In 2013, a study of rate adaptive FEC in optical transport unit (OTU) framing was presented [67]. It proposes to segment OTU4V into tributary slots to realize the variation of parity length without varying the frame length. Combining the conventional attached parity region with the parity transmitted in ODTUs, a NCG improvement of 1.5 dB is expected.

In 2013, an adaptive FEC for energy efficient OTN was reported in [68]. This paper describes from the traffic point of view how an adaptive FEC scheme can help with energy efficient OTNs. It proposes a modification in OTN frame format to confine with variable FEC coding methods in order to reduce the power consumption during periods of low traffic.

The most recently published study on an adaptive FEC scheme is on the spectrum-efficiency of transparent OTN design with variable rate FEC codes [69]. This paper addresses from the network planning standpoint the tradeoff between transmission rate and optical reach. It employs the algorithm described in [66] to illustrate the idea. The case study shows the increase of spectrum efficiency supports total traffic around three times higher than that with mixed line rate.

2.3 Hardware implementation

Thanks to the more advanced CMOS technology, the hardware implementation of FEC has been pushed from a throughput of 3.2 Gb/s to a throughput of 100 Gb/s and is still moving forward. An overview of reported research results can be found in the tables 2.1 to 2.5. The table 2.1 shows two implementations at a low throughput of less than 5 Gb/s, a SD-RS code and a HD-RS code. The implementation for SD-RS with the more advanced CMOS technology shows a reduced voltage supply as well. The table 2.2 shows again one SD-FEC implementation and one HD-FEC implementation. They both have a throughput

Table 2.1: Overview of hardware implementation - part 1

Code	SD-RS [70]	HD-RS [71]
Throughput (Gb/s)	2.56	3.2
Overhead (%)	6.7	6.7
NCG (dB @a reference BER)	-	-
CMOS technology	90 nm	0.18 μ m
Number of gates	45.3 K	21 K
Memory (bits)	-	-
Delay	-	-
Voltage supply	0.98 V	1.8 V
Power consumption	19.6 mW	-

Table 2.2: Overview of hardware implementation - part 2

Code	SD-BTC [72]	HD-RS [73]
Throughput (Gb/s)	12.4	10
Overhead (%)	23.6	6.7
NCG (dB @a reference BER)	10.1 @ 10^{-13}	5.5 @ 10^{-12}
CMOS technology	0.13 μ m	0.16 μ m
Number of gates	16 M	1.8 M
Memory (bits)	4 M	-
Delay	-	5.73 μ s
Voltage supply	-	-
Power consumption	-	343 mW

around 10 Gb/s. With a higher overhead and a more complicated decoding algorithm, the SD-FEC provides almost a double NCG than the HD-FEC can. The tables 2.3 and 2.4 are examples of hardware implementations of the second generation FEC codes, while the table 2.5 includes two implementations of the third generation FEC codes that provide higher NCGs compared to the second generation FEC. It is pointed out in [73] that the power consumption of the decoder core is a small part of the power consumption of an entire chip. Two thirds of the power consumption of an entire chip is due to I/O power. Therefore the power consumption for the second implementation in the table 2.5 is suspected to be the chip power consumption while the other mentioned power consumption values are for the decoder cores.

Besides the listed ASIC decoders, some interesting FPGA implementations are listed below. A 10 Gb/s orthogonally concatenated BCH

Table 2.3: Overview of hardware implementation - part 3

Code	HD-RS [73]	HD-RS [74]
Throughput (Gb/s)	40	115
Overhead (%)	6.7	6.7
NCG (dB @a reference BER)	5.5 @ 10^{-12}	-
CMOS technology	0.16 μm	0.13 μm
Number of gates	400 K	378 K
Memory (bits)	-	-
Delay	1.5 μs	800 ns
Voltage supply	-	1.2 V
Power consumption	361 mW	-

Table 2.4: Overview of hardware implementation - part 4

Code	Concatenated BCH [56]	Concatenated BCH [75]
Throughput (Gb/s)	102.4	110.1
Overhead (%)	6.7	6.7
NCG (dB @a reference BER)	7.98 @ 10^{-12}	9.19 @ 10^{-15}
CMOS technology	90 nm	90 nm
Number of gates	1.4 M	3.732 M
Memory (bits)	-	4.114 M
Delay	13.8 μs	38 μs
Voltage supply	1.1 V	1.1 V
Power consumption	-	-

Table 2.5: Overview of hardware implementation - part 5

Code	i-BCH [76]	SD-TPC [62]
Throughput (Gb/s)	110.1	100
Overhead (%)	6.7	15
NCG (dB @a reference BER)	9.34 @ 10^{-15}	11 @ 10^{-15}
CMOS technology	90 nm	40 nm
Number of gates	3.087 M	640 K flip-flops 6.3 M combinatorial gates
Memory (bits)	5.705 M	9 M
Delay	66 μs	
Voltage supply	-	-
Power consumption	-	7 W (chip)

encoder is presented in [77]. The design was realized in FPGA and the simulations show a data rate of 10 Gb/s with clock frequency of 156 Hz. To eliminate the well-known LDPC error floor issue, the design of a LDPC code and its hardware architecture are jointly investigated [78]. With an FPGA-based study of the dominant error events, the parity check matrix is optimized to lower the error floor to 10^{-13} . A SD-LDPC code of 24576 bits with 20% overhead was implemented in an FPGA chip. The NCG is 10.7 dB at a reference BER of 10^{-13} . Another try on an FPGA chip is a triple-concatenated SD-FEC using LDPC(4608, 4080) [79]. This 20.5% overhead code was implemented in a FPGA chip with a clock frequency of 556 KHz and a throughput of 100 Gb/s. A NCG of 10.8 dB is expected at a post-FEC BER of 10^{-15} with the concatenation of a second generation code.

Besides, a real time 120 Gb/s coherent PDM-QPSK transceiver implemented as a 40 nm CMOS ASIC is reported in [80, 81]. It contains 63 GSamples/s ADCs, DSP and SD-FEC. The chosen turbo product code (TPC) yields a NCG of 11.1 dB at a post-FEC BER of 10^{-15} . The test of ASIC design was carried out in a WDM environment with multi-path interference considered.

Table 2.6 includes some highlights of the hardware implementations from the industry. 100G FEC product releases include VSC9804 [61] and Viasat ECC66100 series [82], HD-FEC and SD-FEC respectively. VSC9804 is a 20% overhead HD CI-BCH code with a NCG of over 10 dB. The ECC66100 series consists of SD-TPC with an overhead of 15% or 20% and NCGs of 11 and 11.3 dB, respectively. Viasat also releases the ECC66200 series for 200G applications [83], based on 7% and 20% overhead SD-TPC codes with NCGs of 10.2 and 11.3 dB respectively. Without revealing details, Huawei [84] and ZTE [85] have announced their in-house self-developed FEC algorithms for 100G or higher bit rate optical transmissions. Huawei's block interleaved convolutional code (BICC) is an LDPC-based SD-FEC scheme. With 20% or larger overhead, it provides over 11.5 dB NCG. The FPGA demonstration is reported in [86]. Huawei points out that this SD-FEC, together with spectrum compression at the transmitter, reduces the transmission penalty caused by rate increases at the transmitter and ensures the desired CG for high overhead SD-FEC. ZTE's 100G SD-TPC has 15% overhead and allows an input BER threshold of between $1.8 \cdot 10^{-2}$ and $2 \cdot 10^{-2}$ that translates to around 11 dB NCG. ZTE declares that this SD-FEC scheme with 15% overhead offers higher transmis-

Table 2.6: 100 Gb/s FEC highlights from the industry

Code	Company	Throughput (Gb/s)	Overhead (%)	NCG (dB)
CI-BCH	Vitesse	100	20	>10
SD-TPC	Viasat	100	15	11
SD-TPC	Viasat	100	20	11.3
SD-TPC	Viasat	200	7	10.2
SD-TPC	Viasat	200	20	11.3
BICC	Huawei	100	20	>11.5
TPC	ZTE	100	15	~ 11

sion efficiency and better wave filtering performance than a 20% overhead FEC scheme. Other companies, for example Altera [88], also have proposals for 100G FEC solutions.

Reduced circuit complexity is a very important issue for 100 Gb/s and above FEC implementation. Viasat's ECC6100 series in 40 nm CMOS technology has more than 20 M equivalent gates. Coriant points out in [87] that close to half of the power dissipation of a 100 Gb/s DSP-ASIC digital logic core in a line card application is from SD-FEC. Therefore, the more mature and cheaper CMOS process is essential to simplify the implementation and reduce the cost in future.

2.4 FEC application

FEC can compensate all kinds of impairments, but the achievable improvements vary from one application to another as the error distributions are different. This section lists some applications with novelties.

A study of using 160-km repeater spans and advanced FEC is reported in [89]. It is attractive to use long repeater spans as it can substantially save capital and operational expenditure. The novelty of this paper includes the use of a span longer than 150 km and a transmission link of 480 km over three 160-km spans as well as the integration of FEC. The experiment was done in a 160 Gb/s RZ-DPSK data transmission link excluding the FEC overhead. The analysis shows the promise of a transmission over 1000 km at 160 Gb/s with a repeater spacing of 160 km.

Employing concatenated FEC to mitigate polarization-sensitivity in all-optical wavelength conversion is reported in [90]. All-optical wavelength-conversion can be efficiently performed by means of semi-

conductor optical amplifier (SOA) with the shortcoming of being sensitive to the relative polarization of optical signals. A FEC mechanism was introduced and demonstrated in a 10 Gb/s lightwave channel that the conversion may be made insensitive to random fluctuations of the polarization. No error was observed after FEC decoding without the control of the polarization before the converter.

A FEC aided demonstration of silicon based wavelength conversion is reported in [91]. The experiment consisted of two cascaded nonlinear optical signal processes, i.e. 160 Gbit/s all optical wavelength conversion based on cross-phase modulation (XPM) in a silicon nanowire and subsequent 160 Gbit/s-to-10 Gbit/s de-multiplexing using a highly nonlinear fiber (HNLF). With the integration of 6.6% overhead FEC, the transmitted sequence was recovered without observing any error.

A paper on the impact of error control with FEC on energy-efficient reliable data transfers over optical networks is presented in [92]. In this paper, two schemes are studied for energy efficient reliable delivery of large files (hundreds of GBs) over core optical networks: automatic repeat request (ARQ), and hybrid ARQ that combines ARQ with FEC. A new model is proposed in hybrid ARQ to estimate the energy consumption for performing encoding and decoding operations by incorporating different block sizes and FEC error correcting capability. The analysis shows that when the pre-FEC channel BER is in excess of 10^{-5} , hybrid ARQ offers better performance than ARQ in terms of energy efficiency. When BER is lower than 10^{-5} , hybrid ARQ behaves similarly to ARQ. Therefore hybrid ARQ seems to fit better in the design of energy efficient network in future.

A study of ECC for pulse amplitude modulation (PAM) signals in data center applications can be found in [93]. This paper experimentally demonstrates PAM modulation with FEC integration for a 25 Gb/s per channel data center, which is a cheaper solution than using QAM modulation format or polarization multiplexing as explained in [94]. The demonstration was done in a transmission distance of over 500 m as specified in [95] and some selected FEC codes failed to provide the minimum CG requirement [96] of 5.8 dB at a BER of 10^{-15} while others succeeded.

A field trial of 112 Gb/s dual-carrier differential quaternary phase-shift keying (DQPSK) channel upgrade in an installed 516-km fiber link and reconfigurable optical add-drop multiplexer (ROADM) is reported in [97]. This demonstration for 100 Gb/s metro area network

requires neither high-end ADC/DSP nor fast optical polarization tracking. No error was observed in the transmission of a 100GE signal over 106 hours with OTU4 framer and FEC.

SD-FEC in a non-AWGN channel is studied in [98]. A conditionally bivariate Gaussian noise model (CBGN) is used to analyze the impact of correlations among the signal's two quadrature components and LDPC codes are evaluated in this channel. It shows that the shape of the noise clouds significantly affects the detection performance for SD decoding. Conventional DSP algorithms may unintentionally shape the noise clouds into AWGN-like clouds, which destroy useful information for SD-FEC.

The hybrid SD/HD FEC scheme under extreme XPM conditions is evaluated in [99]. If TPC code is used and there is no interleaving, the presence of NLs alters the input-output BER relationship. When TPC is replaced by a long LDPC code, input-output BER relationship remains essentially unaffected due to the deeper interleaving innate in the long LDPC code. By interleaving 4 TPC codewords, it also shows the unaffected input-output BER relationship. Interleaving FEC codes helps PMD mitigation as well [100]. With polarization scramblers (PSs), the interleaving LDPC codes are tolerant to a large PMD.

A study of SD faster than Nyquist (FTN) technologies in PDM-QPSK transmission is shown in [101]. FTN signaling can transmit up to twice the bits as ordinary modulation at the same bit energy, spectrum, and error rate. The method is directly applicable to OFDM and QAM signaling [102]. In a 20-channel 224 Gbps (56Gbaud) PDM-QPSK experiment in 50 GHz grid over 3040-km G.652 fiber and EDFA-only link, with 7% overhead SD-FEC, 4 bit/s/Hz net spectral efficiency was achieved. It indicates that SD-FTN algorithm enables 400G long haul transmissions.

In the next generation network solutions, the selection of FEC codes has to jointly consider many factors to balance the tradeoff among performance, energy efficiency and FEC overhead [103, 104, 105].

Chapter 3

Description of papers

This thesis is based on a number of articles already published or submitted to peer-reviewed journals and conference proceedings. This chapter states the main contribution of the thesis, including the description of the novelty, the individual author contribution and comment to the papers.

The included papers are categorized into four aspects, the same as in chapter 2. The papers [A, B] present the results of proposed code algorithms in section 3.1. The paper [C] presents the result on adaptive FEC in section 3.2. In section 3.3 the paper [D] presents a code proposal together with its implementation for 400 Gb/s optical transmissions. In the final section 3.4 the experimental results are presented in the papers [E, F].

3.1 Product code

Paper [A]: Over 10 dB Net Coding Gain Based on 20% Overhead Hard Decision Forward Error Correction in 100G Optical Communication Systems

This paper, presented at *37th European Conference on Optical Communication (ECOC 2011)*, proposes a new encoding and decoding FEC algorithm for 100 Gb/s optical communications. As the research for optical communications moved from 40 Gbps to 100 Gbps based on DP-QPSK modulation and coherent detection, the increased optical signal-to-noise ratio (OSNR) requirement has pushed the study of FEC to evolve from the second generation to the third generation for a NCG

of 10 dB or even higher. The overhead requirement is relaxed in the meanwhile, based on the suggestion from OIF [24]. The proposed code in this paper is one of the first several reported research achievements on 20% overhead FEC with over 10 dB NCG. The error floor turns out to meet today's requirement of 10^{-15} . The hardware implementation is also investigated in the paper and it shows the possibility for an implementation in several state-of-the-art FPGA chips.

Comment: In section 2 where the code construction is explained, the length of leading zeroes is 980, which is a typo. The correct length should be 1656.

The individual author contribution: contributed to the introduction and motivation of the paper; performed the simulation and analysis of the proposed code; prepared and revised the manuscript.

Paper [B]: Application of Beyond Bound Decoding for High Speed Optical Communications

This paper, presented at *Asia Communications and Photonics Conference 2013 (ACP 2013)*, proposes a new decoding FEC algorithm for 100 Gb/s optical communications. In the paper [A], the proposed code takes the advantage of reduced decoding error probability. This paper studies how to improve the decoding capability further, having this advantage considered. The component code in [A] can correct up to 3 errors and detect 4 errors based on minimum distance decoding (MDD) method. In this paper, the decoding of 4 errors is studied theoretically. It shows that there is a high decoding success probability when there are 4 errors. Notice that no decoding error exists if a component has 4 errors in it. When there are more than 4 errors in a component, the decoding error probability is small. The method can be applied to any code with BCH components or similar, not limited to a product code structure.

Comment: The hardware implementation is investigated in the paper. In the later implementation work we carried out, it turned out that the estimated implementation was not practical due to the high fan-out. A realistic implementation can be found in [D].

The individual author contribution: contributed to the introduction

and motivation of the paper; performed the simulation and analysis of the proposed algorithm; suggested the hardware implementation, prepared and revised the manuscript.

3.2 Adaptive FEC

Paper [C]: Adaptive Forward Error Correction in High Speed Optical Communications

This paper, presented at *3rd World Conference on Information Technology 2012*, proposes an adaptive FEC coding scheme with a two-layered coding step to tackle the issue of incoherent transmission scenarios. The first layer uses HD concatenated RS codes to provide a CG of up to 12.25 dB. For lower SNR transmissions, a second coding layer is added. A 3-bit SD extended Hamming(8, 4, 4) code or RM(1, 4) code are considered, which extend the CGs up to 15.75 and 18 dB, respectively. The paper is one of the few research publications on adaptive FEC algorithms.

The individual author contribution: contributed to the introduction and motivation of the paper; supervised the master thesis on this topic of which this paper was part of the outcome, reviewed the manuscript.

3.3 Hardware implementation

Paper [D]: Forward Error Correction for 400 Gbps High Speed Optical Fiber Links

This paper, submitted to *IEEE Communications Letters*, proposes a product code with 5-error-correcting and 6-error-detecting components for next generation high speed optical communications. This code provides a NCG of 10.4 dB at a reference BER of 10^{-15} . Yet the error floor is extremely low and the code can help with a smooth system upgrade when the BER of 10^{-15} is not good enough in future. Besides, the proof-of-concept implementation was done. A reconfigurable hardware implementation scheme is presented to support 100 Gb/s or 400 Gb/s transmissions flexibly.

The individual author contribution: contributed to the introduction

and motivation of the paper; performed the simulation and analysis of the proposed algorithm; performed the hardware implementation, prepared the manuscript.

3.4 FEC application

Paper [E]: High-Speed 1550 nm VCSEL Data Transmission Link Employing 25 GBd 4-PAM Modulation and Hard Decision Forward Error Correction

This paper, published in *Journal of Lightwave Technology*, presents the application of FEC in a short range optical transmission over 100 m driven by the direct modulation with a VCSEL. High-speed 4-level PAM (4PAM) at 25 GBaud is presented in the paper to investigate on the ultimate transmission capabilities of laser sources. Line rate of 100 Gb/s was achieved by emulating polarization multiplexing using the 50 Gb/s signal obtained from a single VCSEL. This experiment demonstrates the possibility of achieving high speed short range transmission with low-cost elements and integrated FEC.

The individual author contribution: contributed to the introduction and motivation of the paper; performed the simulation of the proposed algorithm; performed the FEC encoding and decoding in the experiment, performed the analysis of experimental results, prepared and revised the manuscript on FEC.

Paper [F]: Experimental Performance of FEC for Linear and Nonlinear Optical Fiber Transmissions

This paper, submitted to *Photonics Technology Letters*, experimentally demonstrated the FEC application in a 7-channel WDM transmission at 50 GHz spacing. The data in the middle channel was modulated by a DP-16QAM modulator and transmitted at 11.1 GBaud. After the transmission of 741 km, the received data was captured by digital sampling oscilloscope (DSO) and processed afterwards by off-line DSP blocks. The demodulated data was fed into a HD-FEC decoder to get the errors cleaned. The result shows unmatched curves from simulation results and experimental results, which shows the channel under transmis-

sion was not AWGN channel. Therefore, FEC study has to be combined with the channel study to get a better performance.

The individual author contribution: contributed to the introduction and motivation of the paper; performed the simulation and analysis of the proposed algorithm; performed the FEC encoding and decoding in the experiment, performed the analysis of the experimental results, prepared the manuscript.

Chapter 4

Product codes and their decoding

This chapter is a summary of using FEC codes with a product code structure in 100 Gb/s optical communication systems. Section 4.1 goes through the properties of such FEC codes. Section 4.2 presents the latest research results that will be submitted to a peer-reviewed journal after the internal review.

4.1 Basics of product codes

4.1.1 Code construction

A product code can be structured in a matrix as shown in Fig. 4.1. In the matrix, each row or column is also an ECC, called a component code. The length of each dimension can be different, for example n_1 and n_2 as in 4.1. Corresponding information lengths in a component code are k_1 and k_2 . With this structure, the total length of a codeword is $n_1 \cdot n_2$. And the total information length is $k_1 \cdot k_2$. Therefore, the code rate is:

$$R = \frac{k_1 \cdot k_2}{n_1 \cdot n_2} = \frac{k_1}{n_1} \cdot \frac{k_2}{n_2}. \quad (4.1)$$

And the overhead is expressed as:

$$oh = \frac{n_1 \cdot n_2 - k_1 \cdot k_2}{k_1 \cdot k_2} = \frac{1}{R} - 1. \quad (4.2)$$

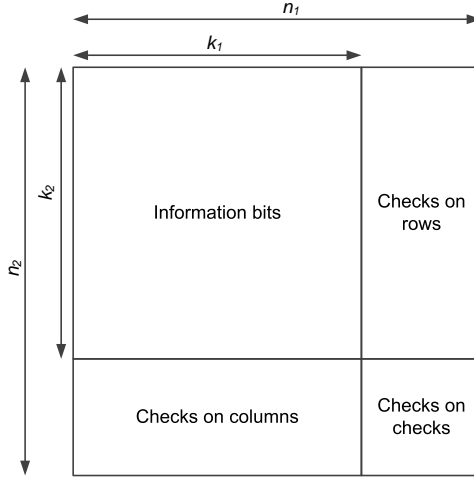


Figure 4.1: A product code structure.

The FEC codes under study in this thesis have $n_1 = n_2 = n$ and $k_1 = k_2 = k$. The code rate and overhead become:

$$R = \left(\frac{k}{n}\right)^2 \quad (4.3)$$

and

$$oh = \left(\frac{n}{k}\right)^2 - 1 = \frac{1}{R} - 1 \quad (4.4)$$

4.1.2 Iterative decoding and error floor

Iterative decoding is a commonly used method for a product code as shown in Fig. 4.2. Components are usually linear block codes and decoded by linear block code decoders. A product code is decoded row-wise followed by column-wise and so forth until a satisfactory BER is obtained or an error floor is reached. Due to the matrix structure, the code is suitable for iterative decoding as there is not much expense in codeword interleaving block when switching decoding between row components and column components.

With iterative decoding, there exists an error floor for a product code. It is a bound that the BER will not be improved much despite the number of iterations. Fig. 4.3 is the simplest error pattern that fails the decoding of a product code by iterative decoding. The example in

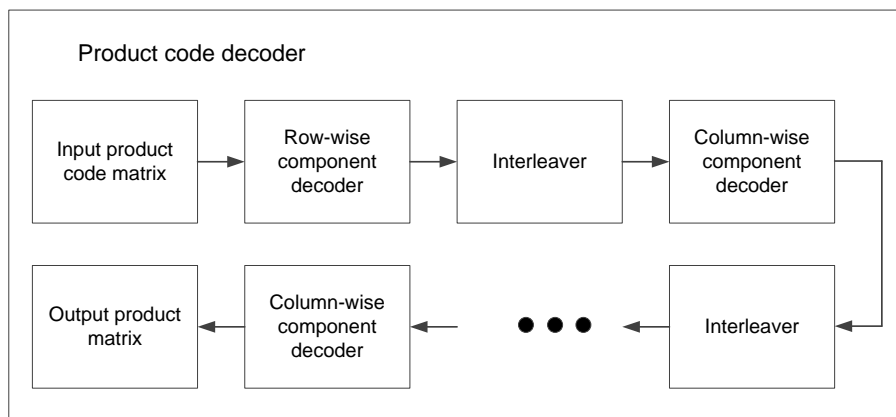


Figure 4.2: Iterative decoding of product code.

the figure is a product code with 3-error-correcting, 4-error-detecting components in both dimensions.

The black spots in the figure stand for error bits. If there exists such a pattern that all components with non-zero syndromes have at least four error bits in each, the iterative decoding will not be able to correct any error bits due to the fact of more than 3 errors in a component. The error floor of a product code with iterative decoding can be expressed

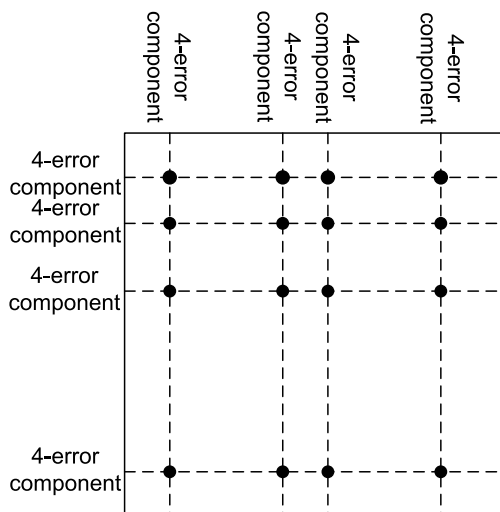


Figure 4.3: Error pattern.

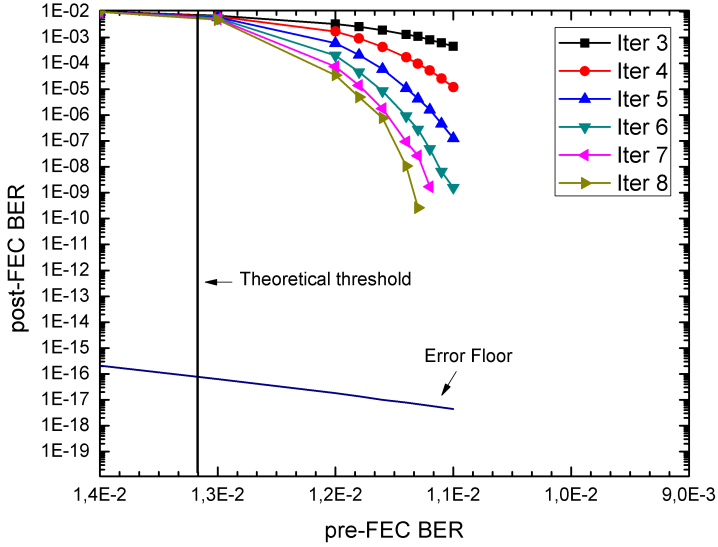


Figure 4.4: Performance of a product code with iterative decoding

as below:

$$BER = \binom{n}{t+1}^2 \cdot p^{(t+1)^2} \cdot \frac{(t+1)^2}{n^2} \quad (4.5)$$

where p is the input pre-FEC BER.

The error floor will limit the usage of a FEC code in its application. FEC codes with high error floor will not be suitable for high speed optical communications. A reference BER of 10^{-15} is currently used as the desired BER after a FEC decoder. If a FEC code shows an excellent behavior at a post-FEC BER of 10^{-7} , but its decoding has an error floor around 10^{-8} , this code with the applied decoding method will not be very useful.

4.1.3 Code performance

Fig. 4.4 shows how the performance is improved by iterative decoding. This figure re-plots the simulation result in the original paper [A]. The parameters are $n = 391$ and $t = 3$. It shows the simulation results after 3 to 8 iterations. The curve drops more quickly and yields more gain when the number of iterations increases. However, the pre-FEC BER is bounded by a theoretical threshold [106], based on the theory of the

sudden emergence of k -core in a random graph [107]. The threshold total number of errors is nc_{t+1} , where

$$c_k = \min\left[\frac{\lambda}{\pi_k(\lambda)}\right], \lambda > 0, \pi_k(\lambda) = P[\text{Poisson}(\lambda) \geq k - 1]. \quad (4.6)$$

In the example we have $t = 3$. So the threshold total number of errors is nc_4 , where c_4 can be obtained from the equation 4.6 by using $k = 4$. The threshold BER then becomes:

$$BER_{threshold} = \frac{nc_{t+1}}{n^2} = \frac{nc_4}{n^2} = 1.3 \cdot 10^{-2}. \quad (4.7)$$

In the meanwhile, the post-FEC BER is bounded by the error floor. Fig. 4.4 shows the theoretical error floor based on the equation 4.5, which is below 10^{-15} .

4.2 Latest achievements

This section presents the latest achievements on single chip FPGA implementation and FEC performance in a metropolitan WDM transmission link with different spacing grids.

4.2.1 Single chip FPGA implementation

Candidate Code

To provide energy efficient FEC, we propose the use of a product code with BCH(255, 230) components in 100 Gb/s optical communication links. The short length of 65025 bits is beneficial for a low complexity implementation while the FEC performance remains as one of the strongest codes. Fig. 4.5 shows the simulation performance. This component corrects up to 3 errors and detects 4 errors. The decoding results of 4 to 6 iterations are plotted in the BER curves. It shows that after five iterations, the curve drops drastically. The pre-FEC BER is around $1.45 \cdot 10^{-2}$ and it translates to a NCG of 10.3 dB with an overhead of 23 %. Based on the formula 4.5, for the pre-FEC BER of $1.45 \cdot 10^{-2}$ and below, there is no error floor issue to reach the post-FEC BER of 10^{-15} .

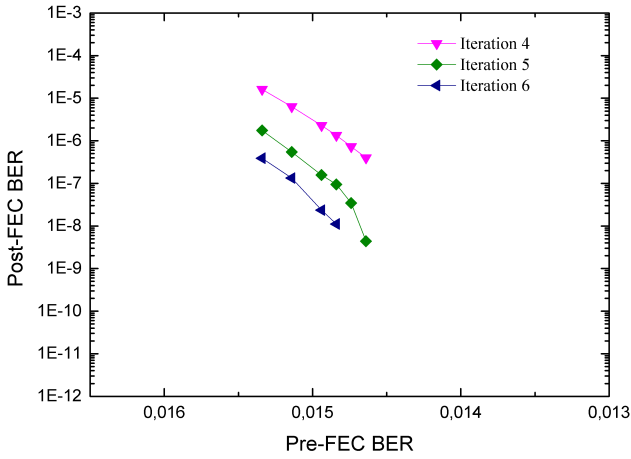


Figure 4.5: Simulation results of a product code with BCH(255, 230) components.

Matrix slicing and slicer decoder

The implementation method is similar to what is presented in [D], with slight modifications. In each iterative decoding, the product code matrix is split into multiple identical blocks. The left part in Fig. 4.6 shows an example of 9 blocks, $B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8$ and B_9 . All row-wise components are split into three slices, S_1, S_2 and S_3 , with blocks B_1, B_2, B_3 in S_1, B_4, B_5, B_6 in S_2 and B_7, B_8, B_9 in S_3 , respectively. The column-wise components are split into three identical slices in a simi-

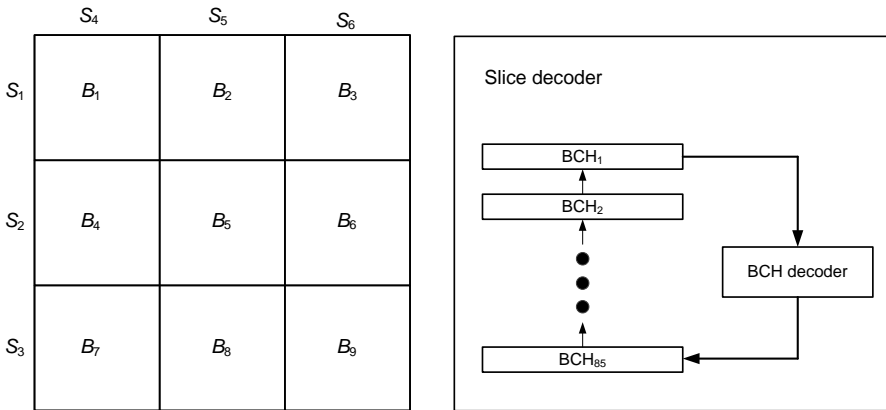


Figure 4.6: Slicing structure and slice decoder.

lar way. The slice S_4 consists of the blocks B_1, B_4, B_7 while the slices S_5 and S_6 contain the blocks B_2, B_5, B_8 and B_3, B_6, B_9 , respectively.

The decoding block for a slice is shown in the right part in Fig. 4.6. Each slice has 85 BCH components. In decoding, the component BCH_1 is fed into the BCH decoder and all other components are shifted one component towards the component BCH_1 . The decoded BCH codeword is returned to the component BCH_{85} . In this way, all 85 components can be decoded within 85 clock cycles plus the delay of the BCH decoder.

Estimation of FPGA resources

We first estimate the required resources for one iterative decoding. It consists of three steps. The first step is to decode all three row-wise slices in parallel. Suppose the BCH decoder delay is 35 clock cycles. So the row-wise decoding can be done in 120 clock cycles. Then the column-wise decoding is done in the same way. Finally the product code matrix is updated for the next iteration within a couple of clock cycles. Therefore one iterative decoding can be done in around 250 clock cycles. This is fast enough for data processing on a 100 Gb/s interface, considering a 400 MHz system clock.

Table 4.1 shows the cost of FPGA resources for different modules. The cost of a BCH decoder is borrowed from [D], where the BCH decoder corrects up to five errors. In this proposed structure the cost of a BCH decoder is expected to be less as it is less complicated to correct up to three errors. One data matrix has 65025 FFs that is the size of the code. One iterative decoding requires three BCH decoders and one matrix storage. The three BCH decoders are first used to carry out three

Table 4.1: Estimation of FPGA resources

Block	ALUTs	Memory ALUTs	Registers	Block memory bits
One BCH decoder	~ 30 K	~ 2 K	~ 50 K	~ 2 M
One data matrix	~ 0	~ 0	~ 65 K	~ 0
Three BCH decoders	~ 90 K	~ 6 K	~ 150 K	~ 6 M
One iterative decoding	~ 90 K	~ 6 K	~ 215 K	~ 6 M
Iterative decoding of 5 iterations	~ 450 K	~ 30 K	~ 1075 K	~ 30 M

in-parallel decoding for row-wise slices, and then used for column-wise slices. We consider five iterations to make a balance between the hardware complexity and the performance. The total cost shown in table 4.1 seems to be promising to fit into a single Altera Stratix-V FPGA chip. The final synthesis result will be presented by the time of the PhD defense.

4.2.2 FEC performance affected by channel wavelength spacing in WDM systems

Candidate code

WDM is an attractive solution in future to enable higher capacity with a smaller spacing grid than today's typically used 50 GHz. In this section, we report an experiment on FEC transmissions over 50 GHz and 25 GHz spaced WDM fiber-optic links to observe the FEC performance. Here we use a product code with BCH(511, 465) components. Each component code corrects up to 5 errors and detects 6 errors. In the simulation, shown in Fig. 4.7 the pre-FEC BRE is around $1.45 \cdot 10^{-2}$ after 8 iterations.

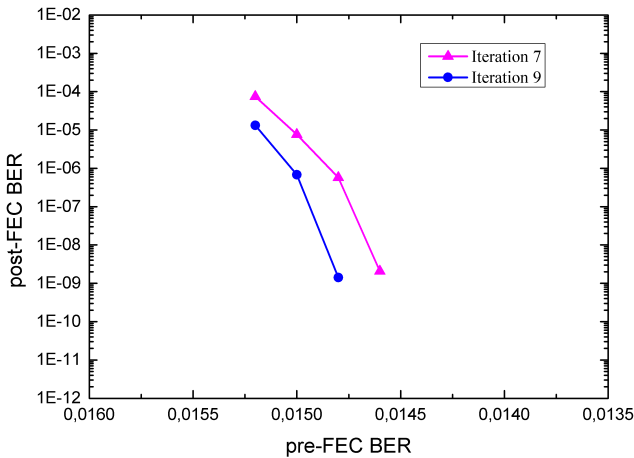
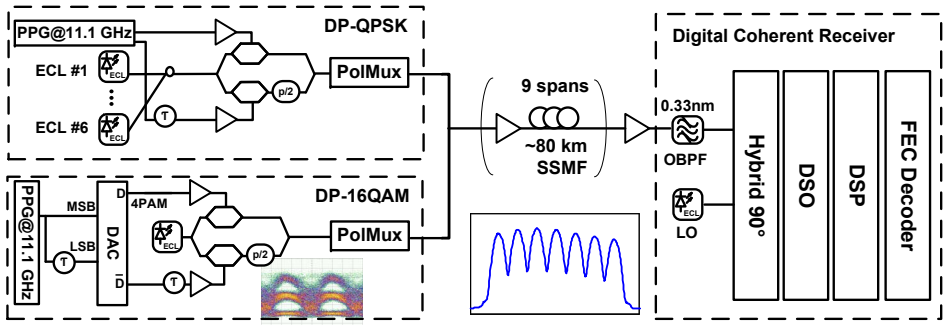


Figure 4.7: Simulation results of a product code with BCH(511, 465) components.

Experimental setup

The system setup in Fig. 4.8 is the same as we present in [F]. The transmitter consisted of 7 WDM channels. The optical channel under test was a DP 16QAM signal at 11.1 Gbaud. The neighboring channels (three on both sides) were 11.1 Gbaud DP QPSK signals, with optical bandwidths similar to the 16QAM channel. A pre-encoded FEC pattern was loaded into a pulse pattern generator (PPG). The 11.1 Gbaud data output from the PPG and its delayed copy were used as inputs to a 4-bit digital-to-analog converter (DAC) to generate two 4-level PAM (4PAM) signals. The 4PAM signals were amplified and supplied to an optical I/Q modulator, along with an optical continuous wave signal originating from an external cavity laser (ECL) with 100 kHz linewidth, creating a 44.4 Gbit/s optical 16QAM signal. PDM was emulated by multiplexing the 16QAM signal with its delayed copy in the orthogonal polarization to obtain a channel with a total bit rate of 88.8 Gbit/s. Fiber transmission was realized over 7 spans of a standard single-mode fiber (SSMF), with each span being approximately 80 km, over a total length of 741 km. The transmission link had no optical dispersion compensation and used EDFAs for span loss compensation. The input power to each span was varied in the range between -5.5 dBm and 3.5 dBm per channel and peak power of all channels was equalized before transmission. A pre-encoded product code was transmitted in



PPG : Pulse pattern generator; MSB : Most significant bit; LSB : Least significant bit; ECL : external cavity laser; 4PAM : 4-level pulse amplitude modulation; PolMux : Polarization Multiplexing; DP-QPSK : Dual-polarization quaternary phase shift keying; DAC : Digital to analog converter that outputs a 4PAM signal and its inverted signal; DP-16QAM : Dual-polarization 16-ary quadrature amplitude modulation; SSMF: Standard single mode fiber; OBPf : Optical band pass filter; LO : Local oscillator; DSO : Digital sampling oscilloscope; DSP : Digital signal processing; FEC : Forward error correction.

Figure 4.8: Experimental WDM setups.

the optical channel column-wise by loading used-defined patterns in PPG. A total of 110,454,183 bits was tested for each channel. At the receiver side, a standard coherent detection scheme was employed. An ECL with a line-width of 100 kHz was used as a LO. Received analog signals were sampled by a DSO with 13 GHz analog bandwidth at a rate of 40 GSamples/s. Acquired traces were processed off-line. DSP included a digital pre-filtering, dispersion compensation, polarization de-multiplexing, carrier phase recovery and digital demodulation. HD data were subsequently decoded by the FEC decoder afterwards.

Analysis of experimental results

Fig. 4.9 includes the experimental results for both 50 GHz and 25 GHz spaced transmissions. The blue curves with solid symbols are the results from the 50 GHz spaced WDM transmission while the red curves with hollow symbols are those from the 25 GHz spaced WDM transmission. The curves with square, triangle, circle and star symbols represent the BER results of pre-FEC analysis, one iterative decoding, iterative decoding after two iterations and iterative decoding after three iterations, respectively. We observe from the curves that:

- The best pre-FEC BERs are obtained in both cases at the power per channel of around -0.5 dBm;
- The pre-FEC BER in the 25 GHz spaced transmission is higher than the corresponding one in the 50 GHz spaced transmission;
- After one iterative decoding no error was observed for the case of the 50 GHz spaced transmission at the power per channel in the range from -3.5 dBm to 1.5 dBm, but in the case of 25 GHz spaced transmission errors were still observed;
- The pre-FEC BER curve in the 25 GHz spaced transmission is flatter than the one in the 50 GHz spaced transmission;
- The working range of input power per channel is narrower in the case of the 25 GHz spaced transmission.

This experiment demonstrates that the channel becomes noisier when the spacing grid is reduced in WDM systems. We notice that when the WDM spacing is reduced from 50 GHz to 25 GHz, the pre-FEC BER curve becomes flatter. The two pre-FEC BER curves have different slopes and the pre-FEC distance, shown in the figure, reaches the maximum value at the optimal input power per channel (-0.5 dBm).

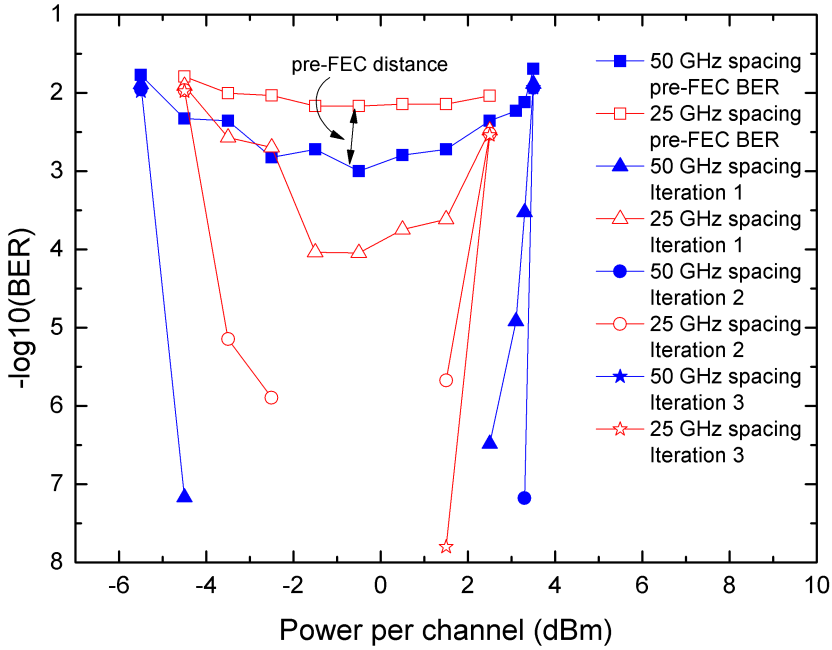


Figure 4.9: Experimental results.

This indicates that the design of FEC has to be updated when the WDM system is updated into a denser grid. The optimized FEC code in a 50 GHz spaced WDM systems will very likely not work for a 25 GHz spaced WDM system.

Chapter 5

Summary

5.1 Conclusions

FEC has been a key technology in enabling the capacity upgrade from 10 Gb/s to 40 Gb/s and 100 Gb/s, due to the explosion of real time application such as online gaming, IP telephony, cloud based application and so on. It will still provide strong support in the next generation optical communications towards 400 Gb/s and beyond. Its capability to compensate various impairments helps to obtain a satisfactory system performance at a BER of 10^{-15} , which is today's general requirement. It can, among many applications, extend the transmission distance, reduce OSNR as well as compensate various losses. It is also beneficial in network planning. Adaptive FEC algorithms can help in network design to balance the traffic load, to strengthen the resilience as well as to provide flexibility. However, the hardware implementation in the meanwhile remains as a big challenge. The FEC aided reliable transmission reduces packet error rate with the trade of a reduced net bit rate as well as the implementation cost of the FEC encoder and decoder. Low cost high performance FEC will always be an attractive research topic. The scientific results and achievements presented in this thesis have extended and contributed to the state of the art.

5.1.1 Product code systems

An overview of the state-of-the-art FEC code algorithms is shown in section 2.1. Among all the codes, the well-known first generation code RS(255, 239) is standardized in ITU-T G.907 to be integrated in OTN.

Though a lot of research work has been carried out on different codes afterwards, the standardization of FECs for 100 Gb/s has remained as a white paper [24]. We propose in [A] the use of a product code with shortened BCH components for 100 Gb/s optical communications. This code is one of the first several codes that provide over 10 dB NCG and less than 10^{-15} error floor based on 20% overhead HD decoding method. The HD algorithm retains the possible simplicity in decoding. Additionally, in [B] the employment of a BBD method is proposed to further enhance a code's decoding capability without changing its encoding structure. In [D], we study a product code with a 5-error-correcting, 6-error-detecting component. The study of the code shows as usual a very high NCG. The essential of this code is the extremely low error floor that will fulfill the requirement in future when 10^{-15} is not good enough [108].

5.1.2 Adaptive algorithm

The paper [C] studies an adaptive algorithm with a concatenated code structure. This code can flexibly provide a very high NCG in noisy circumstances with the cost of reduced code rate. The study of adaptive FEC codes at a network level is not mature, but it can be foreseen that the integration of adaptive FEC algorithms will open a door to more efficient, more robust and more flexible networks.

5.1.3 Hardware implementation

In addition to the theoretical proposal of a 5-error-correcting, 6-error-detecting component in a product code, the hardware implementation result is reported as well in the paper [D]. The reconfigurable structure is presented for switchable implementation between 100 Gb/s and 400 Gb/s. Other data rate processing can be treated in the similar way. This technology enables a smooth upgrade of network elements to meet the demand of higher capacity in future. The analysis of the FEC implementation in a single FPGA chip is also discussed in section 4.2.

5.1.4 FEC application

From the research point of view, every single optical transmission link will refer to a FEC limit as a performance evaluation requirement. More and more system implementations choose to have FEC integrated

as a part in order to get a precise experimental result. With the help of FEC, the capacity is being pushed forward very fast without losing the transmission quality. The paper [E], with the integration of FEC, demonstrates a 100 Gb/s optical transmission with a 1550 nm VCSEL, which is considered to be a cheap solution in short distance optical transmissions. In the paper [F], FEC was applied to a DP-16QAM WDM transmission over 741 km in a metropolitan network scenario. The experimental curves do not match the simulation curves for an AWGN channel, which means the transmission channel is a non-AWGN channel. Therefore in evaluating the performance of an experiment, the post-FEC BER can not be deduced directly from the pre-FEC BER and the NCG property of a FEC code. Instead, FEC has to be implemented in a transmission system to declare the achievable BER. In another word, a perfect FEC code in a certain application has to be designed jointly with the study of the transmission channel. The analysis of experimental results on FEC performance affected by WDM channel spacing, presented in section 4.2, also indicates the necessity of a joint study on FEC and transmission channels.

5.2 Future work

The study of FEC designs approaching the Shannon limit [109] will always be of interest. To maintain the same QoS, more NCG will be desired to compensate the lost quality due to increased transmission capacity. For example, the high order modulation formats are moving from 16QAM to 64QAM, which requests for higher OSNR to maintain the same transmission distance. WDM is being put in a denser grid, which introduces more non-linear effect due to increased total power, inter-channel interference, etc. Besides, as a cost-effective way, a FEC aided transmission should not only in theory reduce the BER, but also needs to think about the implementation cost and energy consumption issues. To find a code with a high NCG, a low error floor, a simple hardware implementation and a low power consumption will still be a challenge.

The study of FEC should be carried out together with its related applications. One aspect is the channel under study. Today the research of FEC codes is independent of the transmission channels and the concept NCG is in the definition for the channel with AWGN. As we have shown in one of our experiment [F] that AWGN is not always the case

in reality, potentially a FEC code can be adapted for a specific channel to obtain better performance. When considering FEC applications at the network level, many aspects should be taken into account. Network planning itself is a broad topic, including the study of throughput, resilience, flexibility, etc. In terms of the network size, it can be categorized as local area network (LAN), metropolitan area network (MAN) and core networks. In terms of technology, it can be divided as cable, wireless and optical communications. Yet none of them is independent. They interact with each other and complicate the topic of network planning. The integration of FEC in network planning will be exciting. What code to use, how to reframe the packet structure, what is the effect are still open issues.

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List of acronyms

4PAM	4-level pulse amplitude modulation
8PSK	8-ary phase shift keying
16PSK	16-ary phase shift keying
16QAM	16-ary quadrature amplitude modulation
32QAM	32-ary quadrature amplitude modulation
64QAM	64-ary quadrature amplitude modulation
ADC	analog-to-digital converter
ARP	automatic repeat request
ASIC	application-specific integrated circuit
AWGN	additive white Gaussian noise
BBD	beyond bound decoding
BCH	Bose-Chaudhuri-Hocquenghem
BER	bit error rate
BICC	block interleaved convolutional code
BPSK	binary phase shift keying
CAGR	compound annual growth rate
CBGN	conditionally bivariate Gaussian noise model
CD	chromatic dispersion

CG	coding gain
CI-BCH	continuously-interleaved Bose-Chaudhuri-Hocquenghem
CMOS	complementary metal-oxide-semiconductor
CWDM	coarse wavelength division multiplexing
DAC	digital-to-analog converter
DBPSK	differential binary phase shift keying
DD	direct detection
DP	dual polarisation
DQPSK	differential quaternary phase-shift keying
DSO	digital sampling oscillator
DSP	digital signal processing
DWDM	dense wavelength division multiplexing
ECC	error correcting code
ECL	external cavity laser
EDFA	Erbium-doped fiber amplifier
FEC	forward error correction
FPGA	field-programmable gate array
FTN	faster than Nyquist
HD	hard-decision
HDL	hardware description language
HNLF	highly nonlinear fiber
IC	integrated circuit
ICI	inter-channel interference
IM	intensity modulation

IM/DD	intensity modulation/direct detection
IP	Internet Protocol
ITU	International Telecommunication Union
ITU-T	International Telecommunication Union's Telecommunication Standardization Sector
LAN	local area network
LDPC	low density parity check
LO	local oscillator
MAN	metropolitan area network
MDD	minimum distance decoding
NCG	net coding gain
NL	nonlinear loss
OBPF	optical band pass filter
OFDM	orthogonal frequency division multiplexing
OIF	Optical Internetworking Forum
OOK	on-off keying
OSNR	optical signal-to-noise ratio
OTN	optical transport network
OTU	optical transport unit
PAM	pulse amplitude modulation
PDM	polarization division multiplexing
PIC	photonic integrated circuit
PMD	polarization mode dispersion
PolMux	polarization multiplexing
PPG	pulse pattern generator

PS	polarization scrambler
PSK	phase shift keying
QAM	quadrature amplitude modulation
QoS	quality of service
QoT	quality of transmission
QPSK	quaternary phase shift keying
RM	Reed-Muller
ROADM	reconfigurable optical add-drop multiplexer
RoF	radio-over-fiber
RS	Reed-Solomon
SD	soft-decision
SDH	synchronous digital hierarchy
SNR	signal-to-noise ratio
SOA	semiconductor optical amplifier
SoC	system on chip
SONET	synchronous optical networking
SSMF	standard single mode fiber
TDM	time division multiplexing
TPC	turbo product code
VCSEL	vertical-cavity surface-emitting laser
VHDL	very high speed integrated circuit hardware description language
WDM	wavelength division multiplexing
XPM	cross-phase modulation

Paper [A]: Over 10 dB Net Coding Gain Based on 20% Overhead Hard Decision Forward Error Correction in 100G Optical Communication Systems

Bomin Li, Darko Zibar, Knud J. Larsen, and Idelfonso Tafur Monroy. Over 10 dB Net Coding Gain Based on 20% Overhead Hard Decision Forward Error Correction in 100G Optical Communication Systems. In *37th European Conference on Optical Communication (ECOC 2011)*, paper Tu.6.A.3, 2011.

Over 10 dB Net Coding Gain Based on 20% Overhead Hard Decision Forward Error Correction in 100G Optical Communication Systems

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Abstract: We propose a product code with shortened BCH component codes for 100G optical communication systems. Simulation result shows that 10 dB net coding gain is promising at post-FEC BER of $1\text{E-}15$.

OCIS codes: (060.2330) Fiber optics communications; (060.4510) Optical communications

1. Introduction

Ever increasing demands of bandwidth have motivated optical transmission systems to evolve from 10G to 40G to 100G. To compensate the increasing loss over the link, forward error correction (FEC) has been considered as a cost effective solution. In this paper we propose a product code with shortened BCH component codes for high speed optical communication systems with 20% overhead. Based on hard decision decoding method, it can achieve potentially 10 dB Net Coding Gain (NCG) at post-FEC bit error rate (BER) of 10^{-15} .

First generation and second generation FEC studied hard-decision FEC (HD-FEC) with various code constructions. The best reported performance is from Scholten *et al.* based on continuously interleaved BCH(1020,988) codewords of 9.35 dB NCG [1]. Justesen also mentioned around 9.3 dB NCG in [2] based on product code with BCH(1023,992) component code. Optical Internetworking Forum (OIF) recommended to increase the overhead to 20% due to the necessity for even higher NCG [3]. The study of HD-FEC is somewhat neglected afterwards.

Meanwhile, soft decision forward error correction (SD-FEC) gained a lot of interest. FPGA emulations are carried out for low density parity check (LDPC) code [4,5] and turbo product code (TPC) [6]. The achieved NCG is between 10.8 dB and 11.3 dB. Various codes are studied, including concatenation of different codes [7] and combination of codes and modulation formats [8]. Simulation results show a potential NCG between 9.7 dB and 11.38 dB. Soft decision decoding uses not only the conventional decision of value 1/0 as in the hard decision, but also information on reliabilities of these decisions. With the expense of more complexity, soft decision decoding method provides more gain than hard decision decoding method. Therefore, more effort is required for real implementation in Field Programmable Gate Array (FPGA) or Application-Specific Integrated Circuit (ASIC). As the reliability information provided to SD-FEC is from signal demodulation block, the two blocks have to be considered together in implementation. Mizuochi *et al.* demonstrated in [4] that SD-FEC and demodulation should be implemented in the same ASIC to achieve the best performance and this consequently increases the complexity of implementation. Power consumption can be another issue due to more information processing.

A difficulty in iterative decoding for HD-FEC is that the introduced decoding errors in the component codes degrades decoding performance to an unacceptable level with accumulative iterations compared to the ideal case of no decoding error. We propose a product code with shortened BCH component codes. The decoding error probability of the component code is reduced to a very low level that has almost no effect on the performance of the product code. This product code has potentially more than 10 dB NCG at post-FEC BER of 10^{-15} .

2. Code Construction and Decoding Algorithm

We choose the product code with (391,357) shortened BCH component codes as the candidate code. This code has an overhead of 20% as recommended by OIF. The code structure is shown in Fig. 1. We first construct a product code with BCH component codes in $GF(2^{11})$. In a BCH component code, the first 980 bits are fixed to 0s. The middle 357 bits are information bits and the last 34 bits are parity check bits that enable the BCH code to correct up to 3 errors. The minimum distance of the BCH code is 8 so that a codeword with 4 errors will not be decoded. The product code in $GF(2^{11})$ is then shortened by removing all fixed 0s and this returns a product code with shortened BCH component codes.

We use iterative decoding for the product code. In the component code decoding stage, each shortened component code aims to correct up to 3 errors. The principle of the component code decoding algorithm consists of

three steps: to restore the BCH code, to decode BCH code and to use the shortened bits for further check. A row or a column is a BCH codeword in $GF(2^{11})$ by extending it with 980 leading 0s. If there are no more than 3 errors, the correct codeword is returned by the decoding. However, a decoding error may happen when there are more than 3 errors in a codeword and it degrades the performance of the product code heavily after multiple iterations. We therefore propose to include a third step in the decoding algorithm to reduce the decoding error probability. If any bit in the shortened bits has value 1 in the returned BCH codeword, a decoding error is reported.

Use t to denote the maximum number of errors a code can correct. Decoding error probability of BCH code is $1/(t!)$ when there are more than t errors. In the proposed code, a BCH component code can correct up to 3 errors. So we have $t = 3$. The introduced errors from decoding error can be regarded as randomly distributed in the codeword, though there are certain relationships between the error positions and the decoding algorithm. As decoding error with 3 new errors dominates, the theoretical decoding error probability of BCH component code is $(1/(t!))(391/2047)^3 = 0.12\%$. Simulation results match the theoretical prediction.

As the decoding error probability of component codes is very small, the performance of the product code does not degrade much compared to the ideal case of no decoding error.

3. Performance Results

Fig. 2 shows the simulation result of the proposed code in an additive white Gaussian noise Channel. One iteration consists of decoding rows once and decoding columns once. After 8 iterations, the curve drops drastically between input BER $1.2 \cdot 10^{-2}$ and $1.1 \cdot 10^{-2}$. This translates to slightly more than 10 dB NCG.

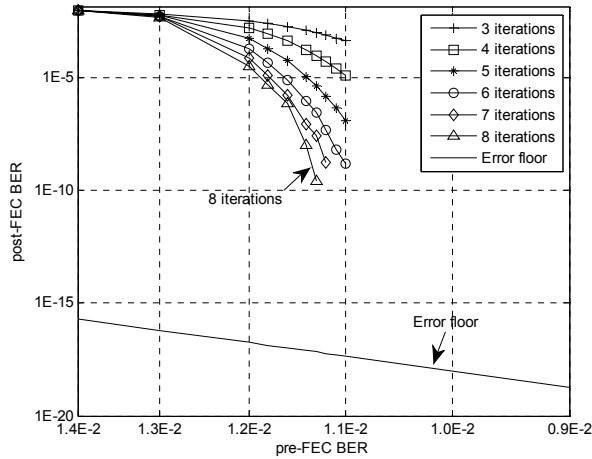


Fig. 2. BER curve

The error floor is calculated based on the formula $(16/391/391) \binom{391}{4} p^{16}$, where p is BER. This means that if the intersecting bits of 4 rows and 4 columns are all wrong, decoding fails. The error floor value is smaller than 10^{-15} as shown in Fig. 2 and no further action is required.

Due to limited number of simulated frames, we take 10 iterations into consideration in the hardware implementation to ensure enough margin to get post-FEC BER of 10^{-15} at pre-FEC BER of $1.1 \cdot 10^{-2}$.

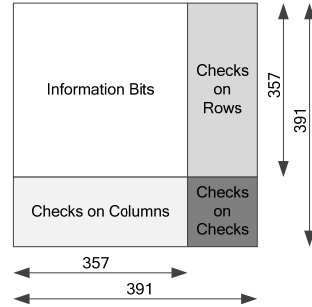


Fig. 1. Product Code Structure

4. Hardware implementation

For easy hardware implementation in future, we employed the decoding algorithm in [9] as component code decoding algorithm. The algorithm takes advantage of the property that the shift of a BCH codeword is also a codeword. For a codeword of length n , it takes n rounds to get the decoding result. In each round, with a pre-setup table, it checks whether there are only 2 or less errors left by flipping the highest bit. If so, the highest bit is flipped. Otherwise the bit keeps its value. The codeword is then shifted by one bit for the next round. After n rounds, the bits in the codeword are back at original positions. Fig. 3 shows the flow of this decoding method. It is also pointed out in [9] that the major circuit area of ROM is $(4m + 1) \cdot 2^m = (4 \cdot 11 + 1) \cdot 2048 = 90K$. We use this algorithm to find the first error bit. The rest error positions will be deduced from checking syndrome values.

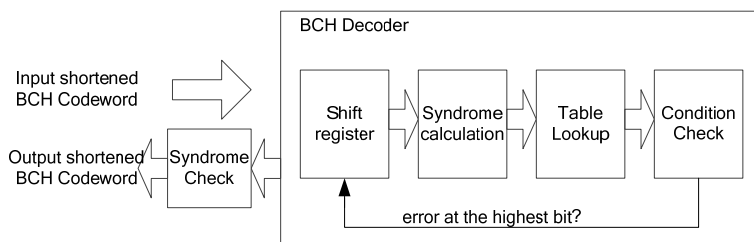


Fig. 3. Flow of Component Code Decoding

Now we look at the implementation complexity. In the row decoding of first iteration, one lookup table is shared by 4 BCH decoders. In total we need $90K \cdot 391/4 \approx 8.7M$ ROM. In this step, we will check the first 190 bits in a codeword. As 4 decoders share one lookup table, we need $190 \cdot 4 = 760$ clock cycles. The required flip-flops of shift registers are $190 \cdot 391 \approx 76K$. The result is forwarded to an interleaver of $391 \cdot 391 \approx 0.15M$ bits. In total the ROM and flip-flops in this step is $\sim 8.7M$ and $\sim 0.225M$. Column decoding is similar to row decoding. The first iteration will cost $\sim 17.5M$ ROM and $\sim 0.45M$ flip flops. The same process is repeated in the second iteration except that we check the last 190 bits when decoding each component codeword. The third iteration will repeat the process of first iteration and so forth. As most errors are corrected in the first 5 iterations, the major circuit required will be $\sim 17.5M \cdot 5 = 87.5M$ ROM and $\sim 0.45M \cdot 5 = 2.25M$ flip flops. The last 5 iterations only correct errors for a few codewords and the added redundancy is limited. It is feasible to take this implementation out in several state-of-the-art FPGAs.

Each step takes around 760 clock cycles as mentioned above. This equals to 1520 ns in case that FPGA implementation works under 500 MHz system clock frequency. To receive a frame on a $100G$ interface takes $391 \cdot 391 \cdot 10\text{ ps} \approx 1529\text{ ns}$. So the implementation is fast enough to work for $100G$ systems.

5. Conclusion

We proposed a product code with shortened BCH component code for high speed optical communication systems. The code provides potentially more than 10 dB NCG at post-FEC BER of 10^{-15} . The hardware implementation is also investigated and the FPGA verification is feasible.

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Paper [B]: Application of Beyond Bound Decoding for High Speed Optical Communications

Bomin Li, Knud J. Larsen, Juan Jose Vegas Olmos, Darko Zibar, and Idelfonso Tafur Monroy. Application of Beyond Bound Decoding for High Speed Optical Communications. In *Asia Communications and Photonics Conference 2013 (ACP 2013)*, paper AF4C.6, 2013.

Application of Beyond Bound Decoding for High Speed Optical Communications

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Abstract: This paper studies the application of beyond bound decoding method for high speed optical communications. This hard-decision decoding method outperforms traditional minimum distance decoding method, with a total net coding gain of 10.36 dB.

OCIS codes: (060.2330) Fiber Optics Communications; (060.4510) Optical Communications

1. Introduction

Optical links are currently experiencing a migration towards higher bitrates. For example, Optical access networks are now operating at 40G regimes [1], while short range systems are being developed for 400G regimes [2]. This incremental improvement in the capacity of the links is changing the paradigm of supported bit error rate (BER), which is moving from a 10^{-12} to a 10^{-15} levels [2]. This increment in the benchmark of supported BER requires improving the system performance in high speed optical fibers, from the class optics, the fiber itself and the digital signal processing algorithms. Forward Error Correction (FEC) plays a key role in this quest since it can provide extra gain to alleviate the technology pressure on the optical side of the system while supporting the signal quality levels. During the past several years, FEC has been integrated in various systems to obtain the desired performance. Foresight examples are studies of WDM Performance and Multiple-Path Interference Tolerance [3], and High-Speed 1550 nm VCSEL [4]. Overall, it becomes utmost important to come up with FEC codes of higher gain and faster processing capability.

In this paper we study beyond bound decoding method, employing the same code as proposed in [5]. Without changing the encoding structure, 0.36 dB more net coding gain (NCG) is achieved, with a total NCG of 10.36 dB. The pre-FEC BER of this 20% overhead hard decision code is $1.4 \cdot 10^{-2}$ and it is above the theoretical threshold obtained by applying minimum distance decoding method. The solution proposed in this paper meets the technical requirements in terms of latency, complexity and gain for next generation optical networks.

2. Principle of Beyond Bound Decoding

Product code with shortened BCH components for high speed optical communications was first studied in [5]. The component code is a shortened BCH code of length $n \leq 2^m - 1$ as shown in Figure 1. The number of information bits in a row/column is denoted k . By inserting $2^m - 1 - n$ leading zeros, each row/column becomes a BCH codeword.

At the decoding part, iterative decoding is employed for the product code. One iteration consists of decoding a product code horizontally once and vertically once. Each row/column is decoded by a component decoding method. In [5], the component decoding method is minimum distance decoding. In this paper, the component decoding method is beyond bound decoding. All returned error bits are checked to be within n bits of a received word or not.

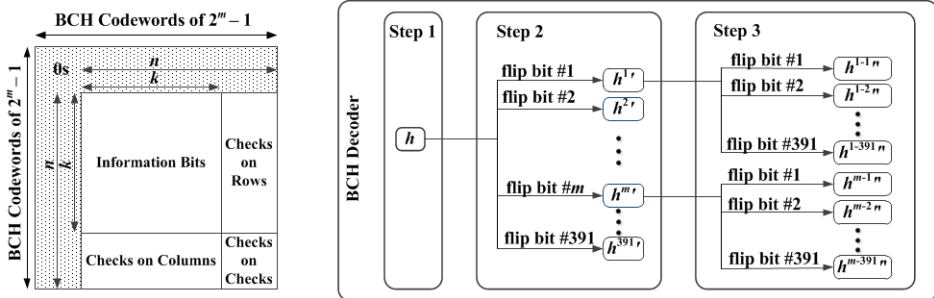


Fig. 1: Code Construction and Circuit Implementation Investigation

Tab. 1: Component Decoding Error by Beyond Bound Decoding

Error Weight (t)	h_0	h_1	h_2	h_3	Decoding Success (%)	Decoding Error (%)	Comments on Decoding Error
0	0	1	1	1	100	0	-
1	1	0	1	1	100	0	-
2	0	0	0	1	100	0	-
3	1	x	0	0	100	0	-
4	0	x	x	0	88.8	-	11.2% not being decoded due to multiple candidate four-error patterns
5,7,9,...	1	x	0	0	0	< 0.12	-
		others			0	-	100% not being decoded
6,8,10,...	0	0	0	1	0	< 0.12	two-error pattern
		x	x	0	0	10.1	unique four-error pattern
		others			0	-	100% not being decoded

If not, decoding error is reported. It is called error position check later in this paper. To keep the encoding part untouched, the code of the same parameters are used in this paper as in [5], that is, $n = 391$ and $m = 11$.

The component has minimum distance of eight. With minimum distance decoding, it only corrects up to three errors. Beyond bound decoding, which is studied in this paper, aims to correct up to four errors. The method is explained in [6]. The basic idea of decoding is to change the value of each bit and check whether the weight of errors is reduced. If so, the value of this bit should be changed, otherwise the original value is kept. A vector $h = [h_0 h_1 h_2 h_3]$ is built to help with error weight change detection. The value h_0 is an even parity check bit while h_1, h_2 and h_3 are the opposite values of corresponding determinants of syndrome matrices. The construction of syndrome matrices follows the rule for BCH code. Table 1 shows the values of the vector h for different weight error patterns.

Component decoding error is a practical issue in iterative decoding of a product code as introduced errors increase decoding iterations. These introduced errors may also possibly build a non-decodable error pattern together with existing errors. Therefore it is important to reduce component decoding error probability. An overview of component decoding error probability is shown in Table 1, where x means do-not-care.

Vectors h' and h'' are calculated to help finding the reduction of error weights. After first flipping the value of one bit, the vector h' is obtained in the same way h is obtained. For example, flip the value of bit 1 and the calculated value of h' is denoted h^1 , as shown in Figure 1. Similarly, the vector h'' is obtained after first flipping the values of two bits. For $t \leq 3$, error correction is done by comparing h and h' . If the error weight is reduced, a candidate error bit is found. Flip all bits one by one and all error bits are returned. All received words in this case are decoded successfully without decoding error. For $t = 4$, most of errors should be corrected by beyond bound decoding. If the error weight is reduced to two by comparing h and h'' , two candidate error bits are found. Update the received word and decode it to find the other two candidate bits as discussed for $t \leq 3$, which in turn builds a candidate pattern. A candidate pattern is wrong if it does not pass error position check. Notice that candidate four-error patterns are not unique. To find all candidate patterns, the combinations of any two bits should be considered in the stage of calculating h'' . Multiple successful candidate patterns prevent a received word from being decoded. The probability of not being decoded can be theoretically calculated in this way. Flip one bit to build a five-error pattern and the decoding error probability is $0.116 \cdot 10^{-2}$ as calculated for the case of $t = 5$. As there are $n - 4$ positions that may return wrong candidate error patterns and each pattern contains four error bits, the probability of not being decoded is $0.116 \cdot 10^{-2} \cdot (n - 4)/4 = 11.2\%$. For $t \geq 5$ and t is odd, the decoding error probability is explained in [5]. It can also be considered in the way of the probability that a random odd-number-error-pattern syndrome corresponds to a three-error pattern [8]. The value is $(1/(3!)) \cdot (n/(2^m - 1))^3 = (1/(3!)) \cdot (391/(2^{11} - 1))^3 = 0.116\%$. For $t \geq 6$ and t is even, it could be wrongly decoded with either a two-error pattern or a four-error pattern. The decoding error probability of a two-error pattern can be analyzed similarly to the case of $t = 5$ and it is much smaller. The decoding error probability of a four-error pattern is the probability of finding one and only one successful four-error pattern. It is $(n/4) \cdot (0.116 \cdot 10^{-2}) \cdot (1 - 0.116 \cdot 10^{-2})^{(n-4)/4} = (391/4) \cdot (0.116 \cdot 10^{-2}) \cdot (1 - 0.116 \cdot 10^{-2})^{(391-4)/4} = 10.1\%$.

3. Simulation Result of the Product Code

The simulation results in Matlab are shown in Figure 2. Simulation results of 10 iterations with white Gaussian noise are shown for both beyond bound decoding method and minimum distance decoding method. The pre-FEC BER of the product code is around $1.4 \cdot 10^{-2}$ by employing beyond bound decoding method. And this translates to 10.36 dB NCG. As shown in Figure 2, there is 0.36 dB improvement in NCG compared to the value of employing minimum distance decoding method.

The theoretical threshold of applying minimum distance decoding method to this 20% overhead hard-decision FEC is $1.3 \cdot 10^{-2}$, aiming for an after-FEC BER of 10^{-15} , as explained in [7]. The simulation shows a pre-FEC BER of around $1.1 \cdot 10^{-2}$ in [5], which falls below the threshold when minimum distance decoding method is employed. In this paper the pre-FEC BER is around $1.4 \cdot 10^{-2}$, which is above the threshold due to stronger decoding capability to of beyond bound decoding method.

The error floor of the product code in this paper is lower than the one in [5], as beyond bound decoding corrects more errors than minimum distance decoding does. The error floor is $< 10^{-15}$ for BER at $1.4 \cdot 10^{-2}$, also shown in Figure 2.

4. Circuit Implementation Investigation

The circuit implementation investigation is also shown in Figure 1, aiming for easy implementation and fast processing. Step 1 is to calculate the vector h . Syndrome storage costs 34 registers, so we estimate 100 registers in total and 8 clock cycles. Step 2 is to calculate h' . Actual values are h^1, h^2, \dots, h^{391} . After bit m ($1 \leq m \leq n$) is flipped, the obtained h' is denoted h'^m . A flag is inserted if it shows an error weight reduction. If all flags indicate q ($0 < q < 3$) errors and there are $q + 1$ flags, the $q + 1$ flags associated positions reflect error bits. For example, suppose the errors are at bits r, s and u . Three flags are inserted after checking h' at the positions of h'^r, h'^s and h'^u , all indicating two errors. At this step, up to three errors will be corrected. We estimate around 10 registers and 8 clock cycles for each h'^m . And 391 copies are required. Step 3 is designed to help finding four-error pattern. It calculates the value of h'' . Actual values are $h^{1-1}, h^{2-1}, \dots, h^{391-1}, h^{1-2}, \dots, h^{391-2}, \dots, h^{1-391}, \dots, h^{391-391}$. Here h^{m-p} ($1 \leq m \leq n, 1 \leq p \leq n$) is the vector h' of h'^m by flipping bit p in step 3. A flag is inserted if the error weight is reduced to two after flipping bit m and bit p . For bit m in step 2, if the number of associated flags in step 3 is three, m is an error bit. Otherwise bit m is left unchanged. The check of flags performs error position check. For example, suppose the errors are at bits r, s, u and v , each bit has three associated flags, that is, flags $h'^{r-s}, h'^{r-u}, h'^{r-v}$ for bit $r, h'^{s-r}, h'^{s-u}, h'^{s-v}$ for bit $s, h'^{u-r}, h'^{u-s}, h'^{u-v}$ for bit u and $h'^{v-r}, h'^{v-s}, h'^{v-u}$ for bit v . We estimate 1 register and 1 clock cycle to calculate and store the final value of error weight indication. Again 391 copies are required. In total the cost for a component decoder is $100 + (10 + 1) \cdot 391 \approx 4401$ register bits and 17 clock cycles. A product code decoder includes 391 copies of a component decoder as well as an interleaver. This requires $391 \cdot 4401 + 3912 = 1.85$ M register bits. Considering 10 iterations of a product code decoding, it takes $10 \cdot 2 \cdot (17 + 1) = 360$ clock cycles. The implementation is fast enough for FEC decoding in 100 Gb/s optical transmissions in an FPGA with a 250 MHz system clock.

5. Conclusion

The application of beyond bound decoding is studied in this paper. A high NCG of 10.36 dB for a product code is obtained in the simulation while the circuit implementation investigation shows the fast processing capability of the code. Meanwhile it keeps the encoding part unchanged. These features meet the current development guides in high speed optical communication links, especially in optical access systems where solutions to reduce the complexity of the optical side are preferred, and in high capacity 400G links, where FEC codes provide more gain to support stricter requirements on BER.

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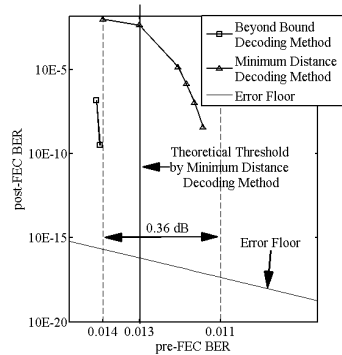


Fig. 2 Simulation Result

Paper [C]: Adaptive Forward Error Correction in High Speed Optical Communications

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Adaptive Forward Error Correction in High Speed Optical Communications

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Abstract

A rate-adaptive coding scheme using two-layered variable rate forward error correction (FEC) for Optical Fiber Transmission Systems with fixed signal constellation and fixed symbol rate is proposed. The first level of coding uses serially concatenated Reed-Solomon (RS) codes with hard-decision decoding which provides a coding gain of up to 12.25 dB. For lower SNR transmissions, a second layer of coding is employed, using either an extended Hamming(8,4,4) code or a Reed-Muller(1,4) code together with soft-decision decoding, with 3-bit quantization. The extended Hamming(8,4,4) code extends the coding gain up to 15.75 dB, while the Reed-Muller(1,4) works up to 18 dB. All coding gains are calculated for an output BER of 10^{-15} . The rate-adaptive algorithm counts the number of values in certain quantization intervals and uses this to estimate the standard deviation and SNR. Estimation error is less than 0.15 dB. The coding scheme proposed is able to handle SNR variations in the range from 10 down to 0 dB, providing information bit rates starting from 100 Gbit/s down to 14.33 Gbit/s when the theoretical transmission bit rate is assumed to be 114.095 Gbit/s.

Keywords: Forward Error Correction, rate-adaptive coding, coding gain, Bit-Error Rate, Signal-to-Noise Ratio;

Selection and/or peer review under responsibility of Prof. Dr. Dogan Ibrahim.

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1. Introduction

Modern optical communication systems employ Forward Error Correction (FEC) to achieve the required performance, but today's optical transmission systems use fixed code rates. However it is not uncommon that the parameters of the channel will vary in time and thus the amplitude of the noise

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will also change. A fixed code rate should handle the worst-case scenario, but this will limit the information bit rate when the channel conditions are better. This means that it is of interest to design a rate-adaptive coding scheme which chooses the best suited code rate. To our knowledge this rate adaptive solution has been studied only in [1], or with limited rate variation in [2] and [3].

This paper is organized in two major parts, first the proposed variable rate FEC coding scheme is discussed and then the solution for the Rate Adaptive Algorithm (RAA) is presented, where the RAA has the role of estimating the Signal-to-Noise Ratio (SNR). We want to satisfy long haul optical transmission requirements and thus aim to cover a SNR range from 0 to 10 dB.

2. Variable Rate FEC Coding Scheme

In the figure below an overview of the overall system is presented:

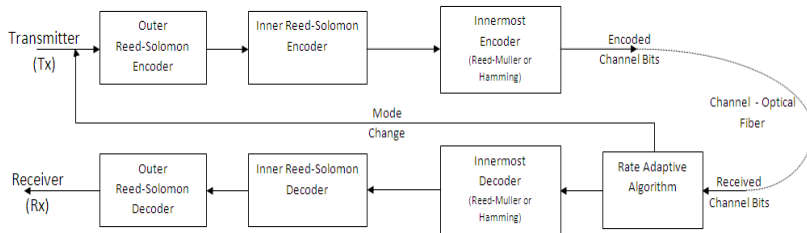


Figure 1. FEC chain

The encoding is structured in two layers. The first layer uses Reed-Solomon (RS) codes over the Galois Field (GF) of size 2^8 . The information is organized into two-dimensional frames, as seen in Figure 2, and both rows and columns are RS encoded. The initial parameters of this concatenated RS-RS codes are $(n, k) = (255, 203)$, where n is the length of the RS codeword and k is the number of information symbols within the codeword, for both row and column encoding. To obtain other rates for the concatenated RS-RS code, shortening (for lowering the rate) and puncturing (for increasing the rate) are used. The parameters of these code rates can be seen in the table below (indices 1, 2 for shortening and 4, 5 for puncturing):

Table 1. RS-RS codes parameters and indices

index	n_o	k_c	n_r	k_r	n_c^p	n_r^p	$n_t^s = k_r^s$	n	k	rate
5	217	203	217	203	38	38	0	47089	41209	0.8751
4	235	203	235	203	20	20	0	55225	41209	0.7462
3	255	203	255	203	0	0	0	65025	41209	0.6337
2	255	203	151	99	0	0	52	38505	20097	0.5219
1	255	203	105	53	0	0	150	26775	10759	0.4018

We have observed slightly better error correcting capabilities for RS-RS codes having the same overall rates, but with different numbers of redundancy symbols for columns and rows, like the ones proposed in [1]. However concatenated RS-RS codes with an equal number of redundancy symbols for both rows and columns were chosen because they provide the least complexity for the RS decoders (extended Euclidian algorithm followed by Chien search used for decoding).

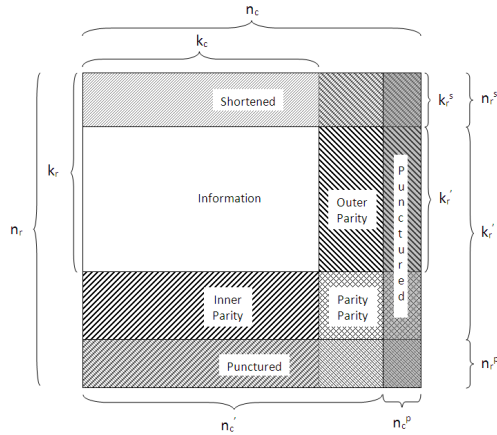


Figure 2. Frame structure

For practical implementation of the concatenated RS-RS codes, puncturing is not a viable option, so RS code rates obtained by puncturing are replaced by RS codes having the same error correcting capability as the ones obtained by puncturing. There is no significant difficulty in implementing such variable rate encoders and decoders.

The target SNR range for this rate adaptive FEC system is 0 dB to 10 dB. The maximum decoder output bit error rate (BER) for the system is aimed at the usual goal, 10^{-15} . Without encoding this requires a SNR higher than 18 dB. The concatenated RS-RS codes provide good coding gains of up to 12.25 dB. However this is not enough to satisfy SNR values less than 5.75 dB. That is why an innermost layer of encoding is added, made out of either the extended Hamming(8,4,4) or Reed-Muller(1,4) codes. To maximize the error correcting capabilities of this second layer soft decision decoding is used, and to keep the Analog-to-Digital Converter (ADC) complexity limited, a 3 bit quantization is proposed as seen in Figure 3. The gain from using more bits was found to be negligible. The second layer of encoding extends the coding gains up to 18 dB, which is enough to cover the whole target SNR range.

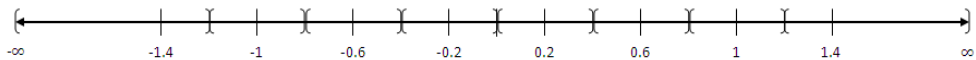


Figure 3. The proposed 3-bit Quantization scheme

The system proposed here has basically the same transmission parameters as in [1] and equation (1) is used to compute the information bit rate R_b [1]:

$$R_b = 2r_L r_C r_R R_s \log_2 M \quad (1)$$

where $r_L = 64/66$ is line code rate used in 10Gbit Ethernet, r_C is the rate of the RS-RS code, r_R the rate of the innermost code, R_s the theoretical symbol rate of the transmission, M the order of the modulation, and 2 quantifies the number of fiber modes (polarization modulation transmission [1]). Thus the bit rate for an uncoded system will be 114 Gbit/s, and by using the proposed coding scheme information bit rates starting from 14.33 up to 100 Gbit/s are obtained.

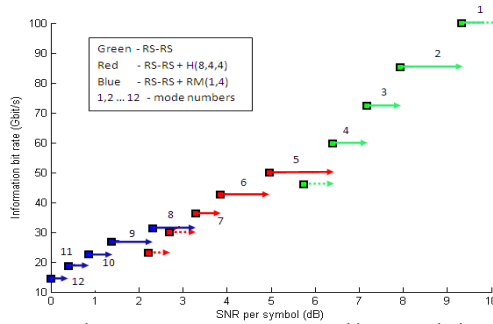


Figure 4. Achievable information bit rate versus SNR. Horizontal lines mark the SNR covered by every mode

In Figure 4 the achievable information bit rates for all modes (15 possible) are illustrated, where we define the mode as the combination of concatenated RS-RS codes and innermost codes that is able to correct the errors for a certain SNR interval. The dotted lines mark suboptimal modes (their information bit rate is lower than that of another mode of lower rate). These results were obtained using the 3 bit quantization defined in Figure 3.

3. Rate-Adaptive Algorithm

The coding scheme is in place but a way to choose the right mode is needed. This means the channel noise, and thus the SNR, must be estimated.

We start by choosing two quantization intervals and, for each received frame, counting the number of values that fall within those quantization intervals. By dividing this number with the total number of bits in the received frame we get an estimate of the probability of a value to fall within that area, P_{inside} .

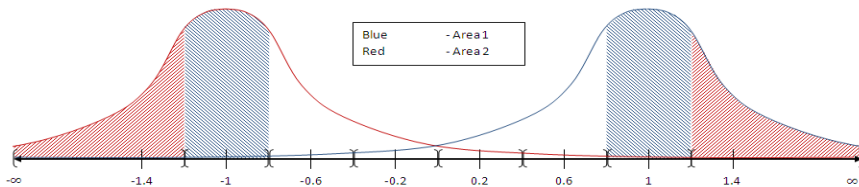


Figure 4. Quantization levels (seen on the axis) and the two areas that are used for counting, where Non Return to Zero channel coding was considered (0 bit = -1, 1 bit = 1)

Since the channel is approximated as being an Additive White Gaussian Noise (AWGN) channel, we have the signal-to noise ratio as:

$$SNR = P_{signal} / P_{noise} = (A_{signal}/A_{noise})^2 = 1/\sigma^2 \quad (2)$$

and we can use the properties of the Gaussian distribution to express the probability P_{inside} as follows:

$$P_{inside} = \text{erf}(z/\sqrt{2}) \leftrightarrow z = \sqrt{2} * \text{erfinv}(P_{inside}) \quad (3)$$

where z represents the number of standard deviations from the mean and $\text{erf}()$ is the error function. For area 1 we count values that are at most 0.2 away from the mean (which are -1 or 1). But with

equation 2 we also get the equivalent of this in standard deviation, so by dividing 0.2 with z we get an estimate of the standard deviation. Equation (2) is then used to obtain the SNR.

When counting the values in area 2 we practically do the same thing as counting the number of values outside area 1, $P_{outside}$, but only on one side of the mean (so we must multiply the counted number by 2). If we take $P_{inside} = 1 - 2P_{outside}$, then equations (2) and (3) can be used to get the SNR estimate for area 2.

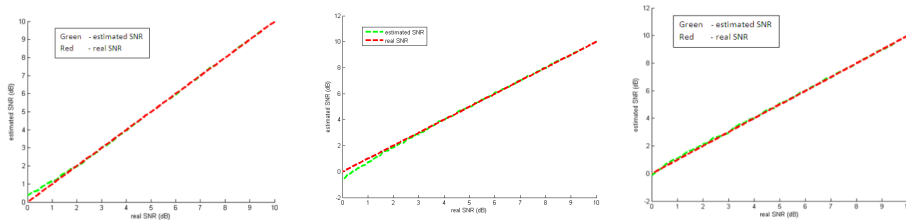


Figure 5. SNR estimate compared to true SNR, when: a. counting in area1, b. counting in area2, c. summing the estimates from the two areas

The SNR estimation results for the two areas can be seen in Figure 5a and 5b. The estimates are very good for SNRs larger than 2 dB, but under this value the precision of the estimation starts to drop. We notice that the estimation errors for the two areas are more or less the same, but they have opposite signs, so by summing the two we can eliminate much of the error, as seen in Figure 5c. In fact estimation errors using this method will be under 0.15 dB.

The estimate is then used to decide which mode should be used, and this information is transmitted back to the receiver.

4. Conclusions

A rate-adaptive coding scheme is presented which provides coding gains of up to 18 dB. The parameters chosen for the concatenated RS-RS codes ensure minimum complexity for the RS decoder. By exploiting the distribution of values within the different quantization levels and the properties of the Gaussian distribution, a very accurate estimate for the SNR is obtained, where the estimation error is below 0.15 dB for any SNR. However further investigations into the nature of the optical fiber channel are needed, since the AWGN model does not reflect all effects. As a consequence of this, changes to the RAA might also be needed.

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Paper [D]: Forward Error Correction for 400 Gbps High Speed Optical Fiber Links

Bomin Li, Knud J. Larsen, Darko Zibar and Idelfonso Tafur Monroy. Forward Error Correction for 400 Gbps High Speed Optical Fiber Links. Submitted to *IEEE Communications Letters*.

Forward Error Correction for 400 Gbps High Speed Optical Fiber Links

Bomin Li, Knud J. Larsen, Darko Zibar and Idelfonso Tafur Monroy

Abstract— This paper studies a reconfigurable forward error correction scheme for 100/400 Gbps high speed links. A product code with five-error-correction components is chosen as the candidate code, which provides a high net coding gain and a low error floor. Simulation shows a net coding gain of 10.4 dB at post-FEC bit error rate of 10^{-15} . A proof of concept synthesis result is also presented, which shows the reconfiguration flexibility in 100/400 Gbps high speed links.

Index Terms—Forward error correction, Optical fiber communication, Reconfigurable architectures.

I. INTRODUCTION

Forward Error Correction (FEC) plays an important role in today's high speed optical communications. The research on forward error correction has been rapidly evolved from 2.5 Gbps to 100 Gbps, following the trend of the evolvement of high speed optical fiber communications. Many results for optical fiber transmission links at 400 Gbps have been reported. One example is an experiment on 400 Gbps transmission over 4,800 km with the help of wavelength division multiplexing (WDM) and advanced modulation format [1]. The research on Tbps transmission has also been carried out. For example, a demonstration on a transmission of a 32.5 Tbit/s is presented in [2]. These trends make research of FEC towards 400 Gbps and above essential. A starting point is to aggregate 4 lanes of 100 Gbps data links. However, the requirement of a single FEC solution can be foreseen. The IEEE 802.3 400G study group published initial thoughts on a single FEC solution [3]. Though the study is for 400G Ethernet, it shows the trend for future high speed links.

With the data transmission speed going up, the reference bit error rate (BER) will be stricter to better evaluate the system performance. Today the value is 10^{-15} , which is lower than the reference BER from decades ago. The value of 10^{-17} is one of the proposals for 400GE [4]. A high net coding gain (NCG) is desired in the meanwhile. Therefore, we study in this paper a product code with five-error-correction and six-error-detection BCH components. To ease the calculation, we choose the component code of 511 bits. This product code has a 20.8% overhead and can achieve a reference BER of $5 \cdot 10^{-44}$ at an input BER of $1.45 \cdot 10^{-2}$, which translates to a NCG of 15.2 dB. With today's recommended reference BER of 10^{-15} , the calculated

NCG is about 10.4 dB. We report also on the FPGA implementation analysis for 400 Gbps processing and on a reconfigurable scheme.

II. PRODUCT CODE

We study the product code with BCH components in the finite field $GF(2^9)$. The code structure is shown in Fig. 1. The component BCH code has a length of 511 bits, within which 46 bits are parity check bits. Therefore the product code has 261,121 bits in length and the code overhead is 20.8%. A component is a five-error-correction and six-error-detection BCH code.

Iterative decoding is employed for the product code. Row components and column components are decoded iteratively. In component decoding, if there are five error bits or less, all errors are corrected in the decoded component. If there are six error bits or more, the component is not changed in the decoding step. The decoding error probability is very small, i.e., $1/2(t!) = 0.0042$, where t is the number of errors a BCH code can correct and the value 2 in the denominator distinguishes even number of errors and odd number of errors. Therefore the introduced error by decoding error can be ignored when evaluating the system performance.

The error floor is the region where the output BER does not improve despite of the number of iterations. How error floor is analyzed for a product code is explained in [5]. Fig. 2 shows the

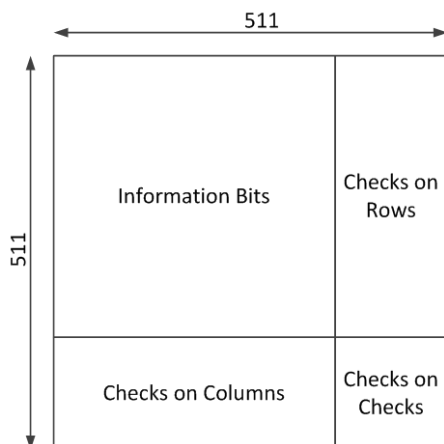


Fig. 1. Product Code Structure

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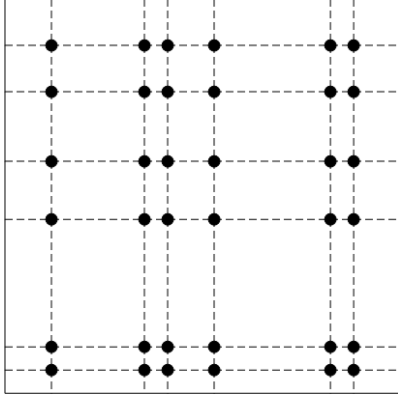


Fig. 2. Error Floor Error Pattern

simplest error pattern that fails a product code with five-error-correction components, where dashed lines stand for BCH codes and black spots stand for error bits. It is a 36-error pattern that fails component decoding in 6 rows and 6 columns. The upper bound expression of the error floor at the BER of p is $\frac{36}{511^2} \binom{511}{6} p^{36}$.

III. SIMULATION RESULTS

Fig. 3 shows the simulation results of the studied product code in an additive white Gaussian noise (AWGN) Channel, done in Matlab. One iteration consists of decoding rows once and decoding columns once. The line with solid triangles shows the result after 7 iterations and the line with solid circles shows the result after 9 iterations. These two lines drop drastically at the pre-FEC BER of $1.46 \cdot 10^{-2}$ and $1.48 \cdot 10^{-2}$ respectively. The theoretical error floor values at these pre-FEC BERs are $6.59 \cdot 10^{-44}$ and $1.07 \cdot 10^{-43}$ respectively. Considering eight iterations, the pre-FEC BER is around $1.45 \cdot 10^{-2}$ and the reference BER can be as low as $5 \cdot 10^{-44}$. This pre-FEC value falls in below the theoretical threshold of $1.64 \cdot 10^{-2}$ based on the analysis method in [5]. The achievable post-FEC BER is much lower than the currently used reference of 10^{-15} . The NCG is 10.4 dB with 10^{-15} as the reference BER..

In the range of the pre-FEC BER of $1.45 \cdot 10^{-2}$ and below, the error floor is less than 10^{-43} .

IV. SYNTHESIS RESULTS

The product code is decoded with eight iterations, that is sixteen half iterations. A half iteration consists of a BCH decoder block and an interleaver block. Fig. 4 shows the reconfigurable interleaver block. To make a proof-of-concept synthesis, the system clock is set to 200 MHz. All the synthesis is done by Quartus II 13.0 with the device setup of Stratix IV EP4SE820F43C3.

In the interleaver block, the data matrix is divided into

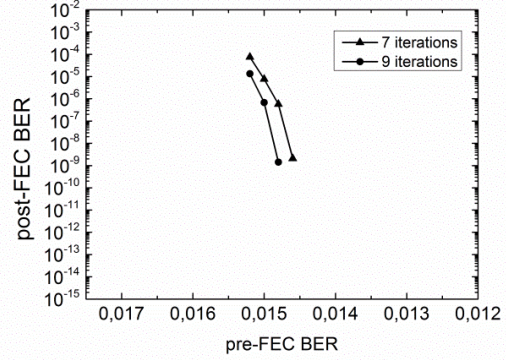


Fig. 3. Simulation Results

sixteen small blocks. Denote them from $M_{1,1}$ to $M_{4,4}$. As the length of a component is 511, we pad one row 0s and one column 0s to make sixteen small blocks identical. In the receiving part, the number of input interfaces is pre-configured. In 100 Gbps data links, since the system clock is 200 MHz, to receive and store one BCH codeword at one clock cycle would be fast enough. So the interleaver is configured to have only one input interface (BCH_in #1). The other three BCH input interfaces are suppressed. Each clock cycle the received BCH codeword is fed into the last row in $M_{4,i}$ ($1 \leq i \leq 4$) and all existing codewords are shifted one row up from the bottom of $M_{4,i}$ to the top of $M_{1,i}$ ($1 \leq i \leq 4$) as shown in Fig. 4. In 400 Gbps data links, four BCH input interfaces are required for the interleaver to be fast enough to process all data. BCH codewords from interface #1, #2, #3 and #4 are fed into the last rows of $M_{4,i}$, $M_{3,i}$, $M_{2,i}$, and $M_{1,i}$ ($1 \leq i \leq 4$). Existing codewords

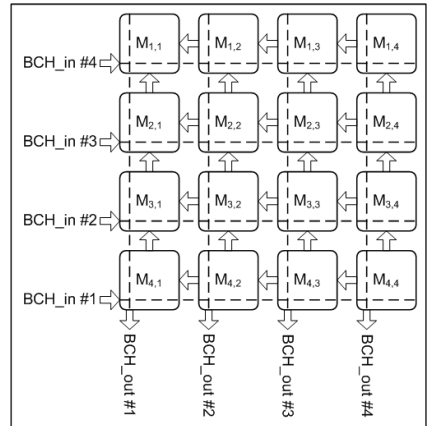


Fig. 4 VHDL Implementation of Interleaver

are shifted one row up inside each small block. After all BCH codewords are received, the output part starts to send interleaved BCH codewords. The output part is similar to the input part. Data is shifted from the right to the left, also shown in Fig. 4. Only interface #1 is used in 100 Gbps data links while all four interfaces output valid BCH codewords in 400 Gbps data links. BCH decoders are connected to active BCH output interfaces. This structure provides not only the advantage of reconfiguration, but also makes it possible to get the synthesis done in multiple devices if necessary. BCH decoder employs the algorithm in [6]. The block synthesis results are shown in Table I.

The estimated resource for FEC implementation is shown in Table II. The implementation presented above is very flexible. Higher speed data links can be supported by increasing the number of block divisions in the interleaver as well as increasing the number of BCH interfaces. The synthesis result can be improved. For example, a faster system clock can be expected, which in turn can reduce the number of BCH interfaces, given a desired data link. Furthermore, BCH decoders of other decoding algorithms can easily be plugged in and the data matrix in the interleaver can be possibly implemented by both registers and memory blocks. All these can well balance the resource usage between registers and memory blocks.

V. CONCLUSION

The product code with five-error-correction and six-error-detection BCH components is studied for 400 Gbps high speed transmissions. Simulation analysis shows high coding gain and extremely low error floor of $5 \cdot 10^{-44}$. The synthesis analysis shows feasible implementation in hardware. This scheme can be flexibly configured to process data in high speed links of 100 Gbps or 400 Gbps or higher, meeting the demand of future high speed systems.

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TABLE I
SYNTHESIS RESULTS OF BLOCKS

Block	ALUTs	Memory ALUTs	Registers	Block memory bits
BCH decoder	~30K	~2K	~50K	~2M
$M_{1,1}$, $M_{2,1}$, $M_{3,1}$ and $M_{4,1}$ in total	~100	0	~132K	0

TABLE II
ESTIMATED RESOURCE OF FEC IMPLEMENTATION

Data Links	ALUTs	Memory ALUTs	Registers	Block memory bits
100 Gbps half iteration	~30K	~2K	~578K	~2M
100 Gbps eight iterations	~480K	~32K	~9.25M	~32M
400 Gbps half iteration	~120K	~8K	~728K	~8M
400 Gbps eight iterations	~1.92M	~128K	~11.65M	~128M

Paper [E]: High-Speed 1550 nm VCSEL Data Transmission Link Employing 25 GBd 4-PAM Modulation and Hard Decision Forward Error Correction

Roberto Rodes, Michael Müller, **Bomin Li**, Jose Estaran, Jesper Bevensee Jensen, Tobias Gruendl, Markus Ortsiefer, Christian Neumeyr, Juergen Roskopf, Knud J. Larsen, M.-C. Amann, and Idelfonso Tafur Monroy. High-Speed 1550 nm VCSEL Data Transmission Link Employing 25 GBd 4-PAM Modulation and Hard Decision Forward Error Correction. *Journal of Lightwave Technology*, vol. 31, no. 4, pp. 689–695, 2013.

High-Speed 1550 nm VCSEL Data Transmission Link Employing 25 GBd 4-PAM Modulation and Hard Decision Forward Error Correction

Roberto Rodes, Michael Müeller, Bomin Li, Jose Estaran, Jesper Bevensee Jensen, Tobias Gruendl, Markus Ortsiefer, Christian Neumeyr, Juergen Roskopf, Knud J. Larsen, M.-C. Amann, and Idelfonso Tafur Monroy

Abstract—Current short-range optical interconnects capacity is moving from 100 to 400 Gb/s and beyond. Direct modulation of several laser sources is used to minimize bandwidth limitations of current optical and electrical components. This total capacity is provided either by wavelength division multiplexing or parallel optics; it is important to investigate on the ultimate transmission capabilities of each laser source to facilitate current capacity standards and allow for future demands. High-speed four-level pulse amplitude modulation at 25 GBd of a 1.5 μm vertical-cavity surface-emitting laser (VCSEL) is presented in this paper. The 20 GHz 3 dB-bandwidth laser is, at the time of submission, the largest bandwidth of a 1.5 μm VCSEL ever reported. Forward error correction (FEC) is implemented to achieve transmission over 100 m virtually error free after FEC decoding. Line rate of 100 Gb/s is achieved by emulation polarization multiplexing using 50 Gb/s signal obtained from a single VCSEL.

Index Terms—Fiber optics communication, forward error correction (FEC), Four-level pulse amplitude modulation (4-PAM), optical interconnects, vertical-cavity surface-emitting lasers (VCSELs).

I. INTRODUCTION

THE rapid growth of Internet and cloud computing applications drives data centers to upgrade their links from the 10 Gb/s commonly used today to 100 Gb/s and beyond in the near future [1] with little or no increase in carbon and real-estate footprint [2]. These two counteracting demands lead to a quest for higher data capacity on short-range optical communication systems. Simultaneously, directly modulated vertical-cavity sur-

face-emitting lasers (VCSELs) are rapidly becoming the preferable type of laser source for these short-range optical interconnect applications due to an attractive combination of attributes, including high modulation bandwidth, low drive voltage [3], and the capability of array integration [4]. Short-wavelength VCSELs have demonstrated modulation speeds up to 40 Gb/s at 850 nm [5], and 44 Gb/s at 980 nm [6]. However, until lately, VCSELs with modulation speed exceeding 10–14 Gb/s have not been available at wavelengths in the *O* and *C* bands around 1300 and 1550 nm, respectively. Recently, direct modulation of 1550 nm VCSELs at 40 Gb/s has been demonstrated [7].

Currently, high-capacity interconnects use the combination of several optical sources to satisfy higher capacity demand. Parallel optics with independent transmission channels or wavelength division multiplexing are both considered and under development.

Parallel optics transceiver modules based on VCSELs have been recently demonstrated up to 480 Gb/s [8]. The module is a single chip 90 nm CMOS integrated circuit with 24 lasers. Each of them modulated at 20 Gb/s.

The existing 100 Gb/s standard for short-range interconnects (100GE-SR10) specifies the use of ten wavelengths each operated at 10 Gb/s, while the next-generation standard (100GE-SR4) specifies the employment of four lasers each operated at 25 Gb/s [9]. Beyond 100 Gb/s, the next OTN rate (OTU5) will be most likely 400 Gb/s, where a proposed architecture is to scale the same technology of 100GE-SR4 to 400GE-SR16 for a cost-effective solution [10]. This solution does not need higher bandwidth transceivers, reducing the associated cost of investment on R&D to develop new technology. However, scaling the same technology will hardly be feasible for more than 16 channels. Quadrupling the data modulation of each laser or channel to 100 Gb/s represents a much more drastic step forward, and can potentially pave the way for 1) an increase in the total link capacity to 400 Gb/s or to 2) a reduction in footprint and complexity of the 100 Gb/s links.

In this paper, we report on research investigation on the capabilities of using VCSELs to achieve high-speed transmission for short-range optical interconnects. We have performed direct modulation of a VCSEL by employing a four-level pulse amplitude modulation (4-PAM) at 25 GBd. This is not a single VCSEL link, as two different polarizations are required. However, in the experiment, we have used a single VCSEL source. The optical signal from the VCSEL was split, delayed, and com-

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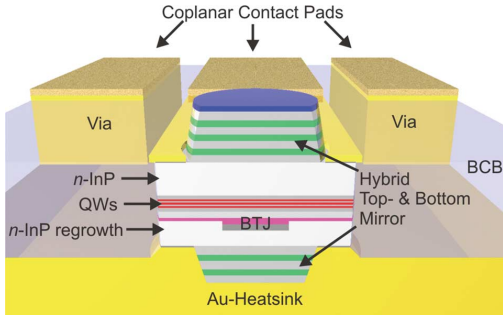


Fig. 1. SC structure of the indium-phosphide-based BTJ VCSELs.

bined in orthogonal polarizations to emulate polarization multiplexing with a total line rate of 100 Gb/s. Forward error-correction (FEC) coding has been implemented resulting in an effective bit rate of 86.5 Gb/s. Error-free demodulation was demonstrated in the experiment with 1.6×10^8 bits of FEC decoding.

II. HIGH-SPEED VCSEL

VCSELs are currently attracting a lot of attention for short-range optical links due to their potential cost-effective fabrication, low power consumption, easy fiber-coupling, and high-bandwidth modulation. For the 1550 nm wavelength range, indium-phosphide-based buried tunnel junction (BTJ) VCSELs implementing a novel short-cavity (SC) concept have recently shown the most promising results with respect to energy-efficient high data-rate transmission [11]. The following two paragraphs shortly discuss the device concept and provide the static and dynamic features of these SC VCSELs.

A. Device Structure

In order to achieve high modulation bandwidth, it is beneficial to reduce the effective cavity length and, consequently, the photon lifetime in the VCSEL cavity [12]. Therefore, the SC-VCSEL concept implements two dielectric distributed Bragg reflectors (DBRs) featuring a short penetration depth of the optical field of only 410 nm compared to typical values of 1500 nm for commonly used epitaxial DBRs based on the Al-GaInAs material system. Fig. 1 depicts an isometric view of the SC-VCSEL structure. Highly compressively strained Al-GaInAs/InGaAs quantum wells yield high (differential) gain and guarantee high relaxation-resonance frequencies being essential to achieve high modulation bandwidths. Small diameter ($< 30 \mu\text{m}$) of the semiconductor mesa, reduced contact-pad areas, and benzocyclobutene spacer layers allow for the reduction of parasitic effects compromising high-speed modulation. For an in detail account on the active region design and the BTJ concept, the reader is referred to [11].

B. Device Performance

Presented results correspond to a typical SC device with a current aperture of $5 \mu\text{m}$ and an effective cavity length of $2.5 \mu\text{m}$. Fig. 2 plots the voltage and output power versus current for different heat-sink temperatures. Threshold currents range from

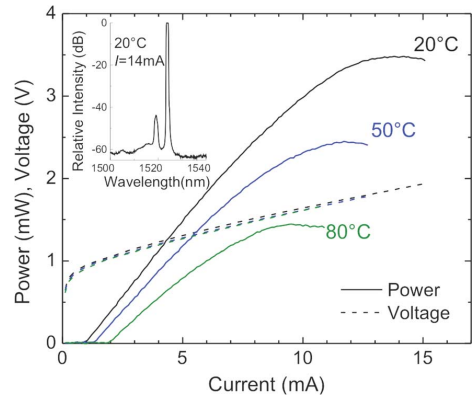


Fig. 2. L - I - V curves of a $5 \mu\text{m}$ SC-VCSEL for 20°C , 50°C , and 80°C heat-sink temperatures.

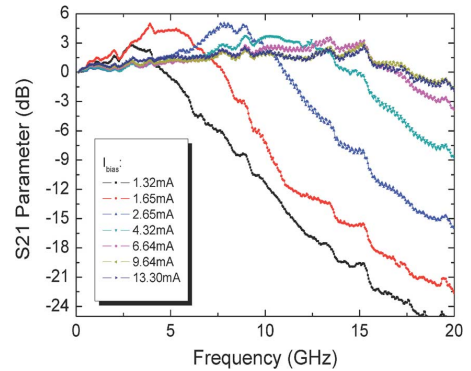


Fig. 3. S21-response for a $5 \mu\text{m}$ device biased at various currents at 20°C .

1.0 mA at 20°C to 1.9 mA at 80°C . Maximum output powers are above 3.5 and 1.4 mW at the respective temperatures. At 20°C , the threshold voltage is only 0.95 V, indicating a voltage drop of less than 150 mV at the heterobarriers for photon energy of 0.8 eV. The inset of Fig. 2 shows the single-mode spectrum of the same device operated at room temperature and roll-over current. The side-mode suppression ratio (SMSR) exceeds 40 dB over the entire current and temperature range.

Fig. 3 plots the small signal modulation response of the same $5 \mu\text{m}$ device for different bias levels at 20°C . Maximum modulation bandwidths exceed 20 GHz. For typical biases applied under large-signal modulation, the relaxation-resonance peak is strongly damped, yielding a flat response as favored by most applications.

Rise and fall times at 20–80% of the devices are 16 and 21 ps, respectively. Measured relative intensity noise is -142 dB/Hz .

III. 4-PAM POLMUX

In order to investigate the ultimate capacity of a VCSEL-based link, multilevel PAM is proposed because of the combination of higher spectral efficiency compared to ON-OFF keying

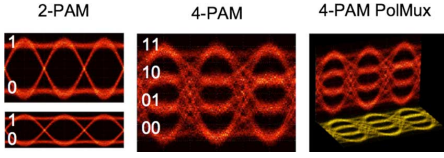


Fig. 4. Eye diagrams for 2-PAM, 4-PAM, and 4-PAM PolMux modulation formats.

(OOK), suitability for direct modulation of VCSELs with full bandwidth exploitation, and simple demodulation. 4-PAM has advantages over OOK of less sensitivity to time jitter and high-frequency noise [13]. Furthermore, two times faster frequency required on OOK usually requires more than double power consumption [13].

CMOS integrated circuits of 4-PAM drivers have been previously demonstrated. Modulation of VCSELs has been demonstrated at 10 Gb/s [14] including 2-taps feedforward equalizer with CMOS 4-PAM drivers. However, CMOS 4-PAM electrical transmitters have reached up to 32 Gb/s with an output swing of 1250 mV [15]. With research equipment, 4-PAM VCSEL modulation up to 30 Gb/s has been presented [16].

Fig. 4 shows a representation of the eye diagram of a 4-PAM PolMux modulation signal used in this study. The 4-PAM signal is the result of adding up two 2-PAM signals, with double amplitude of one respect to the other. In the optical domain, two optical 4-PAM signals are combined with orthogonal polarizations in order to minimize interference on the optical transmission and allowing for independent detection.

IV. FEC

To compensate for transmission impairments, FEC is an efficient solution. Unfortunately, this solution is also rather complex, so various schemes of concatenating simple component codes have been suggested. Furthermore, the performance may be improved by iterative decoding methods. In this paper, we propose two different product codes with shortened Bose–Chaudhuri–Hocqenghem (BCH) component codes and iterative decoding [17]. The resulting product codes have lengths of 1138489 bits and 152881 bits with 7% and 20% overhead, respectively. We choose hard-decision FEC since it has already proved 10 dB net coding gain, and requires less effort than soft-decision FEC for real-time implementation. Fig. 5 shows the code structure for both codes used in the FEC. Both codes are able to correct three errors and detect error patterns of even weight, e.g., patterns with four errors. This detection is included to reduce the risk of making wrong decodings. This risk is further reduced by using BCH codes of original length $2^{11} - 1$ shortened to lengths of 391 and 1067 for the two different overhead values.

As described previously, iterative decoding provides a good performance. The performance as a function of the input bit error rate (BER) may roughly be described as a section where the coding does not improve the performance and then as a rather steep section—as a threshold—where the performance improves drastically down to the so-called error floor where the performance only improves slightly. The overall performance

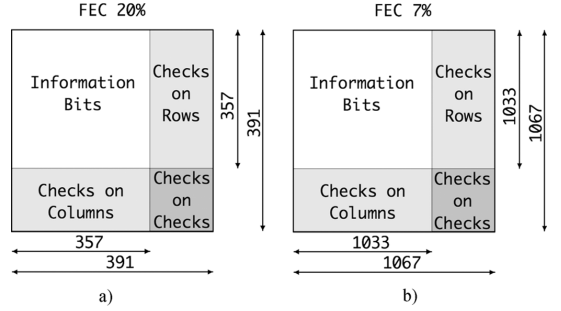


Fig. 5. Product code structures. (a) 20% overhead FEC. (b) 7% overhead FEC.

goal for the presented system is an output BER of 10^{-15} and the codes are chosen such that the error floor may be calculated to be below this number. For a product code, the threshold may be estimated by a method shown in [18] to be 4.8×10^{-3} and 1.3×10^{-2} (aiming at 10^{-15}) for the 7% overhead and 20% overhead codes, respectively.

The codes proposed here are much stronger than the code suggested for IEEE 802.3bj [19] with overhead 2.7%. The suggested code obtains output BER of 10^{-15} at an input error rate at 4.7×10^{-6} .

V. EXPERIMENTAL DEMONSTRATION

In this section, we describe the setup of our experiment to assess the performance of a 100 Gb/s transmission by modulating the VCSEL described in Section II, with the modulation format of Section III and applying the error correction explain in Section IV. Fig. 6 shows the setup of the transmission experiment. The link is analyzed with pseudorandom binary sequences (PRBS) and with both FEC patterns described in Section IV. The PRBS sequence has a pattern length of $2^{11} - 1$. Two uncorrelated 25 Gb/s substrate channels of an SHF 12103 A pulse pattern generator (PPG) are added to form a 50 Gb/s 4-PAM signal. The subchannel addition system is optimized to reduce reflections and improve quality of the electrical signal into the VCSEL. It is composed of a 10 dB and a 3 dB electrical attenuator, and a 6 dB electrical combiner. A high-linearity amplifier from SHF is used to amplify the electrical signal to utilize the linear region of the VCSEL I - P characteristic curve shown in Fig. 2. Time jitter of the electrical signal at the input of the VCSEL is 19 ps. The optimum bias point of the VCSEL was found to be 10 mA, with a driving voltage of 1 V peak to peak. No optical isolator is used on the VCSEL. The optical signal from the VCSEL is launched into a polarization multiplexing (PolMux) system with an optical delay between branches to emulate orthogonal polarization transmission uncorrelated at 100 Gb/s. Polarizations are controlled on the PolMux system to match polarizations of the receiver. The insertion loss of the PolMux system is 5 dB.

The signal is transmitted over 100 m of standard single-mode fiber (SMF-28). On the receiver side, a polarization beam splitter (PBS) separates the two polarizations. The transmission path loss and receiver PBS is 1 dB. Each polarization is detected independently by a 40 GHz photodiode. A Lecroy 30

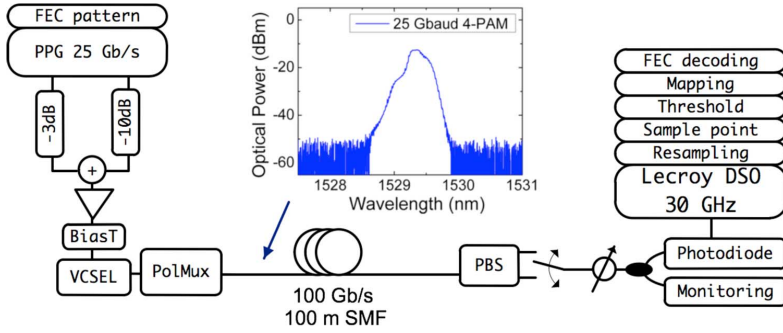


Fig. 6. Experimental setup: forward error correction (FEC), pulse pattern generator (PPG), single-mode fiber (SMF), polarization beam splitter (PBS), digital storage oscilloscope (DSO).

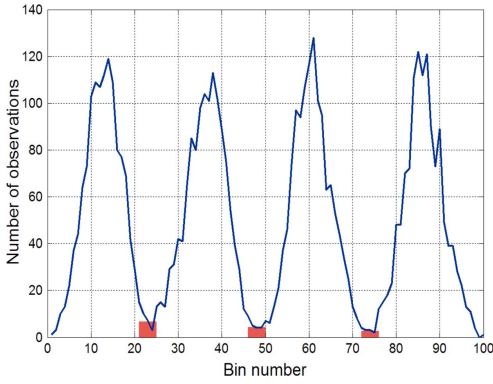


Fig. 7. Histogram in demodulation.

GHz, 80 Gsa/s digital storage oscilloscope (DSO) is used to store the received signal for offline demodulation. The offline signal demodulation includes bit synchronization and adaptive decision threshold gating. Afterward, the offline FEC decoding is performed. The implementation of the decoder is discussed in [17].

VI. RESULTS

Digital upsampling of the signal to an oversampling factor of 10 has been used for better demodulation. Demodulation is done in blocks of 5000 bits, with clock recovery and decision thresholds update every block. Fig. 7 shows the histogram of one block at the optimum sample point of the received signal. The minimums of the histogram are taken as the symbol decision thresholds. The least significant bit (LSB) and most significant bit (MSB) of each symbol are two uncorrelated patterns. After demodulation, error counting of the received LSB and MSB is done independently comparing each bit stream with the corresponding pattern.

Fig. 8(a) shows the BER curve for the MSB after 100 m and back-to-back (B2B) configuration with respect to the received optical modulation amplitude (OMA). Fig. 8(b) shows the BER curves for the LSB. We can observe worst performance in the LSB as it was expected due to its higher error probability on

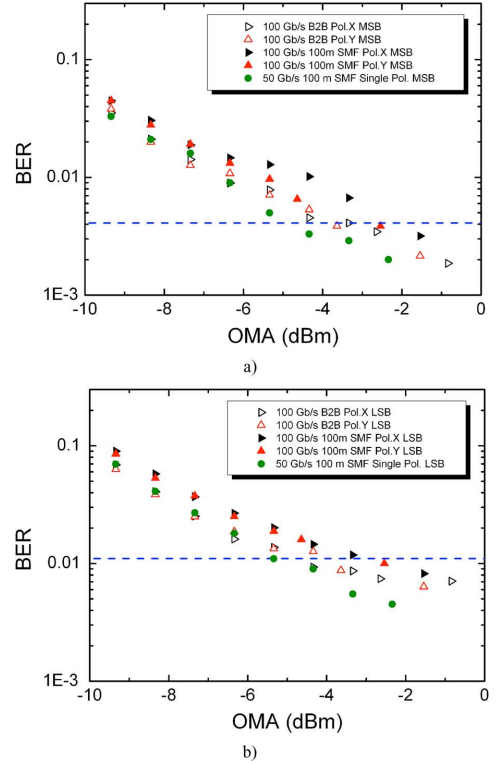


Fig. 8. (a) BER curves for MSB. (b) BER curves for LSB.

the symbol. We have used Gray mapping to facilitate error correction. BER curves for the single polarization transmission are also included in Fig. 8(a) and (b). Penalty of 1 dB on received OMA sensitivity is appreciated compared to dual polarization transmission.

Section IV presents 4.8×10^{-3} and 1.3×10^{-2} as theoretical pre-FEC limit for the 7% overhead and 20% overhead codes, respectively. However, since the decoding of a BCH code sometimes results in a wrong codeword, the theoretical pre-FEC

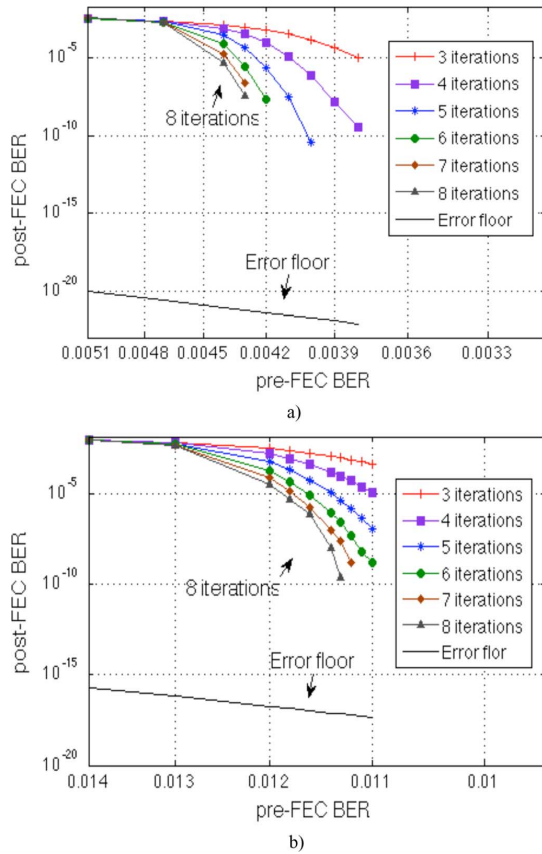


Fig. 9. BER curve simulation. (a) 7% overhead FEC. (b) 20% overhead FEC.

thresholds increase in real implementations. In order to estimate the real pre-FEC error, a simulation of the actual decoding is shown in Fig. 9. Simulating down to 10^{-15} is impossible due to time reasons, but the curves seem to indicate that thresholds of approximately 4.1×10^{-3} and 1.1×10^{-2} , respectively, are achievable. Fig. 8(a) and (b) shows the plot with the estimated real pre-FEC limit. The 7% overhead FEC is applied to the MSB and the 20% overhead FEC is applied to the LSB based on the BER results returned from PRBS sequence tests. Fig. 8(a) and (b) shows with a blue line the FEC thresholds for 7% and 20%, respectively. Transmissions below the threshold can be decoded to an output BER of less than 10^{-15} . By applying different FEC codes to the LSB and the MSB, the received OMA sensitivities for error-free demodulation coincide. We processed 1.6×10^8 bits for the FEC decoding for both channels and got an error-free sequence after the offline demodulation and FEC decoding at -2 dBm received OMA sensitivity. The FEC adapted in this way maximizes the effective bit rate for error-free demodulation. The 7% and 20% overhead of the MSB and the LSM, respectively, result in a total effective bit rate of 86.5 Gb/s. Due to the limited number of FEC frames we can save on the DSO,

we theoretically calculated the error probability in a longer sequence. Based on the theory in [20], as we had zero errors in the experiment after several FEC decoding iterations, we have, with 95% confidence, that the BER of less than 3×10^{-7} is expected in repeated experiments. Since the error floor is less than 10^{-15} , the possible error rate is expected to be smaller especially if more iterations are used, and thus, a virtually error-free demodulation is still expected in a longer time measurement.

VII. CONCLUSION

High-capacity VCSEL transmission has been investigated with multilevel PAM at 50 Gb/s with a total line rate of 100 Gb/s by emulating polarization multiplexing over 100 m SMF.

Error-free demodulation of 1.6×10^8 bits was achieved after FEC with an effective bit rate of 86.5 Gb/s.

The system reduces the number of channels needed to reach an aggregated capacity by increasing bandwidth efficiency and including error correction capability. Scaling by 4 the proposed system, by either spatial or wavelength multiplexing, could be a candidate solution to provide future standard capacity of 400 Gb/s.

Future work will experimentally scale the system with independent sources for orthogonal polarization and channel multiplexing; extend the fiber transmission length and evaluate dispersion effect; and perform reliability test of the VCSEL. Moreover, different combinations of FEC codes could be investigated in order to determine an optimum balance between effective bit rate, computation processing, overhead, and latency.

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Paper [F]: Experimental Performance of FEC for Linear and Nonlinear Optical Fiber Transmissions

Bomin Li, Robert Borkowski, Jose Estaran, Molly Piels, Darko Zibar, Knud J. Larsen and Idelfonso Tafur Monroy. Experimental Performance of FEC for Linear and Nonlinear Optical Fiber Transmissions. Submitted to *IEEE Photonics Technology Letters*.

Experimental Performance of FEC for Linear and Nonlinear Optical Fiber Transmissions

Bomin Li, Robert Borkowski, Jose Estaran, Molly Piels, Darko Zibar, Knud J. Larsen
and Idelfonso Tafur Monroy

Abstract— In this paper we experimentally demonstrated FEC compensation in both linear and nonlinear transmission regimes in a 741 km WDM link. The analysis of the experimental results shows that the performance curve in the experiment does not agree with simulation predictions for an AWGN channel. Today FEC limit is a widely used reference in the system performance evaluation and the referred value is from the simulation results for AWGN channel. The analysis in this paper indicates that to choose an appropriate FEC limit value has to take into considerations the actual transmission channel.

Index Terms—Forward error correction, Metropolitan area networks, Optical fiber communication

I. INTRODUCTION

Terabit and emerging petabit data transmission over optical fibers is being required not only in long haul-links but also in regional and metropolitan area networks. Recently, a high capacity field trial of 54.2 Tb/s for regional distance of 634 km has been reported [1]. Therefore, mitigation of nonlinear optical fiber transmission effects has to be considered for these scenarios too. Nyquist shaping [2] and digital back-propagation [3] have gained a lot of interest to reduce or compensate for dispersion and nonlinear optical fiber propagation impairments. Meanwhile, forward error correction (FEC) is always employed in combination with those techniques to reduce the bit error rate (BER) to a reference value of 10^{-15} .

In this paper, we investigate how FEC itself compensates for performance degradation in both linear and nonlinear transmission regimes in an uncompensated coherent WDM transmission system with a reach sufficient to cover the metro segment of optical networks. Without the use of pulse shaping or pre-compensation of nonlinearities, we demonstrate that for a certain range of optical input power levels, FEC itself can result in desirable BER performance. Furthermore, the detailed experimental analysis shows that, for the purpose of FEC performance analysis, the fiber channel cannot be assumed to be an additive white Gaussian noise (AWGN) channel. Therefore an important discovery of our presented work is that the use of theoretical thresholds for different error correcting

codes, obtained by assumption of an AWGN channel, becomes invalid in nonlinear transmission scenarios.

II. EXPERIMENTAL SETUP

The experimental setup is shown in Fig. 1. The transmitter consisted of 7 WDM channels, spaced 50 GHz apart, shown as an inset. The optical channel under test was a dual polarization (DP) 16-ary quadrature amplitude modulation (16-QAM) signal at 11.1 Gbaud. The neighboring channels (three on both sides) were 11.1 Gbaud DP quaternary phase shift keyed (QPSK) signals, with optical bandwidths similar to the 16-QAM channel. A pre-encoded FEC pattern was loaded into a pulse pattern generator (PPG). The 11.1 Gbaud data output from the PPG and its delayed copy were used as inputs to a 4-bit digital-to-analog converter (DAC) to generate two 4-level pulse amplitude modulated (4-PAM) signals. The 4-PAM signals were amplified and supplied to an optical I/Q modulator, along with an optical continuous wave signal originating from an external cavity laser (ECL) with 100 kHz linewidth, creating a 44.4 Gbit/s optical 16-QAM signal. Polarization multiplexing (PolMux) was emulated by multiplexing the 16-QAM signal with its delayed copy in the orthogonal polarization to obtain a channel with a total bit rate of 88.8 Gbit/s. Fiber transmission was realized over 7 spans of a standard single-mode fiber (SSMF), with each span being approximately 80 km, over a total length of 741 km. The transmission link had no optical dispersion compensation and used erbium-doped fiber amplifiers (EDFAs) for span loss compensation. The input power to each span was varied in the range between -5.5 dBm and 3.5 dBm per channel and peak power of all channels was equalized before transmission. This range was sufficient to observe both the linear regime dominated by amplified spontaneous emission, as well as the nonlinear regime, limited by nonlinear fiber effects. At the receiver side, a standard coherent detection scheme was employed. An external cavity laser (ECL) with a linewidth of 100 kHz was used as a local oscillator (LO). Received analog signals were sampled by a digital sampling oscilloscope (DSO) with 13 GHz analog bandwidth at a rate of 40 GSa/s. Acquired traces were processed offline. Digital signal processing (DSP) included a digital prefiltering, dispersion compensation, polarization demultiplexing, carrier phase recovery and digital demodulation. Hard-decision data were subsequently decoded by the FEC decoder afterwards.

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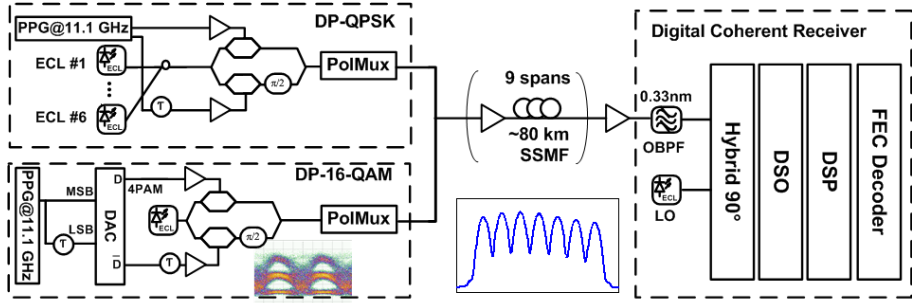


Fig. 1. Experimental setup of 7-channel WDM transmission.

III. PRODUCT CODE

A product code with BCH components was employed in the experiment. The code structure and performance are shown in Fig. 2 and Fig. 3 respectively. This hard decision product code has 511 bits in each dimension as shown in Fig. 2, with a total length of 261,121 bits. Each row and column is a BCH code. It corrects up to 5 errors and detects 6 errors. The code overhead is 20.8%. Fig. 3 is the simulation performance for an AWGN channel. Simulation BER curves after 7 and 9 iterations for AWGN channel are shown in Fig. 2, which shows that the theoretical AWGN pre-FEC BER threshold is around $1.4 \cdot 10^{-2}$, considering 8 iterations in FEC decoding. The error floor is as low as 10^{-43} when calculated using the method explained in [4]. With a reference BER of 10^{-15} , the net coding gain (NCG) is around 10.4 dB.

A pre-encoded product code was transmitted in the optical channel column-wise. A total of 110,454,183 bits was tested for each channel. In Fig. 5, the error distribution is plotted in the format of the code structure shown in Fig. 2. In Fig. 6, the experimental results are compared with the simulation results.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The WDM back-to-back measurement results are plotted in Fig. 4. BER performance is presented as a function of the optical signal-to-noise ratio (OSNR) in dB. The red curve without markers is the theoretical DP-16QAM system performance curve. The black curve with squares represents the

result for BER of DP-16QAM without FEC decoding. The blue curve with triangles represents the BER after the first iteration of FEC decoding and the green curve with diamonds is the result after two iterations. All errors are cleaned after three iterations for OSNR of 17 dB or more.

The BER obtained after transmission over 741 km is shown in Fig. 5 (left). The black curve with squares represents the BER without FEC decoding. The blue curve with triangles is the result after one iterative FEC decoding while the green curve with diamonds is the result after 2 iterations. The green curve in the linear region is not noticeable because there is no measurement between points (a) and (b). In the nonlinear region the measurements between points (c) and (d) return more precise curve. The error distribution matrix and constellation of one of the polarizations are plotted for four selected points, shown in Fig. 5 (right). These four points correspond to per channel input powers of -5.5 dBm, -4.5 dBm, 2.5 dBm and 3.5 dBm. The performance of the other polarization is similar. From that we may conclude that:

- FEC compensates in both linear and nonlinear regimes and the decoding behaviors are similar;
- All measurements between the points (b) and (c) are error-free after 3 iterations, resulting in a BER of less than 10^{-7} with 95 % confidence for the sequence under test [5]. With one or two more iterations, the BER can be expected to brought down further.
- It is not obvious from the curve, but the numerical values show that at the input powers of -5.5 dBm and 3.5 dBm, some errors remain despite of the number of

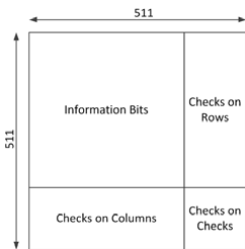


Fig. 2 Product code structure

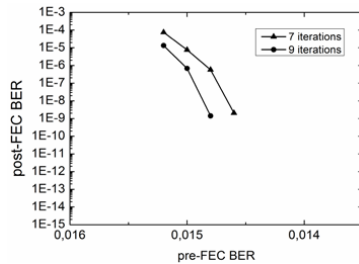


Fig. 3 Product code simulation performance

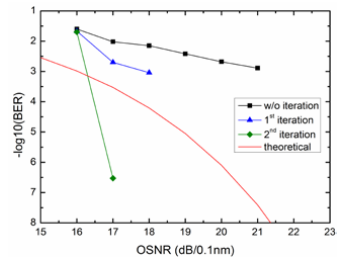


Fig. 4 BER as a function of OSNR for B2B measurement

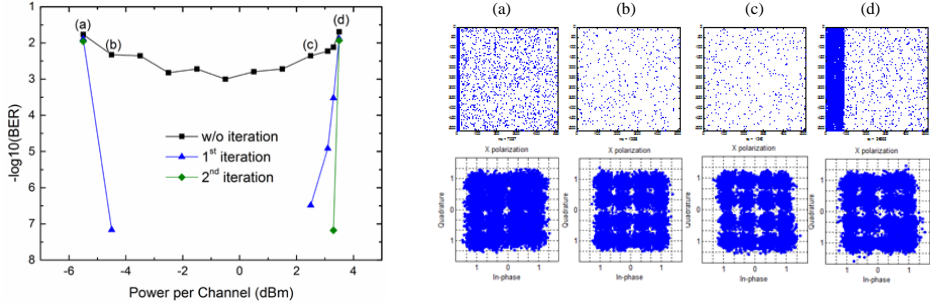


Fig. 5. Left: BER as a function of input power per channel. Right: Error distribution within 511x511 frame (received column-wise) for a random frame and corresponding constellation at input powers of (a) -5.5 dBm, (b) -4.5 dBm, (c) -2.5 dBm, (d) 3.5 dBm.

iterations. The burst-like errors in some columns are suspected to be caused by cycle-slip behavior, which requires further investigation.

To better evaluate the performance, the experimental results are compared with the simulation ones in detail. Fig. 6 is the curve of BER value as the function of the number of iterations. One iteration decodes the product code both row-wise and column-wise once, while half iteration only decodes the product code either row-wise or column-wise. Fig. 6(a) is the comparison results for points (b) and (c) in Fig. 5. The point (b) belongs to the linear regime and point (c) to non-linear. The pre-FEC BERs are $4.7 \cdot 10^{-3}$ and $4.3 \cdot 10^{-3}$ correspondingly. Simulations for AWGN channel are done for these pre-FEC values and the comparisons are shown in Fig. 6. Experimental results are represented by solid curves and simulation results are plotted with dash-dot curves. Red and blue colors indicate points, respectively, from the non-linear and linear regime. Since in the simulation all errors are cleaned after half iteration, the reference value of $4 \cdot 10^{-10}$ is used to plot the curve. This value is a theoretical value with 95% confidence for the number of bits ($2.6 \cdot 10^{11}$) carried out under simulation [5]. The BER value will be lower after more iterations. Notice that the red dash-dot line and blue dotted line overlap in the curve. We clearly observe that the experimental results are worse than the corresponding simulation results for AWGN channel. Fig. 6(b)

is the comparison for points (a) and (d) in Fig. 5. They are in the linear regime and nonlinear regime respectively. Errors corresponding to these two points cannot be mitigated after multiple iterations. The curves are presented in the same way as in Fig. 6(a). Conversely to the analysis of result from Fig. 6(a), for high BER above the theoretical threshold, the experimental results are better than the corresponding simulation results. Therefore:

- The channel under test cannot be regarded as an AWGN channel since the experimental results do not match well the simulation results based on the assumption of AWGN channel.
- Careful consideration of operating conditions of the system (linear/nonlinear regime) is necessary when a theoretical threshold is used as a FEC limit reference.

V. CONCLUSION

We have experimentally demonstrated in a 16-QAM/QPSK WDM metro distance coverage link that FEC can compensate in both linear and nonlinear transmission regimes. The observation of a non-AWGN channel in the experiment indicates that careful analysis of transmission channel is necessary for FEC code selection to reach a certain FEC limit.

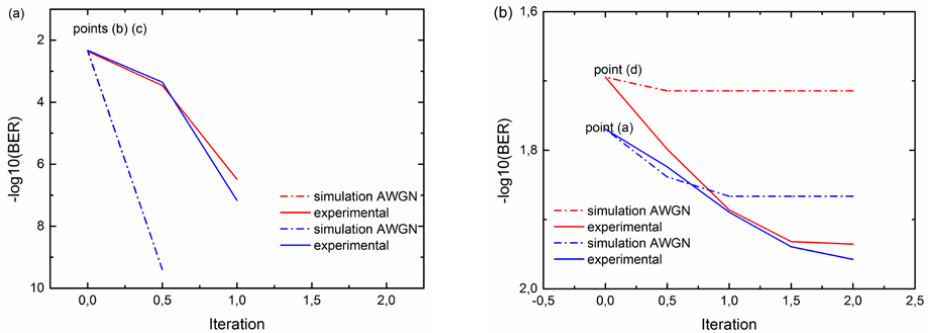


Fig. 6. Comparison of experimental and simulation results (a) BER less than theoretical threshold (b) BER larger than theoretical threshold

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