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Investigation of Transformer Winding Architectures for High Voltage (2.5 kV) Capacitor Charging and Discharging Applications

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Abstract—Transformer parasitics such as leakage inductance and self-capacitance are rarely calculated in advance during the design phase, because of the complexity and huge analytical error margins caused by practical winding implementation issues. Thus, choosing one transformer architecture over another for a given design is usually based on experience, or a trial and error approach. This paper presents analytical expressions for calculating leakage inductance, self-capacitance and ac resistance in transformer winding architectures (TWAs), ranging from the common non-interleaved primary/secondary winding architecture, to an interleaved, sectionalized, and bank winded architecture. The calculated results are evaluated experimentally, and through finite element (FEM) simulations, for a RM8 transformer with a turns ratio of 10. The four TWAs such as, non-interleaved and non-sectioned, non-interleaved and sectioned, interleaved and non-sectioned, and interleaved and sectionalized, for an EF25 transformer with a turns ratio of 20, are investigated and practically implemented. The best TWA for a RM8 transformer in a high-voltage (HV) bidirectional flyback converter, used to drive an electro active polymer based incremental actuator, is identified based on the losses caused by the transformer parasitics. For an EF25 transformer, the best TWA is chosen according to whether electromagnetic interference (EMI) due to the transformer interwinding capacitance, is a major problem or not.

Index Terms— switch-mode power converters, high voltage dc–dc converters, energy efficiency, actuator, transformer parasitics, transformer winding architectures, high voltage transformer

I. INTRODUCTION

Dielectric electro active polymer (DEAP) is an emerging smart material that has experienced significant development and has gained increasing attention over the last decade [1]-[5]. DEAP, when used as actuators, has the potential to be an effective replacement for many conventional actuators due to its unique properties such as, large elastic strain (5-100%), light weight (7 times lighter than steel and copper), high flexibility (100,000 times less stiff than steel), low noise operation, and low power consumption. However, a compact high voltage driver is required to charge and discharge the DEAP from 0 V to 2500 V DC supplied from a 24 V battery. The DEAP actuator applications [6]-[9] require bidirectional high voltage (HV) converters, to charge and discharge the actuators, and to increase the life time of the source, by transferring part of the energy to it. The flyback converter topology is suitable for low power (< 150 W), and high voltage capacitor charging applications, as it can be made very compact with a low number of components [10].

The flyback transformer is the most critical component in the HV driver performance. In Fig. 1, the schematic of the HV flyback converter including the equivalent model of the HV transformer is provided. The high output voltage requirement demands a high turns ratio for the transformer, which calls for a large number of secondary turns. This may lead to a high self-capacitance $C_s$ (in Fig. 1) of the secondary HV winding, resulting in the severe capacitive switching loss, and undesirable, resonating current spikes in the leading edge of the current waveform, which could lead to false triggering of the current limit during the turn-on process [11]. The problem of high self-capacitance in the HV flyback, led early designers in this research area to automatically choose zero current switching (ZCS) primary operation, which gives zero voltage switching (ZVS) in the secondary. Leakage inductance plays a critical role in the HV switched-mode power supply design. The stored energy due to the leakage inductance $L_{lip}$ or $L_{lks}$ (in Fig. 1) of the HV transformer may cause undesirable voltage spikes in the primary and secondary MOSFETs during the charge and discharge processes, respectively, which lead to the use of

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Fig. 1. Schematic of the HV bidirectional flyback converter [7].
active or passive snubber circuits in the converter. Consequently, the leakage inductance creates EMI problems, increases switching losses and reduces energy efficiency. With active snubbers high energy efficiency can be achieved, at the expense of higher cost and added control complexity, whereas the passive snubbers result in switching loss due to the leakage inductance. The ac resistance is also an important parameter to consider, since the ac conduction loss is caused by the high frequency skin and proximity effects, in a flyback converter operating in boundary conduction mode (BCM) or in discontinuous conduction mode (DCM). In order to limit the maximum temperature rise across the transformer, it is necessary to minimize the conduction loss due to the transformer winding resistances. The losses due to the transformer parasitics in the HV flyback converter are explained in [7]. The interwinding capacitance between primary and secondary windings \( C_{\text{int}} \) (in Fig. 1) of the flyback transformer gives an indication of how much common mode noise can be allowed. The interwinding capacitance couples the primary and secondary voltages, greatly reducing the high-frequency ac isolation, and leading to common-mode currents and conducted EMI. In medical applications common-mode noise is especially critical and for some applications, it is necessary to design the HV transformers with lower interwinding capacitances.

Accurate estimation of the transformer parasitics, and their associated losses are required, to evaluate different transformer winding architectures (TWAs), from which the best TWA can be selected, to achieve high energy efficiency. Extensive research has been done for calculating the leakage inductance in conventional transformers [12]-[19]. The capacitance calculation methods have been proposed for inductors, power, planar, and high voltage transformers in [20]-[28]. In [29], [30], the equations for ac resistance calculation are provided. In this paper, the equations to calculate the self-capacitance, leakage inductance and ac resistance for several TWAs are provided.

The influence of transformer parasitics for a low power HV flyback converter has been discussed in [7]. This paper investigates a number of TWAs, to provide a deep insight into transformer design, and its impact on the total loss contribution in a HV bidirectional flyback converter. Two different transformers (with RM8 and EF25 cores), with turns ratios 10 and 20, respectively, are investigated, and practically implemented. The paper is organized as follows: following the introduction, Section II describes the TWAs. Sections III, IV and V provide the calculations of self-capacitance, leakage inductance and ac resistance for different TWAs, respectively. In Section VI, the calculated transformer parasitics are evaluated via FEA simulation using ANSOFT Maxwell. Section VII compares the calculated, simulated, and measured transformer parasitics, for seven different implementations of a RM8 transformer. Section VIII provides the measured transformer parameters, for four different implementations of an EF25 transformer, followed by the conclusions in Section IX.

II. TRANSFORMER WINDING ARCHITECTURES (TWAs)

This paper investigates the four known winding schemes (A, B, C and D) as shown in Fig. 2 [12], [27], [28]. Winding scheme A is the most simple to implement since the next layer starts where the previous layer ended. In winding scheme B, the next layer starts just above the starting point of the previous layer. Winding scheme C split the winding into a number of sections, and each section is individually wounded like winding scheme B. In winding scheme D (bank or progressive winding), the turns progress in a vertical back angled way, where the turns are built on the top of previous turns. It seems like winding scheme D achieves as many angled sections as there are turns in a layer, without the penalty of reducing the fill factor, due to the thickness of the section walls of a sectioned bobbin. The bank winding scheme minimizes the voltage difference between adjacent turns (less inter-turn capacitive energy storage). Another advantage is that, winding scheme D can be easily interleaved, which is not the case for winding scheme C, since it is hard to add section walls in-between windings. The difference in self-capacitance due to the winding schemes is severe [27], [28], because the voltage potentials between the adjacent turns in the winding, and the end-to-end winding voltages are changed.

Several winding buildups (S/P, S/P/S, and S/P/S/P/S/P/S; where S and P are the secondary and primary windings, respectively) are investigated - see Fig. 3. Based on these configurations, seven HV transformer winding architectures \((W_1-W_7)\) are derived and the winding information is summarized in Table I. In order to simplify the implementation of the windings a low turns ratio of 10 is selected. The TWAs \(W_1-W_6\) are wound with 10 primary turns and 100 secondary turns. The TWA \(W_7\) is only implemented with 9 primary turns, due to the nature of the winding architecture. Winding scheme A is employed for the primary winding of all architectures. Moreover, all winding space of the bobbin is utilized to improve the fill factor and to reduce the winding resistance. Equal space allocation for primary (50%) and secondary (50%) winding is adopted for this investigation, thus the primary winding is wounded with a number of parallel wires.

III. SELF-CAPACITANCE

High voltage transformers tend to have a large number of turns in the HV side, which introduces a non-negligible parasitic self-capacitance. It is important to predict the self-capacitance in the design phase in order to avoid severe switching loss, and other problems. The winding self-capacitance is a parameter representing the electric field energy stored in the winding and is considered as a shunt lumped...
Due to large number of turns per layer, the effect of the turn-to-turn capacitance can be neglected, and the main contribution to the self-capacitance comes from the layer-to-layer capacitance, which can be calculated based on the simple parallel-plate or cylindrical capacitor model [12], [27], [28].

The self-capacitance in the transformer windings can be calculated using the electro static energy stored in the volume between the conductors, and is given by

\[ E_{\text{Electric}} = \frac{1}{2} \int_{\text{Vol}} \epsilon E^2 \, dv = \frac{1}{2} C_s U_w^2 \]  

(1)

where \( \epsilon \) is the equivalent dielectric constant of the winding, \( E \) is the electric field strength, \( C_s \) is the self-capacitance, and \( U_w \) is the total voltage across the winding.

Two parallel plate capacitors with a linear potential distribution and a cylindrical capacitor model are shown in Figs. 4a) and 4b), respectively. The energy stored in two adjacent conductive layers [12] with a linear potential distribution, shown in Fig. 4a), is given by

\[ E_{\text{Stored}} = \frac{C_i}{6} \left( U_S^2 + U_T^2 - U_T^2 \right) \]  

(2)

where \( U_S \) and \( U_T \) are the potential difference between the two surfaces at the bottom and top respectively, \( C_i \) is the capacitance between the two surfaces, and is considered as a parallel plate capacitance and is given by

\[ C_i = \varepsilon \varepsilon_0 \frac{h \cdot w}{d_{\text{eff}}} \]  

(3)

![Fig. 4. a) Two parallel plates with a linear potential distribution, b) Cylindrical capacitor model.](image-url)
is the effective distance between two layers (which needs to be calculated for each TWA) and is given by
\[ d_{\text{eff}} = p_{\text{LL}} - 1.15d_a + 0.26p_{\text{TT}} \quad (4) \]

where \( p_{\text{LL}}, d_a \) and \( p_{\text{TT}} \) are the layer to layer pitch, inner diameter, and turn to turn pitch, of the secondary winding, respectively. According to the methods given in [12], the expressions for calculating the self-capacitance for all above mentioned TWAs have been derived and are summarized in Table II. Normally, the cylindrical shape, shown in Fig. 4b), is desired for most winding layers due to the simple winding technique as well as the short mean turn length [27]. If the distance between two layers is much less than the mean diameter for the two layers, the cylindrical capacitor can be considered to be a parallel plate capacitor and (3) can be employed to calculate the capacitance by replacing \( w \) with \( \pi D \) (see Fig. 4b)).

### Table II

<table>
<thead>
<tr>
<th>TWA</th>
<th>Self-capacitance expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_1 )</td>
<td>[ 4 \left( \frac{n_w - 1}{n_0} \right) C_i = \varepsilon_r \varepsilon_0 \frac{b_d l_1}{d_{g1}}; \quad l_{i1} = \pi \left( D + n_d d_a + (n_w - 1)b_w \right) ]</td>
</tr>
<tr>
<td>( W_2 )</td>
<td>[ 4 \left( \frac{n_w - 1}{n_0} \right) C_i = \varepsilon_r \varepsilon_0 \frac{b_d l_1}{d_{g1}}; \quad b_w = (T_w - 1)p_{\text{TT}} + d_a ]</td>
</tr>
<tr>
<td>( W_3 )</td>
<td>[ 4 \left( \frac{n_w - 1}{n_0} \right) C_i = \varepsilon_r \varepsilon_0 \frac{b_d l_1}{d_{g1}}; \quad b_w = (T_w - 1)p_{\text{TT}} + d_a ]</td>
</tr>
<tr>
<td>( W_4 )</td>
<td>[ \varepsilon_r \varepsilon_0 \frac{p_{\text{TT}} l_{i1}}{d_{g1}}; \quad L = (n_w - 1)p_{\text{TT}} + d_a \quad [21] ]</td>
</tr>
<tr>
<td>( W_5 )</td>
<td>[ \varepsilon_r \varepsilon_0 \frac{p_{\text{TT}} l_{i1}}{d_{g1}}; \quad L = (n_w - 1)p_{\text{TT}} + d_a \quad [21] ]</td>
</tr>
</tbody>
</table>

#### Parameters interpretation
- \( \varepsilon_r / \varepsilon_0 \) - relative permittivity of vacuum / dielectric material, and \( \varepsilon_r = 4; \)
- \( b_w \) - the width of the layer;
- \( T_w \) is turns per layer of secondary winding;
- \( D \) - inner diameter of the bobbin;
- \( d_{g1,2,3,4,5} \) - effective thickness of dielectric between two layers [12] [27] for different TWAs;
- \( l_{i1} \) - mean length turn for the TWAs \( W_1, W_2, W_3 \) and \( W_4 \);
- \( l_{i1} / l_{i2} \) - mean length turn between most inner two secondary (\( S_1, S_2 \)) / most outer two secondary (\( S_1, S_2 \)) / most outer secondary and the most inner secondary (\( S_1, S_2 \)) layers for \( W_5 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \); \( \varepsilon_r / \varepsilon_0 \);

#### Table III

<table>
<thead>
<tr>
<th>TWA</th>
<th>Leakage inductance expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_4 )</td>
<td>[ \frac{L_{\text{w}}}{b_w} \left( \frac{n_{w1} h_{w} + (n_{w1} + n_{w2} h_{w})}{6(n_{w1} + n_{w2})} \right) + \frac{n_{w1} + n_{w2} h_{w}}{6(n_{w1} + n_{w2})} ]</td>
</tr>
<tr>
<td>( W_5 )</td>
<td>[ \frac{L_{\text{w}}}{b_w} \left( \frac{n_{w1} h_{w} + (n_{w1} + n_{w2} h_{w})}{6(n_{w1} + n_{w2})} \right) + \frac{n_{w1} + n_{w2} h_{w}}{6(n_{w1} + n_{w2})} ]</td>
</tr>
</tbody>
</table>

#### Parameters interpretation
- \( \mu_r \) - permeability of free air;
- \( l_w \) - mean length turn (MLT) of the winding;
- \( b_w \) - width of the layer;
- \( d_{g1,2,3,4,5} \) - width of the layer excluding the combined width of the sections walls for TWA \( W_5 \); \( d_{g1,2,3,4,5} \); \( d_{g1,2,3,4,5} \);
- For \( W_1, W_2, W_4 \), \( b_w = b_w \); \( b_w \); \( b_w \), \( b_w \) - insulation thickness between primary-to-primary layer / secondary-to-secondary layer / primary-to-secondary layer;
- For \( W_5 \) and \( W_6, n_{w1} \) and \( n_{w2} \) are the number of secondary layers at the top and bottom of a primary winding respectively, having \( n_{w1} \) primary layers;
- For \( W_5 \) and \( W_6, n_{w1} = 2 \) and \( n_{w2} = 2; \)

For remaining variables definitions refer to Tables I and III.
V. AC RESISTANCE

The ac resistance is calculated using equations commonly found in the literature [10], [13], [29]-[30]. The dc resistance of the primary/secondary winding can be calculated by

$$R_{dc} = \frac{\rho}{A} n_{par} A = \frac{\pi d_i^2}{4}$$  \hspace{1cm} (6)

where $\rho$ is the resistivity of copper at room temperature ($\rho = 17.24 \, \text{n}$ at 20 °C), $N$ is the total number of primary/secondary turns, $l_w$ is the mean length turn of the winding, $n_{par}$ is the number of parallel wires, $A$ is the cross sectional area of the winding, and $d_i$ is the inner diameter of the winding excluding the insulation thickness.

The ac resistance per layer of a given winding is given by [30], [36]

$$R_{AC, layer} = \frac{(2m^2 - 2m + 1) \sinh(2Q) + \sin(2Q)}{\cosh(2Q) - \cos(2Q)} - \frac{4(m^2 - m) \sin(Q) \sinh(Q) - \sin(Q) \cosh(Q)}{\cosh(2Q) + \cos(2Q)}$$  \hspace{1cm} (7)

The derivation for (7) is provided in Appendix A. In (7), $R_{DC, layer}$ is the dc resistance per layer of a given winding. The variable $m$ represents the effective number of layers and is given by [10]

$$m = \frac{F(h)}{F(h) - F(0)}$$  \hspace{1cm} (8)

where $F(0)$ and $F(h)$ are the magneto motive forces (MMFs) at the start and end of each layer, respectively. The variable $Q$ is the effective layer thickness normalized with the skin depth, and is given by

$$Q = \frac{\text{layer thickness}}{\text{penetration depth}} = \frac{\pi^{1.5} d_i \sqrt{\frac{d_i T_i}{b_w}}}{\sqrt{\frac{\rho}{\pi \mu_s f}}}$$  \hspace{1cm} (9)

where $d_i$ is the bare wire diameter, $d_i$ is the overall wire diameter including insulation, $T_i$ is the turns per layer of the given winding, and $f$ is the switching frequency.

Assume the variables $\Delta_1, \Delta_2, \Delta_3$, and $\Delta_4$ are assigned as given below,

$$\Delta_1 = \frac{\sinh(2Q) + \sin(2Q)}{\cosh(2Q) - \cos(2Q)}; \quad \Delta_2 = \frac{\sinh(Q) + \sin(Q)}{\cosh(Q) - \cos(Q)}; \quad \Delta_3 = \frac{\cos(Q) \sinh(Q) - \sin(Q) \cosh(Q)}{\cosh(2Q) + \cos(2Q)}; \quad \Delta_4 = \frac{\sin(Q) - \sin(Q)}{\cosh(Q) + \cos(Q)}$$  \hspace{1cm} (10)
The variable $\Delta_i$ in terms of $\Delta_3$ and $\Delta_4$, and $\Delta_2$ and $\Delta_4$ is given by [30]

$$\Delta_i = \frac{1}{2} (\Delta_3 + \Delta_4), \quad \Delta_i = (2\Delta_2 + \Delta_4) \quad (11)$$

Using (10), (11) in (7), the simplified ac resistance per layer is

$$R_{AC, layer} = R_{DC, layer} Q \left\{ \Delta_i + 2 \left( m^2 - m \right) \Delta_i \right\} \quad (12)$$

$$R_{AC, layer} = R_{DC, layer} Q \left\{ \Delta_i + 2 \left( m^2 - 1 \right) \Delta_i \right\} \quad (13)$$

The total ac resistance of $M$ layers for the non-interleaved TWAs $W_i$-$W_4$ is given by

$$R_{AC, total} = R_{DC, layer} Q \left[ \sum_{i=1}^{M} \left\{ \Delta_i + 2 \left( m^2 - m \right) \Delta_i \right\} \right]$$

$$R_{AC, total} = R_{DC, layer} Q \left[ \Delta_i + 2 \left( m^2 - 1 \right) \Delta_i \right] \quad (14)$$

where $R_{DC, total}$ is the total dc resistance of $M$ layers.

To calculate the ac resistance per layer for the interleaved TWAs $W_5$-$W_7$, (12) or (13) needs to be calculated with the corresponding value of $m$ for each layer. The total ac resistance is the sum of all ac resistances in each layer. The total ac resistance referred to the primary is given by

$$R_{AC} = R_{AC, total, P} + \frac{R_{AC, total, S}}{n} \quad (15)$$

where $n$ is the transformer turns ratio, $R_{AC, total, P}$ and $R_{AC, total, S}$ are the total ac resistance of primary and secondary windings, respectively.

In a flyback converter, the primary and secondary currents are 180° out of phase; hence, the conventional equations [29], [30] cannot be used to calculate the ac resistance. The calculation of the total winding loss in a flyback converter [31], [32] using the magneto motive force (MMF) analysis is described in [7].

VI. FINITE ELEMENT ANALYSIS

Different winding architectures ($W_1$-$W_3$) are simulated in Ansoft Maxwell to extract the values of the leakage inductances, self-capacitances and ac resistances. In Fig. 6, the electrostatic energy between the windings is shown for winding schemes B and D. It is noted that the energy density is high between layer to layer, and low between turn to turn as expected in winding scheme B, as shown in Fig. 6a). In winding scheme D, there is a less electrostatic energy between the layers as shown in Fig. 6b), and thus it has a lower self-capacitance.

![Figure 6. Plots from simulation of self-capacitance: a) Energy distribution for winding scheme B; b) Energy distribution for winding scheme D.](image)

Figure 7 shows a close-up of the magneto static energy of the three investigated winding buildups. The leakage flux runs approximately vertically through the windings, and the magneto static energy is highest in the space between the primary and secondary windings. The heavy interleaved buildup (S/P/S/P/S/P/S) has a very low magneto static energy, and thus it will have a very low leakage inductance. The non-interleaved, interleaved, and fully interleaved simulation results are provided in Figs. 7a), 7b), and 7c), respectively. In the non-interleaved buildup, more magneto static energy is stored, between the primary and secondary windings, compared to the interleaved and fully interleaved buildsups. Hence, the non-interleaved buildup will have very high leakage inductance.

The ac resistance at 100 kHz is also simulated for the three winding buildups. A standard mesh which is very fine compared to the skin depth is used to simulate the eddy effects in the winding. A close up plot of the mesh is shown in Fig. 8a).

![Figure 8a. Close-up plot of the mesh.](image)

The diameter of the secondary winding is 0.3 mm and the skin depth at 100 kHz is approximately 0.2 mm. It is noted that the dimensions of the mesh is much lower than the diameter of the winding, and the skin depth at 100 kHz. In Figs. 8b)-8d), a close up of the current density for the three winding buildups is shown. It is noted that the current density in the non-interleaved buildup is much higher compared to the others, and thus the ac resistance will also be higher.

![Figure 8b-8d. Plots showing current density for different winding buildups.](image)

VII. EXPERIMENTAL RESULTS

The measurement setup with 5 of the RM8 transformer prototypes is shown in Fig. 9. The measurement of the transformer parasitics is carried out by the frequency response analyzer PSM1735. The simulated, calculated and measured values [6] of the self-capacitance (measured using the resonance frequency of the impedance plot), leakage
inductance (measured at 10 kHz frequency) and ac resistance (measured at 100 kHz frequency) for the 7 TWAs are shown in the Tables IV, V and VI, respectively. From those tables, it is clear that the measured, calculated and simulated transformer parameters for most of the TWAs closely matches. However, the differences in winding parameters such as an average layer to layer distance and mean length turn may cause errors around ±20%, in cases where the implementation complexity of the TWAs is high.

There are some discrepancies between the simulations, calculations, and measurements of the self-capacitance and leakage inductance of W3, W5, W6, and W7. In self-capacitance calculations, a small change in the mean length turn (MLT) \(l_w\) of the winding and effective distance \(d_{eff}\) between two secondary layers, and the effective permittivity of the dielectric material \(\varepsilon_r\) significantly changes the self-capacitance value. When two dielectrics of different \(\varepsilon_r\) are connected, the equivalent \(\varepsilon_r\) value changes. In leakage inductance calculations, a small difference in the mean length turn (MLT) of the winding, and the effective window width \(b_w\), considerably changes the leakage inductance value.
The discrepancy between the calculation and measurement of the self-capacitance is due to a small increase in the MLT, and a small reduction in effective distance $d_{eff}$, when the winding is practically implemented. Similarly, the discrepancy in the leakage inductance for TWA $W_3$ is due to a decrease in the value of the effective window width, due to the sectioned bobbin. For TWA $W_3$ (interleaved and Z-type), the difference between the simulation and calculation (or measurement) of the self-capacitance could be due to a change in the value of effective permittivity $\varepsilon_r$, which might not be considered during the Maxwell simulations of that particular TWA.

The TWA $W_6$ (interleaved and bank winded) was extremely difficult to implement in the laboratory. The difference between the calculation and measurement of the self-capacitance is due to an increase in the MLT (due to interleaving), when the winding is practically implemented. Similarly, the discrepancy in the leakage inductance for TWA $W_6$, could be due to an increase in the MLT of the winding. For TWA $W_7$ (fully interleaved) the discrepancies between the calculation and measurement of the self-capacitance and leakage inductances are due to an increase in the MLT of the winding, due to heavy interleaving.

A plot of the loss distribution of the energy losses caused by the transformer parasitics, in a bidirectional flyback converter, used for charging and discharging an incremental DEAP actuator [6] is shown in Fig. 10. The winding loss calculation for the flyback transformer is different from that of normal transformer, since the primary and secondary currents are out of phase, in [7] the winding loss is calculated for a flyback transformer with a non-interleaved structure. The same method can be used for the interleaved structures as well.

The calculated transformer parasitics values are used for calculating all losses, in order to provide a fair and useful comparison of the losses. The following specifications are used to calculate the losses in the bidirectional flyback converter [33]: input voltage: 24 V, output voltage: 1500 V, load capacitance: 200 nF, switching frequency during the charging and discharging process: 20-200 kHz, and 26 kHz, respectively, and primary peak current during charge and discharge processes: 2.12 A. The primary magnetizing inductance: 35 $\mu$H. From Fig. 10, it is clear that $W_6$ has the lowest loss among all TWAs followed by $W_4$, $W_7$ and $W_3$. Thus, the structure $W_6$ is highly recommended for high voltage capacitor charging application. In the leakage inductance calculations, the high
VIII. INVESTIGATION USING AN EF25 CORE

A. Practical implementation:

The TWAs investigated in the above sections using RM8 core are not suitable for generating the maximum voltage of 2.5 kV, which is needed to drive the DEAP actuators. Hence, it is needed to investigate the parameters of the transformer further with a higher turns ratio (e.g., n=20). From Section VII, the interesting TWAs for the mentioned actuator application are W3, W4, and W5. When the secondary turns are very high, implementing the TWAs with bank winding scheme (W4 and W5) in the laboratory was extremely difficult, and hence W3 was considered. Table VII provides the details of transformer design using EF25 core [35].

In addition, four different TWAs such as non-interleaved and non-sectioned (W1), interleaved and non-sectioned (W3), non-interleaved and sectioned (W5), and interleaved and sectioned (W8, which is a new TWA) have been practically implemented, using an EF25 transformer. The measured parameters of the transformer for each TWA are provided in Tables VIII, IX, X, and XI, respectively.

### TABLE VII

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Number of primary / secondary turns</td>
<td>18 / 360</td>
</tr>
<tr>
<td>Diameter of primary / secondary winding</td>
<td>0.4 mm (TEX [34]) / 0.14 mm</td>
</tr>
<tr>
<td>Number of layers of primary / secondary winding</td>
<td>3 / 4</td>
</tr>
<tr>
<td>Number of parallel wires of primary / secondary</td>
<td>3 / 4</td>
</tr>
<tr>
<td>Type of core / material</td>
<td>EF25 / N87</td>
</tr>
</tbody>
</table>

By comparing the transformer parasitics of all TWAs with an EF25 core, the non-interleaved and sectioned TWA (W3) has the lowest self and interwinding capacitances, followed by the interleaved and sectioned TWA (W8). The self-capacitances of TWAs W8 and W3 are comparable. However, the leakage inductance of W8 is approximately half of W3, due to very high frequency effects are not considered, because 200 kHz is still a low frequency, and the skin effect will not affect the leakage inductance below 200 kHz.

Figure 10. Energy loss distribution of the losses caused by transformer parasitics in the high voltage capacitor charging application.

### TABLE VIII

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance of primary / secondary</td>
<td>53 μH / 23 mH</td>
</tr>
<tr>
<td>Leakage inductance referred to primary / secondary</td>
<td>1.2 μH / 490 μH</td>
</tr>
<tr>
<td>DC resistance of primary / secondary winding</td>
<td>42 mΩ / 16 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 50 kHz</td>
<td>98 mΩ / 39 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 100 kHz</td>
<td>130 mΩ / 52 Ω</td>
</tr>
<tr>
<td>Self-capacitance of the high voltage winding</td>
<td>42 pF</td>
</tr>
<tr>
<td>Interwinding capacitance</td>
<td>59 pF</td>
</tr>
</tbody>
</table>

### TABLE IX

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance of primary / secondary</td>
<td>47 μH / 20 mH</td>
</tr>
<tr>
<td>Leakage inductance referred to primary / secondary</td>
<td>590 nH / 236 μH</td>
</tr>
<tr>
<td>DC resistance of primary / secondary winding</td>
<td>43 mΩ / 19 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 50 kHz</td>
<td>98 mΩ / 38 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 100 kHz</td>
<td>108 mΩ / 43 Ω</td>
</tr>
<tr>
<td>Self-capacitance of the high voltage winding</td>
<td>21.5 pF</td>
</tr>
<tr>
<td>Interwinding capacitance</td>
<td>160 pF</td>
</tr>
</tbody>
</table>

### TABLE X

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance of primary / secondary</td>
<td>49 μH / 21 mH</td>
</tr>
<tr>
<td>Leakage inductance referred to primary / secondary</td>
<td>1 μH / 357 μH</td>
</tr>
<tr>
<td>DC resistance of primary / secondary winding</td>
<td>39 mΩ / 14 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 50 kHz</td>
<td>91 mΩ / 38 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 100 kHz</td>
<td>117 mΩ / 43 Ω</td>
</tr>
<tr>
<td>Self-capacitance of the high voltage winding</td>
<td>4.3 pF</td>
</tr>
<tr>
<td>Interwinding capacitance</td>
<td>44 pF</td>
</tr>
</tbody>
</table>

### TABLE XI

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance of primary / secondary</td>
<td>49 μH / 21.5 mH</td>
</tr>
<tr>
<td>Leakage inductance referred to primary / secondary</td>
<td>420 nH / 175 μH</td>
</tr>
<tr>
<td>DC resistance of primary / secondary winding</td>
<td>43 mΩ / 19 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 50 kHz</td>
<td>90 mΩ / 39 Ω</td>
</tr>
<tr>
<td>AC resistance referred to primary / secondary winding at 100 kHz</td>
<td>100 mΩ / 43 Ω</td>
</tr>
<tr>
<td>Self-capacitance of the high voltage winding</td>
<td>6.8 pF</td>
</tr>
<tr>
<td>Interwinding capacitance</td>
<td>150 pF</td>
</tr>
</tbody>
</table>
interwinding capacitance, making it unsuitable for high voltage capacitor charge and discharge applications where conducted and radiated EMI are critical. From the above observations, it can be concluded that redesigning the transformer to reduce the interwinding capacitance, usually leads to increased leakage inductance. In other words, interleaving the transformer reduces the leakage inductance and increases the interwinding capacitance.

B. Discussion:

If it is not possible to progressively wind the secondary winding in high turns ratio transformers, it is better to always section the bobbin for end-to-end winding voltages greater than around 250 VRMS which ensures safety and reliability. Furthermore, the maximum voltage rating of the wire insulation should not be exceeded. Almost all transformers in medical applications, have a Farady shield (not a continuous metal layer around the core, it has gap between the ends) between the primary layer(s) and the secondary. This will minimize the common-mode capacitance and help EMI as well. Common mode capacitive coupling is seen and measured during Hi-pot AC testing of the transformer [37].

IX. Conclusions

The analytical equations for calculating the transformer ac resistance, leakage inductance and self-capacitance for seven different winding architectures have been presented. The calculated parasitics for a RM8 transformer, with a turns ratio of 10, are evaluated experimentally, and with FEA simulations. The main contribution to the errors in the comparison, is due to practical winding issues which are not accounted for in the equations. The flyback transformer energy loss distribution is based on the calculated values, and it clearly shows that the TWAs where the self-capacitance is lowest are particularly suitable for high voltage charging applications. Another investigation has been made with an EF25 transformer having a turns ratio of 20. For applications where EMI is not a big problem, interleaved and sectioned TWA is the best TWA, since it has lower leakage inductance compared to the non-interleaved and sectioned TWA. Nevertheless, non-interleaved and sectioned TWA could be most suitable for HV capacitor charge and discharge applications for applications (e.g., medical) where EMI is a major problem.

APPENDIX A

To find the power dissipation in a winding layer, the current density distribution with in a layer is integrated. The current density is obtained by solving the Maxwell’s equations [31]. Integrating it gives the total copper loss \( P \) in layer, and is given by [10],

\[
P = R_{DC,layer} \frac{Q}{I_l} \left\{ (F^2(h) + F^2(0))A_1 - 4F(h)F(0)A_2 \right\} \quad (A1)
\]

Refer to Section V, for the definition of all variables in (A1). If \( F(0) \) and \( F(h) \) are the magneto motive forces (MMFs) at the start and end of each layer, respectively. If \( I \) is the current flowing through the winding, then,

\[
F(h) - F(0) = T_I \quad (A2)
\]

\[
F(h) \text{ can be rewritten in terms of } m \text{ as} \quad F(h) = mT_I \quad (A3)
\]

From (A2) and (A3),

\[
\frac{F(0)}{F(h)} = \frac{m-1}{m} \quad (A4)
\]

The power loss \( P \) becomes

\[
P = R_{DC,layer} \frac{Q}{I_l} F^2(h) \left\{ \left(1 + \frac{F^2(0)}{F^2(h)}\right)A_1 - 4\frac{F(0)}{F(h)}A_2 \right\} \quad (A5)
\]

By using (A3) in (A5), the total power loss \( P \) is

\[
P = R_{DC,layer} Q \cdot I^2 \left\{ (2m^2 - 2m + 1)A_1 - 4m(m-1)A_2 \right\} \quad (A6)
\]

If \( R_{AC,layer} \) is the effective or ac resistance in a given layer, then (A6) can be re-written as,

\[
R_{AC,layer} \cdot I^2 = R_{DC,layer} Q \cdot I^2 \left\{ (2m^2 - 2m + 1)A_1 - 4m(m-1)A_2 \right\} \quad (A7)
\]

The ac resistance in a given winding layer is given by,

\[
R_{AC,layer} = R_{DC,layer} Q \left\{ (2m^2 - 2m + 1)A_1 - 4m(m-1)A_2 \right\} \quad (A8)
\]

REFERENCES


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