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Modeling of Schottky Barrier Diode Millimeter-Wave Multipliers at Cryogenic Temperatures

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Abstract— We report on the evaluation of Schottky barrier diode GaAs multipliers at cryogenic temperatures. A GaAs Schottky barrier diode model is developed for theoretical estimation of doubler performance. The model is used to predict efficiency of doublers from room to cryogenic temperatures. The theoretical estimation is verified experimentally using a 78 GHz doubler cooled down to 14 K. The observed efficiency improvement due to cooling is approximately 4 % per 100 degrees.

Keywords— cryogenic temperature; frequency multiplier; GaAs diodes; millimeter wave; varactor.

I. INTRODUCTION

Varactor frequency multipliers are often used as solid-state sources of millimeter and submillimeter wave radiation in dynamic nuclear polarization systems [1]. The efficiency of polarization in such systems depends on power of electromagnetic radiation delivered to the sample. Traditionally, this power is delivered from sources using long wave-guiding structures, which loss and price scales with operating frequency. Alternatively, the multiplier can be placed close to the sample inside the polarization system, where the temperature of the environment is in the range from 77 to 100 K. Usually, the performance of commercially available multipliers are not specified at such temperatures. The application, however, calls for theoretical and practical evaluation of the multiplier behavior in cryogenic environment. This work investigates the efficiency of Schottky barrier diode GaAs multipliers in the range of temperatures from 14 K to 300 K. First, a model of the diode is developed. The model is then used to predict multiplier efficiency using harmonic balance analysis. The obtained data is compared with experimental results taken from the literature.

Compact diode models are available in most RF and microwave CAD software packages. Such diode models are generic, representing mainly the physical behavior of Silicon pn-junction diodes. Embedded with parasitic networks these diode models can also be used to describe the performance of room temperature Schottky barrier diode multipliers and mixers operating at frequencies up to several hundreds of GHz [2]. The temperature dependence of a pn-junction diode, however, is quite different from that of a Schottky barrier diode due to the different carrier transport mechanisms involved [3]. The physical based Schottky barrier diode model recently developed at the Technical University of Denmark and Goethe University of Frankfurt am Main [4] should in principle be able to predict the temperature behavior at cryogenic temperatures. The physical diode model, however, requires detailed knowledge about the technology used to fabricate the device. Typically, such detailed knowledge is unavailable to circuit designers and models must be based on a few parameters extracted from measured I-V and C-V characteristics on fabricated devices.

The following Section of the paper is dedicated to the development of an electro-thermal diode model, which allows the prediction of the performance of GaAs schottky barrier diode multipliers even at cryogenic temperatures. A simulation setup to test the performance of doublers at cryogenic temperatures is discussed in Section III. The results of the analysis are compared with the measured data for a millimeter-wave doubler in Section IV.
in the device is related to the dissipated power \( p(t) \) by an equivalent first-order network in the thermal model. The thermal resistance is taken independent of temperature despite the well-known dependence of the thermal conductivity of GaAs on temperature. This is done for better convergence during circuit simulations.

The temperature dependent I-V characteristic of a Schottky barrier diode is given by \([5]\)

\[
I_d(V_d, T_d) = AR^* \theta(T_d) \exp \left( -\frac{q \phi_b}{k_b \theta(T_d)} \right) \exp \left( \frac{q V_d}{k_b \theta(T_d)} - 1 \right) \tag{1}
\]

where \( A \) is the anode area, \( R^* \) is the modified Richardson’s constant, \( T_d \) is the absolute temperature, \( \phi_b \) is the barrier height, \( q \) the electron charge, and \( k_b \) is Boltzmann’s constant. The temperature dependence is contained in the so-called slope parameter:

\[
\theta(T_d) = \theta_j \coth \left( \frac{\theta_j}{T_d} \right) \tag{2}
\]

with

\[
\theta_j = \alpha \frac{q \hbar}{k_b} \sqrt{\frac{N_d}{4e \varepsilon_s m^*}} \tag{3}
\]

where \( \hbar \) is Plank’s constant divided by \( 2\pi \), \( N_d \) is the doping of the epi-layer, \( \varepsilon_s \) is the permittivity of the semiconductor, and \( m^* \) is the effective mass of electrons in the conduction band. Physically, the I-V characteristic described by equations (1), (2) and (3) connects the limiting cases of current transport at very low temperatures where tunneling through the barrier dominates, with thermionic emission that dominates at temperatures above approximately 100 K \([6]\). The slope parameter is introduced in a way as to take into account of contributions from transport mechanisms other than thermionic emission also at higher temperatures. It is interesting to note that for a given semiconductor material, the only two unknown parameters determining the temperature dependence of the I-V characteristic are the barrier height and doping of the epi-layer. The leading factor, \( \alpha \), in equation (3), however, models an effective epilayer doping which is experimentally observed to be higher than the nominal \( N_d \) \([6]\). The representation of (1) as implemented in the SDD model is

\[
I_d(V_d, T_d) = I_s(T_d) \left( \exp \left( \frac{q V_d}{\eta(T_d) k_b T_d} \right) - 1 \right) \tag{4}
\]

where the saturation current \( I_s \) and ideality factor \( \eta \) have been introduced. The temperature dependence of the saturation current is evaluated as:

\[
I_s(T_d) = I_s(T_{\text{nom}}) \left( \frac{\theta(T_d)}{\theta(T_{\text{nom}})} \right)^\eta \left( \frac{q \phi_b}{k_b \theta(T_{\text{nom}})} - \frac{1}{\theta(T_d)} \right) \tag{5}
\]

with \( I_s(T_{\text{nom}}) \) representing the saturation current extracted from the measured I-V characteristic at the nominal temperature \( T_{\text{nom}} \). Similar the temperature dependent ideality factor is evaluated as:

\[
\eta(T_d) = \eta(T_{\text{nom}}) \frac{\theta(T_d)}{\theta(T_{\text{nom}})} \tag{6}
\]

The depletion capacitance of the Schottky barrier diode is modeled as \([3]\)

\[
C_j(V_d, T_d) = \frac{C_{jo}}{1 - \frac{V_d}{V_{bi}(T_d) - k_b T_d/q}} \tag{7}
\]

where \( C_{jo} \) is the zero bias junction capacitance extracted from C-V measurements and \( V_{bi} \) is the built-in potential. The built-in potential is related to the barrier height and epi-layer doping through \([3]\)

\[
V_{bi}(T_d) = \phi_b - \frac{k_b T_d/q}{N_s} \left( \frac{N_s}{N_d} \right) \tag{8}
\]

where \( N_s \) is the effective density of states in the conduction band of GaAs. The singularity at high forward bias in (7) is avoided by a linear extrapolation of the depletion capacitance above the voltage \( F_c V_d \) where \( F_c \) is a factor between 0 and 1.

The series resistance \( R_s \) of the Schottky barrier model contains three contributions; the resistance of the undepleted part of the epi-layer, the spreading resistance of the heavily doped substrate layer and the contact resistance. It is assumed that only the epi-layer resistance varies with temperature. In the developed SDD model the total series resistance is partitioned into two parts by using the parameter \( X \) according to \([7]\)

\[
R_s(T_d) = X R_s(T_{\text{nom}}) \left( \frac{T_d}{T_{\text{nom}}} \right)^{0.89} + (1 - X) R_s(T_{\text{nom}}) \tag{9}
\]

where the temperature dependence of the epi-layer resistance is due to the temperature dependence of the low-field mobility of moderate doped n-type GaAs. The resistance \( R_s(T_{\text{nom}}) \) in (9)
is in general bias dependent but typically a fixed value extracted at a moderate to high forward bias can be used with acceptable results.

To illustrate the temperature dependence predicted by the developed model, the I-V characteristics for a triple anode stack are simulated at 77 K and at 300 K, see Fig. 2. The Schottky barrier diodes are assumed to be similar to the diodes from Virginia Diodes Inc. used in the millimeter-wave multiplier discussed later. The measured I-V characteristic at 300 K is available for the triple anode stack. Using a few model parameters \((I_s, \eta, R_s, C_{jo})\) extracted at 300 K it is first verified, as shown in Fig. 2, that our developed SDD model predicts the measured characteristic at 300 K. To predict the performance at cryogenic temperatures, representative values for the remaining model parameters are assumed. From the I-V characteristic at 77 K it is seen that the current level for a given voltage is lower and the slope is steeper than at 300 K in accordance with observations found in the literature [5]-[6].

![I-V characteristics of three anode stack at 300K and 77K. The measured data are shown as symbols. The assumed model parameters are: \(I_s=1.8e-13 \text{ A}, \eta=3.17, R_s=6.0 \Omega, X_n=0.6, C_{jo}=26fF, F_c=0.9, V_d=0.96\) V, \(N_d=1e17 \text{ cm}^{-3}, T_{nom}=300 \text{ K}, R_{th}=500 \text{ K/W}, C_{th}=1e-6 \text{ J/K}, \epsilon_s=13.1\times8.85e-12 \text{ F/m}, \alpha=2.2, m^*=0.068\times9.1e-31 \text{ kg}, N_c=4.37e17 \text{ cm}^{-3}.)

\[ \text{III. DOUBLER CIRCUIT} \]

The model described above is used to evaluate the performance of doublers based on anti-series balanced topology (refer to Fig. 3). The advantage of the anti-series balanced configuration is suppression of odd order harmonics, while the amplitude of the second harmonic is double as high as for the case of an unbalanced single diode doubler. Three diodes are connected in series in each branch in order to enhance the power handling capability. Such an arrangement of diodes is equivalent to a single Schottky diode having triple as high reverse breakdown voltage. In anti-series configuration, diode arrays are fed out-of-phase by an input power source through a balancing transformer \(T_1\). Turn ratio of the transformer is equal to 1. A DC voltage source \(V_d\) is used to bias the diodes. DC blocking capacitors \(C_{cl}\) are placed at the output of the transformer to prevent DC current flowing into the transformer.

DC feeding inductors, \(L_{cl}\), are used to isolate RF signal from DC voltage source and provide DC ground. The generator and load impedances \((Z_g\) and \(Z_L\) respectively) are frequency dependent and chosen to maximize doubler efficiency. \(Z_g\) is conjugate matched to the input impedance of the doubler at frequency of the input signal, and represents a short circuit at 2nd harmonic. The load impedance \(Z_L\), on the other hand, is conjugate matched at the 2nd harmonic of the input signal, and represents a short circuit at the frequency of the input signal. In this analysis, the losses in the matching circuits are neglected. The diodes are reverse biased with negative \(V_d\), which is chosen to maximize efficiency at an input power of 207 mW.

![Fig. 3. Schematic of the circuit setup for harmonic balance simulation of frequency doublers in an anti-series configuration of diode array.]

\[ \text{IV. MODEL VERIFICATION AGAINST MEASURED DATA} \]

The model developed in Section II has been used to evaluate the behavior of a 78 GHz doubler described in [8]. This allows to test the model all the way down to 14 K. The harmonic-balance analysis is applied to the circuit in Fig. 3 to theoretically estimate doubler efficiency at fixed input power of about 207 mW and frequency of interest 78 GHz. The graph in Fig. 4 shows estimated and measured efficiency versus temperature of the 78 GHz doubler.

![Fig. 4. Estimated and measured efficiency versus temperature of the 78 GHz doubler. The measured data is extracted from [8].]
As observed in Fig. 4, the overall behavior of the doubler is well predicted as the measured efficiency values are typically only 1-2 % lower than the estimated ones. It is observed that the predicted efficiency can be greater than 60 % at 14 K temperature, which is comparable with the experimental result of 59 % at the same temperature value. The minor discrepancy between estimated and measured results can partially be explained by the neglected losses in the matching circuit.

The developed Schottky barrier diode model allows us to investigate the reason for the larger multiplier efficiency at cryogenic temperatures by detailed simulations. For high efficiency millimeter-wave multipliers, the Schottky barrier diodes operate in varactor mode. It is thus mainly the non-linear behavior of the C-V characteristic that determines the efficiency of the multiplier. The non-linear C-V characteristic, however, is found to vary little with temperature and can alone not explain the increase in efficiency at cryogenic temperatures. The main reason for the increased efficiency at lower temperature is found to be the increased maximum current of the varactor, when the doubler becomes cold. The maximum current is related to the resistance of the epi-layer which drops to a low value at cryogenic temperatures. Interestingly, the temperature dependence of the velocity saturation effect as described in [6] is shown to be of less importance for the considered millimeter-wave frequency doubler.

CONCLUSIONS

In this work, we have developed and evaluated a Schottky barrier diode model. The model was used to estimate the efficiency of a VDI doubler at 78 GHz at cryogenic temperatures.

The excellent agreement with measured results shows that the model is suitable for predicting performance of millimeter-wave multipliers at temperatures down to 14 K, and, probably, below.

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