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**Knott, Arnold; Ploug, Rasmus Overgaard**

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# Minimizing Crosstalk in Self Oscillating Switch Mode Audio Power Amplifiers

Rasmus Overgaard Ploug<sup>1</sup> and Arnold Knott<sup>1</sup>

<sup>1</sup>Technical University of Denmark – DTU, Kongens Lyngby, 2800 Denmark

Correspondence should be addressed to Rasmus Overgaard Ploug (rop1oug@gmail.com)

## ABSTRACT

The varying switching frequencies of self oscillating switch mode audio amplifiers have been known to cause interchannel intermodulation disturbances in multi channel configurations. This crosstalk phenomenon has a negative impact on the audio performance. The goal of this paper is to present a method to minimize this phenomenon by improving the integrity of the various power distribution systems of the amplifier. The method is then applied to an amplifier built for this investigation. The results show that the crosstalk is suppressed with 30 dB, but is not entirely eliminated by the implementation presented. Future work could include further refinement of the implementation of the concepts, electromagnetic interference investigations or PCB design.

## 1. INTRODUCTION

Traditionally the Pulse Width Modulation (PWM) of the audio input signal in a class D amplifier is made by comparing the audio signal with a higher frequency triangle wave. However, a lot of work has been done in investigating other methods to modulate the audio signal. Especially the field of self oscillating PWM generators has undergone a lot of research (e.g. by [1], [2] and [3]). This

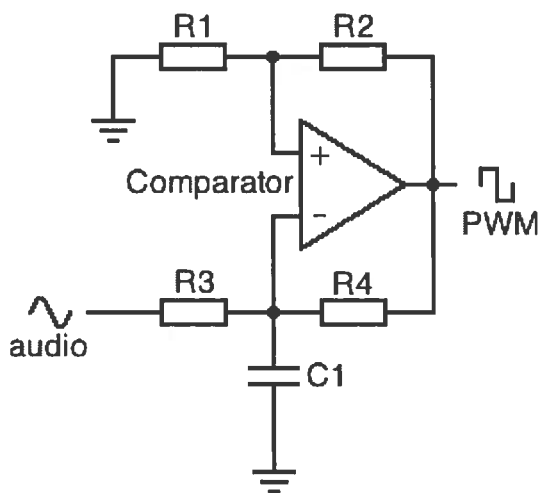


Fig. 1: Self oscillating PWM generator

paper will concentrate on an amplifier made using a self oscillating Astable Integrating Modulator (AIM) which is a hysteretic comparator oscillating to create a PWM approximation (thoroughly explained by [1]). The AIM can be obtained with a very low component cost of only 1 active and 5 passive components making it a very cost effective and low power demanding PWM generator. The circuit can be seen in figure 1. It is a hysteretic modulator where the hysteresis window is determined by R1 and R2, and the carrier signal, which is to be compared, is determined by the capacitor which is charged/discharged through R3 and R4.

### 1.1. Crosstalk

One of the side effects of the AIM is that the switch frequency varies according to the modulation index  $M$  from the 'idle' switching frequency,  $M = 0$ , to a theoretically 0 Hz frequency when  $M$  approaches 1 [1]. This means that when a multi channel amplifier is driven by different audio signals, the frequencies of each channel will vary compared with each other. In addition to this, outer factors like component tolerances make it impossible to run each channel at exactly the same frequency.

These differences in switching frequency can take place in the audible spectrum, and can, as such, be subject to an intermodulation crosstalk appearing as beat tones which degrades the overall audio performance [4].

Intermodulation occurs in systems with two or more fre-

quencies forming additional signals at the sum and the difference between the original signals. E.g. if two signals of frequency  $f_a$  and  $f_b$  appear in the same system, they will intermodulate and signals will appear at frequencies

$$k_a f_a \pm k_b f_b \quad (1)$$

where  $k_a, k_b \in \mathbb{Z}$ . The order of intermodulation  $O$  is given by  $O = |k_a| + |k_b|$  [5].

The term 'crosstalk' is used in the audio field for denoting any type of signal leaking from one signal path to the other. In audio engineering this is typically expressed as a ratio of a signal amplitude leaking from a driven to an undriven channel either linear or nonlinear [6]. However, as implied in this section, the crosstalk of interest in this project, is the crosstalk caused by intermodulation of the switching frequencies in a multi channel switch mode audio amplifier.

The subject has earlier been investigated in a stereo self oscillating switch mode audio power amplifier [4] which, to summarize, concluded that crosstalk indeed was related to the differences in switching frequencies, the filter has an impact on the amount of crosstalk and crosstalk is present even if the amplifier is reduced to only the PWM generating circuits. The amount of crosstalk varied from the millivolt to the microvolt area dependent on how many stages of the amplifier was applied in the test.

## 2. POWER DISTRIBUTION SYSTEM

The emphasis of this paper is based on the hypothesis that the main crosstalk couplings in the amplifier are galvanic and provided by the power supply lines to the various voltage demands in the amplifier design. By lowering the frequency dependent impedance of the power distribution systems (PDS), one would minimize power supply ripples generated by the AC current draw from the very broad spectrum of a pulse width modulated audio signal.

The area of lowering frequency dependent impedance of a PDS, is already refined towards high speed CMOS circuits which demand a very stable supply voltage as the operating voltage has decreased over the years [7]. Concepts from this field of engineering will be applied to the self oscillating switch mode audio amplifier built for this investigation, in order to minimize the crosstalk phenomenon.

### 2.1. Non-ideal Components

In order to model and understand the behaviour and response of a power distribution system the equivalent cir-

cuits for a conductor and a capacitor are declared as in figure 2 and 3.



Fig. 2: Equivalent circuit – conductor

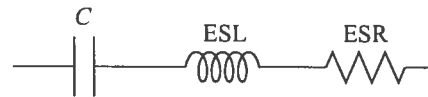


Fig. 3: Equivalent circuit – capacitor

### 2.2. Modeling a PDS

The behaviour of a general power distribution system for a circuit with a switching element can be approximated by a model with a DC voltage source in parallel with an AC current sink which simulates the current consumption of a switching element [8] [9]. An ideal circuit, in which no ripple in the power supply occurs, can be seen in fig. 4a. In fig. 4b the parasitics in the conductors are included, and in 4c a decoupling capacitor is added to form a more realistic power distribution system. Simulations of the circuit of figure 4c show that voltage ripple of several millivolts occurs across the capacitor model which in essence could spread to the rest of the PDS.

### 2.3. Impedance of PDS

The magnitude of a ripple in the power supply distribution system is directly influenced by the output impedance of the PDS,  $Z_o$ , which is seen by the current sink [8]. Therefore the goal of a power distribution system is to present the load with a low impedance in frequencies of interest. Hence a 'target impedance',  $Z_{target}$ , can be appointed which is the maximum value that  $Z_o$  is allowed to have in a defined frequency range so that

$$|Z_o(j\omega)| \leq |Z_{target}(j\omega)| \quad , \quad j\omega < j\omega_{max} \quad (2)$$

where

$$|Z_{target}(j\omega)| = \frac{V_{maxripple}}{I_{max}} \quad (3)$$

#### 2.3.1. Antiresonance

Antiresonance happens if a capacitance and an inductance are connected in parallel with an alternating voltage across. This can take place in a PDS with multiple capacitors in areas of frequency where one capacitor is in its inductive mode, and another in its capacitive area.

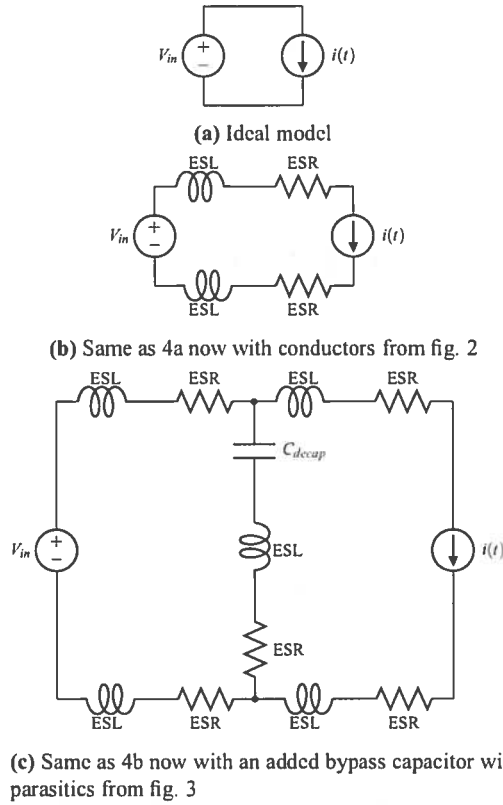


Fig. 4: Models of power distribution systems with increasing complexity

This phenomenon creates a bandstop filter with a very high impedance only limited by the equivalent series resistance of the capacitors. This is also known as a 'tank circuit' having the impedance

$$Z = \frac{Z_L Z_C}{Z_L + Z_C} = \frac{-j\omega L}{(j\omega)^2 LC - 1} \quad (4)$$

In figure 5 the impedance of a system with the equivalent circuit of two parallel capacitors is shown along with the individual impedance of the capacitors. It is easy to see that antiresonance occurs, and the impedance of the system is much higher than the individual impedance of the capacitors.

2.3.2. ESL and ESR values

In order to make qualified estimations on how the PDS will behave, we have to declare the values for ESR and ESL in the conductors and capacitors.

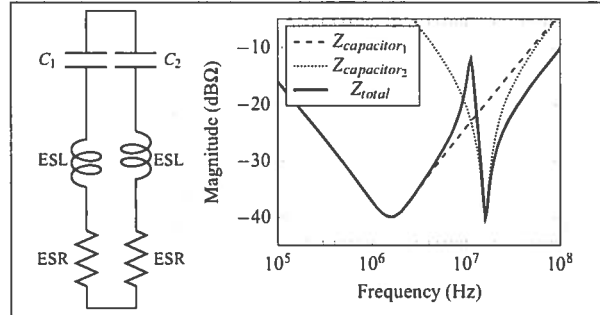


Fig. 5: Antiresonance occurs between two capacitors in parallel forming an LC tank circuit leading to a peak in impedance

Lenght	ESL / nH	ESR / mΩ
5 cm	18.3	1.5
10 cm	42.4	3.7
15 cm	59.4	8.0
20 cm	81.2	9.2
average pr. cm	4.0	0.4

Table 1: Inductances and resistances of striplines at 1 MHz

**Conductor ESL and ESR:** When it comes to conductors, we assume that ESL and ESR is proportional to the length of the conductor. With an HP4194a Impedance/Gain-Phase Analyzer, the series inductance and series resistance of striplines of different lengths were measured at 1 MHz. The result can be seen in table 1, and we can estimate an inductance per unit length of 410 pH per mm and a resistance per unit length of 4.15 mΩ per mm.

**Capacitor ESL and ESR:** The parasitic inductance of multilayer ceramic capacitors was investigated in [10]. The yield of this investigation is shown in table 2.

The parasitic resistance of SMD ceramic capacitors was investigated in [11] and the equivalent series resistance tends to fall with increasing capacitance. Selected results from this investigation are shown in table 3.

For the electrolytic bulk capacitance we assume a parasitic resistance of 100 mΩ and a parasitic inductance of 20 nH.

2.3.3. Decoupling capacitance

In this section a model of a PDS consisting of an on board

Footprint	ESL / pH
0603	870
0805	1050
1206	1200
1210	980

**Table 2:** Parasitic inductance of X7R multilayer ceramic capacitors with different footprints. From [10]

C / $\mu$ F	ESR / m $\Omega$
10	15
1	20
0.1	60

**Table 3:** ESR of X7R multilayer ceramic capacitors with 1206 footprint. From [11]

high capacity bulk capacitance in parallel with a 100 nF ceramic capacitor is investigated. The 100 nF capacitor is placed close to the load to prevent as much influence from the conductor parasitics as possible. Many engineers will recognize this setting as the 'standard' way of decouple DC voltages where it is needed.

In figure 6 it is clearly seen that even though the 100 nF ceramic capacitor provides a low impedance in the high frequency area, large antiresonance occurs at 1-2 MHz stretching roughly to a magnitude of 15 dB $\Omega$ . As a PWM signal has a very broad spectrum, this could cause unwanted ripple in the power supply.

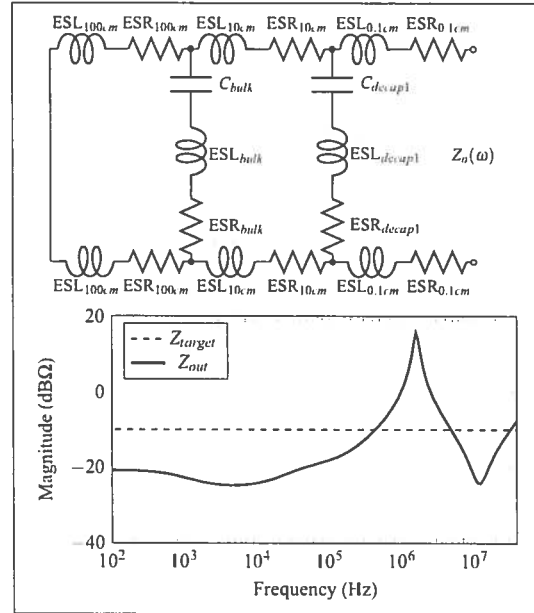
By adding a ceramic capacitor with a higher capacitance we are able to suppress this antiresonance. In figure 7 this setting is modelled with an added capacitance of 10  $\mu$ F, and it can be seen that this addition works well to suppress the antiresonance in that area.

**2.4. Filter Characteristics**

In addition to adding decoupling capacitors, it is also possible to add resistors in series with the power supply before the decoupling capacitors. However, this can only be done in small signal areas where the power demand is limited. This creates an RC lowpass filter which helps by filter any high frequency content that might be in the PDS. The circuit and its filter characteristic can be seen in figure 8.

**3. INITIAL SUMMARY**

The theoretical fundament for the PDS has until now



**Fig. 6:** Circuit diagram and impedance of power distribution system with bulk capacitance and a 100 nF decoupling capacitor close to the load

been presented. The following are relevant conclusions that can be implemented in the following sections:

- High frequency current consumption can lead to ripples in the supply voltage due to parasitics in conductors and decoupling capacitors.
- A PWM signal has a very broad spectrum, which means that impedance of the PDS has to be low in the same frequency area.
- A 'usual' PDS consisting of a large onboard electrolytic capacitor in parallel with a 100 nF ceramic capacitor close to the load can be subject to antiresonant peak in impedance at certain frequencies.
- Additional decoupling capacitance is needed to prevent this peak.
- Decoupling capacitors should be placed hierarchically so the smallest capacitance is closest to the load due to parasitics in the conductors as the parasitics increase with the length of the conductors.

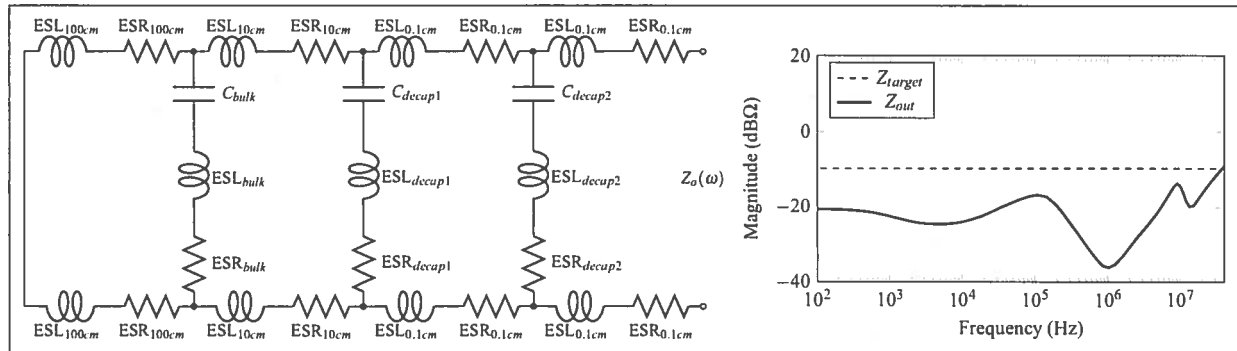


Fig. 7: Circuit diagram and impedance of power distribution system with a 10 uF and a 100 nF decoupling capacitor close to the load

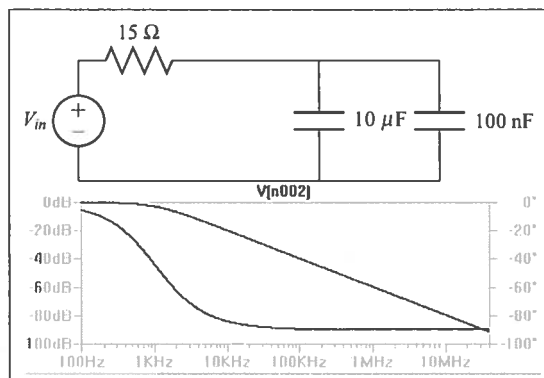


Fig. 8: Filter characteristic. The filter works well to suppress high frequency content (assuming ideal components)

- Model and experiment show that a 10 μF ceramic capacitor in parallel with the 'usual' 100 nF ceramic capacitor can be sufficient to prevent an antiresonance peak.
- Resistance in the PDS before the decoupling capacitance can increase filtering properties between PDS sections.

4. IMPLEMENTATION OF CONCEPTS OF PDS

A test stereo amplifier with an AIM self oscillating modulator in a fullbridge configuration was built to verify that emphasis on the PDS design had an impact on the level of crosstalk. In addition to this the amplifier was designed

without any global feedback networks. A block diagram is shown in figure 9.

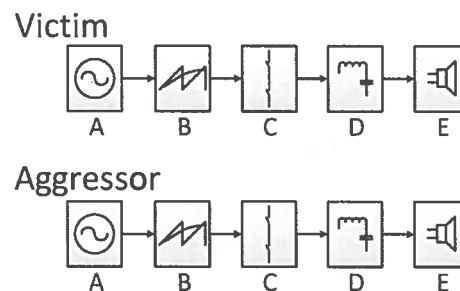


Fig. 9: Stages of the class D amplifier built for this investigation

The letters in the figure correspond to

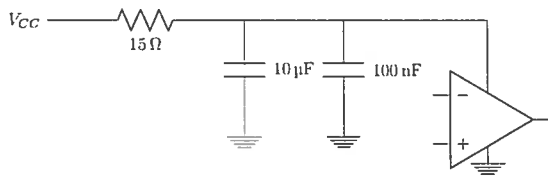
- A Signal input.
- B Self oscillating PWM generator.
- C Power stage. Fullbridge configuration with high- and lowside gatedrivers.
- D Output filter. Second order Butterworth LC filter.
- E Speaker/load.

This system is analogue to the system investigated by [4] (except for the absence of a levelshifting module), however, the channels run at a higher frequency of 330-340 kHz, and a higher rail-to-rail voltage of 25 Vdc. The gain

is approximately 16 dB. The amplifier was constructed on a solid ground plane

**4.1. Decoupling at low current demanding circuits**

As shown in the preceding sections, an improvement of the PDS to a power supply pin can be achieved by adding a 10 μF capacitor in parallel with the 'usual' 100 nF capacitor in order to make a broader range of which high frequency currents are available. In addition to this a resistor of 15 Ω in series with the supply is implemented in order improve the filtering between the channels. The proposed alteration of the circuit can be seen in figure 10. This addition to the decoupling of the DC voltages have been applied for everywhere the implicit voltages are needed.



**Fig. 10:** Proposed decoupling of a power supply pin of an op-amp / comparator to minimize noise in the PDS

The ICs that have been decoupled this way counts AIM comparators, input opamps and gate drivers. E.g. any small signal circuits that can interfere with high derivative currents.

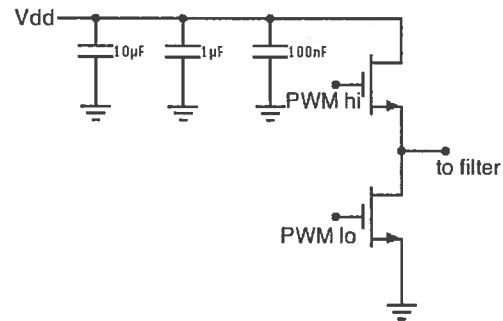
**4.2. Decoupling at the power stage**

The switching elements in this amplifier consist of MOSFETs. The proposed circuit involves an additional 10 μF capacitor (electrolytic because the high voltage exposure making ceramic capacitors of high capacitance vulnerable) which is further decoupled by a 1 μF ceramic capacitor as seen in figure 11 (The MOSFET is in a halfbridge package). No series resistance is added as high currents would make that a highly ineffective solution.

**5. RESULTS**

The results are given by Fast Fourier Transform (FFT) plots from various places in the amplifier. The graphical outcome of an FFT makes it easy to detect any crosstalk related beat tones that might occur in the signal path, as well as providing an easy guideline of how well the crosstalk is reduced.

Every FFT is measured at the same channel (denoted as the 'right' channel), thus making the right channel the



**Fig. 11:** Proposed addition to the decoupling of MOSFET circuit to minimize noise and crosstalk in the PDS

'victim' and the left channel the 'aggressor'. As was seen in figure 9.

The idle switching frequency of the amplifier is ~336 kHz for the right side and ~334 kHz for the left side. However, these frequencies can vary slightly with ± 1 kHz depending on how long the amplifier has been running. Sometimes the difference between the switching frequencies is so low that it can be difficult to distinct from e.g. 50 Hz noise found in the circuit. However, as the switching frequency varies with the modulation index *M*, a DC voltage can be applied at one of the amplifier inputs to force the difference to be more than 1 kHz. This was the approach during the measurements and thus also the main reason why the frequency of the beat tones vary in the measurements.

Any measurements of the output of the filter is with a 4 Ω power resistor load, as the load is considered to be a part of the filter.

Every measurement is made with a Rohde & Schwarz UPP 200 audio analyzer.

**5.1. Initial conditions**

In order to be able to compare the amount of crosstalk of the initial amplifier with the same amplifier with improvements denoted in chapter 3, a measurement of an FFT at the output of the idle victim channel was conducted. The outcome can be seen in figure 12.

It is clearly seen that crosstalk is present (spikes in the FFT), and, apart from the plot, it is quite audible when speakers are connected.

The first spike in the figure is at the frequency corresponding to the difference between the switching fre-

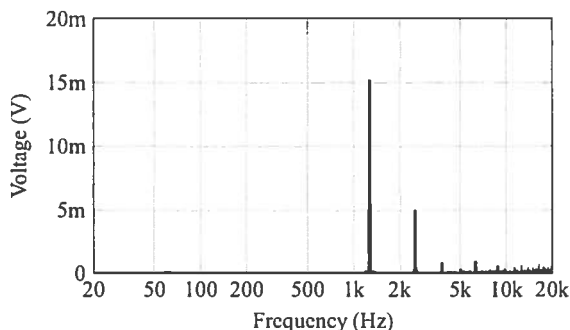


Fig. 12: Measured FFT of the output of the amplifier without any improvements. Crosstalk is present with a main spike of ~15 mV

	crosstalk voltage
Initial	180 $\mu$ V
With 15 $\Omega$ in series	20 $\mu$ V
With 10 $\mu$ F in parallel	18 $\mu$ V
With both 15 $\Omega$ in series and 10 $\mu$ F in parallel	below noise floor

Table 4: Results of adding respectively the 15  $\Omega$  resistor, the 10  $\mu$ F capacitor and both

quencies of the amplifier. The other spikes corresponds to signals of higher intermodulation order (see eq. 1).

### 5.2. Step 1: PWM Stage

Here the effect of adding the extra decoupling components is shown. The measurements are all taken from the output of the comparator in the PWM generator circuit (stage B). The measurements are presented in table form. In table 4 the results of adding respectively 15  $\Omega$  resistors in series and 10  $\mu$ F capacitors in parallel in the PDSs are shown.

Here it can be seen that each individual component contributes to a reduction of the crosstalk magnitude by approximately a factor of 20 dB. When both the resistor and capacitor is implemented it was seen that the level of crosstalk is reduced beneath the noise floor of the PWM generator, thus this solution proves to eliminate crosstalk in the modulator stage.

	crosstalk voltage
Initial (with PDS improvement of stage B)	1.2 mV
With improvement at gate driver	750 $\mu$ V
With additional decoupling at MOSFETs	500 $\mu$ V

Table 5: Results of adding the decoupling elements to the gate drivers and the MOSFETs respectively

### 5.3. Step 2: Power Stage

To measure the improvements in the power stage, FFT's where measured at the output filter to see any impact of the additions to the circuits. It was initially seen that even though crosstalk was eliminated from the PWM stage, it was still present when stage C, D and E was connected. Measurements was made with the decoupling proposed at the gate drivers and with the alternative decoupling at the power MOSFETs. The yield of these measurements can be seen in table 5.

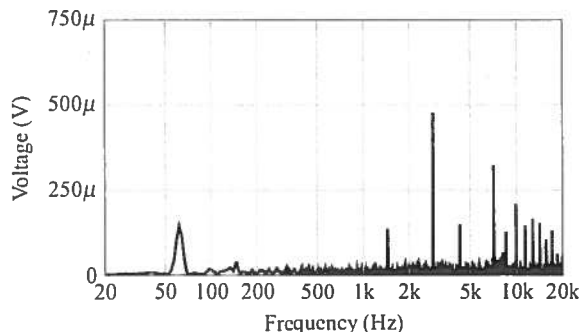
The overall results of the improvements of the power distribution system in a self oscillating class D amplifier are shown in figure 13. This FFT covers the full audio band, and it is seen that the maximum magnitude of the crosstalk has fallen from 15 mV (figure 12) to 500  $\mu$ V which corresponds to 29.5 dB. Crosstalk remains to be audible when connected to a speaker. However, it is greatly reduced and can be masked when playing audio.

## 6. CONCLUSION AND FUTURE WORK

In this project an attempt on eliminating the crosstalk due to intermodulation of the switching frequencies in a self oscillating switch mode audio power amplifier has been done. The work was conducted based on the observations in [4] and is a continuation of all the referenced work.

The emphasis was on the hypothesis that the main crosstalk couplings in the amplifier were galvanic and provided by the power supply lines to the various voltage demands in the amplifier design. By lowering the frequency dependent impedance of the power distribution systems, one would minimize power supply ripples generated by the AC current draw from the very broad spectrum of a pulse width modulated signal.





**Fig. 13:** Measured FFT of the output of the amplifier with the improvements of the PWM stage and the power stage. Crosstalk is reduced but still present with a main spike of  $\sim 500 \mu\text{V}$

Firstly a model of the power distribution system was presented alongside with theory of how to improve the performance of the power distribution system. The theory included adding higher capacitance decoupling capacitors to the power distribution system as well as adding resistors in series with the power lines to filter higher frequency components.

Thereupon it was described how the additions to the circuit was implemented. Every place where a DC voltage was needed was decoupled and filtered as the model suggested except for the power transistors where high currents made a series resistor impossible due to power dissipation.

Lastly the results of the alterations was presented step by step, and overall it was seen that by implementing the concepts from this project the amount of crosstalk in the amplifier under test was reduced by approximately 30 dB.

To summarize: Crosstalk was minimized but not eliminated in this project. Future work is proposed to include investigations of interchannel electromagnetic interference radiated by the power stage and output filter, the influence of higher currents in the power stage, and the effect of implementation on a printed circuit board.

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