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Utilization of non-linear converters for audio amplification

Niels Iversen[1], Thomas Birch[1], and Arnold Knott[1]

[1] *Technical University of Denmark, Lyngby, 2800, Denmark*

Correspondence should be addressed to Thomas Birch (`s091102@student.dtu.dk`)

ABSTRACT

Class D amplifiers fits the automotive demands quite well. The traditional buck-based amplifier has reduced both the cost and size of amplifiers. However the buck topology is not without its limitations. The maximum peak AC output voltage produced by the power stage is only equal the supply voltage. The introduction of non-linear converters for audio amplification defeats this limitation. A Cuk converter, designed to deliver an AC peak output voltage twice the supply voltage, is presented in this paper. A 3V prototype has been developed to prove the concept. The prototype shows that it is possible to achieve an peak AC output voltage twice the supply voltage but also reveals some of the major obstacles and challenges which is also discussed.

1. INTRODUCTION

Switch mode power audio amplifiers (Class D) are known for their superior efficiency compared with linear amplifiers (Class A/AB/B). Therefore Class D amplifiers have become a conventional choice in systems which demand high efficiency, such as mobile systems. The traditional topology used for Class D amplifiers is the Buck topology, typically in a full bridge configuration as shown in fig. 1.

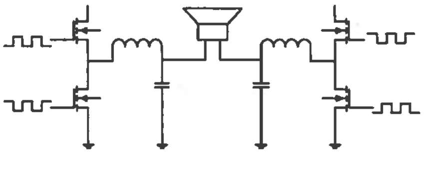

Fig. 1: Full bridge Buck power stage

The transfer ratio of the full bridge Buck (1) is linear. The linear property is desirable when amplifying audio signals because it does not contribute to the Total Harmonic Distortion (THD).

$$\frac{V_o}{V_g} = 2D - 1 \tag{1}$$

Fig. 2 reveals that the DC gain of a full bridge Buck topology is limited and only achieves a gain of -1 to 1. Feeding a class D amplifier with a sine wave, the maximum amplitude of the output sine wave will be Vg thus obtaining a maximum output power of:

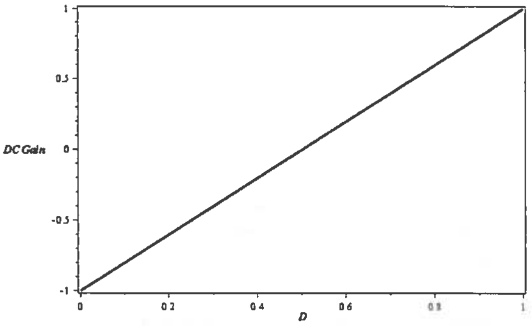

Fig. 2: DC gain of full bridge Buck topology

$$P_{o,max} = \frac{\left(\frac{V_g}{\sqrt{2}}\right)^2}{R_{Load}} \tag{2}$$

where R_{Load} is the speaker impedance. This can become a problem in systems where the voltage supply is low, which is the case for many battery driven systems. Conventional automotive audio systems have a voltage supply of $Vg = 12V$ and speaker impedance of $R_{Load} = 4\Omega$ thus limiting the output power to:

$$P_{o,max} = \frac{\left(\frac{12V}{\sqrt{2}}\right)^2}{4\Omega} = 18W \qquad (3)$$

The conventional way to achieve higher output power in such systems is to add an additional DC-DC converter to drive the amplifier power stage, boosting the voltage supply to a higher level thus obtaining more output power. However the addition of a DC-DC converter will increase the cost, increase the size and decrease the efficiency of the amplifier.

Another way to achieve high output power in such systems is by using another topology for the power stage. Non-linear topologies such as the Cuk topology can be used. Unlike the Buck topology the Cuk topology DC gain is not limited, making it able to deliver higher output power thus avoiding the drawbacks of an additional DC-DC converter. When using the Cuk topology a DC gain of -2 to 2 is possible and therefore, when feeding an amplifier with a sine wave using the Cuk topology as its power stage, the maximum amplitude of the output sine wave becomes $2Vg$. In automotive audio system, with $V_g = 12V$, the output power becomes:

$$P_o = \frac{\left(\frac{2 \cdot 12V}{\sqrt{2}}\right)^2}{4\Omega} = 72W \qquad (4)$$

Unfortunately the non-linear nature of the Cuk topology will cause a high THD. However a sufficient negative feedback system can attenuate these problems, if carefully designed, thereby obtaining good audio performance.

2. THE CUK CONVERTER FOR AUDIO AMPLIFICATION

2.1. Basic operation of conventional Cuk converter

The Cuk converter is a non-linear inverting converter with a transfer ratio similar to Buck-boost and SEPIC converters. Like the SEPIC converter the Cuk uses capacitive energy transfer when operating. Fig. 3 shows the conceptual circuit outline of the Cuk converter. The implementation of the Cuk converter is shown on fig. 4

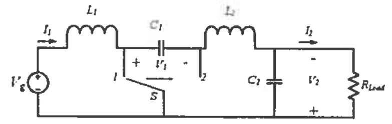

Fig. 3: Conceptual Cuk converter

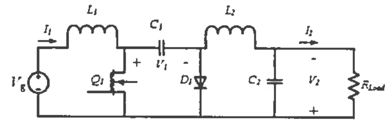

Fig. 4: Implementation of Cuk converter

The Cuk converter is well described in the literature [1] [2] [4] but the behavioral equations are repeated here for convenience.

$$V_1 = \frac{V_g}{1-D} \qquad (5)$$

$$V_2 = -\frac{D}{1-D}V_g \qquad (6)$$

$$I_1 = -\frac{D}{1-D}I_2 \qquad (7)$$

$$I_2 = \frac{V_2}{R_{Load}} \qquad (8)$$

The voltage and current waveforms is shown on fig. 5.

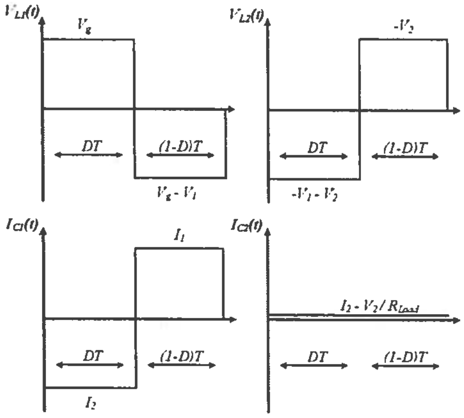

Fig. 5: Cuk converter waveforms

Since the output voltage of the converter is V_2 and the output current is I_2 we can write

$$V_2 = V_o = -\frac{D}{1-D}V_g \tag{9}$$

$$I_2 = I_o = \frac{V_2}{R_{Load}} \tag{10}$$

Using 10 the DC gain of the Cuk converter can be plotted as a function of the duty cycle as shown in fig. 6

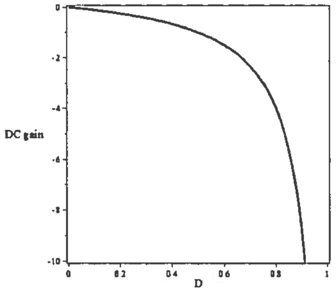

Fig. 6: DC gain of the Cuk converter

2.2. Linearized Cuk for audio amplification

The Cuk converter has a non-linear transfer ratio which is undesired in audio amplifiers. However combining two Cuk converters, as shown in fig. 7, a full bridge configuration is obtained, which linearizes the transfer ratio enables the converter to produce both a positive and a negative DC gain. This circuit is described by [4].

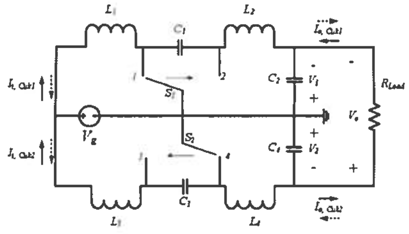

Fig. 7: Combined Cuk converters

In the full bridge configuration the two converters are switching out of phase, meaning that S1 is at position 1 in the time interval DT while S2 is at position 4, thus obtaining the two transfer ratios:

$$V_1 = -\frac{D}{1-D}V_g \tag{11}$$

$$V_2 = -\frac{1-D}{D}V_g \tag{12}$$

The combined transfer ratio for the whole converter can be evaluated as follows:

$$V_o = V_1 - V_2 \Downarrow \tag{13}$$

$$V_o = -\frac{D-(1-D)}{D\cdot(1-D)}V_g \tag{14}$$

Neglecting the inverting property of this transfer function one obtains:

$$V_o = \frac{D-(1-D)}{D\cdot(1-D)}V_g \tag{15}$$

The DC gain of the full bridge Cuk is shown on fig. 8.

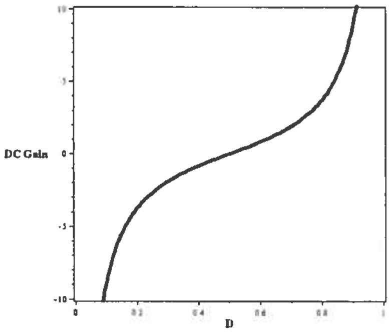

Fig. 8: DC gain of full bridge Cuk

2.3. Note on bidirectional power flow

Even though the full bridge Cuk topology seems suited for audio amplification it still lags a bidirectional power flow which a conventional full bridge Buck topology provides. However this can be obtained by replacing the diode with a MOSFET as shown i fig. 9.

The hardware implementation of the full bridge Cuk converter for audio amplification is now obtained and shown in fig. 10

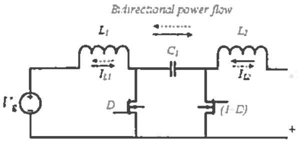

Fig. 9: Biderectional power flow

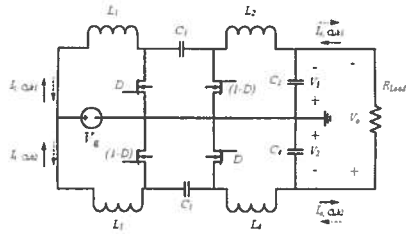

Fig. 10: Hardware implementation of full bridge Cuk converter

3. MATLAB ANALYSIS OF CUK CONVERTER FOR AUDIO AMPLIFICATION

To fully understand the consequences of using the Cuk topology in class D this section presents a thorough investigation of THD and feedback using Matlab. All investigations performed in this section is done with a fixed voltage supply of $V_g = 12V$ and a load resistance of $R_{Load} = 4\Omega$

3.1. THD investigation

In a DC-DC converter the duty cycle, D, of the PWM signal switching the power stage is fixed. In a class D amplifier the PWM signal varies with the audio input. Assuming a class D amplifier is driven with a sine function, the duty cycle will become a sine function as well. This means that the duty cycle can be modelled as follows:

$$D = 0.5 + A \cdot sin(\omega t) \quad (16)$$

A being the variation of the duty cycle, $\omega = 2\pi f$ and t the time. Substituting 16 into 15 yields:

$$V_o = \frac{0.5 + A \cdot sin(\omega t) - (1 - 0.5 + A \cdot sin(\omega t))}{0.5 + A \cdot sin(\omega t) \cdot (1 - 0.5 + A \cdot sin(\omega t))} V_g \quad (17)$$

Performing a FFT analysis of 17 one can visualise the output of the amplifier. Since 17 is an odd function the FFT analysis will contain the fundamental and odd numbered harmonic. Fig. 11 shows the output of the amplifier where $A = 0.25$ and $f = 6666kHz$.

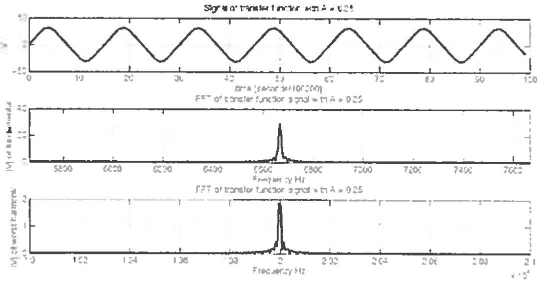

Fig. 11: FFT analysis of audio output

Only considering the 3 harmonic at 20KHz, the THD of the output can be calculated using:

$$THD = \frac{\left(\sqrt{V_{harm}^2}\right)}{V_{fund}} \cdot 100 \quad (18)$$

The RMS voltage of sine waves can be evaluated knowing the magnitude using:

$$V_{RMS} = \frac{|V|}{\sqrt{2}} \quad (19)$$

Using fig. 11 as an example the RMS voltage can roughly be estimated:

$$V_{harm} = \frac{1.9}{\sqrt{2}} \sim 1.34V \quad (20)$$

$$V_{fund} = \frac{30}{\sqrt{2}} \sim 21.21V \quad (21)$$

$$(22)$$

Thus obtaining a THD of:

$$THD = \frac{\sqrt{1.34V^2}}{21.21V} \cdot 100 \sim 6.3\% \quad (23)$$

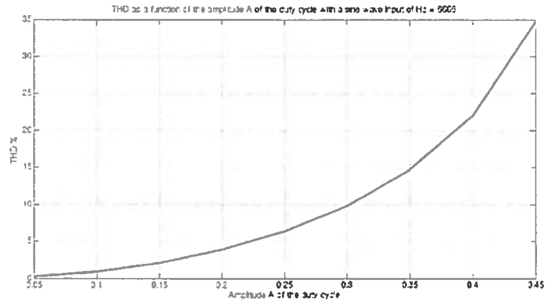

Fig. 12: THD vs. A

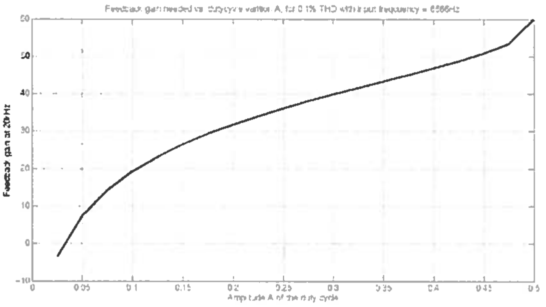

Fig. 13: Feedback gain vs. A

Keeping the input frequency at $f = 6666kHz$ one can calculate the THD for a range of different values of A and obtain a plot of the THD vs. A as shown in fig. 12.

3.2. Investigation of feedback gain

The needed $K_{feedback}$ at 20kHz to compensate for the non-linear behavior of the Cuk topology can be derived knowing the actual THD for a given value of A.

$$K_{feedback} = 20 \cdot log\left(\frac{V_{harm}}{V_{crit,harm}}\right), [dB] \tag{24}$$

Where $V_{crit,harm}$ is the critical RMS value of the harmonic to obtain a wanted THD. The critical RMS value of the harmonic can be determined as follows:

$$V_{crit,harm} = \frac{THD_{wanted} \cdot V_{fund}}{100} \tag{25}$$

Applying 25 in 24 yields:

$$K_{feedback} = 20 \cdot log\left(\frac{V_{harm}}{\frac{THD_{wanted} \cdot V_{fund}}{100}}\right) \tag{26}$$

A typical value for desired THD in class D amplifiers is 0.1%. Using fig. 11 as an example one obtain:

$$K_{feedback} = 20 \cdot log\left(\frac{1.34}{\frac{0.1 \cdot 21.21}{100}}\right) \sim 36dB \tag{27}$$

Using a range of different values for A one can plot the feedback gain as a function of A as shown in fig. 13

3.3. Summary of Matlab analysis

Section 3.1 predict that the THD will increase with duty cycle variation A. The feedback needed to significantly reduce the THD is also very depedent on duty cycle variations as seen in 3.2. A feedback gain of approximately 35-40dB will be sufficient to obtain good audio performance while delivering an output sine wave with $V_{sine} = 2V_g$ amplitude..

3.4. Note on paracitic resistances in the inductors

According to [4] the paracitic resistances in the inductors tend to linearize the full bridge Cuk's transfer ratio further. This will result in a better audio performance of the amplifier reducing the needed feedback gain. An investigation performed in [9] shows that in order to get low power loss the paracitic resistances in the inductors should be as low as possible, since the power loss will be very dependent on this value when aiming for an output sine wave with $V_{sine} = 2V_g$ amplitude.

4. IMPLEMENTATION

A prototype of an amplifier using full bridge Cuk topology has been build with $V_g = 3V$. A small signal AC model have been constructed in order to properly dimension the component values. The final transfer function for a single Cuk power stage, is shown in eq. 28

The differential transfer function, e.g the complete transfer function for the whole power stage, can be written as

$$G_{vd} = \frac{s^2 \frac{C_1 d^4 L_1}{2Rd'^2} + s\frac{L_1 d^2}{2Rd'^2} + 1}{s^4 \frac{C_1 d^4 L_2 L_1 C_2}{2d'^2} + s^3 \frac{C_1 d^4 L_1 L_2}{2Rd'^2} + s^2 (\frac{C_1 d^4 L_1}{2d'^2 R} + \frac{L_1 d^2 C_2}{2d'^2} + \frac{L_2 C_2}{2}) + s(\frac{L_2}{2R} + \frac{L_1 d^2}{2d'^2 R}) + 1} \quad (28)$$

$$G_d = G_d + G_{d'} \quad (29)$$

The following component values have been selected, based on the AC model:

- $L_{1,2} = 5.4\mu H$ and $R_L \sim 50m\Omega$.
- Energy transfer capacitor: $1\mu F$
- Output capacitor: $4.7\mu F$

The prototype utilizes a self oscillating circuit known as 'Astable Integrating Modulator' or AIM, described by [5], for PWM generation. The switching frequency is set to $f_{sw} = 1MHz$. The prototype serves as a proof of concept for increased output power compared with conventional class D amplifiers as predicted by 4. No global feedback has been implemented.

4.1. Driving the MOSFETS

The gate drivers uses individual voltage supplies to drive the low side MOSFETs. This is due to the unconventional half bridge configuration needed in the Cuk topology. In a conventional half bridge the high side MOSFET's source is referred to the low side MOSFET's drain while the low side MOSFET's source referred to ground. Fig. 14 shows the conventional half bridge with a bootstrap circuit on the gate driver.

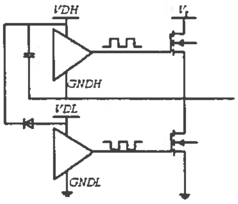

Fig. 14: Conventional half bridge

The half bridge in the Cuk topology is actually two low side MOSFETs on each side of ground as shown in fig. 15. The conventional way to implement this circuit will be to use a n-channel MOSFET for high- and a p-channel MOSFET for low side. However, when switching at high frequencies, sufficient p-channel MOSFETs are not available. Instead the use of an individual battery power supplies for the gate drivers driving the low side MOSFETs is a solution.

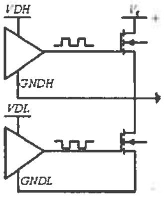

Fig. 15: Half bridge using the Cuk topology

5. MEASUREMENTS

A series of measurements are conducted on the prototype with the specific goal to verify the gain of the power stage. A sine wave of $f_{sine} = 2000Hz$ with an amplitude of $V_{sine} = 0.5V$ is applied to the input in order to see the gain delivered by the power stage. The power stage supply is set to $V_g = 2V$ in the first measurement. The output wave is shown in fig 16.

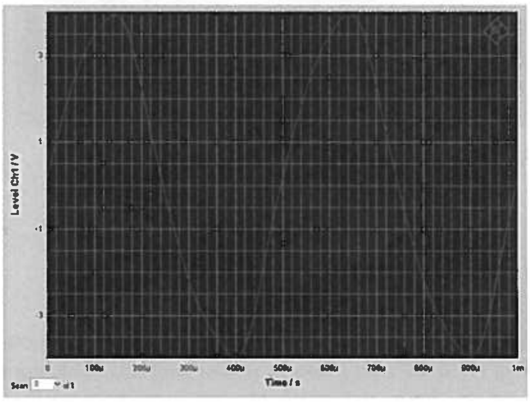

Fig. 16: Output sine of the power stage with 0.5V sine input and 2V power supply

The amplitude of the signal shown in 16 is $V_{pk} \sim 4V$. This yields a power output of:

$$P_o = \frac{(\frac{4V}{\sqrt{2}})^2}{4\Omega} \tag{30}$$

$$P_o = 2W \tag{31}$$

The measurement is repeated for a power supply voltage of $V_g = 3V$. The result is shown in figure 17.

The amplitude of the signal shown in 17 is $V_{pk} \sim 7.5V$ and the power delivered is:

$$P_o = 7W \tag{32}$$

A frequency response measurement with a sine sweep input from 20Hz to 20KHz with the amplitude $V_{sine} = 0.5V$ is conducted. The resultant frequency response is shown in 18

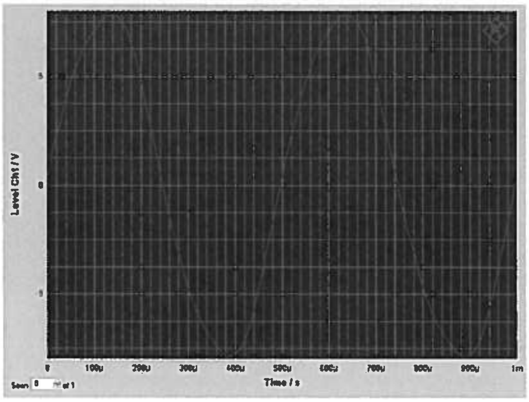

Fig. 17: Output sine of the power stage with 0.5V sine input and 3V power supply

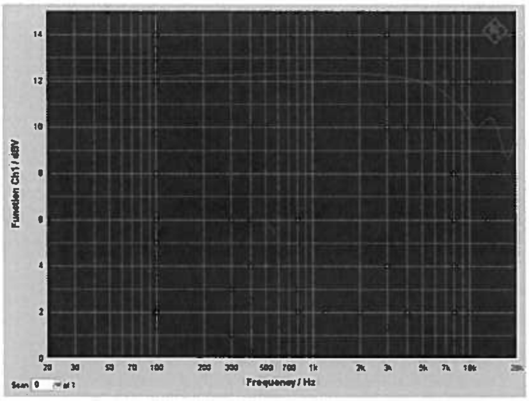

Fig. 18: Frequency response with a sine sweep from 20Hz to 20KHz and 0.5V amplitude

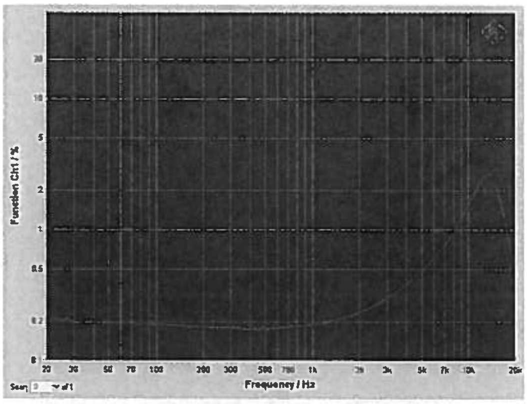

Fig. 19: THD sweep with 0.1V input sine

The frequency response shows a relatively flat response until the roll off at around $f_{bw} = 12KHz$ with minor resonant peaks around $f_{res} = 10Khz \sim$ and $f_{res} = 17Khz$.

THD measurements are also conducted with different input amplitudes. Fig 19 shows a THD measurement with an input sine amplitude of $V_{sine} = 0.1V$ and a power stage voltage of 3V The next measurement is conducted with an amplitude of $V_{sine} = 0.3V$ shown in fig 20 and the last THD measurement is conducted with $V_{sine} = 0.5V$ sine input is shown in fig. 21

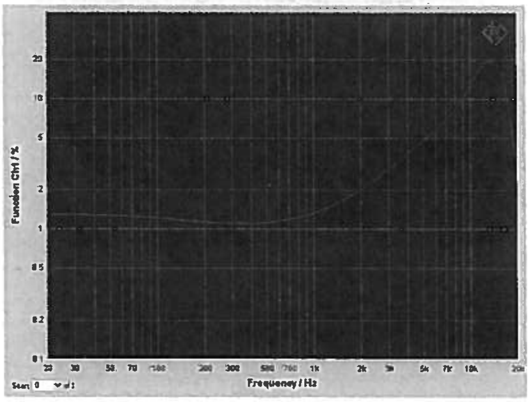

Fig. 20: THD sweep with 0.3V input sine

It is seen that the THD increases along with the input and thereby the duty cycle variation A.

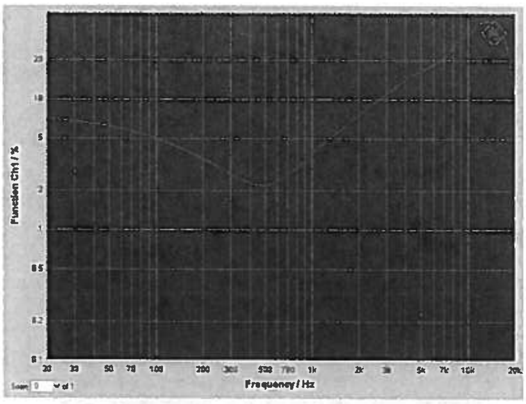

Fig. 21: THD sweep with 0.5V input sine

6. FUTURE WORK

6.1. Driving the power stage

As described in section 4.1 the MOSFETs in the power stage is driven using battery power supplies. This not an optimal solution if the class D amplifier using Cuk topology is to be a serious product in audio systems. Therefore a further investigation of the driver circuit, driving the MOSFETs, will be relevant in order to find an optimal solution to this problem. The development of high speed p-channel MOSFETs might be a solution.

6.2. $12V$ prototype

Based on the results presented in this report a natural next step will be an implementation of a $12V$ prototype with a global feedback system. A $12V$ prototype with good audio performance and good efficiency would be of great interest to automotive audio systems.

7. CONCLUSION

The following can be concluded from the investigation:

- The optimal choice of paracitic resistances is a trade off between good DC gain, feedback gain needed to obtain good THD and power loss. In order to get low power loss the paracitic resistances in the inductors should be as low as possible, since the power loss will be very dependent on this value when aiming for an output sine wave with $V_{sine} = 2V_g$ amplitude.

- Section 3 show that a feedback gain of 35-40dB is sufficient to reduce the THD and obtain a good audio performance.

- Measurements show that the prototype is capable of delivering a sine wave with an amplitude $V_{sine} \geq 2V_g$, e.g greater than two times higher than the power stage voltage. This proves the superiority of the Cuk topology over the conventional Buck topology when it comes to gain and output power.

- As expected, the THD increases dramatically when increasing the duty cycle variation. This is caused by the inherent non-linearity of the converter when reaching the outer most regions of duty cycle variation. This coincides with the theoretical predictions shown in section 3

- The prototype also exposed another set of issues, including driving of the MOSFETs, that deserves a more extensive investigation.

7.1. Perspective

The concept of driving a class D amplifier with a Cuk (or any non-linear converter) is very attractive if the inherent non-linearities can be controlled and the THD can be reduced enough to ensure a proper audio quality. The subject contains many challenges but also shows great potential, judged by the results of work presented in this report. The potential reduction in size and cost is especially interesting to the automotive industry, as earlier stated, and deserves a further examination.

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