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## Behind the Nature of Titanium Oxide Excellent Surface Passivation and Carrier Selectivity of c-Si

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### ABSTRACT

We present an expanded study of the passivation properties of titanium dioxide (TiO<sub>2</sub>) on p-type crystalline silicon (c-Si). We report a low surface recombination velocity (16 cm/s) for TiO<sub>2</sub> passivation layers with a thin tunnelling oxide interlayer (SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub>) on p-type crystalline silicon (c-Si). The TiO<sub>2</sub> films were deposited by thermal atomic layer deposition (ALD) at temperatures in the range of 80-300 °C using titanium tetrachloride (TiCl<sub>4</sub>) as Ti precursor and water as the oxidant. The influence of TiO<sub>2</sub> thickness (5, 10, 20 nm), presence of additional tunneling interlayer (SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub>), and post-deposition annealing temperature were investigated.

We have observed that that SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> interlayers enhance the TiO<sub>2</sub> passivation of c-Si. TiO<sub>2</sub> thin film passivation layers alone result in lower effective carrier lifetime. Further annealing at 200 °C in N<sub>2</sub> gas enhances the surface passivation quality of TiO<sub>2</sub> tremendously.

### INTRODUCTION

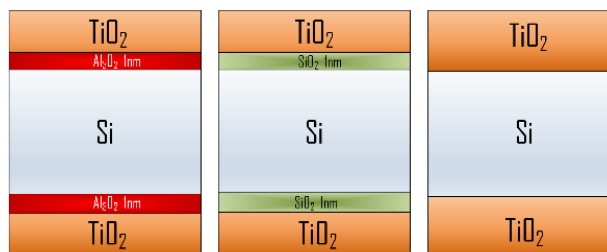
Charge carrier recombination in the silicon is one of the most significant loss mechanisms in conventional c-Si solar cells [1]. In order to reduce surface recombination dielectric films, such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, Al<sub>2</sub>O<sub>3</sub> [2] and TiO<sub>2</sub> [3,4], should be deposited on top of the silicon to passivate the surface. Traditionally, ultra-thin tunnelling SiO<sub>2</sub> and doped with amorphous silicon layer (a-Si:H) with carrier selective properties are used for passivation of high efficiency silicon solar cells [1]. However, Al<sub>2</sub>O<sub>3</sub> with a thickness 10-15 nm, deposited with ALD and annealed at 400-450 °C, is the best surface passivation layer for c-Si wafers at various doping levels [2]. In addition, TiO<sub>2</sub> has also shown excellent passivation properties on c-Si surfaces [4,5]. The best TiO<sub>2</sub> passivation films are grown with ALD at low temperatures of 80-150 °C and annealed at 200 °C. ALD TiO<sub>2</sub> is highly compatible for simultaneous deposition with Al<sub>2</sub>O<sub>3</sub> in the same deposition system [3,6,7]. Both films, TiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> are negatively charged with ideal optical properties (low optical absorption in the visible range and refractive index of 2.4 and 1.65, respectively). TiO<sub>2</sub> is also known as an electron selective contact in heterojunction silicon solar cells [8]. However, additional optimization for the best passivation properties of this film with different configurations is required to promote its applications in industrial silicon solar cells.

In this work, we demonstrate and explain the evolution of passivation properties of thermal ALD TiO<sub>2</sub> depending on deposition temperatures (80-300 °C), thickness (5-20 nm) and different tunnelling interlayers (SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>) on p- and n-type Si wafers. TiO<sub>2</sub> films are able to provide extremely low surface recombination velocity (SRV) in the order of 16 cm/s. Further annealing of the samples allowed enhanced surface passivation by several times. Excellent surface passivation of c-Si with ALD TiO<sub>2</sub> provides opportunities to develop new types of

heterojunction Si solar cells with carrier selective contacts as either an emitter or a surface passivation layer.

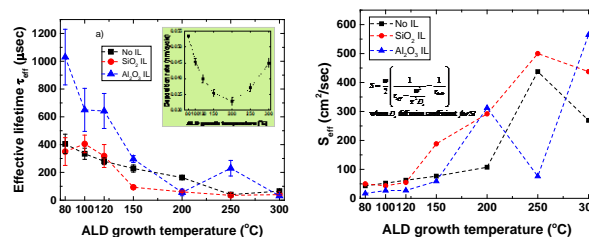
### RESULTS AND DISCUSSIONS

TiO<sub>2</sub> films were deposited onto both sides of c-Si wafers by thermal ALD (Picosun R200). Undiffused double side polished Czochralski wafers (100 orientation, 4-inch diameter, 5 Ωcm resistivity, 350 μm thick) were used as substrates. Prior to any processing all wafers from the box received standard buffered HF cleaning for 30 sec to remove the native oxide, plus a deionized (DI) water rinsing and drying. For SiO<sub>2</sub> layer growth, we used 80% HNO<sub>3</sub> acid heated to 95 °C in a glass beaker to oxidize the wafers for 10 min. The final 1.38 nm thickness of the SiO<sub>2</sub> layers was measured using ellipsometry. For Al<sub>2</sub>O<sub>3</sub> interlayer growth, we used the same ALD Picosun R200 system. We synthesized Al<sub>2</sub>O<sub>3</sub> film from Trimethylaluminum (TMA) precursor and H<sub>2</sub>O oxidant with 10 cycles at 200 °C which resulted in 1 nm thickness according to ellipsometry. After all preparations, we had three groups of wafers: bare hydrogenated Si (from bHF cleaning), SiO<sub>2</sub>-coated and Al<sub>2</sub>O<sub>3</sub>-coated interlayer coated Si wafers. (Fig.1).



**Figure 1: Schematic of ALD TiO<sub>2</sub> surface passivation with Al<sub>2</sub>O<sub>3</sub>, SiO<sub>2</sub> interlayers and with hydrogenated surfaces on c-Si wafers.**

TiO<sub>2</sub> films was synthesised on all the wafers with TiCl<sub>4</sub> precursor and H<sub>2</sub>O as the oxidant. The first experiment included ALD TiO<sub>2</sub> with a constant thickness of 20 nm on the wafers with interlayers. We have found that the deposition rate was a function of ALD temperature as shown in the insert of Fig.2a (green background).



**Figure 2: (a) Carrier lifetime and (b) SRV as a function of ALD temperature for 10 nm-thick TiO<sub>2</sub> films on p-type c-Si samples with different surface interlayers.**

The effective carrier lifetime ( $\tau_{\text{eff}}$ ) of each sample was determined by microwave detected photoconductance measurements in the transient mode (MDP, Freiburg Instruments). The effective recombination velocity ( $S_{\text{eff}}$ ) was determined at an injection level of  $10^{15} \text{ cm}^{-3}$  according to

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2S_{\text{eff}}}{W}$$

where  $\tau_{\text{eff}}$  is the effective carrier lifetime of the sample, while  $\tau_{\text{bulk}}$  is bulk carrier lifetime of the c-Si wafer, and  $W$  is the wafer thickness [1].

Fig. 2a shows that the effective lifetime increases with decreasing deposition temperature. Moreover, the effective lifetime depends significantly on interface layers. The level of surface passivation significantly improves with incorporation of  $\text{SiO}_2$  interlayer and even more for  $\text{Al}_2\text{O}_3$  interlayer as long as the  $\text{TiO}_2$  deposition temperature is low enough. SRV values were calculated according to the formula in Fig. 1b. The best lifetime of 1240  $\mu\text{s}$  and the lowest SRV of 16  $\text{cm}/\text{sec}$  were found for a  $\text{TiO}_2$  deposition temperature of 80°C and an  $\text{Al}_2\text{O}_3$  interlayer (fig.2a-b). In order to gain insight into the phenomenon of the c-Si surface passivation of  $\text{TiO}_2$  films, Fig.3 represents Raman spectra of ALD  $\text{TiO}_2$  films on glass grown at 80-300°C.

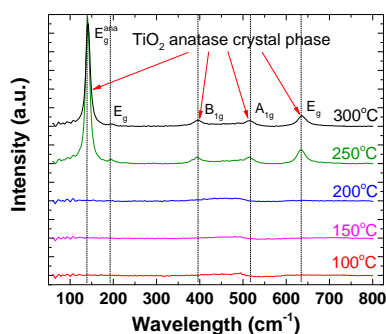


Figure 3: Raman spectra of ALD  $\text{TiO}_2$  for the sample grown at 100°C, 150°C, 200°C, 250°C, 300°C.

Raman measurements confirmed that  $\text{TiO}_2$  films were amorphous after deposition at the temperatures below 200°C and with anatase crystal phase above 250°C [9]. We then conclude that amorphous  $\text{TiO}_2$  films are preferred for c-Si surface passivation compared to crystalline  $\text{TiO}_2$  films.

In Fig. 4, we present  $\text{TiO}_2$  thickness effects on c-Si passivation. Clearly, surface passivation degrades when the  $\text{TiO}_2$  films are not thick enough

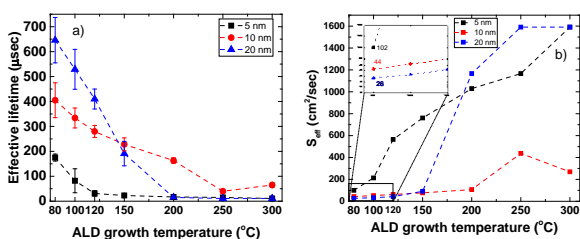


Figure 4: (a) Carrier lifetime and (b) SRV as a function of ALD temperature for 5, 10 and 20 nm thick  $\text{TiO}_2$  films.

We have shown that the highest effective lifetime for all samples was achieved at a growth temperature of 80°C. On other hand it was reported before [10–12] and proven by our current voltage characterization, that 5-6 nm thick  $\text{TiO}_2$  films have potential for application as

carrier selective contacts. Therefore, we continued with  $\text{N}_2$  annealing study of 5 nm thick  $\text{TiO}_2$  films grown at 80°C on hydrogenated Si surface and with  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$  interlayers. Fig. 5 it is seen that the best effective carrier lifetime was achieved by annealing at 200°C for 10 min in  $\text{N}_2$ . Any higher annealing temperatures and longer time decrease carrier lifetime. We have also tested forming gas annealing, but it did not show any significant improvement compared to  $\text{N}_2$  ambient annealing.

## CONCLUSIONS

In conclusion, passivation of c-Si wafer was demonstrated by using thermal ALD  $\text{TiO}_2$  films. We investigated the effect of ultra-thin interlayer on  $\text{TiO}_2$  passivation properties and showed that 1 nm  $\text{SiO}_2$  and  $\text{Al}_2\text{O}_3$  interlayers increase carrier lifetime compared to samples without any interlayers. Further, passivation properties degrade with thinner  $\text{TiO}_2$  films, however thick  $\text{TiO}_2$  films are not preferred for carrier selective contacts. Still, annealing of 5 nm  $\text{TiO}_2$  with interlayers proves that the passivation properties of 5 nm films can be almost as good as those of 20 nm films if an annealing step is included. The highest reported lifetime for samples with  $\text{Al}_2\text{O}_3$  was 1224  $\mu\text{s}$  without any annealing. The full report with annealing of 20 nm thick films and for passivation of n-type c-Si including bright and dark IV measurements results for samples with interlayers, with thickness variation and after annealing will be presented at the conference.

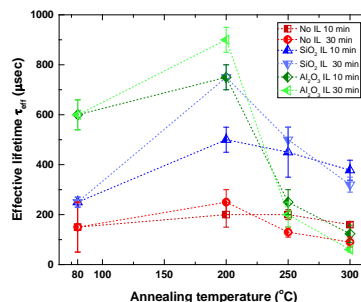


Figure 5: Annealing effect on 5 nm ALD  $\text{TiO}_2$  films on p-type c-Si samples with or without interlayers

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