Behind the Nature of Titanium Oxide Excellent Surface Passivation and Carrier Selectivity of c-Si

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ABSTRACT

We present an expanded study of the passivation properties of titanium dioxide (TiO_2) on p-type crystalline silicon (c-Si). We report a low surface recombination velocity (16 cm/s) for TiO_2 passivation layers with a thin tunnelling oxide interlayer (SiO_2 or Al_2O_3) on p-type crystalline silicon (c-Si). The TiO_2 films were deposited by thermal atomic layer deposition (ALD) at temperatures in the range of 80-300 ℃ using titanium tetrachloride ($TiCl_4$) as Ti precursor and water as the oxidant. The influence of TiO_2 thickness (5, 10, 20 nm), presence of additional tunneling interlayer (SiO_2 or Al_2O_3), and post-deposition annealing temperature were investigated.
We have observed that that SiO_2 and Al_2O_3 interlayers enhance the TiO_2 passivation of c-Si. TiO_2 thin film passivation layers alone result in lower effective carrier lifetime. Further annealing at 200 ℃ in N_2 gas enhances the surface passivation quality of TiO_2 tremendously.

INTRODUCTION

Charge carrier recombination in the silicon is one of the most significant loss mechanisms in conventional c-Si solar cells [1]. In order to reduce surface recombination dielectric films, such as SiO_2, Si_3N_4, Al_2O_3 [2] and TiO_2 [3,4], should be deposited on top of the silicon to passivate the surface. Traditionally, ultra-thin tunnelling SiO_2 and doped with amorphous silicon layer (a-Si:H) with carrier selective properties are used for passivation of high efficiency silicon solar cells [1]. However, Al_2O_3 with a thickness 10-15 nm, deposited with ALD and annealed at 400-450 ℃, is the best surface passivation layer for c-Si wafers at various doping levels [2]. In addition, TiO_2 has also shown excellent passivation properties on c-Si surfaces [4,5]. The best TiO_2 passivation films are grown with ALD at low temperatures of 80-150 ℃ and annealed at 200 ℃. ALD TiO_2 is highly compatible for simultaneous deposition with Al_2O_3 in the same deposition system [3,6,7]. Both films, TiO_2 and Al_2O_3 are negatively charged with ideal optical properties (low optical absorption in the visible range and refractive index of 2.4 and 1.65, respectively). TiO_2 is also known as an electron selective contact in heterojunction silicon solar cells [8]. However, additional optimization for the best passivation properties of this film with different configurations is required to promote its applications in industrial silicon solar cells.
In this work, we demonstrate and explain the evolution of passivation properties of thermal ALD TiO_2 depending on deposition temperatures (80-300 ℃), thickness (5-20 nm) and different tunnelling interlayers (SiO_2, Al_2O_3) on p- and n-type Si wafers. TiO_2 films are able to provide extremely low surface recombination velocity (SRV) in the order of 16 cm/s. Further annealing of the samples allowed enhanced surface passivation by several times. Excellent surface passivation of c-Si with ALD TiO_2 provides opportunities to develop new types of heterojunction Si solar cells with carrier selective contacts as either an emitter or a surface passivation layer.

RESULTS AND DISCUSSIONS

TiO_2 films were deposited onto both sides of c-Si wafers by thermal ALD (Picosun R200). Undiffused double side polished Czochralski wafers (100 orientation, 4-inch diameter, 5 Ωcm resistivity, 350 µm thick) were used as substrates. Prior to any processing all wafers from the box received standard buffered HF cleaning for 30 sec to remove the native oxide, plus a deionized (DI) water rinsing and drying. For SiO_2 layer growth, we used 80% HNO_3 acid heated to 95 ℃ in a glass beaker to oxidize the wafers for 10 min. The final 1.38 nm thickness of the SiO_2 layers was measured using ellipsometry. For Al_2O_3 interlayer growth, we used the same ALD Picosun R200 system. We synthesized Al_2O_3 film from Trimethylaluminum (TMA) precursor and H_2O oxidant with 10 cycles at 200 ℃ which resulted in 1 nm thickness according to ellipsometry. After all preparations, we had three groups of wafers: bare hydrogenated Si (from bHF cleaning), SiO_2–coated and Al_2O_3–coated interlayer coated Si wafers. (Fig.1).

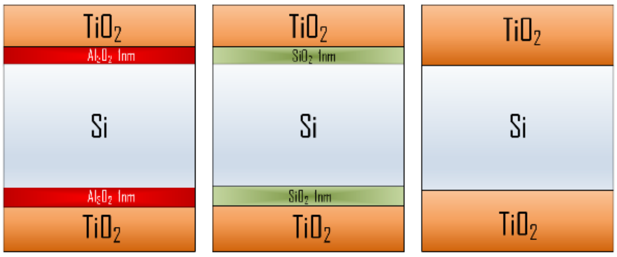

Figure 1: Schematic of ALD TiO_2 surface passivation with Al_2O_3, SiO_2 interlayers and with hydrogenated surfaces on c-Si wafers.

TiO_2 films was synthesised on all the wafers with $TiCl_4$ precursor and H_2O as the oxidant. The first experiment included ALD TiO_2 with a constant thickness of 20 nm on the wafers with interlayers. We have found that the deposition rate was a function of ALD temperature as shown in the insert of Fig.2a (green background).

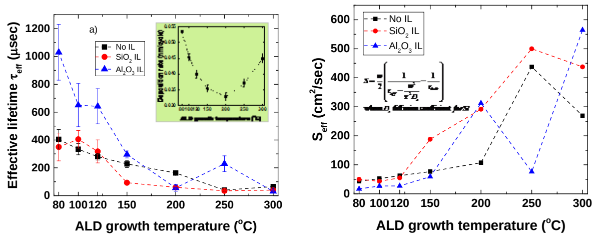

Figure 2: (a) Carrier lifetime and (b) SRV as a function of ALD temperature for 10 nm-thick TiO_2 films on p-type c-Si samples with different surface interlayers.

The effective carrier lifetime (τ_{eff}) of each sample was determined by microwave detected photoconductance measurements in the transient mode (MDP, Freiburg Instruments). The effective recombination velocity (S_{eff}) was determined at an injection level of 10^{15} $\mathrm{cm^{-3}}$ according to

$$\frac{1}{\tau_{\mathrm{eff}}} = \frac{1}{\tau_{\mathrm{bulk}}} + \frac{2S_{\mathrm{eff}}}{W}$$

where τ_{eff} is the effective carrier lifetime of the sample, while τ_{bulk} is bulk carrier lifetime of the c-Si wafer, and *W* is the wafer thickness [1].

Fig. 2a shows that the effective lifetime increases with decreasing deposition temperature. Moreover, the effective lifetime depends significantly on interface layers. The level of surface passivation significantly improves with incorporation of SiO_2 interlayer and even more for Al_2O_3 interlayer as long as the TiO2 deposition temperature is low enough. SRV values were calculated according to the formula in Fig. 1b.The best lifetime of 1240 µs and the lowest SRV of 16 cm/sec were found for a TiO2 deposition temperature of 80C and an Al_2O_3 interlayer (fig.2a-b). In order to gain insight into the phenomenon of the c-Si surface passivation of TiO_2 films, Fig.3 represents Raman spectra of ALD TiO_2 films on glass grown at 80-300℃.

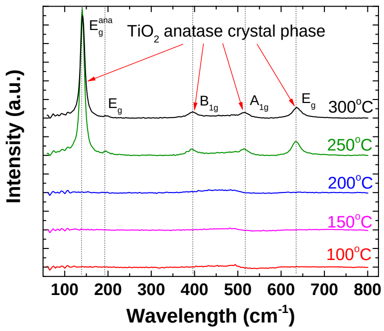

Figure 3: Raman spectra of ALD TiO_2 for the sample grown at 100℃, 150℃, 200℃, 250℃, 300℃.

Raman measurements confirmed that TiO_2 films were amorphous after deposition at the temperatures below 200 ℃ and with anatase crystal phase above 250 ℃ [9]. We then conclude that amorphous TiO_2 films are preferred for c-Si surface passivation compared to crystalline TiO_2 films.

In Fig. 4, we present TiO_2 thickness effects on c-Si passivation. Clearly, surface passivation degrades when the TiO_2 films are not thick enough

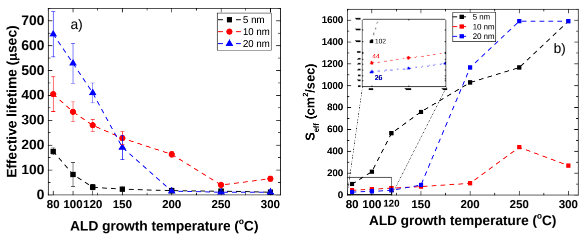

Figure 4: (a) Carrier lifetime and (b) SRV as a function of ALD temperature for 5, 10 and 20 nm thick TiO_2 films.

We have shown that the highest effective lifetime for all samples was achieved at a growth temperature of 80℃. On other hand it was reported before [10–12] and proven by our current voltage characterization, that 5-6 nm thick TiO_2 films have potential for application as carrier selective contacts. Therefore, we continued with N_2 annealing study of 5 nm thick TiO_2 films grown at 80℃ on hydrogenated Si surface and with SiO_2 or Al_2O_3 interlayers. Fig. 5 it is seen that the best effective carrier lifetime was achieved by annealing at 200℃ for 10 min in N_2. Any higher annealing temperatures and longer time decrease carrier lifetime. We have also tested forming gas annealing, but it did not show any significant improvement compared to N_2 ambient annealing.

CONCLUSIONS

In conclusion, passivation of c-Si wafer was demonstrated by using thermal ALD TiO_2 films. We investigated the effect of ultra-thin interlayer on TiO_2 passivation properties and showed that 1 nm SiO_2 and Al_2O_3 interlayers increase carrier lifetime compared to samples without any interlayers. Further, passivation properties degrade with thinner TiO_2 films, however thick TiO_2 films are not preferred for carrier selective contacts. Still, annealing of 5 nm TiO_2 with interlayers proves that the passivation properties of 5 nm films can be almost as good as those of 20 nm films if an annealing step is included. The highest reported lifetime for samples with Al_2O_3 was 1224 µs without any annealing. The full report with annealing of 20 nm thick films and for passivation of n-type c-Si including bright and dark IV measurements results for samples with interlayers, with thickness variation and after annealing will be presented at the conference.

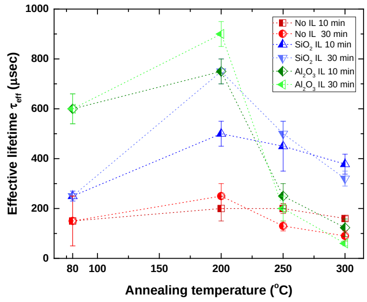

Figure 5: Annealing effect on 5 nm ALD TiO_2 films on p-type c-Si samples with or without interlayers

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