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# DREM: Infinite etch selectivity and optimized scallop size distribution with conventional photoresists in an adapted multiplexed Bosch DRIE process

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## ABSTRACT

The quest to sculpture materials as small and deep as possible is an ongoing topic in micro- and nanofabrication. For this, the Bosch process has been widely used to achieve anisotropic silicon microstructures with high aspect ratio. Reactive ion etching (RIE) lag is a phenomenon in which etch rate depends on the opening areas of patterns, aspect ratio of the trenches and other geometrical factors. The lag not only gives a non-uniform distribution of scallop size, but it also sets a limit for the maximum achievable aspect ratio. The latter since the mask suffers from persistent erosion. While different kinds of hard masks have been suggested to ensure a longer total etch time, here we report a correctly tuned 3-steps Bosch process – called DREM (Deposit, Remove, Etch, Multistep) – without mask erosion. The erosion-free feature is independent of the type of mask. For example, an aspect ratio of more than 50 is achieved for trenches with 1  $\mu\text{m}$  linewidths, while no erosion is observed for 360 nm thin standard photoresists. The mechanism behind this extraordinary infinite selectivity is mainly due to the depletion of  $\text{C}_4\text{F}_8$  deposition species. Furthermore, a linear ramping of the etch step duration is performed to achieve a uniform distribution of scallop sizes along the etch profile. This outperforms the usual broad scallop size distribution when no parameter ramping is performed and improves the straightness of the etch profile considerably, in addition, it allows an easier way to control periodic sidewall shaping. e.g., a sausage-chain-like feature is demonstrated with an almost perfect periodicity.

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## 1. Introduction

Etching silicon is one of the key technologies in mainstream semiconductor industry and dry plasma etching has become indispensable to transfer patterns anisotropically (i.e. directionally). The current trend is to sculpture the silicon as deep and precise as possible while preserving the critical dimension of the original photoresist pattern; i.e. to achieve extreme high aspect ratios. Two perfect examples are the creation of deep silicon pores to create highly area-efficient trench capacitors and the structuring of high-raised silicon pillars useful in the fast evolving photonic crystal discipline. By performing a pulsed process in so-called deep reactive ion etching (DRIE; e.g. the Bosch sequence), the sidewall of trenches can be protected during an etch process and the etch depth can be significant with minimal undercut. However, the achievement of extremely high aspect ratios, e.g. larger than 50, remains challenging. The main reason is that, when etch depth increases, the silicon etch rate slows down due to the notorious

reactive ion etching (RIE) lag [1], while the mask erosion continues at the same speed. This means that the selectivity (etch rate of silicon divided by the erosion rate of mask) drops drastically when the aspect ratio increases and the etching should be halted before the mask is totally eroded away. This issue sets a limit for high aspect ratio etching and a lot of efforts have been undertaken to find a “hard” mask with sufficient high selectivity, e.g. Al [2], Cr [3],  $\text{SiO}_2$  [4], or  $\text{Al}_2\text{O}_3$  [5]. However, a hard mask can be sputtered during etching and creates roughness [6]. Furthermore, the transfer of resist patterns into the hard mask will increase fabrication complexity.

Another issue to consider in Bosch sequences is the non-uniform distribution of scallops [7]. While the scallops are generated during the isotropic silicon etch steps, due to RIE lag the scallop size decreases while the Bosch process continues. This non-uniformity in scallop size is pronounced especially in devices with high aspect ratio. Furthermore, this aspect ratio dependent scallop size distribution will not only change the sidewall profile, but it will also generate difficulties for post-etch sidewall smoothing procedures.

A third important high aspect ratio feature is sidewall corrosion due to off-normal ionic bombardment. It can be due to the not always perfectly straight trajectory of ions leaving the plasma boundary, some

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collisions inside the plasma sheath, or deflection of the charged species by an image force [14]. Although this issue can be very problematic, it has not been truly pronounced in the present work and will therefore not be addressed in detail.

Here we propose a correctly tuned 3-steps cyclic Bosch process (step 1 –  $C_4F_8$  deposition, step 2 – Ar bottom removal, and step 3 –  $SF_6$  isotropic silicon etch) as suggested in previous literature [8]. From now on we will call this procedure DREM (**D**eposit, **R**emove, **E**tch, **M**ultistep). By carefully tuning the balance between deposition and bottom removal, the mask can stay fully intact and an infinite etch selectivity is achieved. Furthermore, a linear time ramping of the etch step is employed to counteract the decreasing etch rate caused by RIE lag. By combining these two techniques, it is possible to etch silicon trenches (1  $\mu\text{m}$  linewidth, 10  $\mu\text{m}$  pitch) with an aspect ratio of more than 50 without degradation of a conventional photoresist while keeping all the scallops downwards the trench almost identical in size rendering the sidewall almost perfectly straight.

## 2. Materials and methods

Silicon wafers (150 mm diameter, single side polished) were given a 65 nm (60 s at 4700 rpm) thick bottom antireflective coating (BARC, DUV42s-6, Brewer Science) in a robot system (Gamma 2 M, Süss) with a soft baking temperature of 60 s at 175 °C. On top of the BARC layer, a 360 nm thick deep ultraviolet (DUV) resist (JSR KRF M230Y, JSR-Micro) was coated (60 s at 2500 rpm) with a 90s soft baking temperature at 130 °C. Afterwards trenches with 1  $\mu\text{m}$  linewidth and 10  $\mu\text{m}$  pitch were patterned by a DUV stepper system (FPA-3000EX4, Canon), which was equipped with a 248 nm KrF excimer laser (intensity 280 mW/cm<sup>2</sup>, dose 21 mJ/cm<sup>2</sup> and focus depth 0.17  $\mu\text{m}$ ). The samples were baked right after exposure for 60 s at 130 °C, and developed in AZ726 (AZ Electronic Materials) for 60 s, rinsed in DI water and dried by spin coating in a gentle nitrogen stream.

The thickness of both the BARC layer (65 nm) and resist (355 nm) were determined by a spectroscopic ellipsometer (Vase, J.A. Woollam Co., Inc.), with a standard deviation of 1 nm. To verify the critical dimension of exposed patterns, scanning electron microscopy (SEM, Supra V60, Zeiss) images were taken both from a top view and cross-sectional view. The results show an average linewidth of 0.95  $\mu\text{m}$  across the wafer, with standard deviation of 0.02  $\mu\text{m}$ . The sidewall angle of the resist was measured to be around 82°.

The plasma etching process was performed in a dual source etching system (DRIE Pegasus, SPTS) from which the settings will be discussed in the next section. The samples were cleaved manually into pieces of around 2 cm by 2 cm and attached to a carrier wafer with Fomblin oil (Solvay Solexis S.P.A.). To ensure sufficient process reproducibility, the

silicon carrier wafers (100 mm, single side polished) were coated with 100 nm  $Al_2O_3$  (alumina) passivation coating by atomic layer deposition (ALD, Picosun R200 ALD system). These carrier wafers have been found to be relatively undisturbed by the plasma and could be reused throughout the experiments.

After etching, the sample pieces were cleaved manually and analyzed by SEM. The analysis of scallop size distribution was performed by Matlab (R2015b, MathWorks), which could extract coordinates of scallop edges from the SEM images.

## 3. Results and discussions

### 3.1. Infinite etch selectivity

The basic parameter setting for the 3-steps DREM process with an illustrative diagram is shown in Fig. 1. A full tool recipe is presented in the supplementary section. In the first **1.8 s deposition step**,  $C_4F_8$  plasma is used to passivate the wafer with a fluorocarbon (FC) layer. A minimum of platen power is applied to ensure low mask erosion [9]. The processing temperature was chosen to be approximate minimum of –19 °C allowed by the tool. Also the pressure is optimized with respect to the 3000 W coil power for maximum FC deposition rate. In the second **1.9 s removal step**, low pressure (5mTorr) argon plasma with high bias power (75 W, with DC bias of around 325 V) is used for 1.0 s to clear the FC film from the bottom of the trenches. By taking rise time of mass flow controllers (MFC) and delay time caused by the reactor residence time into consideration, the process synchronization is established for optimal performance as suggested in [8]. It is easier to maintain low pressure plasma with argon than with e.g.  $SF_6$ , because argon is an electropositive gas (it provides electrons) whereas  $SF_6$  is electronegative (it scavenges electrons). To minimize the coil reflective power, the argon gas flow was chosen to be 200sccm during deposition, and 250sccm during bottom removal and etching. The lowest possible pressure during bottom removal is needed to sharpen the ion angular distribution as much as possible, thus ensure a maximum straight profile. In the third **time-ramped etching step**,  $SF_6$  based plasma is used to etch silicon isotropically at the cleared bottom of the trenches. Again a minimum platen power is applied, to preserve the mask. By using time ramping during this  $SF_6$  step, the scallop sizes can be tuned to be almost identical along the trench. The initial etch step duration was chosen to be 0.6 s to ensure correct initial etches and the final etch step duration  $t_{end}$  was carefully tuned as discussed in the next section. We should notice that switching off the  $SF_6$  flow abruptly after the etch step is bad news for the coil reflected power as the sudden change in plasma chemistry will cause sharp harmful peaks in the reflected power. We have improved this issue by smoothing the gas flow changes

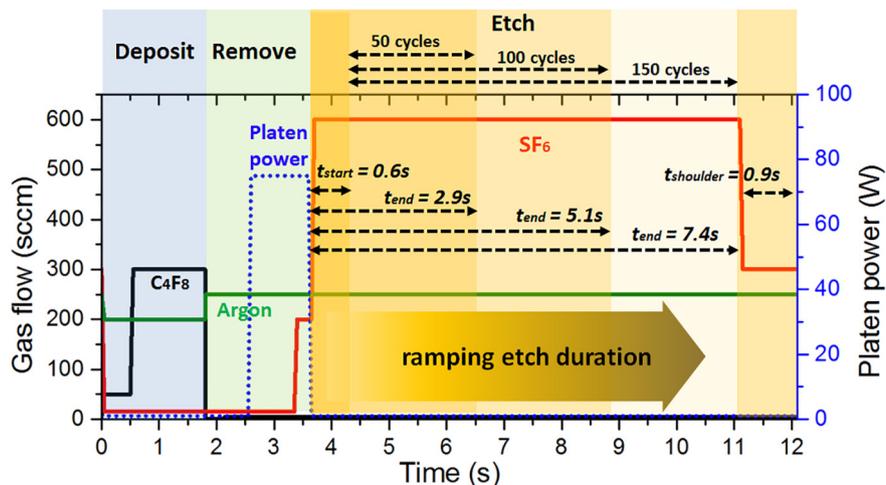


Fig. 1. DRIE parameters and etch sequence.

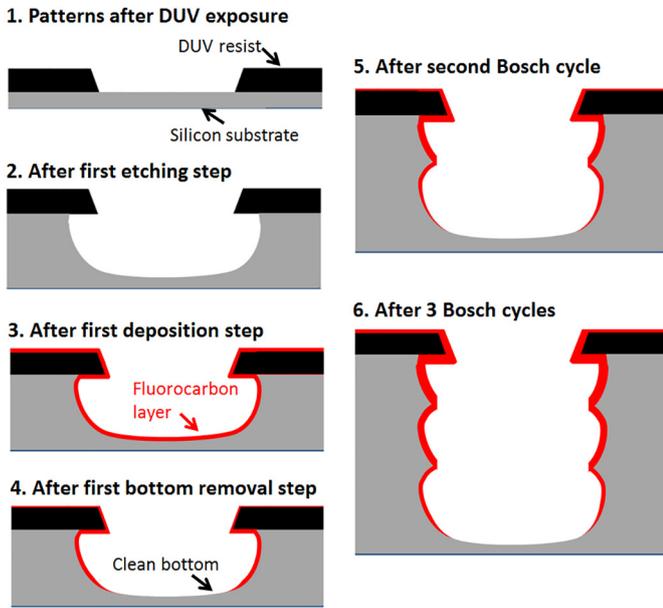


Fig. 2. Schematic of the first DREM cycles showing that silicon is etched without photoresist attack.

with what we call ‘shoulders’. For the SF6 flow, the flow starts with a 0.3 s at 200sccm shoulder and then it goes to 600sccm and it stops the flow with a 1 s at 300sccm shoulder. For the 300sccm C4F8 flow we did the same with a 50sccm shoulder. Using the gas flow shoulders, we could maintain a very high power without matching problems.

The reason why an infinite selectivity is achieved is not because of intrinsic properties of a specifically selected photoresist. Most resist-types have selectivities around 100 or less [10]. Instead, the extraordinary high selectivity is caused by the non-conformal FC deposition inside etched structures. This layer protects not only the features sidewalls, as well as the mask. The mechanism is shown briefly in Fig. 2. Firstly, silicon is etched isotropically using SF6 plasma (Fig. 2.1 and 2.2). Secondly, C4F8 is applied for FC passivation (Fig. 2.3). Importantly, due to depletion of species inside the trenches, the thickness of the FC film is thicker on top of the resist pattern compared with the bottom of the etching trench. Then, the FC film is removed directionally with a bias during the Ar bottom removal step. If the applied bias is just enough for clearing the bottom of the trench, the resist will still be covered by some added FC film residue (Fig. 2.4). Thus, when the etch process goes on to next cycles, the resist (or any other mask material) will always be protected (Fig. 2.5 and 2.6).

The etch profiles of the 1 μm wide trenches are shown in Fig. 3. After etching the BARC layer, 50 cycles were performed to reach an etch depth of 18.8 μm (Fig. 3.a1), while the 360 nm resist remained intact (Fig.3.b1). After 100 cycles, the etch depth was doubled and the resist was still undisturbed (Fig. 3.a2/b2). Noticeably, a rather thick FC layer started to grow at the topside of the etched structure narrowing the trench opening of the flowing gases (Fig. 3.b2). This effect is a direct result from the non-uniform step coverage due to the lack of surface migration. So, the downside of the infinite selectivity (which is based on the non-uniform coating characteristic) is that the smaller openings tend to close while etching proceeds. When we increased the number of cycles further to 150, the etch depth was around 58.1 μm, which implied an aspect ratio of more than 50, while the sidewall of the trench started to be slightly corroded (Fig. 3.a3). Furthermore, the trenches have the tendency to become a slightly more positive tapered towards

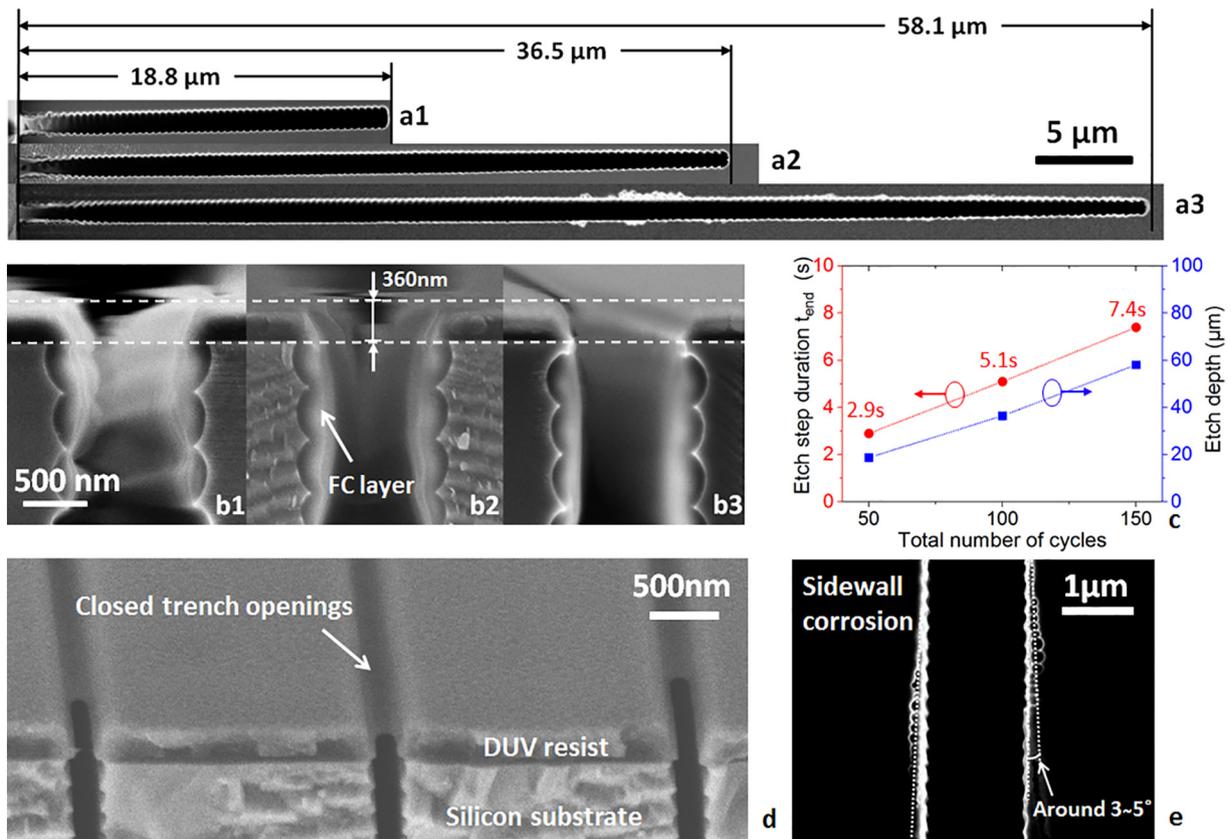


Fig. 3. Etch profile evolution during DREM a1) 50 cycles; a2) 100 cycles; a3) 150 cycles. And the corresponding top parts of the trenches b1) 50 cycles; b2) 100 cycles; b3) 150 cycles. The linearly increasing etching depths for these three processes are shown in (c), with different etching step durations  $t_{end}$  at the end of etch. For trenches with linewidth of 200 nm, the openings are closed as shown in (d). For trenches with high aspect ratio, slight sidewall corrosion can be observed as shown in (e).

the bottom of the trench. This is most likely the result of the slowly closing trench entrance while etching proceeds. The total etch depths and the duration of etch step in the last cycle  $t_{\text{end}}$  are shown in Fig. 3.c, which suggests a linear relation between etch depths and total number of cycles, this is due to the identical scallop sizes given by parameter ramping. Thus, by carefully tuning DREM, silicon can be etched directionally with identical scallops and infinite selectivity with respect to conventional photoresists; i.e. resist is not consumed at all. Obviously any mask (e.g. Cr, SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>), even though not demonstrated here, will be able to perform this task as well. Therefore, DREM is believed to be the key to realize ultrahigh aspect ratio structures with a free choice in masking material.

There are two issues that should be addressed regarding this process. The first is the closing trench most likely due to the lack of surface migration of the growing FC film. On the one hand the FC film will provide the top part of the trench sufficient protection against erosion, but on the other hand the non-conformal layer will limit the incoming etching species and influence the ion angular distribution (IAD), both of which will cause non-uniformity in the etch process. When the process continues the trench will even be fully closed and the etch process will not be able to continue. This effect is especially pronounced for trenches with a very small linewidth (as shown in Fig. 3.d), in which the top part of a 200 nm wide trench is totally closed by the FC layer. The method to solve this problem is to add an oxygen plasma pulse after every SF<sub>6</sub> etch step. Thus the trench can be opened again and DREM can continue. So, in total there will be 4 steps during this process, which the authors have called the DREAM process (Deposition with C<sub>4</sub>F<sub>8</sub>, Removal bottom with Ar, Etching with SF<sub>6</sub>, Ashing with O<sub>2</sub>, Multistep). Clearly, due to the constant removal of FC polymer, the photoresist will also erode quickly and the infinite selectivity with respect to photoresist is lost, thus in this paper, a DREM process (that is to say, a DREAM process without the O<sub>2</sub> ashing step) was performed, which results in a straight profile with a

relatively high aspect ratio. Nevertheless, for hard mask materials DREAM is a viable option.

Another issue is the sidewall corrosion, which can be clearly seen when the aspect ratio is more than 50 (as shown in midsection in Fig. 3.a3 and a close up view in Fig. 3.e). The authors noticed that this sidewall corrosion is closely related to the sidewall angle of the profile. We already discussed that the passivation of ion inhibitors is increasingly limited with increasing aspect ratio and, therefore, the lower region of the sidewall will be less FC protected. However, during the bottom removal step the accelerated argon ions can be transported down to the bottom of trenches virtually unchanged in number. But, due to the non-ideal Ion Angular Distribution (IAD), also the sidewall will be continuously exposed to off-normal incoming energetic ions. Thus when the etching depth increases, the off-normal argon ions will start to corrode the passivation layer and create weak points in the sidewall protection [11]. Since the middle part of the trench has less sidewall protection compared with the top part, and is exposed to the ion bombardment for a longer time than the bottom part, the sidewall corrosion is most pronounced in the middle of the trench. One way to solve this issue is to tune the profile to a slightly negative tapered angle, either by increasing the platen power during bottom removal steps, or by reducing the passivation during the deposition steps. With the profile slightly negatively tapered, the sidewall will suffer less off-normal ion bombardment. The downside of this method is that the infinite selectivity might get lost.

### 3.2. Optimized scallop size distributions

As mentioned in the previous section, parameter ramping was used to achieve uniformly distributed scallop sizes. The direct measurement of scallop sizes along the sidewall, however, can be difficult or cumbersome, and several techniques have been reported before, e.g. using a

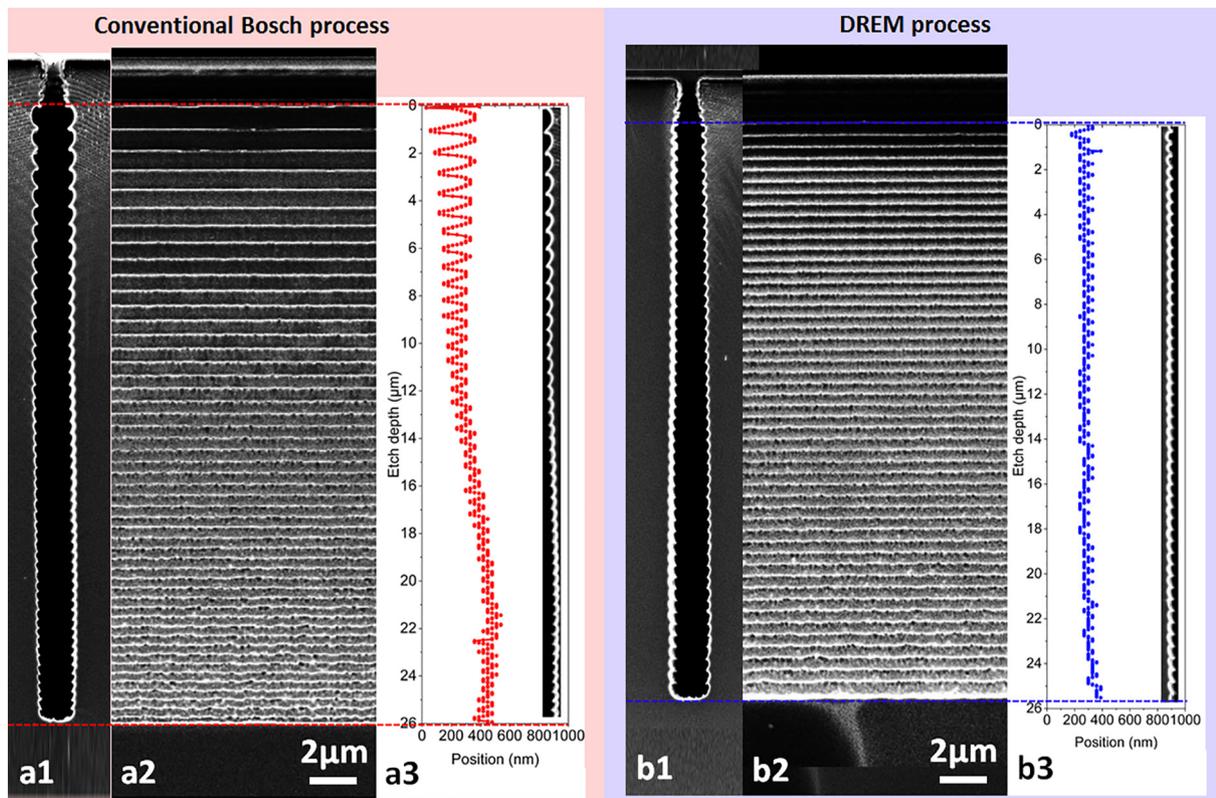


Fig. 4. Etching profile of experiment a (a1) without time ramping, and experiment b (b1) with time ramping. A 2-dimensional view of sidewall surface of exp.1 (a2) and exp.2 (b2). Extracted etch profile from exp.1 (a3) and from exp.2 (b3).

specially built atomic force microscopy (AFM) system as in [12,13], or using a conventional AFM system to scan the surface of a replica from the trench structures [14]. In our experiment, in order to quickly get a quantitative analysis for process optimization, the samples were first manually cleaved and pictured with SEM and further studied by Matlab. Based on the pixel size and coordinates of sidewall edges, the scallop sizes can be calculated and analyzed.

Two experiments were performed to prove the increased uniformity of scallop size distribution. In the first experiment, we performed 'standard' 50 Bosch cycles with a 1.5 s deposition step and a fixed 6.0 s etch

step. The etch depth was 29.4  $\mu\text{m}$  (Fig. 4.a1). In the second experiment, to counteract the effect of changing scallop size and profile straightness due to RIE-lag, the  $\text{SF}_6$  time was linearly ramped from 3.5 s to 8.5 s during 50 DREM cycles. The other parameters were unchanged. The etch depth was 27.5  $\mu\text{m}$  (Fig. 4.b1). Although the etch depth of exp.1 is slightly larger than in exp.2, the scallop sizes can be observed to be more uniform when etch-time ramping is performed. The samples were also cleaved manually along the trench openings, which gave a direct view of 2-dimensional sidewall surface as in Fig. 4.a2 and Fig. 4.b2. The etch profiles of both experiments were extracted from SEM images

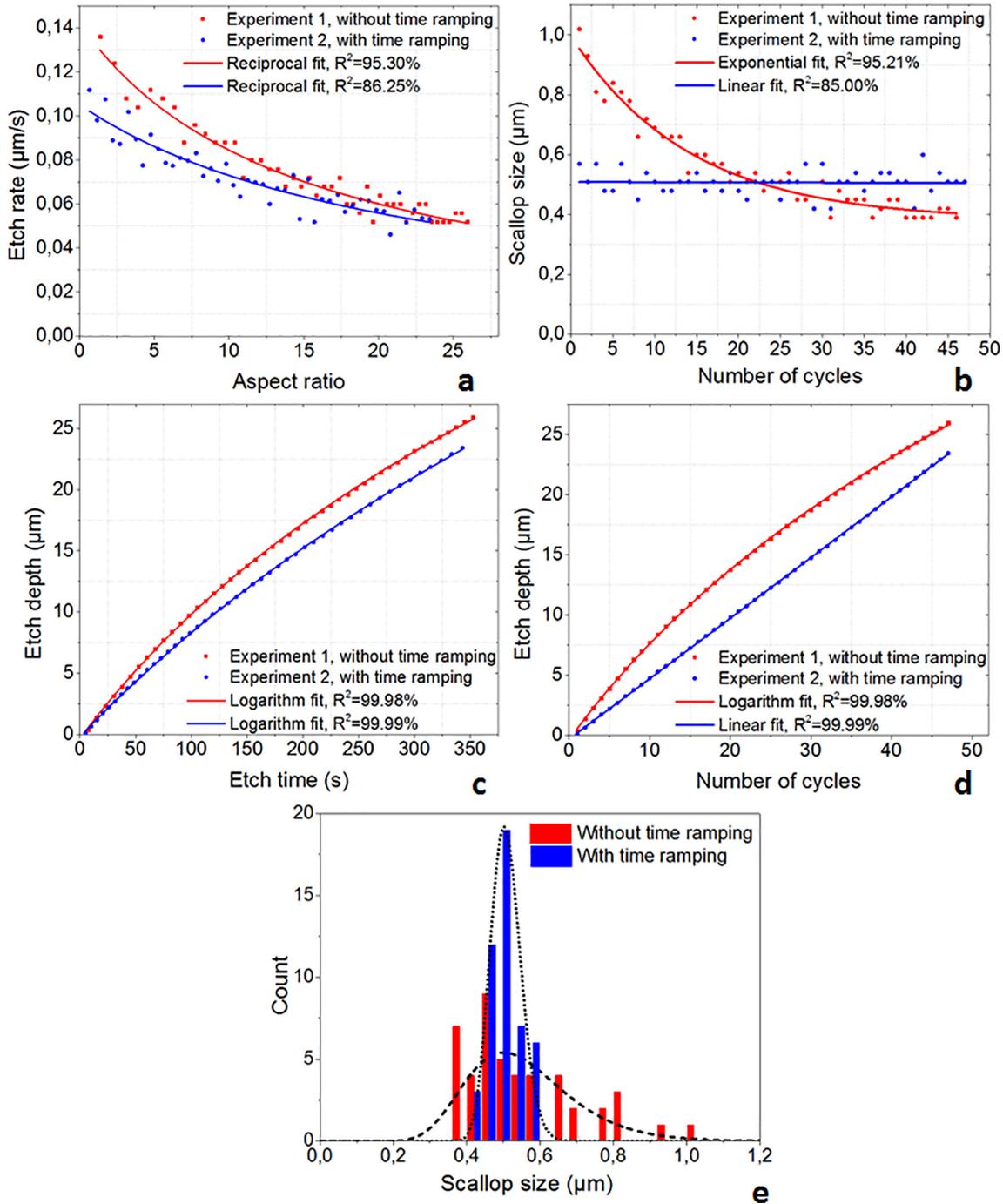


Fig. 5. Etch rate as a function of aspect ratio for both experiment 1 and experiment 2 (a); scallop sizes as a function of number of cycles for both experiment 1 and experiment 2 (b). Etch depth as a function of etch time for both experiment 1 and experiment 2 (c); etch depth as a function of number of cycles for both experiment 1 and experiment 2 (d); scallop size distributions for both experiment 1 and experiment 2 (e).

using Matlab (Fig. 4.a3 and 4.b3), from which we can clearly see an increased uniformity of scallop sizes and profile straightness when performing time ramping.

RIE lag is a phenomenon in which etch rate depends on the opening areas of patterns, aspect ratio of the trenches and other geometrical factors [1]. Some studies explain this by ion angular distribution, which will cause depletion of ions and radicals along the trench and slow down the etch process [15]. Other studies suggest attenuated neutral transport along the trench passage to be the reason [16]. Whatever is the actual cause, when aspect ratio increases the etch rate (scallop size divided by cycle time) for both experiments decreases (Fig. 5.a). Nevertheless, while in exp.1 the average scallop size decreases monotonically (Fig. 5.b), the scallop sizes for exp.2 remains roughly identical (507 nm with 40 nm standard deviation). Of course, the etch depth as a function of time is still nonlinear for both experiments (Fig. 5.c), which also suggests a decreasing etch rate (slope of the curve). However, the

etch depth as a function of number of cycles (Fig. 4.d) is linear for exp.2. A qualitative explanation of this linear relation can be, that in our experiments the linearly increasing etch time can compensate for the decreasing average etch rate, which can be approximated as a quadratic function of aspect ratio [17]. However, depending on different models, the relation between the average etch rate and aspect ratio can be more complicated [18] [19], and for higher aspect ratio etching, a quadratic fitting will deviate from the real average etch rate, thus a linearly increasing etch time will not be sufficient to compensate for the drop of average etch rate.

From the results above, we can see that by performing a parameter ramping during a Bosch process, we can counteract the effect of RIE-lag on the usual non-uniformity of scallop sizes. Since the variance of scallop sizes has a detrimental effect on overall sidewall roughness and sidewall straightness, a higher uniformity of scallop size distribution will make the sidewall much straighter. At the same time it is also

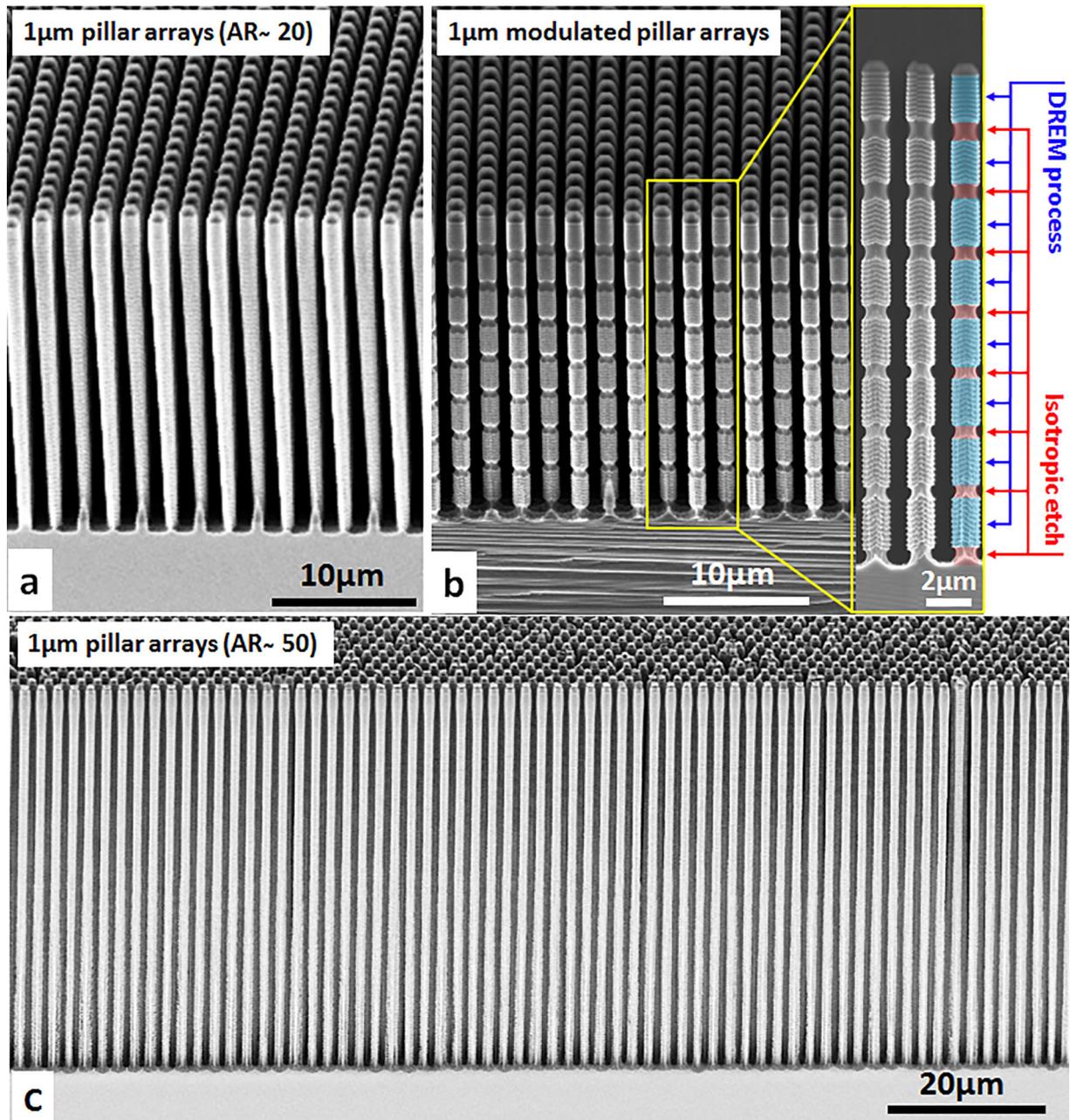


Fig. 6. 1  $\mu\text{m}$  pillars after 100 DREM cycles (a); the same DREM process but repeatedly interrupted by time-controlled isotropic etches that creates sausage-chain-like features (b); 1  $\mu\text{m}$  pillars after 175 DREM cycles (c). (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

a promising method for high aspect ratio etching as for very high aspect ratios, any deviation from a straight profile will limit the maximum achievable aspect ratio.

The strategies discussed above have been successfully applied to pillar structures with diameters of 1  $\mu\text{m}$ . Firstly, 100 cycles of DREM process were applied resulting in an etch depth of 23  $\mu\text{m}$  (Fig. 6.a). Secondly, a combination of DREM process and isotropic etch process was performed, in such a way that every 10 cycles of DREM process were followed by isotropic etch (200sccm  $\text{SF}_6$ , 3000 W coil power, 0 W platen power, the time was ramped up at the same rate as the Bosch cycles), 80 DREM process cycles were performed in total. This specially modified etch process can achieve a modulated etch profile (Fig. 6.b), which consists of straight etch profiles (labeled by blue false color in Fig. 6.b) separated by “nodes” with isotropic profiles (labeled by red false color in Fig. 5.b). We can notice that there is still plenty of photoresist left, and the distance between each ‘nodes’ is very similar (2.5  $\mu\text{m}$ ). These special features couldn't be achieved without the high etch selectivity and an accurate control of etch profiles. As a consequence, DREM can open pathways to manufacture periodic 3D structures beneficial for example in next generation photonics or electronics. Besides, by applying 175 cycles DREM cycles, a high aspect ratio of 50 could be achieved for pillar structures with diameter of 1  $\mu\text{m}$  (Fig. 6.c).

#### 4. Conclusions

A DREM procedure is reported to improve and optimize a conventional DRIE process (Bosch). An aspect ratio of 50 is achieved for 1  $\mu\text{m}$  wide trenches with identical scallops down the trench and without any consumption of conventional photoresist during the etch process. We have achieved a plasma etch process with infinite selectivity. This procedure is promising to etch deep silicon structures without using hard masks, which will not only get rid of sputtering issues, but also simplify the process flow. The reported process can be beneficial for industrial productions, since less materials and less time needs to be invested. The scallop size distribution is optimized using a parameter ramping strategy, which can “correct” the effect of RIE-lag. This process can be favorable for applications as microbattery [20], photonic devices [21], through silicon vias [22], X-ray gratings [23], etc. For post etch processes such as sidewall smoothing by oxidation [24], this uniform distribution of scallops and a straight profile are also favorable, since scallops will be oxidized at almost the same oxidation rate.

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#### Appendix A. Supplementary data

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.mee.2018.01.034>.

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