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Published in:
Applied Physics Letters

Link to article, DOI:
10.1063/1.5026362

Publication date:
2018

Document Version
Publisher's PDF, also known as Version of record

Link back to DTU Orbit

Citation (APA):
Nanoscale patterning of electronic devices at the amorphous LaAlO$_3$/SrTiO$_3$ oxide interface using an electron sensitive polymer mask

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(Received 19 February 2018; accepted 13 April 2018; published online 26 April 2018)

A simple approach is presented for designing complex oxide mesoscopic electronic devices based on the conducting interfaces of room temperature grown LaAlO$_3$/SrTiO$_3$ heterostructures. The technique is based entirely on methods known from conventional semiconductor processing technology, and we demonstrate a lateral resolution of $\sim$100 nm. We study the low temperature transport properties of nanoscale wires and demonstrate the feasibility of the technique for defining in-plane gates allowing local control of the electrostatic environment in mesoscopic devices. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). https://doi.org/10.1063/1.5026362

Since the discovery of a two-dimensional conducting electron system (2DES) at the interface between TiO$_2$ terminated strontium titanate (STO) and lanthanum aluminate (LAO)$_1$, the efforts towards exploring, understanding, and utilizing the electronic properties of oxide interfaces have attracted significant attention from all branches of physics and materials science. One example is the drive towards the integration of oxide interfaces in mesoscopic devices to complement the semiconductor heterostructures and bottom-up grown nanostructures which have been the material platform for two decades of research in quantum transport. The oxide electron systems share the properties of low dimensionality and electrostatic gatability$^2$ with the conventional semiconductor systems but in addition display a wide range of phenomena such as gate-tunable superconductivity, ferroelectricity, magnetism, and spin-orbit coupling caused by strong electron-electron and electron-lattice interactions in regimes not accessible in semiconductors.$^{3,4}$ However, the oxide 2DES is highly sensitive to the quality of the epitaxial interfaces and subsequent surface processing.$^5$ A range of specialized fabrication techniques have therefore been developed for realizing patterned oxide devices while protecting interfaces and limiting post processing. Such techniques range from patterned growth of the oxide top-layer by hard-mask techniques,$^6$ ion irradiation,$^1$ thickness variations of the top layer,$^1$ or the creation of conducting nanostructures using scanning probe lithography.$^3$ Such approaches are more involved than conventional semiconductor processing and often include wet etching which is difficult to control leading to limited reproducibility and resolution.

Most studies so far have considered crystalline STO-based heterostructures where the top-films are deposited at temperatures above $\sim$600 $^\circ$C. Room temperature (RT) deposition such as for the amorphous LAO/STO (a-LAO/STO) system also leads to conducting interfaces where electrons predominately originate from oxygen vacancies$^{14,15}$ and usually exhibit reduced mobilities compared to crystalline LAO/STO.$^{16}$ The key properties of gate-tunability and gate-tunable superconductivity,$^{17,18}$ however, remain intact, and moreover, the highest transition temperature reported for the STO-based 2DES was achieved in the a-LAO/STO system.$^{19}$ Also, recently, studies were performed on the transport properties of negative-U quantum dot devices which were fabricated from a-LAO/STO heterostructures.$^{17,20}$ Thus, the a-LAO/STO system provides an interesting system for mesoscopic oxide devices, and here, we demonstrate that the reduced deposition temperature allows patterning of the interface conductivity by a conventional electron-beam or optical lithography with only minor adjustments. We explore the limitations of the technique in terms of lateral resolution and the performance of nanoscale devices at low temperatures.

Our fabrication procedure is schematically illustrated in Fig. 1(a). The starting point is a (001) STO single crystal with a TiO$_2$ terminated surface$^{21}$ achieved by first sonicating in anisole (AZ1505 photo resist) and heated for 1 min at 120 $^\circ$C. Additionally, the e-beam sensitive polymer mask is cleared from patterned growth of the oxide top-layer by hard-mask techniques.$^6$ The substrates are cleaned in MQ water for 120 s at RT. Substrates are coated with 2% polymethyl methacrylate (PMMA) and cleaned in Milli-Q water for 1 min. We study the low temperature transport properties of nanoscale wires and demonstrate the feasibility of the technique for defining in-plane gates allowing local control of the electrostatic environment in mesoscopic devices. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). https://doi.org/10.1063/1.5026362

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temperature annealing and deposition has previously been used for defining insulating structures in crystalline LAO/STO devices. For defining conducting structures, it is, however, crucial that the exposed surface does not contain any resist residues and previous attempts excluding the last cleaning steps have been found to lead to insulating samples. We have tested the patterning technique for both e-beam lithography and optical lithography yielding similar results; in the following, we present the results obtained using the former technique. The final PMMA resist profile is shown in Fig. 1(e), and a representative AFM image of the surface terraces in the exposed channel is shown in Fig. 1(f) after the cleaning procedure. No discernible differences to the as-treated surface are observed. A top layer of 12 nm a-LAO was grown by room temperature Pulsed-Laser-Deposition (PLD). To investigate the properties of the 2DES induced at the exposed interfaces and the spatial resolution of the lithographical patterning, standard Hall-bars (Fig. 2) were defined as well as structures allowing 4-terminal measurements of leakage currents between parallel wires with varying separations and of the conductance of wires of varying widths. Hall-bar samples were fabricated with a width of \( W = 30 \mu m \) and a length of \( L = 500 \mu m \), and Fig. 2(a) shows a representative sample after the growth of the top layer. Measurements were performed in a dilution refrigerator with a \( T = 20 \) mK base temperature, and standard lock-in techniques were used to measure the longitudinal \( V_{xx} \) and transverse \( V_{xy} \) voltage drops as indicated in the figure. The samples were mounted in a sample carrier using conductive silver epoxy, and the overall carrier density was modulated by biasing the conducting back-plane of the sample \( (V_{BG}) \). No leakage was measured between neighboring Hall-bars on the samples. As seen in Fig. 2(b), the sheet resistance \( R_s = (W/L)V_{xx}/J \) decreases upon cooling as typically observed for metallic oxide interfaces. The dependence of \( R_{xx} \) and \( R_{xy} \) on a perpendicular magnetic field \( B \) at 20 mK is shown in Fig. 2(c). The positive magneto-resistance in \( R_{xx} \) is observed in all samples and has also been reported previously for oxide interfaces and has been attributed to contributions from more than one carrier type. The finite value for \( R_{xy} \) at \( B = 0 \) is attributed to a contribution from the longitudinal voltage drop due to an off-set of the voltage probes or a non-isotropic current path in the sample. Fitting \( R_{xx} \) and the high-field value of \( R_{xy} \) to the two-band model as shown in the figure, we find a higher density \( n_1 = 4.75 \times 10^{13} \text{ cm}^{-2} \) of low mobility \( \mu_1 = 125 \text{ cm}^2/\text{V s} \) and a lower density \( n_2 = 7.5 \times 10^{12} \text{ cm}^{-2} \) of high mobility carriers.

FIG. 1. Schematic illustration of the patterning technique. (a) An STO substrate is prepared with a TiO\(_2\) surface termination. (b) The surface is spin coated in polymer-based electron or optically sensitive resist and (c) conventional techniques are used for exposure and development, followed by careful cleaning. (d) Amorphous LAO is deposited on the substrate by room temperature PLD. (e) SEM image of a 2 \( \mu m \) wide channel taken with a 50° angle to the plane of the substrate. The inset shows an AFM image of the a-LAO/STO. The scale bar is 200 nm. (f) Typical AFM image of the STO surface after cleaning; the color scale is 0–8.5 nm.

FIG. 2. (a) Optical microscopy image and schematic measurement setup for a typical sample used for Hall characterization. (b) Temperature (black) and back-gate (blue) dependence of the sheet resistance. The cooldown curve shows typical metallic behavior, while the back-gate dependency shows similar behavior to an \( n\)-type semiconductor. (c) Low temperature Hall characterization with \( R_{xy} \) (black) and \( R_{xx} \) (blue) and fits to a two-band model (dashed lines).
The spatial resolution of the patterning technique is crucial for fabrication of nanoscale devices. The pattern in the PMMA resist can routinely be defined with a resolution below 50 nm. The conducting interface is, however, not created until the deposition of the LAO top film in the exposed regions, and depending on the ability of the plasma cleaning step described above and of the plasma of the PLD to enter nanoscale patterns in the ~100 nm thick mask layer [Fig. 1(b)], the resulting conducting areas may be smaller than the resist openings. On the other hand, since the interface conductivity is presumably a result of oxygen vacancies created when depositing the top-layer, and that the oxygen diffusion length may be significant, this could lead to conducting regions extending beyond the resist openings. This could be the consequence of under-cut in the exposed resist profile due to exposure by electrons back-scattered from the substrate which is often the case. Thus, in the case where either of these mechanisms are significant, the actual resolution would not be set by the resolution of the lithography. To investigate this, two types of devices were fabricated allowing 4-terminal measurements of (1) the leakage currents between sets of parallel wires with varying separations, $s = 5, 2, 1, 0.5, 0.25 \mu m$, between the resist openings [Fig. 3(a)] and (2) the conductance of wires defined with varying widths, $W = 5, 2, 1, 0.5, 0.25 \mu m$ [Fig. 3(c)].

Considering first the leakage between separated structures, none of the devices showed leakage at low bias and the three largest wire separations show negligible leak currents up to a bias voltage of $|V_{bias}| = 10$ V at room temperature. For the wires separated by 250 nm and 500 nm, however, a leak current is observed for an applied bias of $|V_{bias}| \approx 4.5$ V for the 250 nm wire and at $|V_{bias}| \approx 9$ V for 500 nm. Note that after the devices leak, the currents in Fig. 3(b) are set by a 100 MΩ series resistor included for protection. At low temperatures, the leakage threshold decreased to $|V_{bias}| \approx 150$ mV for the smallest separations probably due to the temperature dependent dielectric properties of STO (see below). For all devices, the observed leakage was reversible, suggesting the origin to be a tunneling effect between the parallel wires rather than the electronic discharge or physical rearrangement of atoms in the sample. From AFM inspection of the resist profiles, the edges of the openings have a roughness of about 25 nm, and since the measured leakage will be dominated by the points of smallest separation, the absence of leakage at low bias shows that the conducting region extends at most 100 nm beyond the resist openings and presumably much less.

Figure 3(d) shows the RT resistance of the wire devices as a function of the width. To reduce the effects of inhomogeneities, each device consists of 5 identical wires in parallel. Each wire is 100 μm long and has two 45 μm long sections that are kept at a width of 5 μm joined together by a central narrow section of length $L$ and varying width $W$. In
of the 2DES and summarize, the results in Fig. 3 show that within an uncertainty of the resist openings even for the most narrow wires. To sum-

width of the conducting region is consistent with the width of structure17 or nearby regions of the 2DES itself can be utilized tively coupled metallic top electrodes isolated from the electron contacts (QPCs). Local gates are usually defined by capaci-

tion and state-of-the-art semiconductor processing. Such systems implementing local electrostatic gate-control of the carrier density in narrow constrictions. Various aspects of the patterning approach were demonstrated using room temperature grown amorphous LAO as the top-layer; however, alternative STO-based conducting room temperature grown interfaces have been reported,16,18 and we expect that the techniques reported in this study may be directly applied to such systems as well. The results present a simple way to bridge the gap between oxide-based quantum device fabrication and state-of-the-art semiconductor processing.

We acknowledge the Villum Foundation for financial support. The Center for Quantum Devices was supported by the Danish National Research Foundation.
