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# Area-Efficiency Trade-Offs in Integrated Switched-Capacitor DC-DC Converters

Frederik Monrad Spliid, Dennis Øland Larsen, and Arnold Knott

Department of Electrical Engineering  
 Technical University of Denmark  
 2800 Kongens Lyngby, Denmark

s113010@student.dtu.dk deno@elektro.dtu.dk akn@elektro.dtu.dk

**Abstract**—This paper analyzes the relationship between efficiency and chip area in a fully integrated switched capacitor voltage divider dc-dc converter implemented in 180nm-technology and a 1/2 topology. A numerical algorithm for choosing the optimal sizes of individual components, in terms of power loss, based on the total chip area is developed. This algorithm also determines the optimal number of parallel phases in the converter, based on an estimate of power consumption in flip-flop based clock circuits. By these means the maximum achievable efficiency as a function of chip area is estimated.

## I. INTRODUCTION

In order to increase the speed and performance of modern electronics, it is constantly sought to increase the number and density of transistors on silicon chips. With circuit power being a primary constraint, the development of integrated power supplies is of great importance. New technologies enable the use of smaller components, increasing the power density of converters, while maintaining the high efficiency of traditional switch-mode converters, examples include [1] and [2].

This paper explores the relationship between chip area and efficiency for a converter with a typical load current for a low power microcontroller in a battery powered device, see Table I for specifications. The converter is designed from a 1/2 series-parallel voltage divider topology, as described in [3] and shown in Fig. 1.

This topology consists only of capacitors and switches, making monolithic integration relatively simple. In order to achieve the highest possible converter efficiency for any given chip area, different capacitor types are examined, and the distribution of area between switches and capacitors that allows the highest efficiency is determined.

The work described in this paper is focused on a converter implemented in 180nm technology, but the same optimization can also be applied to more advanced processes.

Area-driven optimization of switched-capacitor converters has previously been investigated in [4], but in this paper a more detailed optimization of the 1/2 voltage divider is described, taking into account output capacitance and multiphase interleaving.

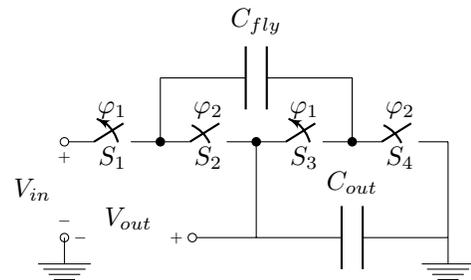


Fig. 1. Converter schematic

## II. SC CONVERTER LOSS ANALYSIS

The power loss in a switched-capacitor converter can be described as 2 groups: *Intrinsic losses*, which depend on the converter topology, and *extrinsic losses*, which include gate loss, parasitic capacitance loss and control circuitry power consumption. The extrinsic losses can be minimized by correctly sizing the switches and capacitor relative to each other. Extrinsic losses can also be minimized by special circuit techniques such as parasitic charge recycling [1].

$V_{in}$	$V_{out}$	$I_{Load}$
1.3 V $\pm 5\%$	600 mV $\pm 5$ mV	450 $\mu$ A

TABLE I. CONVERTER SPECIFICATIONS

### A. Impedance analysis

An idealized model of the SC converter is seen in Fig. 2. The conversion ratio in the converter is defined by the topology and output impedance,  $R_{out}$ . As the name implies, the ideal voltage conversion ratio (iVCR) of a 1/2 voltage divider is 1:1/2, but with a non-zero output impedance and load current, the actual conversion ratio will be slightly lower. The output impedance needed to deliver the desired output voltage at a given load current is described by the following equation, where  $N = iVCR$ :

$$R_{out} = \frac{NV_{in} - V_{out}}{I_{load}} \quad (1)$$

As described in [5] the output impedance of the converter can be approximated by 2 asymptotic expressions: The fast switching limit (FSL), determined by the on-resistance in the switch components, and the slow switching limit (SSL), dominated by the amount of flying capacitance. For the voltage

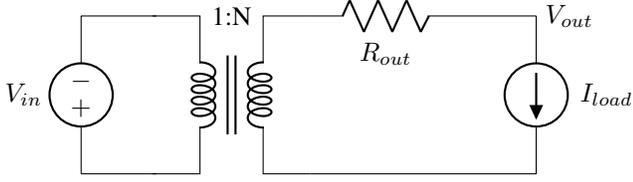


Fig. 2. Model of an idealized switched-capacitor converter

divider, the expressions are as follows:

$$R_{FSL} = \frac{1}{2} \sum_{k=1}^4 R_{onk} \quad (2)$$

$$R_{SSL} = \frac{1}{4C_{fly}f_{sw}} \quad (3)$$

The value of  $C_{fly}$  will increase linearly with the capacitor area, and the on-resistance of the switches can be assumed to be inversely proportional to the gate width for a given gate length.

For converters with an output capacitance in the same range as the flying capacitance, a better fitting approximation of the slow switching limit is described in [3]:

$$R_{SSL} = \frac{C_{out}}{C_{out} + C_{fly}} \cdot \frac{1}{4C_{fly}f_{sw}} \quad (4)$$

The total output impedance can be approximated by the Euclidian norm of the two elements:

$$R_{out} = \sqrt{R_{FSL}^2 + R_{SSL}^2} \quad (5)$$

While the total size of the output impedance is constrained by the conversion ratio and load current, the distribution between the capacitive and resistive elements can freely be chosen.

For optimization purposes, a constant  $\beta$  is introduced to describe the relative size of the two impedance elements:  $R_{FSL} = \sqrt{1-\beta}R_{out}$  and  $R_{SSL} = \sqrt{\beta}R_{out}$ .

### B. Types of losses

The intrinsic losses in the converter depend solely on the conversion ratio and load current of the converter, and is completely independent of the  $\beta$  value:

$$P_{R_{out}} = R_{out} \cdot I_{load}^2 \quad (6)$$

However, the switching losses can be optimized by carefully sizing the individual components. In this paper, two sources of switching losses are considered: the gate loss of the switches, and the bottom-plate losses of the flying capacitor.

$$P_{gate} = \sum_j V_{gate,j}^2 f_{sw} C_{gate,j} \quad (7)$$

$$P_{bp} = V_{out}^2 f_{sw} C_{bp} \quad (8)$$

The parasitic bottom-plate capacitance of the flying capacitor can be described as  $C_{bp} = \alpha C_{fly}$ , where the ratio  $\alpha$  depends on the chosen type of capacitor. The parasitic gate capacitance of each switch can be assumed to increase linearly with the gate area, ideally making it inversely proportional to the on-resistance for a given gate length. The switching frequency can

be described as a function of  $C_{fly}$  and  $C_{out}$  by rearranging (4):

$$f_{sw} = \frac{C_{out}}{C_{out} + C_{fly}} \cdot \frac{1}{4C_{fly}\sqrt{\beta}R_{out}} \quad (9)$$

The switching losses can now be described as

$$P_{gate} = \sum_j V_{gate,j}^2 \frac{C_{out}}{C_{out} + C_{fly}} \cdot \frac{1}{4C_{fly}\sqrt{\beta}R_{out}} \cdot \frac{C_{gate,j}^* f_j}{\sqrt{1-\beta}R_{out}} \quad (10)$$

$$P_{bp} = V_{out}^2 \frac{C_{out}}{C_{out} + C_{fly}} \cdot \frac{1}{4\sqrt{\beta}R_{out}} \alpha \quad (11)$$

Where  $C_{gate,j}^*$  is the gate capacitance per unit gate width for each switch, and  $f_j$  is a function related to the width-resistance product of each switch.

The total power loss in the converter is given by the sum of all three types of losses, where  $\beta$  have great influence:

$$P_{loss} = P_{gate} + P_{bp} + P_{R_{out}} \Leftrightarrow \quad (12)$$

$$P_{loss} = \left( \frac{K_1}{C_{fly}} \cdot \frac{1}{\sqrt{\beta}\sqrt{1-\beta}} + K_2 \cdot \frac{1}{\sqrt{\beta}} \right) \frac{C_{out}}{C_{out} + C_{fly}} + K_3 \quad (13)$$

Where the constants  $K_{1-3}$  depend on topology and component types:

$$K_1 = \frac{1}{4R_{out}^2} \sum_j V_{gate,j}^2 C_{gate,j} f_j \quad (14)$$

$$K_2 = \alpha \frac{V_{out}^2}{4R_{out}} \quad (15)$$

$$K_3 = R_{out} I_{load}^2 \quad (16)$$

For a given set of capacitor sizes, an optimal value of  $\beta$  can be found.

### C. Choice of component types

1) *Switches*: Four switches are used in the converter, and the total on-resistance for each pair of synchronized switches should be  $\sqrt{1-\beta}R_{out}$ . However, the topology causes some of the switches to have a positive source-bulk voltage and the switches will therefore have lower driving voltages and higher threshold voltages due to the body effect, causing large differences in the conductance-width ratios of the transistors.

The topology requires switches  $S_1$  and  $S_4$  to be implemented using PMOS and NMOS transistors respectively, while  $S_3$  and  $S_2$  are implemented with NMOS transistors to be minimize the required gate area. In order for the transistor blocks to have the same total length in the layout, the NMOS transistors are made with 50 fingers, while the PMOS is made up by 48 fingers. The conductance of each transistor is simulated at the minimum driving voltage as a function of transistor width.  $S_2$  and  $S_3$  have a source-bulk voltage equivalent to  $V_{out}$  giving them a minimum  $V_{gs}$  of 635 mV, while transistors 1 and 4 have  $V_{gs}$  equal to the input voltage, giving a minimum value of 1.235 V.

Knowing the relationship between gate width and conductance for each transistor, the distribution of resistance that requires the smallest total transistor area for any given value of  $\sqrt{1-\beta}R_{out}$  can be easily be computed with a script, determining the  $f_j$  values.

Simulated values of the gate capacitances at minimum drive voltages can be seen in Table II. Due to the source-bulk bias, the gate capacitances of  $S_{2-3}$  are different from that of  $S_4$ .

Transistor	$S_1$	$S_2$	$S_3$	$S_4$
$C_{gate}^*$	1003 aF/ $\mu\text{m}$	2630 aF/ $\mu\text{m}$	2630 aF/ $\mu\text{m}$	682 aF/ $\mu\text{m}$

TABLE II. SIMULATED GATE CAPACITANCES

2) *Capacitors*: In the used technology, 3 different types of capacitors are available: MIM, DualMIM and MOS. Through simulations, the capacitance and  $\alpha$  of each type has been determined for different sizes. These values are shown in Table III for effective areas of 300 and 10,000  $\mu\text{m}^2$ , the largest areas for MOS and MIM/DualMIM capacitors allowed in the technology. The DualMIM capacitors are superior to MIM on both parameters. While the MOS capacitor does have a higher capacitance density, the significantly larger value of  $\alpha$  makes it unsuited for use as a flying capacitor. The MOS capacitors could possibly be used as output capacitance, since the parasitic capacitance is only beneficial for this purpose. However, for simplicity DualMIM is used for all capacitors as the difference in capacitance density is small. To simplify calculations, the capacitors are considered to consist of units with an effective area of  $10^4 \mu\text{m}^2$  and capacitance  $C_{unit} = 44$  pF.

	$A_{eff} = 10^4 \mu\text{m}^2$		$A_{eff} = 300 \mu\text{m}^2$	
	$C$ /pF	$\alpha$ /%	$C$ /pF	$\alpha$ /%
MIM	20	0.83	0.6	1.5
DualMIM	44	0.47	1.8	1.0
MOS	-	-	2.4	4.2

TABLE III. COMPARISON OF AVAILABLE CAPACITOR TYPES.

#### D. Optimization

For a given set of capacitor sizes, the value  $\beta$  that gives the minimum power loss can now be determined numerically. As seen in Fig. 3, the optimal value increases with the capacitor size, meaning that with an increase in flying capacitance, the switches should also be made larger.

### III. CHIP AREA CONSIDERATIONS

Most of the total chip area is used for the capacitors, meaning that the most effective way to reduce the size of the converter is to reduce the amount of capacitance. However, as indicated earlier, a smaller flying capacitance will reduce the efficiency of the converter as the switching losses will increase. A smaller output capacitance, on the other hand, will reduce both the losses and the converter size.

#### A. Output capacitance

The required amount of output capacitance is related to the switching frequency and allowed voltage ripple. As described in [3] the needed output capacitance can easily be estimated by considering the SSL case of converter operation. For the voltage divider, (17) can be used to find a size for  $C_{out}$ .  $1/\zeta$  is the fraction of charge trough each switch, and as stated in Table I the allowed voltage ripple,  $\Delta v$ , is 10mV.

$$C_{out} + C_{fly} = \frac{I_{load}}{\Delta v_{out}} \cdot \frac{1}{\zeta f_{sw}} \quad (17)$$

Combining this with (9), the output capacitance can be determined as a function of the flying capacitance, as seen in (18).

$$C_{out} = C_{fly} \cdot \frac{4I_{load}\sqrt{\beta}R_{out}}{\Delta v_{out}\zeta} \quad (18)$$

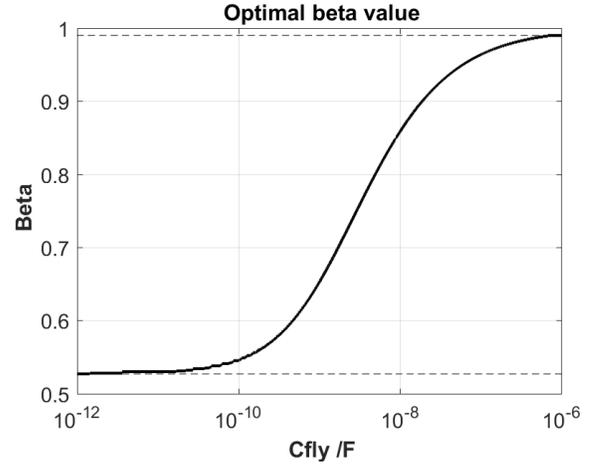


Fig. 3. Optimal  $\beta$  value vs. capacitor size for 3nf output capacitance and minimum input voltage. Dashed lines mark asymptotic values.

This means that the required output capacitance for a given flying capacitance can be reduced by an increase in  $\zeta$ . As described in [3], this can be achieved by means of fragmentation and phase interleaving.

#### B. Multiphase interleaving

By splitting the converter into several phases, the size of the output capacitance can be decreased without exceeding the allowed voltage ripple. By this method, the power density and efficiency of the converter can be improved significantly, as demonstrated in [6]. For a converter with  $n_P$  interleaved phases we have  $\zeta = 2n_P$ , and the output capacitance can be reduced by a factor  $n_P$  compared to the single-phase case. As seen in (9) this will also allow the converter to operate at a lower switching frequency and thus reduce the switching losses in the converter output stage. The flying capacitor and each of the switches are separated into  $n_P$  fragments of equal size, all switches has a duty cycle of 50% and the phases are shifted  $\frac{180}{n_P}$  degrees from each other.

#### C. Total chip area

The total area for each component is slightly larger than their effective areas. For a transistor with a gate length of 180 nm, width  $W$  and  $n$  fingers, the total area for NMOS and PMOS components are described by the following equations.

$$A_{PMOS} = \left( \frac{W}{n} + 840 \text{ nm} \right) \cdot (700 \text{ nm} \cdot n + 1240 \text{ nm}) \quad (19)$$

$$A_{NMOS} = \left( \frac{W}{n} + 480 \text{ nm} \right) \cdot (700 \text{ nm} \cdot n + 400 \text{ nm}) \quad (20)$$

In the used design, the transistors are implemented with 48 and 50 fingers for p- and n-type transistors respectively.

The total area for each capacitor unit with an effective area of  $10^4 \mu\text{m}^2$ ,  $A_{capunit}$ , is  $1.41 \cdot 10^4 \mu\text{m}^2$ . The total area of each capacitor is estimated as  $\frac{C}{C_{unit}} \cdot A_{capunit}$ .

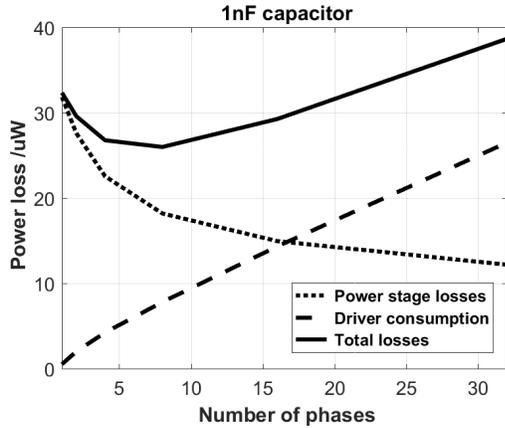


Fig. 4. Power loss vs. number of phases for  $C_{fly} = 1$  nF

#### IV. EFFICIENCY CALCULATIONS

##### A. Power stage

Combining (10), (11) and (18), expressions for the power stage switching losses for a converter with  $n_P$  interleaved phases can be written:

$$P_{gate} = \frac{1}{4\sqrt{\beta}R_{out} + \frac{\Delta v_{out}}{I_{load}}2n_P} \frac{\sum_j v_{gate,j}^2 C_{gate,j}^* f_j}{\sqrt{1 - \beta}R_{out}C_{fly}} \quad (21)$$

$$P_{bp} = V_{out}^2 \alpha \frac{1}{4\sqrt{\beta}R_{out} + \frac{\Delta v_{out}}{I_{load}}2n_P} \quad (22)$$

The intrinsic losses are given by (6), and are independent of both  $n_P$ ,  $\beta$  and  $C_{fly}$ .

These equations indicate that a sufficiently large number of interleaved phases will make the switching losses insignificant, leaving only the intrinsic losses. However, the increased number of phases will require a more complicated gate driver circuit with increased power consumption.

##### B. Clock consumption

In order to drive the switches a digital clock interleaver is used, similarly to [7]. For an  $n_P$ -phase converter, a  $\frac{1}{2^{n_P}}$  clock-divider consisting of  $n_P$  flip-flops is used followed by  $n_P - 1$  additional flipflops for phase-shifting the divided clock signal. This circuit is capable of delivering shifted clock signals to any number of phases that is a power of 2.

The power consumption of the clock interleaver will increase with the number of phases. The power consumption has been estimated through schematic level simulations in Cadence with BSIM3V3-Models. Simulations show that the power consumption of the clock interleaver can be estimated by (23).

$$P_{clk} = f_{sw} \cdot (31.16 \text{ fJ} \cdot n_P^2 + 183.5 \text{ fJ} \cdot n_P - 132.2 \text{ fJ}) \quad (23)$$

Combining this with (21) and (22) it is possible to determine the optimal number of phases for a given capacitor size.

Figure 4 show the total power loss, as well as the separate losses for the clocking circuit and the power stage, as a

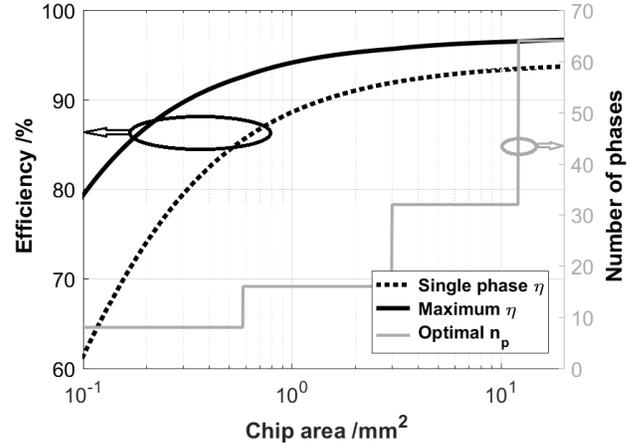


Fig. 5. Efficiency comparison of single-phase converter and a converter with optimal  $n_p$  along with the optimal value of  $n_p$  for varying chip area

function of the number of phases for a converter with  $C_{fly} = 1$  nF.

The power consumption of the clock circuit would be lower in smaller process-nodes, increasing the optimum number of phases and the total efficiency of the converter.

Using a script, the optimal number of phases for each value of  $C_{fly}$  is found. This number increases with the capacitor size, as larger capacitors reduce the switching frequency and the power consumption of the clock interleaver.

Since the area of the clock interleaver is assumed to be much smaller than that of the output stage, it is not included in the estimate of the chip area.

##### C. Area and efficiency

Having determined the optimal number of phases and  $\beta$ -value for any value of  $C_{fly}$  as well as the total chip area as a function of  $C_{fly}$  and the number of phases, the maximum efficiency for any chip area can be estimated. Figure 5 shows the maximum- and single-phase efficiency as well as the optimal number of phases as a function of chip area at the minimum input voltage.

#### V. CONCLUSION

Design consideration for the SC converter were described, and the components of the converter were optimized for minimizing the switching losses at minimum input voltage. A method for determining the optimal number of interleaved phases for any size of flying capacitor has been developed, and the maximum converter efficiency for any silicon chip area has been determined.

The use of interleaved phases has been shown to improve the converter efficiency by several percent, achieving a theoretical efficiency of more than 94% for a chip area of 1 mm<sup>2</sup>.

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