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*Published in:*

Proceedings of IEEE 2016 12th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)

*Publication date:*

2016

*Document Version*

Peer reviewed version

[Link back to DTU Orbit](#)

*Citation (APA):*

Fan, L., Knott, A., & Jørgensen, I. H. H. (2016). Layout Capacitive Coupling and Structure Impacts on Integrated High Voltage Power MOSFETs. In *Proceedings of IEEE 2016 12th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)* IEEE.

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# Layout Capacitive Coupling and Structure Impacts on Integrated High Voltage Power MOSFETs

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**Abstract**—The switching performances of the integrated high voltage power MOSFETs that have prevailing interconnection matrices are being heavily influenced by the parasitic capacitive coupling of on-chip metal wires. The mechanism of the side-by-side coupling is generally known, however, the layer-to-layer coupling and the comparison of the layout impacts have not been well established. This paper presents modeling of parasitic mutual coupling to analyze the parasitic capacitance directly coupled between two on-chip metal wires. The accurate 3D field solver analysis for the comparable dimensions shows that the layer-to-layer coupling can contribute higher impacts than the well-known side-by-side coupling. Four layout structures are then proposed and implemented in a 0.18  $\mu\text{m}$  partial SOI process for 100 V integrated power MOSFETs with a die area 2.31  $\text{mm}^2$ . The post-layout comparison using an industrial 2D extraction tool shows that the side-by-side coupling dominated structure can perform better than the layer-to-layer coupling dominated structure, in terms of on-resistance times input or output capacitance, by 9.2% and 4.9%, respectively.

**Keywords**—integrated circuit interconnections; layout; mutual coupling; parasitic capacitance; power MOSFET

## I. INTRODUCTION

The miniaturization trend of power electronics requires reductions in size [1], and one of the principle approaches is to integrate active components on-chip, such as power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) in SOI (Silicon on Insulator) processes [2] or in nonstandard high-voltage CMOS (Complementary Metal-Oxide-Semiconductor) processes [3]. As the process technologies keep developing, the electrical parameters of on-chip interconnections are becoming the real bottleneck of circuit performances [4], especially for high-power-density converters [5]. The coupling capacitance can be measured on-chip but the accuracy suffers from the supply noise [6]. Section II presents modeling of parasitic mutual coupling of on-chip metal wires, from which the capacitive coupling directly between the wires is specifically analyzed with post-layout 2D extractions and 3D field solvers.

The capacitive coupling of interconnections is embedded in the layout structures of high voltage power MOSFETs. The previously investigated structures such as overlapping circular-gate structure [7], octagonal structure [8], hexagonal structure

[9], waffle-shaped structure [10], and hybrid waffle structure [11] are commonly not permitted by the polysilicon DRC (Design Rule Check) rules in deep submicron processes. The waffle-shaped structure with the angled non-symmetrical connections leads to current unbalance and is therefore not optimal for high current applications [10]. Taking into account the substrate contacts and the guarding rings between the active areas, especially when the waffle structure is actually an effective trade-off between the metal interconnections and the active area [11], the high active area density cannot be a single FOM (Figure of Merit) of a layout structure. Nevertheless, a common principle underneath all the structure improvements is about sharing active areas and/or interconnections in all geometrical directions. In section III, four layout structures are proposed and implemented in a 0.18  $\mu\text{m}$  partial SOI process for 100 V power MOSFETs. In Section IV, the post-layout results are compared and discussed. Section V concludes the paper.

## II. LAYOUT CAPACITIVE COUPLING

### A. Modeling of Parasitic Mutual Coupling

At the schematic level, wires are ideal electrical paths connecting different nodes that have the same net name. However, the wires in integrated circuit layouts are normally made by metal (polysilicon is another example with high sheet resistance), and the distances between the on-chip metal wires are generally in  $\mu\text{m}$  range, resulting in unavoidable mutual capacitive coupling. The modeling of two closely placed on-chip metal wires (*A* and *B*) is shown in Fig. 1. All the components result from the parasitic effects of the layouts.

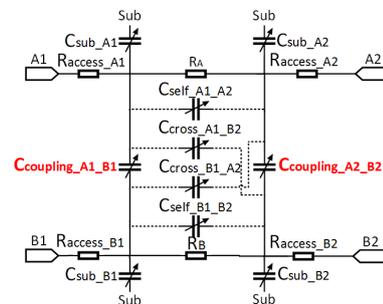


Fig. 1. Modeling of two closely placed on-chip metal wires (mutual coupling from either side-by-side or layer-to-layer). All components are parasitic.

Wire  $A$  is connecting the nodes  $A1$  and  $A2$ , and wire  $B$  is connecting the nodes  $B1$  and  $B2$ .  $R_A$  and  $R_B$  are the intrinsic parasitic resistance of each metal wire. The four  $R_{access}$  represent the parasitic resistance coming from the physical pins to access the real metal wires, where the resistance values are normally less than 1 m $\Omega$ . The four  $C_{sub}$  are the intrinsic parasitic capacitances to the substrate, where the capacitance values are growing with increased length or width. It can also be shown that for the same dimensions, a metal wire located in a lower layer such as *Metal1* (abbreviated as  $M1$  and for the rest of the paper) presents higher intrinsic parasitic capacitance to the substrate, than the associated one if the same wire is located in an upper layer. The modeling in Fig. 1 has a symmetrical structure. The main focus of this paper is the two direct coupling capacitors  $C_{coupling}$ . There are other mutual coupling capacitors  $C_{self}$  and  $C_{cross}$ , which are illustrated with dash lines, representing the fact that when the metal wires are very wide but short in length, there could be mutual coupling between the two nodes of the same wire and cross coupling between non-adjacent nodes that cannot be lumped into  $C_{coupling}$ . These capacitance values are extracted as well and generally much smaller than  $C_{coupling}$ .

### B. Side-by-Side Capacitive Coupling of Metal Wires

The coupling capacitors  $C_{coupling\_A1\_B1}$  and  $C_{coupling\_A2\_B2}$  (in Fig. 1) are not lumped due to the symmetrical structure and the parasitic resistance in between. To reflect the coupling effect, the average value of the two is used. The capacitive coupling between the two side-by-side metal wires located in the same layer has been simulated with the actual layouts using a 2D extraction tool and a 3D field solver (i.e. Calibre xRC and Calibre xACT 3D with high accuracy mode, respectively), and the corresponding results are shown in Fig. 2. Note, it is assumed that there is no power/ground plane above the metal wires (much more expensive to possess on-chip compared to PCB case), and there is global substrate underneath, so that the results are reproducible and not case-dependent. The dimensions of the side-by-side metal wires are defined in Fig. 2(a).  $T$  is the metal thickness.  $S$  is the spacing distance.  $W$  is the common metal width.  $L$  is the common metal length. The reference dimensions of a single metal wire are  $T$  of 555 nm,  $W$  of 0.5  $\mu\text{m}$ ,  $L$  of 5  $\mu\text{m}$ , and  $S$  of 0.5  $\mu\text{m}$ , if not otherwise specified. If the metal wire is located in  $M3$  layer in the used process, then the resulting parasitic resistance is approximately 1  $\Omega$ . There are 5 metal layers available to use with the chosen process modules. The top metal layer  $Mtop$  is generally thicker than the other lower layers to reduce the metal sheet resistance (the  $Mtop$  thickness used is 975 nm), however, this leads to increased capacitive coupling which is shown in Fig. 2(b). The capacitive coupling decreases with increased spacing between the two metal wires, and it is shown in Fig. 2(c). The 2D extraction results are flat out for very small spacing values, due to the extractions limited by the DRC rules. For 100 V side-by-side operations, the spacing  $S$  in excess of 1  $\mu\text{m}$  is generally recommended for all metal layers. The capacitive coupling increases with the width  $W$ , while keeping the same spacing  $S$ , as shown in Fig. 2(d). The 2D extraction results are accurate for small  $W$  values, however, as  $W$  increases,  $C_{coupling}$  becomes more underestimated, mainly because  $C_{self}$  of the same metal wire is increasingly overestimated instead.

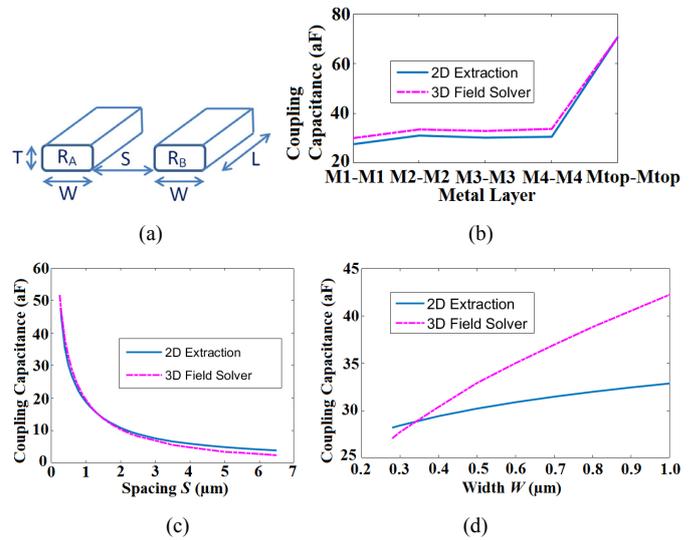


Fig. 2. Side-by-side capacitive coupling. (a) Definition of dimensions. (b) Versus metal layers. (c) Versus  $S$  ( $M3$ - $M3$ ). (d) Versus  $W$  ( $M3$ - $M3$ ).

### C. Layer-to-Layer Capacitive Coupling of Metal Wires

The two metal wires that are located in separate layers can still suffer from capacitive coupling to each other, because of the electric field penetrating the dielectric between the metal layers. The definitions of the dimensions in this case are shown in Fig. 3(a).  $T$  is the metal thickness and  $D$  is the dielectric thickness.  $O$  is the offset distance in the vertical direction.  $W$  and  $L$  are the common metal width and length, respectively. The values of  $T$  and  $D$  can vary between different metal layers even for the same process. Fig. 3(b) shows that the capacitive coupling resulting from the layer-to-layer effects is approximately the same for different metal layers. When the two metal wires have zero offset  $O$  meaning that they are exactly overlapping each other in the vertical direction, the capacitive coupling is strongest in this case, then as  $O$  increases, the capacitive coupling gradually decreases, as shown in Fig. 3(c).

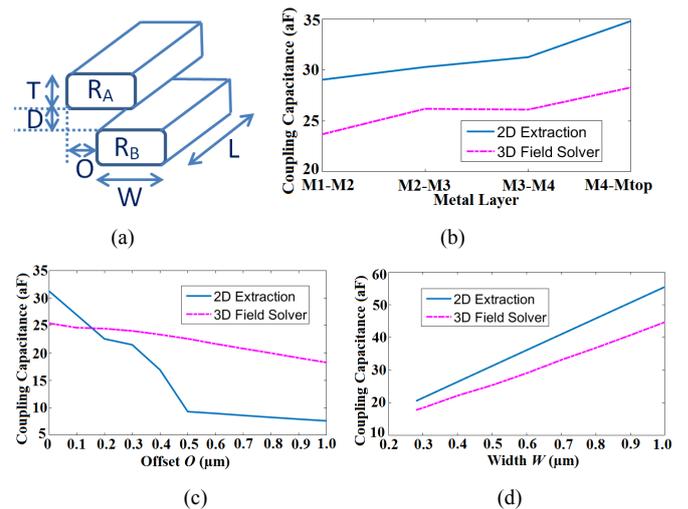


Fig. 3. Layer-to-layer capacitive coupling. (a) Definition of dimensions. (b) Versus metal layers ( $O = 0$ ). (c) Versus  $O$  ( $M3$ - $M4$ ). (d) Versus  $W$  ( $M3$ - $M4$ ).

The capacitive coupling directly between the two metal wires in  $M3$  and  $M4$  becomes stronger as the common width  $W$  increases, and this is shown in Fig. 3(d). In Fig. 3, the common discrepancies between the results of the 2D extraction and the 3D field solver are mainly due to the fact that the 2D extraction tool tends to have unbalanced solutions for the mutual coupling capacitance  $C_{self}$  in the layer-to-layer coupling case and have discontinuous solutions for certain geometrical dimensions. Despite this, the 2D extraction results are still accurate for small offset values and start to converge with the 3D field solver results after the two metal wires are actually moved away in the vertical direction. The 3D field solver is the most accurate and cost-effective way to investigate the capacitive coupling effects, and by comparing the results, it shows that the layer-to-layer capacitive coupling is in the same order or even higher than the side-by-side capacitive coupling, when the metal wires and the dielectric have the comparable dimensions.

### III. PROPOSED LAYOUT STRUCTURES

For the layout structures of integrated high voltage power MOSFETs, a highly compact layout is more difficult to achieve, compared to low-power MOSFETs. On the side of the drain diffusion, the voltage potential is uniformly distributed, thus the corresponding isolation structures can be overlapped. However, there is no uniform potential along the side of the device from the drain diffusion to the source diffusion, and the distributed electric field needs to be properly terminated. Therefore, the associated isolation structures surrounding these edges result in a less achievable device density.

The four proposed layout structures for high voltage power MOSFETs are shown in Fig. 4. The main principles are demonstrated and the real layout implementation is limited by various DRC rules. The gate network is mainly routed in  $M2$  layer and the power distribution is basically achieved in  $M_{top}$  layer. These two and other nearly forty layers are left out on purpose, so that the major capacitive coupling structure between the drain network and the source network can be shown for clarity. In Fig. 4(a), the drain/source connections are lateral stacks of two adjacent metal layers, i.e.  $M3$  and  $M4$ , and the capacitive coupling is mainly dominated by the side-by-side coupling mechanism. The drain/source connections in Fig. 4(b) are laterally routed on different metal layers ( $M3$  and  $M4$ ), thus the capacitive coupling is mainly induced by the layer-to-layer coupling mechanism. The perpendicular mesh structure in Fig. 4(c) can be viewed as a trade-off between parasitic resistances and capacitances, and the resulting parasitic effects depend on the specific geometrical dimensions. Fig. 4(d) serves as a layout structure where the bulk is constructed as a separate terminal, and the Nwell metal strap connections need to be chopped into pieces to make the bulk network route through and reach the chip pad.

### IV. POST-LAYOUT COMPARISONS AND DISCUSSIONS

The comparison of the four proposed layout structures is summarized in Table I. The high voltage power MOSFETs are implemented in a 0.18  $\mu\text{m}$  partial SOI process. The maximum operation voltage between the drain and the source is 100 V, and that between the gate and the source is 5.5 V.

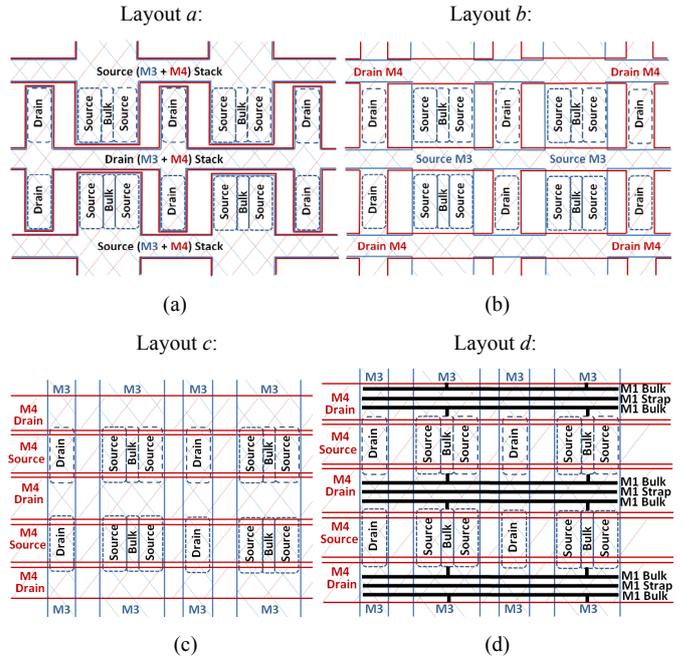


Fig. 4. Proposed layout structures for integrated high voltage power MOSFETs. (a) Drain/source horizontal connection, metal layers stack, mainly side-by-side coupling. (b) Drain/source horizontal connection, on separate metal layers, mainly layer-to-layer coupling. (c) Drain/source vertical connection, perpendicular mesh structure, coupling by geometries. (d) Drain/source structure the same as (c) but with the bulk as a separate terminal.

$$\left(\frac{W}{L}\right)_a = \left(\frac{W}{L}\right)_b = 2 \cdot \left(\frac{W}{L}\right)_c = 2 \cdot \left(\frac{W}{L}\right)_d = 38400 \quad (1)$$

TABLE I. LAYOUT STRUCTURES COMPARISON

R/C	Top chip-level (including chip-pads and ESD protections)					
	Schematic <i>a &amp; b</i>	Post-Layout <i>a</i>	Post-Layout <i>b</i>	Schematic <i>c &amp; d</i>	Post-Layout <i>c</i>	Post-Layout <i>d</i>
Parasitic	No	2D Extract	2D Extract	No	2D Extract	2D Extract
$R_{ds(on)}$ ( $\Omega$ ) <sup>a</sup>	1.542	2.071	2.250	3.085	3.354	3.295
$C_{g-sb}$ (pF) <sup>b</sup>	21.3	46.9	49.5	11.5	25.1	26.7
$C_{gd}$ (pF) <sup>b</sup>	38.1	41.4	39.3	19.1	20.6	20.6
$C_{iss}$ (pF) <sup>b</sup>	59.4	92.7	93.2	30.6	48.0	48.9
$C_{d-sb}$ (pF) <sup>c</sup>	72.1	88.4	85.7	36.0	47.6	48.0
$C_{dg}$ (pF) <sup>c</sup>	38.1	41.4	39.3	19.1	20.6	20.6
$C_{oss}$ (pF) <sup>c</sup>	110.2	132.1	127.6	55.1	69.5	69.8
$R_{ds(on)}$ - $C_{iss}$ (ps)	91.6	192.0	209.7	94.4	161.0	161.1
$R_{ds(on)}$ - $C_{oss}$ (ps)	169.9	273.6	287.1	170.0	233.1	230.0

<sup>a</sup>  $V_{G-SB} = 5$  V,  $V_{DS} = 0.1$  V,  $T = 27$  C, typical process corner.

<sup>b</sup> Test signals into the gate terminal,  $V_G = V_D = V_B = V_S = 0$  V,  $T = 27$  C, typical process corner.

<sup>c</sup> Test signals into the drain terminal,  $V_G = V_D = V_B = V_S = 0$  V,  $T = 27$  C, typical process corner.

The designed ( $W/L$ ) ratios of the four layout structures are according to (1).  $W$  is the effective total gate width, and  $L$  is the channel length. The minimum channel length of  $0.5\ \mu\text{m}$  is chosen for the used process. The top chip-level post-layout parasitic resistances and capacitances are extracted using an industrial 2D extraction tool (Calibre xRC). The 3D field solver is generally not applicable to complicated layout networks, due to its demanding computational requirements. Therefore, the 2D extractions are commonly used in industry, and the extracted results are still meaningful for comparison between topologies. The full details of the modeling, simulation, and extraction of the equivalent nonlinear parasitic parameters of the high voltage power MOSFETs can be found in [2]. A testing frequency of 1 MHz is used as it is the industrial standard measurement frequency [12], [13]. For each structure, the electrostatic discharge (ESD) protection circuits add 1.3-1.8 pF extra parasitic capacitance between the gate and the source terminals (nonlinear voltage dependent).

First, all of the post-layout parameters are much worse than those at the schematic level, which means that the overall performances are heavily impacted or even dominated by the parasitic parameters of the interconnections, rather than the intrinsic transistor parameters. Second, using the products of on-resistance and input or output capacitance as indicators, the side-by-side coupling dominated layout  $a$  is actually better than the layer-to-layer coupling dominated layout  $b$ , by 9.2% and 4.9%, respectively. Even though  $C_{d-sb}$  of layout  $b$  is lower, more metal is spent for the source on  $M3$  thus  $C_{g-sb}$  is higher due to the layer-to-layer coupling with  $M2$ , and the parasitic resistance is higher than the metal stack layout  $a$ . Third, the layouts  $c$  and  $d$  may better fit the high frequency converters where the switching loss is dominated. The lower capacitance is one concern. The part of the on-resistance contributed by the interconnections becomes larger as the transistor sizes increase, rather than inversely scaling with the transistor sizes, i.e. it is a trade-off between  $R$  and  $C$ , but not simply with a  $RC$  constant.

The parasitic coupling capacitance of the interconnections is always superposed on the intrinsic nonlinear parasitic capacitance of the power MOSFETs, and the nonlinearity of the overall total capacitance tends to be reduced in terms of the voltage-dependent capacitance variations becoming relatively less. This kind of linearization may benefit high frequency switching applications, and it is previously investigated with on-die capacitor [14] and external capacitor [15].

The layout of the entire chip design is shown in Fig. 5, and the four proposed layout structures are highlighted with the white color boxes. The die area is  $2.31\ \text{mm}^2$  ( $1520\ \mu\text{m} \times 1520\ \mu\text{m}$ ). The silicon design has been sent to fabrication.

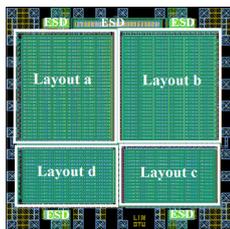


Fig. 5. Layout of the chip design (proposed structures are highlighted).

## V. CONCLUSIONS

The modeling of parasitic mutual coupling of on-chip metal wires is presented, and the capacitive coupling is specifically analyzed for different geometrical dimensions with post-layout 2D extractions and 3D field solvers. It shows that the layer-to-layer coupling can have more impacts than the side-by-side coupling. Four layout structures for 100 V integrated power MOSFETs are proposed and implemented in a  $0.18\ \mu\text{m}$  partial SOI process. The post-layout performances reveal that the side-by-side coupling dominated structure can improve  $R_{ds(on)} \cdot C_{iss}$  by 9.2% and  $R_{ds(on)} \cdot C_{oss}$  by 4.9%. The trade-off between  $R$  and  $C$  depends on the specific applications.

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