



## Infinite Etching Selectivity with Conventional Photoresist in a Bosch Process

Chang, Bingdong; Leussink, Pele; Jensen, Flemming; Hübner, Jörg; Jansen, Henri

*Publication date:*  
2017

*Document Version*  
Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

*Citation (APA):*

Chang, B., Leussink, P., Jensen, F., Hübner, J., & Jansen, H. (2017). *Infinite Etching Selectivity with Conventional Photoresist in a Bosch Process*. Abstract from 43rd International conference on Micro and Nano Engineering, Braga, Portugal.

---

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

## Infinite Etching Selectivity with Conventional Photoresist in a Bosch Process

Bingdong Chang <sup>a</sup>, Pele Leussink <sup>b</sup>, Flemming Jensen <sup>a</sup>, Jörg Hübner <sup>a</sup>, Henri Jansen <sup>a</sup>

<sup>a</sup> DTU Danchip, Technical University of Denmark, Kgs Lyngby, 2800, Denmark

<sup>b</sup> MESA+ Research Institute, University of Twente, the Netherlands

e-mail: henrija@dtu.dk

Keywords: Silicon plasma etching, infinite selectivity, Bosch sequence

Nowadays, deep reactive ion etching (DRIE) has become a standard technology to transfer patterns directionally into silicon, but to achieve high aspect ratios remains challenging. By performing a pulsed process (e.g. a Bosch sequence), the sidewall of trenches can be protected during an etch process and the etch depth can be significantly improved. However, when etch depth increases, the silicon etch rate is limited by RIE lag [1], while the mask is consumed with an almost constant rate. This means that the selectivity (etch rate of silicon divided by etch rate of mask) drops drastically when aspect ratio increases and in the end masks will be totally eroded away. This issue sets a limit for high aspect ratio etching and a lot of efforts have been invested to find a “hard” mask with a high selectivity, e.g. Cr, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, etc. [2]. However, a hard mask can be sputtered during etching and creates roughness. Furthermore, the transfer of resist patterns into the hard mask will increase fabrication complexity.

Here we report a reproducible method to achieve an infinite etching selectivity with a conventional DUV photoresist (JSR KRF M230Y). Etching was performed with a Pegasus DRIE tool (SPTS). Passivation time was kept to be 1.5s, while etching time was carefully tuned using the parameter ramping feature, so that the scallop sizes are almost the same along the trench for different numbers of cycles, other parameters we used are shown in table 1. Etching profiles were inspected with SEM.

The reason why an infinite selectivity is achieved is not because of intrinsic properties of photoresist, which typically results in selectivity of around 100 or less [3]. It's because of the non-conformal fluorocarbon (FC) deposition inside etched structures, which protects the mask. The mechanism is shown briefly in Fig.1. Firstly, silicon is etched isotropically using SF<sub>6</sub> plasma (Fig.1.1 and Fig.1.2). Secondly, C<sub>4</sub>F<sub>8</sub> is applied for passivation (Fig.1.3). Due to depletion of species inside the trenches, the thickness of FC film is thicker on top of resist compared with the bottom of the trench. Then the FC film is removed directionally with a bias. If bias is applied just enough for clearing the bottom of the trench, the resist will be still covered by some FC film (Fig.1.4). Thus when the etch process goes on to next cycles, resist will always be protected (Fig.1.5 and Fig.1.6).

To demonstrate this extraordinary ability, wafers were prepared with 65nm bottom anti-reflective coating (BARC) and 300nm conventional DUV resist and patterned by DUV stepper lithography with 1 micron sized features. After etching the BARC layer, 50 cycles were performed to reach an etch depth of 18.8μm (Fig.2.a), while the resist remained intact (Fig.3.a). After 100 cycles, the etch depth was doubled and the resist still undisturbed (Fig.2.b). Noticeably, a FC layer starts to develop covering the topside of the etching structure making the trench opening smaller (Fig.3.b). When we increased the number of cycles further to 150, the etching depth was around 58.1μm, which implied a high aspect ratio of more than 50, while the sidewall of the trench started to be corroded (Fig.2.c).

In conclusion, by carefully tuning a pulsed process, silicon can be etched directionally with infinite selectivity towards conventional photoresists; i.e. resist is not consumed at all. Obviously any mask (e.g. Cr, SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>), even though not demonstrated here, will be able to perform this task as well. The process is believed to be the key to realize ultrahigh aspect ratio structures with ordinary masking.

		Passivation 1.5s	Etching 3.5s
Gas flow (sccm)	C <sub>4</sub> F <sub>8</sub>	300	5
	SF <sub>6</sub>	15	600
	Ar	200	250
Generators (W)	Coil	3000	
	Platen	1	75

Table 1. DRIE parameters.

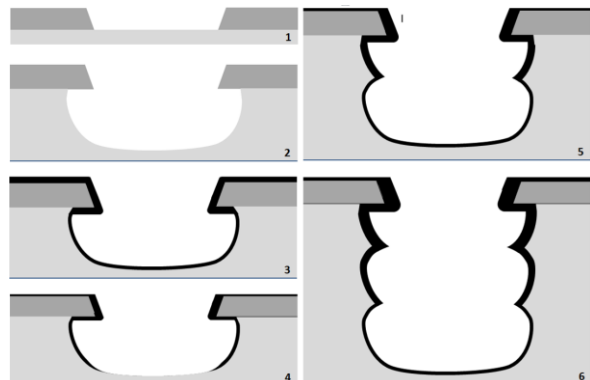


Figure 1. Schematic of first few Bosch cycles during which silicon is etched no photoresist attack.

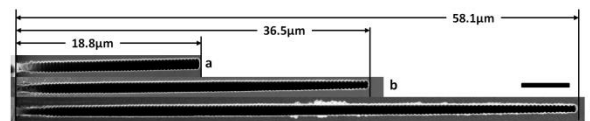


Figure 2. Etch profile evolution (scale bar: 5μm): a) 50 cycles; b) 100 cycles; c) 150 cycles.

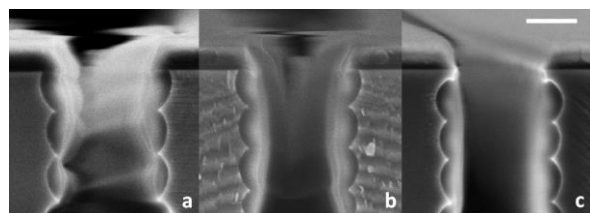


Figure 3. FC film deposition on resist when increasing total etch cycles of Bosch process (scale bar: 500nm): a) 50 cycles; b) 100 cycles; d) 150 cycles.

[1] R. Gottscho, C. Jurgensen, and D. Vitkavage. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena 10.5 (1992): 2133-2147.

[2] P Mukherjee, Pran, et al. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena 25.6 (2007): 2645-2648.

[3] S. Franssila, C. Davis, M. LeVasseur, Z. Cao and L. Yobas. Handbook of Silicon Based MEMS Materials and Technologies. (2015): 356.