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**Chang, Bingdong; Leussink, Pele; Jensen, Flemming; Hübner, Jörg; Jansen, Henri**

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# RIE-lag “Correction” in Bosch Etch Process of Silicon to Enable Profile Straightness and Improved Scallop Size Distribution

Bingdong Chang <sup>a</sup>, Pele Leussink <sup>b</sup>, Flemming Jensen <sup>a</sup>, Jörg Hübner <sup>a</sup>, Henri Jansen <sup>a</sup>

<sup>a</sup> DTU Danchip, Technical University of Denmark, Kgs Lyngby, 2800, Denmark

<sup>b</sup> MESA+ Research Institute, University of Twente, the Netherlands

e-mail: henrija@dtu.dk

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The Bosch process is a standard technique in silicon micro and nanofabrication. By performing passivation and etching sequentially, patterns can be transferred directionally. At the same time, it creates well-known scallops due to the lateral etch. The scallop size typically decreases when the etching process continues, due to reactive ion etch (RIE) lag. This non-uniformity in scallop sizes is pronounced in high aspect ratio devices. We have studied the RIE-lag experimentally and by performing parameter ramping, we have substantially increased the scallop uniformity and improved the profile straightness.

In the experiment, we used an inductively coupled tool ‘Pegasus’ from SPTS. Patterns of 1 $\mu$ m lines on top a silicon wafer were prepared by DUV stepper lithography (size variation below 5%), with 300nm resist (JSR KRF M230Y) on top of a 65nm BARC layer. Etching profiles were characterized by SEM and analyzed quantitatively using Matlab.

In the first experiment, we performed 50 cycles, with 1.5s deposition and 6.0s etch time. The etch depth was 29.4 $\mu$ m measured by SEM (Fig.1.a). In the second experiment, to counteract the effect of changing scallop size and profile straightness due to RIE-lag, we used the parameter ramping feature of Pegasus. The ramped parameter was etch time that increased from 3.5s to 8.5s during processing. The other parameters were like Exp.1. The etch depth was 27.5 $\mu$ m (Fig.1.b). The etching profiles of both experiments were extracted from SEM images using Matlab (Fig.2), from which we can clearly see an increased uniformity of scallop sizes and profile straightness with respect to Exp.1.

RIE lag is a phenomenon in which etch rate depends on the opening areas of patterns, aspect ratio of the trenches and other geometrical factors [1]. Some studies explain this by ion angular distribution, which will cause depletion of ions and radicals along the trench and slow down the etching process [2]. Other studies suggest attenuated neutral transport along the trench passage to be the reason [3]. Whatever is the actual cause, when aspect ratio increases the etch rate (scallop size divided by cycle time) for both experiments decreases (Fig.3, left). While in Exp.1 the average scallop size decreases monotonically (Fig.3, right), the scallop sizes for Exp.2 remains identical (507nm with 40nm standard deviation). The etch depth as a function of time is nonlinear for both experiments (Fig.4, left), which also suggests a decreasing etch rate (slope of the curve). However, the etch depth as a function of number of cycles (Fig.4, right) is linear for Exp.2, the reason for this linear relation is explained in the paper.

In conclusion, by performing a parameter ramping during a Bosch process, we can counteract the effect of RIE-lag, and increase the uniformity of scallop sizes. Since the variance of scallop sizes has a detrimental effect on overall sidewall roughness and sidewall straightness, a higher uniformity of scallop size distribution will make the sidewall much straighter, in the same time it is also a promising method for high aspect ratio etching.

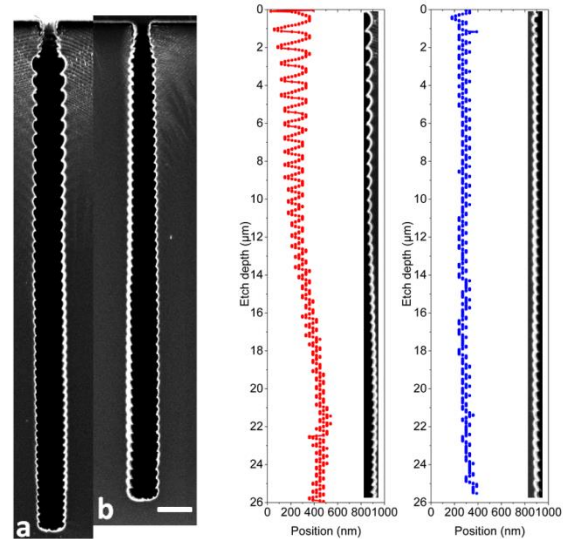


Figure 1. Etching profile of experiment 1 (a) without time ramping, and experiment 2 (b) with time ramping. (scale bar: 1 $\mu$ m)

Figure 2. Extracted etch profile from experiment 1 (left) without time ramping and from experiment 2 (right) with time ramping.

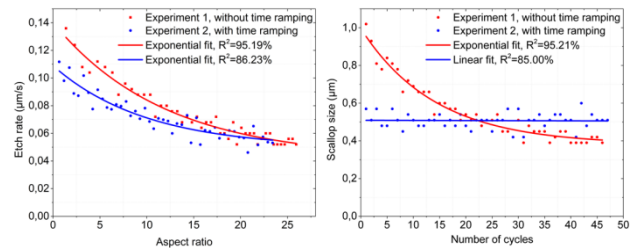


Figure 3. Etch rate as a function of aspect ratio for both experiment 1 and experiment 2 (left); scallop sizes as a function of number of cycles for both experiment 1 and experiment 2 (right).

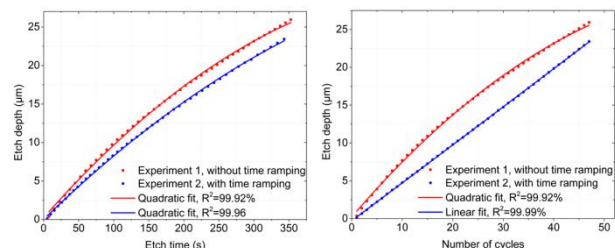


Figure 4. Etch depth as a function of etch time for both experiment 1 and experiment 2 (left); etch depth as a function of number of cycles for both experiment 1 and experiment 2 (right).

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