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Three dimensional engineering of silicon micro- and nanostructures

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Three dimensional (3D) silicon micro- and nanostructures have been an intriguing research topic in various fields, and some special properties and performances have already been demonstrated, e.g. for 3D photonic crystal structures, field effect transistors [1], biosensors. However, it is still considered to be difficult to fabricate 3D silicon structures in a reliable manner with relatively low cost. Some bottom-up approach include multiple steps of silicon deposition, patterning, and removal of silicon oxide. Easier top-down method can be achieved by a wet chemical etch, which is however difficult to integrate with traditional metal-oxide-semiconductor (CMOS) industries. By making use of the scallops formed during a so called Bosch etch process, 3D structures are demonstrated to be easy to be created, however, most of these studies still rely on oxidation and wet release after the process [2],[3], and a accurate control of the structure geometry and process is still lacked. Here we report an improved fabrication process to create 3D silicon structures in both micro- and nanoscale with good shape uniformity, and this method includes only a single-run of plasma etching process without any additional steps or post-process procedures.

The fabrication method is based on a three-step plasma etch process named DREM (deposit, remove, etch multisteps) [4], which can sculpture anisotropic silicon structures with minimum scallop size and good sidewall protection by fluorocarbon (FC) layer. A schematic view of the process parameters are shown in figure 1, during the deposition step (with C4F8) and etch step (with SF6), no bias is applied, thus a conformal coating of FC layer on the sidewall can be achieved, meanwhile minimal damage of SF6 radicals on the sidewall can be induced. Argon is applied to achieve a lower processing pressure. An additional bottom removal step is introduced, during which argon is applied with bias to remove the FC layer in the bottom, this step can reach a small processing pressure, thus a anisotropic etch profile can be achieved.

Now we have DREM process to create anisotropic silicon structures, in order to undercut the structure and make them freestanding, an isotropic etch is applied after the last cycle of DREM sequence (as shown in figure 1), during which SF6 and argon is applied without bias, thus an isotropic etch profile can be achieved, and the silicon structures are then released from the substrate. When the first sequence of DREM cycles followed by an isotropic etch is performed, the second sequence can start, and the first layer of freestanding silicon structure can act as the etch mask for following etch process. After the sequence is applied multiple times, 3D silicon structures with multiple isolated layers can be fabricated.

Figure 2 are scanning electron microscope (SEM) images of different 3D silicon microstructures. In figure 2.a and figure 2.b, 5 stacked layers are created, with the smallest structure sizes of around 2 μ m. In figure 2.b and figure 2.c, 10 stacked layers of silicon microbeams are created, the width of the beams is around 1 μ m, and the gap between two layers is 2 μ m. Figure 3 is the SEM image of a silicon based 3D photonic crystal structure, which has 6 stacked layers, the diameter of the holes is around 2 μ m, and the period is 2.5 μ m, the total area of the structures is 200 μ m by 200 μ m. Figure 4 is SEM image of 3D silicon nanowire (SiNWs) structures, the patterns are defined by electron beam lithography as shown in figure 4.a, with the smallest linewidth of 23nm, by applying the procedure for 2, 3 and 4 times, different number of stacked layers can be created which are shown in figure 4.a, figure 4.b and figure 4.c. the length of the SiNWs is 2 μ m, the gap between isolated layers is around 50nm.

In conclusion, a flexible fabrication method for 3D silicon micro- and nanostructures is presented, which only requires a single-run plasma etching process without additional procedures or post-process wet releasing. 3D structures in both micro- and nanoscale can be created easily, which gives possibilities for 3D silicon based devices and applications.

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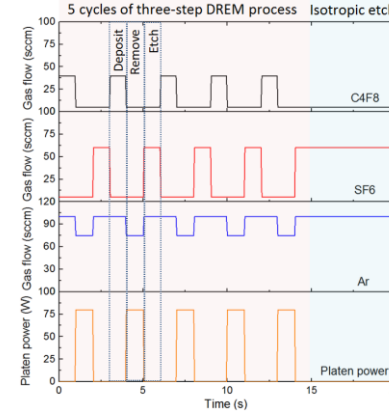


Figure 1. Insert concise explanation of figure 1 here.

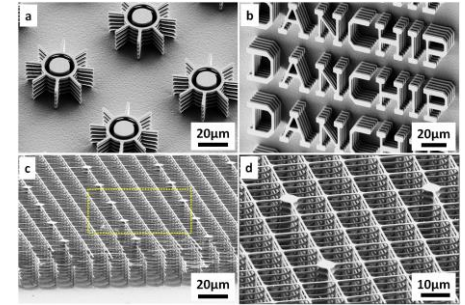


Figure 2. Some examples of 3D silicon microstructures: a) a gear-like structures; b) a logo of “Danchip”; c) silicon micro beam arrays with 10 stacked layers; d) a zoom in of c).

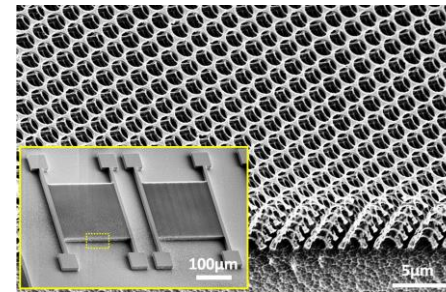


Figure 3. A large area silicon 3D photonic crystal structure with 6 stacked layers.

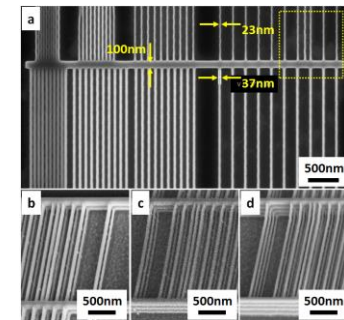


Figure 4. 3D stacked silicon nanowires: a) patterns from electron beam lithography; and after etching, b) 2 stacked layers; c) 3 stacked layers; d) 4 stacked layers