Black Silicon With Ultra-Low Surface Recombination Velocity Fabricated by Inductively Coupled Power Plasma

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Black silicon with ultra-low surface recombination velocity fabricated by inductively coupled power plasma

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Abstract

Black silicon is a naturally antireflective Si surface with great potential for high-efficiency solar cells. In particular, black silicon surfaces can be obtained using reactive ion etch in a maskless, single-step process regardless of crystallinity and with minimal material loss. Surface damage from the etching process, however, result in surfaces with high recombination velocity, thus limiting solar cell efficiency. We have developed a method to texture Si surfaces using non-cryogenic reactive ion etch with a plasma sustained exclusively by inductively coupled power, thereby minimizing surface damage. We achieved a target reflectance of 3% or lower in the wavelength range 300-1000 nm after an etch time of 2 min. Surfaces coated with Al_2O_3 deposited by atomic layer deposition showed recombination velocity as low as 6.9 cm s^{-1} on p-type Czochralski wafers, almost the same values as measured on planar reference surfaces (6.8 cm s^{-1}). This corresponds to an implied open circuit voltage as high as 757 mV for a cell with thickness of 180 μm and base resistivity of 4 Ω cm. These results indicate that our method for texturing of Si surfaces is suitable for fabrication of high-efficiency single junction Si solar cells.

Key Words: black silicon, reactive ion etch, surface damage, surface passivation

1. Introduction

Black silicon (b-Si)[1–3] has shown great potential as surface texturing for silicon photovoltaics thanks to its ultra-low reflectance for mono- and multi-crystalline Si at normal and varying incident angle[4,5,14,15,6–13]. This relaxes requirements on antireflective properties of front surface passivation coatings[16–18]. B-Si can be obtained using a variety of dry etch methods, among which atmospheric pressure dry etch (ADE) and plasma-based reactive ion etch (RIE) are very promising. ADE is a relatively fast, mask-less and plasma-free etching technique able to decrease reflectance of silicon down to around 10% in 1 minute of etching time[19,20], and has been used to fabricate PERC solar cells on multicrystalline Si with efficiency reaching 20%[21]. Similar to ADE, RIE texturing is also of commercial interest because: (i) it is a mask-less, single-step process, and therefore potentially scalable; (ii) it can be used to texture diamond-wire cut multi-crystalline Si wafers and very thin Si wafers with minimal material loss, both of which will likely play a significant role in the future solar cell market[22]. b-Si surfaces obtained by RIE consist typically of nanostructures of various shapes with characteristic dimensions between a few hundred nm and a few μm with no long-range spatial ordering, generated by a delicate balance between isotropic chemical etch and anisotropic physical etch of the Si surface[23,24], and the resulting averaged reflectance is often lower than 1%[2] , i.e. a significant improvement over ADE. The power conversion efficiency of solar cells with RIE texturing has surpassed 22% and 20% for mono- and multicrystalline Si substrates, respectively[25–28]. The current show-stopper for solar cells with b-Si texturing is the increased surface recombination resulting in lower open circuit voltage (V_{oc}) compared to the best conventionally-textured Si solar cells. The increased surface recombination arises mainly from the etch damage induced during RIE. In order to capitalize on the superior optical properties of b-Si, surface recombination must therefore be reduced to levels similar to those measured on competing texturing technologies. Recently, b-Si surfaces characterized by lower recombination rates have been fabricated by decreasing the capacitively coupled power (CCP) during plasma processing[7,29,30], leading to a lower kinetic energy of ions and thus reduced surface damage, as confirmed by high-resolution transmission electron microscopy characterization of individual nanostructures[7]. However, that process still required a certain amount of CCP and etching time ≥ 10 min to reach the desired antireflective properties, which is not convenient in view of process scalability. We have successfully addressed these issues and we present in this work a superior method for fabrication of b-Si by RIE. In particular: (i) we fabricated the b-Si surface *without* the use of CCP, and relied exclusively on the inductively coupled power (ICP)

in our RIE equipment; (ii) we achieved excellent antireflective properties (total reflectance lower than 3% in the wavelength range 300-1000 nm) after 2 min of etching; and (iii) we achieved state-of-the-art effective minority carrier lifetime values in excess of 3 ms on *p-type* Czochralski (CZ) Si, corresponding to surface recombination velocity values of 6.9 cm s^{-1} for textured surfaces, after passivation with Al_2O_3.

2. Results and Discussion

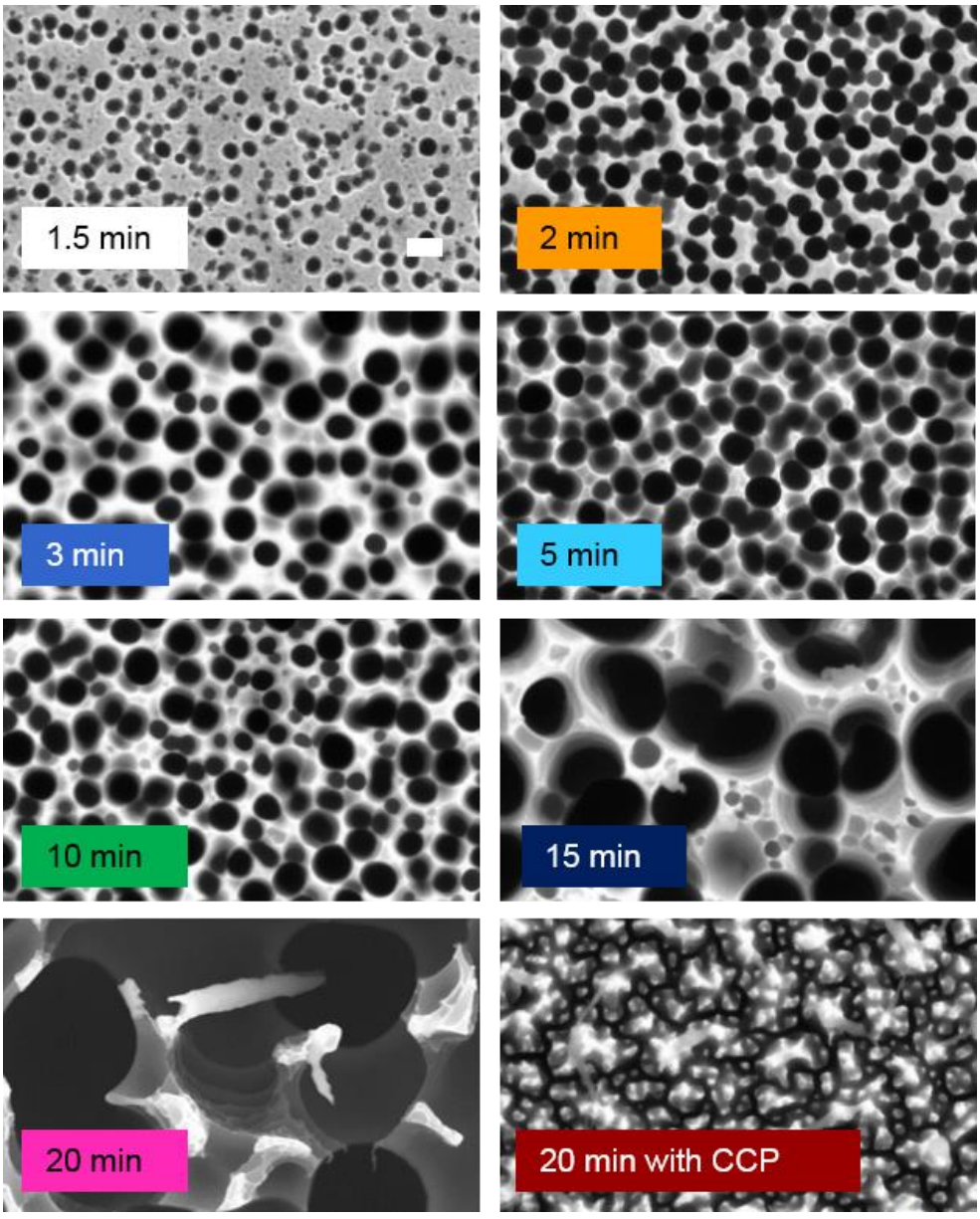

Figure 1. Top-view SEM images of surfaces after RIE texturing, before coating with Al_2O_3 and annealing. The texturing time t_{RIE} is indicated in the bottom left corner of each image. The scale bar represents 200 nm for all images.

When fabricating b-Si by RIE, both CCP and ICP are usually employed. It is usually assumed that the ICP regulates the density of the plasma, while the CCP independently determines the substrates bias voltage, and thus the kinetic energy of the ions. A comparatively low substrate bias voltage is however still present even when CCP is not used due to the large difference in mobility between electrons and ions. Thus, even without CCP, an electrical potential difference is still present between the positively charged ions in the plasma and the substrate. This self-bias effect is responsible for the slight anisotropy of the etching process, which enables the formation of b-Si nanostructures even relying only on ICP to start the plasma.

Here, we fabricated b-Si by RIE using either ICP or CCP, keeping the ratio between SF_6 and O_2 flows in the plasma as well as total pressure and process temperature (0 °C) constant, and varying the etching time t_{RIE}. Figure 1 shows top-view scanning electron microscopy (SEM) images of Si surfaces after RIE for different t_{RIE}. After 1.5 min RIE, the first etching pits have formed with roughly circular cross-section and various diameters. This is in agreement with the current understanding of formation of b-Si, which starts from etching of the native silicon oxide at a faster rate at random spots on the surface due to variations in thickness and/or density[1]. For t_{RIE} = 2 min, the pits start overlapping. The average diameter of etching pits remains rather similar (between 100 and 250 nm) for t_{RIE} up to 10 min, while it becomes considerably larger ($\geq$ 400 nm) for t_{RIE} of 15 and 20 min, with some scallops visible on the sides of the etching pits. When ICP is replaced by CCP a completely different geometry of the nanostructures results after etching for 20 min, characterized by hillocks with various shapes, some of which are connected by Si protrusions.

Cross-section SEM characterization of the surfaces after coating with Al_2O_3 deposited by atomic layer deposition (ALD) for passivation purposes is summarized in Fig. 2. It is clear that the height of the nanostructures increases with t_{RIE}, and that the Al_2O_3 coating is conformal as expected by an ALD process. In addition, for $t_{RIE} \geq 10$ min the etching pits have a paraboloid-like shape. Interestingly, the height of the nanostructures for the surface etched with CCP is approximately one third of that of the nanostructures resulting from employing ICP for the same t_{RIE} (around 500 nm and 1.5 μm, respectively).

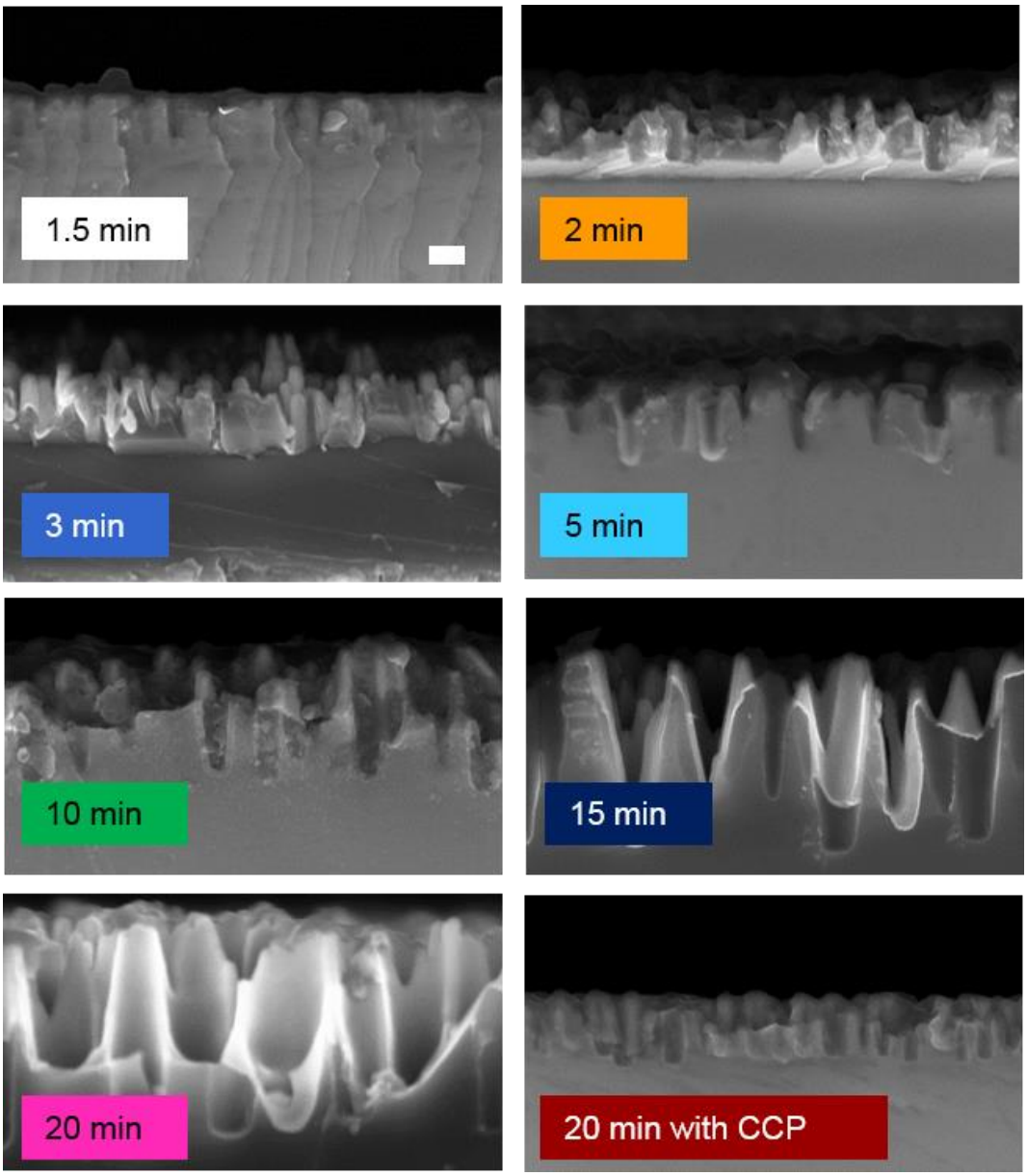

Figure 2. Cross-section SEM images of surfaces after RIE texturing, coating with Al_2O_3 and annealing. The texturing time t_{RIE} is indicated in the bottom left corner of each image. The scale bar represents 200 nm for all images.

Figure 3(a) shows the total (sum of diffuse and specular) optical reflectance R as function of photon wavelength λ in the range 300-1100 nm measured using an integrating sphere. For t_{RIE} = 1.5 min, R is above 2% for 300 nm $\leq \lambda <$ 700 nm and above 5% for 700 nm $\leq \lambda <$ 1100 nm, whereas t_{RIE} = 2 min already results in R values lower than 3% for 300 nm $\leq \lambda <$ 1000 nm. For t_{RIE} = 3 min, R is reduced to below 2% for 300 nm $\leq \lambda <$ 800 nm.

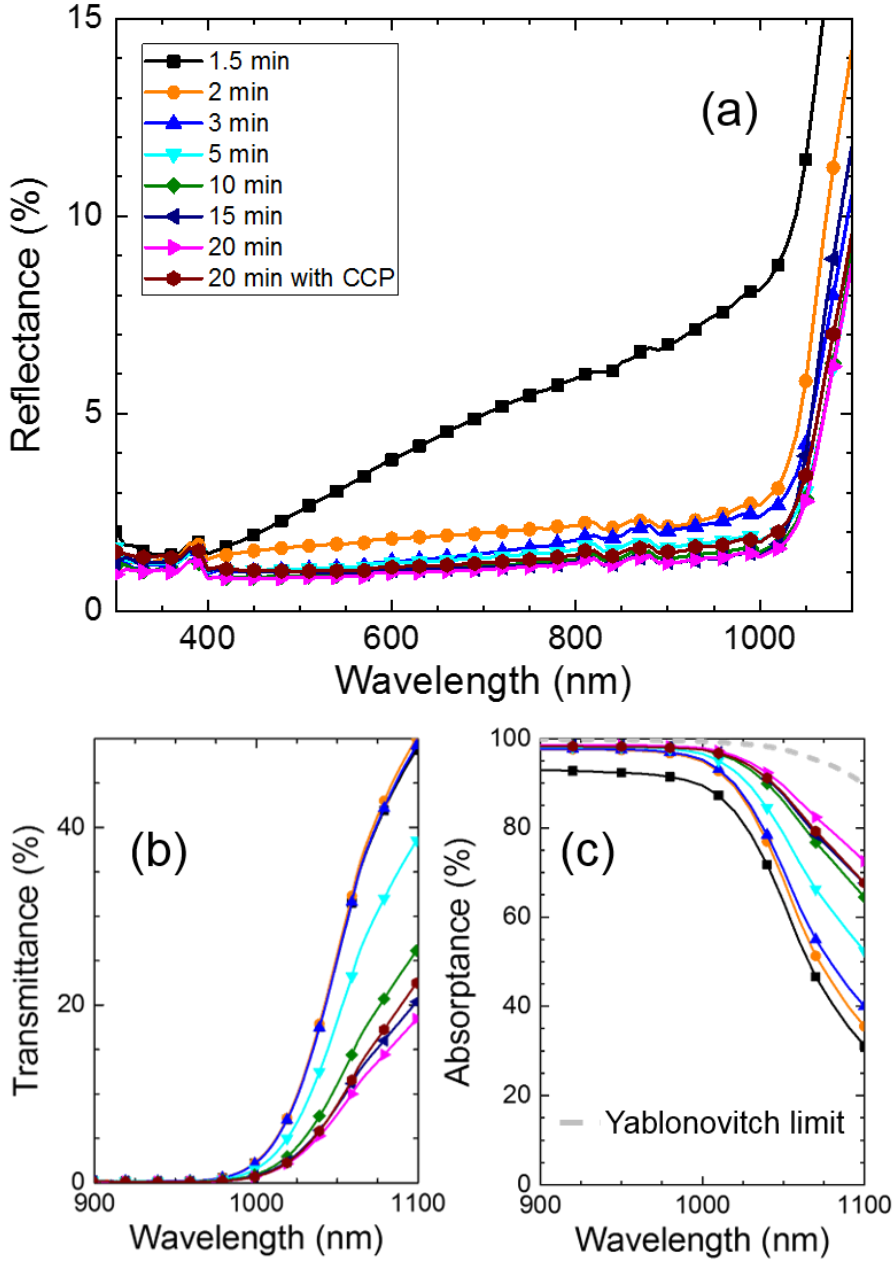

Figure 3. Optical properties of wafers with one surface textured by RIE, before ALD coating and annealing. (a) Reflectance of the front surface. (b) Transmittance through the wafer. (c) Absorptance. The legend is the same for all plots. The grey dashed line in panel (c) shows the absorption in the ideal Yablonovitch limit.

For $t_{RIE} \geq 5$ min, R is very similar and lower than 2% in the full measurement range. The measured reflectance is slightly higher than what has been obtained previously using RIE texturing, where values down to less than 1% at normal incidence[3,25,27] were obtained. We notice that the wafers used for this study are double-side mirror-polished, which have an initial

higher R than saw-damaged removed, solar-grade wafers. In addition, we expect that the R will further decrease upon coating the textured surface with passivation/antireflection stacks (typically SiN_x:H, Al_2O_3 or a combination of the two), thus eliminating front reflection losses as efficiency bottleneck. Furthermore, we note that the values of R obtained here with $t_{RIE} = 5$ min are roughly half of those measured by Hirsch *et al.* using a similar ICP process with same t_{RIE}[31]. The optical transmittance T through the wafers is also affected by the front texturing size, as shown in Figure 3(b). In particular, T is practically the same for t_{RIE} between 1.5 and 3 min, rising steeply from around 0 at 1000 nm to 50% at 1100 nm. Increasing t_{RIE} to 5 or 10 min results in T below 40% and 25% at 1000 nm, respectively. Finally, T is similar and at maximum around 20% for $t_{RIE} \geq 15$ min (including the wafer textured using CCP). It follows from these measurements that t_{RIE} of at least 10 min is required to obtain respectable light-trapping properties. Figure 3(c) shows the optical absorption A calculated by subtracting the measured R and T from 100%. The variation in T is larger than that in R and this determines the trend for A. For comparison, the absorptance in the theoretical Yablonovitch limit A_{Yabl} is also plotted according to the formula[32]:

$$A_{\mathrm{Yabl}} = 1 - \frac{1}{1 + 4n_{\mathrm{Si}}^2 \alpha_{\mathrm{Si}} W},$$

where n_{Si} and α_{Si} are the refractive index and the absorption coefficient of Si, respectively. We note that the Yablonovitch limit is found for isotropic illumination and zero front surface reflection. A Lambertian limit for absorptance that takes into account reflection at the front surface is described in the Supplementary Information (Section S1).

Figure 4 shows effective minority carrier lifetime τ_{eff} as function of t_{RIE}, averaged over an area with diameter of 100 mm for each wafer. Measurements were carried out within 1 h after post-ALD annealing, and then repeated several times over a period of around 300 h, in order to evaluate possible degradation effects of the Al_2O_3 passivation. τ_{eff} degraded with time and stabilized within 200 h; the initial value could be recovered after hotplate annealing for 10 min at temperature as low as 150 °C, as shown in Fig. S1 (Supplementary information). This behavior suggests intercalation of water during storage of the wafers as a likely reason for the decrease of τ_{eff}. Degradation of Al_2O_3 passivation has been observed in previous studies[33–35] and can be prevented by using for instance a SiN_x:H capping layer, as shown in Fig. S2 for non-textured surfaces. Immediately after post-ALD annealing, we measured average τ_{eff} longer than 3 ms for t_{RIE} between 1.5 and 2 min and between 2.5 and 3 ms for $t_{RIE} \geq 3$ min. The average τ_{eff}

of the non-textured wafer reference sample is 3.7 ms. We note that the average τ_{eff} for $t_{RIE} \leq 3$ min is within one standard deviation of the average for the τ_{eff} non-textured wafer. Texturing the Si using CCP instead of ICP results in a much lower average τ_{eff} of 0.89 ms. τ_{eff} stabilized to values higher than 1.5 ms for $t_{RIE} \leq 3$ min and lower than 1 ms for longer t_{RIE}. These results illustrate the effect of platen power on the resulting minority carrier lifetime of RIE-textured samples. Based on the combination of

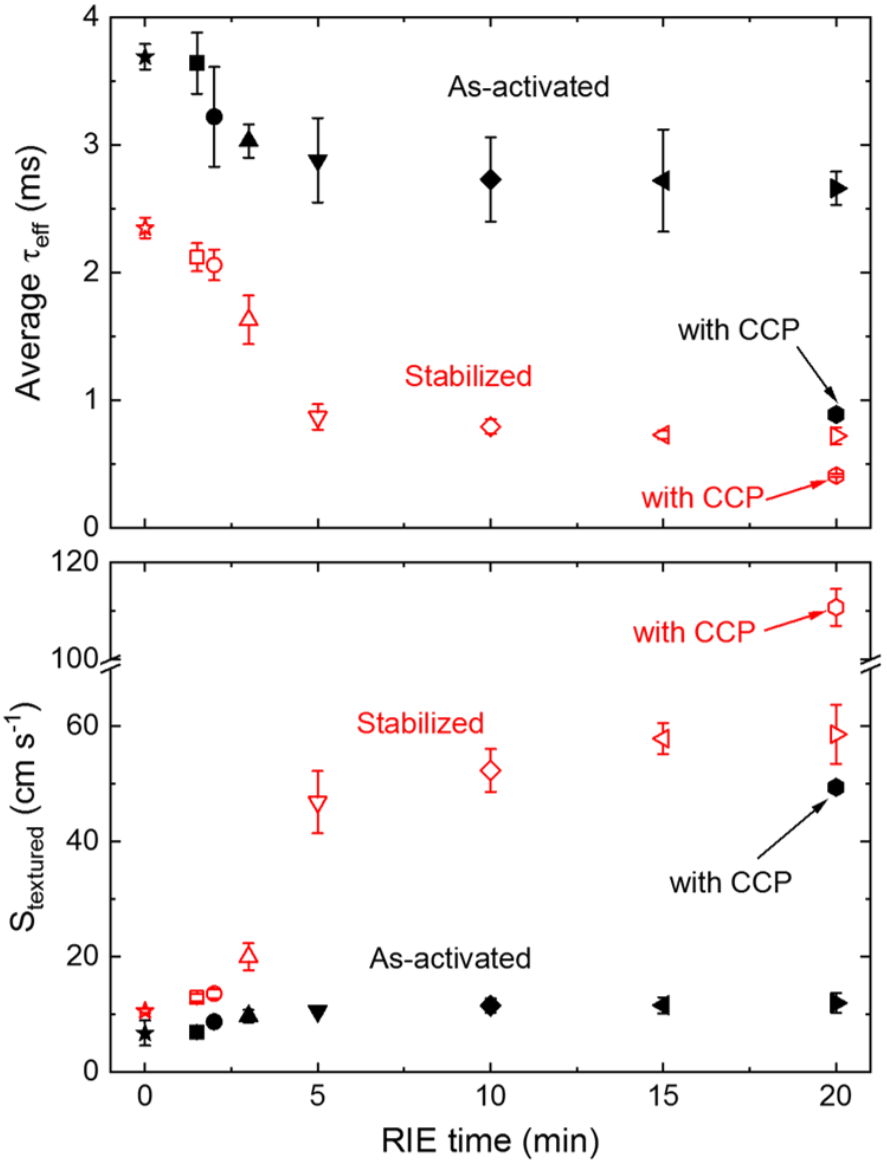

Figure 4. Top: average values of minority carriers effective lifetime τ_{eff} as function of etching time t_{RIE} mapped over 100 mm diameter surfaces, including a wafer textured using CCP. Error bars indicate one standard deviation from the average. Bottom: average effective surface recombination velocity of textured surfaces $S_{textured}$. Error bars indicate one standard deviation from the average. Open symbols indicate values measured within 1 h of Al_2O_3 activation by post-ALD annealing. Closed symbol indicate values measures after stabilization of surface passivation.

optical and lifetime measurements, it appears that RIE texturing for 2 or 3 min provides the best compromise between optical reflectance and surface damage, even though longer t_{RIE} is needed to achieve the best light trapping properties. The effective lifetime can be decomposed into contributions from the bulk and from the surfaces according to the following equation:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{S_{\text{front}} + S_{\text{back}}}{W}$$

Where τ_{bulk} is the bulk lifetime and S_{front} and S_{back} are the surface recombination velocity at the front and back surfaces, respectively. Assuming $\tau_{eff} << \tau_{bulk}$, for a non-textured wafer $S_{front} = S_{back} = S_{planar}$ and one can write $1/\tau_{eff} = 2S_{planar}/W$, from which $S_{planar} = W/2\times\tau_{eff}$. The surface recombination velocity of each textured surface $S_{textured}$ for one-sided textured wafers can then calculated as $S_{textured} = W/\tau_{eff} - S_{planar}$. Results of calculations of $S_{textured}$ are presented in the bottom panel of Figure 4. The calculated average $S_{textured}$ for t_{RIE} of 1.5, 2 and 3 min is below 10 cm s^{-1} (6.9, 8.7 and 9.7 cm s^{-1} respectively). For comparison, S_{planar} is 6.8 cm s^{-1} for the non-textured wafer. $S_{textured}$ increases for longer t_{RIE}, however not dramatically. Texturing Si with CCP instead results in a 5x increase of $S_{textured}$ to 49.4 cm s^{-1}. Extracting $S_{textured}$ from the stabilized lifetime data results in values close to S_{planar} (10.6 cm s^{-1}) only for t_{RIE} of 1.5 and 2 min (12.9 cm s^{-1} and 13.6 cm s^{-1}, respectively). We note that texturing with ICP for 3 min or shorter times in our equipment results in $S_{textured}$ values (before degradation) on par with or even better than the state-of-the-art for p-type CZ (11 cm s^{-1} in the review by Otto *et al.*[3], 20 cm s^{-1} in the record b-Si cells by Savin *et al.*[27] and 10 cm s^{-1} reported by Allen *et al.*[36]). This indicates potential for further efficiency improvements of b-Si solar cells made by RIE texturing, if CCP is omitted from the texturing process. For instance, given S_{planar} = 6.7 cm s^{-1} and $S_{textured}$ = 8.7 cm s^{-1}, the implied open circuit voltage iV_{oc} of a cell with thickness of 180 µm would be 757 mV (see calculation in the Supporting Information). Even including losses due to e.g. metallization, this would enable substantial advancements in state-of-the-art of solar cells with b-Si texturing.

3. Conclusions

We have developed a recipe to texture Si surfaces using non-cryogenic reactive ion etch with a plasma sustained exclusively by inductively coupled power. We achieved a target reflectance of 3% or lower in the wavelength range 300-1000 nm after just 2 min of etch time. Measurements of effective minority carrier lifetime of wafers coated by Al_2O_3 deposited by

atomic layer deposition showed values in excess of 3 ms for etching time equal to or shorter than 3 min on p-type CZ wafers. The passivation offered by Al_2O_3 degraded by approximately 50% before stabilizing after around 200 h, however it could be recovered by simple annealing at 150 °C in ambient atmosphere on a hotplate and degradation could be avoided on non-textured wafers employing a SiN_x:H capping layer. We calculated values of surface recombination velocity of textured surfaces as low as 6.9 cm s^{-1} before degradation, which is better than state-of-the-art for p-type CZ Si textured by reactive ion etch. Fabrication of solar cells with several architectures sharing the front surface texturing developed here is under progress and will be the subject of a future report.

4. Experimental Section

4.1 Fabrication

All wafers were 150 mm diameter, 500 μm thick CZ p-type Si (100). Wafers were textured on one side using an ICP RIE tool (MP0637) from SPTS using the following parameters: process temperature of 0 °C, SF_6 and O_2 plasma with flow ratio of SF_6:O_2 ~ 1:1, total pressure of 24 mTorr. For each wafer the plasma was sustained using either an ICP of 1500 W, or a CCP of 100 W. The process time t_{RIE} was varied between 1.5 and 20 min. All wafers (including non-textured wafers for reference purposes) were cleaned using a standard cleaning (SC) procedure (SC1: 10 min in a NH_4OH:H_2O_2:H_2O = 1:1:5 solution at 70 °C; SC2: 10 min in a HCl:H_2O_2:H_2O = 1:1:5 solution at 70 °C). The SiO_2 layer grown during SC1 was removed by a 30 s dip in diluted HF (5%) at room temperature. The SiO_2 layer grown during SC2 was not removed. Surfaces were passivated by Al_2O_3 using 380 cycles of thermal atomic layer deposition (ALD) at 200 °C using a R200 tool (Picosun). Trimethylalane (TMA) and water were used as precursors for Al and O, respectively. In order to activate the passivation, wafers were annealed in a Tempress furnace at 400 °C for 10 min in a N_2 atmosphere. Capping layers of 75 nm SiN_x:H were deposited by plasma enhanced chemical vapor deposition at 300 °C in a Multiplex PECVD system (SPTS).

4.2 Characterization

The total (diffuse + specular) optical reflectance *R* was measured using a QEXL system (PV measurements) equipped with an integrating sphere. The optical transmittance *T* was measured using a UV spectrophotometer (UV-2600, Shimadzu Co.). Scanning electron microscopy (SEM) images were acquired using a Supra 40VP microscope (Carl Zeiss) at an acceleration

voltage of 5 kV. Effective minority carrier lifetime τ_{eff} was measured with a MDPmap tool (Freiberg Instruments). Lifetime values were extracted at an injection level of 10^{15} cm^{-3} and averaged over a 100 mm diameter area in the center of each 150 mm wafer, due to known edge effects of the passivation process.

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Notes

The authors declare no competing financial interest.

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