



Zero Voltage Switching Control Method for MHz Boundary Conduction Mode Converters

Hernandez, Juan C.; Mira Albert, Maria del Carmen; Petersen, Lars Press; Andersen, Michael A. E.; Petersen, Niels H.

Published in:
IEEE Transactions on Industrial Electronics

Link to article, DOI:
[10.1109/TIE.2019.2926039](https://doi.org/10.1109/TIE.2019.2926039)

Publication date:
2020

Document Version
Peer reviewed version

[Link back to DTU Orbit](#)

Citation (APA):
Hernandez, J. C., Mira Albert, M. D. C., Petersen, L. P., Andersen, M. A. E., & Petersen, N. H. (2020). Zero Voltage Switching Control Method for MHz Boundary Conduction Mode Converters. *IEEE Transactions on Industrial Electronics*, 67(2), 1544-1554. <https://doi.org/10.1109/TIE.2019.2926039>

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

Zero Voltage Switching Control Method for MHz Boundary Conduction Mode Converters

Juan C. Hernandez, Maria C. Mira, Lars P. Petersen, Michael A. E. Andersen, *Member, IEEE*, Niels H. Petersen

Abstract— Boundary conduction mode (BCM) or critical conduction mode (CrM) is characterized by an inductor current that operates in the boundary between continuous (CCM) and discontinuous conduction modes (DCM), making the converter switching frequency dependent on the converter operating conditions. The advantage of this operation mode versus CCM is achieving zero current switching (ZCS) conditions for the converter rectifier, which makes it possible to use silicon (Si) diode rectifiers without having a penalty due to reverse recovery issues. Moreover, the main switch turn on loss is decreased due to ZCS conditions and valley switching operation. However, the penalty is an increased current stress in the circuit, and an increased main switch turn off energy loss. Implementation of synchronous rectifier in BCM converters makes it possible to achieve zero voltage switching (ZVS) conditions by extending the synchronous rectifier conduction time after zero current condition in the inductor. High power density, high efficiency MHz implementations have already been demonstrated in the literature; however, none of the proposed solutions solves the controllability issues of the synchronous rectifier switch. This work proposes and validates a ZVS self-regulating control method for BCM converters operating in the MHz switching frequency range.

Index Terms— Self-regulating control, boundary conduction mode (BCM), high efficiency, high switching frequency, zero voltage switching (ZVS).

I. INTRODUCTION

SWITCHED-MODE mode power supplies (SMPS) technology has been an efficient solution for voltage and current conversion applications from the early 20th century. Compared to linear regulators, SMPS can ideally reach efficiencies up to $\eta = 100\%$. This technology, based on the combination of reactive elements with any type of switch, was initially developed employing mechanical switches, vacuum

tubes, and finally semiconductor based switches such as thyristors, bipolar junction transistors (BJT), and Metal Oxide Semiconductor Field Effect Transistors (MOSFET) [1], [2], [3].

The size and the cost of SMPS is heavily influenced by the size of reactive energy storage elements, which is inversely proportional to the converter operating frequency. Therefore, increasing the converter switching frequency allows for an increased converter power density and reduced cost. However, the switches, far from being ideal, present switching losses that put a practical limit on the maximum attainable converter switching frequency. Resonant SMPS topologies present an alternative solution for eliminating the converter switching losses and increasing the power density [4], at the penalty of an increased current stress due to the increased reactive energy circulation in the circuits.

High frequency BCM based implementations have been demonstrated in the literature, where the increased conduction loss due to the increased current stress in BCM implementations is compensated by the reduction in switching loss [5]. In [6], a 5 MHz ZVS boost BCM implementation with efficiency figures up to $\eta = 98\%$ is demonstrated. As presented in [7] and [8], MHz implementations allow for a large reduction of the converter input inductor and filter, which heavily affects the converter power density. However, pushing the converter switching frequency in BCM implementations is only possible when the converter operates under ZVS conditions, which depend on the converter input to output voltage ratio and the non-linear switching node parasitic capacitance. In [9] a ZVS extension method for BCM converters with synchronous rectification is presented. In this solution, the synchronous rectifier time is increased to create a negative inductor current to discharge the switching node capacitance, achieving ZVS independently of the converter input to output voltage ratio. A MHz BCM boost derived power factor correction circuit with ZVS extension is demonstrated in [10]. However, both of the proposed prototypes, rely on measurements and characterization to map the necessary negative inductor current to achieve ZVS as a function of the converter input and output voltage conditions. This is a time consuming procedure, where components tolerance will create errors that will result in loss of ZVS conditions or increased components current stress. This paper presents a self-regulating control method for ZVS extension where the switching node voltage is regulated in close loop

Manuscript received Month xx, 2xxx; revised Month xx, xxxx; accepted Month x, xxxx.

Juan C. Hernandez and Lars P. Petersen are with ICE Power A/S., Vandtarnsvej 62A, 3B, 2860 Soeborg, Denmark, (jch@icepower.dk, lpp@icepower.dk).

Maria C. Mira and Michael A. E. Andersen are with the Department of Electrical Engineering, Technical University of Denmark, 2800 Kongens Lyngby, Denmark, (mariacarmen.mira@gmail.com, ma@elektro.dtu.dk).

Niels H. Petersen is with Grundfos Holding A/S, Poul Due Jensens Vej 7, 8850 Bjerringbro, Denmark (nhpetersen@gundfos.dk).

control by controlling the synchronous rectifier conduction time. The proposed method is demonstrated in a GaN based MHz boost Power Factor Correction (PFC) BCM implementation, however this solution can be applied to different topologies and applications.

The document is organized into five sections: after the introduction presented in Section I, Section II presents the BCM operation both under valley and extended zero voltage switching mode operation, and the equations that define the converter operation under these modes. Section III presents the proposed self-regulating control method for ZVS extension operation, and Section IV shows the implemented prototype. Finally, the conclusion is presented in Section V.

II. BOUNDARY CONDUCTION MODE OPERATION

Boundary conduction mode corresponds to an operation mode where the converter inductor current operates between the continuous and the discontinuous conduction modes. The ideal switching node voltage and the inductor current waveform are shown in Fig. 1. In this operation mode, the converter switching frequency varies according to (1), as presented in [11]. The parameter M is defined as the converter input to output voltage ratio for a conventional boost converter, as in (2).

$$f_{sw} = V_{in}^2 (1 - 1/M) / 2LP_{out} \quad (1)$$

$$M = V_{out} / V_{in} \quad (2)$$

However, during boundary conduction mode, valley switching or ZVS at the turn on of the main switch are preferred to reduce the semiconductor switching losses. As the converter switching frequency is increased, the valley switching or ZVS time and the switching node rise time need to be taking into account to accurately predict the converter switching frequency [12], [7], [8].

A. Valley Switching Operation

A conventional boost converter with the typical valley switching waveforms under boundary conduction mode operation is depicted in Fig. 1. When the inductor current decreases to zero at t_3 , the rectifier becomes reverse biased, and the parasitic capacitances attached to the switching node resonate with the input inductor. The equivalent circuit during the resonant period, can be simplified to an ideal LC circuit, where the MOSFET output parasitic capacitance (C_{oss}) appears in parallel with the diode junction capacitance (C_j), and resonate with the converter input inductance with angular frequency ω_0 , as in $\omega_0 = 1/\sqrt{L \cdot (C_{oss} + C_j)}$.

In conventional BCM boost implementations, if the switching node capacitance is assumed to be ideal, the boost switch will lose its ability to soft switch when the converter input voltage V_{in} is higher than $V_{out}/2$ or $M < 2$.

B. Natural Zero Voltage Switching Operation

When the converter input voltage V_{in} is smaller than $V_{out}/2$ or $M > 2$, the boost switch will operate under ZVS conditions as shown in Fig. 2. During this operation mode, all the energy stored in the switching node parasitic capacitance is recovered before the boost switch turn on event.

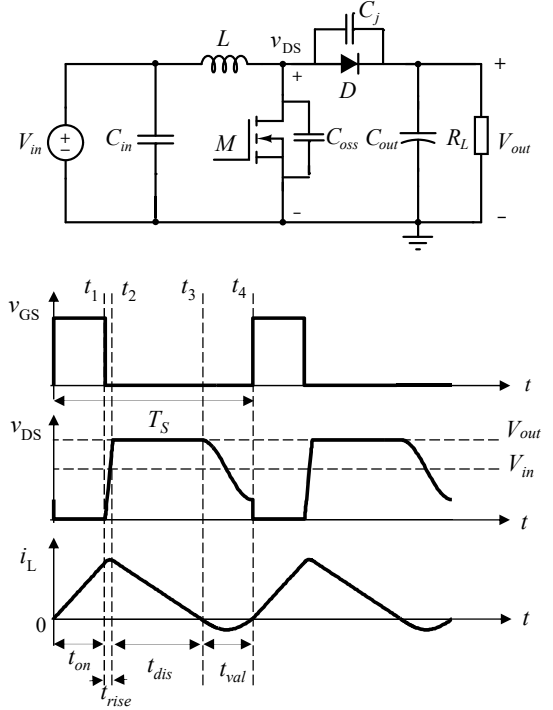


Fig. 1. Conventional boost with BCM valley switching operating waveforms ($M < 2$).

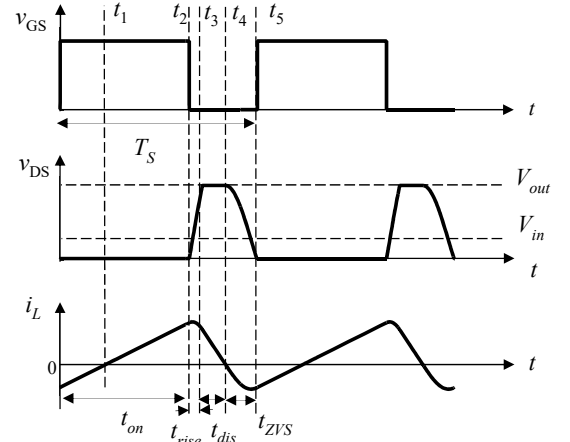


Fig. 2. Key operating waveforms under natural ZVS conditions ($M > 2$).

C. Natural Zero Voltage Switching Operation

If the rectifier diode is replaced with a synchronous rectifier, it is possible to extend the zero voltage switching range of the converter. This can be achieved, as previously presented in [9], [10], by extending the conduction time of the rectifier beyond zero current condition in the inductor. The schematic and the converter operating waveforms under extended ZVS conditions are depicted in Fig. 3.

The time to achieve ZVS can be calculated as shown in (3).

$$t_{ZVS} = \frac{\pi}{\omega_0} + \frac{1}{\omega_0} \arctan \left(\frac{\omega_0 C \left(i_L(t_4)/M + (V_{out} - V_{in}) \sqrt{(1 - 2/M)C/L + (i_L(t_4)/V_{out})^2} \right)}{V_{in}(1 - 1/M)C/L - i_L(t_4) \sqrt{(1 - 2/M)C/L + (i_L(t_4)/V_{out})^2}} \right) \quad (3)$$

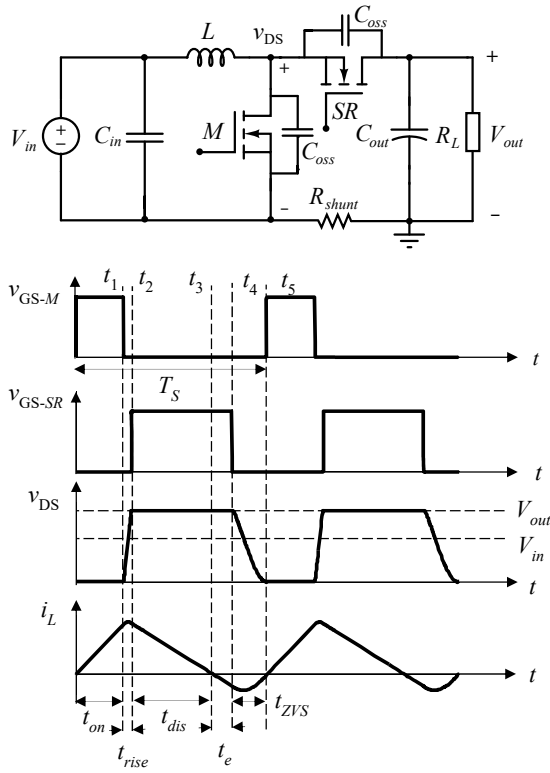


Fig. 3. Conventional boost converter with synchronous rectifier under extended ZVS conditions.

Where the initial current condition and the extra conduction time t_e after zero current condition to achieve ZVS conditions, can be calculated by solving for the inductor initial current condition $i_L(0)$ or by evaluating the energy transfer in the ideal resonant circuit.

Fig. 4 shows the switching node voltage waveform under valley switching conditions ($M < 2$) and the corrected extended ZVS waveform. Initially, under valley switching conditions, all the energy in the resonant circuit is stored in the switching node capacitance. At time instant $1/4 \cdot t_{valley}/2\pi\omega_0$, all the resonant energy in the circuit is stored in the converter input inductor. This energy will be transferred back to the switching node capacitance, producing the switching node voltage to resonate around $V_{in} \pm (V_{out} - V_{in})$. In order to calculate the extra amount of energy that needs to be inserted in to the system to reach ZVS conditions, or to resonate around $V_{in} \pm (V_{in})$ (4) can be used. This expression can be simplified as shown in (5), where $C = 2 \cdot C_{oss}$.

$$\Delta E = \frac{1}{2} C V_{in}^2 - \frac{1}{2} C (V_{out} - V_{in})^2 \quad (4)$$

$$\Delta E = \frac{1}{2} C V_{out}^2 \cdot (2/M - 1) \quad (5)$$

Using (5) it is possible to calculate the input inductor initial current condition, $i_L(0) = i_L(t_4)$, which satisfies ZVS condition at the switching node as shown in (6) and (7). In the same way, the necessary extra conduction time for the synchronous rectifier, can be calculated by using (7), as shown in (8).

$$E_L(t_4) = \frac{1}{2} L \cdot i_L(t_4)^2 = \frac{1}{2} C \cdot V_{out}^2 (2/M - 1) \quad (6)$$

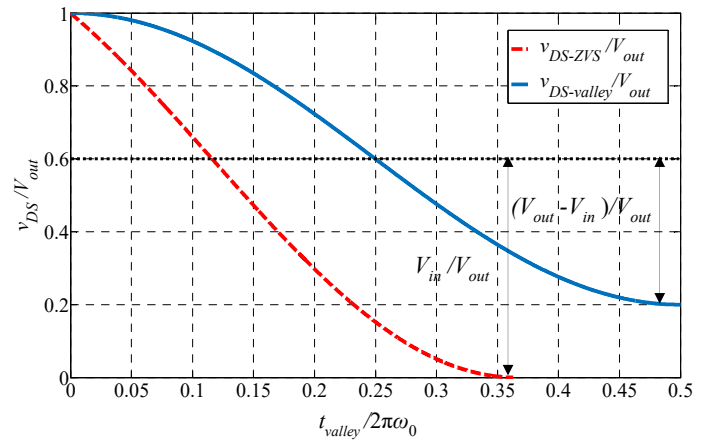


Fig. 4. Switching node voltage waveform under valley switching and extended ZVS conditions.

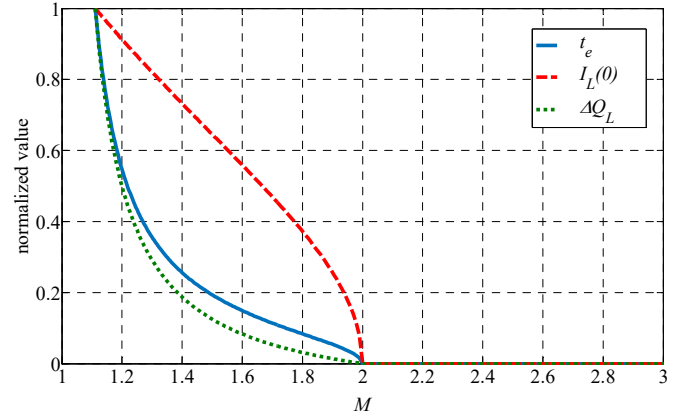


Fig. 5. Extra synchronous rectifier conduction time (t_e), initial inductor current condition ($i_L(t_4)$), and inductor charge increment (ΔQ_L) vs. converter input to output voltage ratio (M).

$$i_L(t_4) = -V_{out} \sqrt{C/L \cdot (2/M - 1)} \quad (7)$$

$$t_e = \frac{-i_L(t_4) \cdot L}{V_{out} (1 - 1/M)} = \frac{1}{\omega_0} \frac{\sqrt{2/M - 1}}{1 - 1/M} \quad (8)$$

Fig. 5 presents the normalized synchronous rectifier extra conduction time (t_e), the initial inductor current condition ($i_L(0) = i_L(t_4)$), and the inductor extra charge (ΔQ_L) required for ZVS operation vs. the converter input to output voltage ratio M . All the variables in this figure are controllable quantities by using synchronous rectifier zero current detection in the first case, or by detecting peak current or integrating the current in the other two cases.

The work presented in [9], [10], [13], [14], [15] and [16] use the time after zero current detection, $t_e = 1/\omega_0 \left(\sqrt{2/M - 1} / (1 - 1/M) \right)$, as the control variable. A curve fitting based on characterization data is used in order to achieve ZVS based on the converter input and output voltage. However, controlling ZVS operation using characterization data, requires computational power and more importantly, is sensitive to components tolerance and variations in the propagation delay times. These tolerances, will produce deviations from the approximated values, which will result in failure to achieve ZVS conditions or an increased circulating reactive energy. These situations will lead to an increased

capacitive switching loss, or an increased current stress in the converter components resulting in a negative effect on the converter efficiency figures. The proposed control method can regulate the switching node voltage to achieve ZVS conditions regardless of components tolerances.

III. SELF-REGULATING CONTROL FOR ZVS EXTENSION

This work proposes the implementation of a closed loop control to ensure ZVS conditions under any circumstances. The implemented control loop is based on sampled information from the converter switching node voltage. Conventional BCM controllers operating under valley switching conditions, use information of the instantaneous switching node voltage in order to determine the turn on instant of the main switch, and minimize the energy stored in the parasitic capacitance. In high voltage, and more specifically in PFC applications, this voltage is sensed through an auxiliary winding in the input inductor (W_{aux}), as shown in Fig. 6. The use of this auxiliary winding makes it possible to scale down the switching node voltage, without using resistor divider networks, which are lossy and have bandwidth limitation problems.

The proposed control method in this work is similar to a conventional valley switching control scheme, where the derivative of the switching node (v_{DS_der}) is used in order to determine the turn on instant of the main switch. The ZVS control block diagram is presented in Fig. 7. Fig. 8 shows the key operating waveforms of the ZVS boost converter with extended synchronous rectifier conduction time. As can be observed in Fig. 8, at t_4 the synchronous rectifier is turned off. After t_4 the resonant interval t_{ZVS} begins, and after the switching node derivative has reached zero volts at t_5 , two events take place. First, the scaled down switching node voltage v_{DS_div} , obtained from the auxiliary winding voltage ($v_{aux} = (v_{DS} - V_{in})/n$), is retained in the sampling capacitor $C_{S\&H-1}$. Second, the main switch M is turned on.

Turning on the main switch at zero switching node voltage derivative, means that the switching node voltage has reached

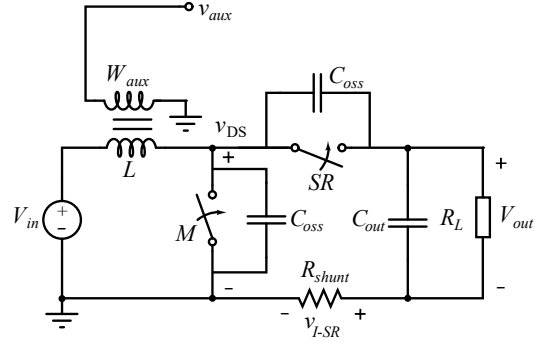


Fig. 6. Boost converter with synchronous rectifier and inductor with auxiliary winding.

its minimum value, and therefore, the main switch can be turned on under minimum switching loss condition. When the main switch M is turned on, the sampled value, which is stored in the sampling capacitor $C_{S\&H-1}$, is transferred to the second sampling capacitor $C_{S\&H-2}$. Therefore, the voltage v_{sample} in this sampling capacitor is a continuous voltage waveform representing the switching node voltage under valley switching conditions (or at zero switching node voltage derivative). This sampled voltage is used as the control variable for controlling the extra conduction time t_e of the synchronous rectifier by means of a PI regulator. The implemented control scheme also includes a low speed loop, which ensures constant on time of the converter main switch M across the line cycle, and regulates the converter output voltage.

Fig. 9 shows a Spice based simulation of the implemented control scheme in a conventional boost PFC converter. This simulation demonstrates the ability of the control loop to regulate the extra conduction time of the synchronous rectifier under a fast changing converter input voltage. In this simulation, the parasitic switching node capacitance is assumed to be ideal. The output capacitance (C_{out}) and load (R_L) are replaced with an ideal voltage source with voltage value V_{out} and the main switch on time (t_{on}) is inserted as a

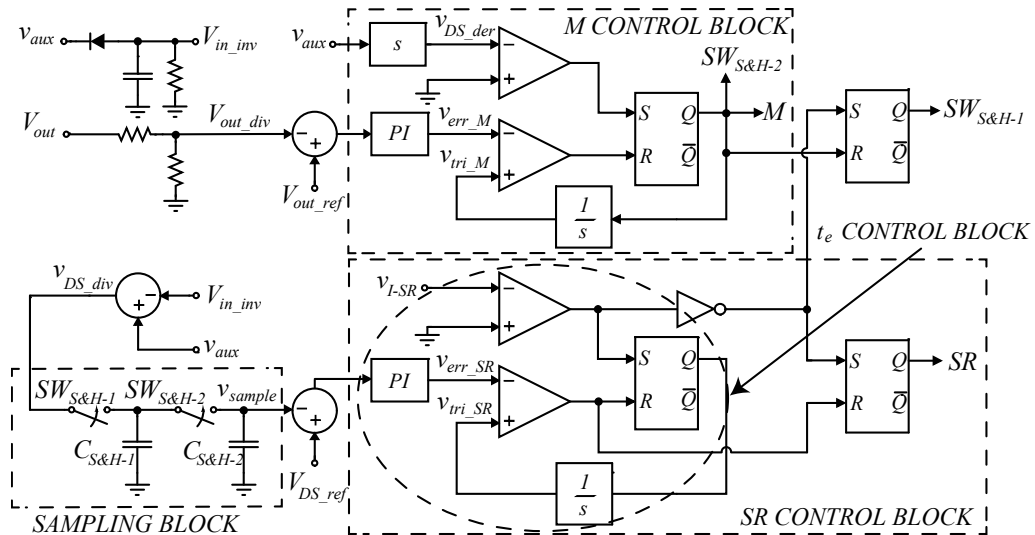


Fig. 7. Proposed ZVS control block diagram.

fixed value. Table I shows the values used in this simulation. The simulated converter input voltage v_{in} (top waveform), inductor current i_L (middle waveform), and the synchronous rectifier error voltage v_{error_SR} (dotted line waveform at the bottom), are plotted across half period of the input line. The simulated error signal is compared to the calculated extra conduction time t_e . The calculated extra conduction time t_e (continuous line waveform at the bottom) is scaled by the gain of the comparator that controls the on time of the synchronous rectifier as in (9). In this simulation, the time base for control of the synchronous rectifier is modeled by an ideal current source and a capacitor with a dv/dt slope of $k = 10 \text{ V}/\mu\text{s}$. As it can be observed, the control scheme accurately predicts the necessary extra conduction time to operate under ZVS conditions across the input line cycle.

$$v_{error_SR} = k \cdot t_e = \frac{dv_{triSR}}{dt} \cdot t_e = 10 \text{ V}/\mu\text{s} \cdot t_e \quad (9)$$

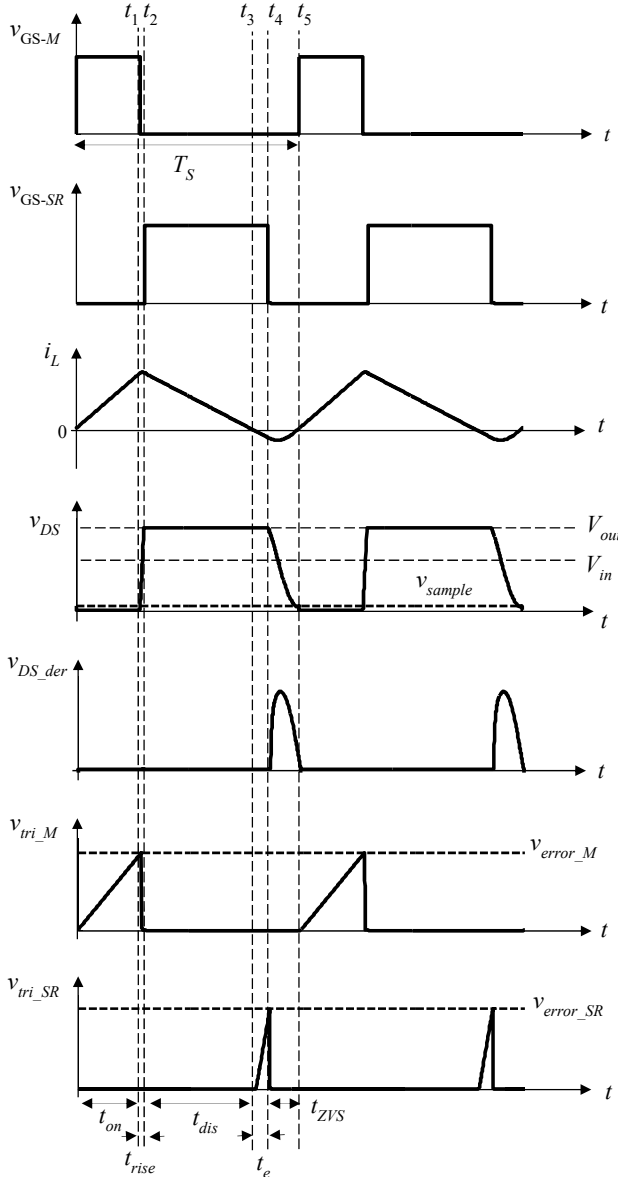


Fig. 8. Key operating waveforms of the ZVS boost converter with extended synchronous rectifier conduction time.

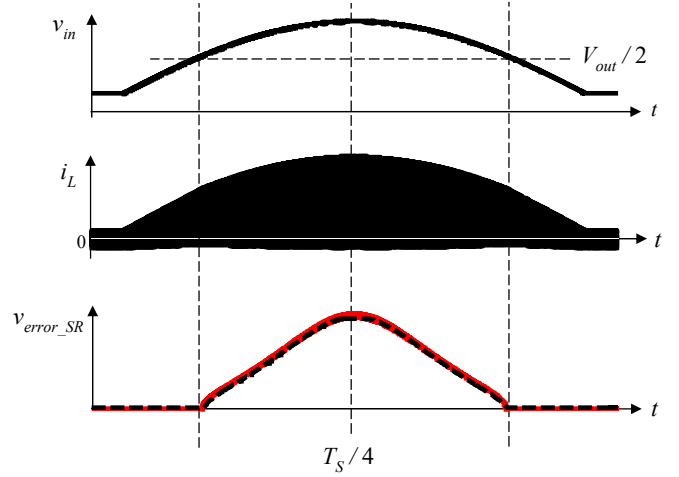


Fig 9. Simulated error output voltage vs. calculated extra conduction time t_e across half line cycle.

TABLE I
SIMULATION PARAMETERS

V_{ac}	230 V_{rms}
V_{out}	400 V
L	100 μH
$C = 2 \cdot C_{oss}$	100 pF
C_{in}	1 μF
$v_{DS}(t_5)$	10 V
k	10 $\text{V}/\mu\text{s}$
t_{on}	0.8 μs

A. Controllability of the Switching Node Voltage

This section presents a modelling approach of the controllability of the sampled switching node voltage $v_{sample} = v_{DS}(t_5)$. An accurate model makes it possible to maximize the control loop error suppression and bandwidth. The controllability can be modelled by obtaining the control-to-sampled switching node voltage transfer function $G_v = \hat{v}_{sample} / \hat{v}_{error_SR}$. Since the extra synchronous rectifier time t_e controls the negative peak inductor current on each cycle, the dynamics of the inductor current will not have any effect on the final switching node voltage. The plant transfer function G_v can be approximated as a gain multiplied by a zero order hold ZOH transfer function, and a delay time $t_5 - t_4 = t_{ZVS}$ from the moment the extra conduction time is refreshed until the next sample is taken as shown in (10).

$$G_v = \frac{\hat{v}_{sample}}{\hat{v}_{error_SR}} = k \cdot \frac{\hat{v}_{sample}}{\hat{t}_e} = H_{ZOH}(s) \cdot e^{-st_{ZVS}} \quad (10)$$

$$= \frac{dv_{tri_SR}}{dt} \cdot \frac{\hat{v}_{sample}}{\hat{t}_e} \cdot \frac{1 - e^{-sT_s}}{sT_s} \cdot e^{-st_{ZVS}}$$

Where T_s is the sampling period, which is equal to the converter switching period. The gain $\hat{v}_{sample} / \hat{t}_e$, can be calculated by particularizing (4) and (6) as in (11) and solving for $v_{DS}(t_5)$.

$$\Delta E = \frac{1}{2} C \frac{(V_{out} - V_{in})^2}{L} \cdot t_e^2 = \frac{1}{2} C (V_{in} - v_{DS}(t_5))^2 - \frac{1}{2} C (V_{out} - V_{in})^2 \quad (11)$$

$$v_{DS}(t_5) = V_{in} - (V_{out} - V_{in}) \sqrt{1 + \frac{t_e^2}{LC}} \quad (12)$$

Finally, this gain can be obtained, according to [13], by linearizing around the steady state operating conditions by calculating the derivative of (12) respect to t_e as in (13).

$$\begin{aligned} \hat{v}_{sample} &= \frac{\partial v_{DS}(t_5)}{\partial t_e} \hat{t}_e \\ \frac{\hat{v}_{sample}}{\hat{t}_e} &= - \frac{(V_{out} - V_{in}) t_e}{\sqrt{1 + \frac{t_e^2}{LC}} \cdot LC} \end{aligned} \quad (13)$$

Fig. 10 shows the calculated and the simulated $\hat{v}_{sample}/\hat{v}_{error_SR}$ transfer function for the set of conditions shown in Table II. As it can be observed, the proposed model composed by a gain and a ZOH transfer function with a delay, shows very good match with the simulated results.

However, the proposed model, assumes $\hat{v}_{sample}/\hat{v}_{error_SR}$ perturbation is not affected by the dynamics of the converter output voltage, which is a valid assumption as long as the relation in (14) is fulfilled. Otherwise, the complete transfer function needs to be derived as shown in (15).

$$\frac{\partial v_{DS}(t_5)}{\partial t_e} \gg \frac{\hat{v}_{out}}{\hat{t}_e} \cdot \frac{\hat{v}_{sample}}{\hat{v}_{out}} \quad (14)$$

$$G_v = \frac{\hat{v}_{sample}}{\hat{v}_{error_SR}} = k \cdot \left(- \frac{(V_{out} - V_{in}) t_e}{\sqrt{1 + \frac{t_e^2}{LC}} \cdot LC} + \frac{\hat{v}_{out}}{\hat{t}_e} \cdot \frac{\hat{v}_{sample}}{\hat{v}_{out}} \right) \quad (15)$$

$$\cdot H_{ZOH}(s) \cdot e^{-st_{zvs}}$$

Where $\hat{v}_{sample}/\hat{v}_{out}$ can be obtained by deriving (12) respect to V_{out} as in (16).

$$\frac{\hat{v}_{sample}}{\hat{v}_{out}} = \sqrt{1 + \frac{t_e^2}{LC}} \quad (16)$$

And where the effect of the extra conduction time on the converter output voltage can be calculated by knowing that the system will behave as a first order system. This is due to the fact that the inductor current is not a state-variable, since the extra conduction time is determined after the zero current detection in each cycle. Therefore, this transfer function can be calculated as the effect of the time perturbation on the average output capacitor and output load current multiplied by their impedances as in (17).

$$\frac{\hat{v}_{out}}{\hat{t}_e} = \frac{\partial I_{C_{out} R_{L_{avg}}}}{\partial t_e} \cdot \frac{R_L}{1 + s C_{out} R_L} \quad (17)$$

Where the average output current circulating through the load and the output capacitor can be derived from Fig. 5 by obtaining the part of the charge of the inductor current that will flow to the output as in (18).

$$I_{C_{out} R_{L_{avg}}} = \frac{1}{T} \left(\int_{t_2}^{t_4} i_L(t) dt + \frac{1}{2} \left(\int_{t_1}^{t_2} i_L(t) dt + \int_{t_4}^{t_5} i_L(t) dt \right) \right) \quad (18)$$

However, as it can be seen in Fig. 11, the proposed simplified model with assumption (14) produces accurate

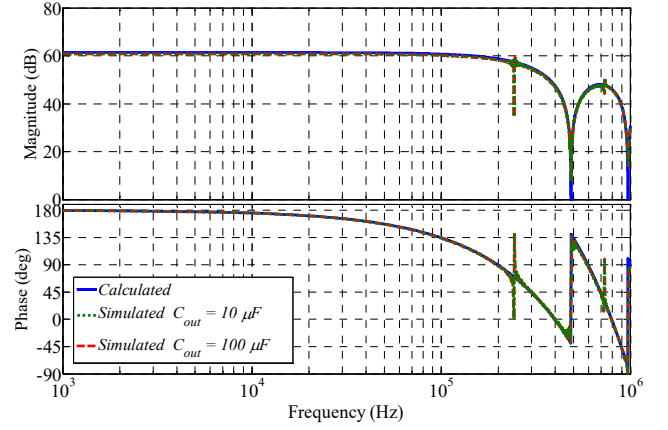


Fig. 10. Simulated vs. calculated control-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{error_SR}$ transfer function.

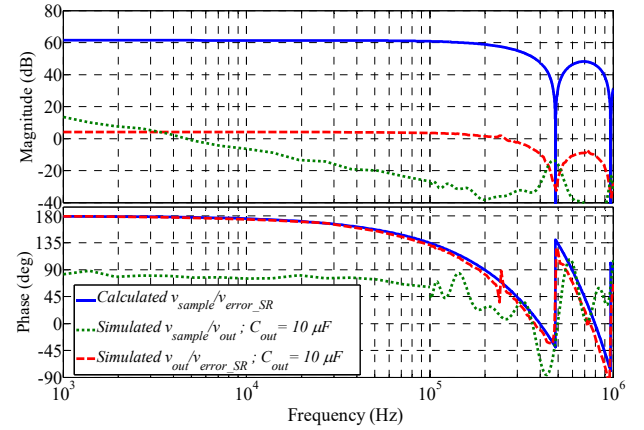


Fig. 11. Simulated control-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{error_SR}$, output voltage-to-sampled switching node voltage $\hat{v}_{out}/\hat{v}_{error_SR}$ and control-to-output voltage $\hat{v}_{sample}/\hat{v}_{out}$ transfer functions.

TABLE II
SIMULATION PARAMETERS

V_{in}	250 V
V_{out}	400 V
L	100 μ H
$C = 2 \cdot C_{oss}$	100 pF
C_{out}	10 μ F, 100 μ F
$v_{DS}(t_5)$	10 V
R_L	1 k Ω
f_{sw}	485 kHz

results due to large ratio between the equivalent switching node parasitic capacitance and the converter output capacitance. This is due to the fact that the perturbations on the extended conduction time t_e , will result in a much larger effect on the sampled switching node voltage than on the converter output voltage. Fig. 11 shows the simulated $\hat{v}_{out}/\hat{v}_{error_SR}$ and $\hat{v}_{sample}/\hat{v}_{out}$, whose product is at least two orders of magnitude smaller than the error to sample plant transfer function G_v .

It is also important to notice, on the one hand, that $\hat{v}_{out}/\hat{v}_{error_SR}$ behaves as a first order system with no

inductor dynamics as predicted; and on the other hand, that the simplified model will be valid unless the converter output to switching node capacitance ratio is drastically reduced and the converter operates under light load conditions. Under these situation, $\hat{v}_{out}/\hat{v}_{error_SR}$ will increase in the low frequency range making assumption (14) no longer valid. However, in any case, due to the low order and fast dynamics of the plant transfer function $\hat{v}_{sample}/\hat{v}_{error_SR}$, it is possible to implement a regulation loop capable of regulating the switching node voltage under fast converter operating conditions.

IV. PROTOTYPE IMPLEMENTATION

The proposed control method is implemented using discrete components in a four layer printed circuit board (PCB). Fig. 12 shows the top and bottom views of the implemented ZVS PFC control board. Fig. 13 presents the integration of the ZVS control board and the power stage. As it can be seen, the implemented control board includes a bridge rectifier and output electrolytic capacitors to test the control in a PFC application. Discrete isolated gate drive circuitry is included for both switches. Current mode controllers are used to drive two low inter-winding capacitance transformers to minimize current injection from fast switching node voltage derivatives (dv/dt). Low propagation delay time capacitive couplers are used for gate signal isolation. The converter power stage is implemented using two Transphorm TPH30002 ($V_{DS} = 600$ V, $R_{DS} = 290$ m Ω) cascode GaN devices, in power quad flat no-lead (PQFN) packages. GaN devices are used in this

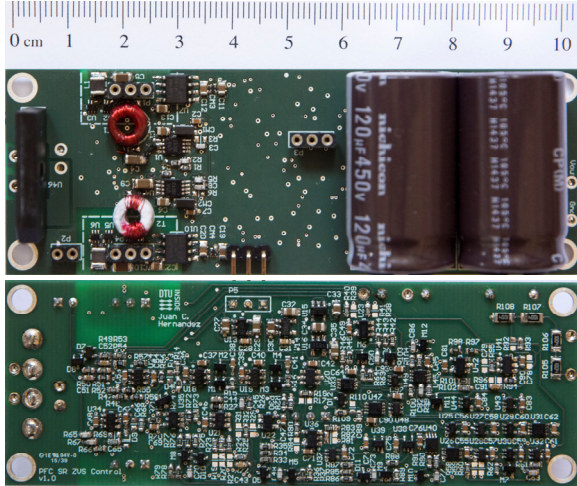


Fig. 12. Top and bottom views of the designed ZVS control PCB.

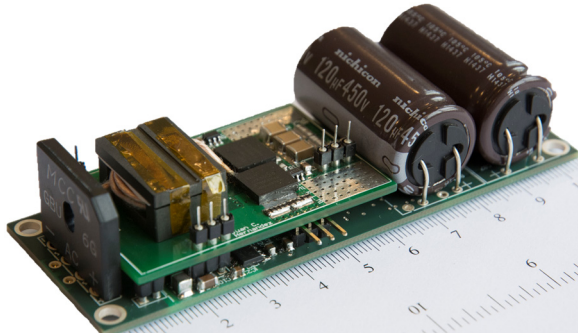


Fig. 13. Integration of the proposed ZVS control and power stage PCBs.

implementation because in this voltage range Si based Superjunction devices suffer from a very large Q_{OSS} charge, which makes them not a suitable choice for very high switching frequency operation. A flat current shunt structure, as presented in [14], [15], [16], is used for zero current detection purposes. This structure allows to maximize the current measurement bandwidth without resulting in large resistive losses or having a large effect on the loop inductance.

Fig. 14 shows the converter switching node voltage v_{DS} , the derivative of the switching node voltage v_{DSder} and the inductor current i_L . The switching node voltage derivative, which, is obtained from the auxiliary winding voltage, is used to determine the main MOSFET turn on instant, and the sampling instant for the ZVS regulation loop.

Fig. 15 shows the converter operating waveforms under extended ZVS operation for $v_{in} = 75$ V and $v_{out} = 110$ V. The reference for regulating the switching node voltage under valley switching conditions is adjusted to produce a value higher than zero, which is set intentionally to make the retained sampled value more visible compared to the v_{DS} waveform. The bottom trace shows the voltage in the first sample and hold cell capacitor $v_{CS\&H-1}$. When the synchronous rectifier is turned on, the first sample and hold switch is turned on and the sampling capacitor voltage is equal to the reconstructed switching node voltage. When the converter switching node derivative reaches zero after the synchronous rectifier is turned off, the first sampling cell will retain the sampled voltage until the next switching cycle. As it can be observed, after the inductor current reaches zero, the implemented control scheme extends the synchronous rectifier conduction time to regulate the switching node voltage based on the stored sample.

Fig. 16 shows the measured control-to-sample plant transfer function $\hat{v}_{sample}/\hat{v}_{error_SR}$ under the conditions depicted in Fig. 15. As it can be observed the plant transfer function behaves accordingly to the proposed gain with ZOH model.

Fig. 17 shows the converter operating waveforms in voltage mode control or constant on time, under a 50 Hz input ac voltage. As it can be observed, the converter operates

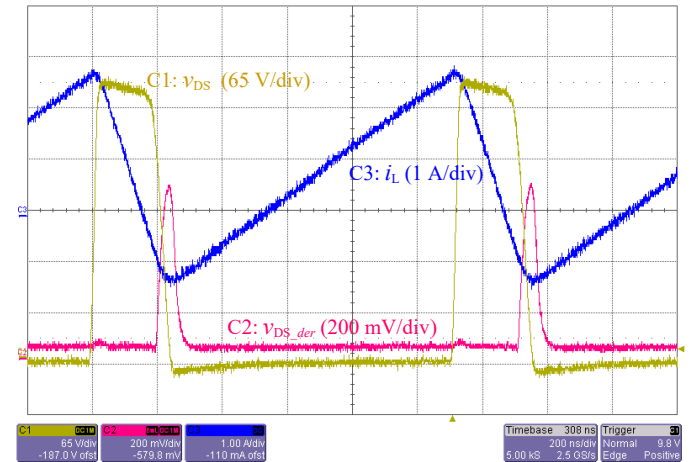


Fig. 14. Converter operating waveforms under extended ZVS operation. C1: switch drain to source signal v_{DS} (65 V/div), C2: switching node voltage derivative v_{DSder} (200 mV/div), C3: inductor current i_L (1 A/div). Time scale: 200 ns/div.

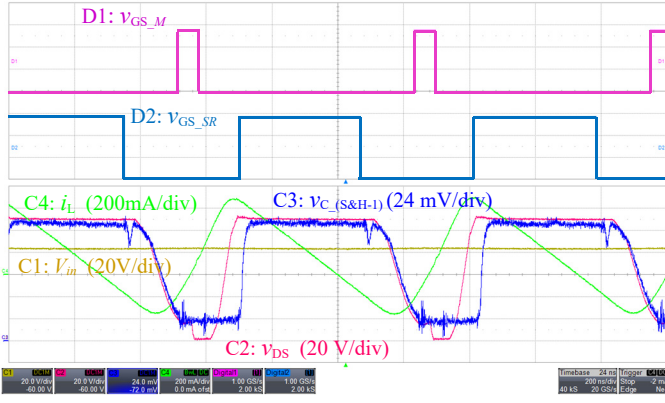


Fig. 15. Converter operating waveforms under extended ZVS operation. Top digital channels: D1: main switch gate signal v_{GS_M} and D2: synchronous rectifier gate signal v_{GS_SR} . Bottom analog channels: C1: converter input voltage V_{in} (20 V/div), C2: converter switching node voltage v_{DS} (20 V/div), C3: first sample and hold cell capacitor voltage $v_{CS,S\&H-1}$ (24 mV/div), and C4: inductor current i_L (200 mA/div). Time scale: 200 ns/div.

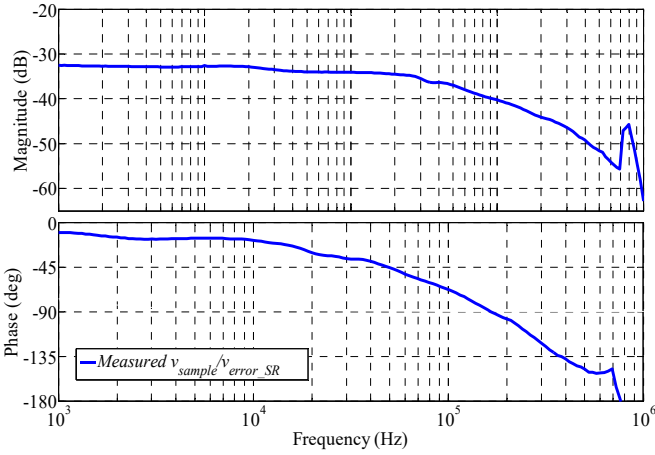


Fig. 16. Measured control-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{error_SR}$ transfer function.

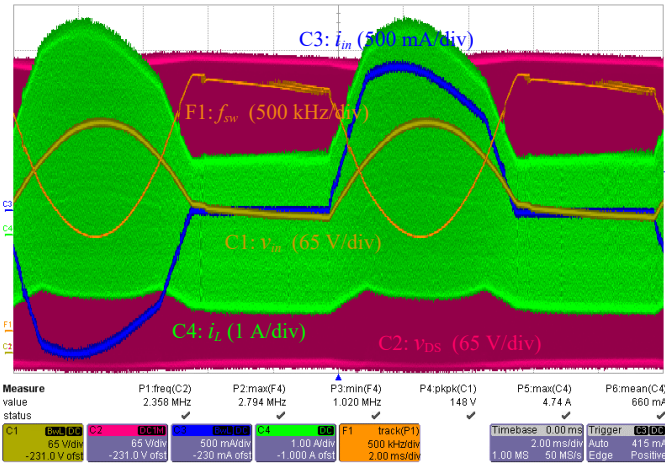


Fig. 17. ZVS converter operating waveforms across the line cycle in voltage mode control. C1: converter input voltage after the rectifier v_{in} (65 V/div), C2: switch drain to source signal v_{DS} (65 V/div), C3: converter input current i_{in} (500 mA/div), C4: inductor current i_L (1 A/div), F1: converter switching frequency f_{sw} (500 kHz/div). Time scale: 2 ms/div.

with a low power factor due to the large amount of reactive energy. As it can be seen, the converter operates with a switching frequency range $f_{sw} = [1 - 2.8 \text{ MHz}]$ for $P_{out} = 200 \text{ W}$ and $V_{ac_rms} = 230 \text{ V}$.

Fig. 18 shows a detail of the converter operating waveforms under ZVS conditions at $V_{ac_rms} = 230 \text{ V}$ ac line input, when the rectified input voltage is maximum. In this figure it can be observed how the synchronous rectifier extra conduction time t_e is controlled to reach a negative inductor current value i_L that ensures ZVS operation of the converter. As it can be observed, ZVS is also achieved when the converter input voltage (C1) is higher than half of the output voltage (whose value corresponds to the switching node voltage (C2) during the synchronous rectifier conduction time), which is the condition for losing the ZVS under conventional valley switching operation. However, a slight rise of the switching node voltage can be observed after the minimum switching node voltage is reached. This behavior is caused by the MOSFET gate driver UCC27511 propagation delay and rise time ($\approx 20 \text{ ns}$).

On the other hand, by looking into Fig. 19, it can be observed, that under this operating mode, as in any conventional BCM implementation with valley switching operation and constant main switch on time, the obtained power factor will be degraded as the converter switching frequency is increased. The reason is that control schemes for valley switching with constant on time, rely on the fact that the average input inductor current will be proportional to the converter input voltage, as long as a constant on time duration is kept for the main switch across the input line cycle. This is a valid assumption, as long as an ideal BCM conduction mode is maintained for the inductor current (meaning the boost switch will be turned on at the next cycle, exactly when the inductor current discharges down to zero). However, as soon as valley switching operation, or extended ZVS operation are introduced, the negative part of the inductor current resulting from the resonant interval, will make this average inductor current value no longer proportional to the input voltage value. The power factor values will be decreased, as the reactive

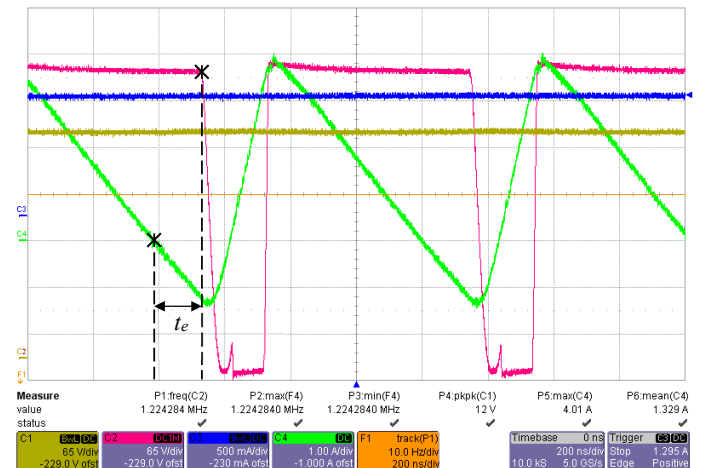


Fig. 18. Detail of the ZVS operation for maximum converter input voltage across the line cycle. C1: converter input voltage after the rectifier v_{in} (65 V/div), C2: switch drain to source signal v_{DS} (65 V/div), C3: converter input current i_{in} (500 mA/div), C4: inductor current i_L (1 A/div). Time scale: 200 ns/div.

power from the resonant periods is increased (increased switching node capacitance and switching frequency) compared to the processed active power. As can be seen from the converter operating waveforms in Fig. 16, under constant on time control, and at these operating frequencies, the large amount of negative inductor current, results in a poor power factor. A different scheme with a variable turn on time, or an inner average current loop, can be implemented in order to improve the circuit power factor. The fast dynamics involved in the proposed ZVS control method makes it possible to implement this approach, while using control schemes with more demanding bandwidth requirements compared to the constant on time regulation. In order to demonstrate this, the proposed control scheme shown in Fig. 7, is modified with a multiplier and an inner current loop to implement an average current control. Fig. 19 shows the converter operating waveforms in average current mode control with a 50 Hz input ac voltage. As it can be observed, under this operating scheme, the converter power factor is greatly improved. In this case, the input current amplifier compensates for the main switch on time t_{on} (C1) across the line cycle, while the ZVS control adjust the synchronous rectifier extra conduction time t_e (C2) without any visible interactions between both control loops.

Fig. 20 presents the measured converter efficiency as a function of the output power with the following operating conditions: $T_{amb} = 25^\circ\text{C}$, $V_{out} = 380\text{ V}$, $V_{ac_rms} = 230\text{ V}$. European mains input voltage is selected in this application, because no advantage would be obtained under US mains input voltage in this specific application. As presented in [9], and as it can be derived from Section II, the efficiency improvement will depend on the converter input to output voltage ratio, and it will be more advantageous under high ac mains input voltage. In order to observe the benefits of the ZVS scheme, a comparison of ZVS and non ZVS control is performed by modifying the control circuitry. As it can be seen, the difference in efficiency at low power levels is clear due to the increased converter operating frequencies and the ratio between active and reactive power in the circuit. The converter switching frequency largely increases near the zero

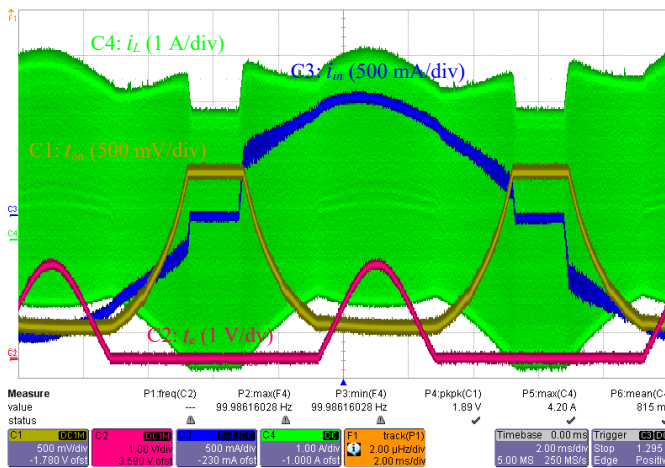


Fig. 19. ZVS converter operating waveforms across the line cycle in current mode control. C1: main MOSFET turn on time t_{on} (500 mV/div), C2: synchronous rectifier extra conduction time t_e (1 V/div), C3: converter input current i_{in} (500 mA/div), C4: inductor current i_L (1 A/div). Time scale: 2 ms/div.

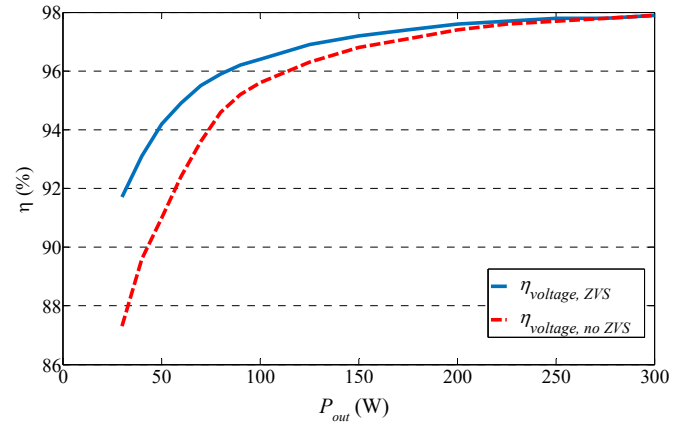


Fig. 20. Converter efficiency vs. output power including the bridge rectifier @ $T_{amb} = 25^\circ\text{C}$, $P_{out} = 300\text{ W}$, $V_{ac_rms} = 230\text{ V}$ and $V_{out} = 395\text{ V}$.

crossings of the input line voltage waveform, as it can be observed in Fig. 17, making the ZVS control crucial to achieve high efficiency operation.

V. CONCLUSION

BCM or CrM mode implementations are gaining popularity due to the integration of wide band-gap GaN semiconductors. Various GaN based BCM converters have been reported in the literature operating in the MHz switching frequency range. It is proven that the increased current stress in BCM implementations using GaN devices is compensated by the reduction in switching losses at the main switch turn on event due to ZCS and ZVS or valley switching conditions. However, the ability of the converter to operate under ZVS conditions, or the amount of energy recovered under valley switching conditions, is determined by the switching node capacitance and the converter input to output voltage ratio M . On the other hand, extension of the ZVS range is possible in implementations using synchronous rectification, which is achieved by extending the synchronous rectifier conduction time after zero current condition at the inductor. This operation mode enables high efficiency MHz implementations independently of the converter operating conditions. However, no previous research has addressed an adaptive control method for this operating mode. As discussed before, previously proposed solutions are based on experimental characterization data making this operation mode non feasible due to component tolerances and variations in the propagation delay times. This work presents and validates a self-regulating control method capable of regulating the synchronous rectifier conduction time based on a regulation loop of the switching node conditions. The proposed method is validated through simulation and experimental results. Moreover, a model is derived to analyze the controllability of the switching node voltage switching conditions. The proposed model is verified and proves the feasibility of the presented control method to achieve ZVS under fast perturbations of the converter operating conditions. Experimental efficiency measurements demonstrate the improvement of using the proposed control method, especially under light load conditions. This solution is demonstrated on a boost PFC circuit, however, this implementation can be employed in other topologies and applications.

REFERENCES

- [1] O. Kiltie, "New Type of D-C to A-C Vibrator Inverter," Am. Inst. Electr. Eng. Trans., 1940.
- [2] W. H. Morman, M. H. Ramsey and R. G. Hoft, "50-kW Thyristor DC-to-DC Converter," Ind. Appl. IEEE Trans., Vols. IA-8, no. 5, p. 617–635, 1972..
- [3] M. Kohno and K. Kuwabara, "Single-ended Dc-to-dc Converter With Two Individually Controlled Outputs," in International Telephone Energy conference, 1978. INTELEC 78., Washington, DC, USA, 1978.
- [4] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. P. Madsen, M. Kovacevic and M. A. E. Andersen, "Evolution of Very High Frequency Power Supplies," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 386-394, 2014.
- [5] X. Huang, Z. Liu, Q. Li and F. C. Lee, "Evaluation and Application of 600 V GaN HEMT in Cascode Structure," IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2453-2461, 2014.
- [6] X. Huang, Z. Liu, F. C. Lee and Q. Li, "Characterization and Enhancement of High-Voltage Cascode GaN Devices," IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 270-277, 2015.
- [7] J. C. Hernandez, L. P. Petersen and M. A. E. Andersen, "Characterization and evaluation of 600 V range devices for active power factor correction in boundary and continuous conduction modes," in IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 2015.
- [8] J. C. Hernandez, L. P. Petersen and M. A. E. Andersen, "A comparison between boundary and continuous conduction modes in single phase PFC using 600V range devices," in IEEE 11th International Conference on Power Electronics and Drive Systems, Sydney, NSW, Australia, 2015.
- [9] B. Su, J. Zhang and Z. Lu, "Totem-Pole Boost Bridgeless PFC Rectifier With Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM," IEEE Transactions on Power Electronics, vol. 26, no. 2, pp. 427-435, 2011.
- [10] Z. Liu, X. Huang, M. Mu, Y. Yang, F. C. Lee and Q. Li, "Design and evaluation of GaN-based dual-phase interleaved MHz critical mode PFC converter," in IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 2014.
- [11] Z. Wang, S. Wang, P. Kong and F. C. Lee, "DM EMI Noise Prediction for Constant On-Time, Critical Mode Power Factor Correction Converters," IEEE Transactions on Power Electronics, vol. 27, no. 7, pp. 3150-3157, 2012.
- [12] Y. Yang, Z. Liu, F. C. Lee and Q. Li, "Analysis and filter design of differential mode EMI noise for GaN-based interleaved MHz critical mode PFC converter," in IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 2014.
- [13] C. Marxgut, J. Biela and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," in International Power Electronics Conference (IPEC), Sapporo, 2010.
- [14] C. Marxgut, F. Krismer, D. Bortis and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 873-882, Feb. 2014.
- [15] Q. Huang, R. Yu, Q. Huang and W. Yu, "Adaptive zero-voltage-switching control and hybrid current control for high efficiency GaN MHz Totem-pole PFC rectifier," in IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.
- [16] Z. Liu, F. C. Lee, Q. Li and Y. Yang, "Design of GaN MHz totem-pole PFC rectifier," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 799-807, Sept. 2016.
- [17] K. Ogata, Modern Control Engineering, 4th ed. Prentice Hall.
- [18] J. A. Ferreira, W. A. Cronje and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits," IEEE Transactions on Power Electronics, vol. 10, no. 1, pp. 32-37, 1995.
- [19] J. C. Hernandez, L. P. Petersen and M. A. E. Andersen, "Ultrafast switching superjunction MOSFETs for single phase PFC applications," in IEEE Applied Power Electronics Conference and Exposition - APEC, Fort Worth, TX, USA, 2014.
- [20] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 2011.



Juan C. Hernandez received the M.Sc. degree in Electrical Engineering and the Ph.D. degree from the Technical University of Denmark, 2012 and 2016, respectively. Since 2017 he has been with ICE Power A/S where he is a Research and Development engineer working with offline converters and switch mode power amplifiers. His main interests include resonant converters, class D amplifiers, and active power factor correction.



Maria C. Mira received the B.Sc. degree in Telecommunications from Miguel Hernandez University, Elche, Spain, in 2009. She received the M.Sc. degree in Electrical Engineering and the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2012 and 2016, respectively. She was a Postdoctoral Researcher at the Technical University of Denmark in 2017 - 2018. Her research interests include modeling and control of switched-mode power supplies, bidirectional converters, and three-port converters for renewable energy systems.



Lars P. Petersen received the master's degree in electrical engineering and the Ph.D. degree in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1999 and 2003, respectively. In 2003, he joined Bang&Olufsen working with offline converters for Class D amplifiers. In 2008, he founded Upcon Technology A/S, a start-up company developing high-efficiency ac/dc converters for telecom and server applications. From 2012, he was a Senior Researcher at the Technical University of Denmark. In 2016 he joined ICE Power A/S where he is Chief Technical Officer. His interests are high power density dc/dc converters and class D amplifiers.



Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor of power electronics at the Technical University of Denmark, where since 2009, he has been the Deputy Head of the Department of Electrical Engineering. He is the author or coauthor of more than 300 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.



Niels H. Petersen received the M.S. degree in Electrical Engineering from Technical University of Denmark, Lyngby, Denmark, in 1985. He was employed at Speed Control A/S from 1985-1990, as Development Engineer. Since 1990, he has been with Grundfos Holding A/S where he currently is Chief Specialist, Power Electronics at Grundfos Core Technology working with power semiconductor technology and he is responsible for power electronics.