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# Wafer bonded CMUT technology utilizing a Poly-Silicon-on-Insulator wafer

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**Abstract**—This paper presents a fabrication process of a Poly-Silicon-On-Insulator (PSOI) wafer that can be used as an alternative to conventional Silicon-On-Insulator (SOI) wafers for fabrication of Capacitive Micromachined Ultrasound Transducers (CMUT). The fabrication of PSOI wafers does, unlike the conventional SOI fabrication, not involve any bonding steps. A batch of PSOI wafers having a 400 nm BOX layer and a  $2.6 \mu\text{m} \pm 0.04 \mu\text{m}$  ( $1\sigma$ ) device layer is fabricated and characterized. A surface roughness of 0.47 nm is measured for the PSOI device layer, and successful fusion bonds (direct bonds) are demonstrated between PSOI wafers and oxidized silicon wafers. A wafer-bonded CMUT using a PSOI wafer is fabricated and electrically characterized, and the expected CMUT performance is observed. Impedance spectra are demonstrated at five different DC biases, the expected spring softening effect is observed when the magnitude of the DC bias is increased.

## I. INTRODUCTION

Silicon-On-Insulator (SOI) wafers are today routinely used in the semiconductor industry and have been applied for numerous applications ranging from P/N junctions [1], Optical applications [2], and in particular for applications in the industry of Micro Electrical Mechanical Systems (MEMS) [3]. The target application for this paper is the Capacitive Micromachined Ultrasound Transducer (CMUT), a technology developed in the 1990's [4] that falls into the category of MEMS devices where SOI wafers are commonly used. The basic structure of a SOI wafer consists of a device layer, a buried oxide layer (BOX), and a handle wafer (substrate). The device layer of the SOI wafer is used in CMUT applications as the vibrating plate or membrane. The device layer of SOI wafers used for wafer bonded CMUTs are required to have bondable surfaces, low electrical resistivity, predictable mechanical stiffness, and preferably a uniform device layer thickness,  $h$ . Monocrystallinity of the device layer is not important for CMUT applications, but, it is essential for other SOI based applications. The ability to customize the thickness and resistivity of the individual layer provides great freedom in a MEMS design. The fabrication processes of CMUTs are either based on a sacrificial release [5] and wafer bonding step, where the latter is the main focus of this work. Several wafer bonding techniques have been demonstrated for CMUT applications [6]–[8]. The device layer thickness, of conventional SOI wafers, can be specified from hundreds of microns down to  $2 \mu\text{m}$  with a uncertainty of  $0.3 \mu\text{m}$ . The SOI wafers used for CMUT applications are typically close to the lower limit, and have typically device layers less than  $10 \mu\text{m}$ .

However, CMUT plates (device layer) thinner than  $2 \mu\text{m}$  plate are highly desirable in some CMUT designs, especially for high frequency or high bandwidth applications. Hence, it becomes challenging for such applications to get the desired wafer specification when conventional SOI wafers are used. A thinner device layer can be obtained by thermally oxidize the SOI wafers and remove the grown oxide subsequently. This process can be controlled with high precision, but, the relative thickness variation increases, since, the uncertainty of the device layer thickness is unaffected by the oxidation process. Variations of the plate thickness,  $h$ , across a CMUT array influence important characteristic CMUT parameters such as resonance frequency and pull-in voltage, which scales with  $h$  and as  $h^{3/2}$ , respectively. Thus, tight control of the plate thickness is necessary for having equal performance of all CMUT in an array. The objective of this paper is to demonstrate the Poly-silicon-On-Insulator wafer as a rapid prototyping tool for CMUT fabrication. The PSOI technology is required to be non-inferior to the already existing SOI technology measured by important CMUT characteristics, such as reliable bonding properties, sufficient electrical properties and uniform device layer thickness across the wafer. Fusion bonded CMUTs must be demonstrated to verify non-inferiority of the PSOI technology, since fusion bonding is more sensitive in terms of surface roughness and cleanliness compared to other techniques such as anodic bonding and polymer bonding. The majority of the CMUTs demonstrated found in the literature have plate thicknesses less than  $5 \mu\text{m}$  and it will therefore be considered as the upper bound of the device layer. In addition, the device layer resistivity should be less than  $1 \Omega\text{cm}$  to be interesting for CMUT applications.

## II. FABRICATION

### A. Fabrication of PSOI wafers

The fabrication process of conventional SOI wafers consists of few steps, first an oxide is grown on a silicon substrate (wafer A) and the oxide surface is thereafter fusion bonded to a new silicon wafer (wafer B). The oxide defines the BOX layer and wafer A defines the handle layer. The device layer is made by wafer B, the thickness is adjusted to match the desired specifications by removing silicon in a grinding process. Finally, a chemical mechanical polishing (CMP) is carried out to obtain the same surface standard as conventional silicon wafers [9]. The fabrication process of PSOI wafers is similar to the fabrication of conventional SOI. However, the

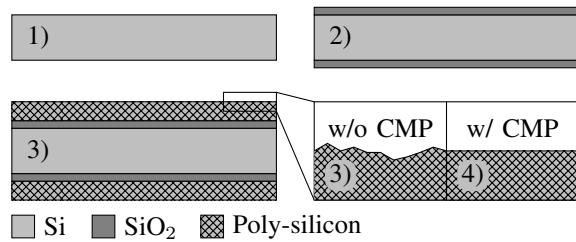


Fig. 1. Fabrication process of PSOI wafers. 1) A standard silicon wafer is RCA cleaned. 2) A thermal oxide is grown. 3) Poly-silicon is deposited in an LPCVD process. 4) The poly-silicon layer is polished (CMP) to reduce surface roughness. Figure is not to scale.

device layer is deposited using a Low Pressure Chemical Vapor Deposition (LPCVD) process instead of being bonded to the oxide surface. The fabrication of PSOI wafers consists of four steps as shown in Fig. 1.

The first step in the PSOI fabrication is a RCA clean of a silicon wafer. This wafer will end up as the handle layer and electrical properties, doping type, and wafer thickness should therefore match desired specifications. In step 2, an oxide is thermally grown that constitutes the BOX layer. A 400 nm dry oxide grown at 1100 °C is used for the PSOI wafers fabrication in this work. The device layer is created in step 3, where a boron doped poly-silicon is deposited using a LPCVD process. The equivalent could be obtained by a phosphor doped poly-silicon, but the deposition rate is substantially lower.

Finally, in step 4, the poly-silicon surface is polished using a Logitech CM62 Orbis Chemical Mechanical Polishing (CMP) machine. The final poly-silicon thickness of a fabricated PSOI has been measured across the wafer using multi-angle reflectometry measurements, the resulting thickness map is shown in Fig. 2. A mean thickness of 2.60  $\mu\text{m}$  with a standard deviation of 0.04  $\mu\text{m}$  has been measured. Additionally, the difference between minimum and maximum thickness is measured to be 0.26  $\mu\text{m}$ , hence, in full compliance with the non-inferior constraint. The surface roughness, of the deposited LPCVD poly-silicon, has been measured using a PLu neox Optical Profiler (confocal microscope) to 6.98 nm prior to the CMP process and 0.47 nm after the CMP process. The true surface roughness could be lower, since these measurements are at the resolution limitation of the confocal microscope. A surface roughness of approximately 0.5 nm has also been measured on a reference silicon wafer. A surface roughness of less than 1 nm is required to achieve successful fusion bond and preferably even lower [10]. The CMP process is therefore essential for fusion bonding to be successful.

The mechanical and electrical properties of a LPCVD poly-silicon are influenced by multiple parameters, including deposition temperature, deposition time, gas composition, tube pressure, and flow conditions among other. The deposition rate of the LPCVD poly-silicon should be high enough to produce 5  $\mu\text{m}$  poly-silicon layer within a reasonable time. At the same time the built-in stress should preferably be tensile and the resistivity should be low. A tensile stress in the poly-

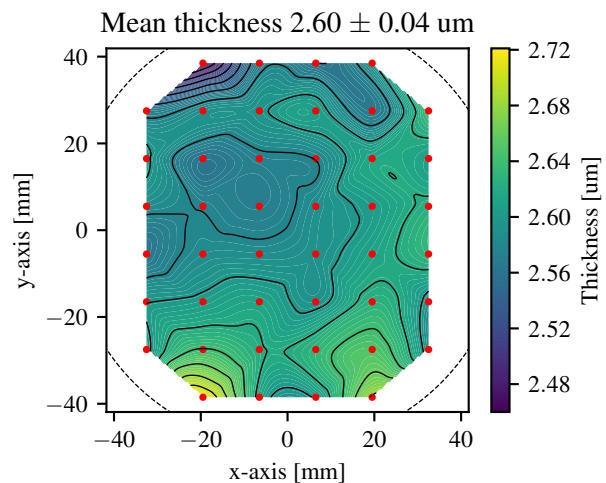


Fig. 2. Interpolated thickness map of a PSOI device layer measured using multi-angle reflectometry. The circumference of the wafer is indicated by the dashed black line, and the 44 red dots indicate the spatial positions of the data points used to generate the thickness map.

silicon prohibits buckling effects in the final CMUT structure. An acceptable resistivity parameter space depends on the CMUT application, and a criterion that describes when the resistivity is low enough for acceptable CMUT performance can be found in [11]. Four point probe measurements of 19 PSOI wafers have been conducted to estimate the resistivity of the device layer, the mean and standard deviation were 0.036  $\Omega\text{cm} \pm 0.019 \Omega\text{cm}$ , and the highest measured resistivity was 0.062  $\Omega\text{cm}$ . Depositing rate, thin film stress, and resistivity do all depend on the deposition temperature [12]–[17], and quantitative values of these parameters are plotted in Fig. 3.

The material properties of the deposited poly-silicon vary from lab to lab, and the data should be interpreted as tendencies and not absolute values. The deposition rate is seen, in Fig. 3 a), to increase as the deposition temperature increases, whereas a reduction in the resistivity is observed in Fig. 3 b) (notice the log y-scale). Hence, rapid fabrication time and low resistivity are obtained by an increased deposition temperature. However, the temperature dependency of the stress is not unambiguous as the deposition rate and resistivity, and extrapolation is therefore difficult. Fusion bonded CMUTs require an annealing step at temperatures on the order of 1000 °C, and annealing time and temperature do also influence the stress and resistivity. The highest process temperature is, however, significantly lower for other CMUT fabrication methods such as anodically bonded CMUTs, where the highest process temperature is on the order of 350 °C [7]. The resistivity and stress values from Fig. 3 b) and c) are therefore directly applicable for anodically bonded CMUTs, but are perturbed during annealing for fusion bonded CMUTs. The minimum device layer thickness for conventional SOI wafers are limited to 2  $\mu\text{m}$ , but, the PSOI technology can provide a device layer ranging from approximately 10 nm

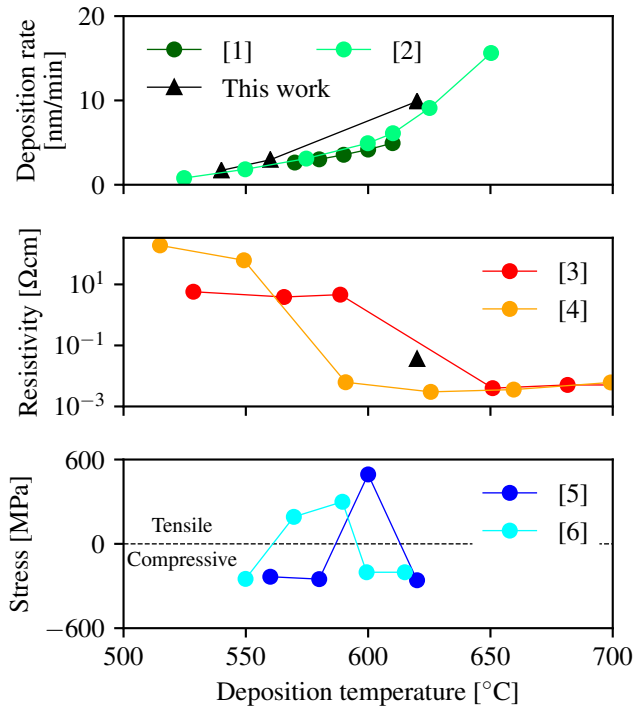


Fig. 3. The deposition rate, resistivity, and stress as function of deposition temperature. The circular markers are from the literature and represents either boron doped or undoped LPCVD poly-silicon and triangular markers indicate measurements of LPCVD boron doped poly-silicon from this work.

TABLE I  
VARIOUS MEASURED PSOI PARAMETERS

Parameter	Samples [#]	Upper bound
Device layer thickness variations	2	$<0.3 \mu\text{m}$
Surface roughness	1	$0.47 \text{ nm}$
Wafer bow	10	$<20 \mu\text{m}$
Device layer resistivity	19	$<0.062 \Omega \text{ cm}$

to  $5 \mu\text{m}$ , and is limited by how thin or how thick layers the LPCVD system can deposit. But, the PSOI technology is also applicable for applications that require device layers of less than  $2 \mu\text{m}$ . The fabrication time of PSOI wafers is two-three days under the assumption of availability of an oxidation furnace, a LPCVD poly-furnace and a CMP machine. The PSOI technology provides a rapid and flexible technology platform for CMUT research and development, as an alternative to the conventional SOI wafers where the delivery time (months) can limit the iteration process of various CMUT designs.

An overview of various measured PSOI parameters can be found in Table I.

### B. Fabrication of CMUTs

The CMUTs in this work have been fabricated using a Local Oxidation of Silicon (LOCOS) process, first demonstrated in 2008 by [18] and described further in [19]. The LOCOS process has numerous beneficial properties for CMUT fabrication such as high dielectric strength, reduced parasitic capacitance, good uniformity, and the gap height can be

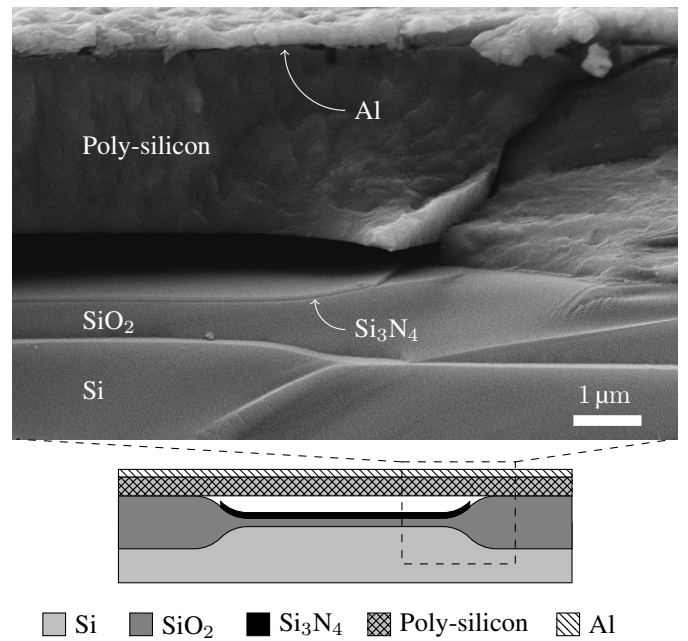


Fig. 4. Cross sectional SEM image of a CMUT fabricated using a PSOI wafer. A thin gold layer of a few nanometer has been sputter to reduce charging effects in the dielectric layers. A sketch of the designed LOCOS CMUT is inserted below the SEM image.

controlled with nanometer precision. The PSOI wafer and the processed LOCOS substrate wafer were both RCA cleaned prior to the fusion bonding process, and pre-bonded using a Süss SB6 wafer bonder, followed by an annealing step at  $1100^\circ\text{C}$  for 70 min. A cross sectional image of a fabricated CMUT has been acquired by a Scanning Electron Microscope (SEM) and shown in Fig. 4. A sketch of the structure has been inserted below the SEM image to illustrate the designed LOCOS structure. The CMUT plate is as expected composed of a polycrystalline material separated from the bottom of the CMUT cavity by the LOCOS bird's beak structure. The CMUT has been diced by an automatic dicing saw and the surface is observed to be frayed as a result of the dicing process.

### III. CMUT CHARACTERIZATION

The fabricated CMUTs have been electrically characterized by impedance measurements. The measurements were performed using an Agilent 4294A Precision Impedance Analyzer with five different DC biases and an AC voltage of  $100 \text{ mV}$ . The impedance magnitude and phase are plotted in Fig. 5 a) and b), respectively, where the expected CMUT behaviour is observed. A distinct resonance frequency is observed in the frequency range between  $5 \text{ MHz}$  and  $6.5 \text{ MHz}$ , and the spring softening effect is confirmed by the frequency shift towards lower frequencies as the magnitude of the DC bias is increased. In addition the phase is approximately, in Fig. 5 b),  $-90^\circ$  for all off-resonance frequencies up to  $10 \text{ MHz}$ , which verifies the expected capacitive properties for the CMUT. The impedance

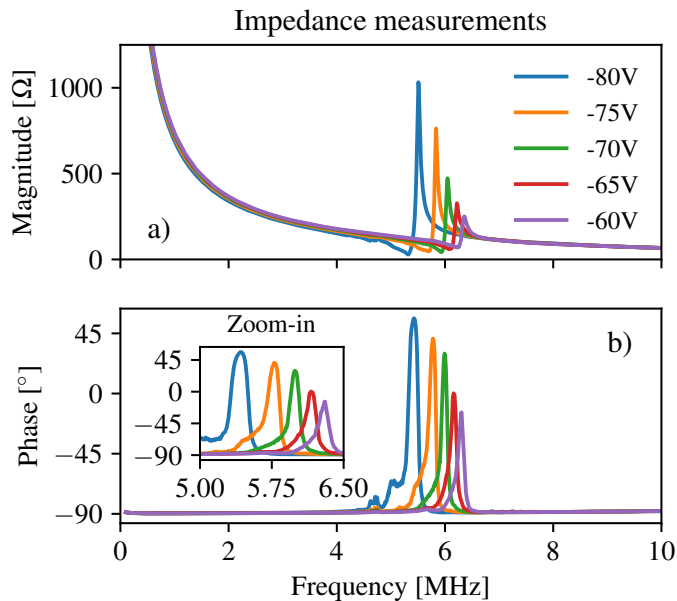


Fig. 5. Impedance measurements of a fabricated CMUT at five different DC biases. The expected spring softening effect is observed for an increased DC magnitude. The applied bias ramp corresponds to 72.2%, 77.8%, 83.3%, 88.9%, 94.4% of the pull-in voltage.

measurements demonstrate the technological potential of PSOI wafers as an alternative to conventional SOI wafer for MEMS devices.

#### IV. CONCLUSION

This paper presented a fabrication method of a Poly-Silicon-On-Insulator (PSOI) wafer. A PSOI wafer was demonstrated applicable for CMUT applications as an alternative to conventional Silicon-On-Insulator (SOI) wafers. Fabrication of PSOI wafers can reduce iteration time for wafer bonded CMUTs, and the device layer of a PSOI wafer can be fabricated thinner than a conventional SOI. The device layer thickness of a fabricated PSOI wafer was measured using multi-angle reflectometry and yielded a mean thickness of  $2.60\ \mu\text{m}$  with a standard deviation of  $0.04\ \mu\text{m}$ . A mean resistivity of 19 PSOI wafers were characterized by four point probe measurements and measured to  $0.36\ \Omega\ \text{cm} \pm 0.19\ \Omega\ \text{cm}$  ( $1\sigma$ ). A surface roughness of  $0.47\ \text{nm}$  was determined by confocal microscopy, and a bondable surface properties was demonstrated by fabrication of a functional fusion bonded CMUT. An impedance analysis of the fabricated CMUT showed the expected CMUT behaviour. A distinct resonance frequency was observed for five different DC biases, and the spring softening effect was confirmed by a frequency shift as the magnitude of the applied DC bias was increased.

#### V. ACKNOWLEDGEMENT

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