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Natasha Goyal,[1] David M. A. Mackenzie,[2] Vishal Panchal,[3] Himani Jawa,[1] Olga Kazakova,[4] Dirch Hjorth Petersen,[5] and Saurabh Lodha[1,a)]

AFFILIATIONS

[1]Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India
[2]Department of Electronics and Nanoengineering, Aalto University, PO Box 13500, FI-00076 Aalto, Finland
[3]Time, Quantum and Electromagnetics division, National Physical Laboratory, Teddington, Middlesex TW11 0LW, United Kingdom
[4]Quantum Technology, National Physical Laboratory, Teddington, Middlesex TW11 0LW, United Kingdom
[5]Department of Physics, Technical University of Denmark, Fysikvej, Building 311, DK-2800 Kgs. Lyngby, Denmark

[a)]Electronic mail: slodha@ee.iitb.ac.in

ABSTRACT

Thermally varying hysteretic gate operation in few-layer ReS_2 and MoS_2 back gate field effect transistors (FETs) is studied and compared for memory applications. Clockwise hysteresis at room temperature and anti-clockwise hysteresis at higher temperature (373 K for ReS_2 and 400 K for MoS_2) are accompanied by step-like jumps in transfer curves for both forward and reverse voltage sweeps. Hence, a step-like conductance (STC) crossover hysteresis between the transfer curves for the two sweeps is observed at high temperature. Furthermore, memory parameters such as the RESET-to-WRITE window and READ window are defined and compared for clockwise hysteresis at low temperature and STC-type hysteresis at high temperature, showing better memory performance for ReS_2 FETs as compared to MoS_2 FETs. Smaller operating temperature and voltage along with larger READ and RESET-to-WRITE windows make ReS_2 FETs a better choice for thermally aided memory applications. Finally, temperature dependent Kelvin probe force microscopy measurements show decreasing (constant) surface potential with increasing temperature for ReS_2 (MoS_2). This indicates less effective intrinsic trapping at high temperature in ReS_2, leading to earlier occurrence of STC-type hysteresis in ReS_2 FETs as compared to MoS_2 FETs with increasing temperature.

Recently, two-dimensional (2D) layered materials have attracted significant research interest for memory applications. Thermally assisted non-volatile memories (NVMs) have been demonstrated using monolayer and few-layer MoS_2.[1,2] In several other reports, large hysteresis in transistor transfer curves, normally undesirable for device performance, has been utilized for NVM applications.[3–6] All of these reports use MoS_2 as the channel or as the charge trapping layer. In thermally assisted NVMs, locally generated heat is exploited for switching between different memory states. MoS_2 has shown excellent switching characteristics compared to other transition metal dichalcogenides (TMDs).[7] Low off current (I_{off}) and a high on/off current (I_{on}/I_{off}) ratio (due to a large bandgap) along with a low sub-threshold slope and high effective mass are some of the advantages of MoS_2, which make it a desirable switching material for memory applications.[8,9] Among the TMDs, ReS_2 has also garnered significant attention recently[10,11] since it behaves as decoupled monolayers stacked on top of each other due to the lack of interlayer coupling and weak interlayer registry.[12] Hence, ReS_2 remains a direct bandgap semiconductor ($E_G = 1.5$ eV) from monolayer to bulk, showing no direct to indirect bandgap crossover as is shown by other TMDs, making it a preferred material for optoelectronic applications.[10,13]

With the increasing packing density of field effect transistors (FETs) on a single wafer, high performance ICs can reach an operating temperature (T) of 370–530 K (Ref. 14), making it important to understand and exploit the changes that occur in the properties of 2D materials at high T. Thermally assisted memory is one such application where locally generated heat is exploited to aid the switching between RESET (RST/STATE 0) and WRITE (WR/STATE 1) states.[15] It can enable embedded in-memory computing that has emerged as a key hardware bottleneck for artificial intelligence/machine learning technologies. However, in-memory computing requires more computational power per unit volume of data storage in the RAM and parallel

TABLE I. Comparison of memory parameters obtained in this work with the previous reports on thermally assisted memory using MoS_2 as the channel material.

References	Material	Operating temperature	Operating voltage (V_{p-p})	RST-to-WR window ($\Delta V_{th}/V_{p-p}$)	RD window	Hysteresis type
1	Monolayer, MoS_2	490 K	−40 V to +40 V	0.44	5.5	STC + ACW
21	Monolayer, MoS_2	350 K	−30 V to +15 V	0.50	7	CW
22	Multilayer MoS_2	300 K	−30 V to +30 V	0.1	—	CW
This work	Few-layer MoS_2	400 K	−100 V to +60 V	0.16	1.9	STC + ACW
This Work	Few-layer ReS_2	375 K	−100 V to +30 V	0.58	7.4	STC + ACW

distributed processing. This increases the operational T of data centers, resulting in several reliability concerns.[16,17] Therefore, enabling low T memory operation in 2D materials is timely and relevant. In this study, thermally varying hysteretic gate operation, in few-layer MoS_2 and in few-layer ReS_2, is studied and compared for memory applications. Four-terminal back gate FETs are used in this study to eliminate the contribution from contact resistance.[18] Clockwise (CW) hysteresis is observed for both ReS_2 and MoS_2 at room temperature (RT), whereas anti-clockwise (ACW) hysteresis along with step-like jumps in the transfer curves leading to a conductance crossover between the forward sweep (FS, −100 V to +100 V) and reverse sweep (RS, +100 V to −100 V) directions (step-like conductance crossover hysteresis or STC hysteresis) is observed at high T. A similar behavior has been previously reported for monolayer MoS_2 FETs.[1] Here, we observe this behavior in both few-layer MoS_2 at 400 K and few-layer ReS_2 at 375 K, attributing the RT CW hysteresis to the dominance of native intrinsic traps and the conductance crossover at high T to charge exchange between the p^+ Si back gate and gate oxide SiO_2. The charge can be trapped in the oxide near the 2D channel/dielectric or the back gate/dielectric interface.[1,19,20] However, the latter is found to be dominating at high T in these systems.[2] A comparison of this work with previous reports on thermally assisted memory is presented in Table I.

We observe lower operating voltage (V_{p-p}), a larger RST-to-WR window, defined as $\Delta V_{th}/V_{p-p}$ (where ΔV_{th} is the hysteresis width), and a larger READ (RD) window for STC hysteresis in ReS_2 devices. Improved memory parameters for ReS_2 FETs at much lower T are attributed to a rapidly reducing effect of intrinsic traps with increasing T. This is verified by T-dependent Kelvin probe force microscopy (KPFM) measurements, which indicate the decreasing work function for ReS_2 (Φ_{ReS_2}) unlike an almost constant work function for MoS_2 (Φ_{MoS_2}) with increasing T.

Figure 1(a) shows an optical image (top) and a 3D schematic (bottom) of the four-terminal back gated transistor structure used to study thermally varying hysteretic gate operation for both MoS_2 and ReS_2 as the channel materials. The TMD sheets were mechanically exfoliated (using adhesive blue tape) from bulk crystals on heavily doped p-type silicon substrates with a 280 nm SiO_2 layer on top.[23,24] Optical microscopy was used to identify the flakes for further processing. Source/drain electrodes were then patterned using electron beam lithography followed by metal deposition. 10 nm Cr and 100 nm Au were used to form source/drain metal contacts with the flakes.

Figures 1 and 2 show the conductance (G) vs back gate voltage (V_{GS}) curves for varying T. Figures 1(d) and 2(d) define the RST, RD, and WR operations for the ReS_2 and MoS_2 memories, respectively. All the measurements reported in this work start with the FS followed by RS. We observe two significant step-like jumps in the G-V_{GS} plots at higher T. The first one occurs during FS at 20 V for ReS_2 [Fig. 1(d)] and at 35 V [Fig. 2(d)] for MoS_2. The second one occurs during RS at −76 V for ReS_2 [Fig. 1(d)] and −66 V for MoS_2 [Fig. 2(d)]. As a result STC hysteresis emerges at 373 K and 400 K for ReS_2 and MoS_2, respectively. These jumps can be prominently observed in the transconductance (g_m) curves in Figs. S1(a) and S1(b) of the supplementary material for ReS_2 and MoS_2, respectively. Along with the jumps occurring at higher T, a switch from CW hysteresis at RT to ACW hysteresis at higher T can also be observed in the transfer curves for both ReS_2 and MoS_2.

The changing hysteresis behavior with varying T is shown in Figs. 3(a) and 3(b) via the change in threshold voltage (V_{th}) for FS (STATE 1, V_{th}^{FS}) and RS (STATE 0, V_{th}^{RS}) with T for MoS_2 and ReS_2, respectively. A transition from CW ($V_{th}^{FS} < V_{th}^{RS}$) to ACW ($V_{th}^{FS} > V_{th}^{RS}$) hysteresis with increasing T can be observed. A larger hysteresis width ($\Delta V_{th} = V_{th}^{RS} - V_{th}^{FS}$) for ReS_2 at much lower T compared to MoS_2 can also be seen. As marked in Figs. 1(d) and 2(d), WR and RST operations are carried out at the end of FS and RS, respectively. A larger ΔV_{th} implies a larger RST-to-WR window, a desirable feature for

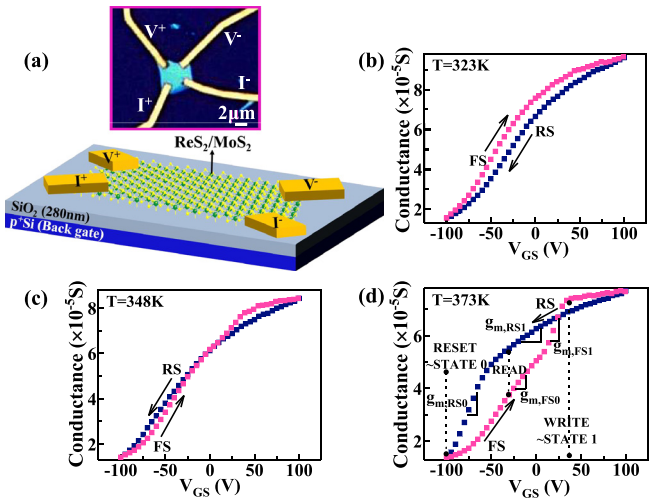

FIG. 1. (a) Optical image (top) and schematic (bottom) of back-gated vdP FETs with the ReS_2/MoS_2 channel. G(S) vs V_{GS}(V) at $V_d = 2$ V for ReS_2 FET showing the evolving hysteresis width with increasing T at (b) 323 K, (c) 348 K, and (d) 373 K, depicting STATES 0 and 1 corresponding to WRITE (WR) and RESET (RST), respectively.[25]

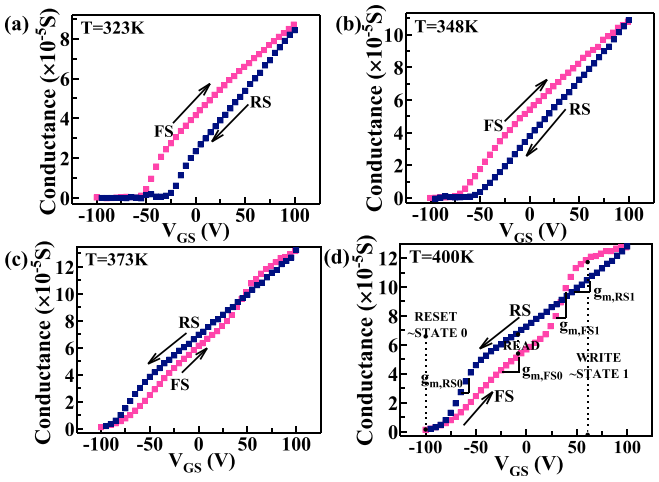

FIG. 2. G(S) vs V_{GS}(V) at $V_d = 0.5$ V for MoS_2 FET showing the evolving hysteresis width with increasing T at (a) 323 K, (b) 348 K, (c) 373 K, and (d) 400 K, indicating memory STATE 0 and STATE 1.[25]

memory operation. Hence, a larger RST-to-WR window is observed for ReS_2 as compared to MoS_2. Figure 3(c) shows the ratio of g_m closer to STATE 0 ($g_{m,RS0}$ for RS and $g_{m,FS0}$ for FS) to g_m closer to STATE 1 ($g_{m,RS1}$ for RS and $g_{m,FS1}$ for FS) as marked in Figs. 1(d) and 2(d). The difference between $g_{m,RS0}/g_{m,RS1}$ and $g_{m,FS0}/g_{m,FS1}$ is defined as the RD window, which rapidly increases with increasing T for ReS_2 at much lower T as compared to MoS_2.

When T is increased from RT to higher T, a change from CW to ACW hysteresis along with step-like jumps occurs during both FS

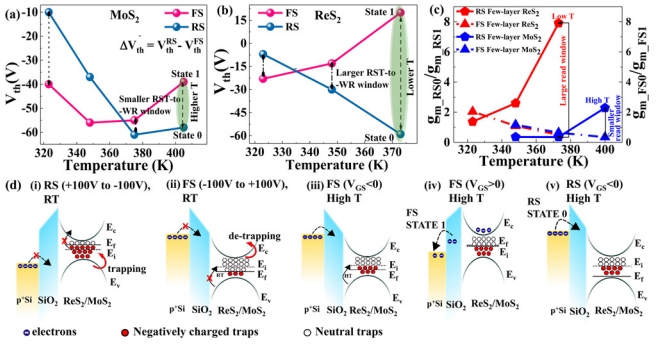

FIG. 3. The change in V_{th}^{FS} and V_{th}^{RS} with varying T for (a) MoS_2 and (b) ReS_2. The shaded green region shows a larger RST-to-WR window for ReS_2 as compared to MoS_2, at much lower T. (c) g_m ratios for ReS_2 and MoS_2 devices during FS and RS close to STATE 0 and STATE 1.[25] (d) Band diagrams of the back-gated FETs with ReS_2/MoS_2 as the channel material. At RT, (i) the onset of RS moves the Fermi level (E_f) closer to conduction band minimum (E_c), which leads to electron (e^-) trapping below E_f (shown by the solid red arrow), while (ii) the onset of FS causes the de-trapping of e^- that are above E_f. As T increases, the intrinsic traps can be occupied by e^- at all voltages due to the availability of thermionic energy. Therefore, at higher T, during FS, (iii) when $V_{GS} < 0$, e^- from the p^+-Si gate jump into the oxide (dashed arrow) screening the applied V_{GS}, while (iv) for $V_{GS} > 0$, these e^- jump back to the gate, causing the first g_m jump (STATE 1). (v) During RS when $V_{GS} < 0$, e^- from the gate jump again to the oxide re-screening V_{GS}, resulting in the occurrence of the second g_m jump (STATE 0).

(leading to STATE 1) and RS (leading to STATE 0). We attribute the fading away of the CW hysteresis with increasing T to electron (e^-) trapping and de-trapping into the deep level channel traps that occur due to intrinsic defects in materials, as previously reported for fully depleted channels.[2,26–28] At the onset of RS (+100 V), these traps below the Fermi level (E_f) get filled by e^-, and hence, an increase in V_{th} is observed [Fig. 3(d)–(i)], whereas at the onset of FS (−100 V), the bands closer to the SiO_2/channel interface bend to favor e^- de-trapping from the intrinsic traps, resulting in reduced V_{th} [Fig. 3(d)–(ii)]. As a result, CW hysteresis is seen at RT. At higher T, the deep level traps have an equal probability of getting trapped irrespective of the voltage applied, and hence, the hysteresis starts to fade away.[2] Instead, an ACW hysteresis with step-like jumps in the G vs V_{GS} profile starts occurring (at 348 K for ReS_2 and at 373 K for MoS_2), which is attributed to the trapping and de-trapping of e^- from the gate into the oxide and vice versa with enough activation energy (E_A) at higher temperature.[1] At high T, at the beginning of FS ($V_{GS} < 0$), the bands bend as shown by the schematic in Fig. 3(d)–(iii) favoring e^- injection from the gate into the oxide causing gate field screening. The stored e^- give rise to a repulsive field in addition to the gate field as long as $V_{GS} < 0$. For $V_{GS} > 0$, the bands evolve [Fig. 3(d)–(iv)] allowing the trapped oxide e^- to jump back into the gate, resulting in a sudden increase in the attractive field seen by the channel and the first g_m jump is observed, which leads to STATE 1 of the memory operation during FS. For $V_{GS} < 0$ during RS, the ejection of e^- from the oxide into the gate is again favored [Fig. 3(d)–(v)], and we see the second g_m jump, leading to STATE 0 of the memory operation. It is important to note that at lower T, the gate e^- do not have the E_A required to overcome the barrier between the gate and the oxide. Hence, intrinsic trapping is the dominating mechanism responsible for CW hysteresis at lower T.

Figure 4(a) plots ΔV_{th} (left axis) and trap density (ΔN_T, right axis) vs T, extracted from Figs. 1 and 2 for ReS_2 (red line) and MoS_2 (green line), respectively, using the following equation:

$$\Delta N_T = \frac{\Delta V_{th} \times C_{ox}}{q}, \tag{1}$$

where the gate oxide capacitance per unit area is given by $C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{d}$, $\varepsilon_r = 3.9$, and oxide thickness $d = 280$ nm. The fits (dashed lines) to ΔV_{th} and ΔN_T in Fig. 4(a) are used to extract the oxide trap density (ΔN_{OT}) and intrinsic trap density (ΔN_{IT}) components for ReS_2 and MoS_2 in Fig. 4(b). ΔN_{OT} is considered to be negligible at RT and the same for both ReS_2 and MoS_2 at all T since both types of devices are fabricated on identical p^+Si/SiO_2 substrates. The algebraic sum of ΔN_{OT} and ΔN_{IT} results in total ΔN_T. For both materials, hysteresis becomes zero at higher T due to the reducing impact of ΔN_{IT}, but the effect of $\Delta N_{IT,ReS_2}$ dies faster than $\Delta N_{IT,MoS_2}$. This is explained by a schematic shown in Fig. 4(c), depicting the inversion from CW to ACW hysteresis with increasing T due to the dominance of ΔN_{IT} and ΔN_{OT} independently at RT and high T, respectively. The evolution of hysteresis with T due to only ΔN_{OT} is shown by the solid pink line, depicting a negligible hysteresis at lower T, which eventually increases for higher T. However, the solid red and blue lines show the effect of ΔN_{IT} on hysteresis for ReS_2 and MoS_2 with T, respectively. Hence, adding the hysteresis effects from the two kinds of traps gives the net hysteresis change as shown by the dashed lines in Fig. 4(b). Steeper reduction in $\Delta N_{IT,ReS_2}$ with T as compared to $\Delta N_{IT,MoS_2}$ can be observed.

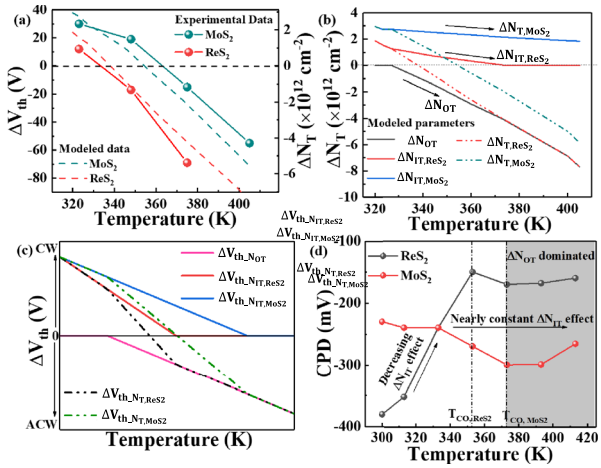

FIG. 4. (a) ΔV_{th} (left axis) and ΔN_T (right axis) vs T extracted from the experimental data (solid line) along with the fitted data (dashed lines) for MoS_2 and ReS_2. (b) Evolution of fitted ΔN_T data (dashed lines) along with ΔN_{OT}, $\Delta N_{IT,ReS_2}$, and $\Delta N_{IT,MoS_2}$ constituents with T. (b) Schematic explaining the evolution of ΔV_{th} due to $\Delta V_{th,N_{OT}}$ and $\Delta V_{th,N_{IT}}$ separately, for ReS_2 and MoS_2, leading to a quicker (lower T) transition from CW to ACW hysteresis for ReS_2. (d) Evolution of average CPD values for ReS_2 and MoS_2 with increasing T.

Finally, T-dependent KPFM measurements were performed to confirm the proposed model. The average contact potential difference (CPD) measured for ReS_2 and MoS_2 is shown in Fig. 4(d). We define CPD by

$$\phi_{sample} = \phi_{tip} - [q \times CPD], \tag{2}$$

where ϕ_{sample} and ϕ_{tip} represent the work function of the sample and the tip, respectively, and q is the electronic charge. The CPD values obtained are consistent with previous reports.[29,30] CPD values for ReS_2 increase with increasing T, whereas they remain almost unchanged for MoS_2. The temperatures for crossover from CW to ACW hysteresis are marked as T_{CO,ReS_2} and T_{CO,MoS_2}. The material with a more negative CPD value implies a larger work function and more e^- depletion [Eq. (2)]. According to previous reports, gas adsorbates that act as e^- acceptors are responsible for e^- depletion, leading to more negative CPD.[30–32] However, all the measurements in this work are carried out in a controlled nitrogen ambient, ruling out the presence of adsorbates as a possible cause for e^- depletion. Therefore, we infer intrinsic trapping as the likely reason for e^- depletion, resulting in more negative CPD values at RT for ReS_2. Moreover, intrinsic trapping can only be observed in devices with fully depleted channels;[2,26] hence, at higher T, the effect of intrinsic traps is nullified and oxide trapping dominates. As shown in Fig. 4(d), T_{CO,ReS_2} is less than T_{CO,MoS_2}, implying that the effect of intrinsic traps persists for much higher T in MoS_2 than for ReS_2 consistent with the proposed model. The CPD maps for ReS_2 are shown in Fig. 5(a) at 323 K and Fig. 5(b) at 373 K and for MoS_2 in Fig. 5(c) at 323 K and Fig. 5(d) at 373 K. The contrast for all the images is adjusted on the same scale, clearly showing the most negative CPD for ReS_2 at RT in Fig. 5(a).

To conclude, in this report, we demonstrate thermally assisted memory using back-gated vdP FETs with few-layer ReS_2 and MoS_2 as the channel materials. The transfer characteristics show a change in the hysteresis direction from CW to ACW with increasing T, along with step-like jumps in the transfer curves at higher T (STC crossover hysteresis). Memory parameters such as RST-to-WR and RD windows are compared for memory operation. The step-like jumps in the transfer curve occur at much lower T for ReS_2 (373 K) as compared to MoS_2 (400 K), making it a better choice for memory applications. These results are ascribed to a combined effect of intrinsic traps at lower T and screening of gate voltage due to electron injection from the gate into oxide trapping sites at higher T. This physical model is corroborated through T-dependent KPFM measurements that show an increase in CPD for ReS_2, while an almost constant CPD for MoS_2 with increasing T. This implies enhanced depletion of electrons in ReS_2 with increasing T, reinforcing the model of faster de-trapping of intrinsic ReS_2 traps with T and hence a lower crossover T.

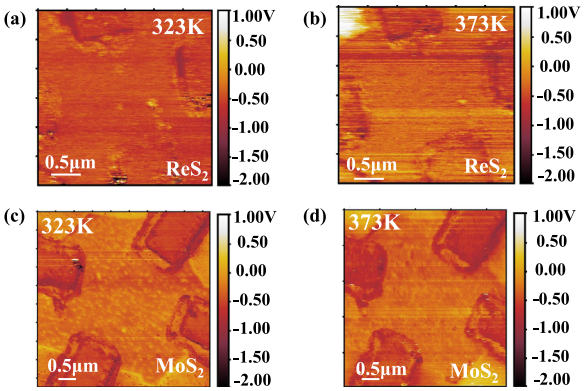

FIG. 5. CPD maps for ReS_2 at (a) 323 K and (b) 373 K and for MoS_2 at (c) 323 K and (d) 373 K. The contrast for all the CPDs is adjusted on the same scale.

See the supplementary material for the transconductance (g_m) vs gate voltage (V_{GS}) plots at varying temperatures for ReS_2 and MoS_2 showing jumps during forward sweep and reverse sweep at high temperatures.

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