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M-PSK Demodulator with Joint Carrier and Timing Recovery

Daniele Giardino, Gian Carlo Cardarilli, *Member, IEEE*, Luca Di Nunzio, Rocco Fazzolari, Alberto Nannarelli, *Senior Member, IEEE* Marco Re, *Member, IEEE* and Sergio Spanò

***Abstract*—In this work, we propose a new digital receiver for Phase-Shift Keying (PSK) modulation based on the integration of the conventional digital Costas Loop circuit with a new timing recovery method. The timing recovery is applied to the PSK demodulator using an Iterative Learning Control (ILC) law and it is based on the minimization of the intersymbol interference using only one sample per symbol. The main advantage of the proposed timing recovery method is the insensitivity to frequency offsets which results in improved performance and robustness of the Costas Loop circuit. Experiments comparing a conventional receiver (cascade of Costas Loop and Early-Late Timing Synchronizer) to the proposed receiver in scenarios characterized by low signal-to-noise ratios and large frequency and phase errors, show that the time needed to reduce the errors of the proposed receiver is seven times smaller than the conventional receiver. Moreover, the impact of the proposed method on the necessary hardware resources (area and power consumption) is negligible.**

***Index Terms*—Carrier recovery, Costas Loop, Digital receiver, Hardware implementation, PSK demodulator, Timing recovery.**

I. Introduction

The performance of a digital communication system is very dependent on carrier and symbol recovery, which are usually performed by the cascade of a carrier recovery subsystem and a symbol recovery block [1], [2]. In M-ary Phase Shift Keying (M-PSK) suppressed carrier modulation schemes, these operations are usually performed using closed-loop systems such as the Costas Loop for the carrier recovery [3]–[5], and the Early-Late or the Mueller and Müller or the Gardner timing synchronizers for the symbol recovery [6]–[8]. The key parameters are the recovery time, also known as lock-in time, and the capability to operate in noisy environments.

In closed-loop systems lock-in time and noise robustness are correlated and their values depend on the bandwidth of the loop filter [4]. Wide-band loop filters are faster in terms of lock-in time, but they are more sensitive to noise. In contrast, narrow-band loop filters are more robust to noise but slower to lock-in [2]. Therefore, synchonizers operating in noisy environment usually implement a narrow-band loop filter.

In space missions, the trade-off between lock-in time and noise robustness is a major issue because the signals are often affected by a low Signal-to-Noise Ratio (SNR) and a large Doppler effect. Specifically, the low SNR requires a narrow-band loop filter, while the large frequency error, associated with the Doppler effect, requires a wide-band loop filter. To address this trade-off, a possible solution is to design systems able to reduce the noise transmitted in the feedback path of the carrier recovery.

This work proposes a new digital receiver for M-PSK modulations suitable for applications with reduced SNR and large Doppler effect.

The starting point is the merge of the digital version of the conventional Costas Loop circuit [4], [9] with a new timing recovery algorithm that works in presence of frequency and phase errors in the receiver. The proposed receiver is designed to reduce the self-noise contribution of the Costas Loop, due to the Intersymbol Interference (ISI) [9]–[11], in parallel to the frequency and phase errors compensation.

In a conventional receiver, the ISI is reduced by a timing recovery algorithm after the Costas Loop, and a timing recovery algorithm requires at least two samples per symbol. As opposed to the conventional receiver, the new timing recovery reduces the ISI in parallel to the Costas Loop by using one sample per symbol, and the self-noise is reduced as well.

As a result, the Costas Loop performance is improved because the self-noise and the lock-in time are reduced, which leads to an increase in both the noise robustness and the capabilities to compensate for the frequency and phase errors due to the Doppler effect.

The main contribution of this paper is a novel method to improve the performance of M-PSK demodulators by a joint carrier and timing recovery algorithms. The method was validated by extensive simulations to determine the improvements over the conventional receiver, composed of a Costas Loop and an Early-Late Timing Synchronizer (ELTS), in terms of lock-in time and noise robustness. Moreover, the results of synthesis in standard cells technology of the proposed receiver show that the additional costs in area and power dissipation, with respect to the conventional receiver, are marginal.

The paper is organized as follows. Section II gives an overview of a conventional digital demodulator. Section III describes the proposed architecture and the proposed timing recovery method. Section IV shows the simulation results and the hardware implementation of a conventional receiver and the proposed receiver. Section V draws the final conclusions.

II. Digital Receiver

Fig. 1 shows a typical receiver for M-PSK suppressed carrier signals realized by using a Costas Loop, for the carrier recovery, connected in cascade with a Early-Late Timing synchronizer (ELTS), for the timing recovery.

D. Giardino, G.C. Cardarilli, L. Di Nunzio, R. Fazzolari, M. Re and S. Spanò are with the DEE, Univ. of Rome "Tor Vergata", Italy.

A. Nannarelli is with the Department of Applied Mathematics and Computer Science, Technical University of Denmark, Denmark.

Contact: giardino@ing.uniroma2.it

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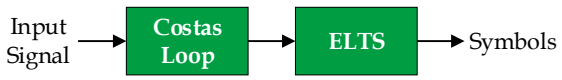

Fig. 1. Conventional digital receiver.

The receiver's functions are: a) phase compensation and frequency shift from the carrier frequency to the baseband by using the carrier recovery block, and b) symbol timing estimation by using the timing recovery block.

Generally, for the M-PSK modulation, the carrier recovery is implemented by using the Costas Loop, a Phase-Locked Loop (PLL) based circuit able to demodulate the received signal and to compensate for the frequency and phase offsets [3]. The architecture of the digital Costas Loop is shown in Fig. 2.

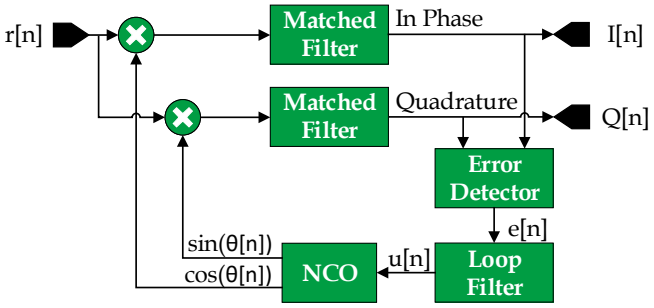

Fig. 2. Digital Costas Loop.

The Costas Loop is composed of two multipliers for the down-conversion of the received signal $\mathrm{r[n]}$, two digital filters (Matched Filters) for the suppression of unwanted frequencies generated by the multipliers that recover the In-phase (I) and the Quadrature (Q) components, a phase Error Detector to generate an error signal based on the known constellation, a Loop Filter to filter the error, and a digital oscillator, e.g., a Numerical Controlled Oscillator (NCO), for the generation of the sine and cosine waveforms.

The design parameters of a Costas Loop are optimized considering both the communication environment and the trade-off between performance and noise robustness. For example, ISI can be reduced by modeling the matched filter with a square-root raised-cosine filter [12], but it is not able to completely eliminate the self-noise introduced by the ISI.

In the Costas Loop, and more in general in the carrier recovery subsystem, the loop filter is the most critical block for the receiver performance as it defines both the lock-in range $\Delta\omega_{\mathrm{L}}$, associated with the maximum frequency and the phase errors that can be corrected, and the lock-in time $\mathrm{T_L}$, that characterizes the duration of the acquisition process [4].

The lock-in range $\Delta\omega_{\mathrm{L}}$ depends on the modulation scheme. For Binary Phase Shift Keying (BPSK) modulation, $\Delta\omega_L = \zeta\omega_n$, while $T_L \approx 2\pi/\omega_n$, where ω_{n} is the natural frequency and ζ is the damping factor of the system. For Quadrature Phase Shift Keying (QPSK) modulation we get $\Delta\omega_L = \sqrt{2}\zeta\omega_n$.

The Costas Loop circuit, described in detail in [4], [9], presents a main drawback: the error is computed in a continuous way, and consequently, also during the symbol transition phase. This increases the self-noise of the error detector degrading the performance of the carrier recovery. Similar considerations can be done for the timing recovery block about the error timing estimation. The error, that for the ELTS is based on the value of the derivative computed in the sampling point, is filtered by a loop-filter connected to a timing generator that adjusts the sampling point. Consequently, the loop-filters need to be configured with the appropriate parameters in order to improve the noise robustness taking account the lock speed.

III. Proposed Architecture

Our proposed solution aims at improving the performance and the robustness of the Costas Loop by reducing the self-noise.

The error detector in Fig. 2 compares the output complex signal of the matched filters $\mathrm{y[n] = I[n] + jQ[n]}$ with the symbols of the constellation, that it is known a priori. The signal $\mathrm{y[n]}$ represents each symbol with N samples affected by the ISI, since the system operates at a sampling frequency N times the symbol rate. Therefore, the known symbol constellation is compared to a not optimal signal by introducing the self-noise due to the presence of the ISI. Consequently, we can represent the signal $\mathrm{y[n]}$ at the input of the error detector as:

$$y[n] = x[n] + N_{AWGN}[n] + N_{ISI}[n] \tag{1}$$

where $\mathrm{x[n]}$ is the desired symbol, $\mathrm{N_{AWGN}[n]}$ is the Additive White Gaussian Noise (AWGN) introduced by the transmission channel, and $\mathrm{N_{ISI}[n]}$ is the ISI noise contribution. The error estimated for each sample of the symbol, also during the transition from a symbol to the next one, produces the additional noise $\mathrm{N_{ISI}[n]}$ called self-noise [9]–[11]. The loop filter in Fig. 2, positioned after the error detector, can mitigate only the effect of $\mathrm{N_{AWGN}[n]}$. Consequently, the term $\mathrm{N_{ISI}[n]}$ can be mitigated only by sampling $\mathrm{y[n]}$ in the optimal time instant of the period symbol [2].

To overcome these limitations, we propose a new receiver that combines the Costas Loop with a new timing recovery method, suitable for all the M-PSK modulations.

The proposed receiver is shown in Fig. 3. The input of the error detector receives the optimal sampled signal from the digital Sample and Hold (S/H), implemented by a register enabled by the new timing recovery block.

The timing recovery block has been specifically designed for this new configuration. In fact, traditional timing recovery algorithms, such as the Early-Late, the Mueller and Müller or the Gardner, cannot be used in the proposed configuration because they are not efficient for large frequency offsets [13].

In our approach, we consider for the input signal $\mathrm{r[n]}$ a sampling rate N times the symbol rate (N integer). In this way, each symbol is represented with N samples. With this assumption, the proposed timing recovery block generates the timing to drive the S/H blocks that will select only the optimal sample for each symbol. This approach allows to minimize $\mathrm{N_{ISI}[n]}$ and, as consequence, the self-noise. The following analysis is also valid for timing recovery blocks

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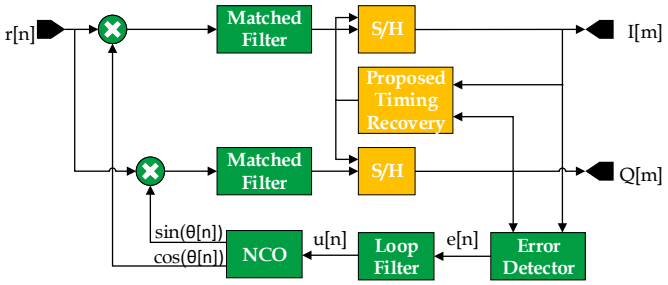

Fig. 3. Merge of the Costas Loop with the proposed timing recovery.

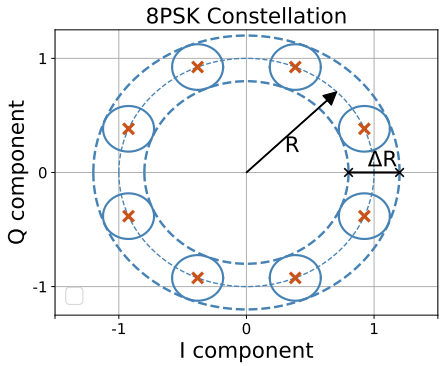

Fig. 5. 8-PSK Constellation. R is the radius of the transmitted 8-PSK constellation and ΔR is the range of the radius of the received points.

that use interpolator filters to increase the time resolution [2]. As a result, the loop filter exhibits better performance and robustness.

A. Proposed Timing Recovery

The new timing recovery algorithm is shown in Fig. 4. It can be used for any M-PSK modulation. The purpose of the timing recovery is to generate a pulsed signal to control the sampling time. The sampling signal is a periodic discrete impulse sequence generated by an impulse generator. Its phase is modified by changing the control signal u[m] (phase signal) to find the optimal sampling point that minimizes the ISI. The signal u[m] is obtained by using a statistical approach and the Iterative Learning Control (ILC). As shown in [14] and [15], the ILC is able to improve the tracking and response performances of a dynamic system, and it can be combined in a feedback system without introducing instability.

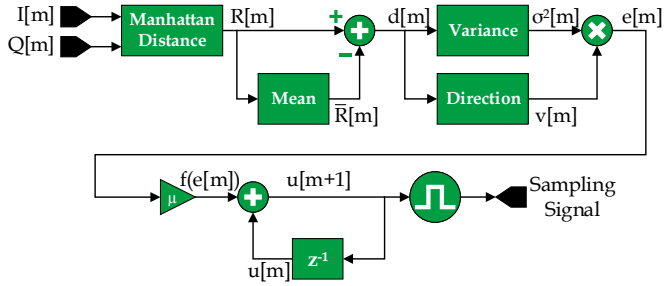

Fig. 4. Proposed Timing Recovery.

As explained in [16], a typical ILC control law is:

$$u[m+1] = u[m] + f(e[m]) \tag{2}$$

where f(e[m]) is a function that depends on the error (the timing error in this case). Fig. 5 shows the transmitted constellation (red crosses) and the set of points received for an 8-PSK modulation. The points received form a cloud around the constellation points. If the phase and frequency are recovered, these clouds have a circular shape.

The extension of the cloud depends on the SNR of the received signal and the sampling accuracy of the symbols. If the sample is taken in the optimal position (usually in the center of the symbol), the ISI is minimized and the points of the cloud have a distance from the origin very close to that of the transmitted constellation point (represented by the central circumference in Fig. 5). In general, the symbol synchronization errors transform the constellation point into a cloud. These regions can be considered within an area limited by the two dotted circles of Fig. 5. The proposed timing recovery is designed to minimize ΔR (variation of the received point radius). In our architecture, we use the variance σ^2_{R} as a measure of ΔR, and finally, to the synchronization error.

We define $d[m] = R[m] - \bar{R}[m]$ where $\bar{\mathrm{R}}[\mathrm{m}]$ is the mean of R[m]. To obtain an error e[m] useful in the ILC control law, we must define a signed error and therefore the use of the variance alone is not enough. For this reason, we introduce a direction signal $v[m] = sign(d[m] - d[m-1])$ to detect statistically if the radius of the received point is increasing or decreasing. The final expression of the error is $\mathrm{e}[\mathrm{m}] = v[m] \times \sigma^2_{\mathrm{R}}[\mathrm{m}]$. Accordingly, the control law becomes:

$$u[m+1] = u[m] + \mu\, \sigma^2_R[m]\, v[m] \tag{3}$$

where μ is the convergence rate parameter [14]. The signal u[m] will converge at a value which minimizes f(e[m]). Note that the timing recovery works at a lower sample rate with respect to the input signal r[n] requiring only one sample per symbol. On the contrary, the discrete impulse generator works with the same rate of the input signal r[n] to adjust the sampling time with the same time resolution of the input signal. We can also increase the resolution through interpolation.

Unlike the other timing recovery methods, the proposed method is insensitive to the frequency offset because it uses the constellation radius for the timing error estimation. Consequently, the timing recovery can start when the carrier is not yet recovered by significantly reducing the lock-in time.

B. Hardware Design Optimizations

To reduce the complexity of the architecture shown in Fig. 4, we introduce some hardware optimizations allowing an efficient implementation of the radius and the variance computations. The radius is computed by using the Euclidean distance $R = \sqrt{I^2 + Q^2}$ that is quite complex requiring two multiplications and a square-root [17]. However, by approximating the Euclidean distance with the Manhattan distance

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$R = |I| + |Q|$, we avoid multiplications and square-root and still get an acceptable estimate of the radius.

Next, we optimize the variance $\sigma^2_{\mathrm{R}}[\mathrm{m}]$ and the mean value $\bar{\mathrm{R}}[\mathrm{m}]$ computations. These two signals are computed with a moving average filter of length N:

$$\bar{R}[m] = \frac{R[m]}{N} + \cdots + \frac{R[m-(N-1)]}{N} = \sum_{i=0}^{N-1} \frac{R[m-i]}{N} \quad (4)$$

$$\sigma^2_R[m] = \frac{d^2[m]}{N} + \cdots + \frac{d^2[m-(N-1)]}{N} = \sum_{i=0}^{N-1} \frac{d^2[m-i]}{N} \quad (5)$$

The computation of $\sigma^2_R[m]$ and $\bar{R}[m]$ requires $\mathrm{N}-1$ adders, for a total of $2(\mathrm{N}-1)$ adders. To reduce the number of adders, we can rearrange the previous equations, obtaining a circuit that uses only two adders for each signal, regardless of N.

The mean value $\bar{\mathrm{R}}[\mathrm{m}]$ (the same method can be applied for $\sigma^2_{\mathrm{R}}[\mathrm{m}]$) can be expressed as:

$$\begin{aligned} \bar{R}[m] &= \sum_{i=0}^{N-1} \frac{R[m-i]}{N} = \frac{R[m]}{N} + \sum_{i=1}^{N-1} \frac{R[m-i]}{N} \\ &= \frac{R[m]}{N} + \sum_{i=1}^{N} \frac{R[m-i]}{N} - \frac{R[m-N]}{N} \\ &= \frac{R[m]}{N} + \bar{R}[m-1] - \frac{R[m-N]}{N} \end{aligned} \quad (6)$$

Thanks to this simplification, only two adders for $\bar{\mathrm{R}}[\mathrm{m}]$ and for $\sigma^2_{\mathrm{R}}[\mathrm{m}]$ are needed, for a total of four adders. By choosing N as a power of two, the division is reduced to a bit-shift.

IV. Experimental Results

The performance of the proposed receiver is analyzed by Fixed-Point (FXP) simulations. The purpose of the analysis is to compare the conventional receiver shown in Fig. 1, composed of a Costas Loop and an ELTS, with the proposed receiver of Fig. 3.

A FXP simulation is performed by using Simulink and considering a noisy channel. By the simulation we highlight the Costas Loop improvements obtained by our method, and compare the performance of the proposed timing recovery to that of the ELTS.

The Simulink results are also used to validate the Synopsys' Verilog post-synthesis simulation.

A. FXP Simulation Results

The experimental setup shown in Fig. 6 is repeated for three transmission chains implementing BPSK, QPSK, and 8-PSK modulation schemes. For brevity, we only show the 8-PSK modulation case because, when the SNR is low, the 8-PSK is more sensitive to noise than the BPSK and QPSK modulations.

In Fig. 6, both receivers (RX) are connected to the same input: the cascade of the transmitter (TX), containing the modulator, and the AWGN channel, used to emulate the noise and to introduce the frequency and phase offsets. The comparison is done at a fixed low SNR for both the receivers. The Costas Loop of both receivers is designed to have the same

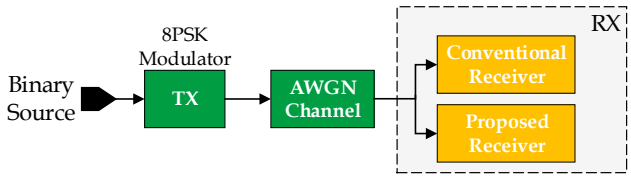

Fig. 6. Experimental setup for 8-PSK modulation.

performance in terms of lock-in time and noise robustness and, consequently, the same parameters for the matched filters, the error detector, the loop filter, and the NCO.

For the simulation, the clock frequency $\mathrm{F_{clk}}$ is set at 1 MHz and the results can be scaled for different clock frequency values. The carrier frequency of the input signal is $\frac{\mathrm{F_{clk}}}{4} + \Delta\mathrm{f}$, where $\Delta\mathrm{f} = 250$ Hz is the frequency offset. The bandwidth of the input signal is $\frac{\mathrm{F_{clk}}}{16} = 62.5$ kHz and, consequently, the symbol is represented by 16 samples. The parameters of the loop filters are chosen to have a lock-in range $\Delta\omega_{\mathrm{L}} = 2\pi\mathrm{f_L} = 3142$ rad/s, where $\mathrm{f_L} = 500$ Hz to ensure a large noise robustness involving a large lock-in time. The sine and cosine waves are generated by a NCO with 20 bits for the accumulator and 10 bits for the phase-amplitude converter [18].

The channel noise is represented by the Energy per Bit to Noise power spectral density ratio $\frac{\mathrm{E_b}}{\mathrm{N_0}} = 15$ dB that is an alternative representation of the SNR.

The carrier recovery time is measured by analyzing the time response of the loop filters of both receivers, which are used to correct the phase of the NCO.

The simulation results shown in Fig. 7 prove that the proposed receiver exhibits a lower lock-in time $\mathrm{T_{L1}}$, with respect to the lock-in time of the conventional receiver $\mathrm{T_{L2}}$. Fig. 7(a) shows the instants $\mathrm{T_{L1}}$ and $\mathrm{T_{L2}}$ in which the carrier is compensated. The lock-in time $\mathrm{T_{L1}}$ is seven times smaller than $\mathrm{T_{L2}}$. Moreover, the loop filter dynamic range, amplitude in Fig. 7(a), is reduced due to the self-noise reduction introduced by our approach.

Fig. 7(b) shows the performances of the symbol estimation in terms of the Modulation Error Ratio (MER), defined as in [19]. For the proposed receiver, the MER grows at $\mathrm{T_{L1}}$ because the carrier has been compensated before the conventional receiver. After $\mathrm{T_{L2}}$, the MER performances are approximately equal.

B. Implementation Results

The conventional and proposed receivers have been coded in VHDL, at RTL level, and synthesized by the Synopsys synthesizer using the STM 90 nm standard cell library.

In telecommunication applications where the PSK modulation is used, the signal bandwidth is usually in the range 0.2 to 8 MHz [20], and the clock period is chosen according to the symbol rate. For this reason, we set a clock constraint of 100 MHz for the synthesis, and, considering 16 samples per symbol, as in the simulation, the bandwidth of the signal is 6.25 MHz. Synthesis results are shown in Table I.

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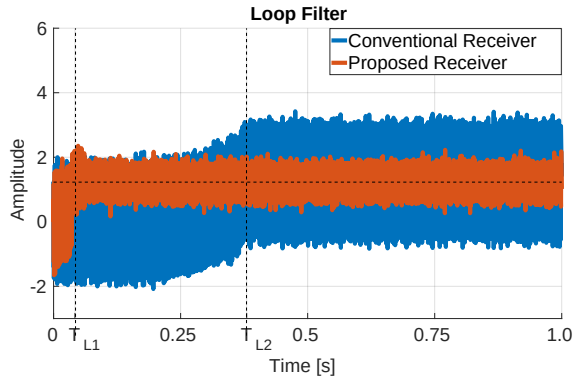
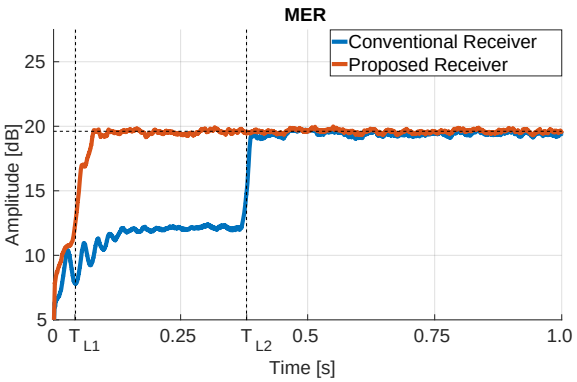


(a) Loop filter Outputs



(b) MER Comparison

Fig. 7. Loop filters (top) and MER (bottom) comparisons between the conventional receiver and the . Parameters of the simulation: 8-PSK signal, $E_b/N_0 = 15$ dB, clock frequency of 1 MHz, lock-in range $\Delta\omega_L = 3142$ rad/s and frequency offset $\Delta f = 250$ Hz. T_{L1} and T_{L2} are the lock-in times of the proposed and the conventional receivers, respectively.

TABLE I
AREA AND POWER CONSUMPTION.

	Area [μm^2]	**NAND Equivalent Gates**	**StaticPower** [μW]	**DynamicPower** [mW]
Conventional	379350	86400	47.14	10.30
Proposed	385600 (+1.65%)	87800 (+1.65%)	47.80 (+1.40%)	10.53 (+2.23%)

For the conventional receiver, the Costas Loop part has an area of 92% of the total due to the large matched filters. The Costas Loop part is the same for both receivers and its area is predominant with respect to the timing synchronizers in both receivers. The synthesis results in Table I indicate that the proposed receiver has a similar area and power consumption, but performs better than the conventional receiver as shown by the simulation results in Section IV-A.

V. CONCLUSIONS

In this paper, a new timing recovery method and a new all-digital receiver for M-PSK modulations is proposed. Unlike other methods such as the ELTS, the proposed method does not require knowledge of the specific modulation and can handle a wide range of frequency and phase offsets. In addition, it works using only one sample per symbol and improves the behavior of the Costas Loop in the suppressed carrier recovery. By performing simulation experiments, we were able to compare the behavior of the conventional and the proposed receivers in presence of frequency and phase offsets and noise. The experiment results proved that the proposed receiver performs better than the Costas Loop in terms of performance and robustness, minimizing the ISI and the self-noise. Moreover, the hardware implementation of the proposed receiver results in similar area and power consumption with respect to the conventional receiver.

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