Fast Estimation of Phase Angle for Three-Phase Voltage Systems under Distorted Conditions

Reza, Md Shamim; Hossain, Md Maruf; Nasif, Ahmed O.; Agelidis, Vassilios G.

Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

Link to article, DOI:
10.1109/JESTPE.2020.3044058

Publication date:
2021

Document Version
Peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

Fast Estimation of Phase Angle for Three-Phase Voltage Systems under Distorted Conditions

Md. Shamim Reza, Md. Maruf Hossain, *Member*, *IEEE*, Ahmed O. Nasif, *Member*, *IEEE*, and Vassilios G. Agelidis, *Fellow*, *IEEE*

***Abstract*-This paper proposes a fast and robust technique for instantaneous phase angle estimation of three-phase voltage systems under unbalanced and distorted conditions. It mainly relies on the Clarke transformation, Teager energy operator and delayed signal cancellation (DSC) approach. Unlike an adaptive DSC-based synchronous-reference frame phase-locked loop (PLL), the proposed technique avoids interdependent loops, thus increasing the overall stability and easing the tuning process. Moreover, it removes the phase loop of the PLL, hence eliminates the requirement of in-loop filter (low-pass filter) and/or loop filter (proportional plus integral controller). As a result, the tuning of these filters is not required and a quicker response is produced. The proposed technique also avoids inverse trigonometric function operation. In addition, it shows harmonics immunity at steady-state and can generate fast dynamic response with a settling time less than one nominal fundamental cycle. Both simulation and experimental results are presented to reveal the benefits of the technique.**

***Index Terms*: Clarke transformation, delayed signal cancellation, phase angle estimation, and three-phase system.**

I. Introduction

A fast and accurate estimation technique for instantaneous phase angle of three-phase voltage systems plays an important role for efficient operation of grid-connected power converters [1-3]. A phase-locked loop (PLL) is the commonly applied technique for phase estimation [4]. Three-phase PLL-based on synchronous-reference frame (SRF) is the simplest one and can provide accurate estimation at high speed under balanced and undistorted conditions. However, it requires in-loop filter or pre-filter as it suffers by harmonics and imbalances [5-9]. The inclusion of additional filter may require optimum tuning and may also introduce interdependent loops.

A moving average (MA) based in-loop filter may slow down dynamic response of the PLL significantly [5]. In this case, a proportional–integral–derivative (PID) controller is suggested as a loop filter to improve the dynamic performance while maintaining a good filtering capability [5, 6]. The MA filter can be replaced by one or more notch filters [7]. On the other hand, a variable sampling frequency based approach may not be suitable for real-time application due to the requirement of changing parameters of other algorithms implemented in the same digital signal processing board [6]. Multiple SRF filtering based PLL structure can reject adverse effects caused by harmonics and negative-sequence (NS) components, but it increases computational effort considerably [10]. Complex coefficient filters (CCFs) can also be used in the pre-filtering stage [8]. In this structure, the CCFs are cross-connected where each of them is responsible for tracking a particular frequency component. An enhanced PLL generates slower response under grid disturbances [9]. Additional second-order generalized integrator (SOGI) based quadrature signal generator (QSG) tuned at harmonic frequencies may be combined with the QSG-SOGI based PLL (SOGI-PLL) to improve the lower-order harmonic filtering capability [11, 12]. Moreover, mixed second- and third-order generalized integrator based PLL (MSTOGI-PLL) can be used to enhance the estimation accuracy under DC offset condition [13].

A delayed signal cancellation (DSC) approach can be used as an in-loop or pre-filter of the SRF-PLL for extracting the phase angle of the fundamental frequency positive-sequence (FFPS) component [14-18]. The in-loop filter based on a cascaded DSC (CDSC) operator increases delay in the control loop of the PLL and slows down the dynamic response [16]. On the other hand, the frequency estimated by the SRF-PLL is fed back to adjust the pre-filter based on CDSC operator to the frequency variations [15]. In this case, the system becomes highly nonlinear due to the presence of interdependent loops [17].

The technical literature shows that the presence of interdependent loops between the phase and frequency estimation reduces the stability margin of the PLL due to the influence of one loop by other one at the same time. In this case, the tuning of proportional plus integral (PI) controller (loop filter) is also more sensitive. In addition, a time delay is generated by the loop filter and hence a slower response is produced. A better stability and an easier tuning process can be achieved by using a separate frequency estimator for the adaptive pre-filter where the interdependent loops between the phase and frequency estimation are avoided. The time delay associated with the PI controller and/or in-loop filter can also be avoided if, instead of the PLL, a separate phase estimation algorithm is used.

The objective of this paper is to propose a relatively fast and robust technique for instantaneous phase angle estimation of three-phase voltage systems. It relies on a Teager energy operator (TEO) based frequency detection algorithm and a CDSC operator based phase estimation approach. Unlike the CDSC based SRF-PLLs, the proposed TEO-CDSC technique avoids interdependent loops between the frequency and phase estimation, thus increasing the overall stability and easing the tuning process. Moreover, it does not need the phase loop of the PLL, thus eliminates the requirement of in-loop low-pass filter (LPF) and/or loop filter (PI/PID controller). As a result,

M. S. Reza is with the Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka, Bangladesh (email: shamim_reza@eee.buet.ac.bd).

M. M. Hossain and A. O. Nasif are with the Department of Electrical Engineering Technology, University of Wisconsin, USA (email: hossainm@uwgb.edu & nasif@uwosh.edu).

V. G. Agelidis is with the Department of Electrical Engineering, Technical University of Denmark, Lyngby, Copenhagen, Denmark (vasagel@elektro.dtu.dk).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

the tuning of these filters is not required and a faster response is produced. It also avoids inverse trigonometric function operations. In addition, it shows harmonics immunity at steady-state and can generate fast dynamic response with a settling time less than one nominal fundamental cycle.

The remaining parts of the paper are organized as follows. Section II contains an overview of the SRF-PLLs based on the CDSC operator. The proposed TEO-CDSC technique is documented in section III. Simulated performance comparison of the proposed technique with the CDSC-PLL [15] and *dq*CDSC-PLL [16] are presented in section IV. Section V contains the real-time experimental results. Section VI includes the conclusions of the proposed work.

II. Overview of CDSC Based PLLs

The voltage signals of three-phase systems can be unbalanced due to the grid faults or sudden connection/disconnection of heavy loads to/from the grid. The unbalanced voltage signals can be expressed by

$$\left.\begin{aligned} v_a(n) &= A_a \sin[\phi(n)] \\ v_b(n) &= A_b \sin[\phi(n) - 2\pi/3] \\ v_c(n) &= A_c \sin[\phi(n) + 2\pi/3] \end{aligned}\right\} \quad (1)$$

Symbols used in (1) are defined as follows. n: sampling index, A_a, A_b and A_c: fundamental amplitudes of phases 'a', 'b' and 'c' respectively, $\phi(n)=\omega n T_s+\theta$: instantaneous phase angle of phase 'a', θ: initial phase angle of phase 'a', T_s: sampling time interval, $\omega=2\pi f$: fundamental angular frequency, and f: fundamental frequency. The unbalanced voltage signals can also be distorted by harmonics due to the non-sinusoidal current drawn by the nonlinear loads connected to the grid. The SRF-PLL is the commonly applied technique for the extraction of phase angle of the FFPS component. However, to obtain an accurate estimation, a pre-filter or in-loop filter is combined with the SRF-PLL under distorted and unbalanced conditions. The following subsections present an overview of the SRF-PLLs based on the pre-filter or in-loop filter relying on the CDSC operator.

A. Three-Phase SRF-PLL Based on CDSC Pre-Filter

Fig. 1 shows the block diagram representation of the three-phase SRF-PLL based on the CDSC pre-filter. In this method, the Clarke transformation generates v_α and v_β signals in α-β stationary reference frame from the three-phase grid voltages (v_a, v_b, and v_c). The generated voltages contain FFPS (v_α^+ and v_β^+), fundamental frequency NS (FFNS), harmonic frequencies PS and NS components under unbalanced and harmonic conditions. A frequency adaptive band-pass filter (BPF) is then used as the pre-filter to extract only the FFPS component. The DSC operator has excellent filtering characteristics and is recently used as the pre-filter for improving the disturbance rejection ability of the SRF-PLL [15, 16, 19, 20]. Several configurations of the CDSC operator can be used under several conditions of the input voltages. The use of a number of DSC operators in the CDSC chain depends on the expected harmonic components [15, 16, 19, 20]. The SRF-PLL relying on the Park transformation, PI controller (loop filter) and integrator is then employed to track the instantaneous phase angle (ϕ^+) of the FFPS component. The CDSC pre-filter based SRF-PLL has two shortcomings. The first one is that the frequency adaptive nature of the CDSC has introduced interdependent loops between the phase and frequency estimation. The frequency

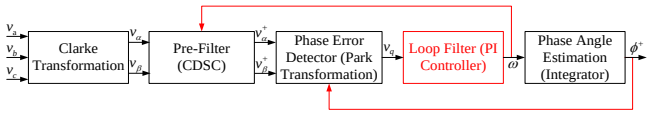


Fig. 1: CDSC pre-filter based three-phase SRF-PLL.

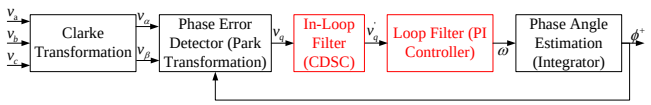


Fig. 2: CDSC in-loop filter based three-phase SRF-PLL.

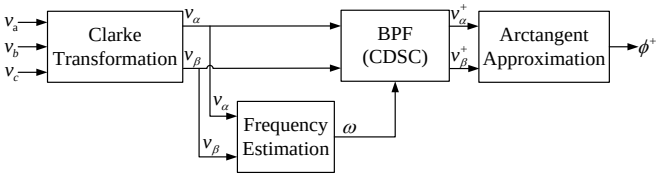


Fig. 3: Proposed grid synchronization technique without using interdependent loops, in-loop and loop filter.

estimated by the SRF-PLL is fed back to adjust the CDSC operator to the frequency variations [15, 19, 20]. In this case, the system becomes highly nonlinear due to the presence of interdependent loops [17]. The interdependent loops reduce the stability margin of the PLL due to the influence of one loop by other one at the same time. In this case, the tuning of the PI controller (loop filter) is also more sensitive. The second one is that a time delay is generated by the loop filter and hence a slower response may be produced.

B. Three-Phase SRF-PLL Based on CDSC In-Loop Filter

The in-loop filter based SRF-PLL is employed to avoid the interdependent loops so that a better stability margin and improved tuning process are obtained. Fig. 2 shows a block diagram representation of the in-loop filter based SRF-PLL. In this method, a fixed tuned in-loop filter is placed just before the loop filter of the PLL. The in-loop filter behaves like a LPF for rejecting all the unwanted high frequency oscillations from the generated q component of the Park transformation. The CDSC structure is also reported as the in-loop filter of the SRF-PLL [16]. However, the CDSC based in-loop filter is tuned at a constant frequency and hence the disturbance rejection capability may degrade under variable frequency environment. Moreover, the in-loop CDSC operator increases delay in the control loop of the PLL and causes sluggish dynamic response [16]. In addition, the PLL structure includes loop filter (PI/PID controller) which creates more dynamic delay.

III. Proposed CDSC Based Phase Estimation Technique

Fig. 3 shows the block diagram representation of the proposed technique for tracking the instantaneous phase angle of the FFPS component. As it can be seen, the proposed technique avoids the interdependent loops between phase and frequency estimation and hence a better stability and relatively easier tuning process can be achieved. The proposed technique also removes the in-loop and loop filters, which help generating faster dynamic response when compared to the SRF-PLL structures shown in Figs. 1 and 2. In the proposed technique, the orthogonal voltage signals of the FFPS component are extracted by using the frequency adaptive CDSC based BPF which is similar to the pre-filter of the SRF-PLL shown in Fig. 1. However, the fundamental frequency for adjusting the window size of the CDSC is tracked by using an auxiliary algorithm. The voltage signals generated by the Clarke transformation are also used as the inputs of the auxiliary algorithm for frequency estimation.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

When compared to the techniques shown in Figs. 1 and 2, the proposed one replaces PLL by an arctangent approximation function, hence it does not require in-loop and loop filter for calculating the phase angle of the FFPS component. The extracted orthogonal voltages, without passing through any other filters, are directly used to calculate the phase angle and hence faster phase estimation can be achieved. The detail functions of each block shown in the proposed technique (Fig. 3) are documented in the following subsections.

A. Clarke Transformation

The voltage signals v_α and v_β in α-β stationary reference frame can be generated from the three-phase grid voltages by using the Clarke transformation shown bellow [21].

$$\begin{bmatrix} v_\alpha(n) \\ v_\beta(n) \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & -1/\sqrt{3} & 1/\sqrt{3} \end{bmatrix} \begin{bmatrix} v_a(n) \\ v_b(n) \\ v_c(n) \end{bmatrix} = \begin{bmatrix} v_\alpha^+(n)+v_\alpha^-(n) \\ v_\beta^+(n)+v_\beta^-(n) \end{bmatrix} \quad (2)$$

where

$$\begin{bmatrix} v_\alpha^+(n) \\ v_\beta^+(n) \end{bmatrix} = \begin{bmatrix} A^+\sin(\omega n T_s+\theta^+) \\ A^+\cos(\omega n T_s+\theta^+) \end{bmatrix}$$

$$\begin{bmatrix} v_\alpha^-(n) \\ v_\beta^-(n) \end{bmatrix} = \begin{bmatrix} A^-\sin(-\omega n T_s-\theta^-) \\ A^-\cos(-\omega n T_s-\theta^-) \end{bmatrix}$$

where (A^+, A^-) and (θ^+, θ^-) are the amplitude and initial phase angle of the FFPS and FFNS components, respectively. All elements of the second row in the Clarke transformation matrix are multiplied by -1 to produce a positive cosine signal for v_β. The voltage signals v_α and v_β, as shown in (2), may contain PS and NS components at harmonic frequencies if the unbalanced three-phase voltages include harmonic distortions. Hence, a BPF is required to extract the FFPS components.

B. BPF Based on CDSC

The characteristics of the CDSC operator as a filter are well studied in the technical literature [15-18]. The orthogonal voltages of the FFPS component can be extracted by using the $CDSC_{4,8,16,32}$ operator when the three-phase voltages are unbalanced and distorted by odd harmonics. The frequency response of the $CDSC_{4,8,16,32}$ operator is shown in Fig. 4 [15]. As it can be seen, the $CDSC_{4,8,16,32}$ operator can extract the FFPS component without any phase shift and amplitude attenuation. It can reject both the PS and NS components of all odd harmonics including the FFNS one. On the other hand, all the odd and even harmonics including the FFNS one and dc offset can also be eliminated by using the $CDSC_{2,4,8,16,32}$ operator.

The block diagram implementation of the $CDSC_{4,8,16,32}$ operator is shown in Fig. 5, where $C_8=\cos(2\pi/8)$, $S_8=\sin(2\pi/8)$ and N is the number of voltage samples in one fundamental time period. As it can be seen, the $CDSC_{4,8,16,32}$ operator is formed by combining DSC_4, DSC_8, DSC_{16}, and DSC_{32} in chain. The $CDSC_{4,8,16,32}$ operator has two inputs and two outputs. The v_α and v_β voltages are used as the inputs and the orthogonal voltages (v_α^+ and v_β^+) of the FFPS component are obtained from the outputs. The number of delays shown in the DSC operator can be integer or non-integer. For the non-integer value of the delays, a relatively simple linear interpolation operation can be executed to enhance the estimation accuracy. The dynamic time delay caused by the frequency adaptive $CDSC_{4,8,16,32}$ operator is 47%

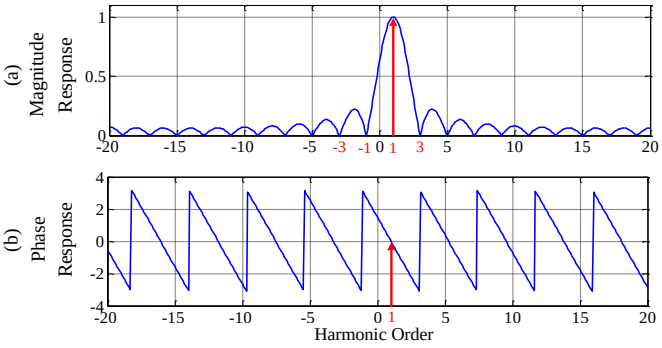


Fig. 4: Frequency response of the BPF based on the operator $CDSC_{4,8,16,32}$. (a) Magnitude response. (b) Phase response.

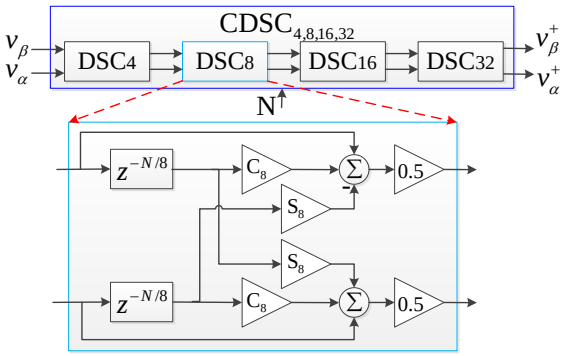


Fig. 5: Block diagram implementation of the BPF based on the $CDSC_{4,8,16,32}$ operator for extracting the orthogonal voltages of the FFPS component.

(=1/4+1/8+1/16+1/32) of the fundamental period. It can be seen from Fig. 5 that the DSC_8 operator is relatively simple to implement and hence the $CDSC_{4,8,16,32}$ operator can be easily executed for the real-time application. The DSC_2 can also combined with the $CDSC_{4,8,16,32}$ to form the operator $CDSC_{2,4,8,16,32}$. In this case, an additional half fundamental time period is required by the operator $CDSC_{2,4,8,16,32}$ when compared to the $CDSC_{4,8,16,32}$ one under dynamic condition. In our proposed technique, the value of N (=f_s/f, where f_s is a fixed sampling frequency) is updated by using the estimated fundamental frequency, as can be noticed in Fig. 3. The outputs of the frequency adaptive CDSC operator can be expressed by

$$\begin{bmatrix} v_\alpha^+(n) \\ v_\beta^+(n) \end{bmatrix} = \begin{bmatrix} A^+\sin(\omega n T_s+\theta^+) \\ A^+\cos(\omega n T_s+\theta^+) \end{bmatrix} = \begin{bmatrix} A^+\sin\{\phi^+(n)\} \\ A^+\cos\{\phi^+(n)\} \end{bmatrix} \quad (3)$$

C. Arctangent Approximation

An arctangent function can be employed to calculate the phase angle of the FFPS component, as expressed by

$$\phi^+(n) = \arctan\left\{v_\alpha^+(n)/v_\beta^+(n)\right\} \quad (4)$$

However, the arctangent operation is computationally demanding for real-time application [22]. Moreover, the division of v_α^+/v_β^+ is ill-conditioned when the value of the voltage sample $v_\beta^+=0$. To avoid the inverse tangent operation and ill-condition, the following approximation function can be used to estimate the FFPS instantaneous phase angle from the extracted orthogonal voltages [22].

$$\phi^+(n) = \begin{cases} \pi+\varphi^+(n) & \text{for } v_\alpha^+(n)<0 \ \&\ v_\beta^+(n)<0 \\ 2\pi-\varphi^+(n) & \text{for } v_\alpha^+(n)<0 \ \&\ v_\beta^+(n)>0 \\ \pi-\varphi^+(n) & \text{for } v_\alpha^+(n)>0 \ \&\ v_\beta^+(n)<0 \\ \varphi^+(n) & \text{for } v_\alpha^+(n)>0 \ \&\ v_\beta^+(n)>0 \end{cases} \quad (5)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

where $\varphi^+(n)=\frac{\pi}{2}.\frac{0.6404\left|v_\alpha^+\right|\left|v_\beta^+\right|^2+\left|v_\beta^+\right|\left|v_\alpha^+\right|^2+\left|v_\alpha^+\right|^3}{\left|v_\beta^+\right|^3+1.6404\left|v_\alpha^+\right|\left|v_\beta^+\right|^2+1.6404\left|v_\beta^+\right|\left|v_\alpha^+\right|^2+\left|v_\alpha^+\right|^3}$

and | | symbol indicates absolute value. In this case, the peak value of approximation error is 0.00811° which is very small [22]. The absolute values of v_α^+ and v_β^+ are used in (5) for calculating φ^+. The value of v_α^+ is maximum when v_β^+ is zero and vice versa. Therefore, the denominator of (5) is always positive and non-zero. As a result, the ill-condition for calculating the instantaneous phase angle from the orthogonal voltage signals v_α^+ and v_β^+ is avoided.

D. Fundamental Frequency Estimation

An auxiliary algorithm is used in the proposed method for tracking the fundamental frequency. It combines the second harmonic generation process and TEO.

D-1. Second Harmonic Generation

The Clarke transformed voltage signal v_α, as shown in (2), under unbalanced condition can be written as

$$\begin{aligned}v_\alpha(n)&=A^+\{\sin(\omega nT_s)\cos(\theta^+)+\cos(\omega nT_s)\sin(\theta^+)\}\\&\quad-A^-\{\sin(\omega nT_s)\cos(\theta^-)+\cos(\omega nT_s)\sin(\theta^-)\}\\&=\sin(\omega nT_s)\{A^+\cos(\theta^+)-A^-\cos(\theta^-)\}\\&\quad+\cos(\omega nT_s)\{A^+\sin(\theta^+)-A^-\sin(\theta^-)\}\\&=\sin(\omega nT_s)A_\alpha\cos(\theta_\alpha)+\cos(\omega nT_s)A_\alpha\sin(\theta_\alpha)\\&=A_\alpha\sin(\omega nT_s+\theta_\alpha)\end{aligned}\tag{6}$$

where

$$\begin{aligned}A_\alpha\cos(\theta_\alpha)&=A^+\cos(\theta^+)-A^-\cos(\theta^-)\\A_\alpha\sin(\theta_\alpha)&=A^+\sin(\theta^+)-A^-\sin(\theta^-)\\A_\alpha&=\sqrt{\{A_\alpha\cos(\theta_\alpha)\}^2+\{A_\alpha\sin(\theta_\alpha)\}^2}\\&=\sqrt{A^{+2}+A^{-2}-2A^+A^-\cos(\theta^+-\theta^-)}\\\theta_\alpha&=\tan^{-1}\frac{A^+\sin(\theta^+)-A^-\sin(\theta^-)}{A^+\cos(\theta^+)-A^-\cos(\theta^-)}\end{aligned}$$

Similarly, the Clarke transformed voltage signal v_β, as shown in (2), under unbalanced condition can be expressed as

$$v_\beta=A_\beta\cos(\omega nT_s+\theta_\beta)\tag{7}$$

where

$$\begin{aligned}A_\beta&=\sqrt{A^{+2}+A^{-2}+2A^+A^-\cos(\theta^+-\theta^-)}\\\theta_\beta&=\tan^{-1}\frac{A^+\sin(\theta^+)+A^-\sin(\theta^-)}{A^+\cos(\theta^+)+A^-\cos(\theta^-)}\end{aligned}$$

In the proposed technique, the voltage signals v_α and v_β, as expressed in (6) and (7), are multiplied to generate the second harmonic. Their multiplication can be expressed by

$$\begin{aligned}v_{eh}(n)&=v_\alpha(n)v_\beta(n)=A_\alpha A_\beta\sin(\omega nT_s+\theta_\alpha)\cos(\omega nT_s+\theta_\beta)\\&=0.5A_\alpha A_\beta\{\sin(2\omega nT_s+\theta_\alpha+\theta_\beta)+\sin(\theta_\alpha-\theta_\beta)\}\\&=A_{\alpha\beta}\sin(2\omega nT_s+\theta_{\alpha\beta})+A_{\alpha\beta}\sin(\theta_{\beta\alpha})\end{aligned}\tag{8}$$

where $A_{\alpha\beta}=0.5A_\alpha A_\beta$, $\theta_{\alpha\beta}=\theta_\alpha+\theta_\beta$ and $\theta_{\beta\alpha}=\theta_\alpha-\theta_\beta$. Expression (8) contains second harmonic and a dc value when the undistorted three-phase voltages are unbalanced. However, the generated dc value can be zero under balanced condition due to $\theta_{\beta\alpha}=0$ for $A^-=0$ and $\theta_\alpha=\theta_\beta=\theta^+$. On the other hand, high-order even harmonics including the second one can be present in (8) when the fundamental component of the unbalanced three-phase voltages is distorted by odd harmonics. Moreover, odd harmonics can be generated in (8) when even harmonics are present in the three-phase voltages. So, v_{eh} always includes the second harmonic whether the balanced/unbalanced three-phase voltages contain harmonics or not. The generated second harmonic component can be extracted for the fundamental frequency detection.

D-2. BPF for Second Harmonic Extraction

The recursive DFT (RDFT) of the voltage signal v_{eh} can be expressed as follows [23].

$$V_k(n)=V_k(n-1)+\{v_{eh}(n)-v_{eh}(n-P)\}e^{-j\frac{2\pi kn}{P}}\tag{9}$$

where P indicates the window size, k is the frequency index and j is the complex operator. The value of P is the number of voltage samples in the window. The real and imaginary parts of the RDFT can also be tracked by (10) and (11), respectively [23].

$$\mathrm{Re}\{V_k(n)\}=\mathrm{Re}\{V_k(n-1)\}+\{v_{eh}(n)-v_{eh}(n-P)\}\cos(\frac{2\pi kn}{P})\tag{10}$$

$$\mathrm{Im}\{V_k(n)\}=\mathrm{Im}\{V_k(n-1)\}+\{v_{eh}(n)-v_{eh}(n-P)\}\sin(\frac{2\pi kn}{P})\tag{11}$$

where Re and Im indicate the real and imaginary operators, respectively. A real time-domain signal with a single frequency can be extracted using the following expression based on the inverse RDFT operation [24].

$$v_{kN/P}(n)=\frac{1}{P}[\mathrm{Re}\{V_k(n)\}\cos(\frac{2\pi nk}{P})+\mathrm{Im}\{V_k(n)\}\sin(\frac{2\pi nk}{P})]\tag{12}$$

For a window size of one fundamental cycle (P=N) and k=2, this approach can extract the second harmonic component by rejecting all the odd and other even harmonics including the fundamental one at a cost of one fundamental cycle dynamic delay. This configuration is useful when the three-phase grid voltages contain DC offset, odd and even harmonics. On the other hand, expression (12) can extract the generated second harmonic component by eliminating all other high-order even harmonics for a window size of half fundamental cycle and k=1 at a cost of half fundamental cycle dynamic delay. This configuration is useful when the three-phase grid voltages contain only odd harmonics. So, the above approach with a half fundamental cycle window can be used in the proposed technique for tracking the generated second harmonic when the grid voltages contain odd harmonics. The output of the BPF based on (12) can be expressed by

$$v_2(n)=A_{\alpha\beta}\sin(2\omega nT_s+\theta_{\alpha\beta})\tag{13}$$

An additional advantage of using this approach is that it can provide the amplitude estimation of the extracted second harmonic component as it relies on the RDFT operation. The amplitude of the extracted second harmonic component can be obtained as follows [23].

$$A_{\alpha\beta}(n)=\sqrt{[\mathrm{Re}\{V_k(n)\}]^2+[\mathrm{Im}\{V_k(n)\}]^2}\,/\,P\tag{14}$$

where k=1 or 2 depending on the size of the window P=N/2 or P=N, respectively.

D-3. TEO for Frequency Estimation

The expression of the TEO for v_2 can be expressed as follows [25-28].

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

$$A_{\alpha\beta}^2(n)\sin^2\left[2\omega T_s\right] = v_2^2(n-1) - v_2(n)v_2(n-2)$$

$$\Rightarrow f = (\sin^{-1}\sqrt{\gamma})/4\pi T_s \quad (15)$$

where $\gamma = \{v_2^2(n-1) - v_2(n)v_2(n-2)\}/A_{\alpha\beta}^2(n)$. As it can be seen, the TEO can be employed to track the fundamental frequency from three consecutive voltage samples when the amplitude of v_2 is known. However, expression (15) requires computationally demanding square root and inverse sine operations. These computationally demanding operations can be avoided by using a polynomial function as follows.

$$f = \sigma_1\gamma^3 - \sigma_2\gamma^2 + \sigma_3\gamma + \sigma_4 \quad (16)$$

where σ_1=50454854.888, σ_2=1014758.195, σ_3=12000.361 and σ_4=15.37262. The values of the above coefficients are obtained using a curve-fitting command 'polyval' in MATLAB by considering 10 kHz sampling frequency and ±10 Hz variation of the fundamental frequency. The frequency difference between the actual relation and approximated function (16) at different fundamental frequencies is shown in Fig. 6. As it can be noticed, the maximum frequency error created by the approximated function is around 0.01 Hz.

The TEO is sensitive to the presence of unwanted frequency components, as it depends on only three consecutive voltage samples. So, it requires robust pre-filtering for extracting the second harmonic and its amplitude. The RDFT method used for the BPF may experience an accumulation error [23]. However, the amplitude accumulation error is eliminated by normalising the second harmonic component using the estimated amplitude. On the other hand, the accumulated phase error is assumed to be constant within the three consecutive voltage samples of the second harmonic component. The TEO algorithm, as shown in (15), is not affected by the constant accumulated phase error for calculating the fundamental frequency.

E. Tuning

The proposed technique shows that the Clarke transformation, CDSC operator and arctangent approximation operation do not contain any feedback path, thus they are unconditionally stable. On the other hand, the frequency estimation approach is also an open-loop structure and stable if the RDFT based BPF is fixed tuned at the nominal frequency of the second harmonic. In this case, the performance of the TEO may degrade when the fundamental frequency deviates from the nominal value because the fixed tuned BPF may not be able to reject unwanted frequency components. However, to obtain improved results, the window size of the BPF may be adaptively adjusted by the estimated fundamental frequency. The adaptive window approach introduces a feedback path in the frequency estimation algorithm. In this case, to obtain stable frequency estimation, the response time of the TEO should be equal or slower than the window size of the BPF [15, 24, 26]. However, the response time of the TEO (relies on only 3 consecutive samples) is actually faster than the window size of the BPF due to PT_s>$3T_s$. For this reason, a first-order infinite-impulse-response LPF can be cascaded with the TEO to provide the required additional time delay to make the frequency estimation stable [15, 24, 26]. In this case, the bandwidth of the LPF should be equal or smaller than the one used for the BPF. The overall dynamics of the proposed method due to the use of the frequency adaptation and LPF will be slower as the LPF introduces a time delay. The dynamic delay will depend on the time constant of the LPF.

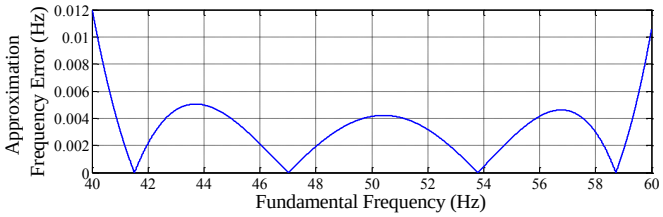


Fig. 6. Frequency error created by the curve-fitting relation (16) for a sampling frequency of f_s=10 kHz.

Table I: Percentage of harmonics specified in European standard EN 50160

Harmonics						THD
3rd	5th	7th	9th	11th	13th	10.464%
5%	6%	5%	1.5%	3.5%	3%	

However, the time delay of the LPF helps to make the frequency estimation stable when a frequency feedback loop is used for the adaptive RDFT based BPF. The slower the response time of the LPF, the slower will be the overall dynamics and the more will be the stability margin of the method.

IV. Simulation Results

Simulated performance of the proposed TEO-CDSC technique is investigated and compared with the pre-filter based CDSC-PLL [15] and in-loop filter based *dq*CDSC-PLL [16] methods. All methods are implemented in MATLAB/Simulink for a sampling frequency of 10 kHz. For a fair comparison, the same number of DSC operators (DSC_4, DSC_8, DSC_{16} & DSC_{32}) are used in all three techniques. The respective references are followed to tune other parameters of the CDSC-PLL and *dq*CDSC-PLL methods. Throughout the simulation studies for comparison, the fundamental component of the three-phase grid voltages is contaminated by harmonics. The percentage of the contaminated harmonics with a total harmonic distortion (THD) of 10.464% is shown in Table I and their amplitudes are chosen according to the European standard EN 50160 [29]. The following case studies are carried out for performance analysis.

Case-1. Steady-State with Harmonics

The steady-state phase error generated by the proposed TEO-CDSC, CDSC-PLL and *dq*CDSC-PLL methods under harmonics is presented in Fig. 7. In this case, the fundamental frequency is varied from 45 Hz to 55 Hz. It can be seen from Fig. 7 that the phase error produced by the *dq*CDSC-PLL method is increasing when the fundamental frequency deviation is increasing from the nominal value. The maximum phase errors created by the proposed, CDSC-PLL and *dq*CDSC-PLL methods are around 0.03°, 0.015° and 0.6°, respectively, for the fundamental frequency variation range of ±5 Hz from the nominal value.

Case-2. Unbalanced Amplitude Step with Harmonics

The distorted three-phase voltage waveforms with unbalanced amplitude steps are shown in Fig. 8(a). The fundamental voltage amplitude steps are +0.2 pu, -0.2 pu and -0.4 pu, from their nominal value for the phases 'a', 'b' and 'c', respectively. The harmonic contents are changed accordingly to keep the THD constant. The responses of the proposed, CDSC-PLL, and *dq*CDSC-PLL techniques are depicted in Figs. 8(b) and (c). As it can be seen, the proposed technique spends around 10 ms and 15 ms as response time for estimating the actual frequency and phase angle, respectively, under dynamic condition. When compared to

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

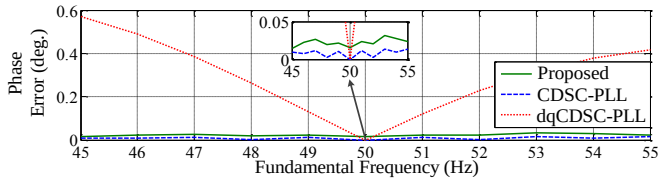


Fig. 7. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under steady-state with harmonics.

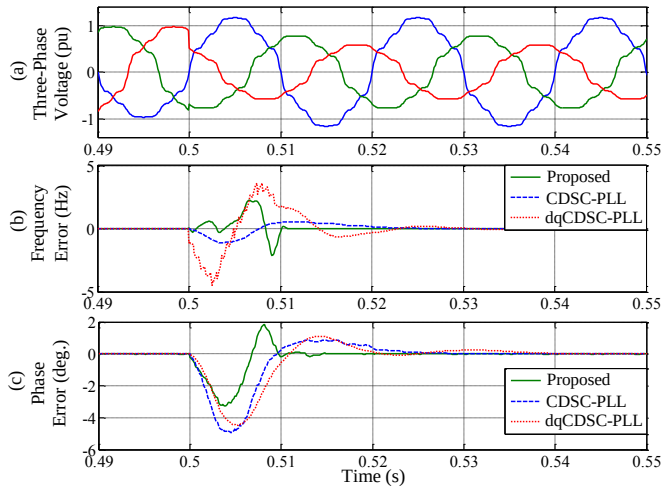


Fig. 8. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under harmonics and unbalanced amplitude steps (1 to 1.2 pu, 1 to 0.8 pu and 1 to 0.6 pu for the phases 'a', 'b' and 'c', respectively, at time 0.5s). (a) Three-phase voltage waveforms. (b) Estimated fundamental frequency error. (c) Estimated FFPS phase error.

the proposed one, both the PLL based techniques show slower response and spend more than 20 ms as transient time for tracking the same parameters under the amplitude step condition.

Case-3. Phase Step with Harmonics

Fig. 9 shows the transient responses of the proposed, CDSC-PLL, and *dq*CDSC-PLL techniques under a phase step including harmonics. The phase step created at time 0.5 s is -20°. In this case, when compared to the CDSC-PLL and *dq*CDSC-PLL techniques, the proposed one shows quicker response for tracking both the fundamental frequency and phase angle. The proposed TEO-CDSC, CDSC-PLL, and *dq*CDSC-PLL techniques take 17.3 ms, 24.3 ms and 34.3 ms, respectively, as settling time for tracking the -20° phase step, as can be noticed in Fig. 9(b).

The settling time comparison among the proposed TEO-CDSC, CDSC-PLL, and *dq*CDSC-PLL techniques under different phase steps including harmonics is shown in Fig. 10. The settling time is estimated based on ±2% error criteria. Fig. 10 shows that the maximum settling time required by the proposed TEO-CDSC, CDSC-PLL, and *dq*CDSC-PLL techniques are 17.8 ms, 26.9 ms and 35 ms, respectively for a phase step range of ±50°. For this condition, the proposed technique improves the settling time for the phase step estimation by 33.83% and 49.14% as compared to the CDSC-PLL and *dq*CDSC-PLL techniques, respectively.

Case-4. Frequency Step with Harmonics

The performance comparison among the proposed TEO-CDSC, CDSC-PLL and *dq*CDSC-PLL techniques under a frequency step and harmonics condition is shown in Fig. 11. The harmonic contents are shown in Table I and the fundamental frequency step created at time 0.5 s is –2 Hz. The settling time taken by the proposed and CDSC-PLL methods are 11 ms and 20.8 ms, respectively, for estimating the frequency step, as can be seen in Fig. 11(a). However, the

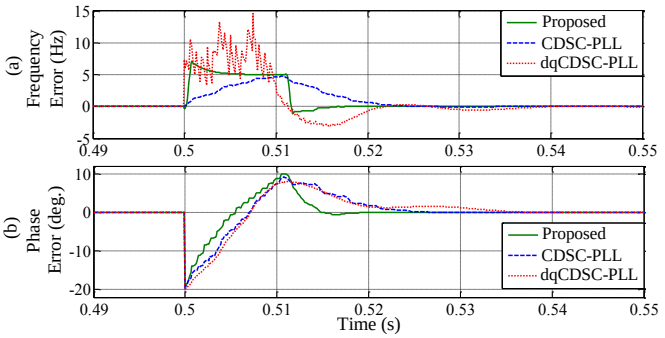


Fig. 9. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under harmonics and -20° phase step at time 0.5 s. (a) Estimated fundamental frequency error. (b) Estimated FFPS phase error.

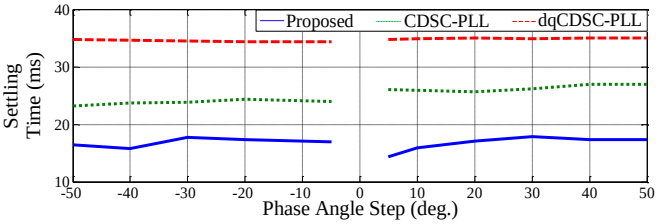


Fig. 10. Simulated settling time required by the proposed, CDSC-PLL and *dq*CDSC-PLL techniques for the estimation of the phase angle steps under harmonics.

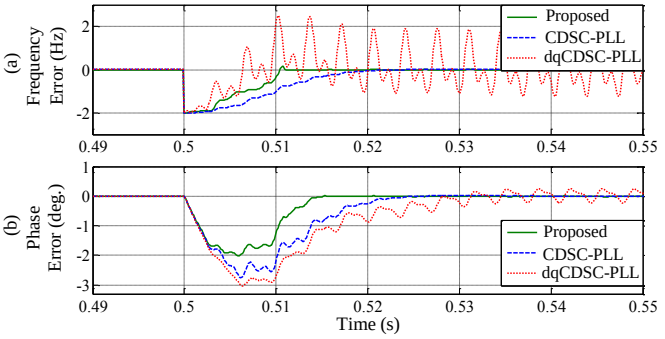


Fig. 11. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under harmonics and -2 Hz step of the fundamental frequency. (a) Estimated fundamental frequency error. (b) Estimated FFPS phase error.

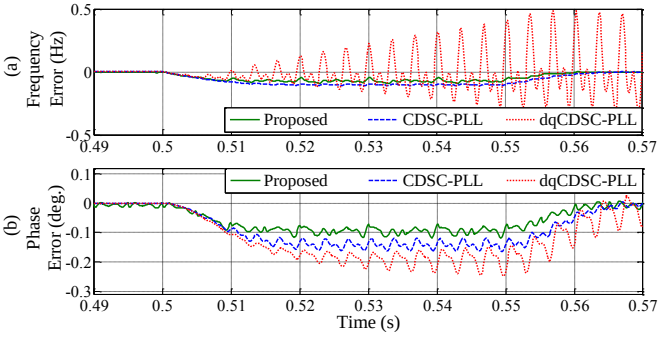


Fig. 12. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under harmonics and -10 Hz/s sweep of the fundamental frequency. (a) Estimated fundamental frequency error. (b) Estimated FFPS phase error.

fixed tuned CDSC based *dq*CDSC-PLL technique produces higher ripples in the estimated off-nominal fundamental frequency. On the other hand, it can be noticed from the phase estimation shown in Fig. 11(b) that the proposed technique takes less than 15 ms to converge to the actual value of the phase angle and also shows a faster response when compared to other two techniques.

Case-5. Frequency Sweep with Harmonics

Fig. 12 demonstrates the dynamic responses of the proposed TEO-CDSC, CDSC-PLL, and *dq*CDSC-PLL

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics

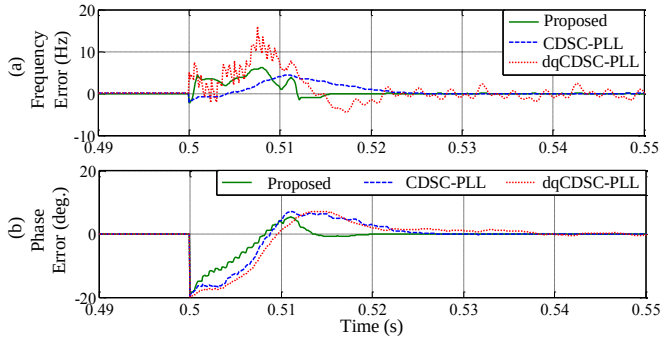


Fig. 13. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under harmonics, -2 Hz frequency step, -20° phase step and unbalanced amplitude steps (+0.2 pu, -0.2 pu and -0.4 pu) including harmonics. (a) Estimated fundamental frequency error. (b) Estimated FFPS phase error.

techniques under harmonics and frequency sweep condition. In this case, the fundamental frequency sweep is -10 Hz/s and it starts from 50 Hz and stops at 49.5 Hz. The frequency sweep of the harmonics is also changed accordingly. The time range of the frequency sweep is 0.5 s to 0.55 s. It can be noticed from Fig. 12 that the proposed TEO-CDSC technique generates smaller transient error in both the estimated fundamental frequency and instantaneous phase angle under the frequency sweep condition as compared to other two PLL based techniques.

Case-6. Steps in Frequency, Phase and Amplitude with Harmonics

The performances of the proposed, CDSC-PLL, and *dq*CDSC-PLL techniques for a combination of frequency step, phase step and unbalanced amplitude step including harmonics are demonstrated in Fig. 13. In this case, the fundamental frequency and phase steps are -2 Hz and -20°, respectively. The fundamental voltage amplitude steps are +0.2 pu, -0.2 pu and -0.4 pu, from their nominal value for the phases 'a', 'b' and 'c', respectively. The harmonic contents are changed accordingly to keep the THD constant. Similar to the individual case studies presented above, the proposed technique generates quicker transient response to follow the frequency and phase angle steps under this adverse condition. The proposed technique also requires less than one nominal fundamental cycle (20 ms) as the response time.

Case-7. Steady-State with DC Offset and Harmonics

Fig. 14 demonstrates the steady-state performance of the proposed, CDSC-PLL, and *dq*CDSC-PLL techniques under DC offset and harmonics condition. In this case study, the $CDSC_{2,4,8,16,32}$ operator is used in all the three compared techniques. For performance analysis, different DC offsets are injected in different phase voltages. The voltage waveforms of phases 'a', 'b' and 'c' in Fig. 14(a) contain 0.05 pu, 0.10 pu and 0.15 pu DC offsets, respectively. It can be noticed from Figs. 14(b) and (c) that the proposed and CDSC-PLL methods are able to reject the negative effects caused by the DC offset and also generate improved phase and frequency estimation when compared to the *dq*CDSC-PLL one.

V. Experimental Results

The real-time performance comparison between the proposed and MSTOGI-PLL [13] techniques is carried out by several experimental case studies in a laboratory setup. The dSPACE DS1104 control board platform is used to conduct the experiments. The proposed and MSTOGI-PLL methods in MATLAB/Simulink environment are uploaded to the

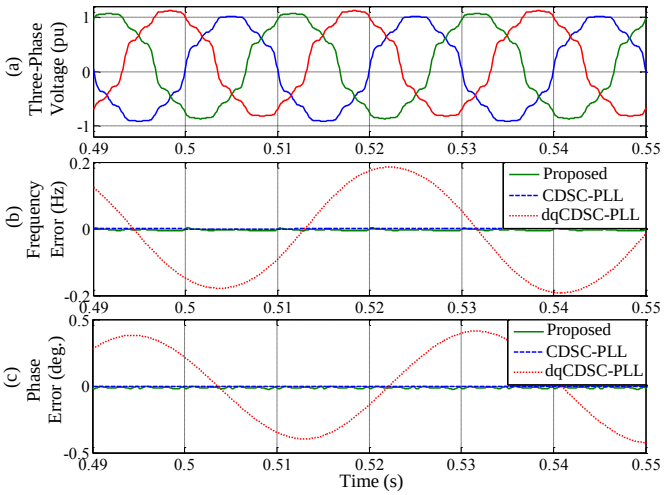


Fig. 14. Simulated performance comparison among the proposed, CDSC-PLL and *dq*CDSC-PLL techniques under DC offset (0.05 pu, 0.10 pu and 0.15 pu for the phases 'a', 'b' and 'c', respectively) and harmonics. (a) Three-phase voltage waveforms. (b) Estimated fundamental frequency error. (c) Estimated FFPS phase error.

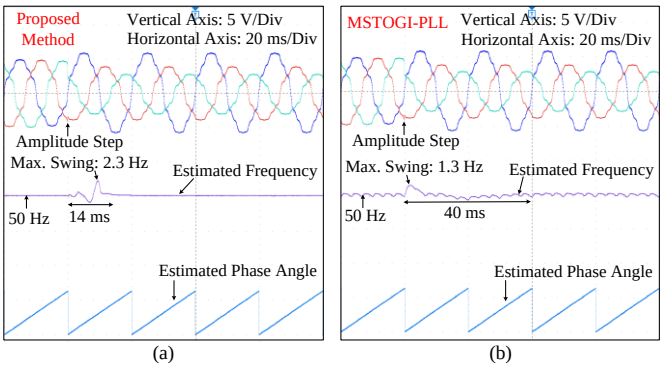


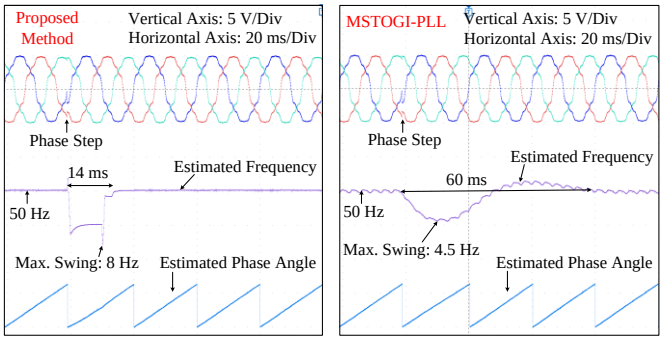
Fig. 15. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under harmonics and unbalanced amplitude steps (1 to 1.2 pu, 1 to 0.8 pu and 1 to 0.6 pu for the phases 'a', 'b' and 'c', respectively).

DS1104 control board using automatic code generation process. The real-time three-phase voltages with various grid events are produced by the DS1104 with the help of the digital-to-analog converters. The generated real-time three-phase voltages are sent to the inputs of the techniques through the analog-to-digital converters of the DS1104. Throughout the experimental studies, the fundamental component of the three-phase grid voltages is polluted by harmonics, as presented in Table I. The real-time experimental results are taken from the display of a digital oscilloscope.

The fundamental voltage amplitudes steps of +0.2 pu, -0.2 pu and -0.4 pu for the phases 'a', 'b' and 'c', respectively, are used to observe the real-time performances of the proposed and MSTOGI-PLL techniques. The voltage waveforms and responses of the proposed and MSTOGI-PLL techniques are shown in Fig. 15. As it can be observed, the proposed and MSTOGI-PLL methods generate maximum around 2.3 Hz and 1.3 Hz swing, respectively, in the estimated fundamental frequency under the considered amplitude step condition. However, the proposed technique can track the frequency and phase angle with a dynamic time of less than one nominal fundamental cycle. On the other hand, the MSTOGI-PLL method requires around two nominal fundamental cycles as the dynamic time. Moreover, the MSTOGI-PLL method produces more ripples at steady-state in the estimated fundamental frequency.

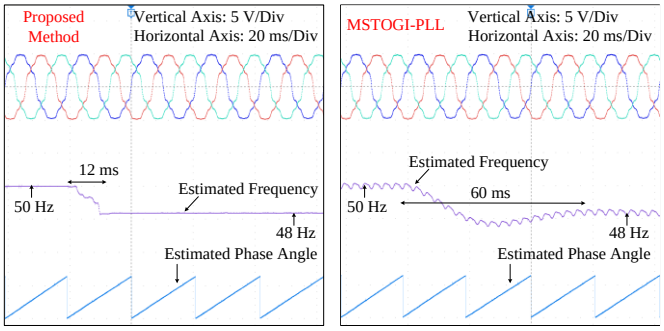
A phase step of -20° including harmonics is used for evaluating the real-time performance comparison between the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3044058, IEEE Journal of Emerging and Selected Topics in Power Electronics



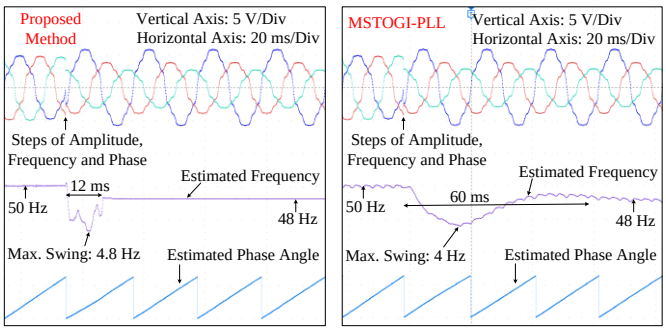
(a) (b)

Fig. 16. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under -20° phase step and harmonics.



(a) (b)

Fig. 17. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under -2 Hz fundamental frequency step and harmonics.



(a) (b)

Fig. 18. Real-time experimental performance comparison between the (a) proposed and (b) MSTOGI-PLL techniques under a combination of harmonics, fundamental frequency step (-2 Hz), phase step (-20^0), and unbalanced amplitude step (1 to 1.2 pu, 1 to 0.8 pu and 1 to 0.6 pu for the phases 'a', 'b' and 'c', respectively).

proposed and MSTOGI-PLL techniques. The voltage waveforms and responses of both techniques are depicted in Fig. 16. As it can be seen, the proposed technique shows larger swing in the estimated frequency but needs less dynamic time when compared to the MSTOGI-PLL. In this case, the proposed method requires less than one nominal fundamental cycle whereas the MSTOGI-PLL one spends around three nominal fundamental cycles as the dynamic time.

The performances of the proposed and MSTOGI techniques for the fundamental frequency step of -2 Hz including harmonics is shown in Fig. 17. In this case, around 12 ms and 60 ms are taken by the proposed and MSTOGI-PLL techniques, respectively, as the response time for following the fundamental frequency step.

The performance comparison for a combination of frequency step, phase step, and amplitude step is shown in Fig. 18. In this case, the steps of the fundamental frequency, phase angle and amplitudes are –2 Hz, -20°, and +0.2 pu, -0.2 pu and -0.4 pu, respectively, from the nominal value. It can be seen from Fig. 18 that the proposed and MSTOGI-PLL methods produce around 4.8 Hz and 4.0 Hz swing, respectively, in the estimated fundamental frequency. However, the proposed technique shows quicker response and generates accurate frequency and phase angle with a response time less than 20 ms whereas 60 ms is required by the MSTOGI-PLL method.

VI. Conclusions

A fast and robust technique based on the Teager energy and delayed signal cancellation operators has been reported in this paper for instantaneous phase angle estimation of three-phase voltage systems. When compared to the delayed signal cancellation based phase-locked loops, the proposed technique removes interdependent loops between the frequency and phase estimation, thus increasing the overall stability and easing the tuning process. Moreover, it avoids the phase loop of the phase-locked loop, thus eliminates the requirement of in-loop and loop filters. As a result, the tuning of these filters is not required and a faster response is produced. It also avoids the online operation of the inverse trigonometric functions. In addition, it shows harmonics immunity at steady-state and generates fast dynamic response with a settling time less than one nominal fundamental cycle. The presented simulated and experimental results have confirmed the practical application of the technique.

References

[1] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "A PLL-based controller for three-phase grid-connected power converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 911-916, 2018.

[2] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A new hybrid PLL for interconnecting renewable energy systems to the grid," *IEEE Trans. Ind. App.*, 2013.

[3] H. Saxena, A. Singh, and J. N. Rai, "Adaptive spline-based PLL for synchronisation and power quality improvement in distribution system," *IET Generation, Transmission & Distribution*, vol. 14, no. 7, pp. 1311 – 1319, April 2020.

[4] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1894-1907, 2017.

[5] S. Golestan, M. Ramezani, J. Guerrero, F. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Overview and design guidelines," *IEEE Trans. Power Elect.*, 2013.

[6] I. Carugati, S. Maestri, P. G. Donato, D. Carrica, and M. Benedetti, "Variable sampling period filter PLL for distorted three-phase systems," *IEEE Trans. Power Elect.*, vol. 27, no. 1, pp. 321-330, Jan. 2012.

[7] F. Gonzalez-Espin, E. Figueres, and G. Garcera, "An adaptive synchronous-reference-frame phase-locked loop for power quality improvement in a polluted utility grid," *IEEE Trans. Ind. Elect.*, vol. 59, no. 6, pp. 2718-2731, June 2012.

[8] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1194-1204, 2011.

[9] M. Karimi-Ghartemani, M. Mojiri, A. Safaee, J. A. Walseth, S. A. Khajehoddin, P. Jain, *et al.*, "A new phase-locked loop system for three-phase applications," *IEEE Trans. Power Elect.*, vol. 28, no. 3, pp. 1208-1218, Mar. 2013.

[10] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A robust synchronization to enhance the power quality of renewable energy systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4858-4868, Aug. 2015.

[11] A. Luna, J. Rocabert, J. I. Candela, J. R. Hermoso, R. Teodorescu, F. Blaabjerg, *et al.*, "Grid voltage synchronization for distributed generation systems under grid fault conditions," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3414-3425, 2015.

[12] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Elect.*, vol. 58, no. 1, pp. 127-138, Jan. 2011.

[13] C. Zhang, X. Zhao, X. Wang, X. Chai, Z. Zhang, and X. Guo, "A grid synchronization PLL method based on mixed second- and third-order generalized integrator for dc offset elimination and frequency adaptability," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1517-1526, Sept. 2018.
[14] M. S. Reza, M. M. Hossain, and A. M. Y. M. Ghias, "Open-Loop Approach for Robust Detection of Selective Harmonic in Single-Phase System," *IEEE Transactions on Industrial Informatics*, vol. 15, no. 12, pp. 6260-6269, December 2019.
[15] Y. F. Wang and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1987-1997, July 2011.
[16] S. Golestan, M. Ramezani, J. M. Guerrero, and M. Monfared, "dq-Frame cascaded delayed signal cancellation-based PLL: Analysis, design, and comparison with moving average filter-based PLL," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1618-1632, 2015.
[17] F. A. S. Neves, H. E. P. d. Souza, M. C. Cavalcanti, F. Bradaschia, and E. J. Bueno, "Digital filters for fast harmonic sequence component separation of unbalanced and distorted three-phase signals," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3847-3859, 2012.
[18] Y. N. Batista, H. E. P. d. Souza, F. A. S. Neves, R. F. D. Filho, and F. Bradaschia, "Variable-Structure Generalized Delayed Signal Cancellation PLL to Improve Convergence Time," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7146-7150, 2015.
[19] Y. F. Wang and Y. W. Li, "Three-Phase Cascaded Delayed Signal Cancellation PLL for Fast Selective Harmonic Detection," *IEEE Trans. on Ind. Elect.*, vol. 60, no. 4, pp. 1452-1463, Apr. 2013.
[20] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1067-1080, 2011.
[21] M. M. Canteli, A. O. Fernandez, L. I. Eguiluz, and C. R. Estebanez, "Three-phase adaptive frequency measurement based on Clarke's transformation," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1101-1105, July 2006.
[22] X. Girones, C. Julia, and D. Puig, "Full quadrant approximations for the arctangent function," *IEEE Signal Proc. Maga.*, vol. 30, no. 1, pp. 130-135, Jan. 2013.
[23] H. A. Darwish and M. Fikri, "Practical considerations for recursive DFT implementation in numerical relays," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 42-49, Jan. 2007.
[24] M. S. Reza, M. M. Hossain, and V. G. Agelidis, "Fast and accurate frequency estimation in distorted grids using a three-sample based algorithm," *IET Generation, Transmission & Distribution* vol. 13, no. 18, pp. 4242 – 4248, Sept. 2019.
[25] J. F. Kaiser, "Some useful properties of Teager's energy operators," in *IEEE Int. Conf. Acous. Spe. Signal Proc.*, 1993, pp. 149-152.
[26] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Single-phase grid voltage frequency estimation using teager energy operator-based technique," *IEEE Journal of Emerg. and Selec. Topics in Power Elect.*, vol. 3, no. 4, pp. 1218-1227, Dec. 2015.
[27] I. Kamwa, A. K. Pradhan, and G. Joos, "Robust detection and analysis of power system oscillations using the Teager-Kaiser energy operator," *IEEE Trans. on Power Syst.*, vol. 26, no. 1, pp. 323-333, Feb. 2011.
[28] M. A. Eldery, E. F. El-Saadany, and M. M. A. Salama, "A simple energy operator computational method for voltage flicker assessment," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1743-1750, July 2006.
[29] European Standard EN-50160, "Voltage characteristics of electricity supplied by public distribution systems," 1999.

Md. Shamim Reza received his B.Sc. and M.Sc. degrees in Electrical and Electronic Engineering (EEE) from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2006 and 2008, respectively, and the Ph.D. degree in Electrical Engineering from the University of New South Wales (UNSW), Sydney, NSW, Australia in 2014. After his PhD degree, he worked as a Research Associate at the School of Electrical Engineering and Telecommunications, UNSW. He also served as a Lecturer, Assistant Professor and Associate Professor at the Department of EEE of BUET. Currently he is working as a Professor at the same Department of BUET. His research interests include grid synchronization, distributed generations, power electronics, smart metering, power quality analysis, and applications of signal processing for electrical power engineering.

Md Maruf Hossain (S'13–M'16) received the B.Sc. and M.Sc. degrees in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2006 and 2011, respectively, and the Ph.D. degree in electrical engineering from the University of Memphis, Memphis, TN, USA in 2016. He is currently serving as Associate Professor of Electrical Engineering at the Resch School of Engineering in University of Wisconsin-Green Bay, USA. Prior to this current position, he was the Herff Fellow at the University of Memphis. His areas of interest include electrical power system's stability and control, power quality, solar and wind energy systems, renewable energy integration in the power grid, and smart grid system.

Ahmed O. Nasif (M'14) received his B.Sc. degree in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology, Bangladesh, in 2003, the M.S.E. degree in Electrical Engineering from Wright State University, USA, in 2005, and the Ph.D. degree in Electrical and Computer Engineering from George Mason University, USA, in 2009. Currently, he is an Associate Professor at the University of Wisconsin-Oshkosh, Wisconsin, USA. His research interests are in novel applications of modeling and signal processing techniques to next generation communication and sensor systems and networks, including biomedical signals and systems, the internet-of-things (IoT) and nanotechnology.

Vassilios G. Agelidis (S'89-M'91-SM'00-F'16) was born in Serres, Greece. He received the B. Eng. degree in electrical engineering from the Democritus University of Thrace, Thrace, Greece, in 1988, the M.S. degree in applied science from Concordia University, Montreal, QC, Canada, in 1992, and the Ph.D. degree in electrical engineering from Curtin University, Perth, Australia, in 1997. He has worked at Curtin University (1993–1999), University of Glasgow, U.K. (2000–2004), Murdoch University, Perth, Australia (2005–2006), the University of Sydney, Australia (2007–2010), and the University of New South Wales (UNSW), Sydney, Australia (2010–2016).

He is currently a professor at the Department of Electrical Engineering, Technical University of Denmark. Dr. Agelidis received the Advanced Research Fellowship from the U.K.'s Engineering and Physical Sciences Research Council in 2004. He was the Vice-President Operations within the IEEE Power Electronics Society from 2006 to 2007. He was an AdCom Member of the IEEE Power Electronics Society from 2007 to 2009 and the Technical Chair of the 39th IEEE Power Electronics Specialists Conference, Rhodes, Greece, 2008.