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Analysis of Charge Pump Topologies for High Voltage Mobile Microphone Applications

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***Abstract*—This paper presents a novel analysis of charge pump topologies for very high voltage capacitive drive micro electro-mechanical system microphones. For the application, the size and power consumption are sought to be minimized, and a voltage gain of 36 is achieved from a 5 V supply. The analysis compares known charge pump topologies, taking into consideration on resistance of transistors and parasitic capacitances of transistors and capacitors in a 180 nm silicon-on-insulator process. The analysis finds that the Pelliconi charge pump topology is optimal for generating very high bias voltages for micro electro-mechanical system microphones from a low supply voltage when the power consumption and area are limited by the application.**

***Index Terms*—Charge pumps; High voltage techniques; Microelectromechanical systems; Microphones; Silicon-on-insulator.**

I. INTRODUCTION

Microphones are used in a wide array of consumer products, such as smart phones, smart watches, laptops, headsets, and tablets [1]. Today, the most widely used type of microphone is the Micro Electro-Mechanical System (MEMS) microphone, as this type of microphone may have a long range of benefits over the alternatives [2]. Multiple applications seek microphones with higher Signal-to-Noise Ratio (SNR) performance to improve or add features. One application is smart assistants, such as Amazons Alexa and Apples Siri [3], where a limitation to the user experience is how well the voice command is picked up. Distinguishing speech from noise is easier if the SNR of the microphone is high.

The dominant contribution to noise in MEMS microphones is the squeezed-film effect [1], [4], which can be reduced by increasing the distance between the backplate and the diaphragm of the microphone. However, doing this will also reduce the signal strength, unless the bias voltage is increased as the air gap is increased. Recent studies have looked into improving the SNR by increasing the air gap and using a bias of a hundred volts or more [5], [6].

A limitation to using more than a hundred volts in a MEMS microphone is the generation of the high voltage, as only a low supply voltage is available in mobile products. Furthermore, MEMS microphones can be as small as 2.5 mm × 1.6 mm × 0.9 mm (Cirrus Logic CS7331P), which leaves very little room for electronics to generate high voltages from a low supply voltage. The most viable option is to go for a fully integrated solution on an Integrated Circuit (IC), as there is no room for discrete components in a MEMS microphone package. Inductors in ICs are generally unsuitable for power conversion, as integrated inductors exhibit poor performance, which leaves switched capacitor converters, such as charge pumps, as the most viable route.

A limitation to high voltage in ICs is the breakdown voltage of the process technology. This limitation can be mitigated by a type of process technology called "Silicon-On-Insulator" (SOI), which can sustain voltages of up to more than 200 V. In this work, a 180 nm SOI process with a breakdown voltage higher than 200 V is used as the targeted platform, and the device parameters to use in the analysis are extracted from the process technology.

The analysis carried out in this work has a focus on high voltage gain, small area, and low power consumption for mobile MEMS microphone applications. The specific goal is that the charge pump should be capable of reaching an output voltage of 180 V from a supply voltage of 5 V, while keeping the area less than 0.25 mm^2 and the power consumption less than 20 µW. As MEMS microphones are based on the capacitance between two plates, the only power consumption is the current leakage in the MEMS module. The current leakage is generally very small, and for a MEMS capacitor of 500 µm × 500 µm with an electric field of 2 MV/cm, the leakage was measured to be less than 1 nA [7]. Hence, the charge pump does not need to deliver significant power, as air gaps of multiple µm are common [1].

The remainder of this paper is organized as follows. Section II presents an analysis of voltage gain in charge pump topologies. In Section III, power loss analysis of selected topologies is carried out. Equivalent output resistance of selected topologies is calculated in Section IV. Settling time is investigated in Section V. Section VI provides a discussion on the two most promising topologies, and finally, the conclusions are presented in Section VII.

II. VOLTAGE SCALING OF CHARGE PUMPS

The most critical design goal for the target application is the generation of 180 V from a 5 V supply. Therefore, the first part of the analysis focuses on the voltage gain of different charge pump topologies.

Six general charge pump topologies were identified from

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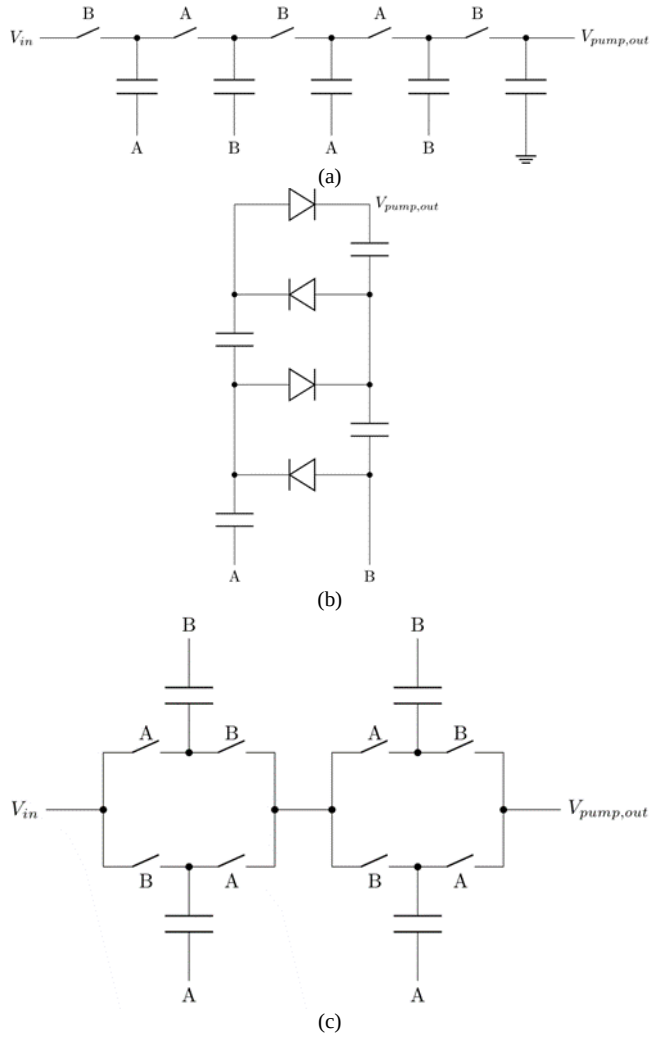
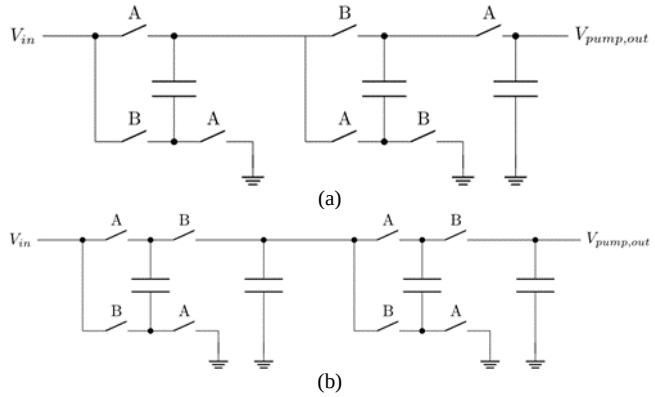
literature, namely, the Dickson [8], the Cockcroft-Walton [9], the Pelliconi [10], Makowski/Fibonacci [11], Doubler [12], and heap [13] charge pumps. Many other topologies exist, but they are in essence just modified versions of the listed topologies, and therefore feature the same voltage gains, voltage swings, and device stresses. The six topologies are depicted in Fig. 1 and Fig. 2, where the clock signals *A* and *B* are non-overlapping.



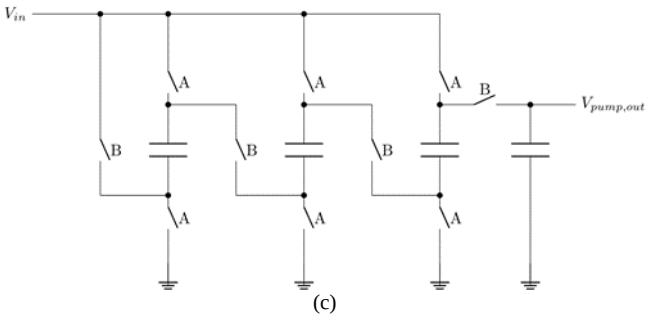
(a) (b) (c)

Fig. 1. The Dickson, Cockcroft-Walton, and Pelliconi charge pump topologies: a) 4-stage Dickson topology; b) 4-stage Cockcroft-Walton topology; c) 2-stage Pelliconi topology.

The voltage gain of all six charge pump topologies can be explained using the generic charge pump topology shown in Fig. 3(a).



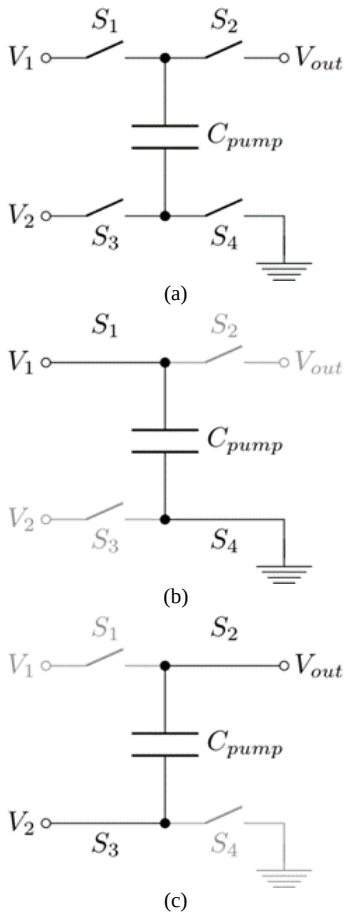
(a) (b)



(c)

Fig. 2. The Fibonacci, Doubler, and Heap charge pump topologies: a) 2-stage Fibonacci topology; b) 2-stage Doubler topology; c) 3-stage Heap topology.

In one phase, the pump capacitor C_{pump} is charged to V_1, as depicted in Fig. 3(b). In the second phase, the capacitor bottom plate potential is lifted by V_2 and C_{pump} is pumping charge to the output, as depicted in Fig. 3(c), with an ideal output voltage of $V_1 + V_2$ The generic topology can represent one stage of all topologies in Fig. 1 and Fig. 2, the only thing that changes is where V_1 and V_2 is supplied from. For example, in the Doubler topology, both V_1 and V_2 are supplied from the previous stage, and in the Dickson topology, V_1 is supplied from the previous stage and V_2 from the clock signal.



(a) (b) (c)

Fig. 3. A generic representation of a charge pump stage and the two phase's stage may be in: a) Charge pump stage; b) Charging phase; c) Pumping phase.

High voltages are achieved with the mentioned charge pump topologies by cascading stages. The voltage gain of the different topologies as a function of the number of stages *N* is shown in Table I. Note that $\varphi = 1.618$ [14].

TABLE I. IDEAL VOLTAGE GAIN FOR A N STAGE CHARGE PUMP OF THE DIFFERENT TOPOLOGIES ($\varphi = 1.618$).

Topology	Voltage Gain
Dickson	$N+1$
Pelliconi	$N+1$
Heap	$N+1$
Cockcroft-Walton	$N+1$
Fibonacci	$\frac{\varphi^{N+2}-(1-\varphi)^{N+2}}{\sqrt{5}}$
Doubler	2^N

The voltages across, respectively, capacitors and transistors/diodes of the different topologies depend in most cases on what stage of the charge pump it is. For ideal charge pumps, the voltages across the different types of devices in stage *k* of a topology are listed in Table II.

TABLE II. MAXIMUM VOLTAGE ACROSS STAGES IN STAGE *K* OF THE DIFFERENT CHARGE PUMP TOPOLOGIES ($\varphi = 1.618$).

Topology	Transistor V_{max} [V]	Capacitor V_{max} [V]
Dickson	$2 \times V_{in}$	$k \times V_{in}$
Pelliconi	V_{in}	$k \times V_{in}$
Heap	$k \times V_{in}$	V_{in}
Cockcroft-Walton	$2 \times V_{in}$	$2 \times V_{in}$
Fibonacci	$\frac{\varphi^{k+1}-(1-\varphi)^{k+1}}{\sqrt{5}}$	$\frac{\varphi^{k+1}-(1-\varphi)^{k+1}}{\sqrt{5}}$
Doubler	$2^{k-1} \times V_{in}$	$2^{k-1} \times V_{in}$

When parasitic capacitances are introduced in a charge pump, the voltage gain changes due to charge sharing. To properly evaluate the voltage gain of the charge pump topologies, the parasitic capacitances due to devices should be included. Hence, the parasitic capacitances of active devices and capacitors were extracted from the SOI process.

Five different parasitic capacitances were extracted for the transistors: t gate to source C_{gs}, gate to drain C_{gd}, drain to source C_{ds}, source to handle wafer C_{sh}, and drain to handle wafer C_{dh} capacitance. For simplification, the bulk was connected to the source, which eliminates the source-to-bulk capacitance from calculations and combines the drain-to-bulk and drain-to-source capacitances into the drain-to-source capacitance. In the SOI process, the bulk is on top of an insulating silicon oxide, which is on top of a layer of substrate. The layer of substrate is also called the "Handle Wafer" (HW). This layering of bulk, insulator, and substrate creates a drain to HW capacitance C_{dh} and a source and bulk to HW capacitance C_{sh}. The capacitances are also depicted in Fig. 4.

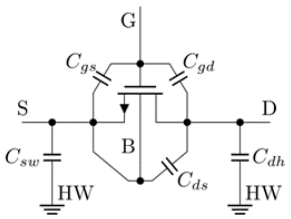


Fig. 4. Extracted parasitic capacitances of transistors.

For a HV diode, the anode to cathode capacitance C_{ac}, anode to HW capacitance C_{ah}, and cathode to HW capacitance C_{ch} were extracted (see Fig. 5).

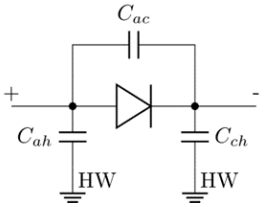


Fig. 5. Extracted parasitic capacitances of 10 V diode.

The parasitic capacitances extracted for a selected range of devices are listed in Table III, together with the minimum device area. The equivalent PMOS transistors of the process have the same voltage ratings and similar parasitic capacitances.

TABLE III. SELECTED SEMICONDUCTOR DEVICES FROM THE SOI PROCESS USED, THEIR SIZE AND PARASITIC CAPACITANCE.

Device	Size [μm²]	C_{gd} [fF]	C_{gs} [fF]	C_{ds} [fF]	C_{dh} [fF]	C_{sh} [fF]
5 V NMOS	3	0.05	0.05	0.13	0.04	0.04
10 V NMOS	19	0.53	0.27	0.08	0.02	0.02
100 V NMOS	510	< 0.01	30.56	12.44	4.04	4.83
200 V NMOS	1758	< 0.01	63.69	7.97	5.67	8.11
				C_{ac} [fF]	C_{ah} [fF]	C_{ch} [fF]
10 V diode	121	-	-	10.05	5.69	1.05

Capacitors have parasitic capacitances as well, this is depicted in Fig. 6, where the parasitic capacitance on the top plate $C_{par,top}$ of the capacitor may be different from the parasitic capacitance on the bottom plate $C_{par,bot}$ of the capacitor. For a range of capacitors available in the IC process, the parasitic capacitances were extracted. The extracted parasitic capacitances are listed in Table IV, along with the voltage rating and capacitance density of the respective capacitors. The parasitic capacitances for the capacitors are based on parasitic extraction from capacitors of 100 fF.

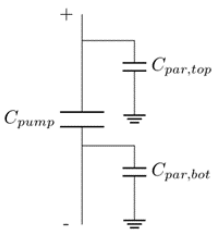


Fig. 6. Extracted parasitic capacitances of capacitors.

TABLE IV. FOUR CAPACITORS AVAILABLE IN THE USED SOI PROCESS AND THEIR PARASITIC CAPACITANCES AS A PERCENTAGE OF THE CAPACITOR CAPACITANCE.

Cap #	Type	Density $\left[\frac{\text{fF}}{\mu\text{m}^2}\right]$	Max voltage [V]	$C_{par,top}$ [%]	$C_{par,bot}$ [%]
1	MIM	2.4	5.5	0.1	1.7
2	MIM	2.0	10	0.5	2.7
3	MOM	0.6	60	3.9	3.9
4	MOM	0.2	200	0.4	50.0

All transistors in the SOI process have a maximum gate to source voltage of 5.5 V, including transistors rated for a +100 V drain to source voltage. Due to this limitation on the gate-to-source voltage, the Dickson and Cockcroft-Walton topologies must be run with a supply voltage of 2.5 V or lower, or run from a 5 V supply and utilize HV diodes. For the Heap, Fibonacci, and Doubler topologies, it is necessary to use 100 V transistors to reach an output voltage of 180 V.

The voltage scaling in Table I is only correct in the ideal case. When parasitic capacitances are introduced, the voltage gain is reduced due to charge sharing. In Fig. 7, a parasitic capacitance C_{par} is introduced on the node, where the top plate of the pumping capacitor is connected. With the parasitic capacitance present, the output voltage is given by

$$V_{out} = V_1 + V_2 \frac{C_{pump}}{C_{pump} + C_{par}}. \quad (1)$$

There is also a parasitic capacitance on the bottom plate, but, e.g., V_1 and V_2 are assumed to be ideal sources, hence the bottom plate parasitic would be connected directly to a supply, and therefore does not affect the voltage. If V_1 or V_2 are supplied from another charge pump stage, the parasitic capacitances on S_1, S_2, S_4, and the bottom plate parasitic capacitances would affect the voltage gain of the supplying stage.

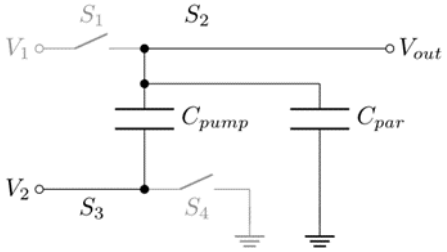


Fig. 7. Example of a parasitic capacitance affecting the output voltage of a charge pump in the pumping phase.

The capacitance C_{par} in Fig. 7 would contain the top plate parasitic capacitances of the capacitor, the parasitic capacitances of the devices used to realise S_1 and S_2, and wiring capacitance.

Expressions of the voltage gain in different topologies, when parasitic capacitances are considered, have been derived and are shown in Table V, where α is given by

$$\alpha = \frac{C_{pump,k}}{C_{pump,k} + C_{par,k}}, \quad (2)$$

where $C_{pump,k}$ is the effective pumping capacitance in stage k and $C_{par,k}$ is the combined parasitic capacitance in stage k on the top plate of the pumping capacitor.

TABLE V. OUTPUT VOLTAGE OF STAGE K OF THE DIFFERENT CHARGE PUMP TOPOLOGIES WHEN CHARGE SHARING IS CONSIDERED.

Topology	Output voltage V_k of stage k
Dickson	$V_{k-1} + V_{supply} \times \alpha$
Pelliconi	$V_{k-1} + V_{supply} \times \alpha$
Heap	$V_{supply} + V_{k-1} \times \alpha$
Cockcroft-Walton	$V_{k-1} + (V_{k-2} - V_{k-3}) \times \alpha$
Fibonacci	$V_{k-1} + V_{k-2} \times \alpha$
Doubler	$V_{k-1} + V_{k-1} \times \alpha$

Given a Dickson topology realised using diodes, depicted in Fig. 8, which is transitioning from phase A to B, the parasitic capacitance in stage 2, denoted $C_{par,2}$, is expressed as

$$C_{par,2} = C_{ac,D2} + C_{ah,D3} + C_{ch,D2} + C_{par,top,C2}. \quad (3)$$

The pumping capacitance is $C_{pump,k} = C_2$. In (3), $C_{ac,D2}$ is C_{ac} of D_2, $C_{ah,D3}$ is C_{ah} of D_3, $C_{ch,D2}$ is C_{ch} of D_3, and $C_{par,top,C2}$ is $C_{par,top}$ of C_2. Only the C_{ac} of D_2 is included in the expression, as C_{ac} of D_3 is in parallel with the conducting diode. Furthermore, it is assumed that the capacitance C_1 is much larger than the capacitance C_{ac} of D_2, such that the reduction in parasitic capacitance due to the serial connection of capacitors is negligible.

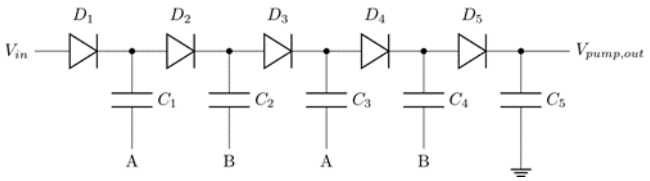


Fig. 8. Diode-based realisation of 4 stages of the Dickson charge pump topology.

In Table V, V_0, V_{-1}, and V_{-2} are equal to V_{supply} the supply voltage. For the Heap, Cockcroft-Walton, and Fibonacci topologies, the stacking of capacitors lowers the effective pumping capacitance, but not the parasitic capacitances. The effective pumping capacitance $C_{pump,k}$ for the Heap, Cockcroft-Walton, and Pelliconi topologies is listed in Table VI, where $C_{stage,k}$ is the capacitance of the capacitor used in stage k. For subscript values of 0 or less, $C_{pump,k-1}$ and $C_{pump,k-2}$ should be omitted from the expressions. For the Dickson, Pelliconi, and Doubler topologies, $C_{pump,k} = C_{stage,k}$, as there is no stacking of capacitors.

To compare the voltage gain capability of the different topologies, the voltage gains for implementations of 0.04 mm^2 and 0.25 mm^2 were calculated using the expressions from Table V and Table VI. The 0.25 mm^2 is the target area, and the 0.04 mm^2 was used to investigate if the topologies could be implemented on less area. Devices used for the calculations were chosen from Table III and Table IV, based on the voltage stress of each device in each stage of the charge pump, which was identified using the

expressions from Table II.

TABLE VI. EFFECTIVE PUMPING CAPACITANCE OF THE HEAP, COCKCROFT-WALTON, AND FIBONACCI TOPOLOGIES.

Topology	Effective $C_{pump,k}$ of stage k
Heap	$\frac{1}{C_{stage,k}^{-1}+C_{pump,k-1}^{-1}}$
Cockcroft-Walton	$\frac{1}{C_{stage,k}^{-1}+C_{pump,k-2}^{-1}}$
Fibonacci	$\frac{1}{C_{stage,k}^{-1}+\left(C_{pump,k-1}+C_{pump,k-2}\right)^{-1}}$

The calculations of voltage gain only consider the reduced voltage gain that is due to charge sharing between pumping capacitors and parasitic capacitances. Voltage drops across diodes and transistors, the area to implement level shifters, the power required to drive level shifters, and leakage were not included in the calculations. The calculations were carried out numerically. First, the area for active devices was allocated based on the used devices and the number of stages, then the remaining area was allocated to capacitors. For each topology, the number of stages was optimized towards achieving the lowest number of stages required to reach a voltage gain of 36, or to the highest attainable voltage gain if a gain of 36 could not be reached.

For all calculated implementations, devices of sufficient voltage rating were used where necessary to save area and maximize pumping capacitance. For example, in the first stage of the Doubler topology, 5 V transistors are used, and in the last stage, 100 V transistors are used. Furthermore, for the Doubler topology, only half of the area was used to yield the area for the capacitors between stages [12]. In topologies, where capacitors are stacked, a higher voltage gain may be achieved by tapering of capacitor sizes [15], this has not been done in the calculations of this paper. Instead, each stage has been allocated an equal amount of area for pumping capacitors. A tapered Heap topology may achieve a 30 % higher voltage gain than a non-tapered Heap topology [15]. For all of the Pelliconi topology, 5 V transistors were used, and for all Cockcroft-Walton and Dickson topologies, 10 V diodes were used.

The calculated voltage gains for the charge pump implementations on a 0.04 mm^2 and 0.25 mm^2 area can be read from the plots in Fig. 9 and Fig. 10.

The Dickson, Fibonacci, Pelliconi, and Doubler topologies were in calculations, all able to reach a voltage gain of 36, both with the 0.04 mm^2 and the 0.25 mm^2 area constraint. From Fig. 9 and Fig. 10, it can be observed that the Pelliconi topology requires fewer stages than the Dickson topology when the area is constrained to 0.04 mm^2. This is due to less parasitic capacitance in each stage and the smaller size of devices used in the Pelliconi topology, both enabled by the lower voltage stress on the transistors.

The Heap and Cockcroft-Walton topologies were not able to reach a voltage gain of 36 at the given area constraints when parasitic capacitances were included. To obtain a voltage gain of 36 with the Heap topology, the area needed to be approximately 11 mm^2. This area could be lower if tapering was used, but even with tapering, the 0.04 mm^2 or 0.25 mm^2 implementations would not reach a voltage gain of 36. No matter how much the area was increased, the Cockcroft-Walton could not reach a voltage gain beyond approximately 14 due to the parasitic capacitances of the capacitors and diodes available in the process. If the input voltage is reduced to 2.5 V to allow the use of diode-coupled 5 V transistors, the voltage gain increases to approximately 18, but the required voltage gain to reach 180 V increases to 72.

As the Heap and Cockcroft-Walton topologies are not able to obtain a voltage gain of 36 with a supply voltage of 5 V, the two topologies are not feasible for the target application on the used platform. In the following section, a further analysis of the Dickson, Pelliconi, Fibonacci, and Doubler topologies is carried out.

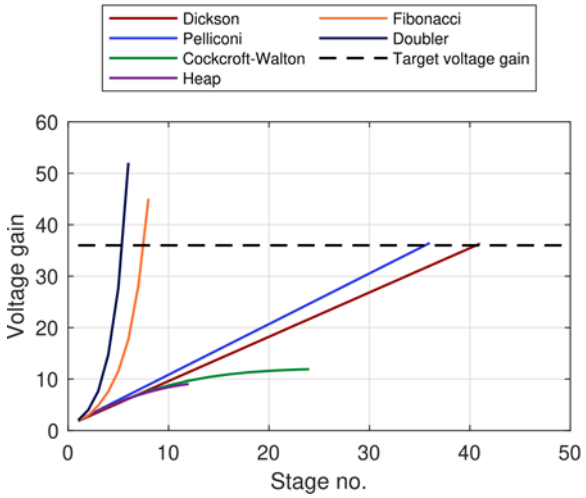


Fig. 9. Voltage gain of charge pumps on a 0.04 mm^2 area with parasitic capacitances present.

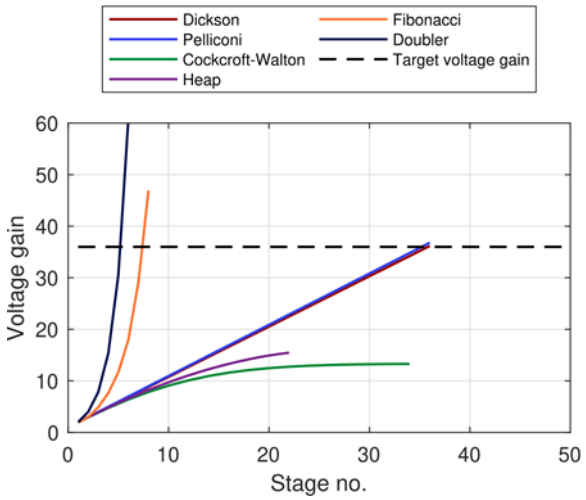


Fig. 10. Voltage gain of charge pumps on a 0.25 mm^2 area with parasitic capacitances present.

III. DYNAMIC POWER LOSSES IN CHARGE PUMPS

As the target application is a capacitive load, the output power is low. At 2 nA and 180 V, the output power is only 360 nW. It is therefore very likely that the power consumption of the charge pump is dominated by switching losses to parasitic capacitances. To determine the most viable charge pump topology, the selected power losses to parasitic capacitances were estimated. Given an ideal

voltage gain for each of the four topologies, the node voltages and the associated voltage swings were determined for each topology.

Switching losses were estimated using (4)

$$P_{loss} = f_{clk} C_{par} V_{swing}^2, \quad (4)$$

where f_{clk} is the switching frequency of the charge pump, C_{par} is the combined parasitic capacitance connected to the node in the topology with the highest voltage swing and the most parasitic capacitance, and V_{swing} is the voltage swing at the identified node.

For the Fibonacci and Doubler topologies, the two nodes in each charge pump with the highest voltage swing were chosen for power loss estimation. The voltage swings of the last stages of the Fibonacci are depicted in Fig. 11, and for the last stages of the Doubler, in Fig. 12, along with the nodes *A* and *B*, which represent the nodes with the highest voltage swing. The capacitor C_2 in Fig. 11 will have a potential of 111 V, thus the capacitor used for C_2 in the Fibonacci topology must be the 200 V capacitor from Table IV, which has a very large bottom plate parasitic capacitance. For the Doubler topology, the capacitor C_3 in Fig. 12 will have a voltage of 90 V, and it must also be a 200 V capacitor.

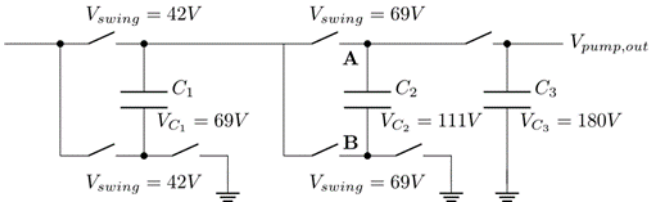


Fig. 11. Voltage swing in the last stages of an ideal Fibonacci charge pump.

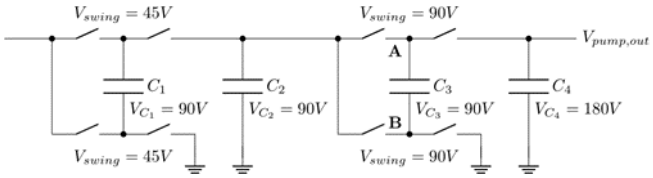


Fig. 12. Voltage swing in the last stages of an ideal Doubler charge pump.

The Dickson and Pelliconi topologies are different from the Fibonacci and Doubler topologies in terms of voltage swing, as the entire charge pumps have the same voltage swing of 5 V in every node. Instead of calculating the power loss in a single node, the parasitic capacitances, including the bottom plate parasitic of the capacitors, of all stages in the charge pumps were determined and used for power loss estimation.

The transistor realization of the Pelliconi topology is depicted in Fig. 13, as it can be observed that there are more than twice as many devices per stage as in the Dickson topology. However, due to the transistors having low voltage stresses, the topology can be implemented using 5 V transistors, which achieves that the Pelliconi topology has less parasitic capacitance than the Dickson topology.

For the four topologies, the parasitic capacitances were estimated by the device sizes found for the 0.04 mm^2 implementations to keep the parasitic capacitances and thereby the switching losses small. For the Doubler and Fibonacci topologies, the switching power loss was also calculated for implementations where the pumping capacitance of the last stage was reduced to 50 fF to minimize the parasitic capacitance. It was calculated that the pumps would maintain a voltage gain of at least 36.

The power losses were calculated using a 100 kHz switching frequency, and the results are listed in Table VII along with the identified voltage swings, pumping capacitance of the last stage in each pump, and the determined amount of parasitic capacitance used for power loss estimation. For the Dickson and Pelliconi topologies, C_{pump} is the pumping capacitance used in every stage of the charge pump.

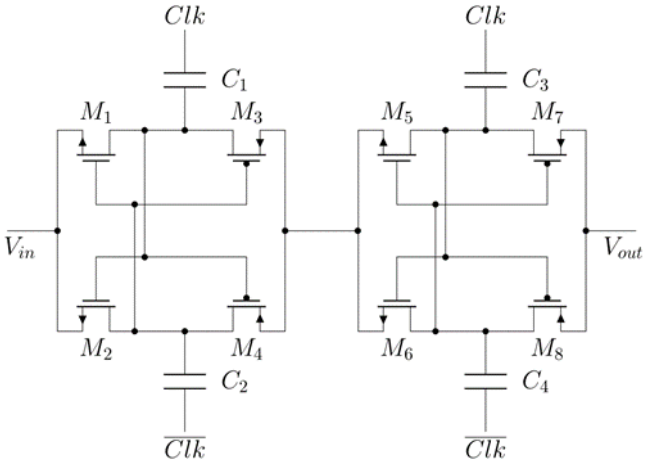


Fig. 13. Transistor realisation of two stages of the Pelliconi topology.

TABLE VII. ESTIMATED SWITCHING LOSSES IN HIGHEST SWING NODE IN CHARGE PUMPS @ 100 KHZ.

Topology	$C_{pump,N}$ [fF]	C_{par} [fF]	V_{swing} [V]	P_{loss} [μW]
Dickson 41 stages	171	4021.77	5	10.55
Pelliconi 36 stages	220	4221.20	5	10.05
Fibonacci 2 nodes	775	456.52	67	217.35
Fibonacci 2 nodes	50	91.12	67	43.38
Doubler 2 nodes	267	200.49	90	162.40
Doubler 2 nodes	50	91.12	90	73.81

Based on the estimated switching power losses, it can be observed that the Doubler and Fibonacci topologies cannot meet the power consumption criteria set in this work. If charge recycling was to be utilized to reduce power consumption, it would require HV transistors to implement, which would likely negate the benefit due to further added parasitic capacitances. This leaves the Dickson and Pelliconi charge pump topologies as the better choices to meet the design goals of this work, and they are therefore the only two topologies investigated in the following section.

IV. SWITCH CAPACITOR CONVERTER EQUIVALENT MODEL

The analysis so far has not considered the power that is to be delivered to the load. In [16], switched capacitor converters are modelled as the circuit depicted in Fig. 14, where the output voltage V_{out} of the converter is the voltage

division of the converter ideal output voltage. The ideal output voltage is defined by the ratio of *m/n* in the transformer, and the voltage division is defined by R_{out} and R_{load}. The output voltage is expressed by

$$V_{out} = V_{supply} \frac{m}{n} \frac{R_{load}}{R_{load} + R_{out}}, \quad (5)$$

where R_{out} is the equivalent output resistance of the converter (in this work, the equivalent output resistance of the charge pump) and R_{load} is the load resistance.

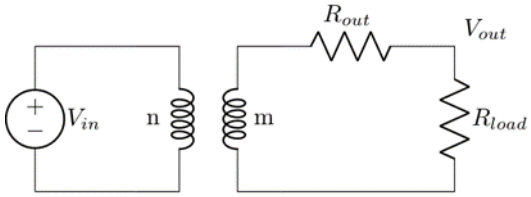


Fig. 14. Switched capacitor converter model as in [16].

The load resistance for this work is 90 GΩ, as this results in 2 nA at 180 V. In [16], the equivalent output resistance is estimated by

$$R_{out} = \sqrt{R_{FSL}^2 + R_{SSL}^2}, \quad (6)$$

where R_{FSL} defines the Fast Switching Limit (FSL) of the converter. R_{FSL} is a function of the on resistance of the switches used to realise the switched capacitor converter, and how the charge is transferred in the converter. In [16], FSL is defined by

$$R_{FSL} = \sum_{j=1}^{phases} \sum_{i=1}^{switches} \frac{1}{D_j} \left(a_{j,i}^r\right)^2 r_i, \quad (7)$$

where $a^r_{j,i}$ is a vector that defines how much charge is transferred by switches in each of the converter's phases, r_i is the on resistance of the different switches, and D_j is the duty cycle of each phase.

In (6), the R_{SSL} component defines the Slow Switching Limit (SSL), and is a function of the switching frequency, capacitor size, and how the charge is transferred by the capacitors in the converter in each phase. In [16], R_{SSL} is defined by

$$R_{SSL} = \sum_{j=1}^{phases} \sum_{i=1}^{capacitors} \left(a_{j,i}\right)^2 \frac{1}{2C_i f_{clk}}, \quad (8)$$

where $a_{j,i}$ describe the charge transfer by capacitors, C_i is the size of the various capacitors, and f_{clk} is the switching frequency of the converter. Details on how to define $a^r_{j,i}$ and $a_{j,i}$ can be found in [16].

The equivalent output resistance was calculated for 36 and 37 stage Pelliconi implementation, and for 41 and 42 stage Dickson implementation, all based on component values from a 0.04 mm^2 area restriction. The ideal voltage gain of the charge pump was based on the gain when parasitic capacitances are present. For the transistors in the Pelliconi topology, an on resistance of approximately 8 kΩ and 37 kΩ was extracted from the PDK for, respectively, minimum sized NMOS and PMOS transistors in the triode region. For the Dickson implementation, an equivalent on resistance of 8 kΩ was assumed for the diodes to be used in the calculations.

The calculated resistances and resulting output voltages for a 90 GΩ load are listed in Table VIII.

TABLE VIII. EQUIVALENT OUTPUT RESISTANCE AND OUTPUT VOLTAGE OF THE 0.04 MM^2 CHARGE PUMPS.

Topology	Ideal gain	R_{FSL} [kΩ]	R_{SSL} [GΩ]	R_{out} [GΩ]	V_{out} [V]
Dickson - 41 stages	36.32	1620.0	2.412	2.412	176.9
Dickson - 42 stages	37.05	1665.0	2.470	2.470	180.0
Pelliconi - 36 stages	36.45	656.0	1.636	1.636	179.0
Pelliconi - 37 stages	37.43	672.0	1.729	1.729	181.5

From Table VIII, it can be observed that the output resistance reduces the output voltage of the 36 stage Pelliconi and the 41 stage Dickson such that they do not reach an output voltage of 180 V. For the 37 stage Pelliconi and 42 stage Dickson charge pumps, the capacitor sizes were reduced to make room for another stage on the 0.04 mm^2. The additional stage increased the voltage gain and the equivalent output resistance, but the increase in voltage gain was higher than the increased reduction in output voltage, making it possible to reach 180 V. Even though the output resistance of the charge pump is high, the output voltage only diminishes a few percent due to the load being 90 GΩ. From the table, it can also be observed that the output resistance is dominated by the R_{SSL} component of R_{out}. For charge pump implementations with larger capacitors or higher switching frequency, R_{SSL} would be lower, and so would the equivalent output resistance.

As the Dickson and Pelliconi topologies still have comparable performance, the settling time performance will be analysed in the next section.

V. SETTLING TIME

Settling time for the charge pumps is also a significant parameter, as microphones often are turned on and off in mobile devices to save power. The equivalent output resistance of the converter and the capacitive load of the microphone will basically work as a capacitor charged through a resistor. The time constants and 95 % settling time were calculated for the Dickson and Pelliconi charge pumps based on a load of 10 pF and the equivalent output resistance from Table VIII. The resulting time constants and settling times are listed in Table IX.

TABLE IX. TIME CONSTANTS AND TIME TO REACH 95 % OF THE OUTPUT VOLTAGE WITH A LOAD OF 10 PF.

Topology	Time constant [ms]	95 % settling time [ms]
Dickson - 41 stages	24.12	72.26
Pelliconi - 36 stages	16.36	49.01

Based on the equivalent output resistance, the Dickson topology takes almost 50 % longer to reach 95 % of the maximum output voltage. Furthermore, this was based on

the Dickson being implemented with switches that had an on resistance of 8 kΩ. The Dickson topology is usually realised using diode-coupled transistors or diodes, as depicted in Fig. 8. When the Dickson charge pump approaches its maximum output voltage, the voltage across the diodes or diode-coupled transistors is reduced.

When the Pelliconi and Dickson charge pumps reach 90 % of their output voltage from a 5 V supply, there is approximately 0.25 V across each transistor in the Pelliconi topology, assuming equal voltage distribution and 0.439 V across each diode in the Dickson topology. For the Pelliconi topology, the transistors will operate in the triode region, and the charge pump will have the R_{out} listed in Table VIII. From the PDK, it was extracted that the 10 V diodes used in the Dickson topology with a voltage of 0.439 V across each conduct 34.62 pA, which is equivalent to a resistance of 12.7 GΩ.

The equivalent on resistance of 10 V diodes will dominate the equivalent output resistance of the Dickson charge pump, as 12.7 GΩ per diode results in an R_{FSL} = 1.04 TΩ. The heavily increased output resistance of the Dickson charge pump will not only increase the time constant significantly, it will also reduce the achievable output voltage of the loaded charge pump, which is obvious given that the current through the diodes must be 2 nA to satisfy the requirement of 180 V for a 90 GΩ load.

As the Pelliconi topology already exhibits better performance than the Dickson on settling time, voltage gain per stage, and power consumption parameters, it was decided not to investigate the equivalent output resistance of the Dickson topology further in this work. In the following section, the possible ways to get around the problem of 10 V diodes are discussed.

VI. DISCUSSION

Given the estimates in Table VII and Table VIII, the Dickson and Pelliconi topologies have a comparable performance. The lower voltage stress in the Pelliconi topology enables the use of 5 V devices, which results in a lower amount of parasitic capacitance. The lower amount of parasitic capacitance results in a lower power consumption, a higher voltage gain per stage, and a lower equivalent output resistance for the Pelliconi topology than what is achieved in the Dickson topology.

When the voltage-dependent behaviour of the devices used to implement switches in the topologies is taken into consideration, it is observed that the performance of the Dickson topology is reduced significantly, while the performance of the Pelliconi topology is only reduced slightly. In the Dickson topology, the performance decreases significantly as the charge pump settles and the voltage across the diodes is reduced. The reduced voltage across diodes leads to a much higher equivalent output resistance, which affects both the time constant for settling and the achievable output voltage negatively. The supply voltage of 5 V does not allow diode-coupled transistors to be used in place of the 10 V diodes. 10 V transistors in combination with level-shifters would mitigate the voltage stress and conductivity challenges, but require extra circuitry, leading to a higher power consumption and the introduction of additional parasitic capacitance. If the supply voltage were 2.5 V instead of 5 V, the Dickson topology would be able to use diode-coupled 5 V transistors instead of 10 V diodes. This would improve the performance of the Dickson topology, as the conductivity of diode-coupled transistors in the SOI process is higher than that of the 10 V diodes when small voltages are applied. Additionally, the parasitic capacitances in the Dickson topology would become less than the parasitic capacitances in the Pelliconi topology, and thereby improve the performance of the Dickson topology.

In the calculations estimating the implementations on 0.25 mm^2 and 0.04 mm^2, the area required for wiring and for the distance between devices were not included. If the capacitor sizes from those estimates were used for a physical implementation, the implementation would be larger than the area used for the calculations. As the estimate of a Pelliconi implementation of 0.04 mm^2 was able to reach 180 V, it should be possible to implement physically on less than the goal of 0.25 mm^2.

VII. CONCLUSIONS

In this paper, an analysis of known charge pump topologies was carried out to determine the optimal topology for a mobile microphone application. The goal of the analysis was to determine which charge pump topology is optimal for reaching 180 V from a 5 V supply, while keeping the area of an IC implementation below 0.25 mm^2 and the power consumption below 20 µW. It was determined that the two most suitable topologies are the Dickson and Pelliconi topologies, and that the Pelliconi outperforms the Dickson topology given the devices available in the SOI process used for device parameters. The Pelliconi topology is predicted to have a significantly shorter settling time than the Dickson topology due to the devices used. Dependent on the devices available, other charge pump topologies may exhibit better performance in other applications. Finally, the estimations of the Pelliconi topology indicate that the charge pump can be implemented on a chip area of less than 0.25 mm^2, as the 0.04 mm^2 estimations meet the output voltage and power consumption goals.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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