An Efficient Voltage Step-up/down Partial Power Converter (SUD-PPC) using Wide Bandgap devices

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Abstract—This paper proposed a novel topology for step-up/down converter based on the concept of partial power processing, which improves efficiency as well as power density. The unified modulation strategy achieves the auto transition between two operating modes without requiring any additional control. The operating principle is analyzed in detail, from which it is found that diode reverse recovery of Si MOSFETs reduces the voltage regulation range in step-down operation mode. Therefore, SiC MOSFET is employed in the high voltage side to avoid duty cycle loss. The SPICE simulations based on the SiC and Si devices have been built, and the simulation results verify the effect of using SiC devices. A 400V prototype based on SiC MOSFET has been built. Measurement results confirm the high efficiency in overall voltage range, and the maximum efficiency exceeds 99%.

Keywords—Step-up/down voltage regulation, partial power processing, unified modulation strategy, SiC devices

I. INTRODUCTION

Recently, Partial Power Processing (PPP) has presented significant advantages in power converter downsizing and efficiency improvement [1]. Compared to conventional full power converters (FPCCs), partial power converters (PPCs) reduce power rating of power electronic devices and systems in different applications, such as solar photovoltaic systems [2], energy storage systems (ESS) [3] and electric vehicle (EV) fast charging stations [4]. The PPC category contains the subcategories of series-connected PPC (S-PPC) and parallel-connected PPC (P-PPC) [5]. The P-PPCs are usually employed in PV module strings, also widely called as differential power processing, which achieve maximum power point tracking (MPPT) at fractional currents regulation [6]. S-PPCs achieve voltage difference regulation by connecting the PPC, input source and load in series, which was first proposed for photovoltaic applications in the spacecraft technology [7], as shown in Fig.1. Ref [8] and [9] summarized and reviewed the various PPP topologies for PV applications. An analysis and comparison between Dual Active Bridge (DAB) and Isolated Full Bridge Boost (IFBB) topologies based on component stress factor (CSF) is performed in [10]. Depending on the output voltage gain, S-PPCs can be further divided into three types: step-up PPC (SU-PPC), step-down PPC (SD-PPC), and step-up and down PPC (SUD-PPC). A SUD-PPC topology was presented in [11], and the results indicate that the SUD-PPC processes the least active power over the same voltage variation range compared to the other two PPCs, resulting in higher efficiency and power density. However, the unified modulation strategy for the SU and SD operating modes of the SUD-PPC is still a challenge.

On the other hand, high switching frequency also offers the possibility of increasing the power density due to the reduced size of passive components. Compared to Silicon (Si) MOSFET, wide bandgap (WBG) devices have smaller on-resistance, lower parasitic capacitance and higher operating temperature, thereby are considered as the promising candidates for high frequency power conversion applications [12], [13].

This paper presented a novel SUD PPC topology and the proposed unified modulation strategy achieves the auto switching between two operation modes in absence of any additional control. The rest of this paper is organized as follows. Section II introduces the operating principle of the proposed topology and modulation strategy. In Section III, duty cycle loss caused by the diode reserve recovery has been analysed. And the simulations results verify that SiC devices can be employed in high voltage side to solve this issue. Section IV presents the experimental results of a 400V prototype to verify the feasibility and practicality of the topology and modulation strategy. Finally, Section V concludes this paper.

II. OPERATING PRINCIPLE

![Fig.1 Schematic diagram of the S-PPC structure.](image)

Fig.2 shows the proposed SUD-PPC, where $V_{c2}$ is the voltage at the port in series with the power source and load in series; $I_{load}$ is the current across the load. It can be observed the system has two connection configurations. One is that the load is placed between points A and B, while the points C and D are connected by wires. Conversely, the load can be also placed between points C and D, while the points A and B is shorted. Two configurations have the same topological characteristics. Similarly to other S-PPCs, the power source, load and one port of the converter are connected in series. Therefore, the converter only processes a portion of the full power, i.e. $V_{c2}I_{load}$. Alternatively, a bidirectional topology can be obtained by replacing the $D_{1,4}$ with active switches. The converter has two operating modes: step-down mode and step-up mode. Fig.3 shows the drive signals and theoretical waveforms of the two operating modes, where $Q_{1,4}$ and $S_{1,4}$ are the drive signals for the corresponded switches in Fig.2; $d_{p}$ and $d_{i}$ are the duty cycle for the $Q_{1,4}$ and $S_{1,4}$, respectively, $d_{p} = d_{i} = 1$. The following is the analysis of the operational states of
two modes, and assume all devices are ideal and ignore power losses.

Fig.2 Configuration of the proposed SUD-PPC.

Fig.3 Driver signals and theoretical waveforms

A. Step-down operating mode

In the step-down mode, the range of \( d_s \) is from 0 to 1, thus \( d_s \) is always smaller than 0. \( Q_{1,4} \) maintain off in this operating mode. As shown in Fig.3, one switching period can be divided into 4 states or subintervals. The first two states are symmetrical to the last two states. Fig.4 shows the equivalent circuits of the first two operating states.

1) State 1, \( t_1-t_2: (d_s-0.5)\times T_s \)

In this subinterval, all low-voltage switches are turned on, power source charges to load directly and no power flows through the transformer and high voltage side, as shown in Fig.4 (a). The inductor current equals to load current, which uniform flows through both low-voltage side bridge arms. The inductor voltage \( v_L \) equals the difference between input voltage \( V_{in} \) and load voltage \( V_{load} \). The inductor voltage for this subinterval is given by

\[
v_L = L \frac{di_L}{dt} = V_{in} - V_{load}
\]

2) State 2, \( t_2-t_3: (1-d_s)\times T_s \)

At \( t_2 \), \( S_{2,3} \) are switched off, \( i_L \) is forced to flow through \( S_1 \) and \( S_4 \). Therefore, the power is transferred from low-voltage side to high-voltage side through the transformer, as shown in Fig.4(b). The inductor voltage side, the current flows through the body diode of \( Q_1 \) and \( Q_4 \). The inductor voltage for this subinterval is given by

\[
v_L = L \frac{di_L}{dt} = \frac{(n-1) \cdot V_{in}}{n} \cdot V_{load}
\]

B. Step-up operating mode

In the step-up mode, all low voltage side switches are on state. And same to step-down mode, one switching period can also be divided into 4 parts. Fig.5 shows the equivalent circuit of the first two operating modes.

1) State 1, \( t_6-t_7: (0.5-d_s)\times T_s \)

In this interval, \( Q_{1,4} \) are turned off while \( S_{1,4} \) are turned on, the power source \( V_{in} \) charges to the load directly, as shown in Fig.5 (a). No power flows through the transformer and high voltage side switches. Therefore, the inductor voltage for this subinterval is the same with that of State 1 in the step-down mode, which is given by

\[
v_{load} = \frac{(n + 2 \cdot d_s - 2) \cdot V_{in}}{n}
\]

2) State 2, \( t_7-t_8: d_s\times T_s \)

At \( t_7 \), \( Q_{1,4} \) are switched on. \( V_{ab} \) equals to \( V_{in} \), thereby \( V_{cd} \) equals to \( V_{ab}/n \). Power is transferred from high-voltage side to low-voltage side, as shown in Fig.5(b). The inductor voltage for this subinterval is given by
\[ V_L = L \frac{di_L}{dt} = \frac{(n+1) \cdot V_{in}}{n} - V_{load} \]  
\[ (5) \]

**Fig. 5** Equivalent circuit of the first two operating states in SU mode.

At \( t_s \), \( Q_1 \) and \( Q_2 \) are turned off, the rest two states begin. It can be observed that the converter works as the inverting isolated buck converter in this mode. Applying volt-seconds principle again, the output voltage in step-up mode is obtained by

\[ V_{load} = \left( \frac{n + 2}{n} \right) V_{in} \]  
\[ (6) \]

**C. Small-signal modeling**

\( d_q \) and \( d_s \) can be expressed by a unified modulation variable \( u \) in (7) and (8), as shown in Fig. 6.

\[ \begin{align*}
  d_s &= u \quad 0.5 \leq u < 1 \\
  d_s &= 1 \quad 1 \leq u < 1.5 \\
  d_q &= 0 \quad 0.5 \leq u < 1 \\
  d_q &= u - 1 \quad 1 \leq u < 1.5
\end{align*} \]  
\[ (7) \quad (8) \]

Substituting (7) and (8) into (3) and (6), the output voltage can be expressed

\[ V_{load} = \left( \frac{n + 2}{n} \right) V_{in} \]  
\[ (9) \]

Introducing (7) into (1) and (2), the averaged equations of inductor voltage in step-down mode is given

\[ \frac{d(i_L)}{dt} = \left( \frac{n + 2}{n} \right) \left( \frac{V_{in}}{T_s} \right) - \left( \frac{V_{load}}{T_s} \right), \quad 0.5 \leq u < 1 \]  
\[ (10) \]

Introducing (8) into (4) and (5), the averaged equations of inductor voltage in step-up mode is given

\[ \frac{d(i_L)}{dt} = \left( \frac{n + 2}{n} \right) \left( \frac{V_{in}}{T_s} \right) - \left( \frac{V_{load}}{T_s} \right), \quad 1 \leq u < 1.5 \]  
\[ (11) \]

\( i_{C2} \) equals the difference between the RMS value of the load current and \( i_L \), which can be expressed by

\[ i_{C2} = C_2 \frac{dV_{C2}}{dt} = \frac{V_{load}}{R} - i_L \]  
\[ (12) \]

Therefore, both modes have the same averaged equation of output capacitor current, which is given in (13).

\[ C_2 \frac{dV_{C2}}{dt} = \left( \frac{V_{load}}{T_s} \right) - \left( \frac{i_L}{T_s} \right) \]  
\[ (13) \]

Consequently, both operating modes of the converter have the same averaged state equations. The small signal equations for the system can be obtained by introducing perturbation around the steady state value for the state variables, such that \( i_L = i_L^* + \dot{i}_L \). Then neglecting the second-order terms, the linearized small-signal equations in Laplace domain, containing only the first-order ac terms, are given by the following equations.

\[ sL \dot{i}_L = \frac{\hat{V}_{in}}{n} + \frac{2V_{in}}{n} \hat{u} - \hat{v}_{load} \]  
\[ (14) \]

\[ sC_2(\hat{v}_{in} - \hat{v}_{load}) = \frac{\hat{v}_{load}}{R} - \hat{i}_L \]  
\[ (15) \]

Rearranging (15) results in the following equation

\[ \hat{\dot{i}}_L = \left( 1 + sRC_2 \right) \hat{\dot{v}}_{load} - sC_2 \hat{v}_{in} \]  
\[ (16) \]

Introducing (16) to (14), the control-to-output transfer function is obtained in (17).

\[ \frac{\hat{v}_{load}}{\hat{u}} \bigg|_{\hat{v}_{in} = 0} = \frac{2RV_{in}}{nR + s^2nLC_2R + snL} \]  
\[ (17) \]

Both operating modes have the same control-to-output transfer function, which means that only one common and unified controller is needed for both operating modes, as shown in Fig. 7.
III. DUTY CYCLE LOSS

In practice, Si MOSFET has long diode reverse recovery time, as shown in Fig. 8 [14]. Therefore, in step-down mode, after the low-voltage side switches have been turned on, the transformer voltage can not drop to 0 immediately due to the reverse recovery of the high-voltage switch, meaning that the new operating states take place between States 2 and 3, and States 4 and 1.

As an example, Fig. 9 shows the equivalent circuit of the added operation state occurred between States 2 and 3. At $t_1$, the capacitors of $Q_3$ and $S_3$ are turned on, the capacitors of $Q_2$ and $Q_1$ start charge to $Q_1$ and $Q_2$, and $Q_1$ and $Q_2$ start to reverse recovery. As a result, the voltage of $Q_2$ and $Q_1$ start to decrease, while voltage of $Q_1$ and $Q_2$ start to increase until the voltage of each high-voltage switch is same and equal to half of $V_{in}$.

In this period, $i_L$ flows through $S_2$ and $S_3$. Assuming $V_{cd}$ equals $V_{in}/n$ in this period, the inductor voltage equation can be expressed by (18)

$$V_L = \frac{d_i}{dt} - \frac{(n+1) \cdot V_{in}}{n} - V_{load}$$

Define $d_n$ as the division of $t_n$ and the switching period. After this subinterval, the low-voltage side is short again and State 1 begins. As a result, the duration of the Sate 1 and 3 reduce to $(u \cdot 0.5 \cdot d_n) \times T_s$.

Fig. 8 Diode recovery waveform [14]

Define $G(u)$ as the gain of the output voltage and input voltage. Considering the diode reverse recovery, $G(u)$ in the step-down mode is obtained

$$G(u) = \frac{(n + 2u - 2 + 2d_r)}{n}$$

(19)

The converter gain considering diode reverse recovery is increased while the regulation range is reduced. Since the $u$ must be larger than $d_r + 0.5$, the minimum value of the output voltage is given

$$V_{Load, min} = \frac{(n - 1 + 4d_r)}{n} V_{in}$$

(20)

A simulation based on the SPICE model was built in SIMetrix to verify the analysis above. Table I shows the semiconductor specifications. Level1 model for semiconductors was selected and the default temperature is 27 degrees. Fig. 10 shows the simulation waveforms at $u=0.7, V_{in}$ is 400V and load is 7Ω. It can be observed that $V_{load}$ is 368V and $t_r$ is 1.13 μs. Since the carrier wave frequency is 100kHz, $d_e$ is 0.113. Introducing $d_e = 0.113$ into (19). The theoretical output voltage is 369.6V. The simulation result shows an error of less than 0.5% compared to theoretical value.

TABLE I. SIMULATION SYSTEM SPECIFICATION

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>High-voltage switch</th>
<th>Low-voltage switch</th>
<th>Low-voltage diode</th>
<th>Switching frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>400V</td>
<td>IPW65R095C7</td>
<td>IRF200P223</td>
<td>V30200C</td>
<td>100kHz</td>
</tr>
</tbody>
</table>

In order to overcome this disadvantage, SiC devices can be employed in high-voltage side due to the shorter reverse recovery time. Fig. 11 show the simulation waveforms based on the SiC MOSFET IMW65R072M at $u=0.7$.
It can be observed that the SiC MOSFET has much shorter reverse recovery time, result in the negligible duty cycle loss. The simulation result of $V_{\text{load}}$ is 350 with an error of about 0.5% compared to the theoretical value 352V calculated in (9).

Considering the losses of semiconductor, inductor and transformer, the proposed presents high efficiency, as shown in Fig.12. It can be observed that the proposed SUD-PPC has the maximum efficiency operating at $\mu=1$, as the all power is transmitted directly to the load. There is only the conductive loss of the low-voltage side, and the maximum efficiency is approx.99.5%.

IV. EXPERIMENTAL RESULTS

A 400V prototype, as shown in Fig.13, has been built to verify the proposed topology and modulation strategy. The same semiconductor devices were used for the prototype as for the SiC based simulation. The experimental setup is also the same as the simulation. Input voltage is 400V, carrier wave frequency is 100kHz and load is 70Ω. Table II shows the rest main components. The interlink capacitors are placed at the ports of $Q_{1,4}$ to reduce voltage oscillation caused by hard switching. For the same reason, a $N_p:N_s=20:5$ PCB transformer was designed to reduce the leakage inductance. Since the block voltage of the output capacitor is the difference between $V_{\text{ab}}$ and $V_{\text{load}}$. A 10µF capacitor with block voltage of 100V is employed as the output capacitor, resulting in a much smaller volume.

**TABLE II PASSIVE COMPONENTS**

<table>
<thead>
<tr>
<th>Component</th>
<th>Input capacitor</th>
<th>Output capacitor</th>
<th>Interlink capacitor</th>
<th>Inductor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>B3291X1 MKP/SH</td>
<td>CKG57KX 7S22A106M</td>
<td>WIMA FKPI1</td>
<td>AGP423 3-153ME</td>
</tr>
<tr>
<td>Value</td>
<td>6.8 µF</td>
<td>10 µF</td>
<td>10nF</td>
<td>15 µH</td>
</tr>
</tbody>
</table>

Fig.12 Simulation efficiency versus $\mu$ at Vin=400V and load=70Ω

Fig.14 (a) and (b) shows the steady state experimental waveforms at $\mu=0.7$ or 1.2, respectively. As it can be observed, the output voltage in these two conditions is close to the theoretical values, which is 353.8V and 431 V, respectively. Additionally, duty cycle loss in the step-down mode can be neglected after using SiC MOSFET in high-voltage side.

Fig.15 shows the transient state waveform of the operation mode switching. In this condition, the reference value of $V_{\text{load}}$ is stepped from 360 to 435V. As it can be observed, the switching process is smooth, which verifies the feasibility of the proposed modulation strategy.

Fig.16 shows the experimental efficiency versus $\mu$. Two 1mΩ current shunt are placed into the circuit to measure the input and output voltage. The voltages of the current shunts and the input source and load are measured by 34465A Digit Multimeter. The experimental results of the system efficiency are close to the simulation results. The proposed topology has high efficiency in overall regulation range, and the maximum efficiency exceeds 99.5%.

![Fig.13 Experimental prototype of the SUD-PPC.](image)

![Fig.14 Steady state waveforms of the prototype](image)

![Fig.15 Transient waveforms of the operation mode switching](image)
This paper proposed a SUD-PPC topology with high efficiency. A unified modulation strategy has been presented for the two operating modes. The detailed analysis of the operating principles has been shown. Moreover, the cause of duty cycle loss is analyzed. As the solution, the SiC MOSFETs have been employed in high voltage side. Finally, a 400V prototype has been built and the experimental results verify the feasibility and practicality of the topology and modulation strategy.

In the future, the power losses of the topology will be analyzed. Moreover, the advantages and disadvantages of GaN and SiC devices in the proposed topology will be compared.

REFERENCES