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A High efficiency and High power density Asymmetrical Half-bridge Flyback Converter for Data Centers

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***Abstract*—The power consumption in data centers continues increasing, thereby pushing the converter to achieve high efficiency and high power density. This paper presents an asymmetrical half-bridge flyback converter for data center applications. Compared with an active clamp flyback converter, it functions as an isolated buck converter, and is more preferable for voltage step-down applications. The operating principle and the design considerations are included in this paper. An interleaving winding layout with uniformed current distributions is used for the planar transformer design. The built prototype satisfies an industrial standard low-profile sixteenth brick requirement, and achieves 94.9% peak efficiency and 468W/inch^3 power density.**

Keywords—asymmetrical half-bridge flyback converter, active clamp flyback converter, planar transformer

I. INTRODUCTION

The ever-growing demand for cloud computing and data processing has consumed significant electric power in 2020, and is expected to continue increasing in the coming future, thereby pushing power converters to be more efficient and compact. The 48V bus distribution system proposed by Google has been gradually adopted to replace the conventional 12V bus. This architecture improves the system efficiency. However, it also poses a challenge to converters' design.

The standard brick size is normally required in the industry. Conventional two-stage structures or converters with multi-stages are proposed and analyzed in many excellent papers. It is known to all that the efficiency of the two-stage converter is the product of the front stage and second stage, which also poses a penalty on system efficiency [1]-[3]. Converters with multi-stages have more functions than single-stage converters. Literature [4] proposes a sigma converter to transfer the majority of the input power through the LLC resonant converter as a DC transformer, while a small portion of power is regulated by the PWM converter to regulate the output. It improves the system efficiency by using the concept of partial power regulation. Another architecture with the functionality of the partial power regulation is proposed in [5]. Two LLCs are integrated into one magnetic core to improve the power density. However, these structures require many power devices or magnetic components, which are hard to realize the power density requirement.

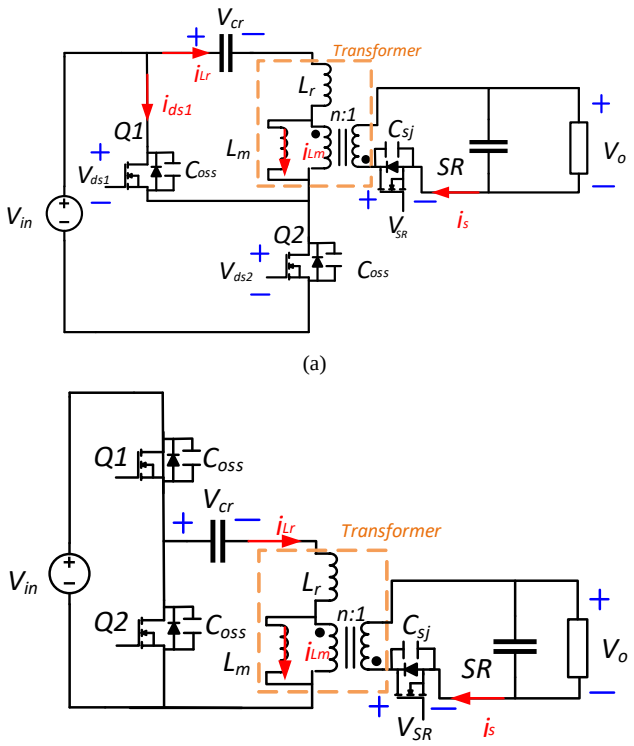
This brings one to re-investigate the single-stage solutions. Switch-capacitor converters [6]-[8] are capable to achieve a significantly high efficiency within a tiny volume. However, gate driver circuits tend to be more complex when there are more power stages. Additionally, these converters are hard to regulate the output voltage and not isolated. A single LLC resonant converter with regulation capability demands a large resonant inductor, which increases the system volume. When the switching frequency swings away from the resonant frequency, the power losses greatly increase due to the circulating energy [9]-[11]. Conventional half-bridge converters and forward converters are usually used to achieve both the efficiency and the power density requirements.

This paper looks into the asymmetrical half-bridge(AHB) flyback converter. It functions as an isolated buck converter and is therefore preferable for voltage-step down applications. The operating principles and design considerations are presented in this paper. A larger resonant capacitor can reduce the primary and secondary RMS current, but increase the turn-off losses. Due to the high current at the secondary side, parallel conductors are used to share the high current. However, the current distributions are usually unbalanced. Three 4:1 interleaving winding layouts with primary conductors in series and secondary conductors in parallel are compared. The winding layout which has the minimum AC resistance is selected. Ansys 2D simulation shows that this winding layout has uniformly distributed current on parallel conductors. The built prototype shows better performance than the state-of-the-art. It achieves 94.9% peak efficiency and 468W/inch^3 power density.

The remainder of this paper is organized as follows: Section II presents the operating principles of the AHB flyback converter. Subsequently, design considerations are given in Section III. Section IV shows the experiment results. Section V concludes this paper.

II. OPERATING PRINCIPEL OF THE ASYMMETRICAL HALF-BRIDGE FLYBACK CONVERTER

Compared with an active clamp flyback (ACF) converter, the asymmetrical half-bridge (AHB) flyback converter is more preferable for voltage step-down applications. Two configurations of the AHB flyback converter are presented in Fig.1. TABLE I summarizes the voltage stress comparison between these two converters. All active components of the AHB flyback converter have smaller voltage stress compared with the ACF converter. Furthermore, from the voltage transfer ratio of V_o/V_{in}, the AHB flyback converter can be regarded as an isolated buck converter, while the ACF converter is an isolated buck-boost converter. Therefore, the former is more suitable for voltage step-down applications.



(a)

(b)

Fig.1. Two configurations of the AHB flyback converter

TABLE I
COMPARISON BETWEEN TRADITIONAL ACF AND AHB FLYBACK

	V_{ds1} or V_{ds2}	V_d	V_o/V_{in}
ACF	$V_{in}+nV_o$	$V_{in}/n+V_o$	$D/n(1-D)$
AHB flyback	V_{in}	V_{in}/n	D/n

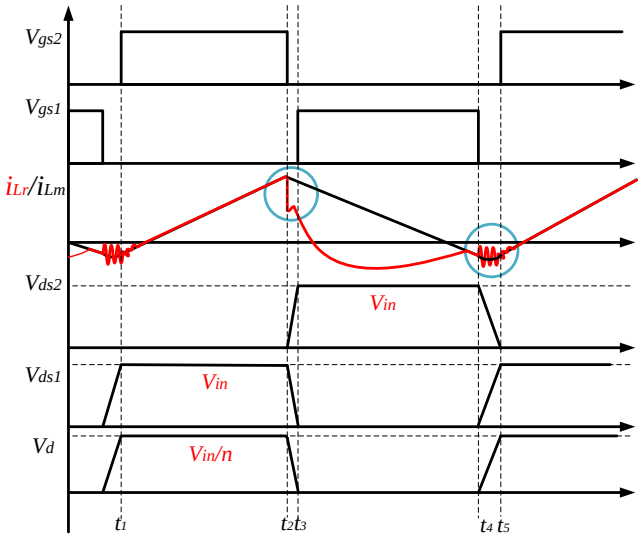


Fig.2. Operating waveforms of the circuit shown in Fig.1(a)

The operating principles of these two configurations are identical. Only the configuration shown in Fig.1(a) is analyzed. Fig.2 presents the main current and voltage waveforms of the circuit shown in Fig.1(a). The steady-state operating principles are given as follows:

Stage 1(t_0<t<t_1): At t_0, switch Q_2 turns on, and switch Q_1 is clamped by the input voltage V_{in}. The magnetizing current i_{Lm} and the resonant current i_{Lr} are increasing linearly and follow:

$$i_{Lm}(t)=i_{Lr}(t)=i_{Lr}(t_1)+\frac{V_{in}-V_{Cr}}{L_r+L_m}t \quad (1)$$

where L_r is the resonant inductor and L_m is the magnetizing inductor.

In this time interval, the secondary rectifier *SR* is blocked and the energy is stored in the transformer (or coupled inductor). The voltage applied to the primary winding V_p is

$$V_p=\frac{V_{in}-V_{Cr}}{L_r+L_m}L_m \quad (2)$$

Stage 2(t_2<t<t_3): There is a current dip on the resonant current during this ZVS transition where switch Q_2 is off. This phenomenon has been analyzed in [12], which is primarily due to the current shared by the primary and secondary parasitic capacitances, C_{oss} and C_{sj}. In this time interval, the resonant current discharges the output capacitance of switch Q_1 and charges the output capacitance of switch Q_2. *SR* is also discharging by the secondary current. This stage ends when switch Q_1 is fully discharged by the resonant current.

Stage 3 (t_3<t<t_4): Switch Q_1 achieves the ZVS turn on at t_3. Secondary rectifier *SR* starts to conduct. The resonant capacitor C_r and the resonant inductor L_r join in the resonance. The resonant current i_{Lr} satisfies:

$$i_{Lr}(t)=i_{Lr}(t_3)\cos(w_r t)+\frac{(nV_o-V_{Cr}(t_3))}{Z_r}\sin(w_r t) \quad (3)$$

where

$$w_r=1/\sqrt{L_r C_r},\ Z_r=\sqrt{\frac{L_r}{C_r}}$$

The voltage applied to the primary winding V_p is

$$V_p=-\frac{V_{Cr}}{L_r+L_m}L_m \quad (4)$$

Assume L_r<<L_m. The magnetizing inductor follows the voltage-second-balance, which is given by

$$D(V_{in}-V_{Cr})=V_{Cr}(1-D) \quad (5)$$

where D is the duty cycle of the switch Q_2. V_{cr} is the average voltage on the resonant capacitor. It can be solved by

$$V_{Cr}=V_{in}D \quad (6)$$

This time interval ends when switch Q_1 turns off.

Stage 4 (t_4<t<t_5): The current dip also occurs in this ZVS transition. Detailed analysis can be found in [12]. The resonant current discharges switch Q_2 and charges switch Q_1. *SR* is charging by the secondary current.

III. Converter Design

The design specification is presented in TABLE I. The input voltage changes from 32~75V and the nominal input is 48V. The leakage inductance of the transformer is utilized as the resonant inductance. The leakage inductance usually has limited energy to realize the ZVS for all devices. The converter is therefore designed to operate at discontinues conduction mode (DCM). The magnetizing current i_{Lm} joins in the charge and the discharge of the parasitic capacitances of all active devices. In this section, the design of circuit parameters for the AHB flyback converter will be introduced.

TABLE I
DESIGN SPECIFICATION

Symbol	Quantity	Value
V_{in}	Input voltage	32~75V
	Nominal input	48V
V_o	Output voltage	5V
P_o	Output power	100W

A. *Transformer*

Similar with an active clamp flyback converter, the AHB flyback converter can achieve higher efficiency with an interleaving winding layout. Fig.3 presents the current waveforms in the transformer, resonant current i_{Lr}, magnetizing current i_{Lm}, and secondary winding current i_s. It can be observed that there is negative conduction of the resonant current. This phenomenon can be explained by the current-second balance of the resonant capacitor C_r. The shaded area II is identical with the other shaded area I. The negative resonant current helps reduce the proximity effect, because i_{Lr} and i_s are in the opposite directions. The AC resistance can be therefore reduced by employing the interleaved winding layout.

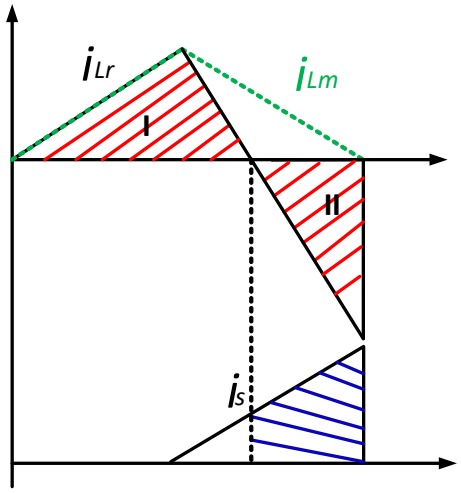


Fig.3. Currents waveforms in the transformer

This design deals with a high current at the secondary side. Parallel connections are necessary for secondary windings to share the high current. Three interleaving winding layouts with secondary conductors connected in parallel, shown in Fig.4, are analyzed and compared. TABLE II documents winding details. They are 4:1 planar windings with primary conductors in series and secondary conductors in parallel. The insulation thickness is assumed to be identical for each layer. AC resistances of these three cases simulated by Ansys 2D are presented in Fig.5. Case I and Case III cross each other at 830kHz. Case III has the smallest AC resistance when the frequency is below the crossing point, while Case I shows the minimum AC resistance when the frequency is higher than the crossing point. From this comparison, depending on the frequency, the optimal winding layouts can be selected accordingly.

TABLE II
WINDING DETAILES

Parameters	Values
Copper thickness (h)	70μm
Turn ratio (n:1)	4:1
Insulation thickness (t)	0.3mm
Window width (b)	5mm
Resistivity (ρ)	1.71×10^{-8} Ω·m
Air permeability(μ_o)	$4\pi \times 10^{-7}$ H/m
Magnetic core	E18/4/10
Relative permeability of the core(μ_c)	900

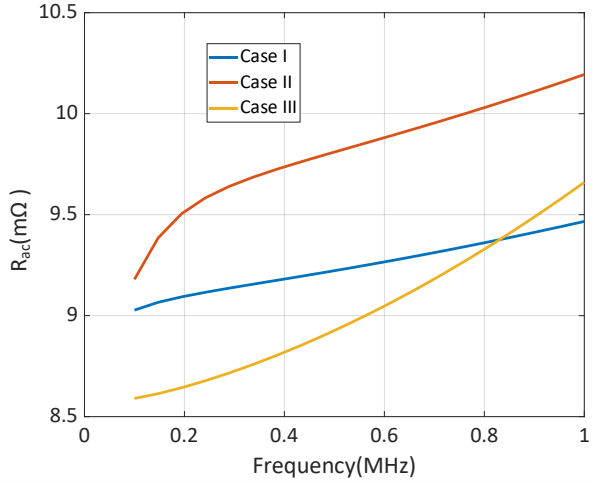
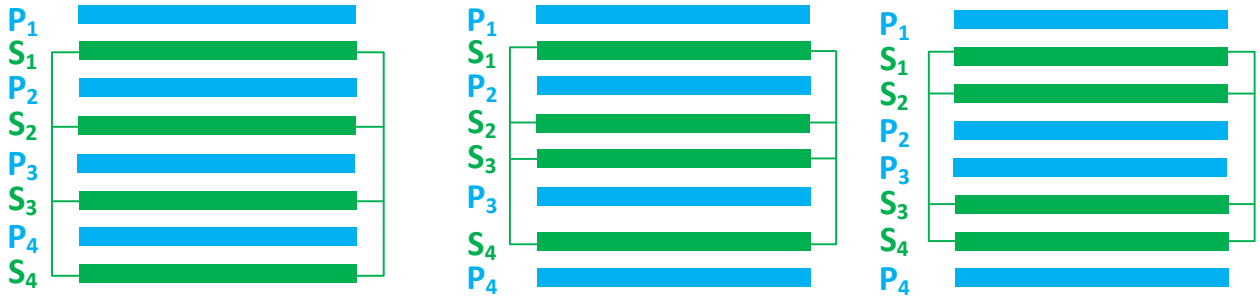
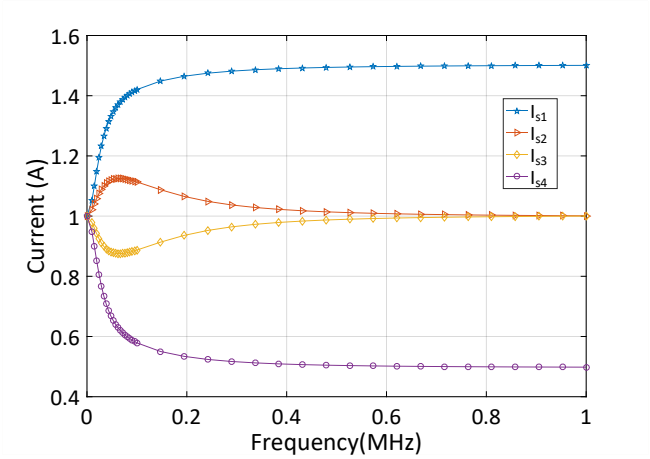


Fig.5. AC resistances of three winding layouts as functions of frequency



(a) Case I (b) Case II (c) Case III

Fig.4 Three winding parallel schemes of a turn ratio 4:1 planar windings with primary series connected and secondary layers parallel connected



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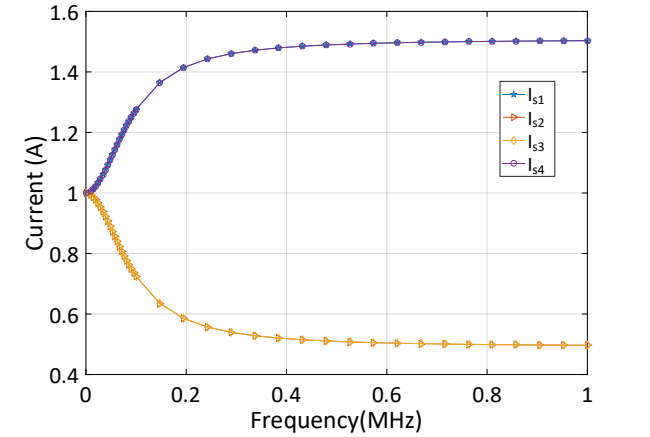

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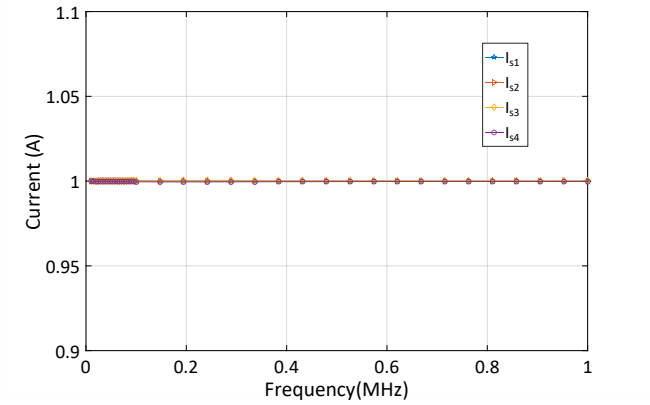


(c)

Fig.6. Secondary peak current on each conductor for (a) Case I, (b) Case II and (c) Case III. The frequency sweeps from 10kHz to 1MHz.

Current distributions of secondary conductors are analyzed by Ansys 2D. Each primary conductor is excited by 1A peak sinusoidal current. The secondary peak current on each conductor is measured and shown in Fig.6. It can be seen that each conductor in Case III has the same current across the whole swept frequency from 10kHz to 1MHz. This winding layout has uniformly distributed current, which the others have unbalanced current distributions. In this design, the switching frequency is below 830kHz. The winding layout shown in Case III is therefore selected for the transformer design.

B. *Magnetizing inductance*

To realize the ZVS for all active devices, the magnetizing inductance should be carefully designed. According to the charge balance during the ZVS transition, it satisfies

$$I_{Lm\_\min} t_d = 2C_{oss} V_{in} + C_{ps} V_{in} \tag{7}$$

Where I_{Lm_min} is the minimum magnetizing current. It is given by

$$I_{Lm\_min} = I_{Lm\_avg} - \frac{nV_o(1-D)(T_s - t_d)}{2L_m} \tag{8}$$

$$I_{Lm\_avg} = I_{Lr\_avg} + I_{s\_avg} = \frac{I_o}{n} \tag{9}$$

I_{Lm_avg} is the average current of the magnetizing current. It is the sum of the I_{Lr_avg} and I_{s_avg}, which are the average i_{Lr} and i_s, respectively. The average i_{Lr} is zero because of the currentsecond balance of C_r. I_{Lm_avg} is therefore equivalent to the referred secondary average current I_{s_avg}. Combining (7), (8), and (9), the magnetizing inductance L_m can be solved by

$$L_m = \frac{n^2 V_o (1-D)(T_s - t_d) t_d}{(4nC_{oss} + 2C_{ps}) V_{in} + 2I_o t_d} \tag{10}$$

C. *Resonant capacitor*

From Fig.7, a smaller resonant capacitor shows almost zero turn-off current for switch Q_1 and secondary rectifier *SR*, while a larger resonant capacitor presents a higher turn-off current. However, a larger resonant capacitor yields smaller primary and secondary RMS current, but higher turn-off loss, as presented in Fig.8. Thus, a trade-off has to be made between the turn-off loss and conduction loss. In this design, the AHB flyback converter is dealing with high current for both primary and secondary sides, where conduction power loss dominates. A larger resonant capacitor is therefore more preferable to reduce the conduction loss.

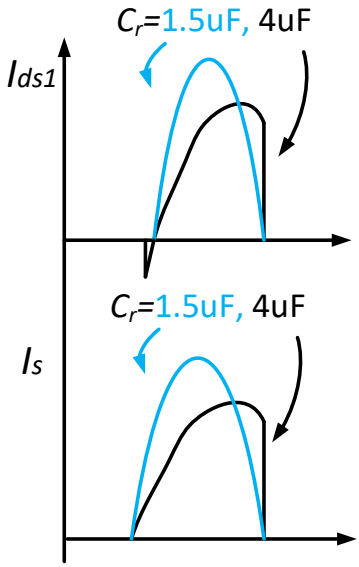


Fig.7. Current waveforms at different resonant capacitors. The switching frequency is 290kHz, and the resonant inductance is 53nH

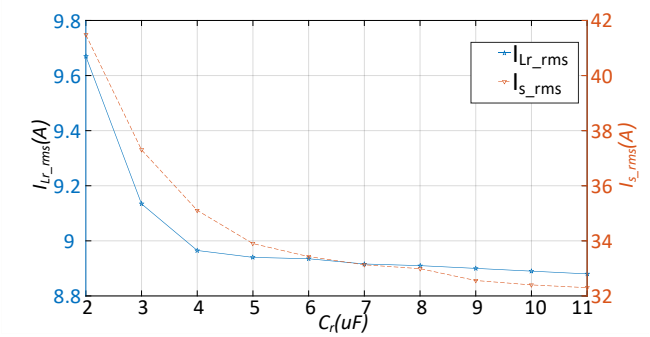


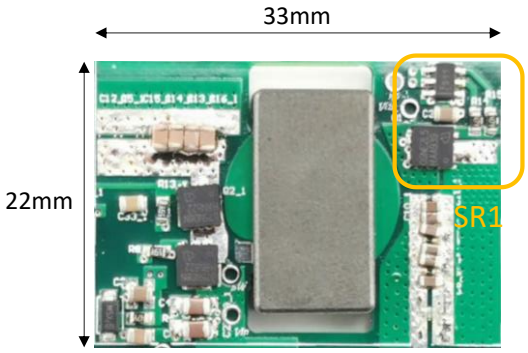
Fig.8. Primary and secondary RMS current as functions of the resonant capacitor C_r

IV. Experiment

The circuit parameters are documented in TABLE III. The magnetic core is ER 18/3.2/10 from Hitachi. A larger resonant capacitor is selected to reduce the primary and secondary RMS current. Fig.9 shows the top view and bottom view of the prototype. It satisfies the standard 1/16 brick size and achieves the power density of 468W/inch^3. Two *SRs* are connected in parallel to share the high current. As mentioned in the previous section, the winding layout show in Case III, an 8-layer PCB, is selected for the planar transformer design. However, this prototype is only built with two 4-layer PCBs to reduce the cost. The detailed configuration is shown in Fig.10. One *SR* is placed on the PCB together with other primary devices. The other *SR* is located on the other PCB which only has planar windings and gate drivers. These two PCBs are soldered together to have the parallel connections of the secondary windings, *SRs* and the series connections of the primary windings. Although the spacing between PCB1 and PCB2 is normally larger than the insulation between each conduction, it does not affect the parallel current distribution.

TABLE III
CIRCUIT PARAMETERS

Circuit parameters	Value
Q_1~Q_2	BSZ075N08NS5
SR	BSC009NE2LS5
Magnetizing inductance L_m	2.2uH
Leakage inductance L_r	53nH
Resonant capacitance C_r	3.3uF
Turn ratio	4:1
Magnetic core	ER18/3.2/10 ML91S



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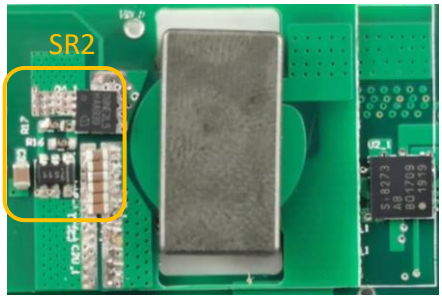


(b)

Fig.9. Top view and bottom view of the prototype

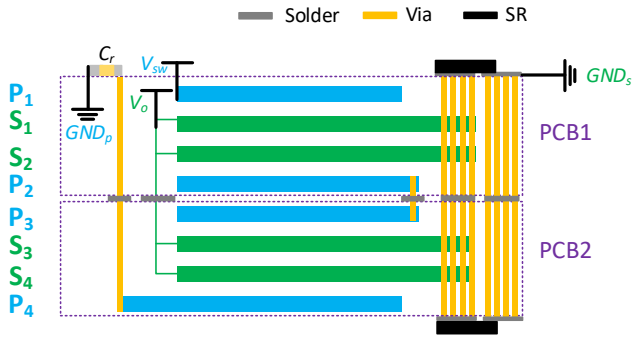
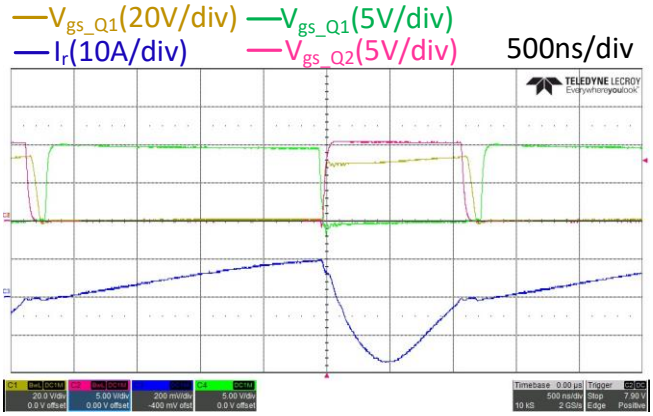


Fig.10. Planar windings configuration

Fig.11 shows experiment waveforms at full load. ZVS is realized at different input voltages. Fig.12 presents efficiency curves. The peak efficiency of 94.9% is realized at 36V. At the nominal input 48V, the peak efficiency is 94.8% at 60W. The efficiency drops to 92.7% at 100W. At 75V, the peak efficiency is 93.3%.



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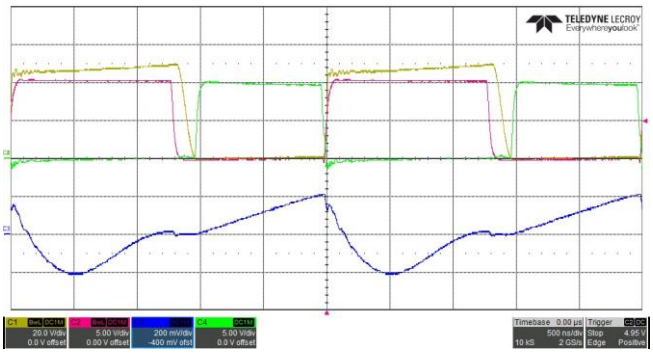

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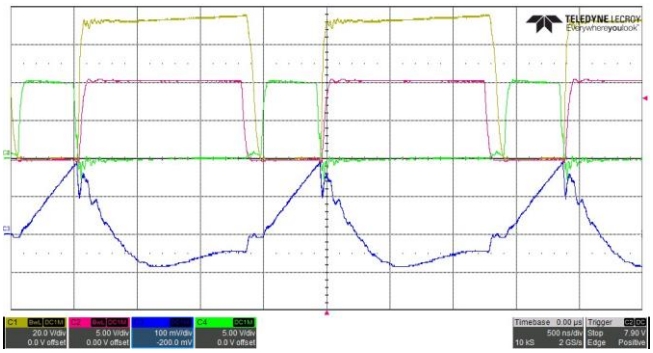

(c)

Fig.11. Experiment waveforms at (a) 36V, (b) 48V and (c) 75V full load

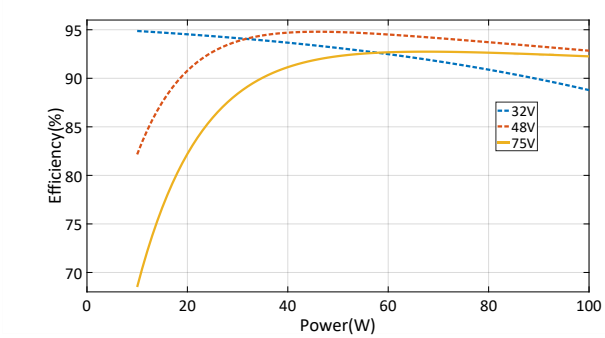

Fig.12. Efficiency curves at 32V, 48V and 75V

The comparison with the state-of-the-art is presented in TABLE IV. The built prototype achieves both the highest efficiency and power density.

TABLE IV
COMPARISON WITH THE STATE-OF-THE-ART

	Input	Output	Peak efficiency	Power density (W/inch3)
V48SC05020	36-75V	5V/20A	91%	229
MYBEB00520AZT	36-75V	5V/20A	93% at V_{in}=48V	136
PKU4105CPI	36-75V	5V/20A	93.6% at V_{in}=48V	256
AHB flyback	32-75V	5V/20A	94.8% at V_{in}=48V	468

V. Conclusion

This paper presents the operating principle and design considerations of the asymmetrical half-bridge (AHB) flyback converter. The impact of the resonant capacitor is analyzed. A larger resonant capacitor tends to induce larger turn-off losses but lower primary and secondary RMS current. This converter also benefits from the interleaving winding layout. A 4:1 interleaving winding structure with balanced current distributions on secondary parallel conductors is selected. The prototype achieves 94.9% peak efficiency and 468W/inch^3 power density.

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