Grid-Forming Converter with Improved Dynamic and Disturbance Rejection Capability

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***Abstract*— This paper proposes a control strategy for grid-forming converter based on a cascaded control scheme with current and voltage controllers. The theoretical analysis demonstrates the possibility of obtaining almost zero steady-state error for the current loop utilizing only a proportional controller with a magnitude and lead compensation functions to achieve high bandwidth. For the voltage loop, a disturbance input decoupling function is proposed to obtain better dynamic response for the converter under load changes. Simulations results prove the effectiveness of the proposed strategy.**

Keywords*— *grid-forming converter, cascade control, lead compensation, disturbance input decoupling.

I. INTRODUCTION

The increasing penetration of renewable energy sources (RESs) in the current energy matrix brings several advantages to the electrical grid, including distributed energy generation where its application may improve reliability and stability of the local electrical grid, in addition to providing benefits to suppliers with the system losses reduction along long transmission lines and the decrease in total investments required to create a new transmission line due to increased energy consumption [1]. Another advantage of using RESs is the reduction in dependence on energy based on fossil resources, which is directly linked to the reduction in greenhouse gas emission, and its inherent limited and exhaustible access [2].

The increasing penetration of RESs, mainly photovoltaic and wind power plants, alongside with energy storage systems (ESSs) is reshaping the traditional power systems into one with an increasing presence of electronic power converters (EPCs) (which aims to make the interface between the RESs and the electrical grid), which poses major operational challenges to utility system operators [3]. Usually, the integration of these RES with EPCs results in converters operating as grid-following converters (GFLC), where their control strategy is generally set to operate at rated output power and to inject it in an energized grid. Normally a power loop is used to control active and reactive power (*P* and *Q)* and to generate the current references for the current control loop, which can use Proportional+Integral (*PI*) controller in synchronous reference frame or Proportional+Resonant (*PR*) controller in stationary reference frame. The GFLC must be perfectly synchronized with the ac voltage at the connection point, also known as point of common coupling (PCC), to regulate the active and reactive power injected into the grid [4].

In case of load variation, for example, GFLC only maintain the current regulated and cannot directly provide frequency and voltage regulation for the electrical grid, since this converter relies on an external voltage source to provide the voltage and frequency references [5]. Aiming to improve the integration of RESs and EPCs, the grid-forming converters (GFMC) were developed, although its main idea had already been proposed many years ago, which consisted of regulating output voltage and frequency [2], [6].

The GFMC usually are interfaced through *LC* or *LCL* filters, with cascaded control loops, an inner current loop and an outer voltage one. The current loop aims to have fast dynamics to compensate for input and harmonic load disturbances, and the voltage loop generates the reference for the first one, as well as is responsible for controlling the output voltage even with the presence of load disturbances [7].

Several works have been developed aiming to improve the GFMC dynamic response, e.g. increase the bandwidth of the controller loops and improve the disturbance rejection capability of the converter. In [8], the authors propose a generic voltage controller with a high-pass filter in the current feedback loop and a simple P controller is used in the current loop. It is shown that the voltage controller has fast voltage tracking. In [9], the authors propose a voltage control strategy to improve the disturbance rejection capability during the parallel operation of a multimodular GFMC. They used a partial load current feedforward control technique in addition to a feedforward control strategy of a two-degrees-of-freedom (2-DOF) voltage controller, where the latter compensates the limitation of the former. In [10], the authors develop the discrete-time model of the LC filter considering the delay and zero-order hold (ZOH) effects, and from that, they could develop a current controller with high bandwidth from two different strategies, which allowed the increase of the voltage loop bandwidth.

Commonly in classical dual-loop AC-voltage control, the current loop is regulated through a *P* controller and the voltage

loop is regulated through *PI* or *PR* controller. However, almost zero steady-state error is not achievable when only *P* controller is used in the current loop, unless a controller with integral/resonant part is used, but an anti-windup algorithm must be also considered to avoid the problem of windup [11]. Furthermore, the insertion of resonant components makes the system more susceptible to instability.

Another problem related to the steady-state error is the current loop reference value limited by the saturation at the voltage loop output. If the error is large, saturation does not provide the desired effect since the real current value is below the reference one. Therefore, it is interesting to obtain approximately zero steady-state error in the internal current loop even with a proportional controller.

To overcome the limitation presented previously, this paper proposes a control strategy so that the current control loop has approximately zero steady-state error using only a simple *P* controller. The disturbance rejection capability of the voltage controller loop is also improved from the disturbance input decoupling (DID).

This paper is divided as follows: Section II describes the system under study. In Section III the problem is addressed, focusing on the current controller design. Section IV presents a voltage controller design to improve the disturbance rejection capability. Simulation results are presented in Section V. And Section VI concludes this work

II. System Description

The topology of a GFMC for standalone application with *LC* filter and inner loops (current and voltage control) is shown in Fig. 1, where V_{dc} is the dc-link voltage (the control of this voltage is not being addressed in this paper, therefore it is assumed that its value is fixed), i_L is the inductor current, v_c is the capacitor voltage and i_o is the output current. A *LC* filter is used to generate regulated voltages at the output, where L_f, R_f and C_f are the inductor, the equivalent series resistance (ESR) of L_f and the capacitor, respectively. The capacitor voltages in αβ-axis frame $v_{c\alpha\beta}$ are controlled by a PR controller, $G_v(z)$, and the voltage reference is given by $v^*_{c\alpha\beta}$. The voltage control loop gives the current reference $i^*_{L\alpha\beta}$ to the P controller ($G_i(z)$) which controls the inductor current $i_{L\alpha\beta}$ in αβ-axis frame. The $\widehat{K}$ parameter is the compensation term to reduce the steady-state error in the current loop. The output current in αβ-axis frame $i_{o\alpha\beta}$ is fed back through the transfer function $G_{DID}(z)$ to improve the disturbance rejection capability of the GFMC. The $G_{dec}(z)$ transfer function is responsible for decouple the capacitor voltage state coupling $v_{c\alpha\beta}$, and will not be detailed in this work, since its function has already been highly discussed in [12].

The closed-loop system control block diagram of the GFMC under study is shown in Fig. 2. The system parameters shown in Fig. 1 are listed in TABLE I. The next section will address the problem related to the non-zero steady state in the current control loop when using *P* controller and how to mitigate it.

III. Current Controller Design

Assuming that the capacitor voltage state coupling was correctly decoupled by $G_{dec}(z)$, the simplified block diagram for the current control loop considering a *P* controller is shown in Fig. 3. The controller was tuned for a bandwidth of 1 kHz, which results in a gain $R_a = 7.84$.

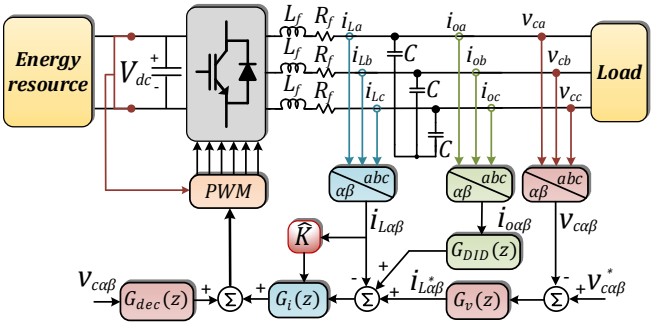

Fig. 1. Grid forming converter with LC filter and multi-loops control.

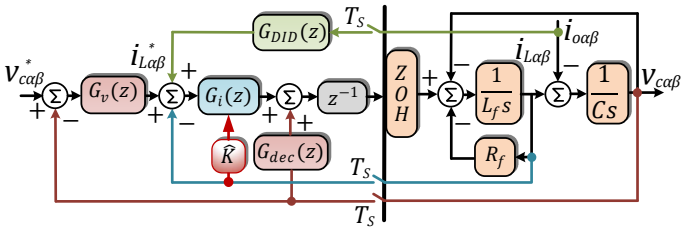

Fig. 2. Closed-loop system control block diagram of the GFMC.

TABLE I. System Parameters

Parameter	Value
Inductor (L_f)	2 mH
Capacitor (C)	30 μF
ESR (R_f)	0.1 Ω
Load (R_l)	15 Ω
Sampling period (T_s)	100 μs

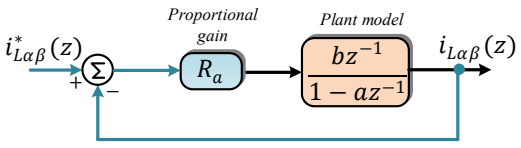

Fig. 3. Closed-loop block diagram for the current loop.

The parameters *b* and *a* are given by (1) and (2), being $\omega_n = 1/\sqrt{L_f C}$, $\xi = R_f/2\omega_n L_f$, $\omega_d = \omega_n\sqrt{1-\xi^2}$ and $\phi = tg^{-1}\left(\sqrt{1-\xi^2}/\xi\right)$.

$$b = C\frac{{\omega_n}^2}{\omega_d}e^{-\xi\omega_n T_s}\sin(\omega_d T_s) \quad (1)$$

$$a = -\frac{\omega_n}{\omega_d}e^{-\xi\omega_n T_s}\sin(\omega_d T_s - \phi) \quad (2)$$

The Fig. 4 shows the closed-loop frequency-response for the system in Fig. 3.

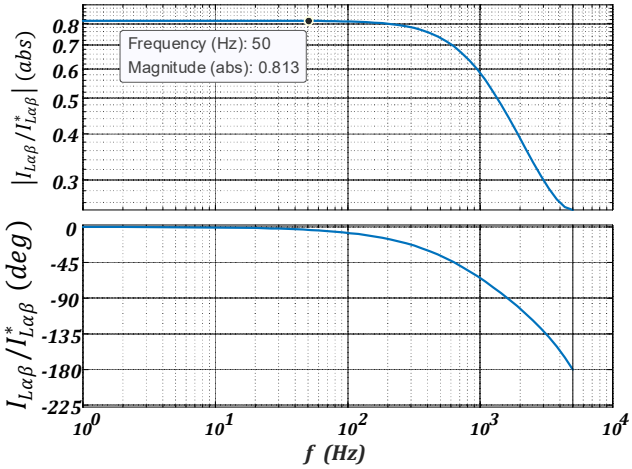

Fig. 4. Frequency-response for the closed-loop current controller with *P* controller and lead compensation.

As can be seen in Fig. 4, there is a magnitude error at steady-state for the fundamental frequency (50 *Hz*), therefore, the following subtopics will cover ways to solve this issue.

A. Magnitude Compensator Design without delay

Initially, the system shown in Fig. 5 is considered, where the computation delay is not considered. The compensation constant $(\hat{K})$ is included to reduce the steady-state error.

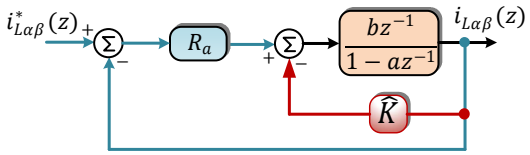

Fig. 5. Closed-loop block diagram with P controller and ideal decoupling.

It is desired to design a compensation and a *P* controller such that the steady-state error is zero.

The closed-loop transfer function is given by (3):

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-1}}{1-\left(a-\hat{K}b-R_a b\right)z^{-1}} \tag{3}$$

For this transfer function to present zero steady-state error at 0 Hz, its value must be $i_{L\alpha\beta}(z)/i^*_{L\alpha\beta}(z) = 1$ when $z^{-1} \to 1$. Replacing $z^{-1} = 1$ in (3), we have (4).

$$1 = \frac{R_a b}{1-\left(a-\hat{K}b-R_a b\right)} \tag{4}$$

After some mathematical manipulations, $\hat{K}$ can be defined as (5).

$$\hat{K} = \frac{a-1}{b} \tag{5}$$

Substituting (5) in (3), yields to (6):

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-1}}{1-(1-R_a b)z^{-1}} \tag{6}$$

The value of the controller gain so that the pole is at a desired location $e^{-2\pi p_d T_s}$, being p_d the bandwidth of the controller, is calculated by (7).

$$R_a = \frac{1-e^{-2\pi p_d T_s}}{b} \tag{7}$$

B. Magnitude Compensator Design with a P controller and the computational delay

However, in digital-controlled systems, the delay due to the computational processing must be considered, as this directly affects the performance of the controllers. Fig. 6 shows the block diagram for the system presented previously, but this time considering the delay of z^{-1}.

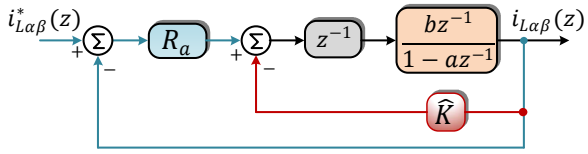

Fig. 6. Closed-loop block diagram with *P* controller and computational delay.

The closed-loop transfer function is given by (8).

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-2}}{1-az^{-1}+b\left(\hat{K}+R_a\right)z^{-2}} \tag{8}$$

For this transfer function to present zero steady-state errors, its value must be $i_{L\alpha\beta}(z)/i^*_{L\alpha\beta}(z) = 1$ when $z^{-1} \to 1$. It is observed that the value of $\hat{K}$ has the same form as in (5). Substituting (5) in (8), yields to (9).

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-2}}{1-az^{-1}+(a-1+R_a b)z^{-2}} \tag{9}$$

If the desired pole locations are at the specified positions p_1 and p_2, the denominator of the closed-loop transfer function must be equated to $(z-p_1)(z-p_2)$. However, for this case is not possible to analytically design the desired location of the pair of poles. Furthermore, if it is desired to increase the bandwidth of the current controller, the phase margin decreases due to the computation delay. One possible solution is to add a lead compensation in series with a *P* gain [10].

C. Magnitude Compensator Design with a P controller with lead compensation

Fig. 7 shows the current loop block diagram with a lead and magnitude compensators. One more degree of freedom for design is added with this lead compensation, as well as it is possible to increase the bandwidth of the current controller. There are two possibilities to insert the magnitude compensator term ($\hat{K}$), after or before the lead compensation as shown in Fig. 7 (a) and Fig. 7 (b), respectively. The analyse will be developed for both cases, starting with the decoupling after the lead compensation.

The closed-loop transfer function of the block diagram in Fig. 7 (a) is given by (10).

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-2}}{(1+k_L z^{-1})\left(1-az^{-1}+\widehat{K}bz^{-2}\right)+R_a b z^{-2}} \quad (10)$$

The value of $\widehat{K}$ that implies (10) having zero steady-state error is the same for the previous cases, and substituting it in (10) yields to (11).

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-2}}{1+(k_L-a)z^{-1}+(a-1-ak_L+R_a b)z^{-2}+k_L(a-1)z^{-3}} \quad (11)$$

As can be seen in (11), the transfer function is 3rd order and it is difficult to design pole placement, since there are three poles and two degrees of freedom in the controller, R_a and k_L.

Considering the system in Fig. 7 (b), where the magnitude compensator is implemented inside the controller (before the lead compensation), the closed-loop transfer function is given by (12).

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b z^{-2}}{1+(k_L-a)z^{-1}+\left(\widehat{K}b-k_L a+R_a b\right)z^{-2}} \quad (12)$$

For this transfer function to present zero steady-state error, its value must be $i_{L\alpha\beta}(z)/i^*_{L\alpha\beta}(z) = 1$ when $z^{-1} \to 1$.

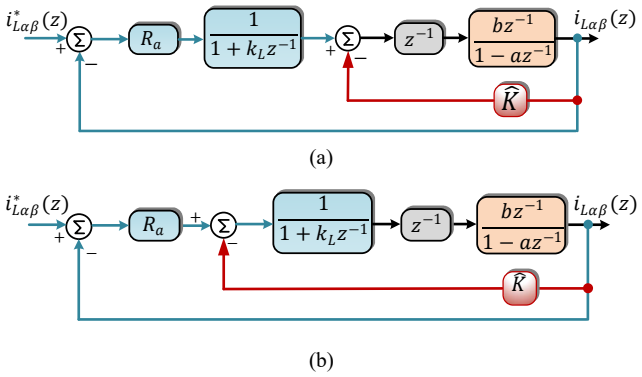

Fig. 7. Closed-loop block diagram with P controller and lead compensation for non-ideal decoupling – a) after the lead compensation b) before the lead compensation.

Therefore (12) can be rewritten as (13).

$$1 = \frac{R_a b}{1+k_L-a+\widehat{K}b-k_L a+R_a b} \to \to \widehat{K} = \frac{(a-1)k_L+a-1}{b} \quad (13)$$

Substituting this value of $\widehat{K}$ into (12) yields to (14).

$$\frac{i_{L\alpha\beta}(z)}{i^*_{L\alpha\beta}(z)} = \frac{R_a b}{1+(k_L-a)z^{-1}+(a-k_L-1+R_a b)z^{-2}} \quad (14)$$

The poles of (14) must satisfy the following relationship: $z^2-(p_1+p_2)z+p_1p_2 = z^2+(k_L-a)z+a-k_L-1+R_a b$, where p_1 and p_2 are the poles to be allocated. Since there are two parameters, the system of equations can be solved, and the gains k_L and R_a are given by (15) and (16), respectively.

$$k_L = a-(p_1+p_2) \quad (15)$$

$$R_a = (p_1p_2-a+k_L+1)/b \quad (16)$$

The equation of the pair of poles p_1 and p_2 can be obtained with more details in [10].

Fig. 8 shows the frequency-response for the system in (14), where the current controller was tuned for a bandwidth of 3 *kHz*, being $R_a = 13.58$, $k_L = 0.5$ and $\widehat{K} = -2.69$.

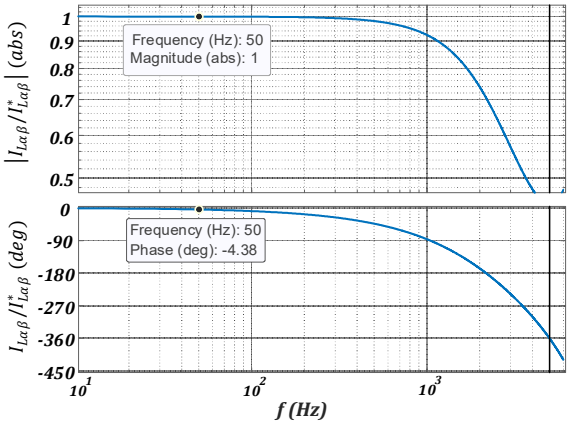

Fig. 8. Frequency-response for the closed-loop current controller with a *P* controller and magnitude compensator before the lead compensation.

As can be seen in Fig. 8, there is no error for the current magnitude value and a small phase shift is obtained at the fundamental frequency, with the proposed magnitude compensator for the current control using only a *P* controller and lead compensation

IV. Voltage Controller Design

To regulate the capacitor voltage value, it was used a *PR* controller. The voltage controller bandwidth was set to 300 *Hz* and the proportional gain was obtained using root locus method. The proportional gain to achieve this bandwidth is $K_{pv} = 0.06$. The resonant gain K_{iv} is chosen following the rule presented in (17), and the set value is $K_{iv} = 37.7$. Being ω_1 the fundamental frequency in *rad/s* [7].

$$K_{iv} \geq 2K_{pv}\omega_1 \quad (17)$$

A. Disturbance input decoupling design

The strategy to improve the disturbance rejection of the GFMC is to use disturbance input decoupling (DID) [13], [14]. Fig. 9 shows how the DID is implemented. It is necessary to measure the disturbance, which in this case is the converter output current, and fed back to the controller to decouple it. The principle to design the transfer function $G_{DID}(z)$ is to cancel, at the output, the effect of the disturbance at the sampling instants. To simplify the design the current loop was approximated by an equivalent first order system with the same bandwidth of the real system, being $\omega_i = 2\pi 3000$ *rad/s*.

The transfer function $G_{DID}(z)$ can be obtained from (18), and δ_z, δ_p and K_{DID} are given by (19)-(21), respectively. The obtained values were $\delta_z = 0.1425, \delta_p = -0.5316$ *and* $K_{DID} = 1.7863$.

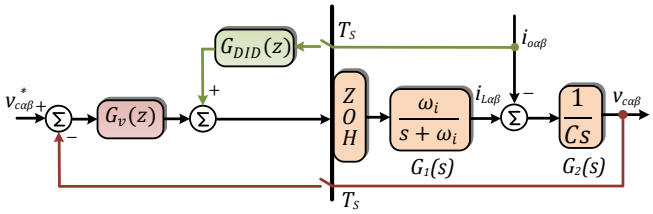

Fig. 9. Closed-loop block diagram to analyse the use of DID.

$$G_{DID}(z) = \frac{Z[ZOH\ G_2(s)]}{Z[ZOH\ G_1(s)G_2(s)]} = K_{DID}\frac{z-\delta_z}{z-\delta_p} \quad (18)$$

$$\delta_z = e^{-T_S\omega_i} \quad (19)$$

$$\delta_p = \left[T_s\delta_z - \frac{1}{\omega_i}*(1-\delta_z)\right] \Big/ \left[T_s - \frac{1}{\omega_i}*(1-\delta_z)\right] \quad (20)$$

$$K_{DID} = T_s \Big/ \left[T_s - \frac{1}{\omega_i}*(1-\delta_z)\right] \quad (21)$$

V. Simulation Results

This section is divided into two parts: the first part will evaluate the current controller performance to verify the developed theoretical analysis, and the second one will evaluate the voltage controller to show the dynamic improvement obtained with the use of DID in face of disturbances. For validating the theoretical analysis, simulations were realized utilizing Simulink. The parameters given in TABLE I are used.

A. Current controller performance

Fig. 10 shows a step response for α-axis current reference $i^*_{L\alpha}$ equal to 1 A peak. The inductor current $i_{L\alpha}$ tracked the reference command correctly and can be seen that the error is almost zero, confirming the theoretical analysis developed.

B. Voltage controller performance

Fig. 11 shows the α-axis capacitor voltage response and voltage error upon a change load at $t = 0.1\ s$ from 15 Ω to 40 Ω with (W/) and without (W/O) DID. It can be noted that in both strategies the controller regulated the voltage correctly, however the strategy with DID had better disturbance rejection response, with less voltage swell, as well as shorter settling time.

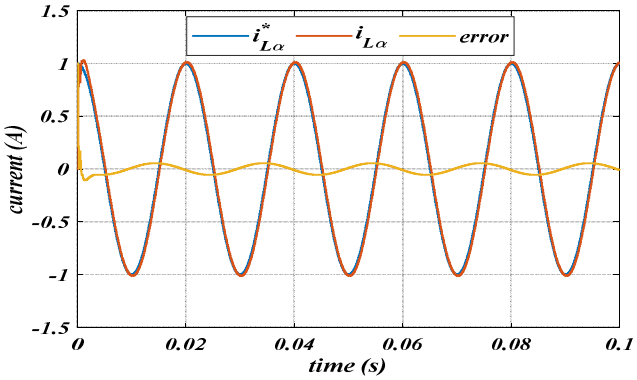

Fig. 10. Step response of the α-axis current using P controller and non-ideal decoupling before the lead-compensation.

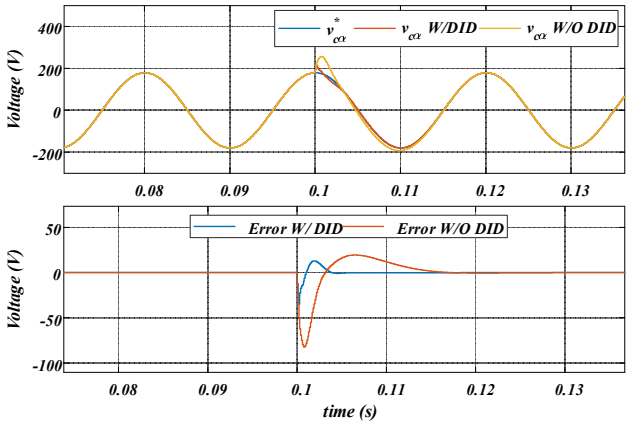

Fig. 11. Capacitor voltage and error signal with and without the use of DID.

VI. Conclusion

This paper presented a control strategy for GFMC, based on a simple *P* control for the current loop, in which it was possible to obtain almost zero steady-state error and high bandwidth using a magnitude compensation function together with a lead compensation. It was also used a disturbance input decoupling function for the voltage controller, which allowed better disturbance rejection response for the converter upon output disturbances.

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