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Packaging of Photodetector Modules for 100 Gbit/s Applications Using Electromagnetic Simulations

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***Abstract*— In this paper we demonstrate ultra-broadband packaging and interconnection designs for photodetector (PD) modules for 100 Gbit/s data transmission applications. The design of packaging and interconnection structures is based on accurate and reliable 3D electromagnetic (EM) simulations. Mode conversion loss due to mode mismatch is identified as the dominant effect of limiting bandwidth of packaged modules. Finally, PD chips are successfully packaged by using wire-bonding technology and conventional coplanar waveguide (CPW) for avoiding mode mismatch. The new packaged PD module demonstrates approximately 100 GHz 3 dB bandwidth.**

I. Introduction

With the booming of large volume and high speed data transmission requirements, the operation frequencies of integrated circuits enter the millimeter-wave domain. Millimeter-wave monolithic integrated circuits (mm-wave MMICs), such as mixers [1] and LNAs [2] operating above 200 GHz, and optoelectronic integrated circuits (OEIC), such as photodetector (PD) chips with more than 100 GHz bandwidth [3], have been recently developed and reported. Passive packaging and interconnection structures, however, may distort the high frequency signals due to high losses, multimode propagations and resonances. Therefore, successful design of packaging and interconnection in the millimeter-wave frequency range is crucial for maintaining the performance of entire high-speed systems.

Fig. 1 shows the relative electro-optical (O/E) response of a packaged PD module. The relative response is a normalized O/E conversion characteristic of an optoelectronic component. The 3dB bandwidth of the packaged PD module is 80 GHz, and the loss of the module is more than 5 dB beyond 90 GHz. Narrow bandwidth and high loss due to the packaging structure will seriously degrade the performance of high-speed data transmission systems. The packaging of such high speed components is very challenging when aiming at more than 100 GHz bandwidth, especially due to the multi-chip module (MCM) structure involving several chip-to-chip and/or chip-to-substrate transitions. We have previously investigated and optimized the transition from the conductor-backed coplanar waveguide (CBCPW) to the coaxial connector using accurate full-wave electromagnetic (EM) simulation methods [4], [5].

In this paper, general chip-to-chip transitions are first investigated using reliable EM simulations [6]. Afterwards, we demonstrate that PD chips can be modeled at a behavioral level in a 3D EM frequency domain simulator. An EM model

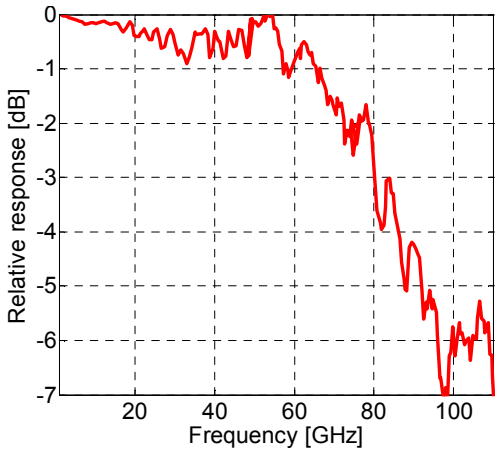

Fig. 1 Measured relative response of a packaged photodetector module.

of the packaged PD module based on the chip model is also presented. The major loss mechanism in the packaging structure is revealed in the simulation results. The new packaging design is proposed for wider bandwidth and lower loss. The packaging design is finally verified by measurement results.

II. 3D Electromagnetic Simulations

Accurate 3D EM simulation is a powerful tool for analyzing complicated packaging and interconnection problems. S-parameters and EM field distribution can be directly obtained from simulation results as a guidance of optimizing and designing passive structures. The accuracy and reliability of EM simulations strongly depends on how well the excitation schemes correlate with the physical setup. Wave port excitations are usually considered to be an efficient way to excite the structure under investigation. However, the boundary conditions of wave ports may introduce unexpected artificial effects [6], especially in the case of planar structures such as coplanar waveguide (CPW). As shown in the inset of Fig. 2, our novel structure models the ground-signal-ground (GSG) probe in on-wafer measurement setups for exciting planar structures. The drawback associated with wave ports is avoided in this way, and the accuracy and reliability of the simulation results are improved [6]. Furthermore, this

excitation scheme enables to retrieve the actual position of the wafer probes during actual measurements.

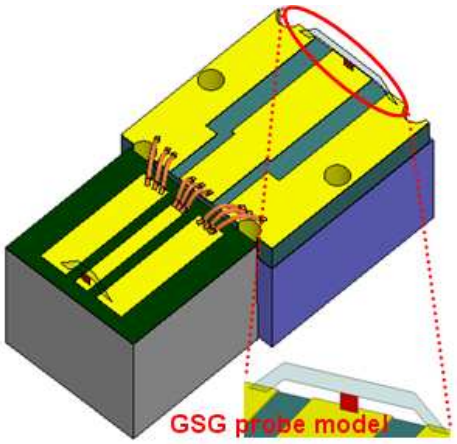

Fig. 2 An EM model of a CPW-CBCPW wire-bonding transition; the excitation structure is enlarged as an inset.

A. Chip-to-Chip Interconnections

Since output pads of MMICs and OEICs, such as the PD chip of interests, are normally CPW structures and CPW/CBCPW are widely used as on-chip interconnection due to their low dispersive and easy grounding merits, chip-to-chip and chip-to-substrate transitions can be generalized as CPW-CBCPW and CPW-CPW transitions. Fig.2 shows a typical CPW-CBCPW transition utilizing wire-bonding technology. The support below the CBCPW is in general chosen to adjust the height of the two chips. Several via holes are drilled in the CBCPW to suppress unwanted multimode propagation and resonances. The EM model of bonding wires resembles the real case. The insertion losses of the CPW-CBCPW transitions with different supportive bricks are shown in Fig. 3 (red curves). Resonances exist in low frequency range, and fast attenuation of the insertion losses starts from 60 GHz. In the EM model of the transition, all the dielectric materials are lossless and only conductive loss of the metal is included in simulations. Both CBCPW and CPW are low loss structures and have 50 Ω characteristic impedance. Therefore, the dominant attenuation contribution must come from the wire-bonding transition.

Fig. 4 shows the electric field pattern at the gap between the CBCPW and CPW at 100 GHz, when the supportive brick is metallic. The pattern is neither CPW mode nor CBCPW mode. The strongest part of the E-field directly faces the metallic brick. A significant part of the EM power does not propagate from one chip to another but leaks into the gap. The leakage power radiates in free space or reflects back to the CPW. If the supportive brick is dielectric, the resonance and fast attenuation is alleviated but still serious. Conclusively, the insertion loss in the transition is dominantly caused by the mode conversion from CPW mode to CBCPW mode and secondarily due to the metallic support. The mode mismatching effect is not significant in the low frequency range but leads to the observed problems in the high frequency range.

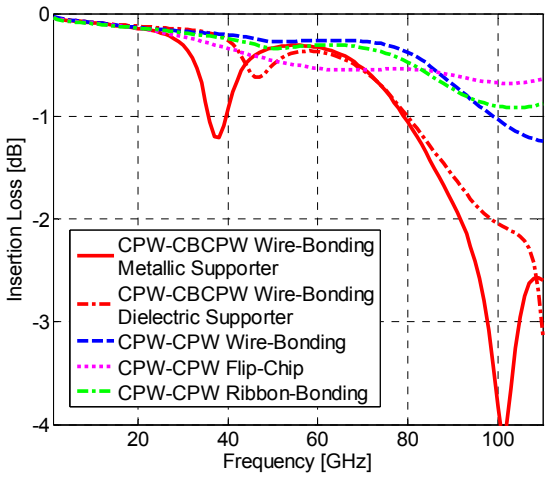

Fig. 3. Insertion losses of interconnections with different integration technologies.

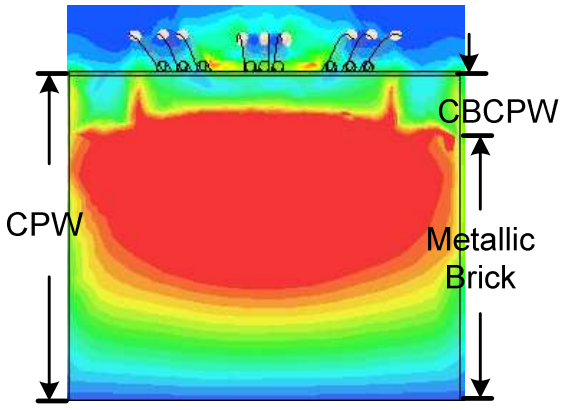

Fig. 4 Electric field pattern at the CPW-CBCPW transition with a metallic brick at 100 GHz.

A straightforward way to solve the problem is to avoid interconnecting two chips with much diverse substrate thicknesses. A CPW with 50 Ω characteristic impedance replaces the CBCPW and the metallic brick. The insertion loss of CPW-CPW wire-bonding transition is demonstrated in Fig. 3, where two chips have similar substrate thickness. A significant improvement of insertion losses is achieved over 60 GHz, and the resonances in low frequency range also disappear. The promising result shows that the CPW-CPW transition using wire-bonding only has 1 dB loss at 100 GHz. Two other technologies, flip-chip and ribbon-bonding, are also applied in CPW-CPW transitions. The insertion losses of the three interconnection technologies in Fig. 3 are comparable with each other. In details, wire-bonding has the lowest insertion loss below 85 GHz. This result clearly states that wire-bonding is an effective and low-cost interconnection technology for W-band applications.

B. PD chips

When chip-to-chip transitions are of interests, accurate EM models of active mm-wave MMICs and OEICs are of importance for packaging and interconnection investigation. Although full 3D EM modeling usually refers to passive

structures, this paper demonstrates that active devices such as PD chips can also be fully modelled in 3D EM simulators at a behavioral level.

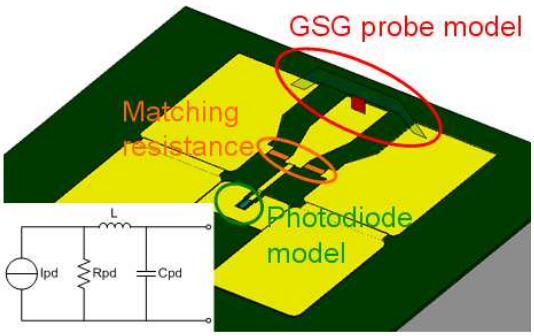

Fig. 5 A fully 3D electromagnetic model of the PD chip, the inset is the equivalent circuit model of the embedded photodiode.

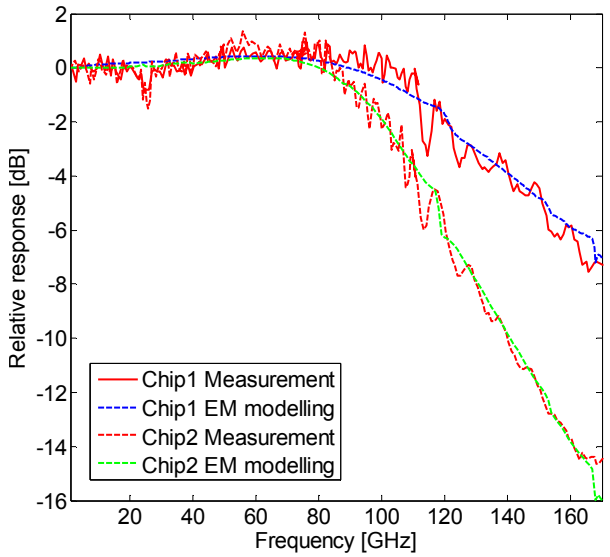

Fig. 6 Comparison between the measured and the modeled relative response of the PD chips with two different p-i-n junctions.

Fig. 5 shows an EM model of a PD chip with a typical on-wafer measurement setup. A GSG probe model is placed on the output CPW pad of the chip. In order to obtain an accurate simulated relative response of the chip model compared to the measured result, the parasitic elements of the excitation structure have to be removed by EM simulation calibration [6].

The bandwidth of PD chips is limited by the passive circuit network of chips and the transit-time effect of pin photodiodes [7]. The passive structures of the chip except the junction capacitance of the diode are accurately captured in 3D EM models such as CPW output pads, air-bridge structures, matching resistance and large DC block capacitors. The limitation by junction capacitance and transit-time effect is modeled by an embedded equivalent circuit in the EM model using lumped elements. The insert in Fig. 5 shows the schematic of the equivalent circuit. The photocurrent of the diode is modeled by a current source Ipd with a parallel resistor of the photodiode Rpd. Cpd is the junction capacitance and L is used to model the bandwidth limitation due to time-transit effects. The values of Cpd and L can be tuned to fit the relative responses of the models to the measurement results of various PD chips. Fig. 6 shows relative responses of two types of PD chips with different areas and thicknesses of the isolation layers of p-i-n junctions. The modeled relative responses perfectly fit the measurement results when the values of Cpd and L are properly assigned. Therefore, the EM model of PD chips is scalable to the dimension of the chips.

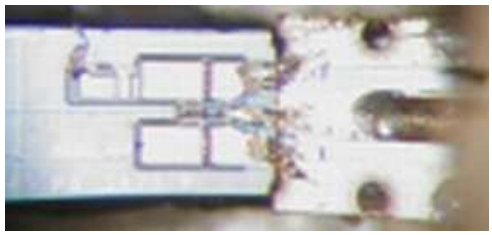

Fig. 7 Micro-photograph of the packaging of the original photodetector module as well as a PD chip.

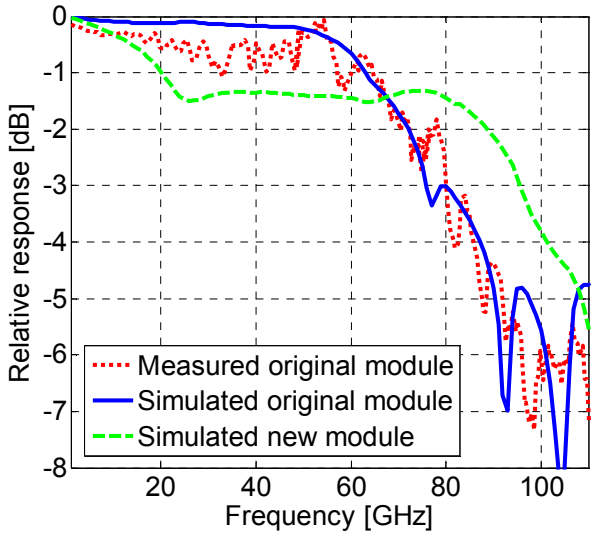

Fig. 8 Measured and simulated relative responses of the original PD module and new PD modules with thick CPW.

C. *Packaged PD Modules*

Fig. 7 shows the micro-photograph of the original packaged PD module. The module is analyzed by accurate EM simulations. The EM model of the module consists of a launch body of 1mm coaxial connector, a PD chip and a CBCPW bridging the connector to the PD. A metallic brick is selected to support the CBCPW to make the CBCPW be at the similar horizontal level as the PD chip. Two major transitions, coaxial connector to CBCPW transition and wire-bonding CPW-CBCPW transition from the CBCPW to the PD chip, are included in the model. The loss of the connector itself is added in the simulated relative response after EM simulations.

A very good agreement between measurement and the EM modeled relative responses of the original PD module is achieved as shown in Fig. 8. The fast attenuation beyond 60 GHz is associated with the chip-to-CBCPW transition, which

is similar to Fig. 2. The wire-bonding CPW-CBCPW transition from the PD chip to the CBCPW is identified as the dominant contribution to the fast attenuation. In the EM model of the new module, a CPW with a comparable height to the PD chip replaces the CBCPW and the metallic support, and the arrangement of bonding wires are optimized [8]. The mode conversion loss in the module packaging is eliminated by this solution as stated previously. The 3 dB bandwidth of the new module is about 95 GHz with improvement of approximately 15 GHz as compared to the original module.

III. Measurement Results

A PD module has been fabricated to verify the performance of the module utilizing the packaging structure with thick CPW. Measurement results in Fig. 9 show that the relative response of the new preliminary module becomes flat in the 60 GHz to 100 GHz range when a thick CPW is used. It proves the mode conversion loss from the PD chip to the CBCPW is completely eliminated in the new module. A remarkable improvement in relative response is achieved above 80 GHz, and the 3dB bandwidth is up to 100 GHz. The high loss in the low frequency range below 80 GHz can be improved by avoiding the impedance mismatch and inhomogeneous CPW substrate in the new packaging structure.

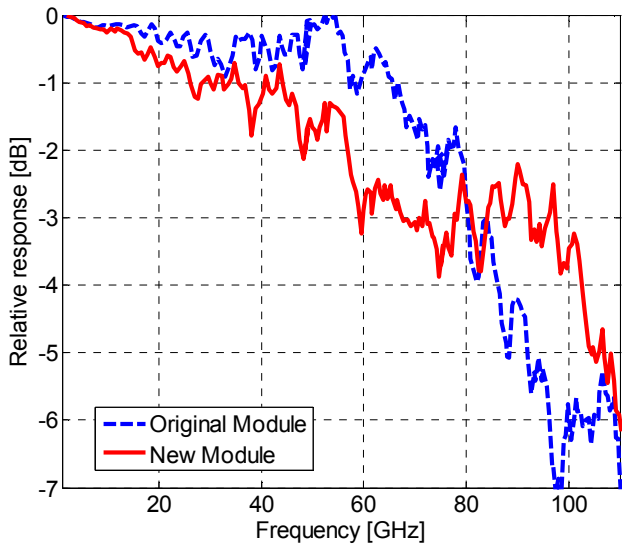

Fig. 9 Measured relative responses of the original module and the new preliminary module.

IV. Conclusions

This paper presents accurate EM models of passive chip-to-chip interconnections and active PD chips in the millimeter-wave frequency range. These models provide reliable tools for designing and optimizing high speed packaging and interconnections. It is shown that the mode mismatch effect is identified as the dominant loss mechanism in the packaging structure in high frequency range. A PD module with approximately 100 GHz bandwidth is developed by using wire-bonding technology with thick CPW for avoiding high mode conversion loss, which is caused by mode mismatch effect.

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